

# Thermomechanical Cleave of Polycrystalline CdTe Solar Cells and its Applications: A Review

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One of the primary research challenges for cadmium telluride (CdTe) solar cells is addressing its open-circuit voltage ( $V_{OC}$ ) deficit. While theoretical studies and single crystal work show  $V_{OC} > 1$  V is possible, devices remain stubbornly low at  $\approx 800$ – $900$  mV. As absorber opto-electronic properties (e.g., hole density, carrier lifetime) are improved, device modeling suggests that interfaces become limiting. Because CdTe-based devices are typically grown in the superstrate configuration, the back interface is relatively accessible for manipulation and study, while the front interface (i.e., the heterojunction region) is buried under microns of material and inaccessible. NREL has developed a novel technique to thermomechanically cleave polycrystalline CdTe device stacks directly at the front interface, enabling characterization and controlled manipulation of this important region. Herein, recent work, primarily from NREL, will be reviewed, including considerations for achieving successful delamination; key scientific discoveries about the front interface that have been enabled by this technique; and practical applications, such as flexible, low-cost solar with high power-to-weight ratio.

possible, the best polycrystalline devices only reach  $\approx 800$ – $900$  mV. One of the major challenges to  $V_{OC}$  improvement has been how to increase absorber hole density while simultaneously maintaining high carrier lifetimes. This has led to a shift in defect chemistry from doping with Cu (historically limited to  $p = 10^{14}$  cm $^{-3}$ ) to group V elements like As, P, or Sb ( $p > 10^{16}$  cm $^{-3}$  demonstrated).<sup>[6,7]</sup> Device modeling<sup>[8–11]</sup> suggests that as absorber hole density increases and the depletion width decreases, the p–n heterojunction (i.e., front) interface limits  $V_{OC}$ . However, because CdTe solar cells are typically grown in the superstrate configuration, the front interface is commonly buried under microns of material and inaccessible. Moreover, high temperatures ( $\approx 500$ – $600$  °C) and reactive environments (e.g., Se and CdCl $_2$ ) used during device processing can substantially alter

buried interfaces after their initial formation, making it challenging to control, or even understand, their properties.


Many technologies, in PV and beyond, have made significant efforts to access buried interfaces to study and modify them. Historically, methods used to access buried interfaces such as ion milling,<sup>[12–14]</sup> mechanical polishing,<sup>[15,16]</sup> or chemical etching,<sup>[17–19]</sup> are labor intensive and can change the structure and properties of the material under study. In situ growth of ultra-thin layers, another common method for preparation of a particular interface suitable for study, can fail to replicate the actual interface of interest because of changes occurring during post-growth processing. This problem is particularly acute in the case of CdTe-based devices that exhibit segregation of chlorine and dopants<sup>[20,21]</sup> and that undergo interfacial redox reactions long after initial formation of the oxide/chalcogenide interface.<sup>[21,22]</sup> Mechanical cleaving is an effective way to access the bulk of a solid without overt perturbation of the material's properties. Especially with multinary materials where sputtering or thermal processes create highly defective layers not representative of the bulk, mechanical cleaving is the method of choice for generation of surfaces that are suitable for surface characterization.<sup>[23]</sup> Generally, cleaving preserves the atomic-scale structure of a bulk material even if the revealed surface has lower energy surface reconstructions.<sup>[14,24,25]</sup> Plan-view cleaving of thin films, although less common than traditional cleaving of single crystals or metallurgical specimens, has also been demonstrated and is often referred to as delamination or lift-off.

Typically, thin film cleaving is achieved in one of three ways (with some variations): sacrificial etching, mechanically, or thermomechanically. All three of these methods have been

## 1. Introduction

Cadmium telluride (CdTe) solar cell technology is one of the least expensive electricity generation sources in the world. CdTe accounts for 40% of the U.S. utility-scale photovoltaic (PV) market, over 5% of the world market, and has about a third of the embodied energy of Si PV, leading to a much lower environmental footprint.<sup>[1]</sup> Yet there is still much room for improvement. While CdTe device models,<sup>[2]</sup> gallium arsenide (GaAs) solar cells with similar bandgap (1.4 eV),<sup>[3]</sup> and single-crystal studies<sup>[4,5]</sup> demonstrate that open-circuit voltage ( $V_{OC}$ )  $> 1$  V should be

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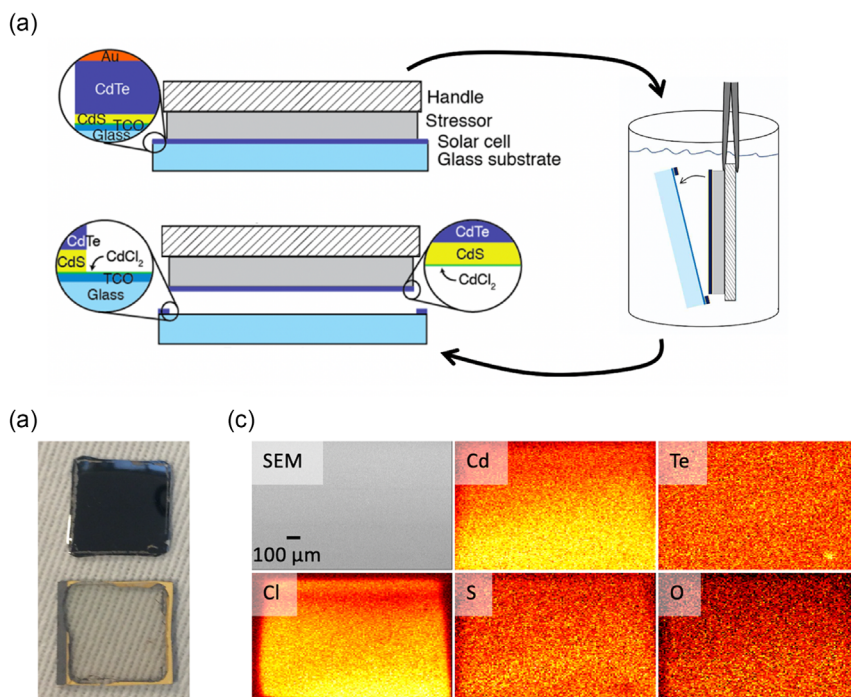
demonstrated for both single crystal (sx) and polycrystalline (px) systems, with varying degrees of success, and are discussed further in Section 2.1. Briefly, thermomechanical cleaving is the preferred method for px CdTe films and solar cells, and is the focus of this work, because sacrificial etching requires additional deposition steps and optimization of device growth,<sup>[26–28]</sup> and mechanical cleaving can result in inconsistent, laterally nonuniform surfaces.<sup>[29]</sup> In addition, sacrificial etching of materials such as MgTe is usually performed in water, raising concerns of altering the interface under study from potential interdiffusion or chemical reactions such as formation of MgO and H<sub>2</sub>.<sup>[30]</sup>

The novel thermomechanical cleave process (**Figure 1**) developed at NREL consists of two steps: 1) application of stressor and handle to the px CdTe film (this can mean gluing a handle,<sup>[31]</sup> such as glass or metal foil, or laminating a polymeric backsheet)<sup>[32]</sup> and 2) thermally shocking the system at low temperatures, typically by dipping in liquid nitrogen (LN<sub>2</sub>). This causes the stressor to quickly contract and cleave the film stack at the oxide/nonoxide interface (e.g., SnO<sub>2</sub>/CdS,<sup>[20]</sup> SnO<sub>2</sub>/CdSe<sub>x</sub>Te<sub>1–x</sub>,<sup>[33]</sup> or MgZnO/CdSe<sub>x</sub>Te<sub>1–x</sub>),<sup>[34]</sup> producing clean and atomically abrupt surfaces which are ideal for diverse surface analysis techniques. The delamination interface is largely determined by the weakest interface, which can be varied to some extent, as discussed in Section 2. In addition, the front contact layers that were removed during delamination (e.g., SnO<sub>2</sub>, MgZnO) can be reconstructed on the cleaved absorber, enabling high-efficiency substrate devices.<sup>[34,35]</sup> By delaminating with lightweight, flexible materials, CdTe devices with high specific power (power-to-weight ratio) can be also achieved while maintaining low-costs, high-throughput processing, and material quality associated with high-temperature growth.

The first section of this review will examine lessons learned regarding the mechanics of thermomechanical delamination and considerations for its successful application. Next, key scientific discoveries about the front interface that have been enabled using the cleave technique will be discussed. This includes the accumulation of two-dimensional (2D) CdCl<sub>2</sub>,<sup>[20]</sup> which appears to passivate the front interface<sup>[34]</sup>; SnO<sub>2</sub>-catalyzed oxidation of chalcogenides<sup>[22]</sup> and group V elements,<sup>[21]</sup> which may help passivate and limit dopant activation, respectively; and the evolution of various emitters (e.g., CdS,<sup>[17]</sup> CdSe,<sup>[33]</sup> MgZnO).<sup>[36]</sup> Finally, applications of the cleave technique, such as high-efficiency substrate CdTe devices, large-area delamination, and delamination using lightweight, flexible materials, will be discussed along with future outlook and proposed improvements that can be made to the technique.

## 2. Achieving Successful Delamination

This section will first give a brief background of the three approaches to delamination (sacrificial etching, mechanical, and thermomechanical). Next, key parameters that can be tuned to affect delamination quality (i.e., area delaminated, yield/completeness, film cracking), rate, and target interface will be discussed. For clarity, parameters are broken into two categories: those which can be varied after (Section 2.2) and during (Section 2.3) fabrication of the film stack. In general, it is preferred to use fabrication conditions that maximize device performance and independently control the delamination process. Thus, the objective of Section 2.2 is to highlight parameters that can be tuned to control delamination, where examples of successful stressor/handle



**Figure 1.** a) Schematic of thermomechanical cleave process showing CdS/CdTe device stack. Adapted with permission.<sup>[32]</sup> Copyright 2018, American Chemical Society. b) Image of cleaved device stack  $\approx 1$  cm<sup>2</sup>. c) Auger micrographs of CdS side of cleave showing uniform, smooth surface. Reproduced with permission.<sup>[20]</sup> Copyright 2017, American Chemical Society.

combinations and considerations on maintaining interface quality after delamination are given, while Section 2.3 discusses device fabrication choices that influence delamination.

## 2.1. Background on Delamination Techniques

Plan-view cleave techniques developed decades ago for epitaxially grown single crystals were primarily viewed as a means of re-using expensive growth substrates.<sup>[37–39]</sup> The sacrificial etch approach, also called “epitaxial lift-off” (ELO) for single crystals,<sup>[30,37,38,40–42]</sup> involves the deposition of a sacrificial layer (e.g., AlAs) between the growth substrate and film stack, which is then preferentially etched to release the stack. While this technique can generate devices with particularly high power densities,<sup>[43]</sup> exceedingly slow etch rates, use of chemically reactive etchants (e.g., HF), and required changes to growth (i.e., additional steps, reoptimization of layers) make this approach non-ideal. For polycrystalline materials, the sacrificial etch approach has been demonstrated using NaCl as the sacrificial layer for CdTe<sup>[26,27]</sup> and CuIn<sub>x</sub>Ga<sub>1-x</sub>Se<sub>2</sub> (CIGS)<sup>[44]</sup> solar cells. In this case, the goal was to fabricate lightweight, flexible devices so a polyimide carrier layer was inserted between the NaCl and device stack which still left the buried interfaces inaccessible. Polycrystalline CdS/CdTe films have also been delaminated from Si wafers using a water-assisted method,<sup>[45]</sup> in which case the interface could be studied. However, it is likely that the interface was altered during this process, e.g., through removal of the water-soluble CdCl<sub>2</sub> layer that was likely accumulated there<sup>[20]</sup> and has been shown to passivate that interface.<sup>[34]</sup> This is discussed further in Sections 2.3 and 3.

Mechanical cleaving, in contrast, eliminates the need for a sacrificial layer but can result in cracked, inconsistent films if not done carefully. In this method, the film stack is typically grown under standard conditions and a carefully chosen stressor and handle are applied to the film and pulled in tension. In the case of epitaxially grown single crystals, this method is often called “controlled spalling”<sup>[39,46]</sup> but can also be referred to as “epitaxial lift-off.”<sup>[47]</sup> In many cases, a crack is carefully initiated such that it will propagate along a preferred crystallographic plane parallel to the surface when pulled in tension. For polycrystalline materials, CIGS has enjoyed the most success being mechanically cleaved.<sup>[48–52]</sup> In this case, cleavage typically occurs at the absorber/back contact interface where MoSe<sub>2</sub>, a van der Waals (vdW) material, has inadvertently formed during processing.<sup>[53]</sup> Delamination of CIGS has allowed characterization of buried interfaces and in some cases reconstruction into bifacial devices.<sup>[50,52]</sup> Purely mechanical delamination of polycrystalline CdTe devices grown under standard conditions has not been as successful, where delamination can be laterally nonuniform,<sup>[29]</sup> occurring between the interdiffused CdS and CdTe.<sup>[54]</sup> However, this may be due to the simple fact that significant efforts were not made to optimize stressor and handle materials and/or applied tensile force.

For thermomechanical delamination, a stressor and handle are applied to a film stack grown under standard conditions and a negative temperature gradient is applied, causing the stressor to contract until spontaneous cleavage occurs. For sx material (e.g., Si,<sup>[55,56]</sup> III-Vs,<sup>[57]</sup> CdTe),<sup>[58]</sup> it is common to

initiate a crack prior to the final anneal step such that delamination will occur during the cooldown. Other studies have thermomechanically cleaved sx films without the preinitiated crack, by applying a much larger thermal strain, e.g., by dipping in LN<sub>2</sub>.<sup>[59,60]</sup> In this case, the cleave depth is determined by the stressor properties relative to the crystal. For polycrystalline material, including CIGS,<sup>[32]</sup> perovskites,<sup>[61]</sup> and CdTe,<sup>[20,32]</sup> the thermomechanical cleave technique has proven effective at exposing buried interfaces, largely due to accumulation of mechanically weak vdW layers at buried interfaces, as discussed in Sections 2.3 and 3. However, some consideration must go into choice of stressor and handle as well several other processing parameters, which will now be discussed.

## 2.2. Postfabrication Parameters to Control Delamination

Most film stacks, regardless of processing, can be successfully cleaved through appropriate choice of the stressor (typically an epoxy or polymer) and handle materials. A few common stressor/handle combinations, important material properties of the stressor, and key attributes/applications are listed in **Table 1**. The two stressor properties with the largest impact are the coefficient of thermal expansion (CTE) and elastic modulus ( $E$ ).<sup>[32]</sup> The CTE of the stressor must be large relative to the film stack, but not so large that delamination occurs prematurely, e.g., during cooldown from a heated cure. Stressors with CTE approximately one order of magnitude higher than the film have generally worked well (see Table 1). CTE cannot be considered alone though, as the stressor must also have a sufficiently high  $E$  (i.e., be stiff enough) to transfer, rather than dissipate, thermal strain energy to aid in crack propagation.  $E$  of  $\approx 100$ – $3500$  MPa has worked previously, where the lower range is useful for flexible applications<sup>[32]</sup> and the higher range generates a rigid platform for surface analysis.<sup>[20]</sup> The thickness of the stressor and handle can also play a role, particularly when CTE and  $E$  of the stressor are relatively low (e.g., for lightweight, flexible applications). For a more thorough discussion on parameters affecting thermomechanical delamination and their effect, the interested reader is directed to the theoretical framework developed by McGott et al.<sup>[32]</sup>

For applications that do not require an electrically conductive backing, Hysol 1C epoxy is commonly used as the stressor with a glass microscope slide as handle. This UHV-compatible epoxy typically provides reliable cleaves with no additional heating (Hysol 1C is cured at room temperature) and a rigid platform for applications like surface passivation, reconstruction of front contact layers, and surface analysis where charge build up is not a major concern (e.g., secondary ion mass spectroscopy [SIMS]). In cases where the film is difficult to delaminate, Hysol 1C epoxy can be paired with a heavier handle with larger CTE that can provide more tensile strain, e.g., a thin brass plate. For applications that require electrical contacting and UHV compatibility (e.g., X-ray photoelectron spectroscopy [XPS]), Epo-tek H20E silver-filled epoxy is commonly used as the stressor with 0.004” aluminum shim-stock as handle. This epoxy does require a low-temperature heated cure ( $\approx 65$ – $70$  °C for  $\approx 12$  h). Thin shim stock is beneficial because it can easily be trimmed to size for sample holders with scissors. Alternatively, a rigid, heavier handle

**Table 1.** Successful stressor/handle combinations for polycrystalline CdTe delamination with key attributes highlighted. Important material properties for stressors given.

Stressor	CTE [ppm C <sup>-1</sup> ]	E [MPa]	h [mm]	Handle	Key attributes
Hysol 1C epoxy <sup>[125]</sup>	63	≈3500	≈2	Glass	Most common, rigid, cured at room temperature overnight, UHV compatible
Hysol 1C epoxy <sup>[125]</sup>	63	≈3500	≈2	Brass	Same as above, brass handle used for difficult-to-delaminate samples
Epo-tek H20E Ag-filled epoxy <sup>[126]</sup>	31	≈5600	≈1	Al shim	Electrically conductive, cured at ≈70 °C overnight, UHV compatible
EVA <sup>[127,128]</sup>	100–200	150	0.1	PET	Flexible, relatively lightweight, laminated at ≈150 °C for ≈10 min, EVA must be low VA%

may be beneficial to produce flatter, uniformly thick epoxy with good coplanarity with the sample holder (e.g., as is important for characterization techniques like electron backscatter diffraction [EBSD]).

The most consistent stressor/handle combination for flexible applications has been a “KPE” multilayer laminate consisting of Kynar polyvinylidene fluoride (≈30 μm), polyethylene terephthalate (PET ≈130 μm), and polyethylene-co-vinyl acetate (EVA ≈150 μm).<sup>[62]</sup> This multilayer laminate is typical of the polymeric backsheets used commercially in silicon PV modules to prevent moisture ingress. To be used successfully as a stressor, it is important that the EVA has low vinyl-acetate content (VA%), which makes it relatively stiff compared to standard EVA used as a stand-alone encapsulant. In commercial backsheets, this low VA% EVA acts as a transition layer between the stiff PET handle and much thicker, soft EVA in contact with solar cells. It is also noted that while KPE is relatively lightweight and flexible, there is significant room for improvement. In addition, EVA requires a heated cure (lamination), which may not be ideal. A disadvantage of all stressors discussed here is their relatively low thermal tolerance (150–200 °C), which limits treatments and/or depositions that can be done on cleaved surfaces. This and other suggested improvements to the delamination process are discussed in Section 4.

Past the choice of stressor and handle materials, the postfabrication processing condition with the most influence on delamination is applied thermal strain, specifically  $\cdot T$  [i.e., cure temperature ( $T_{\text{cure}}$ ) – delamination temperature ( $T_{\text{delam}}$ )] and quench rate.  $T_{\text{cure}}$  is an important consideration if the epoxy or polymer requires elevated temperatures, where more complete, cleaner delamination can result from higher  $T_{\text{cure}}$ .<sup>[32]</sup> However, some stressors may generate too much thermal strain when cured at high temperatures and cause delamination while cooling to room temperature if not carefully controlled. This was found to be the case for an epoxy that was tested briefly, Epo-tek 353ND, for its high thermal tolerance. On the opposite end,  $T_{\text{delam}}$  has been found to affect delamination rate, where lower  $T_{\text{delam}}$  produces significantly faster delamination.<sup>[32]</sup> For example, a 1 × 1 cm area dipped in LN<sub>2</sub> ( $T_{\text{delam}} = -200$  °C) delaminates in 1–2 s, while the same area dipped in a bath of  $T_{\text{delam}} = -30$  °C took 1–2 min to fully delaminate. The ability to control delamination rate through  $T_{\text{delam}}$  should be useful in process control for commercial applications and means that LN<sub>2</sub> would not need to be introduced to manufacturing lines. In addition, large-area delamination necessitates a relatively high  $T_{\text{delam}}$  to reduce thermal strain, as discussed in Section 4.3.

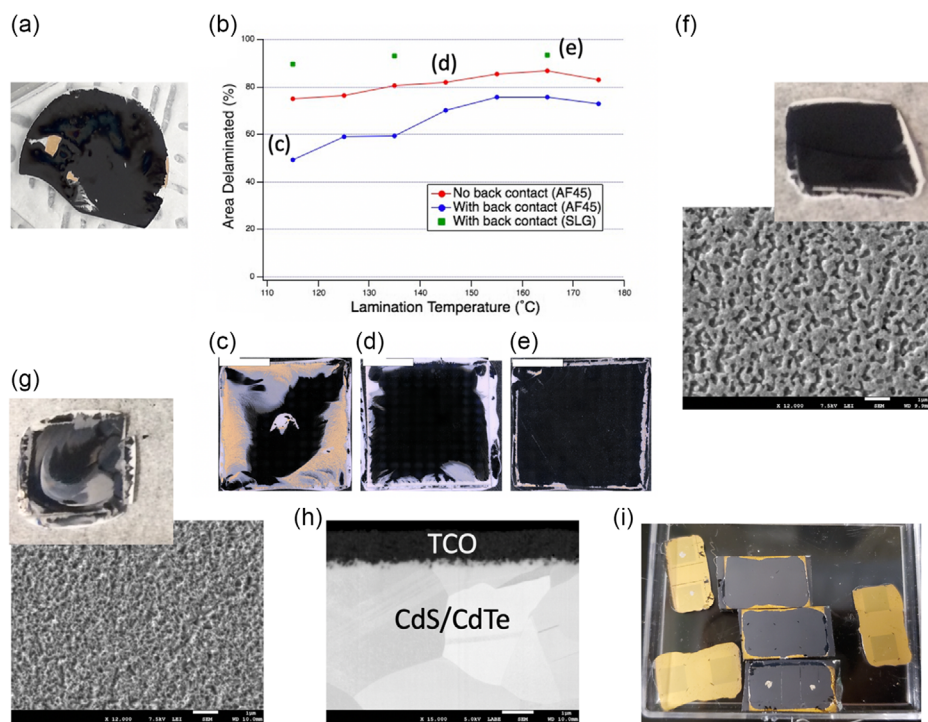
For many applications, it is important to maintain interface quality by cleaving in an inert ambient, e.g., in a LN<sub>2</sub> bath inside

of a N<sub>2</sub>- or Ar-filled glove box. If the sample is cleaved in air, oxidation from either O<sub>2</sub>, CO<sub>2</sub>, or water will change oxidation states and other aspects of the exposed materials that might be of interest. In addition, water-soluble CdCl<sub>2</sub> can be moved around on the cleaved surface and accumulate into rings (Figure 2a) as moisture from the air condenses onto the surface and evaporates as the sample warms to room temperature. After cleaving, the sample should be extracted from the LN<sub>2</sub> bath into a stream of dry N<sub>2</sub> until room temperature is reached. Depending on the application, it may also be important to transfer the sample in an inert ambient (e.g., KF nipple, lens tube, or commercial sample transfer device) as oxidation and/or removal of the CdCl<sub>2</sub> monolayer which remains on the cleaved surface may reduce carrier lifetime and  $V_{\text{OC}}$ .<sup>[34]</sup> Using these precautions, it is believed the surfaces exposed from cleaving the interface are well-preserved and chemically representative of the original front interface in the superstrate configuration. Strain in the film will certainly change however, e.g., through the release of the constraining glass substrate, and it is possible that new defects are generated, primarily at locations of incomplete cleavage.

### 2.3. Fabrication Conditions Influencing Delamination

The most important fabrication conditions that influence delamination (quality, target interface) are the chlorine treatment, architecture of film stack and material properties of the various layers, and roughness of the substrate and back surface. It is well known in CdTe that more aggressive chlorine (e.g., CdCl<sub>2</sub>) treatments can result in unwanted delamination during processing.<sup>[63]</sup> Using the thermomechanical cleave technique, Perkins et al. showed that one result of the CdCl<sub>2</sub> anneal is an accumulation of CdCl<sub>2</sub> at the SnO<sub>2</sub>/CdS interface in CdS/CdTe devices<sup>[20]</sup> and at the oxide/nonoxide interface more generally (e.g., SnO<sub>2</sub>/CdSe<sub>x</sub>Te<sub>1-x</sub>,<sup>[33]</sup> MgZnO/CdSe<sub>x</sub>Te<sub>1-x</sub>,<sup>[34]</sup> or Al<sub>2</sub>O<sub>3</sub>/CdSe<sub>x</sub>Te<sub>1-x</sub>).<sup>[64]</sup> As highlighted by Perkins et al., CdCl<sub>2</sub> is a layered 2D material with only weak vdW bonding between planes.<sup>[65,66]</sup> This creates an easy-to-cleave interface, allowing for extremely clean delamination over large areas. The importance of low-dimensional materials in px PV devices is discussed further in Section 3; of note, here is the implication that other low-dimensional materials (e.g., graphene, C60) may be intentionally inserted to cleave at interfaces of interest. This has been demonstrated in epitaxially grown material (e.g., Ge, GaAs, CdTe) using ultrathin layers of graphene<sup>[67,68]</sup> or by growing on layered substrates such as mica.<sup>[28,69,70]</sup> In this case, it is important that the low-dimensional material be stable to subsequent processing. In CdTe, this may be a useful way to cleave





**Figure 2.** a) Image of cleaved film with  $\text{CdCl}_2$  condensed on surface after delamination in air. b) Plot of percent area delaminated as a function of lamination temperature showing effect of film stack architecture where blue (worst delamination yield, example of delaminated film shown in (c)) indicates a stack with ductile gold back contact and CTE-matched glass substrate (AF45), red (example of delaminated film shown in (d)) indicates a stack with CTE-matched substrate but no gold back contact resulting in better delamination, and green (example shown in (e)) indicates a stack on a substrate with higher CTE mismatch (SLG) and gold back contact; b–e) representative images of delamination yield, with black representing clean lift-off. Scale bars are 5 mm. Reproduced with permission.<sup>[32]</sup> Copyright 2018, American Chemical Society. Image and plan-view SEM of film delaminated from f) relatively smooth TCO, leading to clean delamination and g) TEC12D which has a fine-scale, needle-like roughness (seen in (h) and SEM) that improves film adhesion and leads to worse delamination; h) SEM backscattered cross-section of as-grown CdS/CdTe device on TEC12D showing fine-scale roughness at TCO/CdS interface. Scale bars for (f–h) are 1  $\mu\text{m}$ ; i) delamination at CdTe/Au interface for relatively smooth MOCVD-grown CdTe.

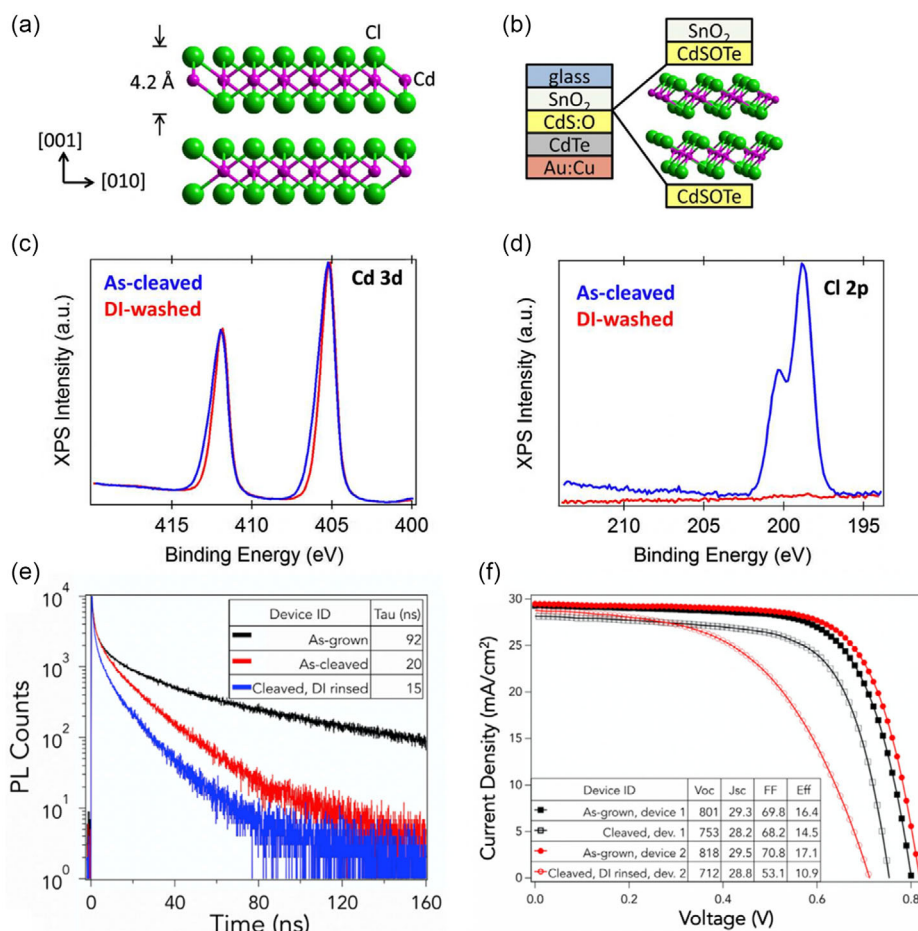
between oxide/oxide interfaces (e.g., glass/TCO to release the entire device stack) where  $\text{CdCl}_2$  does not permeate.

While  $\text{CdCl}_2$  accumulation greatly facilitates delamination, it is important to note that delamination can occur without  $\text{CdCl}_2$  treatment.<sup>[22]</sup> In our lab, we have found delamination of  $\text{CdCl}_2$ -free devices to generally be more difficult and result in surfaces with worse lateral uniformity. Other factors like stressor/handle choice and film stack architecture become more important in  $\text{CdCl}_2$ -free structures. In particular, the growth substrate can have significant influence over delamination quality. For example, a glass substrate with large CTE mismatch with CdTe will produce cleaner delamination than one with smaller CTE mismatch (e.g., soda-lime glass (SLG) with a CTE of  $\approx 8\text{--}9 \times 10^{-6} \text{ K}^{-1}$  versus AF45 with a CTE of  $4.5 \times 10^{-6} \text{ K}^{-1}$  compared to CdTe with a CTE of  $4.9 \times 10^{-6} \text{ K}^{-1}$ ,<sup>[71]</sup> Figure 2b–e).<sup>[32]</sup> The surface roughness of the substrate also plays a critical role. In particular, it has been found that commonly used TEC glass has a very fine-scale surface roughness that can make it more difficult to delaminate (Figure 2f–h), which is a good thing for standard superstrate devices and may facilitate more aggressive  $\text{CdCl}_2$  treatments. In this case, the stressor and handle must be carefully chosen to apply adequate force, particularly if delaminating over large areas. Hysol 1C epoxy and a thin brass plate have been found to work best for difficult-to-cleave samples.

If a different interface in the stack is particularly smooth, e.g., CdTe/Au interface for smooth MOCVD-grown CdTe (Figure 2i), this may create a particularly weak interface, and it can be challenging to achieve delamination elsewhere in the stack. In this case, it may be important to roughen the surface or insert an adhesion promoter to improve interface toughness. Alternatively, a smooth CdTe/back contact interface may be an ideal way to target, cleave, and study the back interface. Finally, the choice of back contact material can have a significant impact on delamination. If a metal or carbon paste is used,<sup>[72]</sup> the bond to the CdTe film tends to be very weak and delamination of the stack will not occur unless the back contact paste is first removed (e.g., with a solvent). Gold, another commonly used back contact material, is ductile and can absorb energy from the stressor that would have otherwise gone to crack propagation, resulting in worse delamination (Figure 2b–e).<sup>[32]</sup> In some cases, aqueous potassium cyanide (KCN) has been used in our lab to selectively remove gold back contacts prior to mounting samples for cleaving.<sup>[73]</sup>

### 3. Science of Buried Interfaces in CdTe

This section will summarize important scientific discoveries made about the front interface using the cleave technique.



**Figure 3.** a) Two-dimensional structure of CdCl<sub>2</sub>. b) Schematic of CdS/CdTe device structure showing location of CdCl<sub>2</sub> within stack; XPS spectra showing the effect of waster washing on c) Cd 3d line-shape and d) Cl 2p intensity. Reproduced with permission.<sup>[20]</sup> Copyright 2017, American Chemical Society. e) TRPL and f) JV curves showing effect of CdCl<sub>2</sub> removal with DI water rinse. Reproduced with permission.<sup>[34]</sup> Copyright 2021, Elsevier.

Because the front interface is directly exposed after cleavage, careful surface analysis can be done without the need for potentially harmful methods used to access buried interfaces (e.g., ion milling, mechanical polishing, chemical etching), enabling discoveries that would have been nearly impossible otherwise. For example, in an XPS study by Perkins et al., a sub-nanometer-thick layer of CdCl<sub>2</sub> was found at the front interface (Figure 3a–d).<sup>[20]</sup> In that study, superstrate CdS/CdTe devices were cleaved at the SnO<sub>2</sub>/CdS interface, and a high chlorine concentration was found on either side of the cleave (Figure 1c). Using angle-resolved XPS, the thickness of these chlorine-rich surface layers was each found to approximately match one molecular layer of Cl–Cd–Cl. Rinsing the cleaved surfaces in water showed that the chlorine was bound in a water-soluble, cadmium-containing compound (Figure 3c,d). Paired with measurement of the Cd 3d modified Auger parameter and due to the exceedingly uniform cleaves over large areas, it was concluded that the compound was CdCl<sub>2</sub>—a 2D layered material with only weak vdW bonding between planes.<sup>[74]</sup> Later studies (and unpublished work) on other device architectures including SnO<sub>2</sub>/CdSe<sub>x</sub>Te<sub>1-x</sub> and MZO/CdSe<sub>x</sub>Te<sub>1-x</sub> show this accumulation layer occurs at the oxide/nonoxide interface regardless of dopant (undoped, Cu, and As).<sup>[21,22,75]</sup>

In a follow-up study, this 2D CdCl<sub>2</sub> layer was found to passivate the front interface and improve V<sub>OC</sub> (Figure 3e,f).<sup>[34]</sup> This agrees with recent theoretical work showing how 2D CdCl<sub>2</sub> can create a defect-free transition between the rutile SnO<sub>2</sub> and zincblende CdTe.<sup>[76]</sup> Identification of similar 2D surface layers in other leading polycrystalline thin-film PV technologies (CIGS,<sup>[77–79]</sup> perovskites),<sup>[80–82]</sup> led to the hypothesis that natural surface passivation may have been an unrecognized key to each technology’s success and hints at how surface passivation may be improved. The interested reader is direct to Ref.[34] for a more detailed discussion. As pointed out by Perkins et al.,<sup>[20]</sup> understanding the 2D nature of CdCl<sub>2</sub> may help explain why MgCl<sub>2</sub>, which has the same 2D structure as CdCl<sub>2</sub>, is the only other chlorine-containing compound to show similar improvements to device performance.<sup>[83]</sup> However, both of these compounds are water soluble, so their accumulation at buried interfaces may present a concern for module stability. It is therefore important to decouple the beneficial properties from the adverse to incorporate better alternatives.

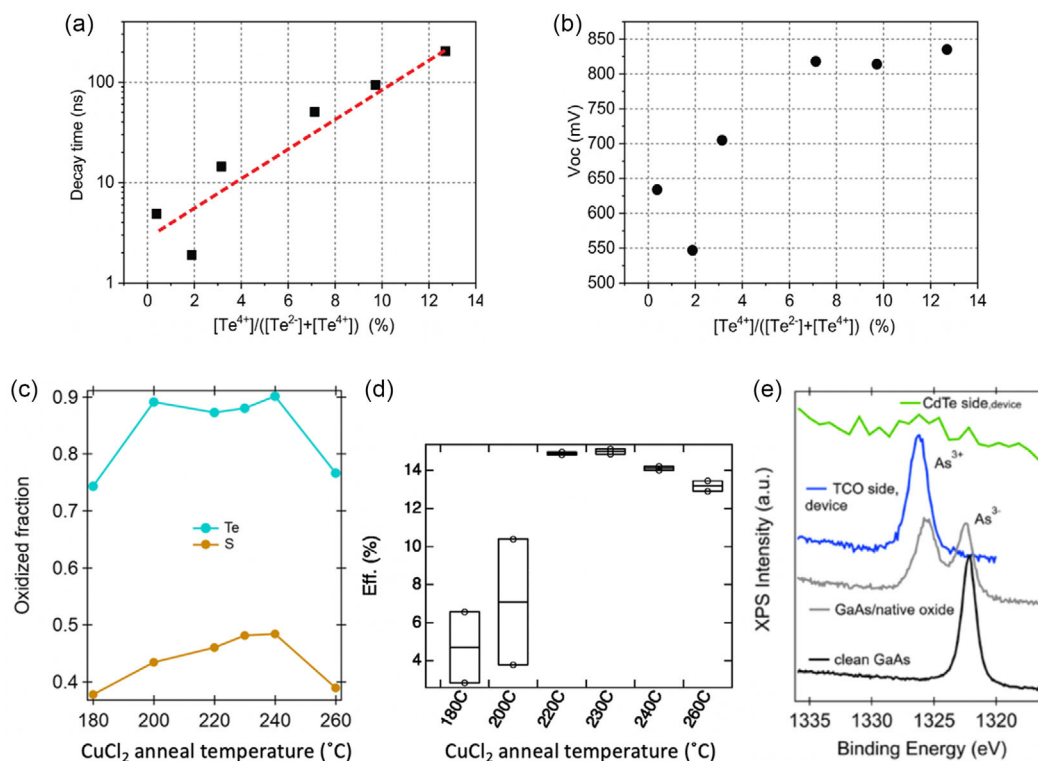
Thermomechanical cleaving has also been instrumental in understanding the evolution of the CdTe device stack, primarily with regard to the emitter, during processing. In cleaved CdS/

CdTe devices, Meysing et al. used glancing angle X-ray diffraction (XRD) to show that CdS recrystallizes from an amorphous structure in the as-deposited state to a hexagonal phase after processing.<sup>[84]</sup> The smooth surface produced from cleaving is also particularly conducive to ion beam depth profiling techniques as it avoids the back surface roughness, sputter induced roughening that increases with time, thereby enabling better depth resolution. For CdS/CdTe devices, Meysing et al.<sup>[17]</sup> used time-of-flight SIMS (ToF-SIMS) profiling to show a complete interdiffusion of CdS and CdTe, and Cu diffusion into the CdS, which they highlighted could be detrimental to performance and contribute to degradation.<sup>[85]</sup> Further, it was found that the interdiffusion between the CdS and CdTe resulted in the same postfabrication bandgap ( $\approx 2.2$  eV) at the front interface regardless of the as-deposited CdS:O bandgap,<sup>[17]</sup> indicating that previous work which found an optimal bandgap (e.g., 2.8 eV) for this as-deposited layer might have been related to controlling the rate/depth of sulfur interdiffusion. For CdSe/CdTe devices, Oklobia et al. used SIMS profiling to show complete interdiffusion of CdSe and CdTe, ending with a final composition of CdSe<sub>0.2</sub>Te<sub>0.8</sub> at the front.<sup>[33]</sup> Because this concentration is too low to make the CdSe<sub>x</sub>Te<sub>1-x</sub> n-type,<sup>[86,87]</sup> they ruled that out as a cause for parasitic absorption in CdSe/CdTe devices.

In the case of MgZnO/CdSe<sub>x</sub>Te<sub>1-x</sub> devices, no interdiffusion of the MgZnO and CdSe<sub>x</sub>Te<sub>1-x</sub> has been observed,<sup>[88,89]</sup> but the MgZnO deposition conditions do appear to affect its stability. Namely, when MgZnO is deposited via reactive sputtering using

Mg and Zn targets in a high-oxygen ambient, MgZnO was found to be stable to device processing.<sup>[36,89]</sup> When the MgZnO was sputtered from hot pressed mixed powder (MgO and ZnO) targets in a low-oxygen ambient, however, Mg concentration, and therefore MgZnO bandgap, was found to decrease after processing and/or annealing.<sup>[88]</sup> In addition, there was evidence for CdSe<sub>x</sub>Te<sub>1-x</sub> oxidation from the MgZnO, which was not observed in MgZnO/CdTe devices.<sup>[89]</sup> It was proposed that Se vacancies could create a deficiency of group VI elements at the MgZnO/CdSe<sub>x</sub>Te<sub>1-x</sub> interface and act as a driving force for oxygen diffusion into the CdSe<sub>x</sub>Te<sub>1-x</sub> layer.

Chalcogenide (Se, Te) oxidation has also been observed when CdSe<sub>x</sub>Te<sub>1-x</sub> is interfaced with other oxides, such as SnO<sub>2</sub><sup>[21,22,75]</sup> and Al<sub>2</sub>O<sub>3</sub>.<sup>[64,90]</sup> The extent of chalcogenide oxidation has also been shown to correlate with improved passivation and  $V_{OC}$  (Figure 4a,b). Amarasinghe et al. proposed that this may be due to the fact that Cd–O dangling bonds are more ionic than Cd–Te dangling bonds, shifting the defect state closer to the band edge<sup>[90]</sup>; they note that a similar effect occurs with zinc substitution of Cd.<sup>[91]</sup> Surprisingly, Perkins et al. have also shown that the extent of oxidation at the front can be influenced by low-temperature ( $\approx 200$  °C) back contact processing (Figure 4c).<sup>[22]</sup> Trends in device efficiency seemed to closely follow trends in fraction of oxidized chalcogenides (Figure 4d). As absorber hole density improves and CdTe devices become more sensitive to front interface recombination, this type of understanding and ability to manipulate the oxidation state at the front interface will likely become increasingly important.



**Figure 4.** a) TRPL decay time and b)  $V_{OC}$  as a function of fraction of oxidized Te ( $Te^{4+}$  measured via XPS). Reproduced with permission.<sup>[75]</sup> Copyright 2021, Wiley. c) Fraction of oxidized Te and S and d) device efficiency as a function of back-contact  $CuCl_2$  anneal temperature for Cu-doped devices. Reproduced with permission.<sup>[22]</sup> Copyright 2019, American Chemical Society. e) XPS spectra of cleaved group V doped devices and reference materials. Reproduced with permission.<sup>[21]</sup> Copyright 2019, IEEE.



In cleaved group V doped devices, ToF-SIMS<sup>[33]</sup> and XPS<sup>[20,92]</sup> have shown segregation of group V atoms at the front interface, where concentrations were  $\approx 10^{19} \text{ cm}^{-3}$  to  $> 10^{20} \text{ cm}^{-3}$ . Like chalcogenides, oxidation of group V elements appears to be promoted directly at the  $\text{SnO}_2/\text{CdSe}_x\text{Te}_{1-x}$  interface (Figure 4e).<sup>[21,92]</sup> While group V oxides are vdW materials<sup>[93,94]</sup> and may help passivate the front interface, oxidative segregation of group V dopants may distort desired doping profiles, limit dopant activation,<sup>[95,96]</sup> and/or result in a high density of trap states at the front interface leading to voltage loss.<sup>[11,97]</sup> Spatial nonuniformities in activation can also lead to potential fluctuations that lead to further voltage loss.<sup>[98]</sup> In a study by Metzger et al.,<sup>[92]</sup> PL and CL were used on cleaved group V devices to show that variation in As activation within  $\text{CdSe}_x\text{Te}_{1-x}$  grain interiors resulted in potential fluctuations of 50–100 meV, which can account for a substantial fraction of the observed voltage loss. Thus, it will be important to engineer the front interface to improve passivation while maintaining high hole density in the absorber.

## 4. Applications and Future Outlook

The first part of this section will outline ways in which the thermomechanical cleave technique can be used to help address important research challenges in CdTe. In particular, cleaved films can be used as a platform to better understand defect chemistry, band alignment, and passivation needs at the front heterojunction interface. The second portion will discuss practical applications and corresponding challenges of the cleave technique, including high-efficiency substrate devices, delamination using lightweight, flexible materials, and delamination over large areas. Future outlook and suggested improvements are noted throughout.

### 4.1. Front Interface Passivation

As highlighted in the 2020 PV technologies roadmap by Wilson et al.,<sup>[99]</sup> one of the most important research challenges currently facing CdTe is simultaneously maintaining high dopant activation in the absorber while reducing recombination at the front (heterojunction) interface. To reduce recombination there, it will be important to better understand 1) defect chemistry at the junction interface to chemically passivate it, 2) band alignment and electron density at the junction after device fabrication to passivate via field effect, and 3) new materials (e.g., tunneling layers) that can be inserted which can simultaneously passivate and extract carriers. The thermomechanical cleave technique can play a pivotal role in all three endeavors.

Examples of how the cleave technique has already been used to develop a novel chemical understanding of the front interface were discussed in Section 3. Past this, it will be important to study group V defect chemistry, particularly regarding differences between activated and un-activated states, metastable and/or compensating donor states (e.g., AX centers),<sup>[100,101]</sup> interactions with impurities like chlorine and oxygen, and spatial distribution of dopants. This is particularly important as theoretical studies show that a buildup of deep donors near the junction can be detrimental to  $V_{OC}$ , while shallow donors or a thin intrinsic layer may be beneficial.<sup>[11]</sup> In this respect, it will also be important

to understand changes in defect chemistry related to Se incorporation near the junction, as well as the interplay between Se and group V defect chemistries. Cleaved group V devices can offer a means of not only studying defect chemistry but also modifying it near the junction.

Understanding band alignment at the heterojunction in completed CdTe devices is important but has historically been very challenging to measure. Reasons for this include the aforementioned buried nature of this interface and the fact that the interface evolves drastically during postgrowth processing. Theoretically, it is known that a small positive conduction band offset (CBO) of  $\approx 0.2\text{--}0.3 \text{ eV}$  is desired to block hole transport at the interface while allowing electron flow.<sup>[9,10]</sup> Moreover, recent modeling shows that CBO can either help negate or accentuate the negative effects of charge build up at the junction in highly doped devices.<sup>[11]</sup> Many experimental methods have been developed to measure band alignment, band offset, and band bending, among which XPS is one of the most common.<sup>[102]</sup> Using this method, valence band offset (VBO) is measured via XPS, bandgap is measured via spectrometry, photoluminescence, and/or quantum efficiency, and CBO is calculated from the combination of the two. Alternatively, the conduction band minimum (CBM) can be directly measured by inverse photoemission spectroscopy (IPES). Band alignment measurements via XPS/IPES typically require three samples: 1) thick p-type junction partner, 2) thick n-type junction partner, and 3) sample with junction formed in which one uniform layer is transparently thin to photoelectrons with  $< 1 \text{ kV}$  kinetic energy ( $\leq 10 \text{ nm}$ ). An active area of research in our lab involves using thermomechanical delamination to prepare samples suitable for XPS-based band alignment measurements. Advantages of this approach include the ability to do detailed electro-optical characterization on completed devices prior to band alignment determination. In addition, XPS/IPES measurements are done on materials that have undergone all of the processing that went into devices and thus include effects of defect creation, impurity segregation, and so on.

Importantly, cleaved films also provide a platform to better understand passivation needs at the junction via direct application of passivating layers and/or chemical treatments. Chemical treatments can provide insight on advantageous stoichiometry, composition, and oxidation state at the front interface. For example, Cd-rich surfaces obtained via reducing treatments have been shown to produce higher carrier lifetimes than Te-rich surfaces,<sup>[103]</sup> but it is unclear if these are ideal conditions at the oxide/ $\text{CdSe}_x\text{Te}_{1-x}$  interface. Furthermore, the oxidation state at the front interface appears to strongly influence performance, but this may have competing effects for different chemical species (e.g., chalcogenides<sup>[22]</sup> vs group V dopants).<sup>[21,92]</sup> By performing surface treatments on high-quality cleaved films, needs for chemical passivation can be evaluated in a high-throughput manner and superstrate device growth can be informed.

This is true for the addition of passivating layers at the junction as well. In addition to high-throughput testing, the cleaved-film platform offers the distinct advantage of allowing passivating materials to be evaluated in their as-deposited state rather than being potentially transformed or degraded during CdTe device processing. This opens the possibility for materials to be tested that may not have been able to withstand standard



high-temperature device processing such as functionalized fullerenes with tunable bandgap,<sup>[104]</sup> phenyl-C60-butyric acid methyl ester (PC<sub>61</sub>BM), or ZnO-based materials.<sup>[105]</sup> Additional passivating materials of interest include low-dimensional structures,<sup>[34]</sup> bilayer designs,<sup>[106]</sup> and ultrathin or patterned insulators like Al<sub>2</sub>O<sub>3</sub>.<sup>[107]</sup> To verify that electrons are not blocked from reaching the front contact, passivated cleaved films can be reconstructed into substrate devices as described in Section 4.2. An example of cleaved films being used in this manner was demonstrated by McGott et al. to show the surprisingly large effect that removing a single monolayer of passivating CdCl<sub>2</sub> from the cleaved surface had on carrier lifetime and V<sub>OC</sub>.<sup>[34]</sup>

It is also important to note some of the advantages of cleaved films offer for characterization. As previously mentioned, the atomically abrupt surfaces produced during delamination enable higher depth resolution for sputter depth profiling techniques as it avoids the rough back surface and cumulative effects of ion beam-induced roughening. Techniques that require smooth surfaces, such as cathodoluminescence (CL), EBSD, and PL imaging, can also easily be performed without the need for polishing if films are grown on relatively smooth substrates prior to delamination. Finally, removal of the defective (often soda-lime) glass substrate means that lower irradiance can be used in techniques like PL, PL quantum yield (PLQY), and external radiative efficiency (ERE), resulting in more accurate measurements.

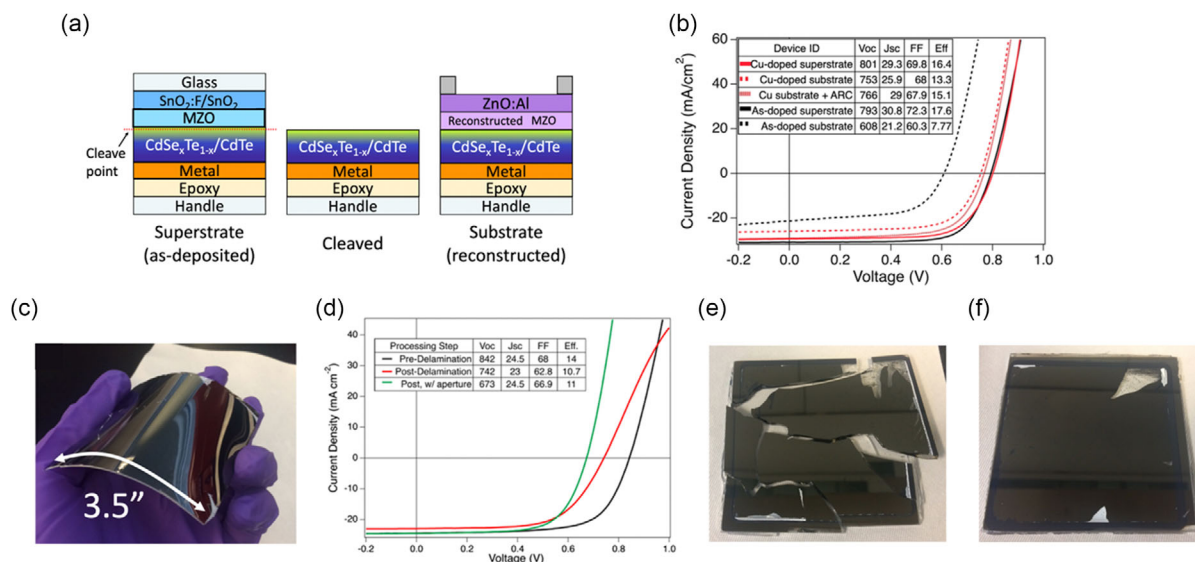
#### 4.2. High-Efficiency Substrate Devices

Relative to superstrate CdTe devices, CdTe grown in the substrate configuration has historically underperformed.<sup>[108]</sup> This is largely due to issues generating an Ohmic back contact, required reoptimization of deposition steps like the CdCl<sub>2</sub> anneal,<sup>[109]</sup> and lower growth temperatures.<sup>[110]</sup> All of these complications can be circumvented if devices are grown under

optimized conditions in the superstrate configuration, then thermomechanically cleaved, and reconstructed in the substrate configuration. Because cleavage occurs at the oxide/nonoxide interface (e.g., SnO<sub>2</sub>/CdSe<sub>x</sub>Te<sub>1-x</sub><sup>[33]</sup> or MgZnO/CdSe<sub>x</sub>Te<sub>1-x</sub>),<sup>[34]</sup> reconstruction typically involves deposition of an emitter and TCO (Figure 5a). By pairing state-of-the-art absorbers with reconstructed emitters of known properties (i.e., that are less likely to evolve during subsequent processing), device modeling can be tested more directly and high-performance substrate devices can be generated.

In fact, the highest-efficiency substrate CdTe device reported in the literature to date was generated using this method (Figure 5b).<sup>[35]</sup> In that study, a 16.4% efficient superstrate Cu-doped CdSe<sub>x</sub>Te<sub>1-x</sub> device was cleaved and reconstructed with a MgZnO/ZnO:Al front contact, producing a 15.1% substrate device (>90% efficiency retention). Interestingly, when the same MgZnO/ZnO:Al front contact was reconstructed on a cleaved As-doped CdSe<sub>x</sub>Te<sub>1-x</sub> device, the efficiency was much lower—only 7.8%, a mere 44% of its original 17.6% efficiency. Briefly, this difference was attributed to increased sensitivity to front interface quality, which may be worse in reconstructed devices due to changes in chemical state and/or sputter damage or nano-cracking, and emitter properties as a result of higher absorber hole density.<sup>[8,9,11]</sup>

This also highlights that reconstructed front contact materials are in no way optimized, particularly for group V-doped absorbers. In particular, the relatively low thermal tolerance of epoxies and polymers typically used as stressors (Section 2.2) limit the choice of emitters that can be tested. A high thermal tolerance may be particularly important for achieving high dopant activation in the emitter. For example, Ga-doped MgZnO shows promise as an n-type junction partner in group V-doped devices as it has tunable CBO (−0.2 to 0.5 eV) and electron density (≈10<sup>19</sup>–4 × 10<sup>20</sup> cm<sup>−3</sup>) but requires a 500 °C vacuum activation anneal.<sup>[111]</sup> Another consideration is the deposition ambient of



**Figure 5.** a) Schematic of reconstruction process with MgZnO (MZO)/ZnO:Al front contact. b) JV data for as-grown (superstrate) and reconstructed (substrate) Cu- and As-doped devices. Reproduced with permission.<sup>[35]</sup> Copyright 2021, American Chemical Society. c) Image of large-area flexible delaminated film and d) JV data for reconstructed flexible device. Reproduced with permission.<sup>[32]</sup> Copyright 2018, American Chemical Society. Images of large (≈3.5" sq.) glass substrates after delamination e) in LN<sub>2</sub> bath and f) LN<sub>2</sub>-cooled block. Reproduced with permission.<sup>[115]</sup> Copyright 2018, IEEE.

the reconstructed emitter or passivating material as it can alter the chemistry at the front interface. For example, reactive sputtering may oxidize the  $\text{CdSe}_x\text{Te}_{1-x}$  surface, which could provide beneficial passivation of chalcogenides on the one hand or form compensating defects that reduce  $V_{OC}$  on the other.

### 4.3. Lightweight, Flexible, and Large-Area Delamination

Stressor and handle materials used for delamination can be chosen to fit a wide variety of final applications as discussed in Section 2.2. This section discusses the limited work that has been done to achieve delamination using lightweight, flexible materials and over large areas as well as special considerations that must be made for each. Thoughts related to the manufacturability of the technique are also given.

A major benefit of the thermomechanical cleave process is the decoupling of growth conditions (e.g., high temperatures, reactive environments) from final packaging. By delaminating using lightweight polymers (Figure 5c), substrate devices with high specific power (power-to-weight ratio) can be achieved while maintaining low-costs, high-throughput processing, and material quality associated with high-temperature growth. This can enable CdTe to enter several emerging PV markets where specific power is of critical importance, such as aerospace and portable charging, which are expected to exceed gigawatt-scale cumulative potential in the next decade.<sup>[112]</sup> While there has not yet been work explicitly attempting to minimize stressor/handle weight, a demonstration of what can be achieved with little optimization was given by McGott et al. (Figure 5d).<sup>[32]</sup> In that study, a commercially available polymeric backsheet commonly used in Si modules was used to cleave a CdS/CdTe device, resulting in over an order of magnitude decrease in areal density (7830 to 350 g  $\text{m}^{-2}$ ) while maintaining 80% of the original efficiency (14% to 11%). It is noted that specific power was not given here as these devices did not include full packaging (e.g., front- and back-sheet, encapsulation, interconnects).

To optimize specific power further, weight and thickness of stressor and handle should be minimized while ensuring that enough strain energy can be generated to produce delamination. In this regard, the theoretical framework developed by McGott et al.<sup>[32]</sup> will be useful. Briefly, the minimization of stressor thickness will allow for a larger elastic modulus while maintaining flexibility. In addition, it may be important to use a material with particularly high CTE and cure at elevated temperature to produce more thermal strain. Another approach to improve specific power may be to eliminate the need for reconstruction, and therefore increase efficiency, by transferring the entire device stack to the polymer sheet. This can be done by inserting a release layer (e.g., C60 or other low-dimensional material with high thermal tolerance) at the glass/TCO interface. A release layer could also aid with delamination over particularly large areas, e.g., a full module.

Apart from generating flexible CdTe modules, large-area delamination can allow for the reuse of glass growth substrates, which are a relatively expensive component of the device stack ( $\approx 20\%$  of module cost in a frameless module).<sup>[113,114]</sup> In this case, it is particularly important to mitigate buildup of residual strain in the glass substrate, which can cause catastrophic

cracking in the glass (Figure 5e,f). The most effective way to mitigate strain buildup is to decrease  $\cdot T$  (e.g., increase bath temperature) and/or quench rate. McGott et al. showed that, depending on stressor and handle, delamination can occur up to bath temperatures of  $-30^\circ\text{C}$ , in which case the delamination rate drastically slows.<sup>[32]</sup> The ability to control delamination rate through  $T_{\text{delam}}$  should be useful in process control for commercial applications and means that  $\text{LN}_2$  does not need to be introduced to manufacturing lines.

The largest area cleaved so far has been  $3.5'' \times 3.5''$  (Figure 5c, done for both CdTe and CIGS),<sup>[32,115]</sup> which has primarily been limited by the size of available growth chambers. In this case, the sample was not dipped in  $\text{LN}_2$  but rather placed stressor/handle side down on a  $\text{LN}_2$ -cooled copper block to reduce thermal strain.<sup>[115]</sup> It was also important to use a flexible stressor/handle that can flex and apply additional torque as the delamination front slowly propagates across the substrate. To mitigate thermal strain in the glass further, a compliant layer (EVA) was laminated to the back of the glass; this layer can absorb strain energy that would otherwise be stored in the glass. Finally, the thinner the glass growth substrate is, the more it can flex in response to strain loads rather than crack.

Much like with wafer reuse for III–V PV, to reuse the glass substrate, it would also be important to fully clean any residual CdTe device layers (e.g., Figure 1b) from the surface. First, surface residue can be minimized by extending the polymer sheet to the glass edges, which was not done in the studies presented here. In a manufacturing line, this could easily be accomplished as modules and polymer sheets would have well-defined, precise dimensions. To remove any remaining surface residue, techniques that are already incorporated into manufacturing lines for end-of-life recycling can be used, such as etching with acid or vacuum blasting,<sup>[116–118]</sup> but in a much less aggressive manner. Standard CdTe module recycling thus provides a bound in terms of expense and energy use with processes including shredding/crushing the module, semiconductor removal via acid etching, liquid-solid separation, and finally precipitation of metal constituents to be sent to a third party for reclamation. Several cycles of glass reuse could significantly reduce the embodied energy and carbon of a flexible CdTe module relative to rigid glass modules where roughly a third of the embodied energy stems from its glass packaging.<sup>[1]</sup> By delaminating the device stack, lightly cleaning the substrate, and reusing it, glass reuse could be done at a fraction of the cost of standard CdTe module recycling. Furthermore, the hazards associated with accidental release of leachate<sup>[116,119]</sup> as Cd concentrations<sup>[118]</sup> in the acid would be drastically reduced per unit module area (of reused glass compared to recycled rigid module).

In manufacturing lines, CdTe solar cells are typically formed through a monolithic interconnect (MLI) process, in which device layers are deposited onto the glass substrate and divided into many smaller series interconnected cells via strategically interspersed laser scribing steps. For thermomechanically cleaved flexible modules, laser scribing steps might be delayed until after films are cleaved, having turned the samples effectively into a substrate configuration (like CIGS) and front contact layer(s) are reconstructed to finalize connections. If devices were to be delaminated with a completed front contact through the intentional insertion of a release layer under the TCO, MLI might

be performed prior to liftoff with proper engineering of release and stressor layers.

Changes to device reliability/stability are also important to consider when manufacturing flexible modules. Relative to flexible superstrate CdTe devices grown on ultra-thin Willow glass,<sup>[120,121]</sup> which show good mechanical robustness, it is expected that cleaved CdTe devices on polymer films may have better flexibility but also lower mechanical robustness due to high mismatch in CTE and elastic modulus with the polymer. However, the front sheet, which is required in modules, can be chosen such that a neutral plane is created at the device layer, reducing strain and improving stability. In addition, the cleave and reconstruction of front contact layers allow the brittle TCO, which is a known source of degradation in flexible PV,<sup>[122]</sup> to be replaced with more ductile materials, such as transparent metal grids<sup>[123]</sup> (e.g., from a scalable process such as cracked film lithography),<sup>[124]</sup> which can maintain their conductivity after many bend cycles. It is not expected that delaminated CdTe PV would face unique reliability challenges compared to other flexible polycrystalline technologies.

## 5. Summary and Conclusion

The thermomechanical cleave technique developed at NREL for polycrystalline CdTe solar cells is relatively new but has already contributed greatly to the understanding and improvement of several areas of the PV technology. Importantly, it provides a simple way to experimentally access the buried front interface (heterojunction region), allowing for detailed characterization of the structural and electro-optical properties that determine in part how the device operates. As absorber hole density increases, passivation of the front interface becomes increasingly important. The surfaces produced from cleaving are ideal for various surface analysis techniques and novel strategies for regrowth of the heterojunction, both of which have enabled a much better scientific understanding of the front interface and CdTe devices as a whole. This review has highlighted a few ways the cleave technique has already been used to do this. First was the discovery of a 2D CdCl<sub>2</sub> accumulation layer <1 nm thick at the buried oxide/nonoxide interface (typically at the p-n heterojunction), which was found to passivate the front interface and improve  $V_{OC}$ . Identification of similar 2D surface layers in other leading polycrystalline thin-film PV technologies (CIGS, perovskites) hints at a broader theme to effective surface passivation. Oxides (e.g., SnO<sub>2</sub>) have also been found to catalyze oxidation of chalcogenides and group V elements at the front interface. While the fraction of oxidized chalcogenides has been correlated with improved passivation and  $V_{OC}$ , group V oxidation may prevent dopant activation and lead to deleterious states near the junction.

Considerations on achieving successful delamination were also discussed, particularly with regard to choosing appropriate stressor/handle combinations for given applications, how to control thermal strain, and fabrication conditions that can produce undesired delamination results. This is important not only so that the technique can be applied to CdTe film stacks of varied architecture, but to different polycrystalline PV materials as well (e.g., CIGS, perovskites). Practical applications of the cleave

technique were discussed. In addition to better understanding the front interface, cleaved films offer a useful platform to directly modify the interface and evaluate the effect on device performance. Cleaved films can also be reconstructed into high-efficiency substrate devices, which can be used to directly test device modeling by pairing optimally grown absorbers with emitter of known properties. Finally, avenues to achieving high specific power and delamination over large areas were discussed. For all of these reasons, it is believed that the thermomechanical cleave technique will continue to grow in importance.

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## Conflict of Interest

The authors declare no conflict of interest.

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buried interfaces, CdTe, delamination, photovoltaics

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