Novel Hybrid Current Limiter for Grid-Forming Inverter Control During Unbalanced Faults

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Nathan Baeckeland and Gab-Su Seo

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Novel Hybrid Current Limiter for Grid-Forming Inverter Control During Unbalanced Faults

Nathan Baeckeland and Gab-Su Seo

Power Systems Engineering Center, National Renewable Energy Laboratory, Golden, CO 80401, USA
E-mails: {nathan.baeckeland, gabsu.seo}@nrel.gov

***Abstract*—Grid-forming (GFM) inverter controls have illustrated many desirable features to enable the bulk integration of renewable resources into the future power grid; however, the performance of GFM inverters during unbalanced faults remains underexplored. This paper proposes a novel current-limiting method for GFM inverters to handle unbalanced fault conditions while providing voltage support to the main grid. The proposed current limiter combines concepts of dynamic virtual-impedance and current-reference saturation limiting, all built in the stationary reference frame, to achieve improved current-limiting performance under unbalanced load/fault conditions. System-wide full-order transient simulations with multiple GFM inverters demonstrate the potential of the method and benchmark the performance against state-of-the-art current limiters. Simulation results portray improved voltage balancing performance of the proposed method compared to both current-reference saturation and virtual-impedance limiting.**

I. Introduction

Grid-forming (GFM) inverter controls are increasingly recognized as the pathway to the bulk integration of inverter-based renewables into the grid [1]. Research efforts on GFM technology have predominantly focused on primary- and secondary-control architectures that facilitate inverters to synchronize, share power, and participate in grid services, such as frequency regulation at scale [1]. The critical aspects of fault tolerance and grid-voltage support of GFM inverters—especially during unbalanced grid faults—remains underexplored [1]. One critical inverter-control element for fault tolerance is the current limiter. The design of the current limiter greatly dictates the inverter's overall fault behavior. A well-established method to limit the inverter currents during faults is the current-reference saturation limiter, which curtails the reference signals feeding into the inner-current control loop [2]. Current limiting can also be achieved through diminishing the reference signal feeding into the outer-voltage control loop through the use of a virtual impedance. Within these current-limiting categories, many different implementations have been considered [2]; however, they primarily focus on balanced faults. Strategies for current limiting under unbalanced conditions—especially for GFM inverters—are rather limited [3]–[8].

This paper proposes a novel current-limiting strategy for GFM inverters under unbalanced conditions. The contributions of this paper are twofold. First, to fully appreciate the benefits of the current-limiting method proposed in this paper, we take a fresh look at the established methods: the current-reference saturation (SatLim) and virtual-impedance (VIMP)-limiting method. By leveraging a simplified steady-state fault scenario, we present new insights into the fault behavior of current limiters of GFM inverters by investigating the inverter output voltage and current phasors under faults. Second, we outline the new limiting method. The method is benchmarked against the SatLim and VIMP strategies through extensive full-order transient simulations.

II. State-of-the-Art Current Limiters and Their Steady-State Fault Behavior

In this section, we shed light on the established current-limiting methods to gain insights into their different influences on the GFM inverter output, i.e., how the current limiter affects the output voltage and current phasors during faults. Consider the conceptual scenario illustrated in Fig. 1, where one GFM inverter is connected to an infinite bus via an inductive line. Fig. 2 illustrates the implementation of the SatLim (2b) and the VIMP (2c) methods into the control system (2a) in detail (the gain ρ is defined in Eq. (2)). Assume there is no prefault power flow over the line, which implies that the inverter terminal voltage, E, the internally generated voltage reference by the primary control block, $E^\star$, and the infinite bus voltage, V_s, are all equal ($1\,\mathrm{p.u.}$, zero angle). The line impedance is set to $j0.1\,\mathrm{p.u.}$, i.e., purely inductive. At $\mathrm{t}{=}0\,s$, we consider a voltage drop at the infinite bus of $0.5\,\mathrm{p.u.}$, and we investigate the phasor-fault-behavior of the output current and voltage of the GFM inverter. For this effort, we consider only balanced conditions for simplicity. The insights can be extrapolated to unbalanced faults. We further assume that the inner-current and outer-voltage control loops have reached a steady-state fault behavior. This translates into a zero-error feeding into these control loops. Last, we assume that the primary control bandwidth is significantly lower than the voltage and current control loops, so $E^\star$ can be assumed equal to the prefault conditions (e.g., droop control with a small $P(\delta)$ gain).

With these considerations in mind, new steady-state voltage and current phasors can be calculated during the voltage drop. (More details on how to calculate these phasors can be found in the appendix.) We repeat this calculation for a multitude of different maximum allowable output currents of the inverter, I_max, ranging from $5\,\mathrm{p.u.}$ to

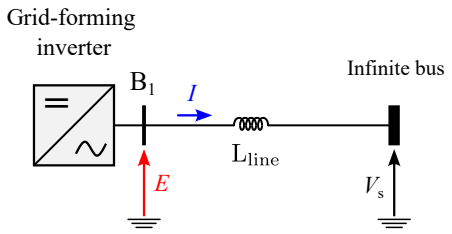

Fig. 1: Conceptual scenario with one GFM inverter connected to an infinite bus via an inductive line.

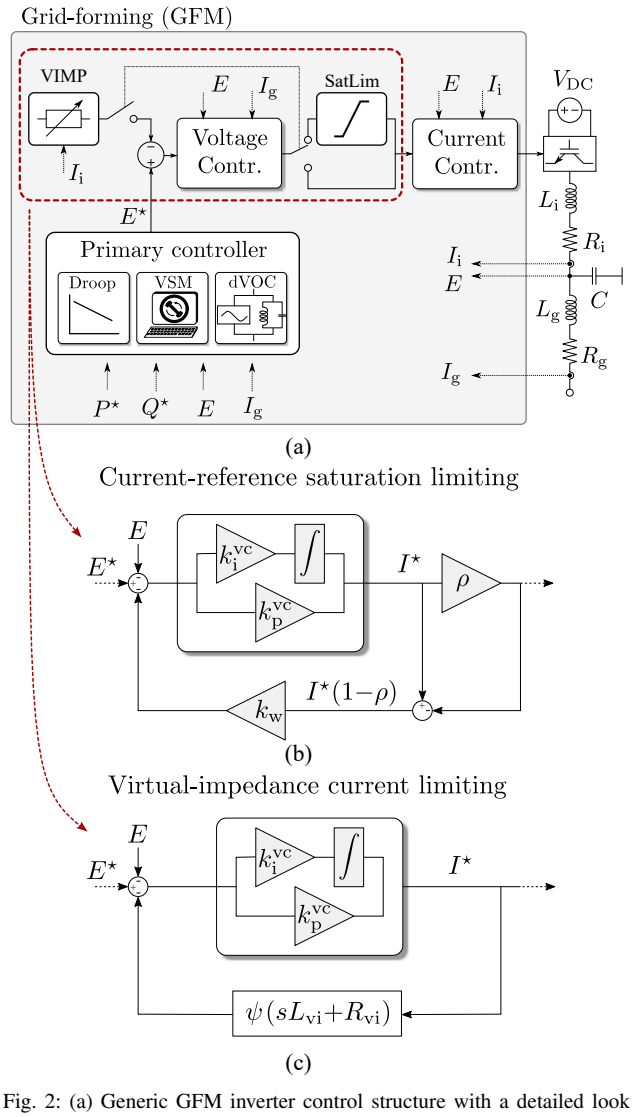

Fig. 2: (a) Generic GFM inverter control structure with a detailed look at the outer-voltage control loop with the (b) current-reference saturation limiting (SatLim) and (c) virtual impedance (VIMP) current limiting [5].

1.2 p.u.. Namely, the maximum allowable current, $I_{\max}$, dictates how severely the current limiter intervenes. The resulting inverter's output voltage and current phasors are collectively depicted in Fig. 3 for both the SatLim and the VIMP methods. (These sets of phasors do not visualize a dynamic inverter response but rather a collection of steady-state operating points under different boundary conditions and parameter set points.) Note that when $I_{\max}$ is set to 5 p.u. or higher, the SatLim does not intervene (the current does not surpass the maximum current), which results in a purely inductive output behavior of the inverter. Intuitively, this makes sense because the line is purely inductive, and

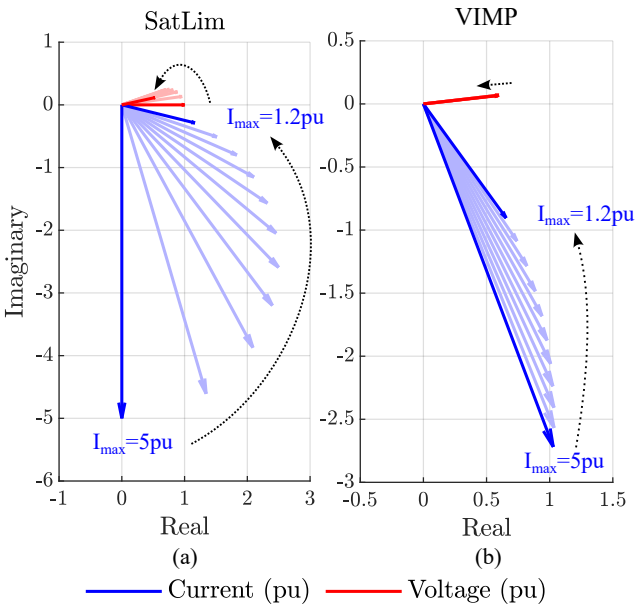

Fig. 3: Inverter output voltage (red) and current (blue) phasors of the SatLim (a) and the VIMP (b) for different values of $I_{\max}$.

$E^\star$ and V_s are in phase; however, when $I_{\max}$ decreases, the output behavior of the inverter becomes more resistive. Note that for more resistive lines, the whole set of phasors in Fig. 3a would shift in angle towards resistivity. For a common $I_{\max}$ of 1.2 p.u., the angle between the output voltage and current phasors is only 23°.

As illustrated in Fig. 3b, the inverter's behavior under VIMP limiting is clearly different. Because of the inherent nature of the VIMP, limiting occurs even for an $I_{\max}$ of 5 p.u.. (See appendix and [5] for more details.) To provide voltage support during faults in practical grids, the virtual-impedance angle should be parameterized to match the grid impedance angle [5]. Depending on whether a transmission or a distribution grid is considered, this angle can adopt more inductive or resistive values. In this exercise, we arbitrarily set the angle of the virtual impedance to 45° for illustration purposes. In Fig. 3b, we observe that for decreasing values of $I_{\max}$, the output current is nearing the set angle of the virtual impedance; however, due to the nature of VIMP limiting, it is not possible to use the full current capabilities of the inverter, e.g., the output current is calculated to be 1.11 p.u. for an $I_{\max} = 1.2$ p.u.). This conceptual scenario leads to two observations. First, the SatLim fully utilizes the overcurrent capacity of the inverter but loses control over the phasor angles. When the SatLim intervenes, the GFM inverter behaves more resistive. Second, the VIMP limiting allows for some degree of control over the output impedance angle of the inverter, but it cannot control the current amplitude. Fully utilizing the overcurrent capacity of the inverter is not possible with VIMP limiting.

III. Proposed Hybrid Current Limiter

In this section, we propose a novel current-limiting method that combines the aforementioned SatLim and VIMP limiting strategies. As such, the proposed method unites the best of both strategies —it enables the full use

of the inverter's overcurrent capacity up to $I_{\max}$ while maintaining control over the output-impedance angle of the inverter. Fig. 4 illustrates the conceptual control structure of the proposed current-limiting method. Notice that the structure is similar to the SatLim method but the anti-windup gain has been replaced by a virtual impedance.

To illustrate the current-limiting behavior of the new method, we consider the same conceptual scenario in Fig. 1 used in Section II, i.e., a voltage drop of 0.5 p.u. at the infinite bus is applied. Fig. 5 depicts the steady-state output current and voltage phasors of the GFM inverter. Fig. 5a illustrates the resulting phasors for changing values of $I_{\max}$ with the virtual impedance angle fixed to 45°. Similar to VIMP limiting, this angle should match the grid impedance angle to provide better voltage support during faults. Fig. 5b illustrates the phasors for changing values of the virtual impedance angle with $I_{\max}$ fixed to 1.2 p.u.. As shown, by choosing the angle of the anti-windup virtual impedance, one can control the angle of the inverter's output impedance without compromising the inverter's current capability.

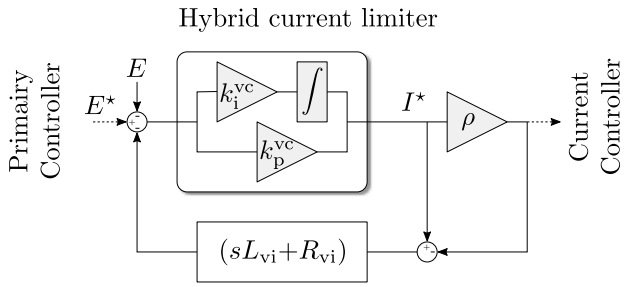

Fig. 4: Conceptual outline of the control structure of the proposed hybrid current limiter.

Extending this hybrid current-limiting strategy for unbalanced conditions yields the GFM control structure shown in Fig. 6. The control system is an extension on the work presented in [5]. The control system is constructed in the stationary reference frame for better (higher bandwidth) unbalanced signal handling. The gain, ρ, is defined by (15)–(18) in [5]. More details on the controller design can be found in [5]. The magnitude and angle of the virtual impedance in the anti-windup feedback loop of the proposed limiter are design parameters. The choice for the virtual-impedance angle, $\angle Z_{\text{vi}}$, follows the design of the VIMP explained in [5]. For the impedance magnitude, $|Z_{\text{vi}}|$, a similar design strategy as that for a regular anti-windup can be adopted; however, constructing a structural approach to tuning the virtual impedance is outside the scope of this paper and is considered for future work. An additional low-pass filter is placed in series with the virtual impedance to alleviate sensitivity to noise from the derivative action.

IV. Simulations

In this section, full-order transient simulations are presented to demonstrate the operation of the proposed method and to benchmark it against the SatLim and VIMP methods. This section contains two simulation setups: one with a single GFM inverter connected to an infinite bus through a line and one with 5 GFM inverters interconnected by a 14-bus network where a severe unbalanced fault is applied.

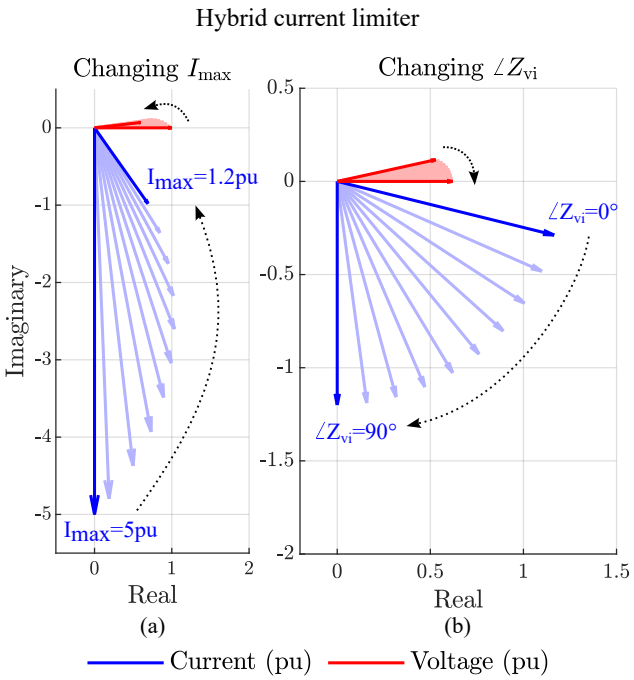

Fig. 5: Voltage (red) and current (blue) phasors (a) for changing values of $I_{\max}$, while fixing the virtual impedance angle to 45°, and (b) for changing values of virtual-impedance angle values while fixing $I_{\max}$ = 1.2p.u..

A. Single GFM Unbalanced Fault Simulations

Consider the fault scenario in Fig. 7, where a single GFM inverter is connected to a stiff grid via a transmission line (θ_ℓ = 75°). At t=0.5 s, an unbalanced line-to-line fault between phase 'b' and 'c' is applied on the transmission line. This simulation is repeated three times while iterating between the SatLim, VIMP limiter, and the proposed hybrid current limiter. For the SatLim and the VIMP GFM controls, we leverage the models from [5]. For the GFM controls with the proposed hybrid current limiter, we leverage the GFM model depicted in Fig. 6. The control parameters are summarized in Table I. The objective of this simulation is to assess the influence of different limiters on the unbalanced fault behavior of the GFM inverter at the unit level.

The results of the unbalanced fault scenario of Fig. 7 are shown in Fig. 8. For each of the three current limiters, the instantaneous phase currents and the steady-state sequence phasors during the fault are depicted. The sequence phasors are calculated over one period immediately after the transients created by the fault have died out. Fig. 8a illustrates that, with the SatLim, the unbalanced currents are limited to the maximum allowable current of $I_{\max}$ = 1.2 p.u.. The same holds true for the proposed hybrid current limiter (Fig. 8c). Limiting the phase currents up to $I_{\max}$ with VIMP limiting is not feasible, as shown in Fig. 8b, where the phase currents remain a few percentages less than $I_{\max}$. Although the decreased overcurrent capability of VIMP limiting comprises only

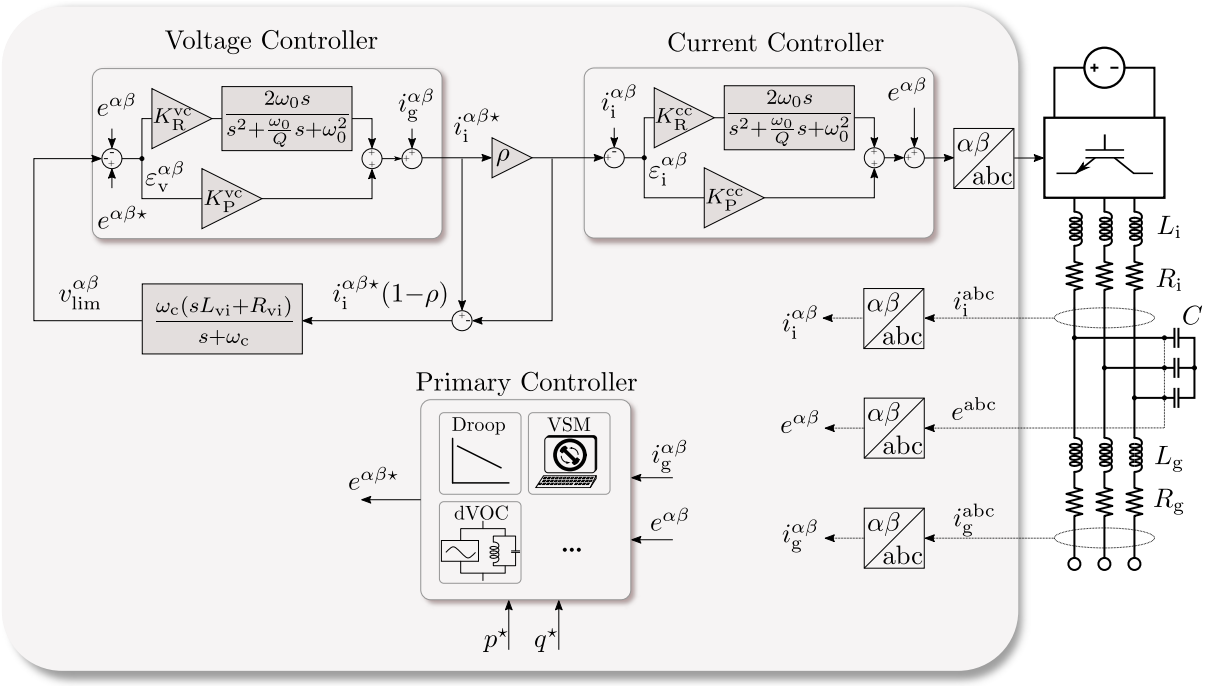

Fig. 6: Control architecture of the GFM inverter with the implementation of the proposed hybrid current limiter.

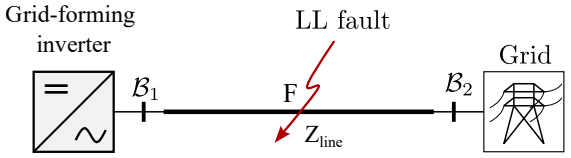

Fig. 7: Simulation scenario with one GFM inverter connected to a stiff grid via a tranmission line upon which a line-to-line fault is applied.

a few percentages, this effect is more pronounced during system-wide faults, as illustrated in the next subsection. The voltage and current sequence phasors during the fault are illustrated in Fig. 8d-f, which display the significant impact of the limiter on the fault behavior of the inverter. The VIMP (Fig. 8e) and the hybrid current limiter (Fig. 8f) allow for controlling the impedance angle of the inverter. As such, they display similar behavior typically seen with synchronous generators during a Line-to-line fault in an inductive grid. The SatLim does not have a means of controlling the current angle, which translates into resistive—even slightly capacitive—inverter behavior during the fault. The capacitive behavior of the inverter was not predicted in Section II, as we made the assumption that the infinite-grid voltage, V_s, and the internal inverter voltage, $E^\star$, are in phase. During real-life faults, this assumption does not hold, which results in a capacitive inverter behavior. The inability of the SatLim to control the output impedance angle of the inverter has a significant impact on the voltage support provided by the inverter, as illustrated hereafter.

B. System-Wide Unbalanced Fault Simulation

Consider the all-inverter 14-bus network in Fig. 9 with 5 GFM inverters interconnected. On line ℓ_3 between bus 2 and 3, an unbalanced line-to-line fault is applied. Details about the network setup and parameters can be found in [5] and in Table I. This simulation is repeated for each current limiter. Fig. 10 depicts the magnitude of the inverter output currents, sequence voltages, and voltage balance for each of the five inverters. The results illustrate that the proposed hybrid current limiter enables the full use of the overcurrent capabilities of the inverter (see Fig. 10a), which is comparable to SatLim. Further, the hybrid limiter exhibits similar positive-sequence voltage support to VIMP, as shown in (Fig. 10b), and significant improvement in the negative-sequence voltage suppression (Fig. 10c) compared to both the SatLim and the VIMP limiter. This is a consequence of the combined advantages of limiting the output current to $I_{\max}$ while maintaining control over the output angle of the inverter. As a result, the proposed hybrid limiter outperforms the SatLim and the VIMP limiter in voltage balancing (Fig. 10d). In this paper, we define voltage balance as $1 - \exp\left(-V^+/V^-\right)$. Table II summarizes the pros and cons of each investigated current limiters.

V. Conclusion

This paper proposed a novel current-limiting strategy for GFM inverters during unbalanced grid conditions. The new current limiter combines the state-of-the-art implementations of virtual-impedance and current-reference saturation limitings. As such, it combines the best of both current-limiting methods: i) It allows for fully using the overcurrent capabilities of the GFM inverter, and ii) it allows for controlling the output impedance angle of the GFM inverter, which results in superior voltage balancing compared to the two conventional methods. Through unit-level (to an infinite bus) and system-wide (IEEE 14-bus system) simulations, the performance and benefits of the proposed hybrid current-limiting methods are evaluated in

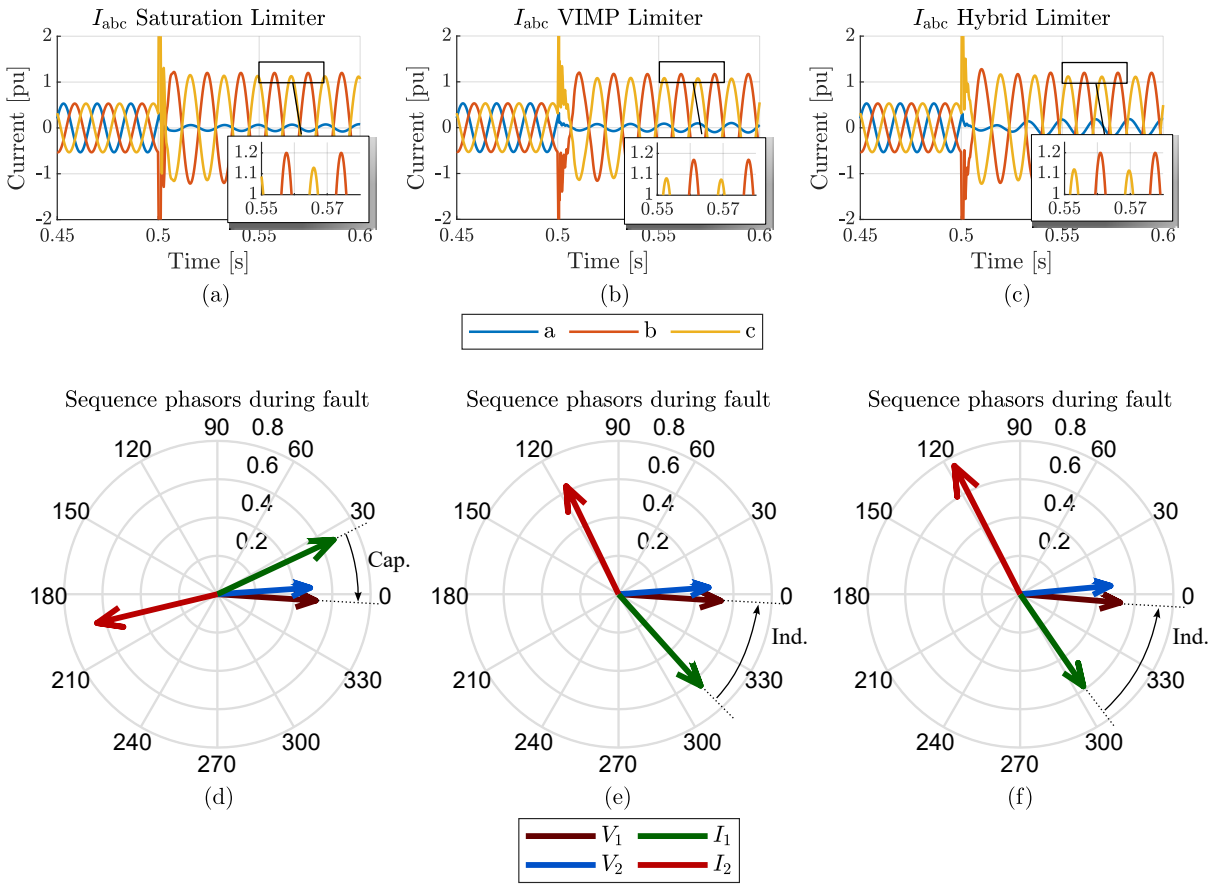

Fig. 8: Instantanuous current waveforms and steady-state sequence phasors of the GFM inverter with the three different current-limiting methods: (a) and (d) for SatLim, (b) and (e) for VIMP, and (c) and (f) for hybrid.

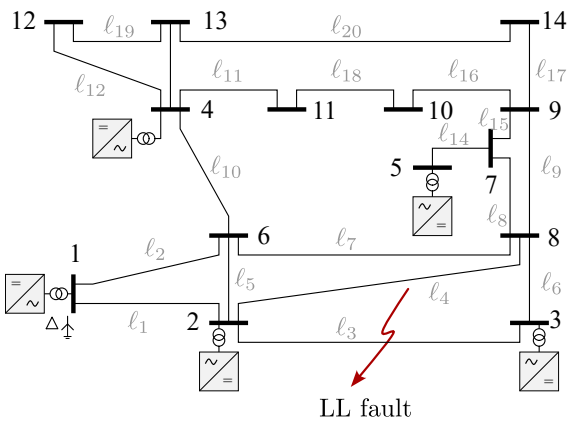

Fig. 9: Five GFM inverters interconnected in a 14-bus network while applying a line-to-line fault between bus 2 and 3.

TABLE I: Inverter and Network Parameters.

Parameter	Value	Unit	Parameter	Value	Unit
ω_s	$2\pi 60$	rad · s^{-1}	K_P^{cc}	0.9801	p.u.
θ_ℓ	75	°	K_R^{cc}	0.0306	p.u.
$L_{tr}\omega_s$	0.03	p.u.	K_P^{vc}	1.2889	p.u.
R_{tr}	0.001	p.u.	K_R^{vc}	0.1444	p.u.
$L_i\omega_s$	0.0196	p.u.	ω_i	$2\pi 3000$	rad · s^{-1}
R_i	0.0139	p.u.	ω_v	$2\pi 500$	rad · s^{-1}
$C\omega_s$	0.1086	p.u.	$\lvert Z_{vi}\rvert$ (VIMP)	0.8333	p.u.
$L_g\omega_s$	0.0196	p.u.	$\lvert Z_{vi}\rvert$ (Hybrid)	1	p.u.
R_g	0.0139	p.u.	θ_{vi} (VIMP)	80	°
I_{max}	1.2	p.u.	θ_{vi} (Hybrid)	80	°

* ω_s: nominal angular grid frequency, θ_ℓ: line impedance angle, L_{tr} and R_{tr}: transformer's inductance and resistance, L_i, R_i, C, L_g, and R_g: the LCL output filter parameters, K_P^{cc}, K_R^{cc}, K_P^{vc}, and K_R^{vc}: inverter control gains for the proportional resonant controllers for the inner-current and outer-voltage loops, ω_i and ω_v: inner-current and outer-voltage loop bandwidths, $|Z_{vi}|$ and θ_{vi}: magnitude and angle of the virtual impedance, both given for the VIMP and Hybrid limiter.

detail. Especially, the improved voltage balancing performance during unbalanced faults in a multi-bus network is striking, which confirms the high potential of the novel approach and motivates further study on its design and interaction with other control blocks.

Acknowledgments

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Appendix

A. *Current-Reference Saturation Limiting*

In a steady state operation, the error feeding into the voltage controller is zero. As such, we derive the following

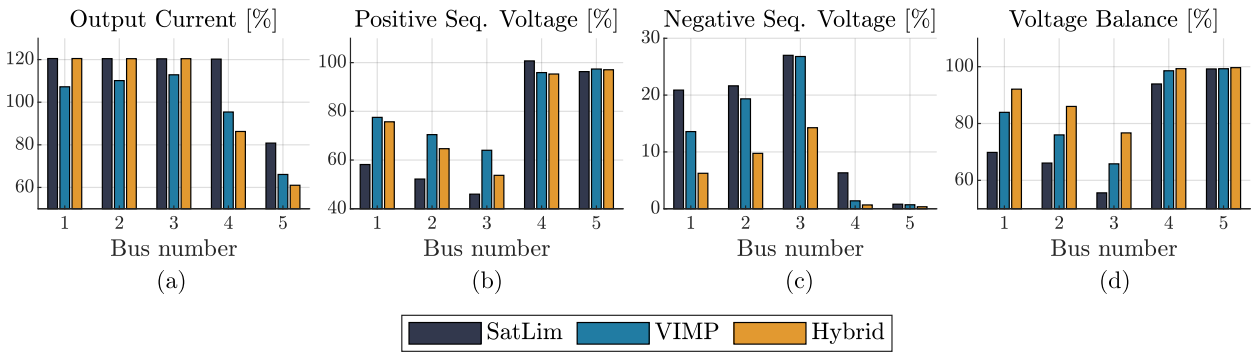

Fig. 10: Comparison of the three current-limiting methods in terms of (a) output current, (b) positive sequence voltage, (c) negative sequence voltage, and (d) voltage balancing.

TABLE II: Comparison of Current-Limiting Strategies.

	SatLim	VIMP	Hybrid
Output impedance angle control	✗	✓	✓
Full use of overcurrent capacity	✓✓	✗	✓✓
Voltage support and balancing	✗	✓	✓✓

expression:

$$\begin{aligned} 0 &= E^\star - E - \Delta V \\ &= E^\star - \rho I^\star Z_\ell - V_\mathrm{s} - (1-\rho) I^\star k_\mathrm{w}, \end{aligned} \tag{1}$$

where Z_ℓ denotes the line impedance, and k_w denotes the anti-windup gain. The gain ρ is defined by:

$$\begin{aligned} \rho &= \min\left(1, \frac{I_\mathrm{max}}{|I^\star|}\right) \\ &= -\frac{1}{2}\left(-1 - \frac{|I^\star|}{I_\mathrm{max}} + \sqrt{\left(\frac{|I^\star|}{I_\mathrm{max}} - 1\right)^2}\right). \end{aligned} \tag{2}$$

From (1) and (2), we derive the following system of equations: one for the real and imaginary axis:

$$\begin{aligned} E_\mathrm{d}^\star - \rho(R_\ell I_\mathrm{d}^\star - \omega_\mathrm{s} L_\ell I_\mathrm{q}^\star) - V_\mathrm{s,d} - k_\mathrm{w}(1-\rho) I_\mathrm{d}^\star = 0 \\ E_\mathrm{q}^\star - \rho(\omega_\mathrm{s} L_\ell I_\mathrm{d}^\star + R_\ell I_\mathrm{q}^\star) - V_\mathrm{s,q} - k_\mathrm{w}(1-\rho) I_\mathrm{q}^\star = 0, \end{aligned} \tag{3}$$

where the real part of variables is denoted by the subscript 'd', and the imaginary part is denoted by subscript 'q'. We can now solve (3) for $I_\mathrm{d}^\star$ and $I_\mathrm{q}^\star$.

B. Virtual Impedance Current Limiting

Recognizing that the voltage-controller error is zero during steady state, the following expression can be defined:

$$\begin{aligned} 0 &= E^\star - E - \Delta V \\ &= E^\star - I^\star Z_\ell - V_\mathrm{s} - \psi I^\star Z_\mathrm{vi}. \end{aligned} \tag{4}$$

The gain, ψ, is inspired by [5] and is defined by:

$$\psi = \begin{cases} \left(\dfrac{|I^\star| - I_\mathrm{th}}{I_\mathrm{max} - I_\mathrm{th}}\right) & \text{if } |I^\star| > I_\mathrm{th}, \\ 0 & \text{if } |I^\star| \le I_\mathrm{th}. \end{cases} \tag{5}$$

The virtual impedance magnitude, $|Z_\mathrm{vi}|$, is determined by the nominal voltage, E_0, and maximum current, I_max, [5]:

$$|Z_\mathrm{vi}| = \frac{E_0}{I_\mathrm{max}}. \tag{6}$$

The angle of the virtual impedance is a design choice. From (4), (5), and (6), we derive the following system of equations to identify the inverter's output current under faults:

$$\begin{aligned} E_\mathrm{d}^\star - R_\ell I_\mathrm{d}^\star + \omega_\mathrm{s} L_\ell I_\mathrm{q}^\star - V_\mathrm{s,d} - \psi(R_\mathrm{vi} I_\mathrm{d}^\star - \omega_\mathrm{s} L_\ell I_\mathrm{q}^\star) = 0 \\ E_\mathrm{q}^\star - \omega_\mathrm{s} L_\ell I_\mathrm{d}^\star - R_\ell I_\mathrm{q}^\star - V_\mathrm{s,q} - \psi(\omega_\mathrm{s} L_\ell I_\mathrm{d}^\star + R_\mathrm{vi} I_\mathrm{q}^\star) = 0. \end{aligned}$$

C. Hybrid Current Limiting

Similarly, one can find the equality in steady state:

$$\begin{aligned} 0 &= E^\star - E - \Delta V \\ &= E^\star - \rho I^\star Z_\ell - V_\mathrm{s} - (1-\rho) I^\star Z_\mathrm{vi}, \end{aligned} \tag{7}$$

where ρ is defined in (2), and Z_vi is a design choice. From the above, we conjure the following set of equations, to solve for the inverter's output current:

$$\begin{aligned} E_\mathrm{d}^\star - \rho(R_\ell I_\mathrm{d}^\star - \omega_\mathrm{s} L_\ell I_\mathrm{q}^\star) - V_\mathrm{s,d} - (1-\rho)(R_\mathrm{vi} I_\mathrm{d}^\star - \omega_\mathrm{s} L_\mathrm{vi} I_\mathrm{q}^\star) = 0 \\ E_\mathrm{q}^\star - \rho(\omega_\mathrm{s} L_\ell I_\mathrm{d}^\star + R_\ell I_\mathrm{q}^\star) - V_\mathrm{s,q} - (1-\rho)(\omega_\mathrm{s} L_\mathrm{vi} I_\mathrm{d}^\star + R_\mathrm{vi} I_\mathrm{q}^\star) = 0. \end{aligned}$$

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