



# Epitaxial Integration of Dirac Semimetals with Si(001)

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**Abstract:** Topological semimetals contain novel combinations of properties that make them useful in a variety of applications, including optoelectronics, spintronics and low energy computing, and catalysis. Although they have been grown with high quality as bulk single crystals, incorporation with semiconductor substrates will ultimately be required to maximize their technological reach. Here, epitaxial growth of the Dirac semimetal  $\text{Cd}_3\text{As}_2$  on Si(001) is demonstrated through two routes. First,  $\text{Cd}_3\text{As}_2$ (112) epilayers are grown on Si(001) via an intermediate CdTe(111) buffer layer. Second,  $\text{Cd}_3\text{As}_2$ (112) is grown directly on Si(001). This work sets the foundation for integration of novel semimetal materials with existing CMOS technology.

**Keywords:** molecular beam epitaxy; topological semimetals; thin films; silicon

## 1. Introduction

Topological semimetals offer a unique combination of properties relevant for a wide variety of applications. Dirac semimetals, which contain pairs of degenerate, linear band crossings, present high electron mobilities [1], broadband light absorption [2], fast carrier dynamics, and low thermal conductivities [3]. Weyl semimetals, in which the pairs of nodes are non-degenerate and of opposite chirality, share many of these same properties, along with added sensitivity to light polarization [4] and the potential to exhibit large spin Hall angles [5]. Such properties are advantageous for photodetectors [6,7], optical switches [8], spin-orbit torque devices [5], thermoelectrics [9–11], and catalysts [12]. Additionally, the surface and bulk electronic states have topological protection arising from the symmetry of the crystal, resulting in increased robustness from a variety of defects and scattering mechanisms [4]. Many of these materials were initially synthesized as bulk crystals, allowing for the study of their basic properties. Advances in thin film synthesis and integration with semiconductor device structures are now required to access and utilize their unique properties in devices.

Thin film synthesis of the Dirac semimetal  $\text{Cd}_3\text{As}_2$  by molecular beam epitaxy (MBE) has yielded the highest mobility thin film semimetals to date.  $\text{Cd}_3\text{As}_2$  has a tetragonal crystal structure ( $a = b = 1.26$  nm and  $c = 2.54$  nm) [13,14], making it amenable to epitaxy on zinc blende and diamond lattices. Although bulk single crystals have the highest reported mobilities [1], much progress has been on tailoring growth approaches on conventional substrates to minimize extended defects, while also achieving lower carrier concentrations. The atomic arrangement of its lowest energy (112) surface is similar to that of (111) zinc blende surfaces, and high quality growth was first achieved on GaAs(111) substrates [15]. Since then, epitaxy has also been carried out on GaSb(001) [16] and commercially relevant GaAs(001) [7,17] substrates, presenting clear pathways to designing and fabricating integrated device structures. Combined with II-Te or III-Sb buffer layers, all have templated the growth of  $\text{Cd}_3\text{As}_2$  with room temperature mobilities of 10,000–20,000  $\text{cm}^2$ . A key enabling feature has been the use of lattice-matched buffer layers to reduce relaxation-induced defect formation. The next frontier in harnessing the properties of topological semimetals is to grow them on Si(001) substrates.



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Integration of topological semimetals with Si offers two distinct possibilities, among others. First, it could enable the incorporation of optoelectronic functionality into Si-based devices. Significant effort has been made recently to incorporate III–V compounds with Si. However, the low defect tolerance of III–V devices require growth strategies to minimize defect formation, such as using anti-phase domain free GaP [18], or quantum dot structures, such as InAs on GaAs, that can withstand high defect densities better than typical quantum wells due to the dots' ability to emit independently of each other [19]. Expanding the selection of materials that offer greater defect tolerance and additional functionality will help to advance optoelectronic device technologies, including photodetectors. The reduced dependence of electron mobility on dislocation density in Cd<sub>3</sub>As<sub>2</sub> [20] and demonstration of photodetectors [7] despite greater than 10<sup>8</sup> cm<sup>−2</sup> dislocation densities indicate that topological semimetals could enhance Si-based optoelectronic devices. Beyond this robustness, additional optical mechanisms arising from chirality in Weyl semimetals, such as the bulk photovoltaic effect [21] or the circular photogalvanic effect [22], would also be accessible in these materials and introduce novel light interactions. Second, topological semimetals have been proposed to replace metal interconnects as their dimensions continue to shrink [23,24]. Outperformance is made possible by electron conduction through the surface states, which are topologically protected against backscattering. This application would require topological semimetals to be grown directly on Si with higher electron mobilities.

Here, we report two approaches to grow Cd<sub>3</sub>As<sub>2</sub> on Si(001) substrates. The first utilizes a thin CdTe(111) buffer to re-orient the crystallographic direction for Cd<sub>3</sub>As<sub>2</sub> growth in its low energy (112) orientation, analogous to previously demonstrated growth of CdTe(111) directly on GaAs(001) [17]. When paired with a lattice-matched secondary buffer, we show that Cd<sub>3</sub>As<sub>2</sub> can be synthesized with room temperature mobilities of approximately 4100 cm<sup>2</sup>/V-s. This value is only slightly lower than layers grown on on-axis GaAs(111). The second approach is to grow Cd<sub>3</sub>As<sub>2</sub> layers directly on Si(001) without any II–VI buffer layers. X-ray diffraction shows only Cd<sub>3</sub>As<sub>2</sub>(112) oriented peaks and in situ electron diffraction shows rotational dependence, suggesting the orientation can be switched without the use of a buffer. These results provide a starting point for the integration of Cd<sub>3</sub>As<sub>2</sub> and other topological semimetals with Si and the design of related device structures for a variety of potential applications.

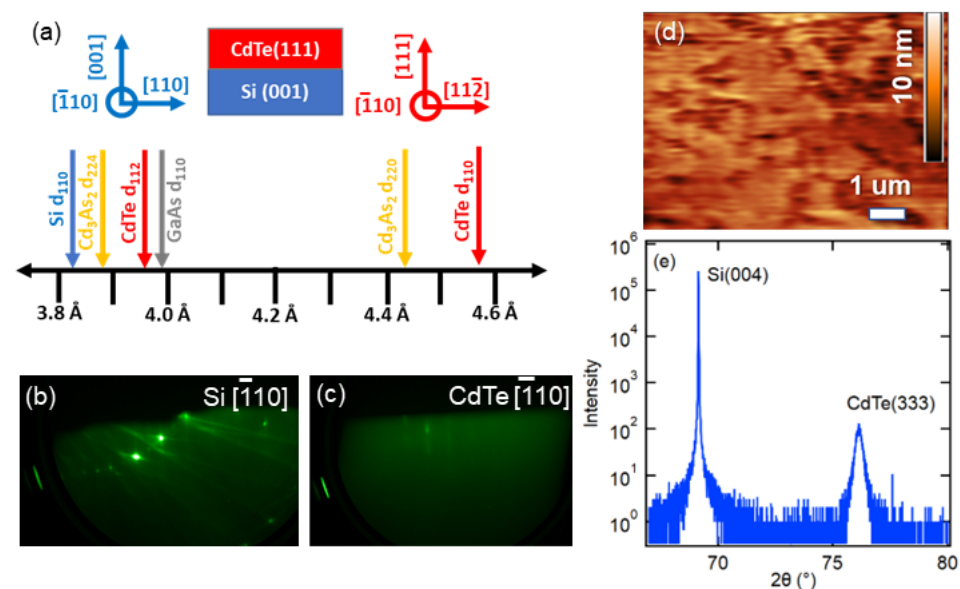
## 2. Materials and Methods

On-axis 1 × 1 cm Si(001) substrates were prepared using a standard RCA clean process, leaving a thin surface oxide layer [25]. The substrates were immediately loaded into a dual chamber Omicron EVO system, outgassed at 600 °C in a buffer chamber, and heated above 850 °C to remove the native oxide in a II–VI growth chamber. Cd and Te were evaporated from standard effusions cells, and As<sub>4</sub> was supplied by a Veeco As cracker. For Cd<sub>3</sub>As<sub>2</sub> growth on II–VI buffer layers, the substrates were cooled to 195 °C under As<sub>4</sub> and then Te for initial CdTe nucleation, followed by a ramp in temperature to 220 °C and a 5 min anneal at 350 °C under a Te overpressure. A 2/1 Te/Cd ratio is used during growth of the CdTe layer. For some samples, an additional Zn<sub>(1−x)</sub>Cd<sub>x</sub>Te buffer, with a composition approximately lattice matched to Cd<sub>3</sub>As<sub>2</sub>, was subsequently grown on the annealed CdTe layer at 290 °C also using a Te overpressure during growth. For Cd<sub>3</sub>As<sub>2</sub> growth directly on Si, the substrates followed a similar cool down procedure from the oxide removal step under As<sub>4</sub>/Te. In all cases, Cd<sub>3</sub>As<sub>2</sub> growth was carried out at approximately 115 °C under As-rich conditions with ultraviolet light exposure from an xenon lamp with up to 100 W of supplied power, as described elsewhere [26]. Electrical measurements were performed in a Quantum Design Physical Properties Measurement System on 6-point Hall bars fabricated by standard photolithographic methods and etchants containing hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>) and ammonium hydroxide (NH<sub>4</sub>OH). Temperature dependent Hall measurements were performed under fields of +/−100 Oe with excitation currents of 100 μA. Three-dimensional carrier concentrations were calculated using a film thickness extracted through ellipsometry. X-ray diffraction (XRD) was performed on a Rigaku Smartlab system using an incident

2-bounce Ge (220) monochromator. Atomic force microscopy (AFM) was performed in air using a Nanosurf FlexAFM system in dynamic force mode with a vibration amplitude of approximately 5mV over  $10 \times 10 \mu\text{m}$  regions.

### 3. Results

Figure 1a summarizes the relationship between the atomic spacing within the relevant layers and orientations. In particular, rotation of the crystallographic orientation reduces the mismatch between the CdTe layer from  $>10\%$  to  $<1\%$  in the case of GaAs by rotating the crystal to align the  $[110]_{\text{GaAs}}$  and  $[11\bar{2}]_{\text{CdTe}}$  axis. Attempts at using a ZnTe(001) as an interlayer analogous to GaAs(111) buffer structures would be possible but would require optimal growth conditions and microns of material to achieve high quality material [27]. Additionally, this would ultimately result in  $\text{Cd}_3\text{As}_2(001)$ , which is a much higher energy surface [7]. High quality growth of CdTe(111) directly on GaAs(001) was previously achieved by engineering the interfacial chemistry to promote a strain-driven change in the crystallographic orientation [17,28,29]. That approach critically relies on maximizing Ga-Te bonding at the interface, namely a high temperature anneal combined with a Te pre-growth exposure, to create a pseudoepitaxial relationship with the (111) surface [30].



**Figure 1.** Summary of CdTe(111) growth on Si(001): (a) layer schematic of data shown in (b–d) along with crystallographic orientation of the major axis of Si (blue) and CdTe (red) as well as a plot of atomic spacing of Si, GaAs in the  $\langle 110 \rangle$  direction, and CdTe,  $\text{Cd}_3\text{As}_2$  in  $[110]$ ,  $[220]$  and  $[11\bar{2}]$ ,  $[22\bar{4}]$  directions, respectively.  $\text{Cd}_3\text{As}_2$  has a 2:1 epitaxial relationship with the semiconductor layers; (b) RHEED image of Si(001) following oxide desorption; (c) RHEED image of CdTe(111) following anneal; (d) AFM image of CdTe(111) surface; (e) XRD of CdTe(111) grown directly on Si(001).

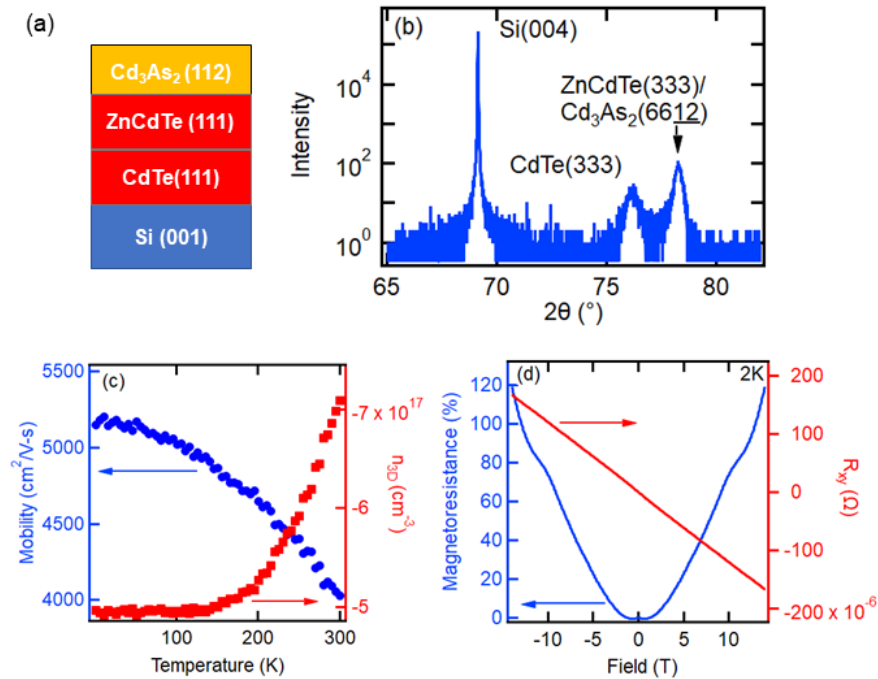
Although interfacial engineering is more limited with an elemental semiconductor, an analogous approach was also shown to work for Si [31] and is employed here. Following desorption of the surface oxide at high temperatures, as evident in the reflection high energy electron diffraction (RHEED) pattern shown in Figure 1b, As and Te surfactants are used during cool down to create a favorable bonding arrangement for CdTe epitaxy in the (111) orientation with minimal anti-phase domains.  $\text{As}_4$  is supplied until approximately  $450^\circ\text{C}$ , and then Te is supplied. It has been suggested from X-ray photoelectron spectroscopy that Te-Si bonding is favorable, whereas Cd-Si bonds are not formed, and further postulated that allowing Te to diffuse to step edges is critical to creating highly oriented films [32]. Often a substrate miscut of multiple degrees is used for this purpose in order to intentionally create steps to suppress twin domains. In this system, however, larger miscuts were

shown to decrease crystal quality and increase tilt between the two layers [31]. On-axis substrates generally have a miscut of up to  $0.5^\circ$  and provide the starting surface with some density of steps. Whereas a spotty RHEED pattern was present during the initial CdTe nucleation phase, further annealing under Te results in a streakier RHEED (Figure 1c) pattern and ultimately a surface roughness of approximately 1 nm, as observed in AFM (Figure 1d). XRD patterns show only peaks related to the substrate and CdTe(111), with a (333) rocking curve peak full-width half-max (FWHM) of 730 arcseconds for 100 nm thick CdTe layers. Although this FWHM value is larger than those reported for similar growths on GaAs(001) [17], previous reports of CdTe growth on Si required thicknesses of  $>1 \mu\text{m}$  to achieve superior FWHM values [31]. This increased thickness is likely due to the limited ability to tailor the interface. FWHM of 60 arcseconds on GaAs(001) and 140 arcseconds on Si(001) have been reported on optimized samples with thicknesses  $> 8 \mu\text{m}$  [32], however, that amount of material is likely prohibitive for many applications.

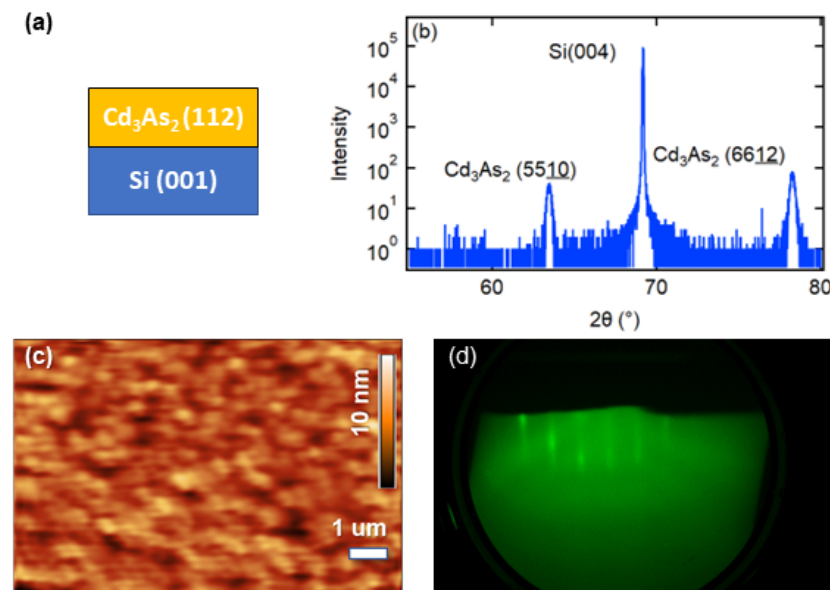
In order to obtain a two step buffer structure to establish a lattice-matched template for  $\text{Cd}_3\text{As}_2(112)$  growth, a  $\text{Zn}_{1-x}\text{Cd}_x\text{Te}$  layer with approximately 42% Zn was grown atop the CdTe(111) nucleation layer, as shown in Figure 2a. The use of a lattice-matched buffer layer, even if only 100 nm thick, was shown to significantly enhance the mobility of similar structures on GaAs(111) substrates [26], and an analogous approach was shown to be effective on GaAs(001) [17]. Any attempts to introduce Zn into the initial nucleation layer resulted in both (111) and (001) related peaks visible in XRD patterns, highlighting the role of strain in this orientation change. Although no change in threading dislocation density was observed using electron channeling contrast imaging, evidence of other extended defects was observed in relaxed  $\text{Cd}_3\text{As}_2$  films that were not present in films grown on lattice-matched buffers. Studies in the (001) system showed minimal dependence on the threading dislocation density on the carrier mobilities of bulk thin films [20]. II–VI (111) and  $\text{Cd}_3\text{As}_2(112)$  related peaks are visible in the XRD pattern ( $\text{Cd}_3\text{As}_2$  has a 2:1 epitaxial relationship with II–VI layers). A resulting room temperature mobility of  $4100 \text{ cm}^2/\text{V-s}$  was measured and rose to  $5200 \text{ cm}^2/\text{V-s}$  at 2K. Carrier concentrations, as measured by the Hall voltage, decreased from  $7.0 \times 10^{17} \text{ cm}^{-3}$  to  $5.0 \times 10^{17} \text{ cm}^{-3}$  over that temperature range, slightly higher than typical values on GaAs substrates. These mobility values are similar to those measured in  $\text{Cd}_3\text{As}_2$  epilayers grown on on-axis  $\text{ZnCdTe}(111)/\text{CdTe}(111)/\text{GaAs}(001)$  [17] and  $\text{ZnCdTe}/\text{GaAs}(111)$  structures but below those grown on miscut GaAs(111) and GaAs(001) substrates to control for twin defects [26]. Magnetoresistance data taken at 2K looks typical of  $\text{Cd}_3\text{As}_2$  films, with a polynomial shape at lower fields that slowly transitions to a linear shape with increasing field. The main difference is that the transition to linear behavior occurs at a much larger field value and with a much lower overall magneoresistance amplitude due to the lower mobility. This linear behavior is a typical fingerprint of topological semimetal systems and has been theorized to arise due to a combination of small potential fluctuations due to disorder and a scattering time much larger than the cyclotron period [33]. Hall voltages were linear through at least 14T from 300K to 2K, indicating the transport is dominated by a single electron carrier.

Finally, in an attempt to directly integrate  $\text{Cd}_3\text{As}_2$  with Si, the II–VI buffer layers were omitted, and  $\text{Cd}_3\text{As}_2$  growth was initiated immediately following cool down from the high temperature Si oxide desorption step under identical As/Te exposures, followed by an As exposure directly prior to growth. The direct  $\text{Cd}_3\text{As}_2$  nucleation occurred at similar temperatures as on II–VI buffer layers ( $100\text{--}115^\circ\text{C}$ ), but exhibited hazy, spotty RHEED patterns for a much longer period of time. AFM images, shown in Figure 3b, reveal a rougher (approximately 4 nm) surface morphology than typical (112) layers. Peaks related to  $\text{Cd}_3\text{As}_2(112)$  were only visible in the XRD spectrum, with no evidence of any [001] domains. The switch from the [001] orientation of the substrate is likely due to the much higher energy of the  $\text{Cd}_3\text{As}_2(001)$  surface [26] combined with a similar surface bonding mechanism that reorients CdTe in the  $\langle 111 \rangle$  direction. RHEED observed during growth reveals a pattern and surface reconstruction typical of  $\text{Cd}_3\text{As}_2$  [17], as well as a changing pattern with rotation, consistent with a film with in-plane epitaxial registry rather than

a textured polycrystal. Electrical measurements are not possible on the film due to the use of p-type substrate in this particular case. However, similar growth attempts directly on GaAs(001) resulted in room temperature mobilities of approximately  $2000 \text{ cm}^2/\text{V}\cdot\text{s}$ , approximately half of typical values of relaxed films grown on on-axis GaAs(111) substrates and CdTe/ZnTe buffer layers.



**Figure 2.** Growth of  $\text{Cd}_3\text{As}_2$  on  $\text{CdTe}(111)/\text{Si}(001)$ : (a) layer schematic of sample shown in (b–d); (b) XRD pattern of  $\text{Cd}_3\text{As}_2$  grown on a two step II–VI buffer on  $\text{Si}(001)$ ; (c) temperature dependent Hall data showing carrier concentration (right axis) and mobility (left axis); (d) magnetoresistance (left axis) and  $\rho_{xy}$  (right axis) as a function of magnetic field taken at 2K.



**Figure 3.** Demonstration of direct growth of  $\text{Cd}_3\text{As}_2$  on  $\text{Si}(001)$ : (a) layer schematic; (b) AFM image of  $\text{Cd}_3\text{As}_2$  grown directly on  $\text{Si}(001)$ ; (c) XRD pattern of  $\text{Cd}_3\text{As}_2/\text{Si}(001)$  showing only (112) related peaks; (d) RHEED pattern of  $\text{Cd}_3\text{As}_2$  surface.

#### 4. Discussion

Although the electron mobility of Cd<sub>3</sub>As<sub>2</sub> epilayers grown on lattice-mismatched buffers remains high relative to semiconductors with similar dislocation densities, it is still sensitive to the surface on which it is grown. Because conventional GaAs and Si substrates do not have the same lattice spacing as Cd<sub>3</sub>As<sub>2</sub>, buffer layers play an important role in aiding nucleation and minimizing dislocation formation in the Cd<sub>3</sub>As<sub>2</sub> epilayers. In cases where (001) substrate orientations are preferred for device design or manufacturing considerations, the ability to switch the orientation of Cd<sub>3</sub>As<sub>2</sub> to its preferred (112) surface, through growth on a buffer layer or directly on the substrate, is also beneficial, providing smoother surfaces and than if a (001) orientation was preserved throughout the structure. The decrease in lattice mismatch in one direction with this rotation also requires less buffer layer material to achieve crystalline quality in such a structure.

We note three important aspects that play a role in the growth of Cd<sub>3</sub>As<sub>2</sub> on Si(001). First, although an analogous crystallographic orientation rotation takes place, the lattice mismatch between Si and CdTe ([1 $\bar{1}$ 0] and [11 $\bar{2}$ ], respectively) is much greater than that between GaAs and CdTe in the same directions (−3.3% vs. 0.7%). The 4-fold symmetry of the substrate also opens the possibility of anti-phase domain formation. Both establish the potential for enhanced extended defect generation in the Cd<sub>3</sub>As<sub>2</sub> epilayers than growth on GaAs. Second, growths here were performed on on-axis Si(001) substrates. From previous growth efforts on GaAs(111) and (001) substrates, it is well known that twin domains can easily form in both the Cd<sub>3</sub>As<sub>2</sub> and the underlying II–VI buffer layers and can significantly limit the electron mobility. This point is highlighted by the fact that, despite the larger lattice mismatch, the room temperature mobility reported here for growth on Si(001) is on the lower end of what was reported for on-axis GaAs(111) (4000–6000 cm<sup>2</sup>/V-S) [26]. Growth on miscut substrates helps to reduce twin domains, and for applications where these substrates are acceptable, much larger mobilities are likely achievable, even if the CdTe buffers may decrease slightly in crystalline quality from this [31]. Finally, it is possible that the epitaxial registry between the Cd<sub>3</sub>As<sub>2</sub>/Si is much weaker than on CdTe/Si structures, but because (112) is a much lower energy surface, minimizing this surface energy is largely driving the orientation shift in the case of growth directly on Si rather than the interfacial bonding and strain. No evidence is observed that these films are textured polycrystals, but pervasive, smaller scale in-plane misorientations are possible and more likely than when the growth structures contain buffer layers.

Growth of Cd<sub>3</sub>As<sub>2</sub> directly on Si offers an epitaxial route for applications where buffer layers would hinder vertical device performance or their incorporation is not possible while also providing the simplest growth approach possible. Deposition temperatures of only 100–150 °C are compatible with most structures and would allow for Cd<sub>3</sub>As<sub>2</sub> films to be added late in the device fabrication process if combined with appropriate surface cleaning prior to growth. For structures that can withstand higher temperatures and require higher material quality, films may be annealed at temperatures well above 150 °C. As noted earlier, the epitaxial registry may be quite weak, leading to in-plane disorder, and previous reports consistently show the limitations that extended defects put on the electron mobility. Starting from amorphous films, an annealing approach was shown to greatly improve crystal quality with short 500–600 °C exposures (5 min) on SrTiO<sub>3</sub> (001) [34] and led to mobilities above 30,000 cm<sup>2</sup>/V-s. The high vapor pressure of Cd<sub>3</sub>As<sub>2</sub> requires thin films to be encapsulated to survive such high temperatures, such as using low-temperature atomic layer deposition of Al<sub>2</sub>O<sub>3</sub>, or SiN/SiO<sub>2</sub> deposited on CdTe capped samples. Given the starting level of crystallinity in these thin films, similar levels of improvement should be possible.

Expanding the material selection to Weyl semimetals using similar approaches may also be possible to further expand possible applications. TaAs has recently been grown in thin film form on GaAs(001) as both a thin single crystal [35] and a polycrystal [5]. Beyond the previously discussed properties of chiral topological semimetals, the use of Weyl semimetals as an interconnect material is also promising due to their unique

conductivity scaling with dimensionality [23], which, unlike conventional metals such as copper, does not increase with decreasing length scales because of its surface states. Growth of materials such as TaAs and NbAs will be more difficult due to higher synthesis temperatures (>350 °C) and the possibility of interfacial silicide formation. Cd<sub>3</sub>As<sub>2</sub> can alternatively be magnetically doped to form a Weyl semimetal but would face additional growth challenges [36].

## 5. Conclusions

This work details two routes to epitaxially integrating Cd<sub>3</sub>As<sub>2</sub> onto Si(001) using both II–VI buffers and direct growth onto the substrate. These synthesis routes build on previous approaches for growth on compound semiconductors but tailor them for Si, significantly extending the technological uses of a topological semimetal. The combination of these strategies allow for a variety of device designs, and the low temperature growth process is compatible with a variety of existing Si device processing requirements. Although the electron mobility is lower than in Cd<sub>3</sub>As<sub>2</sub> films grown under optimized conditions on GaAs(111) or (001) substrates, we outline several additional approaches to realizing future improvement depending on the parameters and restrictions of the application. Ultimately, integration of Dirac and Weyl semimetals with Si(001) substrates expands the possibilities for (opto)electronic device design and performance beyond what is currently possible in integrated multiferroic oxides or direct-band gap compound semiconductors, or even conventional metallic interconnects. This study establishes a foundation for future integration advances of these systems.

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**Conflicts of Interest:** The authors declare no conflict of interest.

**Sample Availability:** Samples of the compounds are available from the authors.

## Abbreviations

The following abbreviations are used in this manuscript:

MBE	Molecular beam epitaxy
RHEED	Reflection high energy electron diffraction
AFM	Atomic force microscopy
XRD	X-ray diffraction
FWHM	Full-width half-max

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