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Ultrathin stable Ohmic contacts for high-temperature operation of β-Ga_2O_3 devices

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ABSTRACT

Beta gallium oxide (β-Ga_2O_3) shows significant promise in high-temperature, high-power, and sensing electronics applications. However, long-term stable metallization layers for Ohmic contacts at high temperatures present unique thermodynamic challenges. The current most common Ohmic contact design based on 20 nm of Ti has been repeatedly demonstrated to fail at even moderately elevated temperatures (300–400 °C) due to a combination of nonstoichiometric Ti/Ga_2O_3 interfacial reactions and kinetically favored Ti diffusion processes. Here, we demonstrate stable Ohmic contacts for Ga_2O_3 devices operating up to 500–600 °C using ultrathin Ti layers with a self-limiting interfacial reaction. The ultrathin Ti layer in the 5 nm Ti/100 nm Au contact stack is designed to fully oxidize while forming an Ohmic contact, thereby limiting both thermodynamic and kinetic instability. This novel contact design strategy results in an epitaxial conductive anatase titanium oxide interface layer that enables low-resistance Ohmic contacts that are stable both under long-term continuous operation (>500 h) at 600 °C in vacuum ($\leq 10^{-4}$ Torr), as well as after repeated thermal cycling (15 times) between room temperature and 550 °C in flowing N_2. This stable Ohmic contact design will accelerate the development of high-temperature devices by enabling research focus to shift toward rectifying interfaces and other interfacial layers.

I. INTRODUCTION

β-Ga_2O_3 is a strong candidate for next-generation high-temperature electronic device manufacturing for both power and sensing applications. As a material, it shows excellent figures of merit for high-voltage operation and high frequency switching, due to its large bandgap and high theoretical breakdown field.[1–3] Additionally, β-Ga_2O_3 is readily n-type dopable at shallow levels, with Si and Sn being the most common dopants.[1] From a manufacturing perspective, single-crystal Ga_2O_3 substrates can be grown by both Czochralski (CZ) and edge-defined film-fed growth, which allows for potential industrial scaling. Projective cost modeling suggests that as the technology develops, the economic viability and technological value of Ga_2O_3-based devices will continue to improve and be competitive with existing SiC and GaN technologies.[4,5]

Reliable and stable Ohmic contacts are necessary for all types of Ga_2O_3-based devices. Currently, many groups use some variation of the commonplace Ti/Au metallization scheme, where most frequently a Ti layer of at least 20 nm is applied, followed by a chemically protective and electrically conductive Au layer.[6–18] Variations that include additional diffusion barrier layers are also common.[19–24] This contact scheme is most frequently annealed at 470 °C for 90 s in nitrogen. Titanium is chosen as an interlayer due to its good adhesion to both semiconductors/oxides and other metals, as well as its desirable electrical properties—Ohmic contacts of this design regularly demonstrate minimal degradation at or

around room temperature operation. For Ga_2O_3-based devices, this contact scheme has demonstrated low specific contact resistances, on the order of $10^{-3}\,\Omega\,cm^2$ for traditional n-type substrates,[16,17] and between 10^{-5} and $10^{-6}\,\Omega\,cm^2$ for surface treated substrates (e.g., ion implantation).[12,13]

While these contacts demonstrate acceptable stability at room temperature, few studies have examined the effects of long-term, high-temperature operation on their performance; to date, the few studies done reveal significant problems with rapid contact degradation even at relatively modest temperatures (300–400 °C). One group showed that a Si-implanted substrate treated with a reactive ion etch demonstrated stability with this metallization scheme over the course a 100+ h thermal aging procedure at 300 °C. Compared to this treated substrate, the contact resistance of an untreated metal-semiconductor junction increased by almost 40% over the same period.[17] Previously, we subjected a vertical Schottky device with a 20 nm Ti/100 nm Au Ohmic contact to repeated thermal cycling, up to 410 °C, and found that the series resistance of the device increased by several orders of magnitude.[18] This is problematic for applications where operation to 600 °C is desired.

Degradation of this standard Ohmic contact design is hypothesized to be due primarily to the formation of a 3–5 nm Ti/TiO_x "defective" interfacial layer between the Ga_2O_3 and the Ti contact. This is supported by thermodynamic analysis, as annealing can provide conditions that are favorable for the formation of several different titanium oxides, resulting in redox reactions between titanium and gallium oxide. This is thought to result in a gallium-rich suboxide layer in contact with a TiO_x suboxide layer. In addition, the remainder of the unreacted Ti either forms nanocrystals within Au[16] or migrates through Au to the outer surface over time, likely due to favorable thermodynamic driving factors (i.e., gradients in oxygen chemical potential), as well as facile Ti-diffusion kinetics that increases with temperature.[18,25] As such, electrical performance can be marred by the high Ti mobility and its redistribution during device operation. Both the formation of an oxide layer on top of the gold contact layer and the formation of nanocrystalline scattering sites are thought to reduce the performance and reliability of the Ohmic contact.

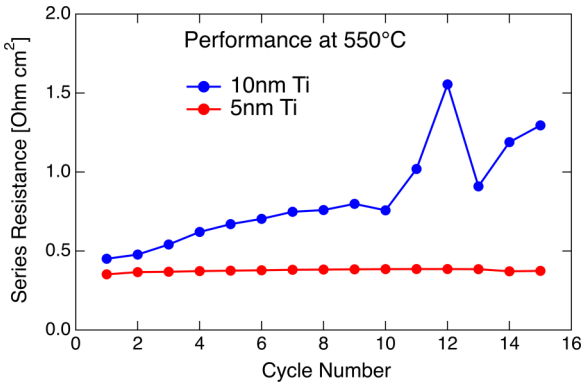

FIG. 1. Main result of this work, showing the comparative performance of stable 5 nm and unstable 10 nm Ti contacts at 550 °C for 15 cycles.

While Ti migration is thought to be detrimental to contact stability, the thin Ti/TiO_x "defective" interfacial layer that forms between the Ga_2O_3 and the Ti contact can potentially be beneficial. Several studies of the oxidation state of Ti at the Ti/Ga_2O_3 interface suggest the presence of various $Ti_xO_{(2x-1)}$ Magnéli phases, which have been shown to be highly conductive and stable in oxidizing environments.[26–29] These findings suggest that leveraging and controlling the interfacial reaction while minimizing excess mobile Ti can potentially be used to improve contact stability.

Here, we show that an ultrathin titanium interlayer maximizes the completion of the reaction with the Ga_2O_3 substrate while minimizing subsequent Ti diffusion. We first compare the performance of a Ti/Au contact to (001) $Sn:Ga_2O_3$ with 5 and 10 nm of titanium through repeated thermal cycling (15 times) in a N_2 atmosphere. We find that the 5 nm thick Ti contact shows excellent stability and performance under long-term temperature cycling, whereas the 10 nm thick Ti contact shows both greater series resistance and inconsistent thermal and temporal behavior (Fig. 1).

We then further validate both 5 and 10 nm Ti contact designs by fabricating a pair of 12 double-Ohmic vertical devices which we subject to extended high-temperature thermal treatment (600 °C) in a vacuum chamber ($\leq 10^{-4}$ Torr) for an extended period of time (i.e., >500 h for 5 nm; >300 h for 10 nm). We find that for the 5 nm sample, all 12 devices show excellent performance, stability, and repeatability during this extended high-temperature exposure. All 12 devices on the 10 nm sample also demonstrate Ohmic behavior, albeit with both greater variability between devices and overall higher resistances when compared to the 5 nm sample.

Through TEM analysis of the thermally cycled samples, we find that high-temperature operation of the 5 nm samples results in the formation of a highly crystalline, epitaxial titanium oxide interfacial layer which we hypothesize contributes to the reliable, conductive Ohmic contact behavior. Conversely, TEM investigation reveals incomplete oxidation of the thicker 10 nm Ti-based contacts, which correlates with the unstable thermal and temporal behavior of these devices. This also likely explains the thermal instability of the even thicker 20 nm Ti-based contact scheme commonly adopted in the field. We find that diffusion of Ti to the outer surface occurs in both 5 and 10 nm Ti samples, suggesting that its effects are secondary to those of the interfacial contact layer quality.

II. EXPERIMENTAL METHODS

To test the Ohmic contacts, we employ both thermal cycling ("cycle") and long-term thermal holds at static temperature ("soaking") under an inert, flowing atmosphere (N_2) and vacuum ($\leq 10^{-4}$ Torr), respectively.

A. Sample preparation

Devices were fabricated using (001) Sn-doped Ga_2O_3 from Novel Crystal Technologies. Photoresist was removed from the as-delivered substrate via an organic wash, followed by a sulfuric acid/peroxide rinse. The bi-metal deposition of Ti/Au via e-beam was performed with a Temescal FC2000 Evaporation System in high vacuum ($\leq 2 \times 10^{-6}$ Torr) without venting between layers. Contacts fabricated for thermal cycling consist of two large-area

pads (average area of each $\cong 0.13\,cm^2$) deposited on a $5 \times 10\,mm^2$ piece of Ga_2O_3 substrate in a lateral configuration. Contacts fabricated for thermal soaking consist of a monolithic large-area back contact, and a 3×5 matrix of $500\,\mu m$ square pads (area of each pad $= 2.5 \times 10^{-3}\,cm^2$) in a linear transmission line method configuration as a front contact.

The difference in device design between the thermal cycling and thermal soaking experiments had multiple intentions. First, the instrument in which the thermal cycling was performed has stationary probe tips. Given the wide temperature range, we chose a large area to help alleviate any thermal expansion that might cause the probes to slip off. Second, the large area aided in the post-mortem analysis by ensuring the presence of regions that were unaffected by mechanical damage from the probe tips. Finally, the variation in contact size allows evaluation of performance for both large- and small-area pads.

Following contact deposition, samples were annealed via rapid thermal processing (ULVAC-RIKO MILA-3000 Rapid Thermal Processing Unit) at 550 °C for 90 s in flowing N_2. On separate $10 \times 10\,mm$ substrates with metallized corners, the carrier concentration was determined via high-temperature Hall measurement from 50 to 400 °C via a custom instrument.[30] Values were approximately constant in this temperature range at $\sim 4 \times 10^{18}\,cm^{-3}$. See supplementary material[33] for a more detailed depiction of these results, including resistivity and mobility.

B. Electrical characterization

For thermal cycling, two-probe measurements (source I, measure V) were performed by a Keithley 236 SMU in an Instec HCP621G-PMH probe station under flowing nitrogen at 40 SCCM. A single thermal cycle consisted of ramping from 25 to 550 °C and back down to 25 °C in 75 °C increments. Each temperature increment was allowed to equilibrate for 15 min before electrical measurements were performed.

Thermal soaking experiments were performed in a custom McAllister vacuum probe station with two probe arms, each equipped with three-axis stepper motors. The stepper motor and temperature could be controlled externally, enabling sequential measurement of multiple devices without breaking vacuum. A vacuum level of $\leq 10^{-4}$ Torr was maintained by an Agilent TPS-compact vacuum pump. Electrical measurements were performed with the same Keithley 236 SMU. To initiate the long-duration thermal soak, the probe station was first ramped from room temperature to 600 °C at approximately 50 °C per hour, with electrical measurements collected after each 75 − 90 °C increment.

Both probe stations utilized a silver stage with embedded thermocouples for a temperature feedback loop via the temperature control software. It was assumed that hold times (15 min for cycling, 1–2 h for soaking) were long enough for thermal equilibration to occur between the stage and the device. Device design and testing configurations for both cycling and soaking are shown in Fig. 2.

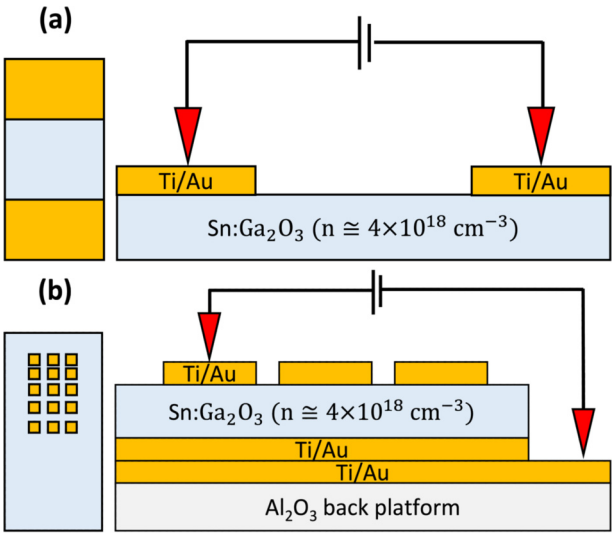

FIG. 2. Top-down and profile views of device architecture and measurement scheme for (a) thermal cycling and (b) thermal soaking measurements. Contacts are comprised of a thin titanium layer (5 or 10 nm) capped by a 100 nm Au layer. Carrier concentration is determined from temperature-dependent Hall measurements.

III. RESULTS AND DISCUSSION

A. Thermal cycling

Figure 3 summarizes the results of electrical measurements for 5 and 10 nm Ti contact architectures subject to extended thermal cycling. For both samples, the temperature was ramped from 25 to 550 °C and back down to 25 °C in increments of 75 °C. Electrical measurements were performed during each temperature increment after a 15-min equilibration period, and a total of 15 cycles were performed, as was summarized in Fig. 1. Total testing time was approximately 90 h for each of the contact architectures.

The 5 nm sample exhibited extremely stable and consistent behavior. Averaged over all cycles, the series resistance increased very slightly with increasing temperature (e.g., from $\approx 0.31 \pm 0.035\,\Omega\,cm^2$ at room temperature to $\approx 0.32 \pm 0.032\,\Omega\,cm^2$ at 550 °C), as well as with increasing cycle number. After 15 cycles, the room temperature series resistance increased from $\approx 0.26\,\Omega\,cm^2$ (cycle 1) to $\approx 0.37\,\Omega\,cm^2$ (cycle 15), a change of 44% or $0.11\,\Omega\,cm^2$.

In contrast, significant variability in the measured series resistance was observed for the 10 nm sample, especially with increasing cycle number. The first eight cycles produced relatively consistent resistance values that gradually increased from $\approx 0.6\,\Omega\,cm^2$ (cycle 1) to $\approx 1.4\,\Omega\,cm^2$ (cycle 8). Series resistance was highest at room temperature and trended toward a minimum at 325 °C before gradually increasing again at still higher temperatures. After the first eight cycles, the series resistance behavior became less consistent, particularly at lower temperatures, with values ranging between ≈ 1.5 and $5\,\Omega\,cm^2$, representing an increase of 250%–900% compared to the initial cycle behavior.

B. Thermal soaking

After reaching 600 °C, the series resistance of the 12 devices was periodically measured every 1–3 days. The 5 and 10 nm samples were

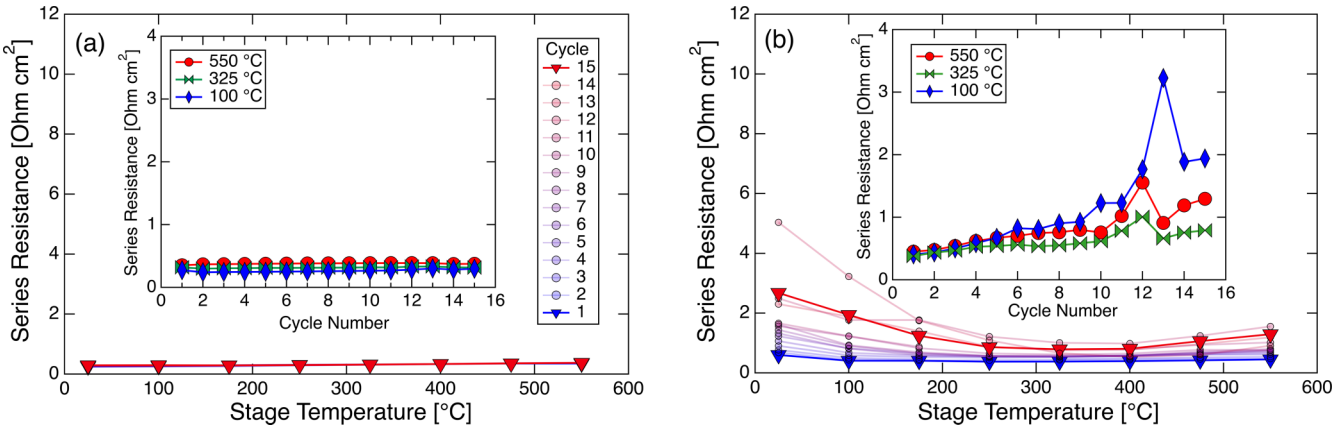

FIG. 3. Thermal cycling experiments for (a) 5 and (b) 10 nm Ti architectures, shown on the same scale bar and using the same legend. The insets show series resistance as a function of cycle number for three different temperatures.

soaked separately under the same conditions and testing procedures. An alumina platform with the 5 nm Ti/100 nm Au metallization scheme was utilized to access the back Ohmic contact of the devices. Shown in Fig. 4(a), the 12-device average series resistance of the 5 nm Ti sample decreased in magnitude from an initial value of $7.7 \pm 2.09\,\Omega$ to a final value of $5.95 \pm 0.23\,\Omega$ over the course of the >500-h thermal soak at 600 °C. Figure 4(b) shows the 12-device average series resistance of the 10 nm Ti sample also decreased with time, from an initial value of $16.08 \pm 0.99\,\Omega$ to a final value of $9.96 \pm 0.68\,\Omega$ over the course of the >300-h soak at 600 °C. This represents a factor of ~2 increase when compared to the 5 nm Ti sample. Contact resistances extracted from TLM measurements after significant thermal stress were on the order of $10^{-3}\,\Omega\,\text{cm}^2$ for both 5 and 10 nm architectures.

Note that the values in Fig. 4 are reported in Ω instead of $\Omega\,\text{cm}^{-2}$ as they include the probe tip resistance, leads, etc., which were found to contribute significantly to the overall resistance. Measurements of each of these contributions were attempted; however, they yielded results that proved too difficult to confidently deconvolve. Hence, we report the lumped resistance values in their entirety. See supplementary material[33] for full results of both TLM measurements and back platform resistances.

The first ≈50 h of thermal soaking produces the greatest variability for the 5 nm sample; after this, all variations seen in the average series resistance across all devices are within one standard deviation of the mean. This behavior suggests a "break-in" period occurs during the initial ~50-h period at temperature during which thermal or electrical processes drive the system toward a uniform,

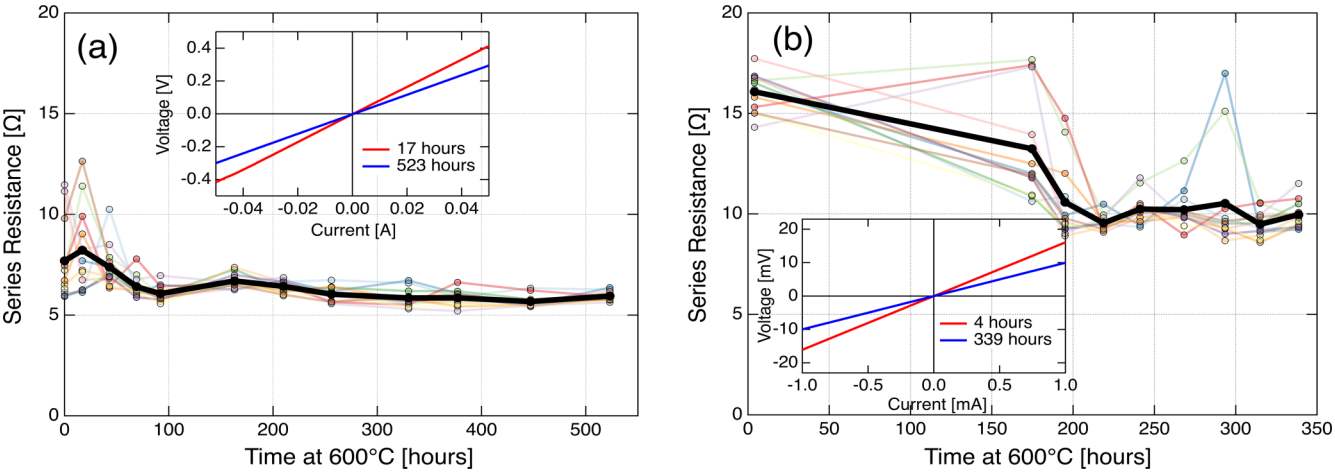

FIG. 4. Time evolution of series resistance for (a) 5 and (b) 10 nm Ti architectures on an absolute scale. The insets show 12-device average IV curves at the start and end of the soaks. Note the difference in units between the insets.

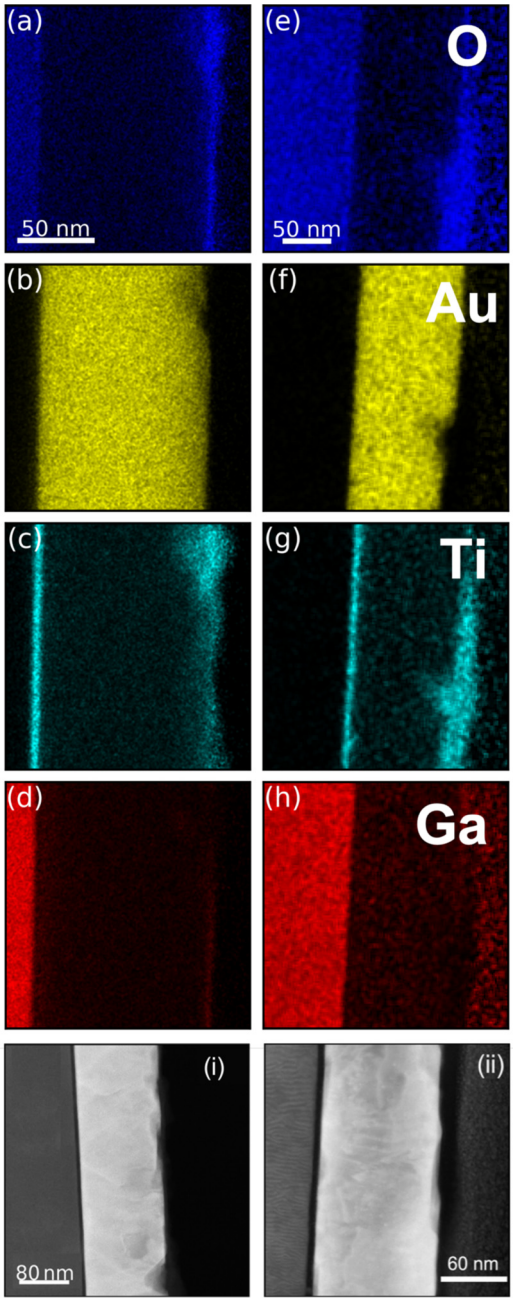

FIG. 5. EDS spectral images showing the atomic concentration of [(a)–(d)] the O, Au, Ti, and Ga content from the 5 nm sample, respectively, and [(e)–(h)] the O, Au, Ti, and Ga content from the 10 nm sample, respectively, with the substrate, Ti adhesion layer, Au layer, and capping material visible in the field of view. There are several similar features in both samples—Ga deposits on the Au in a thin even layer; and oxidized Ti migrates to the surface but in inconsistent clumps where there is a divot in the Au. Figures (i) and (ii) show STEM HAADF images of the 5 and 10 nm Ti samples, respectively, by atomic number contrast. Note the difference in Ti layer thickness consistencies between samples.

stable equilibrium. Contrasting this, the resistances of the 10 nm Ti devices showed more significant variability for the entirety of the soak, suggesting a wider range of conduction mechanisms or contact morphologies that might not achieve uniformity under these testing conditions.

C. TEM/EDS analysis

To understand this behavior, TEM lamellae were prepared from the 5 and 10 nm Ti samples that were repeatedly cycled between room temperature and 550 °C. An FEI Helios Nanolab 600i was used following standard focused ion beam (FIB) lift-out techniques and a 2 kV clean final step to minimize specimen ion beam damage.[31] The 5 nm specimen was capped with carbon via permanent marker before FIB lift out to protect the top surface, while the 10 nm specimen was capped only with electron-beam Pt GIS deposit followed by ion-beam Pt GIS deposit. The 5 nm specimen was lifted out parallel to the substrate (010) plane while the 10 nm specimen was lifted out parallel to (100). The thicknesses of both specimens were optimized for analytical and diffraction analyses, approximately 70–80 nm. TEM specimens were analyzed in an FEI Talos F200X Scanning Transmission Electron Microscope (STEM) at 200 keV. A camera length of 98 mm was used for STEM imaging with a spot size of 9 for micrographs and a spot size of 5 for Energy Dispersive Spectroscopy (EDS) mapping. Microprobe mode, a camera length of 98 mm, and a spot size of 7 were used for diffraction mapping. EDS spectral images were semi-quantitatively analyzed using Cliff-Lorimer methods and published k-factors.[32]

EDS spectral images of the two specimens (Fig. 5) reveal that in both samples, Ti and Ga have migrated through the gold layer to the top surface of the device. Gallium forms a very thin (<5 nm), uniform layer across the top Au surface, while Ti is inconsistently distributed across the Au surface with some thicker regions and some regions where very little Ti is present. Intensity profiles across this wide field of view indicate that this outer Ti layer is oxidized. Since sample preparation was carried out using a Ga FIB, contamination giving the impression of Ga presence cannot be discounted. However, the 5 nm Ti specimen provides good evidence that this Ga layer is real and not an artifact since the carbon capping contains no Ga and is sufficiently thick to protect the buried Au surface from any Ga implantation due to the milling process. Ga implantation from the side during sample thinning would be expected to be consistently dense throughout and mostly removed by the final 2 kV polish.

The bottom two panels of Fig. 5 show HAADF images of the 5 and 10 nm samples, contrasted by atomic number. The Ti contact appears as the thin dark layer in both TEM images. In both cases, the actual Ti layer thickness observed in the TEM cross sections is slightly smaller than the nominal target thickness (~8 nm for "10 nm" contact and 4.5–4.7 nm for "5 nm" contact), demonstrating the need for a high degree of precision when fabricating contacts. Additionally, the Ti layer of the 10 nm specimen shows slightly more thickness variation. The single-crystal Ga_2O_3 substrate underlying the 10 nm Ti sample (leftmost layer in the TEM image) has vertical striations most likely due to more aggressive specimen preparation curtaining the lamella or possibly due to

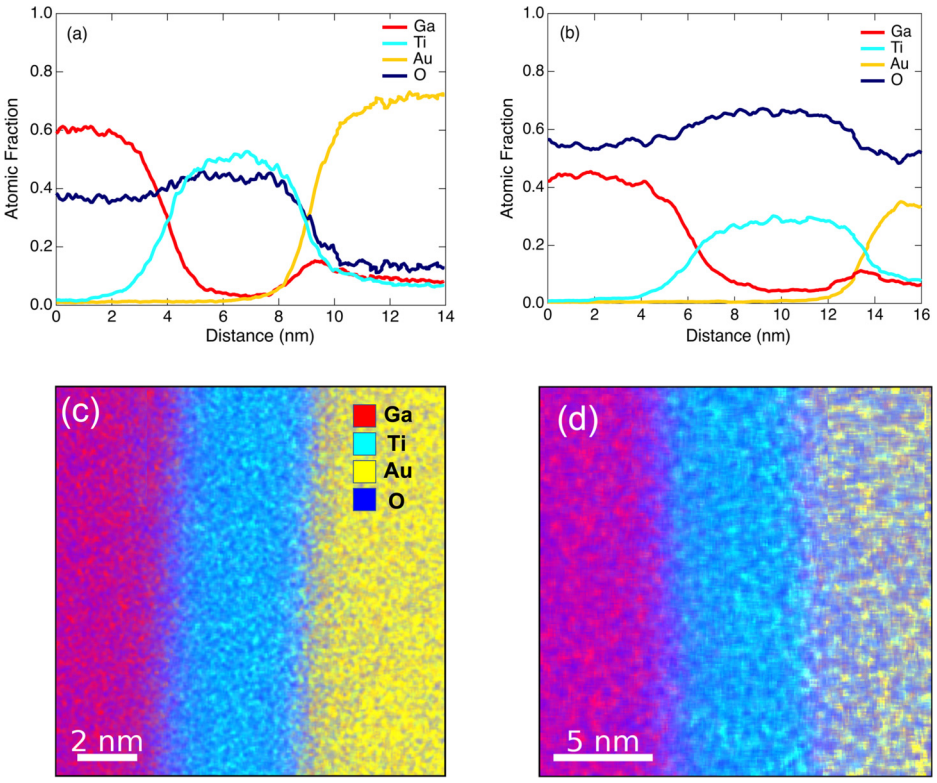

FIG. 6. (a) Semiquantitative atomic fraction EDS profile through the 5 nm Ti layer, showing moderate oxygen concentration in the Ti layer and Ga concentration present at the Ti-Au interface. (b) Semiquantitative atomic fraction EDS profile through the 10 nm Ti layer, showing significant oxygen concentration that approaches TiO_2 stoichiometry, in the Ti layer and Ga present at the Ti-Au interface. (c) EDS map showing distribution of Ga, Ti, Au, and O in 5 nm sample across the Ti layer region. (d) EDS map showing distribution of Ga, Ti, Au, and O in 10 nm sample across the Ti layer region.

differences in milling behavior of the differing crystallographic plane of the substrate.

Figure 6 shows intensity profiles of the EDS signal from the narrow field of view EDS maps at the Ti/Ga_2O_3 interfacial layer. In both specimens, the Ti layer is oxidized, with the 10 nm layer having a higher oxygen fraction than the 5 nm layer. The oxygen fraction in the 10 nm layer approaches the value expected for stoichiometric TiO_2, but the EDS map indicates significant oxygen content throughout the sample including in the gold layer; hence, conclusions related to the exact stoichiometry of the interfacial layer cannot be established with full certainty. Experimental differences such as changes in lamella thickness between the two samples can cause atomic fraction quantification irregularities. Additionally, as shown later, the Ti layer contains significant amounts of anatase TiO_2 so the actual Ti:O ratio is expected to be near 1:2 in both samples. The intensity profiles also show that there is Ga diffusion into the Ti layer and a small peak of higher Ga concentration between Ti and Au, further confirming that Ga is likely migrating through the samples, leading also to the Ga layer previously noted on the top Au surface of the samples.

D. Diffraction analysis

STEM-convergent beam electron diffraction pattern maps were taken of each sample aligned with the zone axes of the planes parallel to the lamellae, i.e., [100] and [0$\bar{1}$0] for the 10 and 5 nm samples, respectively. Using the experimental setup defined earlier, the focused probe diameter was sub-nm at the specimen. Representative diffraction patterns from each layer of each sample are shown in Fig. 7. The (001) substrate reflection is co-oriented with the surface in both cases. The titanium layer diffraction patterns were indexed against elemental Ti as well as rutile, anatase, and brookite TiO_2 phases. The best matches were the [310] and [201] anatase zones for the 10 and 5 nm samples, respectively. The anatase diffraction patterns of both samples indicate that {$\bar{3}$16} is co-oriented with the growth plane. The 10 nm sample shows a substantially more amorphous character (diffuse intensity rings around the direct beam) and diffraction spots from a secondary phase in the diffraction patterns of the Ti layer. In contrast, the substrate and the Au diffraction patterns lack any signs of amorphous character in either sample. The Au diffraction patterns reveal a textured polycrystalline structure. ⟨110⟩ zones make up most of the specimen with (111) generally oriented in the growth direction. The thin Ga layer indicated by EDS between Ti and Au was not evident in these diffraction maps.

Separate diffraction maps were taken from the TiO_x clusters on the top Au surface of the 5 nm sample only. This material is polycrystalline with grains on the scale of 1 nm. The grains are not epitaxial and only some diffraction patterns are on a discernable zone. Both rutile and brookite diffraction patterns are identifiable, but with significant amorphous character. However, this amorphous contribution could come largely from the protective capping added during sample preparation rather than the sample itself. Although not investigated, we presume that the TiO_x clusters

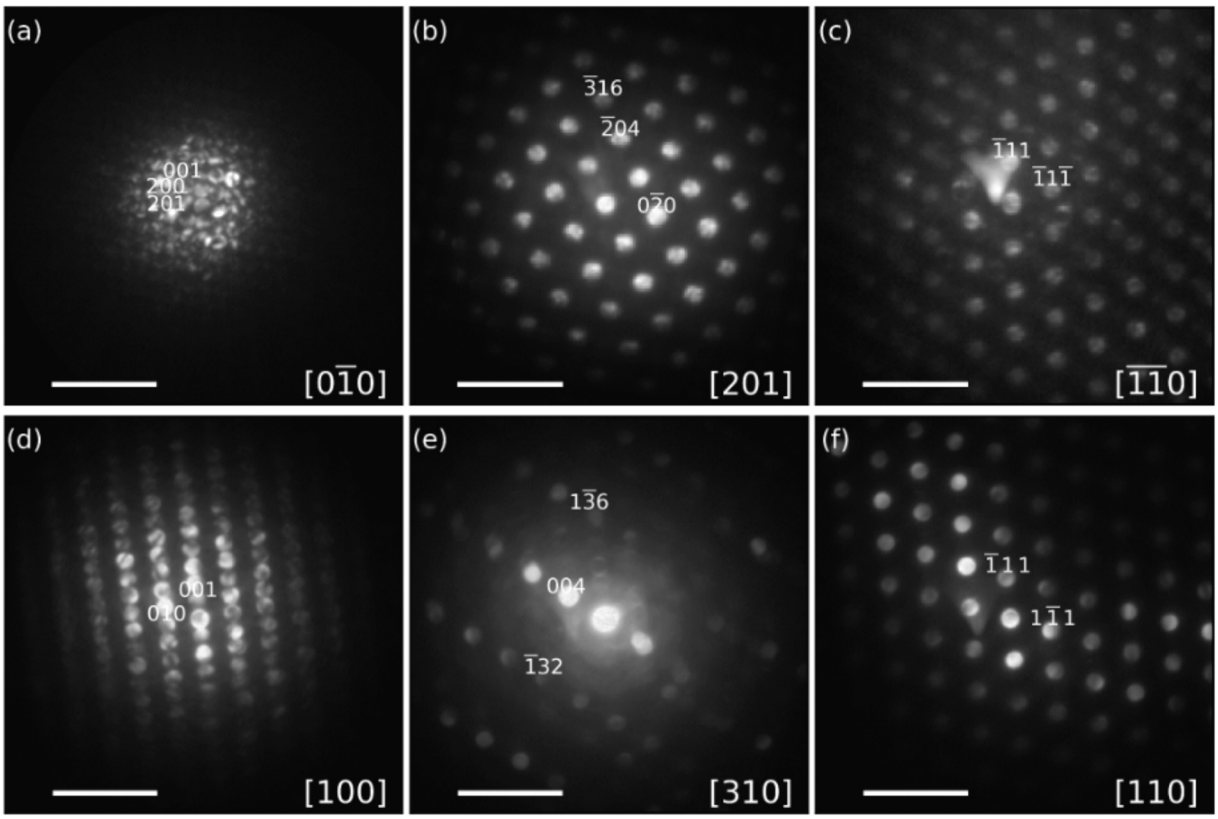

FIG. 7. Diffraction patterns from representative areas of each sample, 5 nm diffraction patterns in the top row and 10 nm in the bottom row. Scale bar is 10 $Å^{-1}$ in all panels. (a) Ga_2O_3 viewed on the [0$\bar{1}$0] zone axis. This diffraction pattern was recorded separately from the rest of the map to improve signal-to-noise and contrast around the closely spaced diffraction spots. (b) Ti layer identified as anatase TiO_2 phase viewed on the [201] zone axis with ($\bar{3}$16) co-oriented with the Ga_2O_3 (001) reflection. (c) Au [110] diffraction pattern with ($\bar{1}$11) reflection co-oriented with the Ga_2O_3 (001) reflection. (d) Ga_2O_3 viewed on the [100] zone axis. (e) Ti layer identified as anatase TiO_2 phase viewed on the [310] zone axis with (1$\bar{3}$6) co-oriented with Ga_2O_3 (001) reflection. Note the significant amount of amorphous character and secondary phases present in this diffraction pattern compared to the other patterns within this sample and the other sample. (f) Au [110] diffraction pattern with ($\bar{1}$11) co-oriented with Ga_2O_3 (001) reflection.

formed on the top Au surface of the 10 nm sample are similarly structured with a mix of rutile, brookite, and amorphous TiO_x.

The diffraction mapping results indicate epitaxial growth of anatase in both cases, but the 10 nm layer has some amorphous character and secondary phase and does not complete its transformation from elemental Ti to fully oxidized anatase TiO_2. The implied epitaxial relationship $(001)_{Ga_2O_3}||(\bar{3}16)_{TiO_2}$ and $[0\bar{1}0]_{Ga_2O_3}||[201]_{TiO_2}$ is at first improbable. First, the anatase [201] and [310] zones are not perpendicular; they are 78° separated. The anatase diffraction patterns off-zone from [310] do, however, appear very similar to [310] even at large mistilts. Simulations of diffraction patterns 90° perpendicular to $[210]_{anatase}$ (i.e., 12° from [310]), nevertheless, share many of the same reflections as [310] and include the ($\bar{3}$16) reflection. So, the 10 nm Ti diffraction pattern is only close to [310] and not fully on zone.

We also consider the oxygen-containing $(\bar{3}16)_{anatase}$ planes relative to the Ga_2O_3 substrate, shown in Fig. 8. Both planes have a similar offset dumbbell motif; the O–O spacing in the [210] direction of anatase TiO_2 as well as the [010] direction of Ga_2O_3 is approximately 3.1 Å. The O–O spacing between adjacent dumbbells is also similar at 6.2 and 6.4 Å for TiO_2 and Ga_2O_3, respectively. There is a reasonable atomistic matching pattern to explain this epitaxial growth pattern and diffraction evidence supporting this co-orientation in both specimens and viewed in separate directions.

To summarize, TEM analysis shows that in both the 5 and 10 nm cases, the Ti layer forms epitaxial anatase phase TiO_2; Ti migrates to the surface and forms unevenly distributed titanium oxide patches; and Ga also migrates to both the Ti-Au interface and the surface and forms a thin, evenly distributed layer. The key difference between the two specimens is that the 5 nm anatase layer is fully crystalline whereas the 10 nm anatase layer contains a substantial amount of amorphous TiO_x second phase that affects the performance of the Ohmic contact.

IV. SUMMARY AND CONCLUSIONS

We have successfully fabricated Ohmic contacts to (001) Sn: Ga_2O_3 using an ultrathin layer of Ti (5 nm) with a Au capping

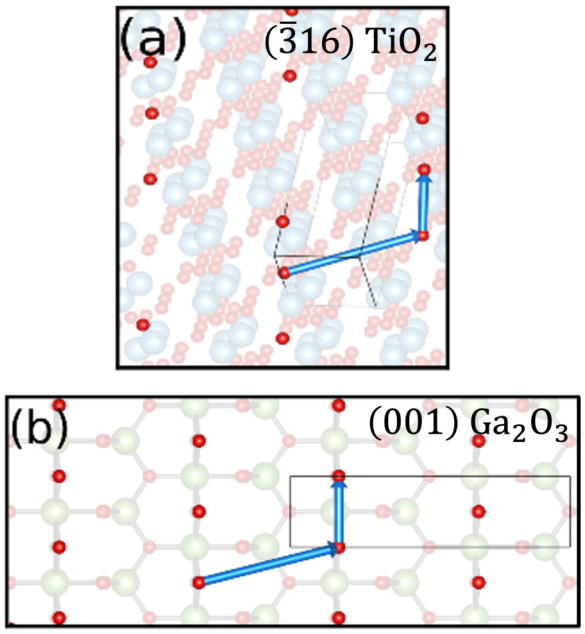

FIG. 8. Cross sections of (a) anatase TiO_2 ($\bar{3}16$) and (b) Ga_2O_3 (001) planes showing oxygen sublattice in bright red and semi-transparent underlying crystal structure. The corresponding geometry for the possibility of epitaxial growth is marked with blue arrows. The crystals are oriented in the proposed epitaxial relationship.

layer (100 nm). These contacts show remarkable stability and excellent Ohmic performance after both extensive thermal cycling between 25 and 550 °C in N_2 and long-term thermal soaking at 600 °C for >500 h under vacuum conditions. Through TEM analysis, we show that the 5 nm Ti layer is sufficiently thin that it completely transforms to an epitaxial, highly conductive anatase titanium oxide layer, which provides a stable Ohmic contact. In contrast, the 10 nm Ti layer does not fully react during thermal cycling, leading to a partially amorphous TiO_x layer that does not enable a stable Ohmic contact. Additionally, the 10 nm Ti design showed both larger resistances and greater variability in performance during a similar >300-h soak at 600 °C. While Ti is found on the outer surface of the Au layer in both 5 and 10 nm Ti samples, the homogeneity of the interlayer at the Ga_2O_3 interface appears to have a greater impact on the overall performance and stability of the contact. Integration of this ultrathin Ohmic contact design will aid development of high-temperature devices, by specifically shifting research focus to stable rectifying interfaces, p-type heterojunction materials, and other functional layers.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

William A. Callahan: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Edwin Supple:** Data curation (lead); Formal analysis (lead); Methodology (equal); Visualization (lead); Writing – review & editing (equal). **David Ginley:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Writing – review & editing (equal). **Michael Sanders:** Conceptualization (equal); Methodology (equal). **Brian P. Gorman:** Methodology (equal); Writing – review & editing (equal). **Ryan O'Hayre:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Writing – review & editing (equal). **Andriy Zakutayev:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Project administration (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material (Ref. 33).

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