Multiphysics Co-Optimization Design and Analysis of Double-Side Cooled Silicon Carbide-Based Power Module

Preprint

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National Renewable Energy Laboratory

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MULTIPHYSICS CO-OPTIMIZATION DESIGN AND ANALYSIS OF DOUBLE-SIDE COOLED SILICON CARBIDE-BASED POWER MODULE

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ABSTRACT

With the rapid growth of Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs), much more rigorous design targets have been set for automotive power electronics, including high power density, high reliability, and low cost. Novel power module and inverter technologies based on wide bandgap (WEG) semiconductors have been developed to meet these design targets, while providing optimal power semiconductor operating temperature and promising thermomechanical performance. Compared with conventional cooling techniques which are normally applied only on one side of power module, double-side cooling approach is now believed to be the solution to enable high power density and low thermal resistance of WEG semiconductor-based power electronics.

In this work, we develop a three-phase power module that is double-sided cooled using dielectric fluid jet impingement. In each phase, four silicon carbide (SiC) power semiconductors are bonded to copper busbars without electrical insulation layers. A finite element analysis (FEA) model is created for thermal and thermomechanical analysis. Based on FEA modeling results, we select particular dimensions for a parametric study to optimize thermal and mechanical performance. Using a multi-objective genetic algorithm (MOGA)-based optimization method, we have minimized the maximum junction temperature and thermal stresses within the power module. The multiphysics co-optimization approach has enabled an efficient design process of power modules with greatly reduced computational cost, as compared to conventional processes that rely on exhaustive numerical simulations and iterations.

Keywords: Power electronics, multiphysics, optimization, double-sided cooling, finite element analysis

1. INTRODUCTION

Rigorous design targets of high-power density power electronics for automotive applications have motivated the popularity of wide bandgap (WBG) semiconductors. enormous efforts have been devoted to developing packaging architectures to unlock their potentials to permit high operating temperature, high power density and high switching frequency [1]. The temperature limit of WBG semiconductors around 250 °C has enabled the possibility of less complicated cooling systems, but also has necessitated the redesign of power module packages and thermal management systems (TMSs) to accommodate such a high temperature. Innovative package design and cooling strategies are discussed to lower the junction temperature to allow for optimized performance and reliability [2]. Luo *et al.* [3] has reviewed advancements with the packaging design of SiC power modules from commercial off-the-shelf (COTS) products to research efforts, covering three aspects: module layout and structures, packaging materials and module integration trend. Joshi *et al.* [4] summarized thermal packaging of automotive power electronics and introduced emerging work/trends on advanced packaging options for SiC power modules from three areas: die-attach, thermal interface materials (TIMs) and high heat flux cooling.

Traditional power module packages have a seven-layer configuration, including heat sink, baseplate, substrate, device and TIMs between these layers. During regular operations, excessive heat from the active region in device transfers from the bottom of device, through multiple layers, and eventually dissipates into coolant or ambience. Thermal management of such configuration is greatly influenced by the thermal resistance from the interior solid layers. A review from National Renewable Energy laboratory (NREL) has compared compares the performance of current electric-drive vehicle power electronics TMSs [5]. Schematics of typical power module configuration in EVs are shown in Figure 1. In these packages, thermal interface material (TIM) layers commonly contribute the highest thermal resistance, while the substrate also yields large thermal resistance, due to the low thermal conductivity of the insulative materials. Therefore, novel

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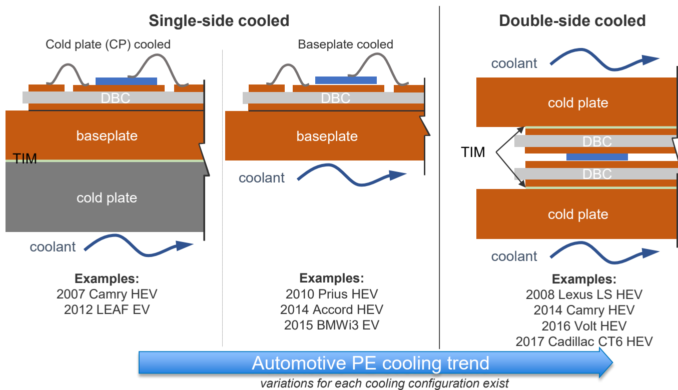

FIGURE 1. Schematics of typical power module configurations. Automotive examples are listed below the schematics. [5]

package architectures are necessary to shorten the thermal pathway from junction to ambient to enhance overall thermal performance. Improvements have been identified in a commercial insulated gate bipolar transistor (IGBT) power module by integrating the baseplate with heat sink by eliminating the TIM that attaches the power module to heat sink [5]. Compared to single-side cooled package, trends are observed to use both sides of power modules for cooling. Double-side cooled packages have been studied proven to have significantly reduced the thermal resistance and permits higher heat loss [6,7].
Selection of coolants also has tremendous impact on power electronic package and associated thermal management performance. While cooling techniques using conventional coolants, such as water and water-ethylene glycol (WEG), cannot provide high heat transfer rate for systems of high power density, utilization of dielectric fluids for cooling has become a viable solution to achieve significantly higher heat transfer coefficient (HTC) [8–10]. In addition, because of the electrical insulation characteristic, dielectric fluid-based cooling approach allows redesign of package without insulation layers and thus brings coolant closer to heat sources. Elimination of solid insulative layer, such as direct-bonded copper, helps to improve the thermomechanical performance and reliability [11].

Therefore, in this work we have designed a compact silicon carbide-based three-phase power module that uses dielectric fluid-based jet impingement cooling technique to cool both sides. To ensure that the system is thermally effective and

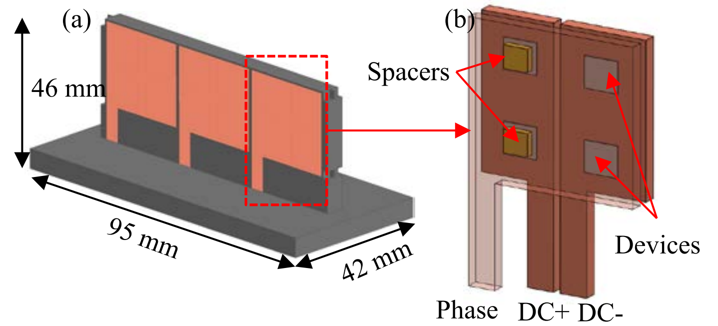

FIGURE 2. (a) Computer-aided design (CAD) model of the conceptual double-sided cooled power module, and (b) layout of devices/spacers inside one phase (the phase busbar is set to be transparent for better presentation).

reliable, we defined multiple objectives to accomplish in the power module deisgn [16]. To avoid the conventional exhaustive parametric iterations in power module design, we have implemented a numerical approach that aims to optimize multi-physical aspects of the power module. We first develop a power module design that consists of multiple semiconductors and interconnectors, as a “baseline” with initial dimensions. Then we create a finite element analysis (FEA) model of the power module and conduct multiphysics study to compute thermal and thermomechanical characteristics. Based on the parameters and results of the “baseline” design, we utilize a multi-objective optimization approach to simultaneously accomplish various design goals. In section 2, 3 and 4, we will give a brief review of the power module design and FEA modeling procedure. These sections will be succeeded by results and discussions on the multiphysics FEA analysis and optimization process in Section 5.

2. DOUBLE-SIDE COOLED POWER MODULE

Nowadays, a major challenge in power electronics design is efficient TMS for high power density and fast-switching operations. The objective of this work is to develop a high-performance double-side cooled (DSC) SiC-based power module with low junction-to-coolant thermal resistance and induced thermal stress. Figure 2(a) shows the conceptual DSC module which has an overall dimension of 95 mm × 42 mm × 46 mm and consists of three phases packaged by molding plastic. There are no electrical insulation layers such as direct bonded

Table 1. Physical properties of the materials in the double-side cooled power module.

	Copper [12]	**SiC** [13]	**Sintered Silver** [14]	**Molding** [15]
Thermal conductivity (W/m·K)	390	Temperature-dependent	350	0.3
Density (kg/m^3)	8933	3100	10400	1350
Coefficient of thermal expansion (10^{-6}/ºC)	17	4.5	20	40
Tensile strength (MPa)	210	137	61	60
Young’s modulus (GPa)	115	410	4	10
Passion’s ratio	0.31	0.18	0.37	0.40

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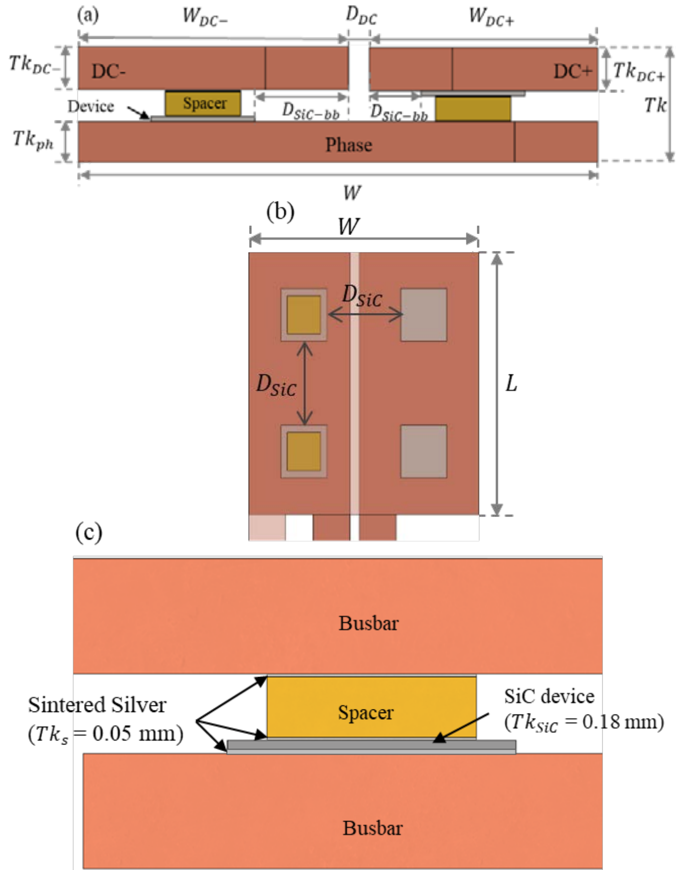

FIGURE 3. Schematic of the power module CAD model, showing the definition of geometric parameters in one phase: (a) sectional view, (b) top view, and (c) magnification of the package architecture.

copper (DBC) in the package because dielectric fluid-based jet impingement is intended to be used to cool the SiC devices. As illustrated in Figure 2(b), each phase has four SiC devices - two of them are bonded to DC+ busbar using sintered silver, and other two are bonded to the phase busbar in a "flip-over" manner. Copper (Cu) spacer is attached to the top surface of each device using sintered silver paste to keep safe clearance distance between electrical interconnectors. In this design, Cu spacers have a footprint of 3.63 mm × 3.63 mm, and a thickness of 1.5 mm, which is subject to parametric study. The SiC devices have a dimension of 5 mm × 5 mm × 0.18 mm, with a 0.01-mm layer to represent the active region in FEA simulation. Sintered silver paste for die attachment and substrate attachment all have a thickness of 0.05 mm. Material properties to be used in the multiphysics model are summarized in Table 1.

3. MULTIPHYSICS ANALYSIS OF DSC POWER MODULE

Thermal stresses and induced deformation are the main causes of reliability issues in power electronics. In this DSC power module design, SiC devices are bonded to copper interconnectors which are directly cooled by dielectric fluid jet impingement. The mismatches in coefficient of thermal expansion (CTE) between dissimilar materials can lead to performance degradation or failure. To study the thermomechanical characteristics, we developed a FEA model of the DSC power module based on the CAD drawing in Figure 2. To facilitate the optimization procedure, we defined the major dimensions in power module as shown in Figure 3. When we created the CAD model in SOLIDWORKS, dimensions that are subject to parametric study in FEA were named with a prefix "DS_". If the value of a parameter with prefix "DS_" is altered in ANSYS, it will interface with the CAD tool to update dimensions and new CAD model will be imported into ANSYS. This "communication" mechanism enables the exploration of a large number of design points without laborious manual alteration of input values. Table 2 reports the values of all geometric parameters in the baseline design. There are six parameters given the prefix "*DS_*" in SOLIDWORKS: Tk_{ph}, Tk_{DC+}, Tk_{DC-}, W_{ph}, W_{DC+} and W_{DC-}. In addition, there will be geometric constraints to be considered when determining the bounds of the six parameters in optimization study, which will be discussed in Section 5.

TABLE 2. Summary of the geometric parameter definitions and values used in baseline design.

Geometric parameters	**Symbol**	**Value (mm)**
Length of one phase	L	25
Width of one phase	W	25
Thickness of one phase	Tk	5.28
Thickness of SiC device	Tk_{SiC}	0.18
Thickness of sintered silver layer	Tk_{ss}	0.05
Length of phase busbar	L_{ph}	25
Width of phase busbar	W_{ph}	25
Thickness of phase busbar	Tk_{ph}	2
Length of DC+ busbar	L_{DC+}	25
Width of DC+ busbar	W_{DC+}	13
Thickness of DC+ busbar	Tk_{DC+}	2
Length of DC- busbar	L_{DC-}	25
Width of DC- busbar	W_{DC-}	11
Thickness of DC- busbar	Tk_{DC-}	2
Thickness of spacer	Tk_s	1.05
Distance between devices	D_{SiC}	8
Distance between DC busbars	D_{DC}	1
Distance between device and busbar edge	D_{SiC-bb}	≥ 1

A mesh-independence study was conducted before the multiphysics FEA simulation. We generated meshes using various grid sizes, and the total number of nodes varies from 1 million to 20 million, as shown in Figure 4. We refined the

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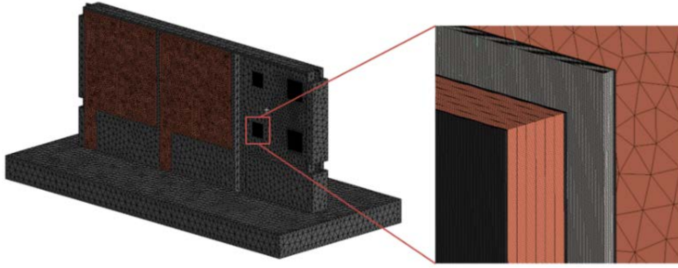

FIGURE 4. Meshing of the power module, with a zoomed-in view of the interior packages.

meshes in thin bodies, such as sintered silver and SiC devices, to capture the thermomechanical behaviors. FEA simulation was then carried out with different meshes and the variability profiles of temperature and stress with the number of nodes are exhibited in Figure 5. It is observed that when the total number of nodes is less than 5 million, both results show rapid decrease with increasing number of nodes. When the number of nodes is more than 5 million, its impact on temperature and stress becomes insignificant, with nearly flat profile. Therefore, we selected a grid size that generates 3.8 million nodes to mesh the power module for FEA analysis and optimization in this work.

4. OPTIMIZATION METHODOLOGY

To seek dimensions that yield optimal thermal and mechanical performance, we employed a multiple-objective optimization approach. After the numerical model of the baseline design was solved, the parameter set and results were transferred to a response surface optimization tool. In this tool, we selected input parameters and assigned lower and upper bounds to each one of them. Then based on the inputs parameters and associated variability bounds, we applied design of experiments (DOE) method to create a series of design points, each of which is connected to a multiphysics FEA simulation. The purpose of DOE method is to establish a data base with sufficient design points to represent the entire design space. With DOE method, a correlation between the inputs and outputs is created,

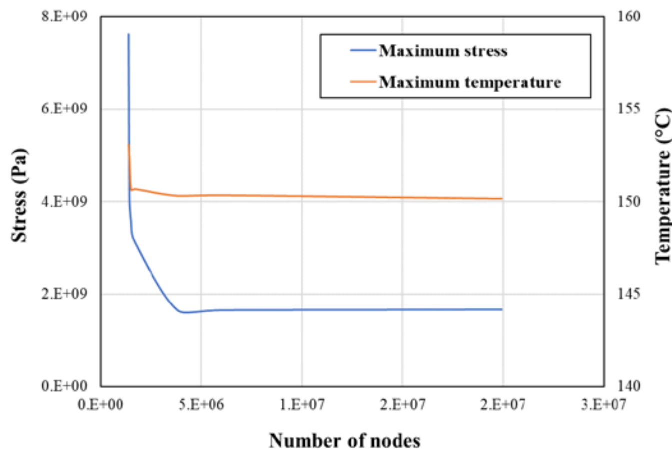

FIGURE 5. Variation of maximum temperature and stress with number of nodes.

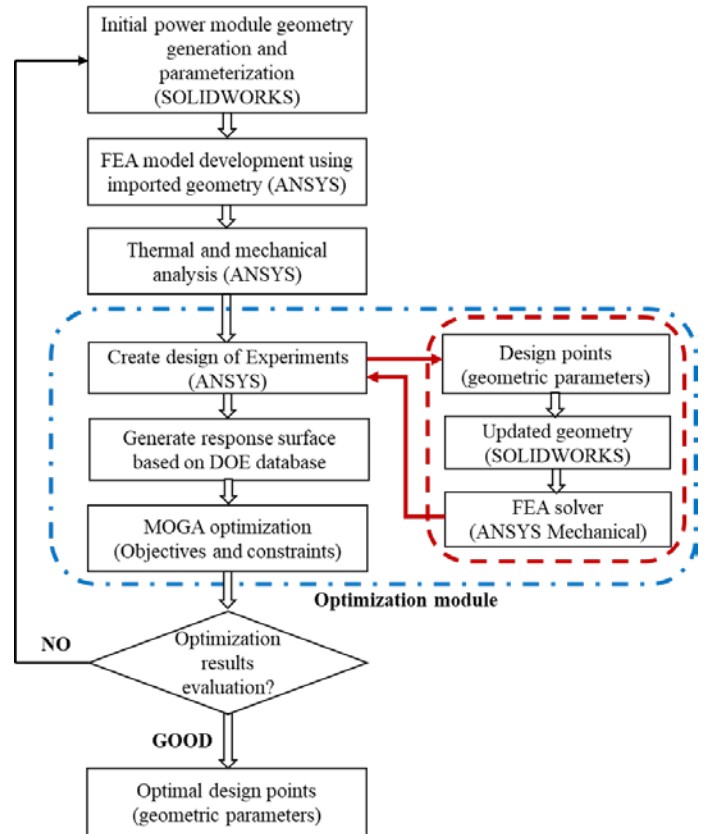

FIGURE 6. Flowchart of the multiphysics analysis and optimization procedure.

and this correlation is defined as the response surface. There are various DOE schemes to generate design points - Central Composite Design (CCD), Box-Behnken Design, Optimal Space Filling Design, Custom + Sampling, Sparse Grid Initialization, and Latin Hypercube Sampling Design. Details and selection criteria can be referred to ANSYS manual. In this study, we chose the Optimal Space Filling scheme, which permits independence between the number of samples and the number of input parameters, leading to a flexibility to define sample points based on available computational resources. Optimization of parameter of interest was achieved using the Multi-Objective Genetic Algorithm (MOGA), which yields optimal design points by randomly searching the entire design space. MOGA is commonly used due to the advantages of fast convergence, strong searching ability, and convenience to set solution model, which make it very suitable for solving multi-objective optimization problems.

Figure 6 is a flowchart of the design and optimization procedure, the steps of which include: (1) create a power module model with initial dimensions and specify variables for parametric study; (2) import the CAD model into FEA tool and convert it into a numerical model; (3) set modeling parameters (heat generation, boundary conditions, *etc.*) and conduct thermal and thermomechanical analyses; (4) transfer the inputs and outputs from

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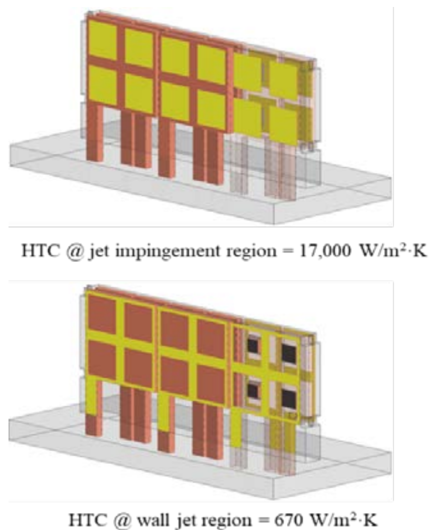

FIGURE 7. Convective boundary conditions at the different regions of the power module. Fluid temperature is 70 ºC.

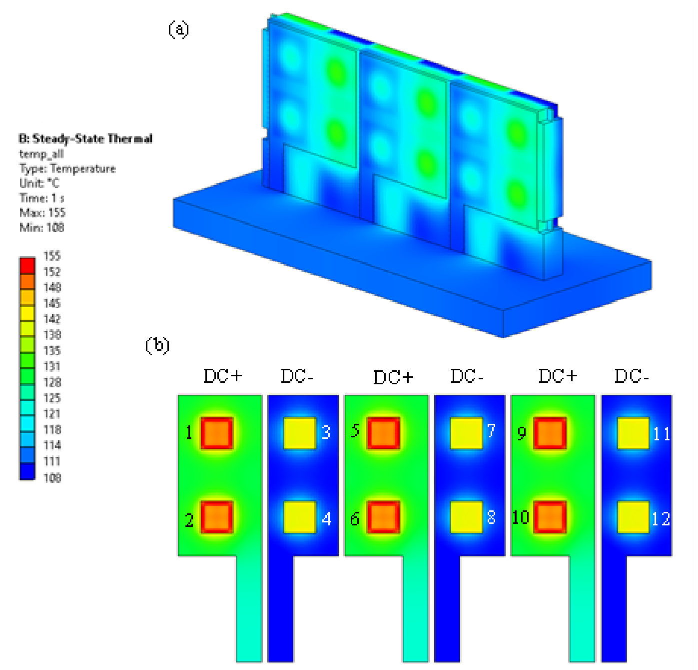

FIGURE 8. (a) Temperature contour of entire power module, and (b) temperature contour of 16 devices.

baseline case into the optimization tool and apply DOE method; (5) Use the solutions of design points to generate the response surfaces; (6) conduct optimization to seek optimal solutions – if the optimization results meet design goals, the process is completed, otherwise, return to step (1) to make necessary revisions in power module design and repeat the process until an optimal design is accomplished.

5. RESULTS AND DISCUSSION

5.1 Thermal analysis results

Before performing multi-objective optimization, we conducted a multiphysics FEA study of the baseline design shown in Figure 1. Materials used in the FEA simulation is listed in Table 1, and dimensions of the parts in power module are reported in Table 2. To represent the active region in SiC device, a thin layer of 0.01 mm thickness was created with a heat generation of 179 W, yielding a power density of 7.2×10^{11} W/m^3. Although dielectric fluid-based jets impingement is intended to be used to cool the DSC power module, we did not include a manifold or fluids in this work. Instead, assuming that each device is dedicatedly cooled by two jets from the opposite sides, we imprinted eight 10 × 10 mm squares over the interconnector surfaces with prescribed HTC to mimic the jet impinged area. As seen in Figure 7, on each phase busbar, there are four squares highlighted in yellow, each of which represents a jet impingement over a discrete SiC device. The HTC applied at the highlighted area is 17,000 W/m^2·K and fluid temperature is 70 ºC. There are another four squares imprinted on the surface of DC busbars with the same HTCs, as shown in Figure 7 after changing the transparency. In jet impingement cooling, the highest heat transfer rate occurs at the stagnation region, therefore, in wall jet region shown in Figure 7 (b), we used as a significantly lower HTC as 670 W/m^2·K with a fluid temperature of 70 ºC. HTC values at stagnation region and wall region were computed using a preliminary computational fluid dynamics (CFD) analysis, which is not discussed in this work.

The steady-state thermal FEA was performed on the entire power module to compute the maximum junction temperature of all 12 devices. Modeling results are presented in Figure 5, including temperature contours of entire power module and discrete devices. The maximum junction temperature of all devices for the steady-state condition was found to be 155 ºC with the devices attached to DC+ busbars, and minimum junction temperature was observed to be at the devices attached to phase busbars. As illustrated in Figure 3, in each phase, two devices are bonded to DC+ busbar by sintered silver paste, while another two being bonded to phase busbar. To be more specific, if we index the 12 devices as noted in Figure 8(b), devices #1, #2, #5, #6, #9, and #10 are directly bonded to DC+ busbar, and the rest six devices are directly bonded to phase busbars. Obviously, devices attached to DC+ busbar have significantly reduced surface area for convective heat transfer, as compared to the devices attached to phase busbars, leading to relatively higher junction temperature. Both maximum and average junction temperatures of the 16 devices are reported in Table 3, indicating that devices in three phases show analogous temperature distribution because of the nearly symmetric structure. The variation of maximum junction temperature for all devices is about 5 ºC, which is a parameter to be studied in the optimization process.

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TABLE 3. Maximum and average junction temperatures of the 16 SiC devices.

Device	Substrate	$T_{j,\,max}$ (°C)	$T_{j,\,average}$ (°C)
1	DC+	154.1	149.1
2	DC+	154.5	149.6
3	*Phase*	149.7	144.1
4	*Phase*	149.7	144.3
5	DC+	154.0	149.1
6	DC+	154.7	149.6
7	*Phase*	149.6	144.1
8	*Phase*	149.7	144.3
9	DC+	154.1	149.1
10	DC+	154.4	149.5
11	Phase	149.5	144.1
12	Phase	149.8	144.3

5.2 Thermomechanical analysis results

Once the thermal analysis is completed, the temperature profile of power module was imported into a static thermomechanical model as the thermal load, to determine the stress profile within the module. Material properties used for analysis are reported in Table 1. A 3-2-1 boundary condition was applied to the power module to prevent rigid-body motion without inducing deflections. The 3-2-1 constraint is to prevent all three translational freedoms at the first vertex, two translational freedoms at second vertex, and one translational freedom at the third vertex, as illustrated in Figure 6. In addition, we estimated the exerted force at interconnector surface by the momentum of jet flow. We first computed the dynamic pressure P ($P = 0.5 \cdot \rho \cdot v^2$, in which ρ is fluid density and v is jet velocity at exit). Then we computed the normal force exerted on the impinged surface, as $F = P \cdot A$, wherein A is the area of jet exit. From a preliminary study of the jet impingement-based cooling system, each of the jet slot is about 1.75 mm wide and 10 mm long, and jet velocity at nozzle exit is 0.35 m/s. Thus, the exerted force was determined to be 1.2×10^{-3} N and was imposed along the normal direction of the imprinted square faces where HTC of 17,000 W/m²·K were assigned, as shown in Figure 9.

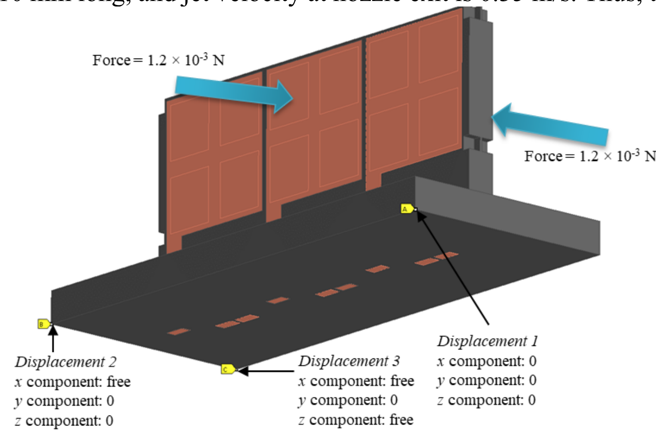

FIGURE 9. Boundary conditions applied in thermomechanical FEA analysis.

Figure 10 shows the results of thermomechanical FEA study, including von-Mises stress and deformation. In general, the mechanical design of power module aims to yield stress lower than the material yield tensile strength to keep the module within the elastic regime. In Figure 10(a) we plotted the von-Mises stress contour of the entire module, which shows that the maximum stress of 3.4×10^9 Pa occurs at the edge of SiC device. It can be explained by the heat dissipation from SiC device to substrate and spacer. The stress in copper parts shown in Figure

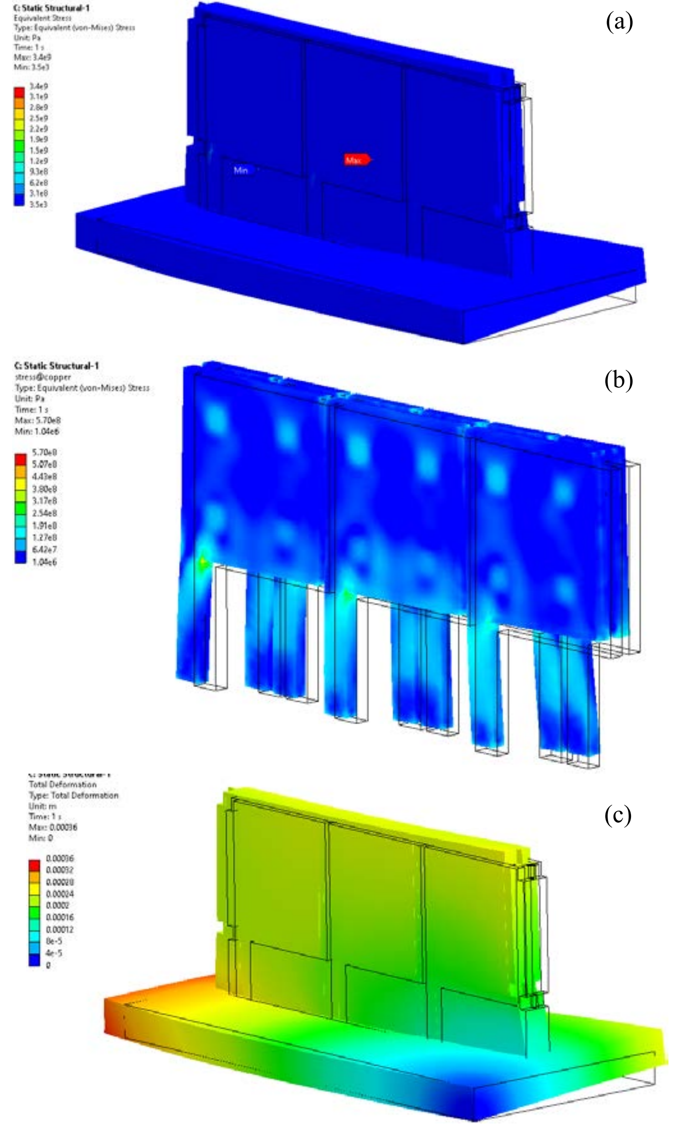

FIGURE 10. (a) von-Mises stress contour of entire power module, (b) von-Mises stress contour of copper parts, and (c) deformation contour of the power module.

TABLE 4. Bounds and constraints of DOE method input parameters.

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Symbol	Lower bound (mm)	Upper bound (mm)	Design constraints
$\boldsymbol{Tk_{ph}}$	1.5	2.55	$Tk_{DC+} = Tk_{DC-}$
$\boldsymbol{W_{DC+}}$	11	13	$T_{ph} + Tk_{DC+} + Tk_s = 5.05$ mm
$\boldsymbol{Tk_{DC+}}$	1.5	2.55	$W_{DC-} + W_{DC-} = 24$ mm
$\boldsymbol{W_{DC-}}$	11	13	
$\boldsymbol{Tk_{DC-}}$	1.5	2.55	
$\boldsymbol{Tk_s}$	1	2.05	

10(b) varies from 1.0×10^6 to 5.7×10^8 Pa, and the maximum stress is found to be at the corners of busbars. Stress in copper parts is more than one order of magnitude lower than that in SiC devices, which is probably attributed to the thermal spreading effect in spacers and busbars, hence relieving the thermal stress accumulation in copper. It is noted that the maximum stress of SiC devices is higher its yield strength, leading to a factor of safety less than 1, suggesting a possibility of material yielding. In addition, the maximum stress of copper parts is at the same order of magnitude as its yield strength, therefore the yield factor of safety is close to 1. Deformation in Figure 10(c) indicates that the maximum deformation due to thermal stress is about 0.4 mm, while most of power module has a deformation less than 0.1 mm.

5.3 Design and experiments and optimization results

From the thermal and thermomechanical FEA study of the baseline design, we learnt that the maximum junction temperature is 155 ºC, with a 5 ºC variation of 12 devices. The maximum stress in coppers is higher than the yield strength. Therefore, we utilized the response surface optimization method in ANSYS Workbench to seek geometric parameters that can improve both thermal and mechanical performance. As described in Section 3, we first chose specific parameters as inputs, and assigned variability bounds to each of them to create a series of design points. In this work, there are six parameters set to be alterable - Tk_{ph}, W_{DC+}, Tk_{DC+}, W_{DC-}, Tk_{DC-}, and Tk_s, as reported in Table 4. Although there are six parameters, we did not apply all of them as inputs because of design constraints, including

(1) DC+ and DC- busbars have the same thickness;

(2) because the total thickness of each phase is 5.38 mm, and device and sintered silver layer have fixed thickness of 0.18 mm and 0.05 mm, respectively, therefore the total thickness of busbars and sinter silver layer equals 5.05 mm;

TABLE 5. Optimization objectives and constraints.

Parameters	Objectives	Constraints
$\boldsymbol{T_{j,max}}$	Minimize	None
$\boldsymbol{\Delta T_{jmax}}$	Minimize	None
$\boldsymbol{\sigma_{max}}$	Minimize	None
$\boldsymbol{\sigma_{max,Cu}}$	Minimize	None
$\boldsymbol{Tk_{ph}}$	None	1.5 mm $\leq Tk_{ph} \leq$ 2.55 mm

(3) because a 1-mm gap between DC busbars must be maintained, the total width of DC+ and DC- busbars equals 24 mm.

With imposed constraints, we selected W_{DC-}, Tk_{DC-}, and Tk_s, as the input parameters in the DOE method. Output parameters include maximum junction temperature ($T_{j,max}$), maximum junction temperature difference (ΔT_{jmax}), maximum von-Mises stress (σ_{max}) of power module, and maximum von-Mises stress of coppers ($\sigma_{max,Cu}$). Then thermal and thermomechanical analyses were performed at each design point to generate a date base that contains defined inputs and modeling outputs. The response surface was created using genetic aggregation model. The goodness of fit was measured by computing the room mean square (RMS) error and coefficient of determination values.

Response surface optimization provides a pathway to optimize multiple parameters under various constraints. In this study, we have set both objectives and constraints in the optimization process. The objectives include minimization of multiple parameters - $T_{j,max}$, ΔT_{jmax}, σ_{max} and $\sigma_{max,Cu}$, and the only constraint is the variability bounds of phase busbar thickness, as summarized in Table 5. Using the MOGA method, the optimization results are reported and compared with baseline design in Table 6. The optimized power module has a $T_{j,max}$ of 153.7 ºC and temperature variation of devices, ΔT_{jmax}, of 4.7 ºC, both of which are slightly lower than the baseline design. Thermal stress in optimized case presents more significant decrease, 14% for σ_{max} and 8% for $\sigma_{max,Cu}$, respectively. In summary, improvements with both thermal and mechanical performance for optimized design is not significant, which suggests that baseline design already has nearly optimal thermal and mechanical performance with the initial design parameters, which have minor variable margin in this work. Future work includes revision of the interconnectors form factor and surface features to reduce the thermal stress and increase the factor of safety.

TABLE 6. Comparison of the baseline and optimized designs.

Parameters	Baseline design	Optimized design
$\boldsymbol{Tk_{DC+}}$ (mm)	2	1.7
$\boldsymbol{Tk_{DC-}}$ (mm)	2	1.7
$\boldsymbol{Tk_{ph}}$ (mm)	2	2.5
$\boldsymbol{Tk_s}$ (mm)	1.05	1.0
$\boldsymbol{W_{DC+}}$ (mm)	13	12.8
$\boldsymbol{W_{DC-}}$ (mm)	11	11.2
$\boldsymbol{T_{j,max}}$ (ºC)	155	153.7
$\boldsymbol{\Delta T_{jmax,Cu}}$(ºC)	5.15	4.7
$\boldsymbol{\sigma_{max}}$ (Pa)	3.4×10^9	2.9×10^9
$\boldsymbol{\sigma_{max,Cu}}$ (Pa)	5.8×10^8	5.3×10^8

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6. CONCLUSION

In this work, we applied a multiphysics optimization procedure to design a DSC power module with dielectric fluid jet impingement cooling system. The DSC power module has three phases, each of which consists of four SiC devices and features "ceramic-less" configuration. Cooling of power module is achieved by impinging dielectric fluid directly on electrical interconnectors. In the thermal and thermomechanical FEA simulations, we applied a constant HTC over specific area to imitate the jet impingement cooling. Temperature profile of baseline power module shows a maximum junction temperature of 155 ºC, with a 5 ºC variation of 12 devices. Induced thermal stress in SiC devices is higher than yield stress, leading to low safety factor. We then implemented used a response surface optimization approach to simultaneously minimize the temperature and thermal stress, for improving the performance of power module. Selective geometric parameters were used as inputs in the DOE method to establish a design space, and results of DOE method were then applied to define a correlation between inputs and outputs. Based on the correlation, we adopted a MOGA-based optimization to achieve multiple design goals. The optimization results show slight improvement as compared to the baseline design, due to a fact that the dimensions in baseline design have just minor design margins from the manufacturability perspective. Future work includes revision of the interconnectors form factor and surface features to reduce thermal stress and increase the factor of safety, while maintaining an optimal thermal performance.

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REFERENCES

[1] Seal, S., and Mantooth, H., 2017, "High Performance Silicon Carbide Power Packaging—Past Trends, Present Practices, and Future Directions," Energies, **10**(3), p. 341.

[2] Wang, P., McCluskey, P., and Bar-Cohen, A., 2013, "Hybrid Solid- and Liquid-Cooling Solution for Isothermalization of Insulated Gate Bipolar Transistor Power Electronic Devices," IEEE Transactions on Components, Packaging and Manufacturing Technology, **3**(4), pp. 601–611.

[3] Huazhong University of Science and Technology, and Chen, C., 2017, "A Review of SiC Power Module Packaging: Layout, Material System and Integration," CPSS Transactions on Power Electronics and Applications, **2**(3), pp. 170–186.

[4] Broughton, J., Smet, V., Tummala, R. R., and Joshi, Y. K., 2018, "Review of Thermal Packaging Technologies for Automotive Power Electronics for Traction Purposes," Journal of Electronic Packaging, **140**(4).

[5] Moreno, G., Narumanchi, S., Feng, X., Anschel, P., Myers, S., and Keller, P., 2021, "Electric-Drive Vehicle Power Electronics Thermal Management: Current Status, Challenges, and Future Directions," Journal of Electronic Packaging, **144**(1).

[6] Nakatsu, K., Nishihara, A., Sasaki, K., and Saito, R., 2013, "A Novel Direct Water and Double-Sided Cooled Power Module and a Compact Inverter for Electrified Vehicles," *2013 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1–6.

[7] Gerbsch, E. W., 2010, "Fluid Cooled Semiconductor Power Module Having Double-Sided Cooling."

[8] Tuma, P. E., 2011, "Design Considerations Relating to Non-Thermal Aspects of Passive 2-Phase Immersion Cooling," IEEE, pp. 1–9.

[9] Tuma, P., Moreno, G., Narumanchi, S., Bennion, K., Brandenburg, S., Olszewski, M., and Burress, T., 2010, "Passive 2-Phase Immersion Cooling of Commercial and Developmental Insulated Gate Bipolar Transistor (IGBT) Modules," IMAPs.

[10] Barnes, C. M., and Tuma, P. E., 2010, "Practical Considerations Relating to Immersion Cooling of Power Electronics in Traction Systems," IEEE Transactions on Power Electronics, **25**(9), pp. 2478–2485.

[11] B. Kelly, G. Moreno, S. Myers, S. Narumanchi, Y. Joshi, and S. Graham, 2021, "Dielectric Fluids for the Direct Forced Convection Cooling of Power Electronics," *2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pp. 1–6.

[12] "Oxygen Free Copper – UNS C10100,", https://www.azom.com/article.aspx?ArticleID=6314.

[13] "Property of Silicon Carbide (SiC)", http://www.qualitymaterial.net/news_list85.html.

[14] Wereszczak, A. A., Vuono, D. J., Wang, H., Ferber, M. K., and Liang, Z., 2012, "Properties of Bulk Sintered Silver as a Function of Porosity.", ORNL report.

[15] "Overview of Materials for Polyphenylene Sulfide (PPS) with 40% Glass Fiber Filler", https://www.matweb.com/search/datasheet.aspx?matguid=301e3f904d6a43a7922601c9d11ded91&ckck=1.

[16] Ndao, S., Peles, Y., and Jensen, M. K., 2009, "Multi-Objective Thermal Design Optimization and Comparative Analysis of Electronics Cooling Technologies," International Journal of Heat and Mass Transfer, **52**(19), pp. 4317–4326.

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