Power Module Precursors and Prognostics

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National Renewable Energy Laboratory

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FY23–FY24: Year 2 of 2

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OVERVIEW

Timeline

- Project start date: Aug. 1, 2022
- Project end date: Sept. 30, 2024
- Percent completed: 90%

Budget

- Total project funding: $300,000
  - DOE share: 100%
- Funding for FY 2023: $150,000
- Funding for FY 2024: $150,000

Barriers

- Reliability, performance, and cost.

Partners

- N/A

RELEVANCE

- The aging and failure diagnostics of silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs), a critical component in vehicular technology applications, are of great importance for personnel safety and reliable operation.
- Precursors can be used to identify and quantify the degree of device aging but are usually difficult to acquire and quantify in practical implementation.
- Identifying precursors whose detection can be effectively implemented in a portable device and developing the detection method are valuable.

SUMMARY

Developed analytical model for the turn-ON and turn-OFF transients and expansion of detectable aging precursors

- An analytical model of the SiC MOSFET half-bridge circuit during switching transients is developed and validated with SPICE simulation and experimental test results.
- Based on the analytical model, the detectable precursors using the gate-source voltage (v_{gs}) peak value measurement scheme is expanded to determine changes in ON-state resistance ($R_{ds,ON}$) as well as gate threshold voltage (V_{th}).

Accelerated lifetime cycles and tests on multiple SiC MOSFETs samples

- In addition to last year's device under test (DUT) (Wolfspeed CCS020M12CM2 sixpack), two new models of SiC MOSFET samples with different manufacturers and characteristics are procured to expand aging samples.
- Accelerated lifetime cycles were conducted on the new samples using our in-house aging station that rendered samples with various mechanisms and levels of aging.

Fabricated and validated the aging detector prototype

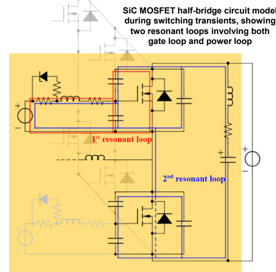
- The aging detector circuit has been finalized, and the prototype detector board was fabricated and tested.
- Detection tests using the prototype board are carried out on all aging samples, and the results are consistent with the analytical model and simulation results.

APPROACH

Development of analytical model of the SiC MOSFET half-bridge during switching transients

The model is developed by identifying different resonant loops within the circuit at different temporal stages and unifying the two stages in one system.

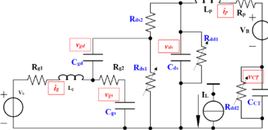
- The oscillations during the switching transients result from the SiC MOSFET device capacitance and parasitic inductances within the packaging and circuit layout.



SiC MOSFET half-bridge circuit model during switching transients, showing two resonant loops involving both gate loop and power loop

- Two resonant loops involve the gate loop and gate loop plus power loop, respectively. They are distinguished by the conduction states of the MOSFET during the transients.
- The circuit model of the two loops are unified by approximation of the MOSFET conduction states and other variable circuit components using continuous functions. The final unified analytical model is a system of ordinary differential equations (ODE).

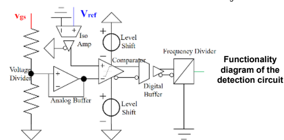
Equivalent circuit model during the transients with state variables in red boxes and variable components in blue



Unified analytical model

Leveraging the pulse-capturing and counting capability of the detection circuit for accuracy

- Critical active components for the detection circuit are identified and sourced for sufficient capture of V_{gs} peak patterns.
- By capturing and counting intersection pulses for a longer time interval, the influences of perturbations and noises can be mitigated. This will help obtain accurate V_{gs} peak values.



Functionality diagram of the detection circuit

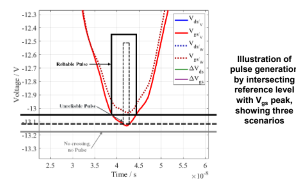
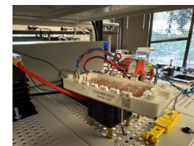


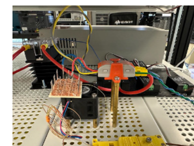
Illustration of pulse generation by intersecting reference level with V_{gs} peak, showing three scenarios

Accelerated lifetime cycles on multiple SiC MOSFET samples

- Multiple SiC MOSFET samples, including Wolfspeed CCS020M12CM2 six pack, C3M0075120D single, and Infineon FS55MR1-2W1M1H-B11 six pack, have been procured. These samples are made by different manufacturers, and they exhibit dissimilar electrical characteristics.
- Power cycles and power-induced temperature cycles have been induced to obtain samples having different aging levels.



Power cycles on the CCS020M12C M2 six-pack module

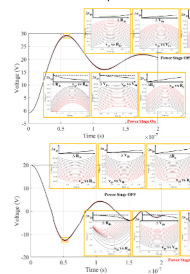


Temperature cycles on the FS55MR1-2W1M1H-B11 six-pack module

TECHNICAL ACCOMPLISHMENTS AND PROGRESS

Expansion of detectable aging precursors and summary of corresponding V_{gs} peak sift pattern

- After studying the analytical model, it is found out that the change of gate threshold voltage (V_{th}) can also be detected by observing the combination of V_{gs} peak shift patters at different transient instants and in different running conditions.
- Corresponding SPICE models providing consistent results have been developed and simulated to validate this finding.



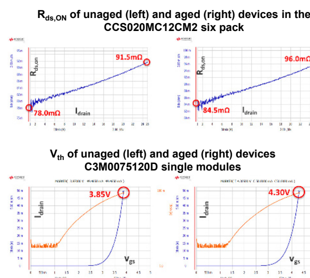
Analytical model simulation results revealing the patterns of V_{gs} peak shift in different scenarios; top: turn-ON transient, bottom: turn-OFF transient

Induced ON-state resistance ($R_{ds,ON}$) and V_{th} in SiC MOSFET samples from the accelerated cycles

- Two types of cycles are run on the aforementioned samples. The power cycles are run on the CCS020M12CM2 six pack, which has higher thermal capacity, and thermal cycles are run on the FS55MR1-2W1M1H-B11 six-pack and C3M0075120D modules.
- The resulting differences in $R_{ds,ON}$ and V_{th} in the two groups of samples shown below are approximately 8.6% and 11.0%, respectively.

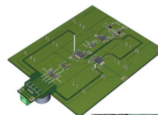
$R_{ds,ON}$ of unaged (left) and aged (right) devices in the CCS020MC12CM2 six pack

V_{th} of unaged (left) and aged (right) devices C3M0075120D single modules

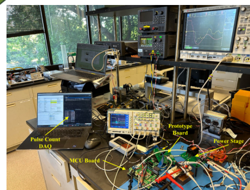


Experimental validation of the prototype aging detector

- The prototype detection board is fabricated and plugged-in to the gate driver board without any extra hardware. A TMS320F28377D-based development board is employed for both gate control and pulse capturing and counting.
- The four aforementioned samples with different $R_{ds,ON}$ and V_{th} are tested in working conditions listed in the first section. The pulse counting results and the implied V_{gs} peak values are consistent with analysis and SPICE simulations.



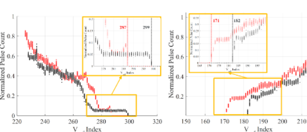
Top-left view of the prototype aging detection board



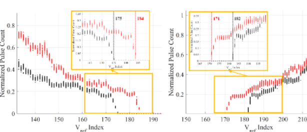
Test bench with the aging detector and half-bridge (synchronous buck)

- The most recent results have been presented at the 2024 IEEE Applied Power Electronics Conference (APEC).

Pulse counting results corresponding to different $R_{ds,ON}$ values for a new (red) and aged (black) device during turn-ON (left) and turn-OFF (right), @ 30V bus voltage. A larger number represents higher voltage.



Pulse counting results corresponding to different V_{th} values for a new (red) and aged (black) device during turn-ON (left) and turn-OFF (right), @ 30V bus voltage. A larger number represents higher voltage.

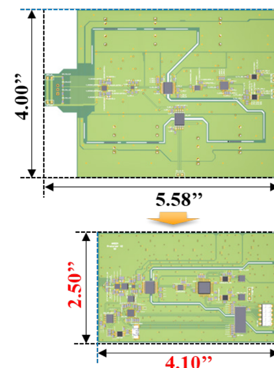


FUTURE WORK/CHALLENGES AND BARRIERS

- Additional devices with different degrees of aging should be procured and prepared for further evaluation of the performance of the aging detector. Presently, aging is induced by low-frequency power and temperature cycles. A new test fixture is being developed to emulate real-world converters and perform accelerated aging of SiC MOSFETs under various loading conditions. This will help create a comprehensive set of aging mechanisms.
- A new version of detection board has been designed (see below). This version has significantly reduced form factor (by 54% area) and an integrated gate driver with the purposes of higher portability and higher peak detection precision. It will be tested in the next phase.
- Considering the multi-dimensional information pick up capability of the signal acquisition circuit, other types of aging mechanisms and their corresponding precursors and detection methods should be studied.

Any proposed future work is subject to change based on funding levels.

Layout of the new version detection board with integrated gate driver



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