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## Preprint

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# Design, Optimization, and Validation of GaN-Based DAB Converter for Active Cell Balancing in BTMS Applications

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***Abstract*—This paper focuses on the design of a bidirectional dual active bridge (DAB) DC/DC converter that utilizes Gallium Nitride (GaN) switches as active components. In the existing literature, MOSFET-based DAB for active cell balancing is available, but GaN-based DAB converter for active cell balancing is still new. The proposed modular isolated GaN-based DAB converter is designed as an individual module of active cell balancing for behind-the-meter storage (BTMS) applications, targeting high-power charging stations. Modular isolated converters are connected to each cell (low voltage bus), and each cell is connected in series to build up a battery module. According to the reference current command of supervisory control, each DAB converter can transfer power back and forth through the high voltage (HV) bus to balance the State of Charge (SoC) between the cells. Each module DAB converter is designed at a 50 W power rating. Switch power and transformer losses are analyzed for different switching frequencies, showing the optimum switching frequency for minimum losses. Furthermore, the procedure to select the required gate driver and the PCB layout optimization are discussed. Finally, the DAB performance analysis of GaN-based DAB and Si-based DAB is provided for a battery module operating with a $LiFeMnPO_4$ prismatic cell with 3.2V 20Ah rated values.**

***Index Terms*—Active cell balancing, Behind-the-meter storage (BTMS), Bidirectional DC/DC converter, Dual Active Bridge (DAB), Field Effect Transistor (FET), Gallium Nitride (GaN), $LiFeMnPO_4$ prismatic cell, State of Charge (SoC).**

## I. Introduction

For a battery pack to operate safely and maintain a long lifetime, battery management systems (BMSs) are necessary. Due to variations among the cell parameters, the charge levels among the cells expose a mismatch in the battery pack. Balancing the cells is necessary to compensate for the mismatches to avoid over-charging or over-discharging. Although traditional passive cell balancing methods are cost-effective and straightforward architectures, active cell balancing methods exhibit superiority over the passive cell balancing methods in efficiency and heat dissipation [1], [2]. Instead of dissipating the excess energy in the highest charge level cell, the active cell balancing method redistributes the excess charge among the cells. Thus, overall system efficiency increases [3]. Different DC/DC converter topologies have been investigated extensively in the literature for active cell balancing methods. The DAB topology not only offers a symmetric structure and zero voltage switching (ZVS) but also reduces switching losses and provides galvanic isolation [4]. The DAB topology utilizes transformer leakage inductance as the primary source of the main energy transfer [5]. Therefore, the requirements of the transformer size are smaller than other bidirectional isolated converter topologies [6]. Si-based DAB converters have already been demonstrated to implement active cell balancing systems [3]. The utilization of Wide-Bandgap (WBG) devices presents an advantageous solution for BTMS applications, owing to the inherent constraints of weight, volume, and efficiency in such systems. Particularly, WBG devices, such as Gallium Nitride Field-Effect Transistors (GaN FETs), emerge as a feasible option for implementing DAB converters. GaN semiconductors exhibit superior characteristics, notably enabling higher switching frequencies compared to conventional Silicon (Si)-based semiconductors [4]. This feature proves instrumental in achieving enhanced performance in DAB converters. By harnessing the stored energy of the transformer leakage inductance, GaN-based converters are able to effectively discharge the energy stored in the output capacitance of the switches, thereby facilitating Zero Voltage Switching (ZVS) operation. A significant advantage of GaN devices lies in their substantially reduced output capacitances in comparison to Si-based semiconductor switches. This attribute ensures the attainment of ZVS over a broad operating range, leading to notable improvements in the efficiency of the DAB system. Thus, the integration of GaN FETs in DAB converters showcases the potential for enhancing the overall performance and efficiency of BTMS applications.

This paper proposes the design of an optimized modular isolated GaN-based DAB converter to utilize active cell balancing for a series battery pack with an auxiliary low voltage (LV) bus for BTMS applications. The parametric sweep analysis does an optimized design for the significant component selections for varying DAB parameters. The Printed Circuit Board (PCB) layout optimization for GaN-based DAB for active cell balancing is discussed. The functionality of the DAB is validated with the experimental result. Finally, an efficiency comparison between GaN-based and Si-based DAB converters with the

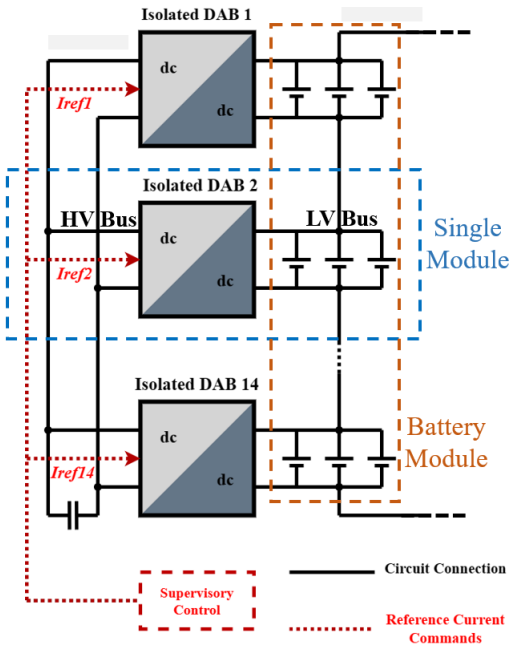



Fig. 1. Modular DC-coupled battery pack for BTMS applications.

TABLE I
MODULAR ISOLATED DAB CONVERTER SPECIFICATIONS

| Parameter Name | Value |
|---|---|
| Battery side voltage range | 2.14 - 4.20V (3.3V Nominal) |
| LV bus voltage range | 8.56 - 16.8V (12V Nominal) |
| Rated Power | 50W (Bidirectional Flow) |
| Isolation | Galvanic Isolation |

same specifications is provided.

## II. OVERVIEW OF THE SYSTEM

The modular battery pack design overview, including the associated modular isolated DAB converter, is shown in Fig. 1. The battery pack consists of series and parallel connected battery cells to increase the battery module's voltage level and total capacity for different applications. Individual cells actively balance their SoCs by transferring back and forth charge to the HV bus with the bidirectional power processing capability of the DAB. A supervisory control monitors the individual cell SoC and generates the reference current command to balance the SOC between the cells [7]. Table I gives specifications for an isolated DAB converter.

## III. DAB DESIGN APPROACH

The focus is to build an energy-efficient, isolated, and compact GaN-based DAB converter, which will be used for active cell balancing with bidirectional power flow. The power flow is controlled by the single phase shift modulation (SPS) with a fixed switching frequency and a fixed 50% duty ratio. The power flow equation (1) for the bidirectional DAB converter (Fig. 2) is written as [8]:

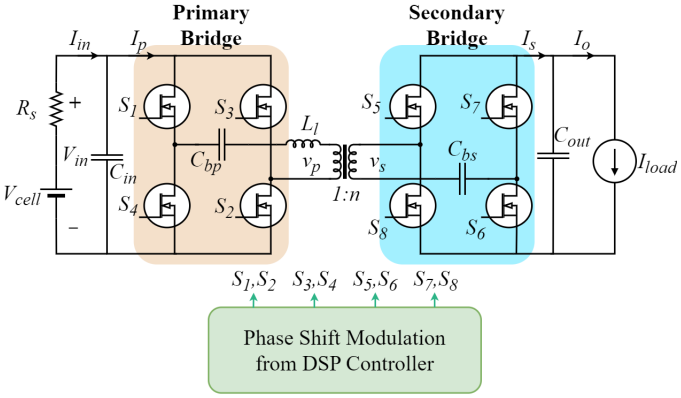



Fig. 2. Schematic of a basic DAB converter.

$$P = \frac{V_{in} V_o d(1-d)}{2 f_s n L_l} \tag{1}$$

where $V_{in}$ is the primary-side voltage; $V_o$ is the secondary-side voltage; $d$ is the phase shift; $f_s$ is the switching frequency; $n$ is the transformer turns-ratio, and $L_l$ is the leakage inductance of the primary plus leakage inductance of secondary with respect to the primary. The absolute maximum value of $d$ for maximum power flow in any direction is 0.5. For the same power flow, with the increase of leakage inductance, the required phase shift also increases. By introducing an external inductor, the value of $L_l$ can be adjusted to a suitable value to ensure ZVS at the operating condition. The ZVS depends on the DAB converter gain ($M$) and inductor current ($I_1$ and $I_2$) as follows [8]:

$$M = \frac{V_o}{n V_{in}} \tag{2}$$

$$I_1 = [(2d-1) + M]\frac{V_{in} T_s}{4 L_l} \tag{3}$$

$$I_2 = [1 + M(2d-1)]\frac{V_{in} T_s}{4 L_l} \tag{4}$$

where $T_s$ is the switching period. Fig. 3 shows typical voltage and current waveform for the DAB converter.

The necessary conditions to achieve ZVS at both the leading and the lagging bridge, the leakage inductor current $I_1$ and $I_2$ must be greater than zero. When $M$ equals 1, $I_1$ and $I_2$ are positive for positive phase shift and leading and lagging full-bridge operating at ZVS (Fig. 4). When $M$ is not equal to 1, there is non ZVS region for a positive phase shift. In this experiment, the value of M is 0.9091 for the nominal case. When M is less than 1, the necessary conditions of ZVS in the lagging full bridge and the leading full bridge are given in (5) and (6), respectively [9]:

$$d > \frac{(1-M)}{2} \tag{5}$$

$$d > \frac{(M-1)}{2M} \tag{6}$$

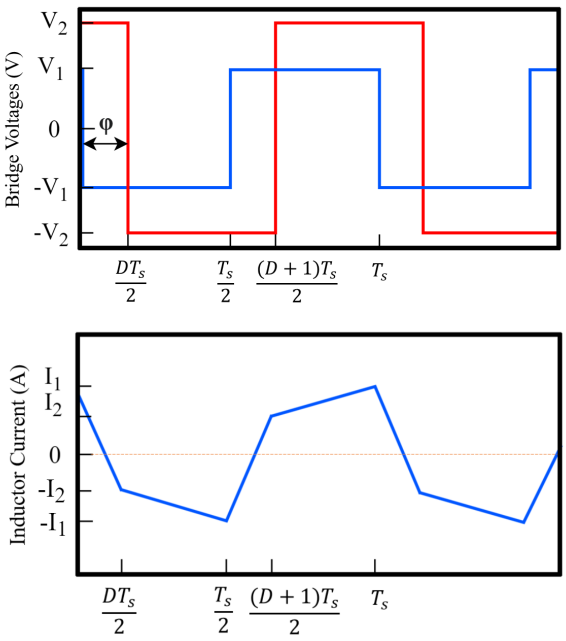



Fig. 3. Typical DAB waveform in single phase shift mode.

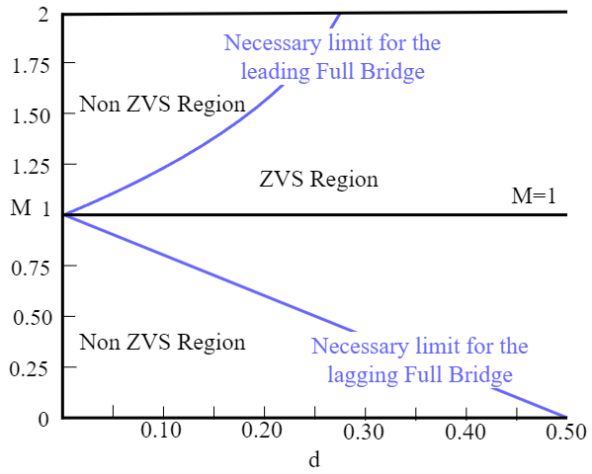



Fig. 4. Necessary condition to achieve ZVS in both leading and lagging full bridge as a function of $M$ and $d$. [9]

For the selection of the switching frequency, it is necessary to consider that at lower switching frequencies, peak currents and RMS currents increase, thus increasing conduction and copper losses in the transformer. Higher switching frequency decreases these conduction and copper losses but increases the switching loss. ZVS helps to eliminate the turn ON loss of the switching device but turn OFF loss remains. GaN switches have extremely low turn OFF loss, so the DAB-GaN combination gives the best result in terms of efficiency since it almost eliminates the switching loss. Hence, GaN switches exhibit superior efficiency, particularly at elevated switching frequencies, compared to silicon-based switches.

Primary and secondary side switch and transformer losses

TABLE II
SPECIFICATIONS OF THE DAB TRANSFORMER

| Datasheet Parameter | Value |
|---|---|
| Transformer Turns Ratio | 1 : 4 |
| Primary Side (LVS) Resistance | $4.2m\Omega$ |
| Secondary Side (HVS) Resistance | $7.2m\Omega$ |
| Magnetizing Inductance (Ref. HVS) | $143.5\mu H$ |
| Leakage Inductance (Ref. HVS) | $0.125\mu H$ |

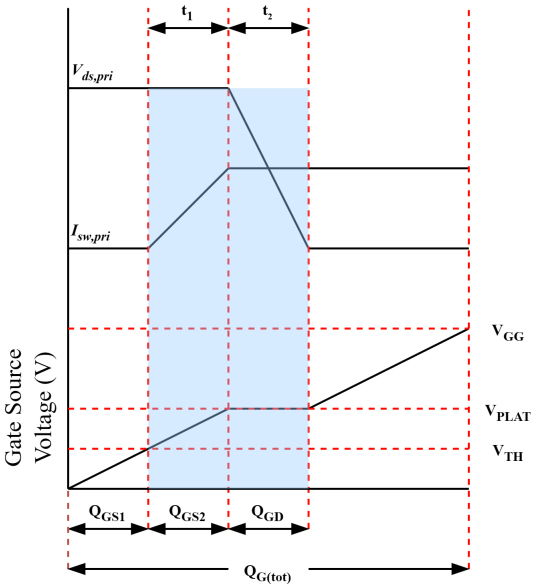



Fig. 5. Switch Turn-ON Transient

under different switching frequencies are calculated analytically at nominal operating conditions. Primary side transformer copper loss is calculated using (7) based on the transformer specifications given in Table II.

$$P_{xfr-loss(pri)} = I^2_{rms(pri)} R_{pri} \tag{7}$$

where $I_{rms(pri)}$ is the transformer's primary side RMS current, $R_{pri}$ is the transformer primary side winding resistor.

Energy during $t_1$ and $t_2$ are calculated using (8) and (9), respectively:

$$E_{t1} = V_{ds,pri} \frac{I_{sw,pri}}{2} t_1 \tag{8}$$

$$E_{t2} = I_{sw,pri} \frac{V_{ds,pri}}{2} t_2 \tag{9}$$

Time duration of $t_1$ and $t_2$ are dependant on the gate-source voltage ($V_{GS}$), corresponding charges $Q_{GS2}$, $Q_{GD}$ and total gate resistance of $R_G$. Equations for $t_1$ and $t_2$ are derived by calculating gate currents $I_{g1}$ and $I_{g2}$. The voltage across the gate-source, as it increases from threshold voltage $V_{TH}$ to plateau voltage $V_{PLAT}$, averaged for simplicity during $t_1$.

$$I_{g1} = \frac{0.5(V_{PLAT} + V_{TH})}{R_G} \tag{10}$$

$$I_{g2} = \frac{V_{PLAT}}{R_G} \tag{11}$$

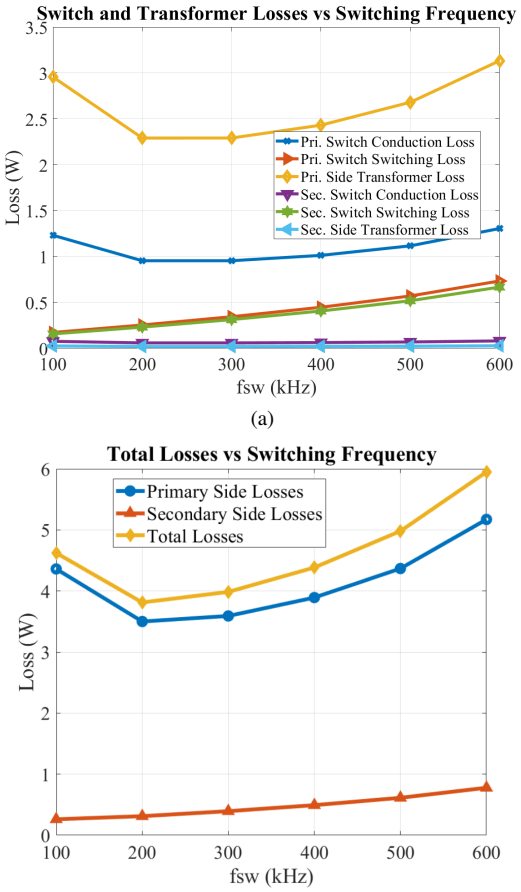



Fig. 6. The relation between losses and frequency at rated power: (a) Transformer and switch losses vs. switching frequency; (b) Total losses vs. switching frequency

Time duration $t_1$ and $t_2$ are calculated using (12) and (13).

$$t_1 = \frac{Q_{GS2}}{I_{g1}} \tag{12}$$

$$t_2 = \frac{Q_{GD}}{I_{g2}} \tag{13}$$

Turn-on and turn-off losses are considered to be equivalent. Thus overall switching loss for a primary switch is calculated using (14):

$$P_{sw-loss(pri)} = 2(E_{t1} + E_{t2})f_{sw} \tag{14}$$

As the DAB converter is operating in the ZVS region at rated power, the modified switching loss equation at ZVS is presented in (15), and the conduction loss in (16):

$$P_{ZVS-sw-loss(pri)} = (E_{t1} + E_{t2})f_{sw} \tag{15}$$

$$P_{cond-loss(pri)} = I^2_{sw-rms(pri)} R_{ds_{on}} \tag{16}$$

where $I_{sw-rms(pri)}$ is the primary side switch RMS current, $R_{ds_{on}}$ is the turn-on resistance of switch. These equations are also used to calculate losses for the secondary side. According to the analytical results, at around 200 kHz, DAB exhibits the lowest losses as shown in Fig. 6.

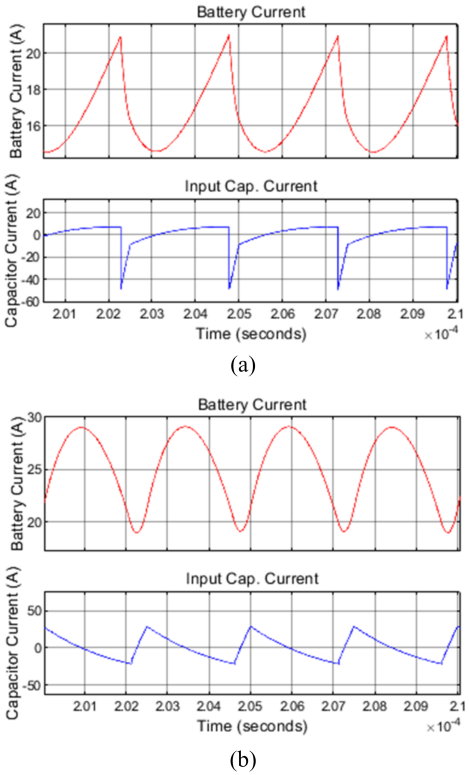



Fig. 7. Battery current and DC-link capacitor current (a) at nominal battery voltage and 2.6 mF DC-link capacitance; (b) at battery's lower cut-off voltage and 2.8 mF DC-link capacitance.

TABLE III
SPECIFICATIONS OF THE SWITCH (EPC2024)

| Datasheet Parameter | Value |
|---|---|
| $Rds_{ON}$ | $1.2\,m\Omega$ |
| Threshold Voltage ($V_{TH}$) | $1.4\,V$ |
| Plateau Voltage ($V_{PLAT}$) | $2.5\,V$ |
| Internal Gate Resistance ($R_{Gint}$) | $0.3\,\Omega$ |
| Gate-Source Charge ($Q_{GS1} + Q_{GS2} = Q_{GS}$) | $3.8 + 1.2 = 5\,nC$ |
| Gate-Drain Charge ($Q_{GD}$) | $2.5\,nC$ |

Due to the higher switching frequency, DC-link capacitor requirements decrease for filtering elements. Still, the capacitor must have a higher resonance frequency to mitigate the high-frequency ripple at the LV and HV buses. Therefore, tantalum capacitors are used as DC-link capacitors instead of bulky electrolytic capacitors. Tantalum capacitors provide higher resonance frequency, smaller size, and less weight than electrolytic capacitors. Besides, the value of the capacitor must keep the peak-to-peak current ripple less than 50%. The simulation result shows that, at nominal battery voltage (3.3V), the peak-peak current ripple is 45% (Fig. 7(a)) for 2.6 mF DC-link capacitance. For the battery's lower cut-off voltage (2.14 V), the peak-peak current ripple is 42% (Fig. 7(b)) for 2.8 mF capacitance.

For the transformer selection, the inductor current $I_1$ and $I_2$ are two essential parameters as the peak and the RMS current handled by the transformer depending on the magnitude of the

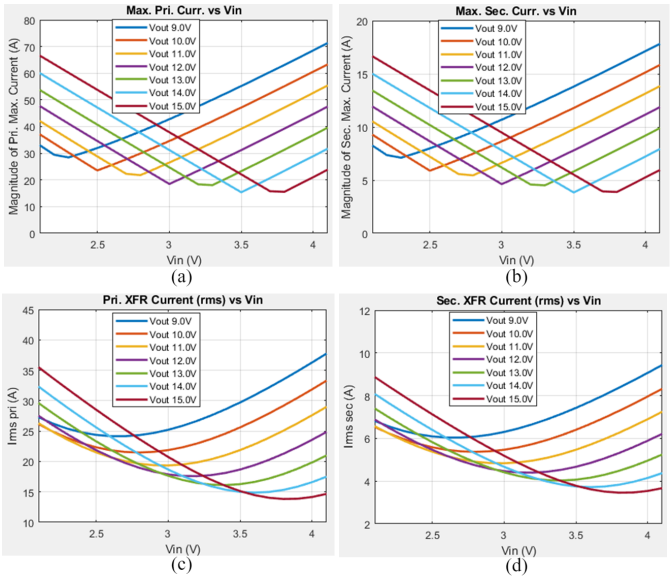



Fig. 8. The relationship between $V_{in}/V_o$ and (a) $I_{max(pri)}$; (b) $I_{max(sec)}$; (c) $I_{rms(pri)}$; and (d) $I_{rms(sec)}$, where $L_l$ is 20 nH and $T_s$ is 5 $\mu$s.

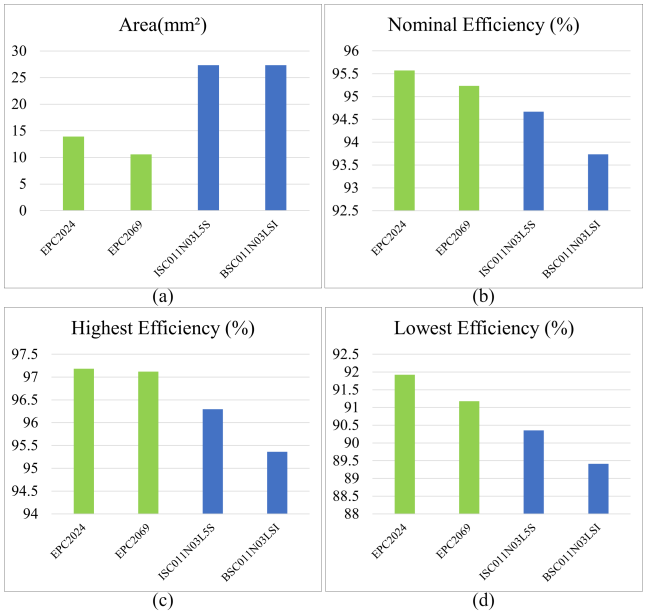



Fig. 9. Comparison between GaN and Si switches (a) Area comparison; (b) Efficiency at nominal condition; (c) Highest efficiency; (d) Lowest efficiency.

maximum value of the inductor current (17), (18), (19), and (20) [8]. Besides, as the cell voltage changes depending on the SoC level, the relationship between transformer current, $V_{in}$, and $V_o$ is also necessary, which is presented in Fig. 8.

$$I_{max(pri)} = max(|I_1|, |I_2|) \tag{17}$$

$$I_{max(sec)} = \frac{I_{max(pri)}}{n} \tag{18}$$

$$I_{rms(pri)} = \sqrt{\frac{I_1^2 + I_2^2 + I_1 I_2 (1 - 2d)}{3}} \tag{19}$$

$$I_{rms(sec)} = \frac{I_{rms(pri)}}{n} \tag{20}$$

where $I_{max(pri)}$ and $I_{max(sec)}$ are the Peak primary and secondary current of the transformer, respectively, and $I_{rms(pri)}$ and $I_{rms(sec)}$ are RMS primary and secondary currents of the transformer respectively. Peak primary and secondary side switch currents are determined by the peak primary and secondary side transformer currents, respectively. The relation between switch RMS current and transformer RMS current is (21) and (22).

$$I_{sw-rms(pri)} = \frac{I_{rms(pri)}}{\sqrt{(2)}} \tag{21}$$

$$I_{sw-rms(sec)} = \frac{I_{rms(sec)}}{\sqrt{(2)}} \tag{22}$$

Besides, the continuous operation regions of the switches are limited by the same operating regions of the transformer currents. Based on the current requirement at the nominal power flow and availability of the switches, the comparative analysis between four (two GaN and two Si) switches is shown in Fig. 9. In the results, the EPC2024 GaN switch shows higher efficiency over other switches with a relatively small form factor.

For the gate driver selection, the peak gate current of the switch and power dissipation in the gate should be considered. The pack current required by a switch to be turned on can be calculated using (23):

$$I_{g-peak} = \frac{\Delta V_{gs}}{R_{ext} + R_{int}} \tag{23}$$

where $\Delta V_{gs}$ is the difference between the turned-on and turned-off gate to source voltage, $R_{ext}$ is the external gate resistance, and $R_{int}$ is the internal gate resistance of the switch. By adjusting the external gate resistor, the required time to turn the switch on and off can be controlled. Higher gate resistance slows the switch response, eventually increasing the switching losses. Lower gate resistance reduces the switching losses but causes ringing in the gate voltage. Power dissipation for the gate driver (per channel) can be calculated by (24):

$$P_{gd} = \Delta V_{gs} f_s Q_G \tag{24}$$

where $Q_G$ is the total gate charge of the switches connected to the single channel of a gate driver.

PCB layout optimization is another crucial part of the optimum design in high-frequency applications. At high switching frequency, the impact of PCB-parasitic becomes more significant, which causes lower efficiency and higher stress on the switch [10]. The transient simulation in the LTspice, with the selected gate driver (LMG5113) and switches, shows with the increase of the power loop inductance from 0.2 nH to 1 nH, the overshoot increases from 15% to 39% (Fig. 10).

For the optimum PCB design layout, the magnetic field self-cancellation technique in a multi-layer PCB structure is used to reduce the loop inductance [10], [11]. The design utilizes

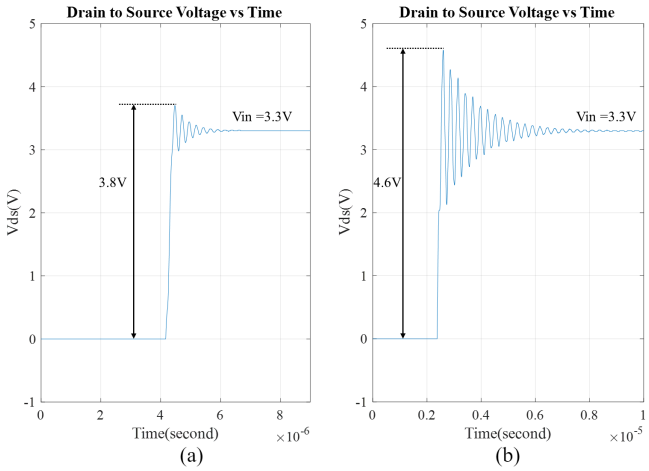



Fig. 10. Drain to source voltage overshoot across the LVS GaN FET for the loop inductance of (a) 0.2nH; (b) 1nH.

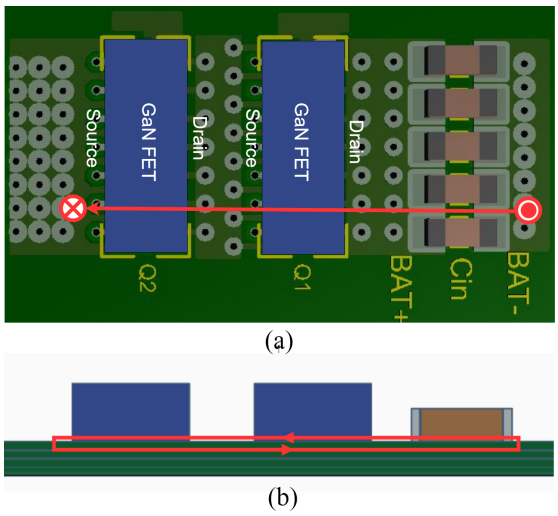



Fig. 11. Optimum PCB Layout (a) Top view; (b) Side view.

the first inner layer as a power loop return path, shown in Fig. 11(b). The top layer power path is right on the top of the bottom return path to ensure a smaller loop size (Fig. 11(a)). The power flow direction of the top and the bottom path is opposite to each other, which provides self-cancellation in the magnetic field.

## IV. Experimental Validation

In the experimental setup, there were ten modular 50 W DAB converters, each integrated with a single 3.2V, 20 Ah, LiFeMnPO4 prismatic cell. The secondary side of the DAB converters is connected in parallel to form 12V̇ LV DC bus. Each DAB at the output connects 188 uF capacitors, making the total capacitance 1.88 mF at the 12 V bus. Table IV shows the specifications of a single DAB in the experimental setup.

At the rated power, the drain to source voltage of the LV and HV side GaN FETs was observed (Fig. 12b). Due to the optimization of the PCB layout, the power loop inductance

TABLE IV
Specifications of Tested Single DAB

| Parameter Name | Value |
|---|---|
| LV Side | 1 LiFeMnPO4 cell connected |
| HV Side | 188$\mu$F Capacitor connected |
| Low Side Voltage | 3.2V |
| High Side voltage | 12V |
| Rated Power | 50W (Bidirectional Flow) |
| Transformer Turns Ratio | 1:4 |
| DC-Link Capacitance | 4.84mF (22 x 220$\mu$F) |
| Leakage Inductance Value | 133.33nH |
| Switching Frequency | 200kHz |
| DSP Processor | TMS320F280025C |
| Switch | EPC2024 |
| Gate Driver | LM5113 |

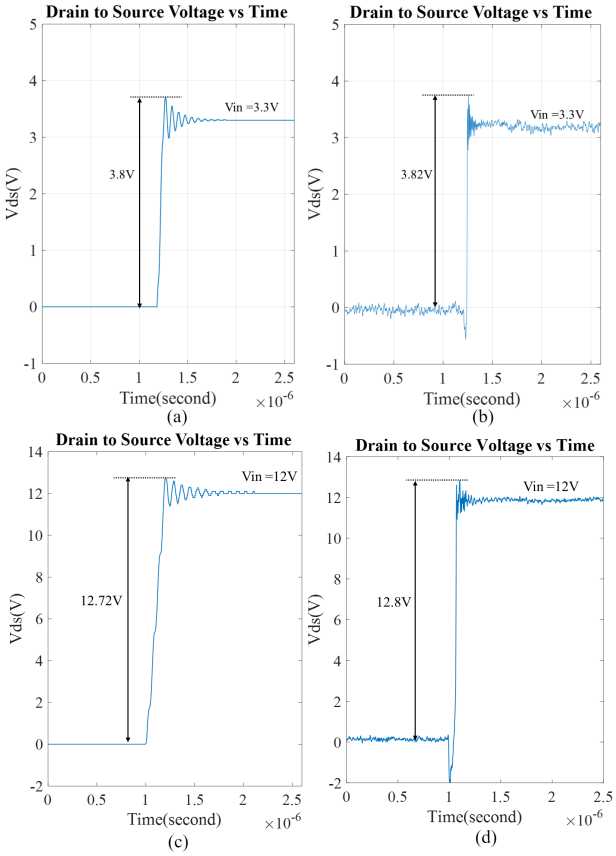
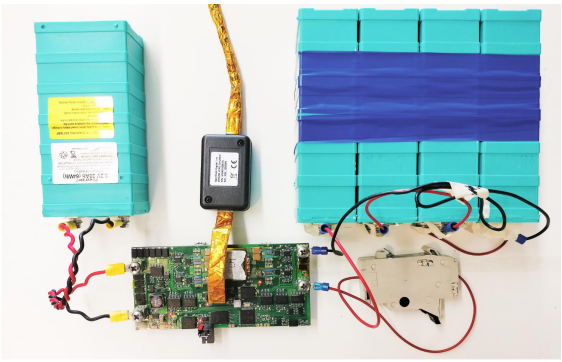
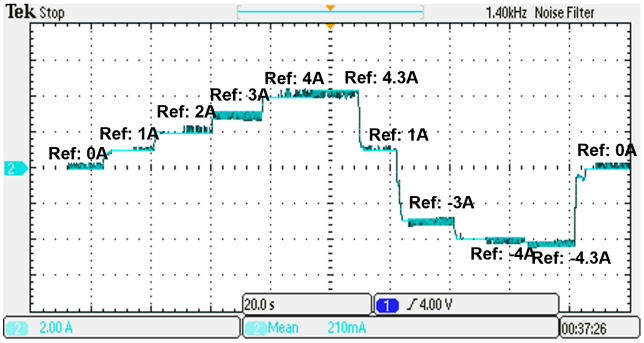



Fig. 12. Drain to source voltage overshoot (a) Simulation result at LV side; (b) Experimental result at LV side; (c) Simulation result at HV side; (d) Experimental result at HV side

reduces, which reduces the drain to source voltage overshoot across the switch significantly. Each DAB was tested with the bidirectional power flow. An internal closed-loop control was implemented into each DAB. The closed-loop control generates the phase shift according to the supervisory control's given LV side current command to the DAB while maintaining the HV side bus voltage. Fig. 13a shows the experimental setup to check the closed-loop control where a single LiFeMnPO4 cell (3.2V) is connected at the LV side and Four LiFeMnPO4 cells are connected in series to form HV side. Fig. 13b shows



(a)




(b)

Fig. 13. (a) Closed-loop control test setup (b) DAB Current Regulation for Different Reference Currents.

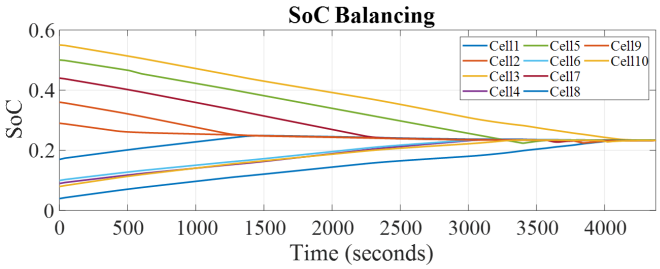



Fig. 14. SoC Balancing between 10 cells

that the DAB converter can regulate current (LV side) based on the supervisory controller's reference current command. Here the negative current means the LV side cell is charging, and the positive current means the LV side cell is discharging.

For the SoC balancing between the ten cells connected with each DAB, communication between the supervisory controller and all the DABs is required. Considering the reliability, scalability, fault tolerance, and cost, the Controller Area Network (CAN) communication protocol was used for this purpose. The SoC balancing for ten cells is shown in Fig. 14. In Fig. 14, the initial SoCs of the cells was between 10% to 55%, and the SoC became balanced at around 4700 sec. After balancing the cells' SoCs, all the cell currents reached close to zero. There was still some current flow to regulate the HV side bus. During the whole balancing process, the HV side BUS was regulated with a 12V constant voltage. Another DAB was designed and

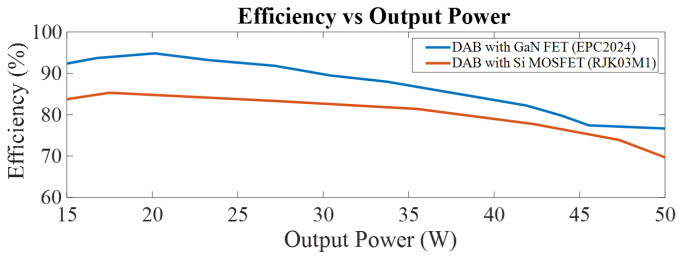



Fig. 15. Efficiency Comparison Between Si and GaN-Based DAB.

made with the same specification using the Si MOSFET switch for the efficiency comparison between GaN-based DAB and Si-based DAB for different power levels. Fig. 15 shows that the GaN-based DAB has much higher efficiency for all levels of power flows. The efficiency drops at the low power level because the DAB operates at the non-ZVS region for a small phase shift, as for the nominal case, $M$ is less than unity. So, the performance of the proposed design is validated through the experimental results.

## V. Conclusions

This work uses a compact and efficient GaN-based isolated DAB converter for active cell balancing. The high-frequency transformer, switches, gate driver, and DC-linked capacitor selection criteria have been discussed. The effect of parasitic power loop inductance and the optimized PCB layout have been mentioned. After the functionality testing, the efficiency between GaN-based DAB and Si-MOSFET DAB, with the same specifications, has been compared. The comparison between GaN-based DAB, with optimum design, shows better efficiency over the Si-based DAB converter. The high electron mobility of the GaN FETs allows an increase in the switching frequency, which reduces the size of the filtering components. Finally, designed DAB converters have balanced the SoCs of ten cells.

## References


[1] D. B. Yelaverthi, M. M. U. Rehman, and R. Zane, "Differential power processing three-port dual active bridge converter for active balancing in large battery packs," in *IEEE Energy Conversion Congr. Expo. (ECCE)*, 2018, pp. 5591–5597.

[2] M. Räber, D. O. Abdeslam, A. Heinzelmann, and A. Ramirez, "Performance estimation of a cell-to-cell-type active balancing circuit for lithium-ion battery systems," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, 2017, pp. 1005–1010.

[3] M. Evzelman, M. M. U. Rehman, K. Hathaway, R. Zane, D. Costinett, and D. Maksimovic, "Active balancing system for electric vehicles with incorporated low-voltage bus," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7887–789, 2016.

[4] Z. Zhang, J. Huang, and Y. Xiao, "GaN-based 1-MHz partial parallel dual active bridge converter with integrated magnetics," *IEEE Trans. Power Electron.*, vol. 68, no. 8, pp. 6729–6738, 2021.

[5] M. Kheraluwala, R. Gascoigne, D. Divan, and E. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, 1992.

[6] A. S. Babokany, M. Jabbari, G. Shahgholian, and M. Mahdavian, "A review of bidirectional dual active bridge converter," in *Int. Conf. Elect. Eng./Electron., Comput., Telecommun. Inform. Technol.*, 2012, pp. 1–4.

[7] A. Chowdhury, A. Siddiquee, P. Mishra, M. E. Haque, M. J. Kisacikoglu, A. Thurlbeck, E. Watt, M. A. Rahman, Y. Sozer, and J. Holt, "Design of a multi-chemistry battery pack system for behind-the-meter storage applications," in *IEEE Applied Power Electron. Conf. Expo. (APEC)*, 2023, pp. 3044–3049.

[8] V. M. Iyer, S. Gulur, and S. Bhattacharya, "Optimal design methodology for dual active bridge converter under wide voltage variation," in *IEEE Transport. Electrific. Conf. Expo. (ITEC)*, 2017, pp. 413–420.

[9] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, 2015.

[10] D. Reusch and J. Strydom, "Understanding the effect of pcb layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, 2014.

[11] J. Lu, H. Bai, A. Brown, M. McAmmond, D. Chen, and J. Styles, "Design consideration of gate driver circuits and pcb parasitic parameters of paralleled e-mode gan hemts in zero-voltage-switching applications," in *IEEE Applied Power Electron. Conf. Expo. (APEC)*, 2016, pp. 529–535.