PHIL Interface Design for Use With a Voltage-Regulated Amplifier

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BACKGROUND/INDUSTRY IMPACT

- Power hardware-in-the-loop (PHIL) has emerged as a leading strategy to thoroughly assess the impact of proprietary inverter controls on a specific power system [1].
- A three-step approach of PHIL interface development for amplifiers with built-in voltage regulation is introduced and is validated in hardware with a 30-kW grid-following inverter.

PROJECT OVERVIEW/OBJECTIVES

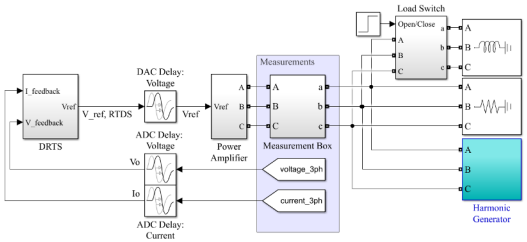
- Unregulated power amplifiers have an inherent inaccuracy challenges due to delays.
- These delays create a phase lag between the outgoing amplifier reference and the incoming voltage (or current) measurements. The total phase lag will lead to a phenomenon known as illusionary reactive power [2].
- Recently, regulated power amplifiers are commercially available.
- This work proposes the use of phase-lead compensator which can be used as an alternative method to compensate for the delay.
- This effectively removes the illusionary reactive power.

Key interface components

Three key components are used in the software interface:

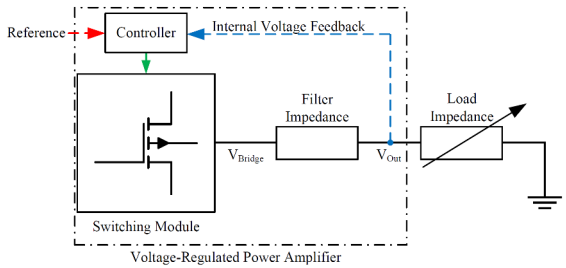
- Low pass filter – The first operation is passing the incoming current measurements through a low-pass filter to remove external measurement noise.
- Phase Lead Compensator – The filtered current waveform is passed through a phase lead compensator to remove illusionary reactive power by injecting an equivalent amount of phase lead.
- Band-Stop Filter - Finally, the PCC voltage, passes through a band-stop filter to remove possible frequency components that would excite a resonance point of the power test bed.

Software design

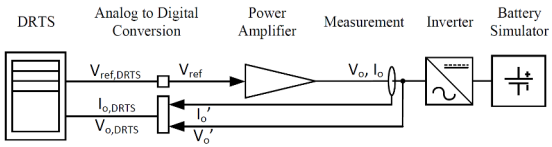


Software testbed model

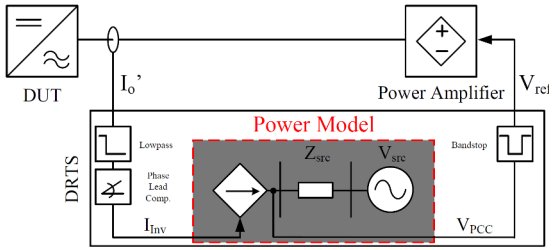
Voltage-regulated power amplifier impedance model



Laboratory hardware setup with signal labels



Proposed physical control model of PHIL setup



30-kW experimental hardware test bed.

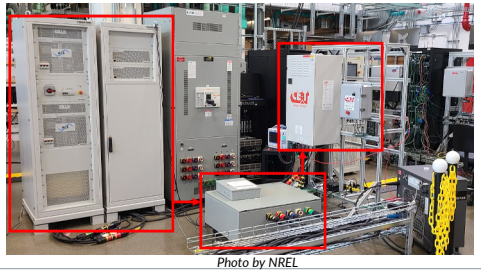
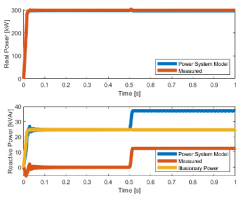
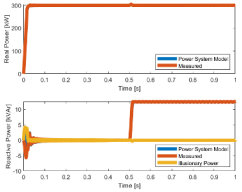


Photo by NREL

Software results



Software real and reactive power waveforms from uncompensated interface.



Software real and reactive power waveforms from compensated interface.

Hardware results

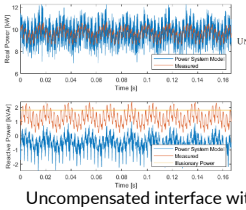


TABLE I
UNCOMPENSATED HARDWARE INTERFACE: REAL AND REACTIVE POWER MEAN MEASUREMENTS

Measurement Point	Value
Inverter real power set point	10 kW
DRTS measured real power (P_{HW})	9.6334 kW
DRTS power model real power (P_{SW})	9.6334 kW
Inverter reactive power set point	0 kVAr
DRTS measured reactive power (Q_{HW})	1.2629 kVAr
DRTS power model reactive power (Q_{SW})	-0.538 kVAr
Illusionary reactive power	1.8013 kVAr

Uncompensated interface with the grid-following inverter injecting 10 kW of real power.

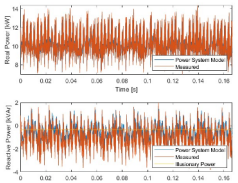


TABLE II
COMPENSATED HARDWARE INTERFACE: REAL AND REACTIVE POWER MEAN MEASUREMENTS

Measurement Point	Value
Inverter real power set point	10 kW
DRTS measured real power (P_{HW})	10.284 kW
DRTS power model real power (P_{SW})	10.303 kW
Inverter reactive power set point	0 kVAr
DRTS measured reactive power (Q_{HW})	-1.0127 kVAr
DRTS power model reactive power (Q_{SW})	-0.659 kVAr
Illusionary reactive power	0.353 kVAr

Compensated interface with the grid-following inverter injecting 10 kW of real power.

SUMMARY

This study introduced a three-step approach to develop PHIL interface for power amplifiers with built in voltage regulation:
(1) Run the test bed with variable harmonics to determine the resonance regions.
(2) Measure the amount of phase lead compensation required to avoid a reactive power error.
(3) Validate the proper lead compensation operation and iterate if necessary.

- The software model interface reduced the illusionary reactive power from 24.75 kVAr to 0.0397 kVAr.
- The hardware model interface saw a reduction from 1.8 kVAr to 0.353 kVAr.
- The next logical extension of this work is for voltage source inverters operating in grid-forming mode.

References

[1] K. Prabakar, B. Palmintier, A. Pratt, A. Hariri, I. Mendoza and M. Baggu, "Improving the performance of integrated power-hardware-in-the-loop and quasi-static time-series simulations", IEEE Trans. Ind. Electron., vol. 68, no. 11, pp. 10938-10948, Nov. 2021.
[2] N. Ainsworth, A. Hariri, K. Prabakar, A. Pratt, and M. Baggu, "Modeling and compensation design for a power hardware-in-the-loop simulation of an ac distribution system," in 2016 North American Power Symposium (NAPS), pp. 1–6, IEEE, 2016.

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