# Overcurrent Limiting in Grid-Forming Inverters: A Comprehensive Review and Discussion

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***Abstract*—Grid-forming (GFM) inverters are increasingly recognized as a solution to facilitate massive grid integration of inverter-based resources and enable 100% power-electronics-based power systems. However, the overcurrent characteristics of GFM inverters exhibit major differences from those of conventional synchronous machines. Accordingly, an in-depth characterization of GFM current-limiting strategies is needed to ascertain their performance during off-nominal conditions. Although GFM current-limiting controls are primarily necessary to protect the inverter power stage, they determine the inverter behavior during and after an off-nominal system disturbance. As a result, they can profoundly impact device-level stability, transient system stability, power system protection, and fault recovery. This article offers a comprehensive review of state-of-the-art current-limiting techniques for GFM inverters and outlines open challenges where innovative solutions are needed. One key contribution of this article is the use of graphical methods that allow for intuitive understanding and visually aided comparisons of current-limiting methods. With this approach, we evaluate various performance criteria for different limiting methods, such as fault current contribution, voltage support, stability, and post-fault recovery. We also discuss the latest standards and trends as they require inverter dynamics under off-nominal conditions and outline pathways for future developments.**

***Index Terms*—Current limiting, fault ride-through, grid-forming (GFM) inverters, stability.**

## I. Introduction

THE presence of inverter-based renewable energy resources, such as wind turbines, solar photovoltaics, and fuel cells, is increasing in modern power grids. Additional examples of grid-connected inverters include battery energy storage, STATCOMs, and high-voltage dc. Today, most installed inverters act as *grid-following* (GFL) units whose ac outputs mimic a current source by following the measured grid voltage with the use of a *phase-locked loop* (PLL) [1]. As the share of GFL *inverter-based resources* (IBRs) grow and fossil-fuel generation is retired, so do the concerns for power system integrity since grids were initially predicated on the use of synchronous generators (SGs) for system stabilization. This has triggered increased interest from the power system industry to incorporate grid-forming (GFM) capabilities in grid-connected inverters to provide grid services that enhance reliability and stability [2]. In recent years, inverters with GFM capabilities have been recognized as a pathway to facilitate the transition to a sustainable power grid. Many leading research organizations, transmission system operators, and multinational consortia around the world are working towards incorporating GFM capabilities into grid-connected inverters and streamlining grid codes for GFM technologies [3], [4], [5], [6], [7].

Despite significant interest in this area, many questions related to GFM inverter control remain unanswered [8]. Open questions are particularly centered around the behavior of GFM control dynamics during off-nominal and contingency conditions [2], [3]. The physical origin of the problem is the inherent limits in the overcurrent capabilities of power semiconductor devices within an inverter. Generally, converter size and thermal management costs increase as the magnitude and duration that the converter must reliably tolerate increase. This tradeoff results in inverter designs that can only tolerate overcurrents marginally exceeding the nominal value for inverter cost reduction. SGs, on the other hand, can deliver 5–10× their rated current for a certain period of time without damage, and this property has been leveraged to enhance power system robustness during disturbances. The high overcurrent capabilities and rotational inertia associated with machines lie at the heart of existing power system reliability and protection schemes [9]. Given the aforementioned differences between SGs and IBRs, it is clear that the transition to an inverter-based system will bring many challenges [10], [11]. On the upside, inverters offer immense flexibility due to their use of programmable digital controls, which shape their dynamics, and high switching frequencies that far exceed the dynamics of interest in power systems and, therefore, provide fast actuation. Accordingly, the GFM inverter behavior is primarily determined by the inverter control software design giving flexibility [12].

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The subsystem that protects the inverter hardware from thermal breakdown during excessive overcurrents is current limiting within the inverter control loops. Once a disturbance occurs in the grid (i.e., short-circuit faults, phase or frequency jumps, overloading, inrush phenomena for motor start or cold load pickup, or black start), the inverter may be forced into an overcurrent condition, which triggers the limiter to curtail the output currents. In that case, normal operation is overridden and the current limiter dominates inverter dynamics during the disturbance and recovery process. Many different current-limiting strategies have been proposed in the literature and each has its own merits and drawbacks. However, no method has been found to work accurately and reliably for all possible types of grid disturbances. Given that current limiter actions strongly impact GFM inverter dynamics and power system operation, careful consideration of the limiter design with respect to the entire power system is required. In this article, we investigate existing current-limiting approaches proposed in the literature and shed light on the merits and drawbacks of each method with respect to various performance attributes and under different grid conditions. With this approach, this article provides clarity on this critical topic and inspires new research ideas for the future.

The rest of this article is organized as follows. In Section II, we introduce basic concepts for GFM inverter current limiting that will be used in the rest of the article. In Section III, we provide an overview of the existing current-limiting strategies in the literature that are applicable to GFM inverters. Section IV briefly touches on GFM current limiting in single-phase inverters. In Section V, we discuss the impacts of various current-limiting methods on transient and small-signal stability, inverter-level GFM dynamics, the post-fault recovery process, and how these limiters handle unbalanced conditions. In Section VI, we broaden our scope and discuss the importance of grid codes. This section also gives a summary of efforts by leading organizations toward GFM-tailored standards. In Section VII, we briefly discuss how the current limiting of GFM inverters affects the efficacy and reliability of power system protection based on pertinent literature. Finally, Section VIII concludes this article.

## II. Setting the Scene: Challenges of GFM Current Limiting

Before taking a deep dive into the peculiarities of GFM current limiting, it is crucial to understand and appreciate the vast challenges associated with current limiting in GFM inverters. In this section, we contemplate what the idealized GFM current limiter looks like, and initiate discussions that serve as the storyline for the remainder of this article.

Current limiters in power electronics inverters are essential for a specific reason: the limiter must protect the device against thermal hardware damage caused by sourcing excessive output currents. This is the primary objective of current limiting. In that spirit, ideally, overcurrents should be curtailed quickly and accurately; however, once the current limiter engages, the entire control architecture of the inverter is altered, which leads to a different dynamic output behavior of the inverter. As such, the current limiter should not only facilitate quick and accurate limiting, but also restrain from causing any small-signal instability or inducing excessive harmonics in the inverter output voltage and currents. The altered inverter dynamic behavior resulting from current limiting can affect the system. For instance, the change in inverter output terminal behaviors can translate to network-wide attributes, such as power system protection, transient stability, voltage support, and grid synchronization. With the increasing responsibilities of GFM inverters to provide grid services and stabilize the grid, the actions of the limiter during disturbances with respect to system attributes must be taken into account in the GFM design process.

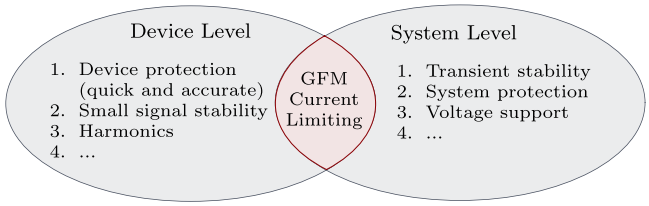


Fig. 1. Graphical representation of the challenges facing current limiting in GFM inverters both on device level and system level.

These device- and system-level challenges for GFM current limiters are graphically summarized in Fig. 1. Unfortunately, designing a current limiter that performs optimally for all these aforementioned aspects, both on a device level and a system level, is challenging and requires a deep understanding of the current-limiting mechanisms. Throughout this article, we review various current-limiting architectures and illustrate that every current-limiter design makes compromises and tradeoffs. In that way, this article provides a better understanding of the boundary condition in which we design current limiters and aims to give the reader a comprehensive understanding of GFM current-limiting mechanisms. Also, note that this article focuses on the output current limiting for generic three-phase and single-phase GFM inverters; it does not deal with any specific power conversion topology. For instance, overcurrent limiting and protection for modular converters, such as cascaded H-bridge converters [13] and modular multilevel converters [14], [15], can differ and require additional efforts.

## III. Overview of Current-Limiting Methods

In this section, we discuss the most common and recently proposed methods to limit the output current of three-phase GFM inverters, which we classify as either direct or indirect current-limiting methods. Direct current limiters aim to curtail the inverter output current to the maximum designed level by directly manipulating the current-reference control signals or semiconductor switch signals. Indirect current limiters curtail the output current by indirectly manipulating and diminishing the voltage-reference and/or power-reference signals in the inverter controls. Fig. 2 illustrates five direct and indirect current-limiting methods that are discussed in this work (indicated in red), integrated into a prototypical GFM control architecture. In the remainder of this work, we often refer to the conceptual GFM

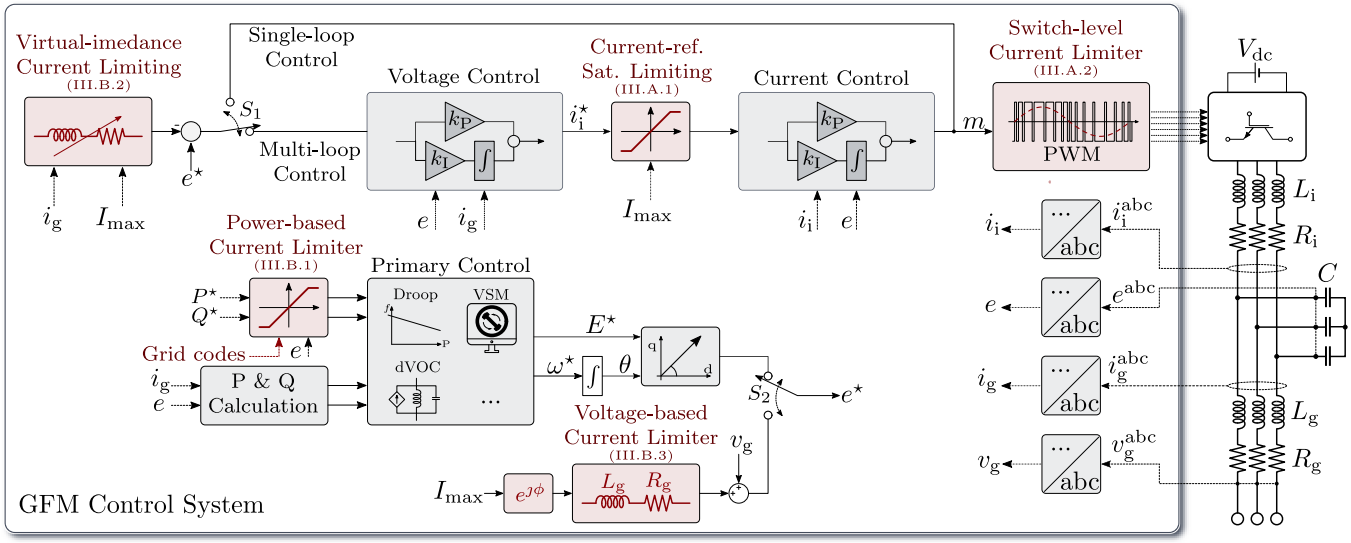


Fig. 2. Overview of direct and indirect current-limiting methods for GFM inverters.

control architecture and signal notations in Fig. 2. To serve as a baseline for our narrative, the conceptual GFM control topology, illustrated in Fig. 2, is introduced.

The GFM inverter can be built out of cascaded control loops, which comprise an inner-current, outer-voltage, and primary control loops. The output $LCL$-filter currents and voltages are sensed and fed as inputs to these various control loops. Depending on the reference frame that is leveraged in the controls, the input measurements are first transformed using Clarke and Park transformations. Based on the output and reference power, the primary controller generates the internal inverter reference for the capacitor voltage magnitude, $E^\star$, and the frequency and angle reference, $\omega^\star$ and $\theta$, respectively. As shown in Fig. 2, typical primary control methods include droop control [16], virtual synchronous machine (VSM) control [17], and dispatchable virtual oscillator control (dVOC) [18], [19], [20].

The reference voltage vector, $e^\star$, is directed as an input to the outer-voltage loop, which in turn controls $i_{\mathrm{i}}^\star$ that serves as the reference to the inner-current control loop. The output of the inner-current controller, $m$, called the modulation index, drives the pulsewidth modulation block that controls the semiconductor switches. Notice that, as indicated by the switch $S_1$ in Fig. 2, the cascaded voltage–current loops or the inner-current loop can be bypassed, which transforms the GFM inverter into a single-loop controlled or current control-less inverter [18], [21]. All the current limiters that are discussed hereafter are conceptually illustrated and highlighted in red.

Further, in Fig. 2, we use the following notations. We denote the reference active and reactive power set points by $P^\star$ and $Q^\star$, respectively; $i_{\mathrm{i}}$ and $i_{\mathrm{g}}$ denote the inverter- and grid-side $LCL$-filter currents, respectively, with the superscript indicating which reference frame is leveraged; $e$ and $v_{\mathrm{g}}$ denote the $LCL$-filter capacitor voltage and the terminal voltage, respectively, with the superscript indicating the reference frame; $L_{\mathrm{i}}$, $R_{\mathrm{i}}$, $L_{\mathrm{g}}$, and $R_{\mathrm{g}}$ denote the inductive and resistive components of the inverter- and grid-side inductive parts of the $LCL$ filter, and $C$ denotes the $LCL$-filter capacitor; $I_{\max}$ denotes the maximum rated current of the inverter.

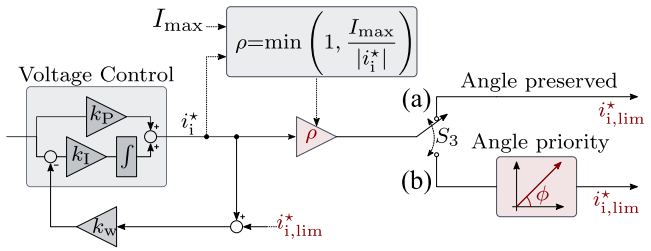


Fig. 3. Generic control structure of a current-reference saturation limiter (a) with fixing the output current angle, $\phi$, and (b) without fixing $\phi$.

## A. Direct Current-Limiting Methods

This section introduces and reviews state-of-the-art current-limiting methods that directly limit the GFM inverter current. This includes methods that saturate the reference signal feeding into the inner-current control loop (current-reference saturation limiting) or control the inverter switch signals to promptly limit the current (switch-level current limiting). These two methods feature superior dynamic current-magnitude limiting performance because they exploit the high control bandwidth of the inner-control loops or directly control the switch signals without going through the slower outer cascaded loops (e.g., the voltage control loop and the primary control loop shown in Fig. 2). As such, direct limiting methods quickly and accurately curtail the current. In what follows, we discuss the current-reference saturation limiter and the switch-level current limiter in more detail and review the pertinent literature.

*1) Current-Reference Saturation Limiting:* Fig. 3 illustrates a generic current-reference saturation limiting control structure where the current-reference signal, $i_{\mathrm{i}}^\star$—which is generated by an outer control loop, such as the voltage controller—is being

saturated to limit the output current during disturbances. The saturation gain, $\rho$, dynamically scales the current-reference signal, $i_{\mathrm{i}}^{\star}$, according to

$$\rho = \begin{cases} 1 & \text{if } |i_{\mathrm{i}}^{\star}| < I_{\max} \\ \frac{I_{\max}}{|i_{\mathrm{i}}^{\star}|} & \text{if } |i_{\mathrm{i}}^{\star}| > I_{\max} \end{cases} \tag{1}$$

where $|i_{\mathrm{i}}^{\star}|$ denotes the magnitude of the reference current and entails a separate calculation [22]. In the literature, various types of limiters are used to track and curtail the magnitude of the current, such as root mean square (RMS) limiters, circular limiters, and elliptical limiters. Mahamedi et al. [23] used a magnitude calculator to individually monitor phase RMS currents and limit phase currents. In [24], [25], a circular current limiter is proposed to limit the peak of the sinusoidal signal without causing distortion in the output currents, which could be caused by an instantaneous hard current limiter, such as clipping the sinusoidal current. Moawwad et al. [26] proposed an elliptical current limiter, which represents the locus for the total instantaneous current (i.e., positive and negative-sequence currents). The limits of the direct and quadrature components of the converter current are adaptively defined to fully use the overloading capability. Baeckeland et al. [27] used a resonant integrator to track the line-current amplitudes. In that work, the reference currents are proportionally scaled, referring to the maximum phase current if the limiter is activated. Computing the current magnitude cannot be achieved instantaneously; therefore, this step can cause delays in detecting an overcurrent and thus affect the response time, likely causing a momentary overcurrent and affecting the stability margins of the inverter [27]. More explanation on this is found in Sections V-A and V-B.

With the current-reference limiter in place, the limited reference signal feeding into the inner-current control loop, $\rho\, i_{\mathrm{i}}^{\star}$, can never surpass the maximum allowable current, $I_{\max}$, as shown in (1). Because of the high bandwidth of the inner-current control loop, the output current closely tracks the reference, $\rho\, i_{\mathrm{i}}^{\star}$, and with that, quick and accurate current limiting is acquired. Many works have described various implementations, depending on the type of reference frame used in the controls [23], [25], [27], [28], [29], [30], [31], [32]. (More discussion on reference frames is found in Section V-E.) As illustrated in Fig. 3(a), the current-reference saturation gain, $\rho$, rescales the magnitude of $i_{\mathrm{i}}^{\star}$ without manipulating the current-phasor angle. This retains the current-phasor angle demanded by the voltage controller. This type of limiting is presented in [24], [25], [27]; however, as shown in Fig. 3(b), it is possible—after saturating the magnitude of the reference signal—to manipulate and prioritize the active or reactive current during the disturbance [23], [31], [33], [34], [35], [36], [37]. Manipulating the current-phasor angle, $\phi$, can provide a tightly controlled output current during disturbances; however, it is worth contemplating whether this method retains the voltage-source behavior of the GFM inverter during limiting as desired (more discussion is found in Section V-C).

*2) Switch-Level Current Limiting:* Switch-level current-limiting methods directly modulate the switching command signals feeding into the semiconductor switching bridge to curtail the output current, as illustrated in Fig. 4. The switching command fed into the semiconductor switching bridge is blocked as soon as the instantaneous inverter output currents exceed the maximum current threshold. Because this method directly affects the switching command signals, i.e., bypassing other control blocks in series, rapid and accurate current limitations can be achieved. Du et al. [38], [39] proposed a switch-level current-limiting control strategy that immediately suppresses the currents during overloading using a hysteresis loop. By directly controlling the switching command signals, this method can limit the overcurrent in a few switching cycles, which is significantly faster than any other limiting method discussed in this work. Gurule et al. [40] and [41] demonstrated this method through experimental results; however, bypassing the entire GFM control structure and directly manipulating the switching command signals can cause controller instability and severely degrade power quality due to waveform peak clipping, as illustrated in Fig. 4. More so, this can lead to integrator windup in the hierarchical control loops. (More discussion on integrator windup phenomena during current limiting in Section V-D.) For those reasons, switch-level current-limiting methods are rarely proposed in the literature as the primary current-limiting technique in inverters. In conjunction with a primary current-limiting method, the switch-level current limiter can provide quick backup protection to secure the inverter hardware against high and fast-rising transient currents.

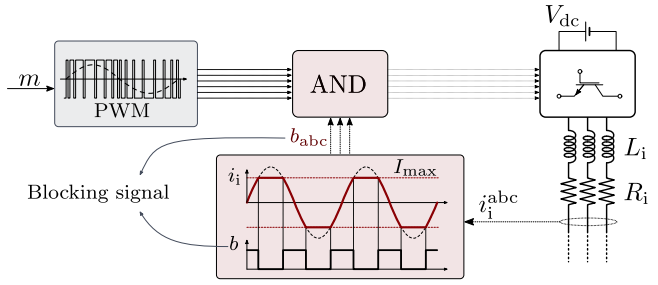


Fig. 4. Generic control structure of a direct switch-level current limiter.

## B. Indirect Current-Limiting Methods

This section introduces and reviews methods that indirectly limit the inverter output current by 1) modulating the power set points that feed into the primary GFM controller; 2) incorporating a virtual impedance (VI) in the voltage feedback loop; or 3) implementing a voltage limiter. Each category is discussed in detail.

*1) Power Set Point Modulation Current Limiting:* This current-limiting method aims to curtail the output current by adaptively reducing the power set points during overcurrent conditions. This method is studied in [42] and [43], where the power set points, $P^{\star}$ and $Q^{\star}$, are dynamically rescaled as a function of the magnitude of the output voltage, $E$ (see Fig. 5). In addition, by prioritizing reactive power during grid voltage drop conditions, the GFM inverter can support the grid voltage and straightforwardly comply with the grid codes requiring reactive current provision, e.g., IEEE 1547 (more discussion is found in Section VI). As illustrated in Fig. 5, the power set points feeding

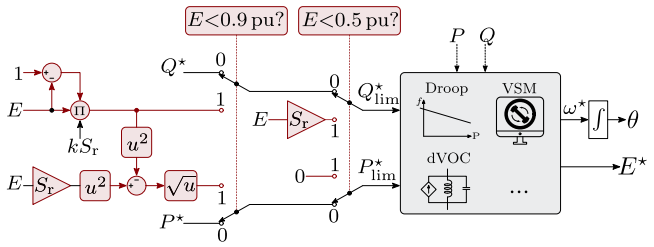


Fig. 5. Generic control structure of a power set point modulation current limiter.

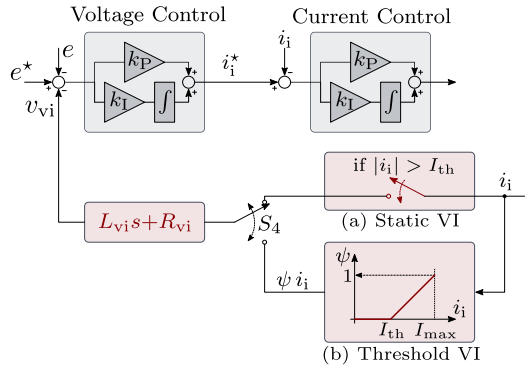


Fig. 6. Generic control structure of a (a) static and (b) threshold VI current limiter.

into the primary controller, $P^{\star}_{\text{lim}}$ and $Q^{\star}_{\text{lim}}$, can be modified as follows:

$$P^{\star}_{\text{lim}} = \begin{cases} P^{\star} & \text{if } E > 0.9\,\text{pu} \\ \sqrt{(E\,S_{\text{r}})^2 - (Q^{\star})^2} & \text{if } E \leq 0.9\,\text{pu} \end{cases} \tag{2}$$

$$Q^{\star}_{\text{lim}} = \begin{cases} Q^{\star} & \text{if } E > 0.9\,\text{pu} \\ k\,S_{\text{r}}\,(1-E) & \text{if } 0.5\,\text{pu} < E \leq 0.9\,\text{pu} \\ E\,S_{\text{r}} & \text{if } E \leq 0.5\,\text{pu} \end{cases} \tag{3}$$

where $E$ denotes the inverter output voltage in per unit, $S_{\text{r}}$ denotes the rated apparent output power in per unit, and $k$ denotes the ratio of the voltage drop at which the reactive power is injected into the grid, as often defined in grid codes [42], [43]. It is not clear, however, how power set point modulation current limiters can retain the GFM properties during faults and ensure effective, accurate, and quick current limiting. This method has the potential to improve transient stability by achieving equality of the power injection with the power set point during prolonged faults (more discussion is found in Section V-A); however, significant overcurrent cannot be avoided during the initial few fundamental cycles after fault inception due to the low-bandwidth outer controls (e.g., up to 10 fundamental cycles in [43]), which would require significant overcurrent headroom in the inverter hardware design and thermal management to avoid potential reliability issues and damage to the inverter. Further, note that power set point current-limiting methods are based on arbitrary criteria that only partially relate to the current magnitude, e.g., a voltage drop of 10%, as shown in Fig. 5. Equations (2) and (3) have no dependency on the maximum rated current, $I_{\text{max}}$. Therefore, current limiting within the inverter boundaries cannot be ensured. In addition, it is questionable whether this method works effectively during unbalanced faults, frequency drops, or phase jumps while retaining stability. These concerns make this method unsuitable as a stand-alone limiting method, and, therefore, should be combined with another limiting approach.

*2) VI Current Limiting:* During normal conditions, a GFM inverter can be represented as a voltage source behind an impedance, which remains small for voltage regulation. During overcurrent conditions, on the other hand, the inverter output impedance cannot remain the same. As the output current of the inverter is curtailed by a current limiter (independent of the limiter type) the equivalent output impedance of the inverter modulates as a function of fault severity and other conditions [44]. A VI current limiter curtails the current by increasing the inverter output impedance. By redirecting the sensed output current through a VI and subtracting the VI voltage drop from the voltage-reference signal, current limiting can be achieved [45], [46], [47], [48]. Note that, compared to direct current-limiting methods that modulate the current reference, VI current-limiting methods modulate the voltage reference, thereby preventing the voltage controller from commanding an excessive inverter output current. This concept is illustrated by the generic VI current-limiting control structure shown in Fig. 6. With the switch $S_4$, one can choose to enable a static VI, as shown in Fig. 6(a) [48], [49], or a threshold VI, illustrated in Fig. 6(b) [50], [51], [52], [53]. A static VI limiter activates a constant VI in a fault with a short rise time [48]. Since it handles overcurrents in an ON/OFF fashion, the static VI excessively limits the output current, even during light overloading conditions, yielding under-utilization of the inverter's fault current capabilities. Because the fault current provision is an essential metric for system protection and recovery, a static VI is often not a preferred limiting method [44]. Moreover, a static VI can lead to latch-up, in which the inverter stays in current limiting and cannot return to normal operation even after the fault clears [49]. Several of these drawbacks can be circumvented. First, one can multiply the current signal with a threshold function, as denoted by $\psi$ in Fig. 6(b). This threshold function only enables the VI current limiter when the inverter output current exceeds a certain threshold, $I_{\text{th}}$, and it gradually increases the VI magnitude as a function of the output current. This technique resolves the latch-up issue and limits the output currents closer to $I_{\text{max}}$. For the threshold VI limiter, the VI voltage drop, $v_{\text{vi}}$, can be described by

$$v_{\text{vi}} = (sL_{\text{vi}} + R_{\text{vi}})\, i_{\text{i}} \psi \tag{4}$$

where $L_{\text{vi}}$ and $R_{\text{vi}}$ denote the inductive and resistive parts of the VI, respectively. As illustrated in Fig. 6(b), the threshold function, $\psi$, can be defined by [52]

$$\psi = \begin{cases} 0 & \text{if } |i_{\text{i}}| \leq I_{\text{th}} \\ \frac{|i_{\text{i}}| - I_{\text{th}}}{I_{\text{max}} - I_{\text{th}}} & \text{if } |i_{\text{i}}| > I_{\text{th}}. \end{cases} \tag{5}$$

The function $\psi$ can take various forms, ranging from a discontinuous linear function of the inverter output current, such as

in (5) [52], to a nonlinear discontinuous function [27]. Making the function $\psi$ exponential can increase the fault current provisioning utilization of the inverter [27]. Also, a nonlinear $\psi$ can accommodate a smooth transition between activating and deactivating the VI, which eliminates unwanted transient phenomena [54]. A low-pass filter on the VI voltage can be opted to alleviate the noise created by the derivative action of the virtual inductance [43]. Notice that to avoid unwanted activation of the limiter during normal conditions, the threshold current, $I_{\text{th}}$, must be chosen equal to or greater than the nominal current. At the same time, $I_{\text{th}}$ must be smaller than the maximum rated current, $I_{\text{max}}$, to avoid overcurrent [52]. In other words, the output current should never exceed the maximum rated current, $I_{\text{max}}$, even in the worst-case scenario that is a bolted three-phase fault at the inverter terminals, i.e., minimum load impedance [45]. The magnitude of the VI is, therefore, tuned such that the current remains within its bounds during a bolted three-phase fault. One can define $|Z_{\text{vi}}|$ by

$$I_{\text{max}} \geq \left| \frac{e_0}{Z_{\text{g}} + Z_{\text{vi}}} \right| \approx \frac{E_0}{|Z_{\text{vi}}|} \Rightarrow |Z_{\text{vi}}| \geq \frac{E_0}{I_{\text{max}}}. \tag{6}$$

In (6), the impedance of the grid-side output filter, $Z_{\text{g}}$, can be neglected because during heavy limiting, the VI magnitude will be dominant [27]. Tuning the $\frac{X_{\text{vi}}}{R_{\text{vi}}}$ is less straightforward. According to [55], the $\frac{X_{\text{vi}}}{R_{\text{vi}}}$ ratio must be high enough to ensure that the inverter output impedance, during current-limiting operation, is primarily reactive from a droop control perspective [53]; however, some resistance in the VI is required for damping and, as such, to retain small-signal stability [10], [45]. (More on the effect of current limiting on small-signal stability in Section V-B.) Denis et al. [55] proposed a tradeoff where $\frac{X_{\text{vi}}}{R_{\text{vi}}} = 5$. In Section V-A, we delve into the effect of the $\frac{X_{\text{vi}}}{R_{\text{vi}}}$ on large-signal stability.

Despite these advanced VI current-liming methods, some inherent disadvantages must be considered. Because this type of current-limiting method uses the reference of the voltage controller, its current-limiting bandwidth is smaller than a direct current-limiting method that uses a faster, inner control loop; therefore, a VI current limiting can be too slow to limit the fast-rising transient peak current during the initial stage of a fault. Also, although making $\psi$ an exponential function can help, it is not possible to limit the overcurrent to $I_{\text{max}}$ with VI impedance limiting. The inverter's fault current provisioning capabilities, as a result, can remain underused by a few percentages [27].

*3) Voltage-Based Current Limiting:* The voltage-based current limiter curtails the inverter output current by decreasing the voltage reference feeding into the voltage controller during overcurrent. Though this is similar to VI current limiting, the voltage curtailment is computed in a different manner. During overcurrent, the limiter computes the voltage curtailment, $e^{\star}_{\text{lim}}$, such that the output current matches $I_{\text{max}}$. This concept is illustrated in Fig. 7. During normal operation, $e^{\star}$, generated by the primary controller, feeds into the outer-voltage controller. Once an overcurrent is detected, switch $S_2$ is activated, and the limited reference voltage can be computed as follows:

$$e^{\star}_{\text{lim}} = v_{\text{g}} + (L_{\text{g}}s + R_{\text{g}}) I_{\text{max}} e^{\jmath\phi} \tag{7}$$

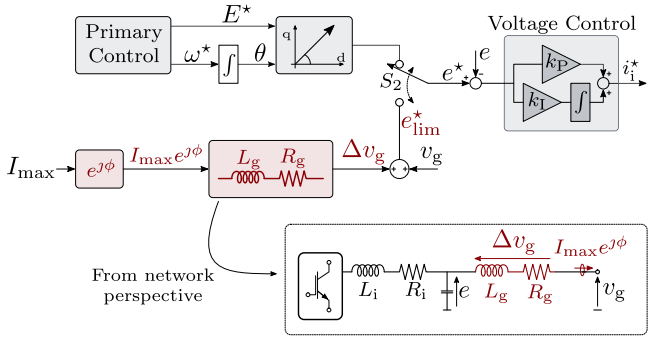


Fig. 7. Generic control structure of a voltage-based current limiter.

where $\phi$ is the desired output current angle with respect to the capacitor voltage, $e$. As illustrated in Fig. 7, this type of current-limiting can limit the grid-side current of the inverter to $I_{\text{max}}$ with a phase angle of $\phi$ [56], [57]. Note that regulating the output current angle requires knowledge of the grid voltage, which can necessitate the use of a PLL to track the grid voltage [58], [59]. Recently, the Western Electricity Coordinating Council approved a model of a GFM inverter that uses a voltage-based current-limiting approach [60]. These models require detailed information of the line parameters and the voltage of the grid [60], [61].

Notice that the GFM inverter becomes a controlled current source during current limiting, similar to a GFL inverter, which can have a destabilizing effect in weak grids [62], [63]. Bypassing the primary controller for current limiting can lead to frequency windup in the primary controller and complicate the fault recovery process. Complementing the voltage-based current limiter with a power set point current limiter can alleviate frequency windup to a certain extent; however, instability challenges due to frequency disturbances remain. The intricate interplay between voltage regulation and frequency stability underscores the need for comprehensive solutions that simultaneously address both aspects. Further, detecting overcurrent is a straightforward criterion to engage the limiter; however, deactivating the limiter cannot be commanded based on current measurements because the current is being fixed to $I_{\text{max}}$. Deactivating the limiter, therefore, requires an additional logic. All these phenomena can make it challenging to implement a voltage-based current limiter.

*4) Others:* Taking inspiration from the concept of VI current limiters, [64], [65], [66], [67] propose a nonlinear modified droop controller with current-limiting properties. The proposed controllers can limit the inverter current under normal or fault conditions without external limiters, additional switches, or monitoring devices. In [68], a fast symmetrical fault ride-through method is proposed using a hysteresis control. During the fault, new power references are calculated, and the synchro-converter switches to the hysteresis control to restrain inrush fault current. In [69], the output current of the inverter is limited by controlling the power angle. This approach ensures synchronization stability after a voltage sag or a frequency jump. In [70], [71], a frequency feed-forward term is incorporated into the active power-frequency droop controller; however, the technique

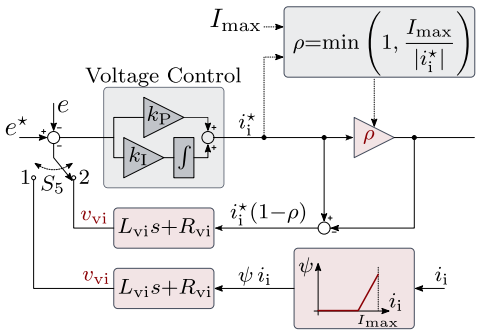


Fig. 8. Generic control structure of two hybrid current limiters, described in [44] ($S_5$ in position "2") and [74] ($S_5$ in "1").

suggested in [70] is applicable only to grid voltage sag scenarios, whereas the one in [71] is suitable only for grid frequency drop cases. Abrantes-Ferreira et al. [72] proposed a strategy to mitigate overcurrent in a weak grid by maintaining a constant voltage and controlling the power angle with local measurements; however, this approach can be ineffective in cases of overcurrent caused by significant voltage drops. Last, Groß and Dörfler [73] presented a method to restrict the output currents by projecting the GFM reference dynamics onto a constraint on the output current. The authors illustrate that this method can outperform conventional approaches such as VI limiting.

### C. Hybrid Current-Limiting Method

Both direct and indirect current limiters have advantages and disadvantages. Direct current limiters excel at rapidly constraining overcurrents, whereas indirect current limiters often outperform their counterparts in retaining GFM characteristics and transient stability (more discussion is found in Section V). The synergistic use of both types of current limiters exploits their unique strengths, enhancing the overcurrent limitation capabilities and affording greater control over the limited current. The hybrid current limiters proposed in the literature hold promise for enhancing the dynamic behavior of GFM inverters during faults, significantly contributing to system protection and facilitating post-fault recovery through improved grid synchronization.

Fig. 8 illustrates two prominent, recently proposed, hybrid current limiter methods. Qoria et al. [74] proposed to hybridize a VI current limiter and a current-reference saturation limiter, as conceptually illustrated in Fig. 8 (switch $S_5$ to "1"). The current reference that enters the current controller is curtailed by the saturation gain, $\rho$, in (1), while at the same time, the voltage reference is curtailed by the VI voltage drop, $v_{vi}$ in (4). For a severe fault, during the first few cycles after the fault inception, the current-reference limiter, known for its fast action, will dominate and constrain the fault current to $I_{\max}$. Once the initial stage of the fault has passed, the VI current limiter takes over because the threshold current for the VI current limiter is set lower than $I_{\max}$ in (5). On the other hand, Baeckeland and Seo [44] proposed the implementation of a VI embedded in the antiwindup path of the current-reference saturation limiting. This hybrid limiting concept is illustrated in Fig. 8 with switch $S_5$ set at "2," In this case, the current reference is limited by the saturation gain, $\rho$, at all times. The amount of current being limited, denoted by $i_i^\star(1-\rho)$, is fed to the VI. The voltage drop across that VI is subtracted from the voltage reference. Note that with this concept, the inverter's fault current provisioning capabilities are fully used, which is a distinct disadvantage of VI limiting. At the same time, this method allows precise control over the output impedance angle, resulting in superior voltage balance within the system. Another combination of VI and current-reference saturation limiting is proposed in [75] and [76]. This method entails the direct calculation of independent single-phase currents from the instantaneous measurements of voltages at the point of common coupling alongside the virtual back-electromotive force voltages calculated in the outer loop. Subsequently, each phase current is individually constrained by dedicated saturation limiters, ensuring precise control and management. Another hybrid method that combines a VI-based limiting with a fast sinusoidal current limiter is proposed in [77].

Apart from combining VI current limiting and current-reference saturation limiting, other hybrid limiting solutions have been proposed in the literature. A few works combine concepts of direct current limiting with a power limiter. In [78], a circular current limiter is used to limit the fault current, and at the fault clearance, a phase angle control loop is realized by changing the active power set point to ensure smooth and rapid post-fault recovery. Liu et al. [24] and Taul et al. [43] proposed a hybrid current limiter that selects between droop control and power-reference control based on grid code requirements, and a circular limiter is used to limit the current reference. In addition, in [43], virtual resistance is also momentarily added during the fault recovery to provide additional system damping, i.e., it is only activated for post-fault stabilization. Some works combine a VI current limiter and a power limiter. For a single-loop GFM inverter, Liu et al. [42] proposed a power-reference adjustment to limit the steady-state fault current of the inverter. In this method, a transient virtual resistor is used only during the inception and clearance of the fault to limit the transient overcurrent. An investigation of transient stability using a phase portrait analysis reveals that the adjustment of the outer power reference effectively retains synchronization between the GFM converter and the grid during grid faults. In [79], the current limitation is achieved by dynamically rescaling the reference voltage vector, $e^\star$, and active power reference, which combines concepts of voltage-based and power-based current limiting. The proposed strategy does not require any system knowledge and claims to retain the converter's GFM properties with successful symmetrical and asymmetrical fault ride-through. Zeng et al. [80] proposed to augment threshold VI with voltage information during current limiting to improve current-limiting performance, particularly during phase jumps. The combination of two direct current-limiting techniques is also possible. Calculating the RMS, which is required to determine the magnitude of the output current, can take up to one full fundamental cycle, leading to a delayed fault response of the GFM inverter [23]; therefore, Sadeghkhani et al. [25] combined a current-reference saturation limiter with a switch-level current limiter, which clips the fast-rising peak currents that surpass $I_{\max}$.

TABLE I
OVERVIEW OF DIRECT, INDIRECT, AND HYBRID CURRENT-LIMITING METHODS

| Current-Limiting Methods | Reference Frame | References | Key Features |
|---|---|---|---|
| Direct Current Limiter | dq-frame | [28], [29], [30], [31], [34] | Operates as a current-controlled source. Implemented either by saturating current reference [83] or directly controlling at switch level [38]. Current-reference saturation can be of three types: instantaneous [84], magnitude [85], and priority-based limiter [86]. |
| | abc-frame | [23], [25], [81], [82] | |
| | $\alpha\beta$-frame | [27], [24], [32] | |
| Indirect Current Limiter | dq-frame | [28] | Operates in voltage-controlled mode. Can be achieved by limiting power set points [87], adding virtual resistance or impedance [45], or limiting the output voltage [88]. May require dynamic adjustment of the VI or the power reference for improved current utilization. |
| | abc-frame | [87], [88] | |
| | $\alpha\beta$-frame | [27], [77] | |
| Hybrid Current Limiter | dq-frame | [74], [78] | Combines different current-limiting methods for better control over the fault current. Can exploit advantages of both direct and indirect current limiters. For example, one can use a current saturation to quickly suppress the fault current and VI for improved transient response. |
| | abc-frame | [42], [75], [76] | |
| | $\alpha\beta$-frame | [24], [43], [44], [77] | |

In summary, Table I provides a comprehensive overview of direct, indirect, and hybrid current limiters—subcategorized based on their reference frame used for implementation—along with relevant references. (More discussion on the reference frame and its effect on current-limiting performance is presented in Section V-E.) In the next section, we briefly look at how current-limiting concepts for three-phase GFM inverters can be leveraged for single-phase inverters.

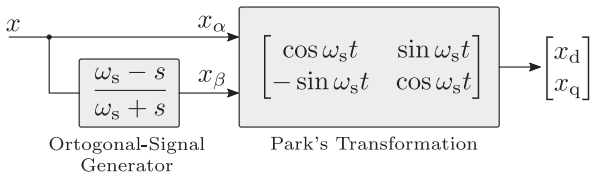


Fig. 9. Conversion of a single-phase signal in natural reference frame to synchronous reference frame using an orthogonal signal generator and Park transformation, where $\omega_s$ denotes the system frequency.

## IV. CURRENT LIMITING FOR SINGLE-PHASE INVERTERS

Single-phase GFM inverters are gaining prominence in modern power systems, notably for their applications in rooftop photovoltaic systems and single-phase solid-state transformers. Extensively distributed single-phase inverter-based generation can facilitate highly resilient systems capable of delivering uninterrupted power and bottom-up system restoration [89]. Therefore, developing robust current-limiting techniques becomes imperative for the widespread adoption of single-phase GFM inverters.

Many current-limiting techniques designed for three-phase GFM inverters can be engineered for use in single-phase GFM inverters. For example, in [90], current-reference saturation limiting is used in the dq-frame; however, as conveyed in Fig. 9, the control of a single-phase inverter in the dq-frame requires the synthesis of orthogonal components. Common methods for generating orthogonal signals include second-order generalized integrators (SOGI) [91], [92], and Hilbert transformations [93], [94], among others. These transformations may introduce delays and can potentially lead to stability issues during grid faults [95]. Therefore, adapting traditional current-limiting methods designed for three-phase GFM inverters to single-phase configurations can pose a challenge. To overcome the drawbacks of SOGI, improved orthogonal signal generation schemes are proposed in [96] and [97]; therefore, their application for single-phase GFM inverters under faults would be an interesting research topic.

To reduce the reliance on filtering techniques, such as SOGI or Hilbert transforms, direct control of inverter currents in the natural reference frame can be used, i.e., without converting signals to the synchronous reference frame, for which proportional resonant (PR) controllers can be leveraged. In the single-phase natural reference frame, concepts of current-reference saturation or VI current limiting can be implemented [98]. In addition to the more traditional limiting techniques, nonlinear current-limiting controllers for single-phase grid-tied inverters are proposed in [99] and [100] to improve closed-loop stability under both normal and fault conditions. This approach, based on nonlinear input-state stability theory [101], facilitates inverter currents to remain below a specified threshold even during transients, without the need for external limiters, additional switches, or

monitoring devices. However, a tradeoff exists—the controller can only operate at unity power factor, meaning reactive power control is unavailable. Building upon this concept, a more generic control structure presented in [64] achieves both current limiting and droop control while considering the system's nonlinear dynamics. This method offers greater flexibility compared to [99]. While these single-phase GFM current-limiting techniques show promising features, further research is needed to evaluate their efficacy across various operating conditions and system configurations for field deployment.

Conclusively, there are many ways to curtail the output current of three-phase and single-phase GFM inverters, with each of them intended to obtain a reasonable compromise between the device and system-level GFM limiting requirements as listed in Fig. 1. Sections III and IV acknowledged the vast majority of three-phase and single-phase GFM limiting methods; however, providing an exhaustive list of all the possible limiting methods along with their performance attributes lies outside the scope of this work. From here on, we continue the GFM current-limiting discussion based on the most prevalent limiting methods described.

## V. Impacts of Current-Limiting Methods

Based on the discussion on the operating principles and fundamental characteristics of different current-limiting methods, we now delve into their impact on the device-level and system-level attributes during and after faults, including transient stability, small-signal stability, voltage-source behavior, post-fault recovery, and the response to asymmetrical faults.

### A. Impact on Transient Stability

During severe disturbances, such as voltage drops, phase jumps, and frequency jumps, caused by faults or large transients in the network, an inverter can struggle to regain an equilibrium operating point or even lose synchronism with the connected grid. The conventional approach to transient stability assessment in traditional power systems is based on the rotor dynamics of SGs. Starting from the well-known swing equation of SGs, we can infer whether the rotor of an SG can retain synchronism with the grid during and after faults and disturbances [9]. Although GFM inverters do not have a physical rotor, they have an internal reference angle that is governed by the primary controller (see Fig. 2). By deriving the power-angle characteristics of a GFM inverter, we can leverage this classical approach to assess the transient stability of GFM inverters.

The primary controller of a GFM inverter generates a reference voltage and angle based on the output power and its set point. A variety of methods can be leveraged for GFM primary control [102], [103]. The most commonly described methods in the literature are droop control [16], VSM control [17], and dVOC [104], [105] (see Fig. 2). Hereafter, we explain the effect of current limiting on the transient stability of GFM inverters based on the droop primary controller, but the concepts are extendable to other primary controllers. The droop-control dynamics are captured by

$$\begin{aligned} \frac{\mathrm{d}\theta}{\mathrm{d}t} &= \omega^\star = \omega_0 + m_\mathrm{p}\,(P^\star - P) \\ E^\star &= E_0 + m_\mathrm{q}\,(Q^\star - Q) \end{aligned} \tag{8}$$

where $\theta$, $\omega^\star$, and $E^\star$ denote the reference angle, frequency, and voltage amplitude that feed into the cascaded inner controls, respectively. The nominal frequency and voltage are denoted by $\omega_0$ and $E_0$, respectively; $m_\mathrm{p}$ and $m_\mathrm{q}$ denote the droop gains; and $P$, $Q$, $P^\star$, and $Q^\star$ denote the active and reactive output power and the set points for power, respectively. In normal operation, the output power of the GFM inverter drives the inverter frequency to match the grid frequency, and therefore the GFM inverter is stable and synchronized with the grid. When a fault occurs in the grid, on the other hand, it is likely that the GFM inverter cannot drive its frequency to match the grid frequency due to the current limit. For example, upon a severe grid voltage drop in the grid, the active output power, $P$, drops according to (8), and therefore the GFM reference frequency increases, potentially causing the GFM inverter to lose synchronism with the grid in the event of a prolonged fault. From a control theory perspective, this can be understood as a form of integrator windup. This phenomena of losing synchronization during faults is not unique to GFM inverters and also exists with SGs (although with SGs, the driving force is of a physical nature rather than a control-induced phenomena); however, due to stringent current limits, GFM inverters are more prone to transient instability than SGs in the way described above.

In the following, we explore how the different current-limiting methods discussed in Section III affect the transient stability of GFM inverters using power-angle, $P-\delta$, curves. For GFM inverters, we define $\delta$ as the angle difference between the inverter output voltage, $E$, and the grid voltage, $V_\mathrm{g}$ (see Fig. 2). During current limiting, the inverter output voltage and angle cannot track the references generated by the primary controller. Since the transient stability of the inverter is determined by the dynamics of the internal angle, we use the virtual power angle, $\delta'$, instead of $\delta$. The virtual power angle, $\delta'$, is defined as the angle difference between $\theta$ (generated by the primary controller) and the grid voltage phasor angle, $\angle V_\mathrm{g}$, [106], [107]. In the following, we use the example of a voltage drop disturbance to explain the mechanisms of GFM transient instability. Notice, however, that the behavior of GFM inverters under other fault types, such as phase jumps, frequency jumps, or overloading, can be understood via the same $P-\delta'$ curves. Essentially, transient instability occurs when the angle $\delta'$ falls outside the stable region where the IBR can settle to a stable equilibrium point. For voltage drops and overloading, this can occur due to the discrepancy between $P^\star$ and $P$, whereas for frequency and phase jumps, this can occur due to the shift in grid-voltage phasor angle that directly affects $\delta'$. Next, we discuss in detail the impact of the commonly used direct and indirect current limiters on transient stability.

*1) Transient Stability Under Direct Current Limiting:* In Section III-A, we discuss two approaches to directly curtail

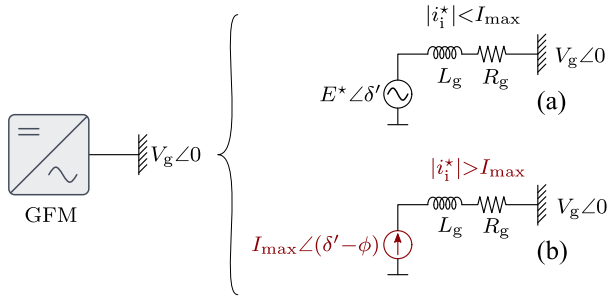


Fig. 10. Circuit equivalent of the considered GFM inverter during (a) normal operation and (b) current-reference saturation limited operation with current-phasor angle priority.

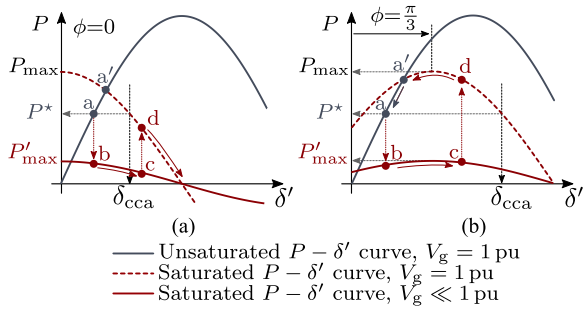


Fig. 11. Conceptual $P-\delta'$ curves for the current-reference saturation limiter and the angle trajectory during a generic voltage drop fault with (a) $\phi=0$ and (b) $\phi=\frac{\pi}{3}$.

the output current of the GFM inverter: the switch-level current limiter and the current-reference saturation limiter. For the latter, we distinguish between fixing the angle of the limited current (or prioritizing the active or reactive current) and preserving the current angle. We focus our discussion on the transient stability of the current-reference saturation limiter with angle priority because this is a common method described in the literature. Understanding the stability aspect of this method serves as a foundation for other methods and thus facilitates further development of improved limiting methods. Fig. 3 shows that with current-reference saturation limiting, the GFM inverter acts as a constant current source once the inverter current reference, $i_i^\star$, exceeds $I_{max}$. Consequently, we can represent the GFM inverter during both normal and current-limited operation as an equivalent circuit network, as depicted in Fig. 10. Notice that the angle, $\phi$, refers to the local reference frame, which is set by the primary controller angle, $\theta$ [70]. Based on Fig. 10, the output power, $P$, of the inverter can be approximated by

$$P=\begin{cases}\frac{EV_g}{X_g}\sin(\delta')=P_{max}\sin(\delta') & \text{if } |i_i^\star|<I_{max}\\ V_gI_{max}\cos(\delta'-\phi)=P'_{max}\cos(\delta'-\phi) & \text{if } |i_i^\star|>I_{max}\end{cases} \tag{9}$$

where $P'_{max}$ and $P_{max}$ are the maximum power transfer capabilities of the inverter with and without considering the current limiter, respectively. The grid-side inductive filter reactance is denoted by $X_g$, and $\phi$ is the current-reference angle, which is a tunable parameter in the case of current-reference saturation limiting (see Fig. 3). Notice that we assume the output inductive filter to be lossless for simplicity of analysis [70], [108]. How filter resistance affects power transfer and transient stability has not been well addressed in the current literature. Also note that (9) describes the power transfer under one specific type of current limiting. The limiter affects the output current angle and amplitude of the inverter and therefore yields a different $P-\delta'$ behavior. The $P-\delta'$ relationship may greatly differ depending on the type of current limiter and auxiliary dynamics [44], e.g., antiwindup (discussed in Section III-C), impacting large-signal behavior.

To explain the mechanisms driving the GFM inverter's transient behavior, we consider the inertia-less droop primary controller from (8) that is subject to a grid voltage drop. First, we consider the angle $\phi$ to be set to zero [70], [107], [108], [109]. A conceptual drawing of the $P-\delta'$ curves of this voltage-drop scenario is depicted in Fig. 11(a). Three $P-\delta'$ curves, as defined in (9), are projected. The unsaturated curve (solid grey) presents the $P-\delta'$ characteristic when the limiter is inactive and the grid is operating at nominal values. The dashed red curve represents the $P-\delta'$ characteristic for conditions when the current limiter is engaged and the grid is operating at nominal values. This occurs for $\delta'$ values beyond operating point a'. Last, the solid red curve represents the $P-\delta'$ relation for conditions when the current limiter is engaged and the grid is operating at an undervoltage condition. Note that not all points on these three curves are feasible operating points for the GFM inverter. First, we assume that the inverter in prefault conditions is operating at the equilibrium point "a" on the unsaturated curve and injects power matching $P^\star$, as visualized in Fig. 11(a). The current limiter is not engaged. At some point in time, a voltage drop occurs at the inverter terminals, forcing the inverter into current limiting. With no grid frequency or phase jump assumed, the output power immediately drops to point "b" in Fig. 11(a), and the $P-\delta'$ relation shifts from sinusoidal to cosinusoidal behavior, in accordance with (9). Due to the curtailed current and the degraded voltage, the output power, $P_b$, is smaller than the reference, $P^\star$, which causes the inverter's internal reference angle to accelerate according to (8). Inferring from Fig. 11(a), this situation will eventually lead to GFM inverter instability if left unaddressed: the output power cannot match the reference, and the inverter angle will continue to deviate, not settling, i.e., loss of synchronism with the grid. Stability will be retained only if the fault clears before $\delta'$ reaches the critical clearing angle (CCA), $\delta_{cca}$. To illustrate this, Fig. 11(a) shows a fault clearing at point 'c." The grid voltage is restored; however, the inverter angle $\delta'$ has drifted beyond $\delta_{cca}$. The inverter jumps to the unstable point 'd' and remains in current limitation. Consequently, $P_d<P^\star$, forcing the inverter angle to further accelerate and thus causing instability [see Fig. 11(a)]. The speed of the angle drift is determined by the inequality of the active power and its respective set point, as well as the primary control gains, as defined in (8). To streamline the discussion, we did not consider any inertia emulation in the primary controller. Synthetic inertia in the GFM primary control can lead to angle overshoot

and oscillations during and after a disturbance, which, in turn, reduces the transient stability margins of the inverter [108]. To analyze the transient stability with inertia, one must consider the equal-area method, which is well-described in classical power systems theories [9]. Besides that, the $P-\delta'$ curves remain the same.

In the aforementioned discussion, we considered the current-phasor angle, $\phi$, to be zero. By increasing the angle $\phi$, better transient performance can be obtained [33]. This is illustrated in Fig. 11(b), where $\phi$ is set to 60°. When a voltage drop occurs, the output power of the inverter drops from the equilibrium point "a" to point "b," after which the inverter angle starts accelerating ($P_{\mathrm{b}} < P^{\star}$). We clear the fault when the inverter passes point "c," and therefore it jumps to point "d." Note, with $\phi$ being 60°, the saturated $P-\delta'$ curves have shifted according to (9), and as a result, the $\delta_{\mathrm{cca}}$ has increased. At point "d," the power becomes $P_{\mathrm{d}} > P^{\star}$ such that angle deceleration ensues according to (8), after which the inverter ultimately settles back to stable equilibrium point "a." With this approach, $\phi$ cannot be set too high. If $\phi$ continues to increase, point "a′" will drop below the prefault point "a." If that happens, the inverter stays in current limiting and thus cannot return to point "a," even when the fault successfully clears within the CCA boundary; the inverter is confined to current limiting.

Leveraging power-angle characteristics to assess GFM transient stability is extendable to other types of faults and disturbances, such as frequency jumps, phase jumps, and overloading. Regarding phase jumps, the GFM inverter can withstand phase jumps up to $\delta_{\mathrm{cca}}$. The larger $\delta_{\mathrm{cca}}$, the more robust the inverter is against phase jumps [110]. Similarly, a frequency drop forces $\delta'$ to gradually deviate from the grid, according to the droop. A higher $\delta_{\mathrm{cca}}$ results in more tolerance against more severe and longer-lasting frequency jumps. In overloading, due to the current limiting, the GFM inverter cannot provide the load required, which can cause a voltage drop and an inverter angle deviation from the grid, posing a risk of loss of synchronism. The larger $\delta_{\mathrm{cca}}$, the longer the GFM inverter can ride through severe overloading. As such, the current-reference saturation-limited GFM inverter in Fig. 11(b) can ride through more severe phase jumps, frequency jumps, and overloading conditions, than the one in Fig. 11(a). In a similar fashion as discussed above, we can assess transient stability for other direct current-limiting methods such as current-reference saturation limiting with angle preservation. Compiling the correct power-angle characteristics is more challenging, but they can be found using numerical or simulation-based methods, as described in [111], [112]. Once the $P-\delta'$ curves are established, the same stability concepts can apply.

*2) Transient Stability Under Indirect Current Limiting:* In this section, we expand our discussion on transient stability of GFM inverters to indirect current-limiting methods. Among the indirect current-limiting strategies discussed in Section III-B, we focus on transient stability of GFM inverters with threshold VI current limiting because this is the most prevalent indirect limiting method described in the literature. The same insights and framework can be used to understand the impacts of other indirect limiting methods.

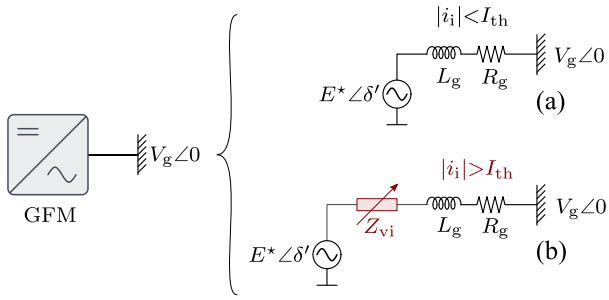


Fig. 12. GFM circuit equivalent during (a) normal and (b) VI current-limited operation.

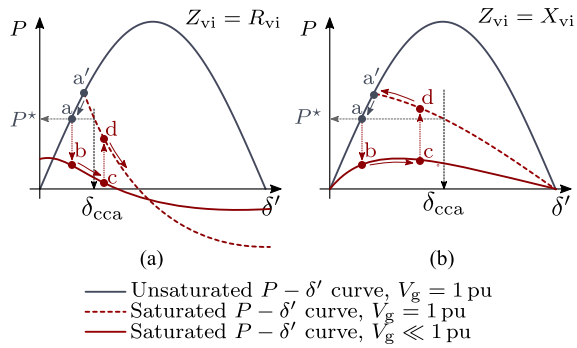


Fig. 13. Conceptual $P-\delta'$ curves during a generic voltage drop fault for (a) a purely resistive VI and (b) a purely inductive VI, as reported in [110] and [112].

The VI current limiter curtails the output current by reducing the voltage reference feeding into the voltage controller, thereby preserving the inherent voltage-source characteristics of the GFM inverter, as shown in Fig. 12. Writing down the power-angle relation during normal and current-limited operation yields

$$P=\begin{cases}\frac{E^{\star}V_{\mathrm{g}}}{Z_{\mathrm{g}}}\cos(\varphi_{\mathrm{g}}-\delta')-\frac{V_{\mathrm{g}}^2}{Z_{\mathrm{g}}}\cos\varphi_{\mathrm{g}} & \text{if } |i_{\mathrm{i}}|<I_{\mathrm{th}}\\ \frac{E^{\star}V_{\mathrm{g}}}{\not{Z}_{\mathrm{inv}}}\cos(\not{\varphi}_{\mathrm{inv}}-\delta')-\frac{V_{\mathrm{g}}^2}{\not{Z}_{\mathrm{inv}}}\cos\not{\varphi}_{\mathrm{inv}} & \text{if } |i_{\mathrm{i}}|>I_{\mathrm{th}}\end{cases}$$

where $\not{Z}_{\mathrm{inv}}\angle\not{\varphi}_{\mathrm{inv}}=Z_{\mathrm{vi}}\angle\varphi_{\mathrm{vi}}+Z_{\mathrm{g}}\angle\varphi_{\mathrm{g}}$. The arrow denotes a variable parameter: for threshold VI current limiting, $Z_{\mathrm{vi}}$ is a function of the output current and therefore not a constant [110]. In [110] and [112], the authors present the $P-\delta'$ curves for a dynamic VI, both for purely inductive and resistive VIs. Because the VI is dynamically adjusted as a function of the inverter output current, $Z_{\mathrm{vi}}$ becomes a variable, leading to unintuitive $P-\delta'$ curves. Fig. 13 illustrates these $P-\delta'$ curves for a generic voltage drop, as reported in [110] and [112], in a similar fashion as discussed in Section V-A1. We consider a purely resistive VI in Fig. 13(a) and a purely inductive VI in Fig. 13(b). The $P-\delta'$ trajectories are conceptually visualized for a generic voltage drop. Notice the significant impact of the VIs on the $P-\delta'$ relation and therefore how severely that impacts the transient stability. As visualized in Fig. 13, having a purely resistive VI can quickly lead to instability due to the small CCA; upon a voltage drop, the inverter follows the trajectory from point "a" to "d" after which it continues to drift into instability. On the

other hand, implementing an inductive VI greatly increases the CCA and thus enhances the transient stability against a fault, as shown in Fig. 13(b). The inverter with the inductive VI, after the generic voltage drop, now follows the trajectory a-b-c-d-a′-a and retains stability after the fault clearing. This aligns with the observation for direct current limiting, where the CCA of the GFM inverter increases when increasing the current angle, $\phi$. In a similar fashion as outlined for direct limiting methods, the $P-\delta'$ curves and the companion $\delta_{\text{cca}}$ can be leveraged to assess transient stability for various fault types, including phase and frequency jumps, and overloading.

Other works have also investigated the impact of VI-based current-limiting methods on GFM inverter stability. In [74], a range of VI magnitudes, spanning from zero to the maximum required impedance under worst-case conditions, are considered. The studies in [74] and [108] include an analysis of the critical clearing time under VI current limiting. The results confirm that the VI can improve transient stability for an extended period of fault duration in the system compared to current-reference saturation limiters. In [108] and [49], different adaptive transient control strategies are proposed to enhance the transient stability margins. Zhang et al. [112] Shen et al. [113] highlighted the influence of the VI's resistive or inductive properties in shaping the accelerating and decelerating regions during faults and the impact on transient stability. According to the equal-area criterion, a larger decelerating region enhances the stability prospects of GFM inverters [9]. Zeng et al. [80] illustrated that augmenting threshold VI current limiting with voltage information increases transient stability robustness during phase jumps.

In addition, various approaches have been proposed in the literature to further improve the transient stability of GFM inverters under current-constrained operation. One approach is to dynamically lower the power set point as a function of the grid voltage during a fault to increase the CCA and, as such, improve the transient stability [69], [114]. This approach can work well for voltage drops, but it remains ineffective during frequency jumps, phase jumps, or overloading, because the grid voltage may remain near the nominal value during such faults. In [115], the power set point is limited as a function of the frequency which improves transient stability for frequency deviations but not for voltage drops or phase jumps. Awal et al. [116] proposed a method to lower the power set point when the current limiter saturates using a PI compensator (i.e., while $\rho < 1$ in Fig. 3). As such, this method allows for lowering the power set point during any kind of disturbance that pushes the inverter into an overcurrent. This method has drawbacks. During voltage drops, simply reducing the $P^\star$ cannot alleviate current limiting, which can result in a continuous decrease of $P^\star$, and with it, the internal GFM frequency may still lose synchronism with the grid. Therefore, long-standing faults or overloading will lead this method to instability. Placing a lower bound on the $P^\star$ could help, but compromises the effectiveness for phase and frequency jumps. Further validation for more fault scenarios is required to draw clear conclusions for this method. A similar method leveraging PI controllers is proposed in [39]. Another approach is to reshape the $P-\delta'$ curve of the inverter through a separate control block. In [117], the integrator in the primary control (generating the reference angle) is temporarily frozen to the pre-fault operating point when the current limiter engages to avoid the loss of synchronism with the grid. Notice, however, that this strategy does not work well with phase- and frequency-jump-induced overcurrents. Kkuni and Yang [110] proposed a method that adds virtual power to the primary controller to manipulate the output power perceived by the primary controller and improve transient stability. A similar approach is proposed in [70] and [118], where the authors add an additional term that is a function of $\delta'$ in the primary controller to improve grid synchronization. Huang et al. [119] proposed to limit the power angle such that grid synchronization is enforced during any kind of disturbance that pushes the inverter into an overcurrent; however, limiting the power angle is achieved by following the grid-voltage phasor using a PLL, which basically renders the GFM unit into a GFL inverter as soon as current limitation is reached. Luo et al. [85] proposed adding saturation blocks at three different positions in the power control loop and demonstrate improved transient stability by either decreasing the acceleration area or increasing the deceleration area in the $P$–$\delta'$ curve. Notice that many of the above-described methods are trying to counteract the integrator windup in the primary control and, as such, act as antiwindup measures. The effectiveness of the aforementioned methods to enhance transient stability of GFM inverters during overcurrent conditions for a voltage jump ($V_{\text{g}}$-jump), frequency jump ($f_{\text{g}}$-jump), and phase jump ($\theta_{\text{g}}$-jump) is listed in Table II. It provides a general idea of how effective these methods are for the three different disturbance types without quantitative evaluation.

TABLE II
TRANSIENT-STABILITY ENHANCING METHODS FOR GFM INVERTERS

| Transient-stability enhancing method | $V_{\text{g}}$-jump | $f_{\text{g}}$-jump | $\theta_{\text{g}}$-jump |
|---|---|---|---|
| Freezing the GFM angle [117] | ✓ | – | – |
| Power set point scaling as a function of output voltage [43], [69], [114] | ✓ | – | – |
| Power set point scaling through PI controller [39], [116] | ✓ | – | – |
| Power scaling as a function of frequency [115] | – | ✓ | – |
| Manipulating GFM frequency as function of $\delta'$ (direct or indirect) [70], [110], [118] | ✓ | ✓ | ✓ |

All aforementioned references pertaining to transient stability assessment rely, explicitly or implicitly, on deriving and leveraging the relationship between $P$ and $\delta'$. Yet, this is not the only direct method; another approach to assess transient stability is based on Lyapunov's theory and energy functions. Although some works have illustrated the potential of this method for GFM inverter stability analysis [120], [121], [122], [123], more research is needed to practically and systematically apply this method for GFM inverters during current-limited operation.

In summary, both current-reference saturation limiting and VI-based current limiting offer distinct opportunities to improve transient stability. The current-reference saturation-limited GFM inverters can improve transient stability by increasing the current-phasor angle, $\phi$, whereas the VI-based ones

can improve transient stability by increasing the $\frac{X_{vi}}{R_{vi}}$ ratio of the VI. Nevertheless, for both limiting types, the transient stability margins are decreased during current limiting. Employing additional control methods to prevent wind-up of the primary-control reference frequency and angle can further enhance transient stability of GFM inverters. Even so, both direct and indirect current limiting methods introduce tradeoffs; setting the limiter purely inductive can lead to latch-up and issues in fault recovery for the current-reference saturation limiter or it can reduce small-signal stability margins for the VI-based current limiter (discussed next). Careful consideration of both transient (i.e., large-signal) and small-signal stability margins is therefore important when designing GFM controls with current limiters.

### B. Impact on Small-Signal Stability

In the above discussion about the transient stability of GFM inverters under current limiting, we pointed out that a more inductive GFM fault behavior during current limiting improves transient stability margins; however, there is an important tradeoff. Increasing the inductive characteristic of the limiter can reduce the small-signal stability margins of the GFM inverters, as reported in [10]. Other works that address the small-signal stability of GFM inverters during current-limited operation include [45], [124], [125]. In [45], a comprehensive small-signal analysis is presented to determine the optimal VI magnitude and $\frac{X_{vi}}{R_{vi}}$ ratio. The findings reveal that, while a high $\frac{X_{vi}}{R_{vi}}$ ratio (highly inductive) can result in insufficient damping, only an excessively low $\frac{X_{vi}}{R_{vi}}$ ratio (highly resistive) may induce small-signal instability. Miranbeigi et al. [125] pointed out that the presence of PWM delays can impact small-signal stability, especially in scenarios with low $\frac{X_{vi}}{R_{vi}}$ ratios. To address this challenge, a delay compensation method has been proposed in [125]. In addition, Wu and Wang [124] introduced an adaptive VI tuning technique to ensure small-signal stability. Paquette and Divan [45] analyzed the impact of the $\frac{X_{vi}}{R_{vi}}$ ratio in a system, where a GFM inverter is connected in parallel with a SG. Nevertheless, the issue of small-signal stability in multi-inverter systems remains insufficiently explored in the current literature. Although small-signal stability analysis of GFM inverters under normal operating conditions is well-established in the literature, only a few works include the impact of the current limiter. More research is needed to understand the tradeoff between large- and small-signal stability in GFM inverters under current constraints.

### C. Impact on Retaining GFM Nature Under Faults

The precise definition of the GFM capabilities of IBRs remains a topic of discussion within the community. Nevertheless, certain fundamental capabilities and principles are increasingly being articulated in new standards and grid codes. As described in [4] by the Australian Energy Market Operator and North American Electric Reliability Corporation, a GFM inverter should behave as a voltage source behind an impedance while in normal operation (within current capability limits). More discussion on GFM grid requirements is found in Section VI. Whether and how this voltage-source behavior should extend to current-limiting operation remains an open question; however, it is a common understanding that maintaining the voltage-behind-impedance nature of the inverters can improve grid stability and voltage support during faults, improve fault recovery, enable overload-bearing black start, and more [126].

As illustrated throughout this work, some current-limiting methods, such as the current-reference saturation limiter with a predefined current-phasor angle, render the GFM inverter into a controlled current source during overcurrent, as shown in Fig. 10. The outer voltage and primary controller are bypassed, and the GFM inverter loses its ability to regulate the terminal voltage [127]. Indirect current-limiting methods, such as VI current limiting, on the other hand, do not saturate the reference signal feeding into the current controller. As such, they retain the voltage-source behavior and control the terminal voltage (to a certain extent) while limiting the output current, as illustrated in Fig. 12. This can improve voltage support during balanced and unbalanced faults, enhance the synchronization of GFM inverters under an overloaded black start, and help existing power system protection systems, such as distance protection, remain effective and reliable in an inverter-heavy grid [12], [44], [128], [129].

Hybrid current limiters that combine direct and indirect current-limiting principles are, at first sight, difficult to unambiguously classify as either a voltage source or a current source during current-limited operation. For hybrid limiters that combine current-reference saturation and VI limiting, however, the control over the terminal voltage can be retained, as shown in [74] and [130]. Other works, such as [43], [79], [127], explore and propose hybrid current-limiting methods with the specific objective of improving large-signal stability during faults. How these methods translate in circuit equivalences and whether they retain a voltage-source behavior is not clear, though many of the works mentioned show potential of improved performance in various ways by combining a variety of limiting principles into a hybrid solution.

Conclusively, the current-limiting method plays a crucial role in regulating the voltage-source behavior of GFM IBRs, while respecting the inverters' limitations. To fully benefit from the GFM concept, further study is necessary. It is vital for all parties—such as inverter vendors, system operators, and regulatory bodies—to collaborate and identify robust solutions that are practical and cost-effective.

### D. Impact on Post-Fault Recovery and Synchronization

Enabling current-limiting controls during disturbances that push the inverter beyond its rated capabilities is a necessity to avoid irreversible hardware damage; however, once the fault clears, the GFM inverter should return to normal operation as quickly as possible and stabilize the grid. Immediately recovering the GFM voltage-control capabilities after a fault without adverse effects is not an obvious task, since the control parameters may have shifted to states that fall outside a normal operating range (e.g., control integrator states). As a result, GFM inverters can experience stability issues during their fault-recovery process, which can have device- and system-level impacts [35].

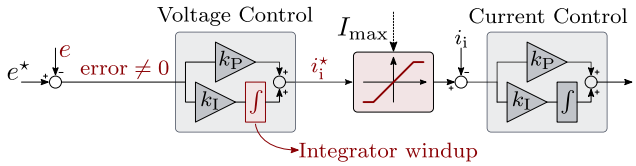


Fig. 14. Integrator windup issue during faults.

One typical issue is the windup of control integrators during current limiting. A common example is wind-up in the voltage controller; the current-reference saturation limiter curtails the signal feeding into the inner-current controller due to which the inverter cannot inject the required current to build up the output voltage, $e$, to satisfy the reference, $e^\star$ (see Fig. 2). The integrator of the inverter voltage controller continues to integrate the error due to the unregulated output voltage. If no countermeasures are taken, the integrator will accumulate a substantial error throughout the duration of the fault, as illustrated in Fig. 14. Note that this phenomenon can occur in any instance of cascaded control loops where reference signals in the inner loops are being curtailed.

Once the fault clears and the grid returns to nominal operation, the voltage control loop of a GFM inverter must quickly regain control over the terminal voltage; however, due to the accumulated error in the integrator, the reference commands can take a significant amount of time to return to a value within the normal range. Unless it immediately returns to normal operation, the inverter can continue to inject its maximum rated current into a healthy grid, which can lead to overvoltage at the terminals. This can be followed by premature and aggressive control corrections, leading to excessive oscillations in the current and voltage outputs. All of which can compromise the stability of the system immediately after fault clearance. More discussion on the post-fault instability caused by the windup is found in [131] and [110].

Integrator windup can be prevented by using proper antiwindup techniques. They are designed to avoid integrator accumulation that results from the discrepancy between the controller output and the actual control action realized, which can cause undesirable control behavior [52]. By reflecting the amount of unrealized control effort due to the limit in the preceding control signal (i.e., the amount of current exceeding the limit in the GFM application), the states of the outer-loop control can stay within a reasonable range to improve the post-fault control performance [132]. Note that the implementation of an antiwindup varies and modulates the dynamic control behavior [31], [111], [133], [134], [135], [136]. Pawar et al. [133] and Ghoshal and John [136] used conditional integration, and Ghoshal and John [136], Teodorescu et al. [134], and Richter and Doncker [135] used tracking integration. In [137] a two-axis antiwindup PI regulator is proposed to limit the current commands within a circular boundary. Even when antiwindup techniques are employed to address this problem, they require knowledge of the system parameters to ensure closed-loop system stability, which may not be available or may vary in practical situations [138]. Also note that, equipped with an integrator antiwindup, the inverter can still remain in current limiting after the fault clearing due to latch-up, resulting from the primary controller behavior (see Section V-A), which prevents the inverter from a successful fault recovery [131].

In contrast to current-reference saturation limiters, VI current limiters have a fundamentally different post-fault behavior. Rather than manipulating the current reference, they are designed to adjust the voltage reference as a function of the output current. At the cost of responsiveness and limiting accuracy, reducing the voltage reference naturally limits the fault current without winding up the inner control loops, allowing the GFM inverter to retain control over the voltage and current independent of the limiting conditions [35], [45], [74]. Notice that the primary controller, which governs the voltage and angle reference, can still be affected by integrator windup, which can cause transient instability, as discussed in Section V-A. Moreover, the results in [111] reveal that a GFM inverter with circular current limiters can also avoid these phenomena since the inverter behaves similarly to those with virtual resistors.

Hybrid current-limiting solutions can be sought to circumvent the issue of outer-voltage integrator windup while alleviating the negative effects typically seen with VI current-limiting methods. The hybrid limiter described in [44], for example, saturates the reference current signal and implements a VI in the antiwindup feedback loop. This way, no windup of the outer-voltage loop occurs, the voltage-behind-impedance behavior is retained, and the current-reference saturation ensures quick and accurate current limiting. Moreover, the VI in the antiwindup feedback loop gives control over the internal inverter impedance, which can drastically improve grid synchronization in the face of faults, fault recovery, and overloaded black starts [129].

In addition, integrator windup in the outer-voltage loop diminishes the control over the output voltage and current-phasor angles, which can compromise postfault synchronization with the grid. With current-reference saturation limiting without antiwindup measures, the output voltage becomes uncontrolled, which can aggravate a loss of synchronization. Adding antiwindup measures can help regain control of the output voltage, but the angle remains uncontrolled. In fact, [44] illustrates that the internal impedance of the GFM inverter becomes purely resistive when employing a current-reference saturation limiter with a conventional anti-windup feedback loop with a constant gain, without manipulating or prioritizing current-reference angles. VI current-limiting methods and hybrid solutions can circumvent this issue. They retain control over the output voltage and phasor angle, and as such, the internal impedance of the inverter. Nonetheless, integrator windup of the internal angle reference in the primary controller can still occur, which can lead to a loss of synchronization and transient instability. (Measures to avoid primary-control integrator windup are further discussed in Section V-A.) Gu and Green [139] and Sepehr et al. [140] discussed the synchronization principle after faults in light of angle dynamics in an inverter-heavy power grid. In [33], a theoretical approach is proposed to explain the post-fault behavior of GFM inverters with VIs.

Post-fault transients caused by inverter-current limiting can also cause system-wide issues [141], [142]. They can

compromise the recovery process and even activate protective relays. This, in turn, can result in unnecessary disconnections of inverters and potentially cause cascading events that can lead to a system failure. To avoid this type of catastrophic event, the current-limiting method should be carefully designed through system-wide studies. To mitigate this issue, a series dynamic VI model is proposed in [43], and a parallel VI model is proposed in [143]. These VIs remain active exclusively during the fault recovery phase of the GFM inverter and do not function as a current limiter.

### *E. Impact on Asymmetrical Fault Ride-Through*

Approximately 95% of faults occurring in power systems are unbalanced single-line-to-ground and line-to-line(-to-ground) faults, with only 5% being three-phase faults [144], [145]. Nevertheless, the literature on GFM current limiting lacks comprehensive coverage of strategies and fault ride-through methods specifically tailored for asymmetrical faults and unbalanced conditions [11]. Namely, during unbalanced overcurrent events, the GFM inverter current must be limited such that all phases individually do not exceed the maximum rated current. A current limiter designed for only balanced conditions does not guarantee correct current limiting in the individual phases, nor does it guarantee stable control without oscillations or properly maintaining the output voltage. Injecting balanced currents into an unbalanced grid can even lead to overvoltage in the unaffected phase(s) during the disturbance [82], [87], [146], [147]. As such, careful design of the current limiter with unbalanced conditions is imperative for a practical GFM inverter. Although the high-level principles of direct and indirect limiting methods still apply, some additional aspects must be considered.

During unbalanced disturbances or loading, positive-sequence, negative-sequence, and potentially zero-sequence currents will flow through the network. For the inverter to retain control over its output voltage during such unbalanced conditions, it must control both positive- and negative-sequence signals (and zero-sequence signals in the case of a four-wire inverter). The inverter's ability to do so heavily depends on which reference frame is used to implement the controls: the synchronous reference frame (dq-frame), the stationary reference frame ($\alpha\beta$-frame), or the natural reference frame (abc-frame) [148]. In each frame, unbalanced components appear in different ways, as illustrated in Fig. 15. In the following, we discuss the fundamentals of each frame and how they can be leveraged for GFM control and current limiting during unbalanced conditions.

*1) Current Limiting in Synchronous Reference Frame:* The synchronous reference frame, or dq-frame, is a popular reference frame for inverter control systems, often preferred for its simplicity. Namely, in the direct-quadrature (dq-) frame, balanced three-phase sinusoidal signals translate into two separate dc signals (given some decoupling techniques), allowing straightforward control design and analysis [149] for which conventional PI controllers can be used; however, unbalanced conditions superimpose a ripple at twice the line frequency, $2\omega_s$, on the dq signals, as illustrated in Fig. 15. Because the PI

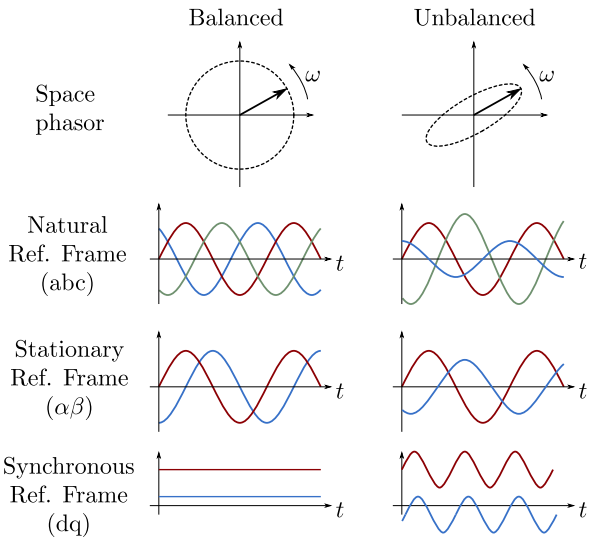


Fig. 15. Conceptual drawing of the effect of unbalance in different reference frames.

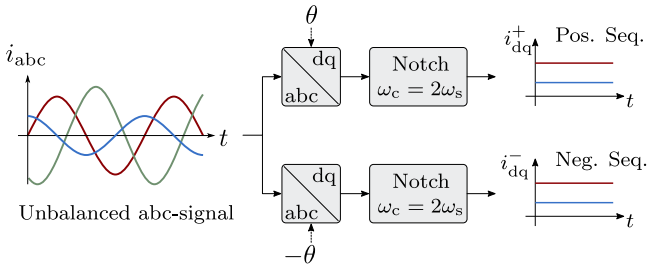


Fig. 16. Concept of sequence separation in the DDSRF using notch filters with the cutoff frequency, $\omega_c$, set to the double-line frequency, $2\omega_s$.

controllers are not designed to handle the double-line frequency signals, the dq-frame controls do not work properly for the negative-sequence components, requiring additional controls to address this. Consider an unbalanced set of $abc$ signals that we transform into the dq-frame using Clarke and Park transformations, the $2\omega_s$ oscillations are superimposed:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = [\mathbf{abc} \rightarrow \mathbf{dq}] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} (I_{DC})_d + A_d \cos(2\omega_s t + \theta) \\ (I_{DC})_q + A_q \cos(2\omega_s t + \theta) \end{bmatrix} \tag{10}$$

where $[\mathbf{abc} \rightarrow \mathbf{dq}]$ represents the Clarke and Park transformations, $\omega_s$ denotes the line frequency, and $A$ denotes the conceptual amplitude of the ripple signal. It is clear that the dq-frame, although a convenient option for balanced conditions, is insufficient for inverter control under imbalance. A solution to the issue is to separate the positive- and negative-sequence components and control each sequence in its own synchronous reference frame. This concept is called a double-decoupled synchronous reference frame (DDSRF) [150]. Separating the positive- and negative-sequence signals can be achieved by, for example, notch filters tuned at the double-line frequency, as conceptually illustrated in Fig. 16 [23], [151]. Other methods, such as delayed

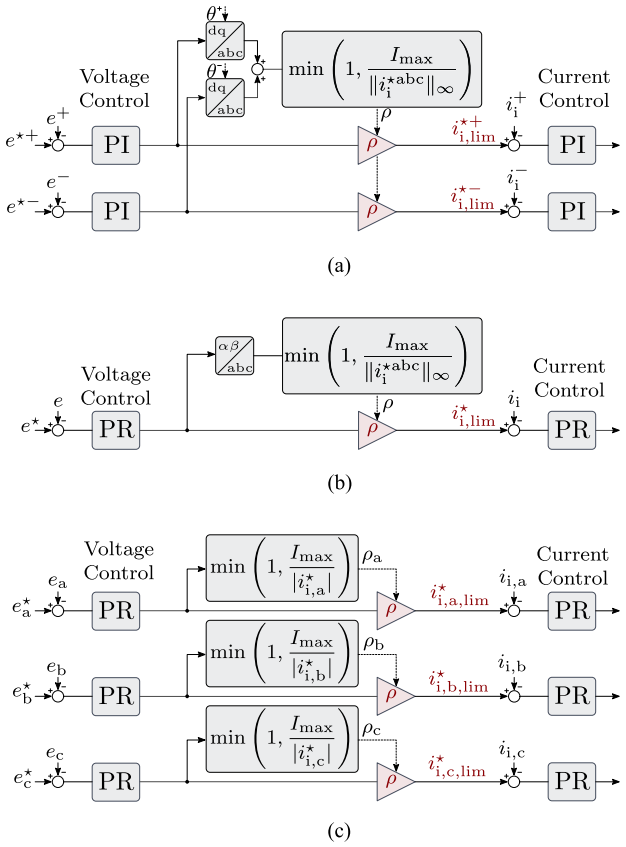


Fig. 17. Generic control structure of current-reference saturation limiters in the (a) double-decoupled synchronous reference frame, (b) stationary reference frame, and (c) natural reference frame.

signal cancellation, can be used for the same purpose [152]. Avdiaj et al. [153] proposed multiple approaches to generate a negative-sequence current reference under unbalanced grid conditions based on flexible control objectives.

In the DDSRF, direct or indirect current-limiting methods discussed can be leveraged. Freytes et al. [154], Awal et al. [155] proposed direct current limiters, and Li et al. [28] and, Avdiaj et al. [153] proposed VI current limiters in the DDSRF. In [155], an elliptical current limiter is used for asymmetrical current-reference generation for positive and negative sequences in a virtual oscillator control GFM inverter. Fig. 17(a) illustrates a generic current-reference saturation limiting method in the DDSRF.

In summary, GFM inverter control in the DDSRF allows for control and current limiting in unbalanced conditions. By using this frame, separate control over positive- and negative-sequence signals is possible if required (e.g., for prioritizing one sequence over the other); however, these benefits come at a cost. Due to the need to separate sequence signals, filtering techniques, such as notch filters, must be implemented, i.e., sequence components cannot be separated instantaneously. This can create significant delays in the control system that reduce the stability margins. To prevent small-signal instability from the reduced margin, the control bandwidth needs to be reduced, which makes DDSRF-based GFM inverters sluggish during transients [156]. As a result, this can have a negative effect on system-wide stability during and after faults [27]. Further, [155] notes that the relationship between converter phase currents and symmetrical components is highly nonlinear, and therefore controlling phase currents by managing symmetrical components causes challenges in control design and analysis. To address the limitations associated with the decomposition into symmetrical components, per-phase dq-control is proposed in [157], [158], [159] for three-phase four-wire systems. This approach involves individually controlling three single-phase quantities in the dq-frame. Therefore, the discussion on the current limiting of single-phase GFM inverters, as delineated in Section IV, remains pertinent in these contexts.

*2) Current Limiting in Stationary Reference Frame:* Some of the drawbacks of DDSRF, such as the sluggish response caused by sequence separation, can be alleviated by building the GFM controls in the stationary reference frame, or $\alpha\beta$-frame. In the $\alpha\beta$-frame, three-phase sinusoidal signals are transformed into two sinusoidal signals using the Clarke transformation, as illustrated in Fig. 15. For balanced three-phase signals, the transformation yields two sinusoidal signals with the same amplitude, one leading the other by $90^\circ$. Because of the sinusoidal nature of the control signals, PR controllers need to be used instead of PI [160]. In the $\alpha\beta$-frame, the degree of unbalance affects the angle and amplitude of the sinusoidal signals, i.e., no double-line frequency component appears; therefore, the PR controllers, tuned at the fundamental frequency, can handle the unbalanced conditions without additional techniques, such as sequence separation, and as such, avoid the resultant filtering delays [12], [27]. To exploit these advantages, [27], [77], [161] propose current limiters in the $\alpha\beta$-frame. Baeckeland et al. [27] proposed an improved current-reference saturation limiting method and a novel VI current limiter in the $\alpha\beta$-frame. The work illustrates the ability to reliably limit and control unbalanced conditions with high control bandwidths, which is challenging in the DDSRF. A combination of $\alpha$-axis voltage control and $\beta$-axis current control is explained in [161]. This method not only limits the output current of the faulty phase, but also keeps the healthy phase voltage constant during faults. Zarei et al. [77] implemented a fast sinusoidal current limiter and an adaptive VI-based voltage generator in the $\alpha\beta$-frame. Note that, despite the advantages of this frame, $\alpha\beta$-frame current limiters cannot prioritize one sequence over the other because unbalanced signals are not distilled into positive and negative sequences. If separate sequence control is required (e.g., imposed by grid codes), this is a significant drawback. Fig. 17(b) illustrates a generic current-reference saturation limiting method in the $\alpha\beta$ frame.

*3) Current Limiting in Natural Reference Frame:* The last reference frame is the natural reference frame, or abc-frame. Because the physical three-phase signals are already in the abc-frame, no transformation is needed. Similar to the $\alpha\beta$-frame, PR controllers must be used to track the sinusoidal signals. In that sense, this frame is similar to the stationary reference frame; however, it provides the possibility to fully control and limit each phase separately and independently from each other. In [25], [75], [76], [81], the authors propose limiting the current

in each phase independently. In [75] and [76], a hybrid current limiter is proposed where the inner control loop utilizes three separate Kalman filters to estimate the magnitude and phase of three single-phase currents, and then saturation blocks are used to limit each phase currents independently. The proposed approach can also flexibly limit the negative-sequence current as a percentage of positive-sequence currents based on grid code requirements. In [23], the current controllers work in the decoupled synchronous reference frame, while the current limiter operates in the natural reference frame, therefore, limiting each phase current independently under faults. By limiting each phase current separately, under an asymmetric fault, only the affected phase(s) will be current limited, while the healthy phase(s) can continue to operate normally, as illustrated in Fig. 17(c). This operation can be beneficial in, for example, grids with single-phase loads, because it can provide continuous service in healthy phases. Note that independently controlling and limiting each phase can induce the flow of zero-sequence currents [82], [146]. This type of individual phase control is, therefore, only truly possible for three-phase, four-wire inverters. The three-phase, four-wire topology may have an extra switch leg and a dedicated zero-sequence controller to regulate the zero-sequence current [162]. For three-phase, three-wire inverters, limiting the phase currents in the natural reference frame can cause overvoltage issues [82], [87], [146]. References Pokharelet al. [163] and Roh [164] suggested that four-wire inverters are more effective than three-wire topologies in terms of harmonic distortion, leakage current, capacitor voltage fluctuation rate, and total loss, particularly during faults and unbalanced conditions.

Conclusively, considering asymmetrical fault ride-through is imperative for practical current limiter designs. Each reference frame presents distinct advantages and limitations. The selection depends on requirements and tradeoffs regarding control accuracy, computational burden, controller design complexity, stability, and overall system performance during faults. Requirements imposed by grid codes, such as specific sequence injection, should also be considered in the reference frame selection and control design owing to the frame-specific merits and limits discussed. Further technological advancements in this area will help overcome the challenges.

## VI. Grid Codes for IBR Operation Under Current Limiting

For reliable power system operation and to safeguard the stability and continuity of the power supply under various grid conditions, grid operators enforce rules and requirements on generator units operating in their grids. These requirements are based on the characteristics of SGs and decades of operational experience; however, with the proliferation of IBRs in the grid, the need for inverter-oriented fault ride-through and dynamic voltage-support requirements has become prominent [12], [165]. Grid codes for IBR-heavy systems must evolve, considering the distinct merits and limitations of IBRs. In recent years, this has led to world-wide revisions and creations of grid codes. One significant change in many grid codes related to overcurrent limiting is the requirement for operation capabilities under off-nominal grid conditions. In the revised codes, inverters must stay connected to and remain synchronized to the grid over an extended range of off-nominal grid conditions, such as voltage and frequency excursions, for longer periods of time without tripping. This type of requirement directly relates to the current-limiting control discussed in this article [166], [167]. In addition, proactive actions during those off-nominal conditions should be implemented to benefit the entire system operation. They can include injecting short-circuit currents during a voltage drop to support the grid voltage and to avoid a total blackout by facilitating the fault detection and protection mechanisms [167], [168]. In case of unbalanced faults, some grid codes require the injection of reactive current into positive and negative sequences [147], [167], [168], [169]. The required amount of current injection is defined as a function of the amount of positive-sequence voltage drop or negative-sequence voltage rise during a fault.

As of today, most grid codes are primarily drafted within the paradigm of GFL inverter controls, in which the inverter behaves as a controlled current source during both normal and abnormal conditions. Programming specific active or reactive current injection during off-nominal grid voltage or frequency conditions in GFL inverters, as a result, can be straightforwardly implemented by modifying the current-reference saturation limiter. Since this type of modification does not affect the current source nature, the inverter can continue using a PLL to maintain synchronism with the grid. In GFM inverters, on the other hand, mandating a specific amount of current injection or rendering the inverter control into a current source contradicts the GFM principle of retaining the voltage-source behavior. For example, specific reactive current injection requirements can be programmed with the current-reference saturation limiter with fixed current-phasor angle, as discussed in Section III-A and illustrated in Fig. 3; then, the inverter may not retain the voltage-source behavior that likely provides more benefits to the power system operation under contingencies and the post-fault recovery, especially in weak grids. How to unlock and exploit the GFM capabilities under fault conditions and how to drive and reflect them in grid codes, however, is not clear as of today. Significant study is necessary to obtain a better understanding of GFM inverter operation under faults and to facilitate standardization. To fill this gap, we review the latest grid codes related to the fault and current limiting of IBRs. Though some are not specific to GFM inverters, understanding the motivation of the needs and trends in code changes would illuminate the pathways.

First, we discuss recently developed GFM inverter grid codes. In 2022, National Grid issued GC0137 for Great Britain's system operation [7], [170]. This code is designed to address technical issues in the grid with the increasing share of IBRs with GFM capabilities. Although not mandatory, this code would facilitate the integration of GFM IBRs by enhancing the understanding of the new technology and encouraging stakeholders to integrate GFM functionalities into their products. Related to current limiting, GC0137 specifies GFM-IBR operation under large frequency excursions (2 Hz/s) and short-circuit current injection under terminal voltage drops (down to 0 pu), both of which are likely to drive a GFM inverter into current limiting. These require

GFM inverters to ride through (i.e., maintain synchronism) and proactively react to faults in an extended operational range, which is well beyond what is typically required for non-GFM IBRs. The Universal Interoperability for Grid-Forming Inverters (UNIFI) consortium issued "Specifications for Grid-forming Inverter-based Resources Version 1" in 2022 and Version 2 in March 2024 [3]. Although it does not provide numeric performance metrics by design, it specifies GFM-IBR capabilities in abnormal conditions, including retaining GFM characteristics under faults, contributing to system-wide stability, and recovery after events, all of which depend on the current limiting design. It reconfirms the importance of the current-limiting design. In addition, the UNIFI specification discusses the response to asymmetrical faults that requires a GFM inverter to regulate a balanced internal voltage by allowing unbalanced currents, i.e., negative-sequence current injection. In addition, the European Network of Transmission System Operators [5], the Australian Energy Market Operator [4], and the North American Electric Reliability Corporation [2] are leading the way to draft requirements for GFM inverters.

We provide more specifics in the latest codes related to GFM operation under abnormal conditions. National Grid GC0137 [7] introduces a fault current injection requirement mandating GFM inverters to exhibit a fast current response compared to GFL inverters against faults. In this code, the GFM inverter is required to inject the reactive current into the grid within 5 ms following a grid voltage drop below 0.9 pu. Complying with this short time frame can pose a challenge if the response is not inherent to the GFM IBR, i.e., voltage-source nature. On the other hand, the grid code also requires that the active power response must not be faster than 5 Hz to avoid system resonance. To satisfy this requirement, the control dynamics during faults should be carefully designed while respecting the inverter's hardware limits. Also, notable are the latest IEEE standards, IEEE 1547-2018 [166] and 2800-2022 [167], since they detail the advanced functionalities needed from IBRs. In both standards, inverters should not trip but maintain synchronism with the grid during grid faults for an extended period of time, unless they are allowed or required to trip [166], [167]. Compared to GC0137, which requires power injection even during a total voltage collapse ($V_g = 0$ pu), the inverters under IEEE 1547 Category II, which is the most demanding category for abnormal operations, for example, are mandated to temporarily cease to energize under a voltage drop below 0.3 pu [166]. This can lead to under-utilization of the GFM inverter's capability if applied and can affect system stability in certain conditions. Future standards should establish requirements for GFM inverters that are engineered to offer extended ride-through capabilities to fully benefit from inverter-heavy power systems.

As discussed, new grid code developments are in progress, and revisions of current standards are ongoing; however, so far no standard has been established that clarifies GFM-IBR performance under fault conditions, which would allow the full utilization of the potential of GFM inverters. This is because the fundamental understanding of GFM inverter behavior is still being established. Research, development, demonstration, and deployment activities are paramount to establishing a deeper understanding of this underexplored topic and will be foundational in the development of widely accepted grid codes.

## VII. System Protection in IBR-Heavy Grids

Over decades of operating SG-driven power grids, traditional power system protection methods have proven reliable by leveraging the typical voltage-source-behind-impedance behavior of an SG. A few typical SG fault attributes used to that end include high fault currents supplied by the SG and a near-constant internal SG impedance that tends to be highly inductive. Overcurrent, distance, and directional protection are some examples of protection methods that employ these SG characteristics; however, IBRs in the system—of any type—complicate the reliable detection and clearing of faults. Inverters cannot provide high overcurrents, and the internal impedance angle is predominantly dictated by the controls and the design of the current limiter. As such, many questions circulate in the community about the protection of inverter-dominated grids, e.g., should inverter controls or hardware be modified to comply with existing protection schemes, or should protection schemes be adapted for inverters [8]. In this section, we discuss common protection schemes, focusing on how they are affected by inverters and how GFM inverters with current limits can provide solutions.

The most common protection scheme, particularly in low-voltage and medium-voltage grids, is overcurrent protection. This type of protection, and by extension directional overcurrent protection as well, relies on the presence of significant overcurrents to detect a fault in a power system dominated by SGs [171]. In an inverter-heavy system, however, detecting a fault by scanning for overcurrent can become arduous due to the limited overcurrent capabilities of inverters whose short-circuit currents barely exceed their rating [172]. Deploying GFM IBRs can potentially alleviate this issue because they can proactively respond to faults, i.e., by providing the maximum current available to facilitate the protection mechanism rather than providing reduced current or early tripping that may appear in GFL inverters. Because it originates from the inverter hardware limits, however, this issue cannot be fully solved by simply implementing GFM controls in the IBRs replacing SGs, especially in the areas of weak system strength. Oversizing the inverters is a straightforward solution and can enable extended GFM funtionalities [4], [7], but additional value streams for the overdesign should be clearly defined and implemented by system operators to justify the additional costs [173]. In an attempt to address the issue of detecting overcurrent, advanced adaptive overcurrent protection schemes have been proposed [174], [175], [176], [177]; however, selectivity is a major challenge [178].

Another widely employed protection scheme is distance protection, which is primarily used in medium- and high-voltage distribution and transmission grids. Based on local voltage and current measurements, distance protection schemes compute the impedance between lines and estimate the relative distance to a fault on that line [179]. Conceptually, distance protection works well when the sources at both ends of the protected line have a similar fault behavior [179]; however, with a mix of

TABLE III
ADVANTAGES AND LIMITATIONS OF CURRENT LIMITERS

| Current-Limiting Methods | Advantages | Limitations |
|---|---|---|
| Direct Current Limiter | **1.** Can precisely limit the fault current and exhibits superior current-limiting performance in steady state.<br>**2.** Switch-level current limiters are very fast, curtailing the output within a few switching cycles.<br>**3.** Leverages the maximum current-injection capability of the inverters.<br>**4.** Offers flexibility in setting the fault-current reference angle, which might aid grid-code compatibility. | **1.** Inverter loses voltage-source nature during current-limiting conditions.<br>**2.** Most direct current limiters require manipulate the current reference from the current controller, which excludes the option for single-loop GFM inverters (except for the switch-level current limiters).<br>**3.** Prone to instability caused by integrator windup and power quality issues. |
| Indirect Current Limiter | **1.** VI-based limiters retain the voltage-source nature during current-limiting conditions.<br>**2.** Can be realized with or without a current control loop; hence, they are suitable for both single-loop and multi-loop control.<br>**3.** Tracks the reduced voltage reference during the fault; therefore, post-fault grid synchronization is straightforward.<br>**4.** Minimal windup issues offer better transient stability. | **1.** For VI-based limiters, the selection of parameters requires system knowledge and assumptions regarding the worst case scenarios.<br>**2.** VI-current limiting can result in under-utilizing the converter's maximum current contribution capability.<br>**3.** Voltage-based limiters may need grid-voltage information using a PLL, which can cause stability issues in a weak grid. |

IBRs and SGs, where the IBR current limiter can—intentionally or unintentionally, as discussed in Section III—manipulate the phase angle of the current, the distance protection can make a wrong impedance-estimation decision [12]. Previous simulation and hardware-in-the-loop studies have shown that distance protection is prone to failure in lines with (GFL) inverters, especially during unbalanced line-to-line faults [180], [181], [182], [183], [184], [185], [186], [187]. On the other hand, studies that investigate the interplay between GFM inverters and distance protection remain sparse. Baeckeland [12] and Baeckeland et al. [128] demonstrated through simulations and hardware validation that traditional distance protection can properly function with GFM inverters equipped with certain control and current limiter design considerations. The study illustrates that with a highly inductive VI current limiter, the GFM inverter behaves similarly to an SG (as illustrated in Fig. 12), which benefits distance protection, especially in a grid where IBRs and SGs coexist.

Last, we discuss the effect of IBRs on line-differential protection. Line-differential protection computes the sum of the current flowing into and out of a line. According to Kirchoff's current law, this sum must always equal zero if there is no fault on the line [188]. When there is a fault on the line, this criterion is not met. This makes line-differential protection highly reliable. On the other hand, it requires reliable communication links to exchange the measurement data from both ends of the line, and it cannot provide remote backup protection. Unlike overcurrent and distance protection, which rely on specific attributes of SGs, the concept of line-differential protection is agnostic to the source type (either SGs or IBRs) feeding the line. For the same reason, line-differential protection is, conceptually, not affected by the control type of inverters, i.e., whether they are GFL or GFM. Though, some studies report that line-differential protection, especially the alpha plane differential protection scheme, can be affected by the altered fault current behavior of inverters [189], [190]. Nevertheless, with some modifications in the relay settings and high-bandwidth communication, line-differential protection remains a reliable protection system for IBR-heavy grids [191], [192].

In summary, the presence of IBRs can complicate the protection of power systems due to known challenges, such as low fault current levels, as well as unknown factors that arise from the unpredictability of IBR behavior. Compared to GFL IBRs, GFM IBRs can alleviate concerns and benefit system protection by proactively responding to faults with fault current provision, but their benefits could be limited due to the hardware limit, which motivates inverter oversizing [173]. The compatibility of inverter controls and current limiter topologies with existing protection schemes is often overlooked but deserves attention in the inverter design process. On the other hand, advancements in protection technology, aided by novel communication methods and developed information technologies, can enable a paradigm shift in power system protection. Detailed electromagnetic transient modeling and simulation studies are essential to understanding changes in protection system behavior under faults in inverter-heavy grids and to guide the energy mix transition while ensuring reliable system protection.

## VIII. CONCLUSION

This article explored various aspects of the current-limiting methods employed in GFM inverters. This final section consolidates key points, provides a cohesive narrative, and offers our perspective on the findings and existing research gaps presented in the review.

The primary objective of current limiters is to curtail the output current of the inverter, protecting the inverter hardware from overloading and thermal damage. Although seemingly straightforward, the design intricacies of current limiters ripple through the power network, impacting many aspects of the power system, including stability, grid support during disturbances, protection, post-fault recovery, and more. This paper highlighted the challenges of developing GFM current limiters and inverter controls that perform well on all these fronts. Although no one-size-fits-all solution exists, the review identified specific design aspects that confer distinct advantages. In the

following, we highlight the most notable ones (a summary is provided in Table III).

A well-established method to limit the inverter output currents is curtailing the reference signal feeding into the current controller. Current-reference saturation limiting provides responsive and accurate limiting; however, if left untreated, it can create integrator windups in the outer control loops and does not provide control over the current and voltage phasor angles. The latter is particularly important for improving transient stability and grid synchronization, boosting the voltage during grid voltage sags and faults, and facilitating power system protection. Adding antiwindup feedback loops and prioritizing reactive or active current in the limiter block can help alleviate some of these issues.

VI current-limiting methods, on the other hand, do not create the windup of the outer-voltage loop control integrators and can provide control over the current and voltage output phasors during faults and disturbances. For that reason, they report better performance in terms of transient stability, voltage support, and power system protection. On the downside, VI current limiting curtails the voltage-reference input fed into the outer-voltage loop, which, therefore, is inherently slower than the current-reference saturation limiting methods, potentially causing momentary overcurrents and thus requiring an increased design margin or use in combination with an additional method for inverter protection and reliability. Also, VI current limiting cannot fully use the overcurrent capability of the inverter. Careful consideration of these tradeoffs is essential when using a VI current limiter.

This review also discussed recent works that propose hybrid current-limiting solutions that combine the merits of two methods. Although more research is needed, these papers show promising results regarding reliable current limiting, angle control, stability, black start, and system protection. Although tradeoffs are unavoidable because of the hardware constraint of limited inverter currents, hybrid current-limiting methods elucidate a pathway for future developments.

Last, throughout this work, several gaps in the current state of research became apparent. Hereafter, we list the most notable points for further research and remaining challenges in the space of GFM inverters during current-limited operations:

1) Although the effect of current limiting on the transient stability of GFM inverters during disturbances is covered extensively in this article, very few references take small-signal stability into consideration. Since engineering improved current-limiting behavior in large-signal response can trigger small-signal stability issues, mapping out the sweet spot between optimizing for small- and large-signal stability in GFM inverters during current-limited operation is a point for further research.
2) In this article, we outlined a general picture of the challenges associated with protecting GFM inverter-driven grids (or IBR-driven grids, for that matter); however, solid and widespread solutions both from power-system and power-electronics perspectives are lacking in the current literature. Developing solutions for power system protection incorporating the current-limiting behavior of GFM inverters would require more effort within the community.
3) This article has shown that there are many different ways to achieve effective current limiting in GFM inverters; however, we do not yet understand how well these different GFM current limiting methods will interoperate with each other. While this study provides a fundamental basis, future power grids will feature thousands, if not millions, of GFM inverters coexisting with other generation assets. Understanding how these various GFM current-limiting and fault-behavior strategies interact with each other and other sources in terms of system stability and protection is critical but mostly unknown.
4) Arguably one of the most pressing gaps in the development and deployment of GFM technology is the lack of GFM inverter-tailored grid codes. In fact, many of the aforementioned GFM challenges could be overcome with well-designed grid codes that clearly outline the required behavior of GFM inverters under off-nominal conditions. Novel GFM-tailored grid standards can streamline GFM developments, build clarity and common ground among stakeholders, and facilitate field deployment of this promising technology.

In summary, more efforts are necessary to understand GFM inverter behavior under current limiting and to illuminate the pathway to well-defined and widely acceptable grid codes for GFM IBRs and IBR-heavy grids. Research, development, and demonstration activities are crucial to clearly defining how GFM inverters should behave under current-limiting and off-nominal conditions.

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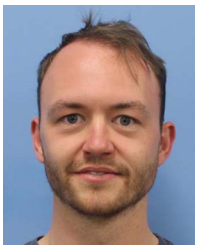

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