# Toward High-Throughput Deposition of III-V Materials and Devices Using Halide Vapor Phase Epitaxy

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# Toward high-throughput deposition of III-V materials and devices using halide vapor phase epitaxy

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## ABSTRACT

III-V devices are used in countless applications due to their excellent physical properties. They could become more prevalent, especially in area-intensive applications such as solar power, if they can achieve significant cost decreases through increasing scale. The development of high-throughput growth systems can help to achieve this scale, leading to the use of III-V devices in areas where they are not currently economically feasible. Here, we describe a pilot-production, pseudo inline HVPE reactor with the potential to greatly increase the throughput of III-V devices. We show computational modeling results that both informed system design and the understanding of the impact of different process parameters on the deposition. We show the throughput possibilities of this reactor with an example solar cell device design but note that this system is agnostic to the device structure and can be used to increase the throughput of lasers, LEDs, transistors, and more III-V devices.

**Keywords:** HVPE, low cost, high throughput, III-V, photovoltaics.

## 1. INTRODUCTION

III-V materials and devices are of tremendous technological importance, owing to their combination of tunable, direct bandgaps that correlate with useful parts of the electromagnetic spectrum and their excellent optical and electronic properties. One reason for their success in many types of devices, including lasers, light emitting diodes, solar cells, transistors, etc., is that they can be deposited with very high levels of crystalline perfection using a number of vapor phase growth methods. Both molecular beam epitaxy and organometallic vapor phase epitaxy have a long history of producing high-quality III-V materials and high-performance devices. Before these techniques were fully developed, halide vapor phase epitaxy (HVPE) was known for its ability to produce very pure III-V materials, but until recently the device structures attainable using this deposition technology were somewhat limited.

The recent reemergence of HVPE for the growth of relatively complex high-efficiency solar cell structures [1] gives scientists and process engineers another option for III-V deposition when it may not be entirely clear that another option was needed. However, HVPE growth holds substantial promise for the manufacturing of III-V materials and devices at a scale that is not clearly attainable today. Scale is the largest available lever to reduce deposition costs [2], and costs currently limit area-intensive III-V devices such as solar cells to niche markets that can afford the device performance premium.

Here, we describe a first-of-its-kind, pilot-production HVPE reactor that has the potential to reach device production scale unattainable by any III-V deposition system available today. We describe some of the design aspects that enable the system operation and show the potential for high throughput deposition of a common solar cell structure. This reactor, while designed for solar cell production, is agnostic to the device design and can be used for many useful III-V devices.

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# 2. PILOT-PRODUCTION D-HVPE SYSTEM

## 2.1 System description

Figure 1 shows a photograph of the pilot-production HVPE reactor installed at the National Renewable Energy Laboratory (NREL). The system was co-designed by NREL and Kyma Technologies (Raleigh, NC), with Kyma leading the construction. This reactor, like our previous R&D HVPE system [3], uses multiple growth chambers for the deposition of different device layers. Moving the wafer between growth chambers instead of changing flows within a chamber is essentially required when making multilayer structures using HVPE, but importantly, this need also leads directly to the possibility of fully inline deposition, which is a necessary leap beyond today's batch technologies. The need to move the wafer is due to the *in situ* generation of reactants within the chamber and the need to purge those reactants, and reestablish a new steady state, before the growth of a layer with a different composition. Growth of heterostructures without motion between chambers leads to significant growth of unintentionally graded material that may impact device performance [4]. The pilot-production reactor has three growth chambers that exist within a common vacuum chamber, plus another two chambers in the same vacuum space: one for heating and deoxidizing the substrate, and one for post-growth cooling. In addition, there are individual loadlocks for loading the substrate and unloading the finished wafer. In this way, the system represents a "pseudo inline" reactor in that wafers are loaded on one side and removed from the opposite end, although there will necessarily be back-and-forth motion between the growth chambers to build up the required device stack. The system is capable of deposition on industry-standard 6" substrates. Each growth chamber has the ability to grow (Al,Ga,In)(As,P) alloys with both p-type and n-type doping, leading to flexibility in the deposition procedure (see below).

Figure 1. Photograph of the pilot-production HVPE system installed at NREL.

## 2.2 Select design considerations

Each of the growth chambers, as well as the heat-up and cool-down chambers, exist in a common vacuum space to allow for mechanical motion of the substrate from one chamber to another. One concern in an open design such as this is the potential for cross contamination, that is, reactants from one growth chamber migrating to another and unintentionally incorporating into the material being grown there. This can obviously lead to the deposition of unintended material that can negatively impact device performance and should be minimized. We devoted significant modeling resources to understanding the impact of different physical designs and process parameters on the potential for crosstalk. We cannot provide greater detail on these modeling efforts due to the sensitive nature of the system design. However, Figure 2 shows the results of computational fluid dynamics (CFD) modeling quantifying the amount of arsine gas that unintentionally leaks outside the process space, e.g., outside one of the growth chambers, as a function of certain process variables. Figure 3 shows the results of a related study that provided understanding of the impact of process parameters



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on the uniformity of the precursor gases at the substrate surface. These and other CFD results yielded valuable design guidance for the system itself, as well as understanding of how process variables are expected to impact practical effects such as growth rate, spatial uniformity, cross contamination, and material utilization.

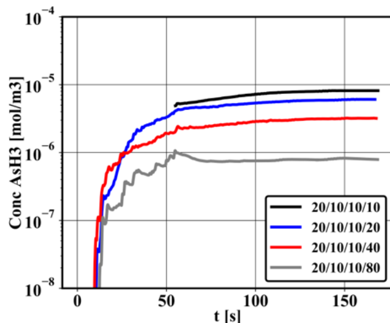


Figure 2. Results of computational fluid dynamics modeling showing a reduction in unintentional precursor leakage as a function of process parameters.

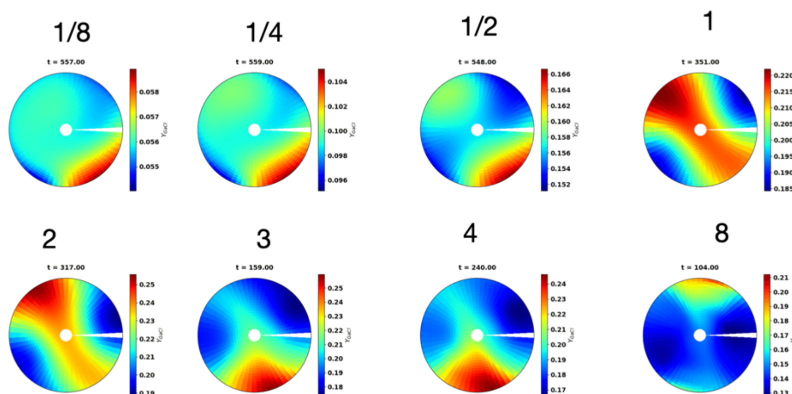


Figure 3. Results of computational fluid dynamics modeling showing the impact of changing process parameters on the uniformity of the GaCl concentration on the 6" substrate.

## 3. D-HVPE SYSTEM THROUGHPUT

As discussed above, the HVPE reactor enables pseudo inline operation, with a wafer entering from one side and coming out the other. Each growth chamber can deposit any alloy from the (Al,Ga,In)(As,P) material families, leading to significant design flexibility when choosing which chamber to use for which device layer. Table 1 shows an example of the sequence required to deposit a two-junction GaInP/GaAs solar cell using the back-and-forth pseudo inline process enabled by this system. The arsenide and phosphide materials are colored red and blue, respectively, in the table, and the three growth chambers are denoted GC1, GC2, and GC3. This is just one of countless possible procedures for the deposition of this particular structure. Growth does not need to start in GC1 nor end in GC3. It is possible to design a process that, for example, avoids switching from the growth of an arsenide to a phosphide, or *vice versa*, within a single chamber should that be required for the creation of high-performance structures. This example sequence represents the growth of a solar cell structure, however it is also evident that the layer compositions and ordering can be changed to create any number of III-V devices, including transistors, LEDs, different types of multijunction solar cells, and more.

HVPE has a demonstrated ability to deposit different materials with growth rates from sub-nm/s to several µm/min levels. We previously showed GaAs growth rates in excess of 500 µm/h [5] and GaInP rates over 200 µm/h [6] before reaching the limits of our mass flow controllers. Neither material showed quality degradation at these rates, and the still-increasing growth rate trends imply that even faster rates are possible. It is not required in this pseudo inline process to



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match the deposition time of each layer as it would be in a fully inline system where wafers move in concert. However, we believe, given previously achieved growth rates, that all of the layers in the device structure shown in Table 1 can be deposited in < 30 s without approaching any physical limits. Even the much thicker absorber layers can be deposited in < 30 s with previously demonstrated growth rates. The caveat to this is that it is currently unknown how long it will take to change the chemistry within one growth chamber in order to switch from the growth of one material to another [7]. This may ultimately limit the throughput of the pilot-production, pseudo inline system, but this limitation would not exist for a future, fully inline system that has a growth chamber devoted to each device layer. Even without increasing the growth rate for the thicker absorber layers, Table 1 shows that the total growth time for this two-junction solar cell structure is < 8 min. With reasonable assumptions related to equipment uptime and material yield, this pseudo inline system should be able to produce as much as 300 kW/yr of high-efficiency solar cells. This represents – from one growth system – a significant fraction of the worldwide production capacity for these devices today and represents a viable pathway to tremendous scale for the purpose of lowering cost. The time-per-wafer throughput metric is obviously device specific, but this HVPE reactor should be able to produce devices of similar complexity at a rate of ~ 50,000 – 100,000 6” wafers/yr.

Table 1. Example of the process flow for the deposition of a high-efficiency GaInP/GaAs two-junction solar cell. Arsenide materials are colored red, and phosphides are blue.

| **Layer/Process** | **Location** | **Thickness (nm)** | **Deposition time (s)** | **Device purpose** |
|---|---|---|---|---|
| Heat up | Heatup chamber | | | Oxide removal |
| GaAs | GC1 | 300 | 20 | Epitaxial liftoff protection layers |
| GaInP | GC2 | 100 | 20 | |
| AlAs | GC1 | 10 | 20 | |
| GaInP | GC2 | 100 | 20 | |
| GaAs | GC1 | 300 | 20 | Contact |
| n-AlInP | GC2 | 20 | 20 | Window |
| n-GaInP | GC3 | 100 | 20 | Emitter |
| p-GaInP | GC2 | 1100 | 120 | Absorber |
| p-(Al,Ga)InP | GC3 | 100 | 20 | Back surface reflector/tunnel junction |
| n-(Al,Ga)InP | GC2 | 100 | 20 | Tunnel junction |
| n-GaInP | GC3 | 30 | 20 | Window |
| n-GaAs | GC2 | 1800 | 120 | Absorber |
| p-GaInP | GC3 | 300 | 20 | Emitter |
| Cool | Cooling chamber | | | |
| | | Total deposition time → | 460 s | |



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# 4. CONCLUSIONS

The largest lever on the cost of III-V devices is production scale, and the development of growth systems with much higher throughput can aid in increasing scale, and therefore, in reducing cost. We recently designed and built a first-of-its-kind, pilot-production, HVPE reactor for the deposition of III-V solar cells. We used CFD modeling to aid the design process and to understand the impact of process variables on growth rate, spatial uniformity, and other measurables. This reactor is designed to deposit high-efficiency solar cell structures in minutes, and the reactor design can accommodate any arbitrary device design, leading to the possibility of increased throughput and scale in a number of III-V device industries.

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