Development of a Hybrid Single/Two-phase Capillary-Based Micro-Cooler using Copper Inverse Opals Wick with Silicon 3D Manifold for High-Heat-Flux Cooling Application

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Abstract— **Previously, two-phase capillary-based cooling from narrow (200 to 1000 µm) heater bridge copper inverse opal (CIO) wicks with heat flux levels exceeding 1400 Wcm^{-2} with low superheat ~ 10 °C was demonstrated. Here, we demonstrate the area scaling of the proposed technology to large-area micro-cooler for the high-heat-flux cooling of microprocessors and power electronics. We developed a hybrid single/two-phase micro-cooler that relies on capillary-wicking in a 25-µm-thick Copper Inverse Opals (CIOs) with an open channel silicon 3D-manifold for liquid delivery and vapor extraction, to achieve a high heat flux ~ 400 Wcm^{-2} over a heated area of 1 cm^2. For the range of inlet water (21 °C) flowrates from 5 to 60 mL(min)$^{-1}$, we achieved total thermal resistances and vapor qualities of 0.68 cm^2°CW^{-1} to 0.2 cm^2°CW^{-1} and 0.55 to 0.12, respectively. The high heat flux levels are achieved with flowrates that are 10× smaller than conventional single- or two-phase microchannel cooling technology. The corresponding two-phase thermal resistances are in the range of 0.05 to 0.02 cm^2°CW^{-1} with temperature superheat of 8 to 6 °C. While the overall performance of the large-area (10 × 10 mm^2) capillary-based micro-cooler degraded compared to previous demonstration of the technology for a heated area of 5 × 5 mm^2, preliminary computational fluid dynamics (CFD) modeling indicates that an improved manifold design will be able to achieve comparable performance.**

Keywords*— *Porous Copper Inverse Opals, Capillary flow, Two-phase boiling, Silicon 3D manifold, Data centers, Energy efficiency

NOMENCLATURE

A	Heated area, cm^2
$\bar{T}$	Average temperature across the heated area, °C
T	Temperature, °C
d	Thickness, m
k	Thermal conductivity, Wm^{-1}K^{-1}
$\overline{q''}$	Average heat flux across heated area, Wcm^{-2}
$\dot{m}$	Flow rate, mL(min)$^{-1}$
C_p	Specific heat capacity, Jkg^{-1}K^{-1}
h_{fg}	Latent heat of vaporization, Jm^{-3}
$\overline{R''}$	Mean thermal resistance, cm^2°CW^{-1}
x_e	Exit quality
	Greek symbol
α	Heat conduction loss constant, Wcm^{-2}°C^{-1}
ρ	Water density, kgm^{-3}
	Subscript
0	Inlet water temperature
2-phase	Boiling heat transfer contribution
base,CIO	Temperature at the bottom of CIO wick
cond	Conduction heat transfer contribution
drain	Properties at drain
heater	Temperature across the heater
in	Inlet
max	Maximum value
min	Minimum value
NB	Nucleate boiling prior to dry-out
overall	Thermal resistance with respect to inlet temperature of liquid
sat	Saturated condition
sens	Sensible heat transfer contribution
Si	Silicon substrate below the base of CIO
total	Total heat flux applied to heater

I. INTRODUCTION

Thermal-power challenges and increasingly expensive energy demands pose threats to the historical rate of increase in processor and power electronics performance. Energy-efficient computing and heterogeneous integration promise substantial reduction in energy demand for emerging and growing computing needs. However, these conflicting trends have resulted in a substantial increase in both heat flux and power density, which reduced the efficacy of conventional cooling technology solutions. Previous work has demonstrated air and single-phase liquid cooling for low-to-moderate heat loads [1].

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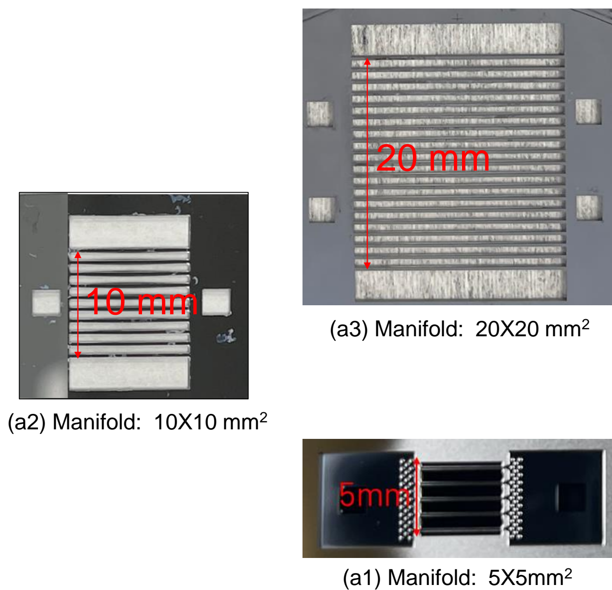

Figure 1. Silicon-based 3D manifolds with three different footprint areas: (a1) 5 × 5 mm^2, (a2) 10 × 10 mm^2, and (a3) 20 × 20 mm^2 respectively. The area scaling of the capillary-based two-phase cooling can be feasible using the microchannel manifold by efficiently supplying liquid over the large, heated area.

However, the large thermal resistance between the junction temperature and coolant requires refrigeration facility to reduce the inlet coolant temperature, resulting in an overall increase in energy consumption to operate the cooling system [2, 3]. Conventional two-phase microchannel cooling is capable of removing high heat fluxes for current- and next-generation electronics [4], but it is difficult to achieve a stable flow for large critical heat flux while maintaining low superheat and pressure drop. High thermal conductivity porous structures are great candidates to enhance the two-phase boiling process owing to numerous nucleation sites and high capillary force for efficient liquid supply within pores [5, 6], and thus are widely incorporated in flow boiling in microchannels [7], two-phase jet impingement cooling [8], and evaporative spray cooling [9]. Recent works by Zhang and Palko, et al. [5, 10] demonstrated feasibility of ultra-high-heat-flux heat removal exceeding ~ 1000 Wcm^{-2} with low superheat ~ 10 ℃ from narrow (200 to 1000 µm) bridge copper inverse opal (CIO) wick heaters. Such outstanding thermal performance is due to the capillary-fed liquid flow from both sides of the microbridge and two-phase boiling within the high thermal conductivity and permeability CIO wick, resulting in the complete liquid and vapor phase separation over the width of the bridge. The optimum width of the bridge is twice the capillary wicking length, which is the characteristic length scale where the maximum critical heat flux (CHF) occurs [10]. CHF depends on the effective liquid-vapor permeability within the wicking structure of CIO and depends on the pore and connecting neck diameters as well as the liquid-solid contact angle [10]. As noted before, for practical high-heat-flux microprocessors and power electronics applications, the outstanding performance of the narrow-bridge CIO must be scaled up to larger areas.

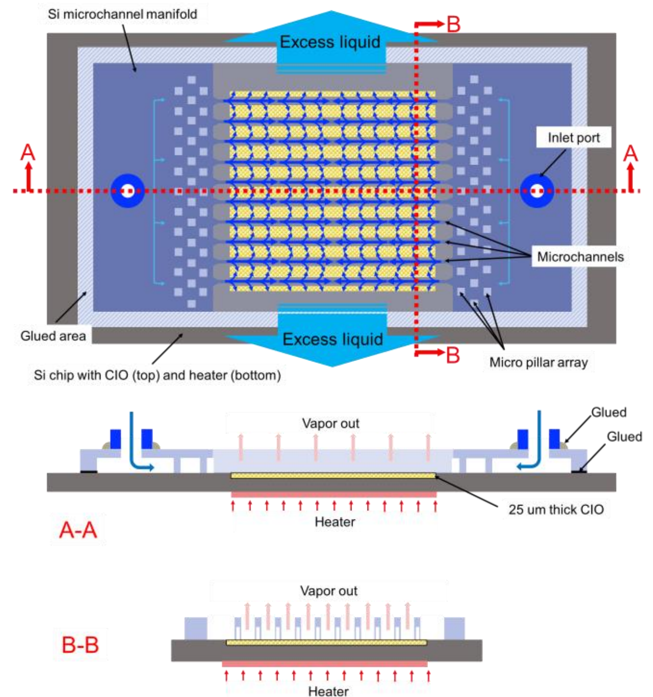

Figure 2. Illustration of the proposed capillary-assisted micro-cooler that consists of an integrated silicon microchannel manifold and a silicon chip. One side of the silicon chip is coated with CIO microstructures for improved thermal performance, while a heater is fabricated on the other side. The supplied liquid is delivered along each channel (blue color arrows) and is uniformly distributed over the CIO wick and changes phase to vapor that exits vertically (red color arrows in A-A and B-B cross-sections) while the excess liquid flows sideways and drained.

In the present work, the area scaling over 10 × 10 mm^2 microprocessor footprint is achieved by design and microfabrication of a unique silicon (open) microchannel 3D manifold for efficient liquid delivery and vapor extraction to achieve complete vapor-liquid phase separation or vapor exit quality ~ 1. The specialized 3D silicon manifold basically replicates the narrow microbridge wick structure to cover the much larger area by drawing liquid from side reservoir using capillary force in open silicon microchannels. The silicon-based 3D manifold facilitates efficient liquid distribution and vapor extraction over large chip area. The area scalability of the silicon-based micro-cooler from 5 × 5 mm^2 to 20 × 20 mm^2 footprint area can be achieved by using conventional silicon microfabrication technology (Figure 1).

The silicon 3D-manifold is simply placed over a silicon chip covered with ~ 25 µm thick CIO wick for efficient capillary-fed two-phase boiling as shown in Figure 2. A unique feature of the proposed micro-cooler is that a permanent bonding between the 3D manifold's open microchannels and CIO/silicon chip is not required. The two liquid inlet ports are bonded on Si microchannel manifold to deliver coolant via plastic tubing. The microchannels within the manifold are open at the bottom to uniformly distribute liquid over the large-area CIO wick, where the gap between the silicon microchannels and CIO are bridged

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(filled) by liquid menisci. The wide openings between adjacent 3D manifold's microchannels serve as conduits for the vapor escape or to extract the excess subcooled liquid from the wick structure. Two silicon micropillar arrays are fabricated within the 3D manifold plenums to ensure consistent flow distribution across all microchannels [11]. The complete cooler unit is realized by bonding (glued) the perimeter of the 3D manifold plenums to the cold plate, thus enclosing the wick within the microchannel array. Cross-section of the micro-cooler are described in A-A and B-B planes, as shown in Figure 2. The applied heat flux by the heater initiates the boiling within CIO wick and the vaporized water along with any subcooled liquid can exit through the gap between the microchannels. Thermal-power challenges and increasingly expensive energy demands pose threats to the historical rate of increase in processor and power electronics performance. Energy-efficient computing and heterogeneous integration promise a substantial reduction in energy demand for emerging and growing computing needs. However, these conflicting trends have resulted in a significant increase in both heat flux and power density, which reduced the efficacy of conventional cooling technology solutions.

II. MICROFABRICATION PROCESS

A. *Cold plate*

The microfabrication process of copper inverse opals wick for the large-footprint (10 × 10 mm^2) heater chip is similar to that for the heater chip with 5 × 5 mm^2 area, which is detailed in a recent publication [12]. Both halves of the fabricated cold plate are shown in Figure 3. For the wick side of the cold plate, we fabricated a ~ 25-µm-thick CIO layer (Figure 3a) with pore-to-neck diameter ratio is 0.5 as depicted in the scanning electron microscopy (SEM) images (Figure 3b). For the other side, the two mesh type heaters are fabricated that are separately powered using two independent power supplies. Furthermore, four electrical contact pads are placed for the four-probe electrical measurement to accurately estimate the power dissipation (Figure 3c). The mesh-type heater design (~ 20 Ω), as shown in Figure 3d, allows for uniform heat flux distribution over the active area compared to the serpentine configuration.

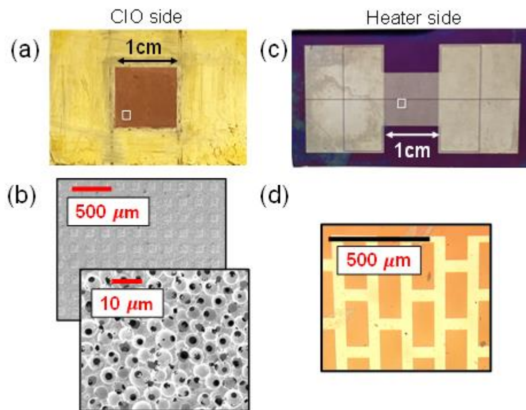
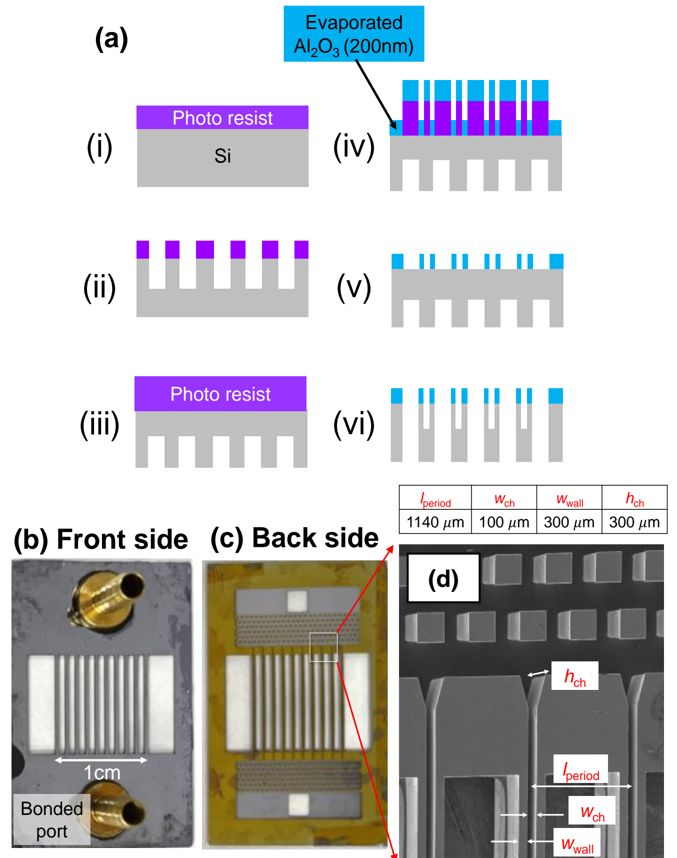


Figure 3. (a) The optical image of the front side of cold plate with CIO. (b) The SEM image of CIO. (c) The optical images of the back side of cold plate with mesh heater. (d) The optical microscopy image of the pattern of mesh heater.

B. *Silicon channel manifold*

The fabrication process for the large-area (100 mm^2) 3D silicon microchannel manifold differs from that of the 5 × 5 mm^2 micro-cooler [12], see Figure 4(a). We pattern the manifold microchannel using photolithography and etch to a depth of approximately ~300 µm using deep reactive-ion etching technique (DRIE - Step i and ii) in a ~ 650 µm thick silicon wafer, followed by removing the residual photoresists (PR) using Piranha solution. For rear side micromachining, we use an aluminum oxide film mask known for its ultra-high selectivity ratio during the DRIE process [13]. To create the aluminum oxide mask, we initially form patterns using PR and then deposit a 200-nm-thick aluminum oxide onto the patterned photoresist (Steps iii and iv). To etch the silicon on the backside, a carrier wafer is necessary to prevent cracking during the deep etching process. However, due to the etched features created in Step i and ii, thermal interfaces between the carrier wafer and the sample are introduced, along with air gaps within the features. This results in an increase in temperature of the sample during DRIE, potentially leading to damage on the photoresist mask by creating cracks, through which undesired features are formed, and therefore reducing the yield.



l_{period}	w_{ch}	w_{wall}	h_{ch}
1140 µm	100 µm	300 µm	300 µm

Figure 4. (a) Fabrication process of the 3D manifold. (b) and (c) The optical images of the front and back side of the 3D manifold. (d) The SEM image of the manifold`s backside reveals the pillar array, open liquid delivery, and vapor exit microchannels. A table representing the detailed dimensions of the silicon manifold is included.

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Subsequently, we immerse the samples in acetone to remove the alumina layer on photoresist (Step v). Finally, we conduct etching until the features etched at the frontside become accessible from the backside of the wafer (Step vi). The remaining PR is removed by soaking the sample in a Piranha solution for 20 minutes at 120 °C. The tubing inserts are bonded to the two square liquid inlets using EPO-TEK 353ND epoxy. The optical images of both sides of the fabricated manifold, and the SEM image at the backside are shown in Figure 4(b) - 4(d), depicting pillar array, open microchannel, and phase separation aperture, key dimensions of manifold channels and coolant/vapor flow paths. The 3D manifold and cold plate are joined at the periphery using an acryl-based adhesive, to create an assembly for the cooler operation. Again, we should emphasize that there is approximately 5~10-μm gap (no bonding) between the liquid microchannels and the CIO.

III. EXPERIMENT

To facilitate the thermofluidic experiment, as shown in Figure 5, a 3D printed resin polymer sample holder is fabricated to accommodate the micro-cooler chip while providing the necessary support for the chip and fluidic delivery and drainage lines, as well as providing electrical and optical access from the backside of the cold plate. The manifold and cold plate combination is carefully secured on the sample holder using silicon grease to prevent coolant leakage. The proposed capillary-fed micro-cooler does not require a pump for flow delivery in the entirely two-phase operation. However, to examine both the single- and two-phase regimes, we use a syringe pump to provide fine control (over) supply liquid into the inlet ports at either end of the 3D manifold. The cross-sectional view of the micro-cooler integrated with the sample holder, along with a detailed experimental setup, is illustrated. The electrical current along the mesh heater at the base of the cold plate is applied by the power supply and its voltage drop is measured by using a multimeter.

The electrical current is measured from the voltage drop across a 0.1 Ω shunt resistor, which is connected to the heater in series. The total power generation of the heater is deduced by multiplying the measured voltage drop across the mesh heater by the measured electrical current. By tracking the temporal fluctuation of the electrical resistance, when the electrical resistance surge occurs near the dry-out, the power supply is promptly deactivated to prevent any thermal-induced damage on the micro-cooler. A CHF is identified by the rapid increase in the electrical resistance of the heater over a 10-second duration. If the CHF is not observed, we elevate the voltage of the power supply. During each iteration, the system is closely monitored for any rapid surge in the electrical resistance that would imply the onset of CHF.

Along with the electrical measurements, the temperature map of the 10×10 mm^2 heater is recorded with an infrared (IR) camera (Teledyne FLIR, A600), which is situated below the sample. To minimize the emissivity variation, black paint is sprayed over the heater, setting the emissivity value at 0.95. We calibrate the measured temperature using the IR camera with the temperature reading from the thermocouple, which shows an error in temperature that falls within 2 °C for a range spanning from ambient temperature to 200 °C. Please note that the sensitivity of the IR measurement is better than 0.1 °C, therefore, we can monitor shifts in superheat for different flowrates. As noted, for higher flowrates, we provide an oversupply of water, part of the water changes phase from liquid to vapor. But the remaining excess water flows over the 3D manifold to the left and right, and is collected through the drain pan/holes integrated in the 3D-printed sample holder. The amount of liquid passing through the drain is accurately measured using the digital scale.

The total amount of fluid discharged over a set duration is calculated to derive the flow rate of drained water. The flow rate that undergoes boiling is determined by subtracting the flow rate measured at the drain (using an electronic scale) from the inlet flow rate.

$$\dot{m}_{2-\text{phase}} = \dot{m}_{\text{in}} - \dot{m}_{\text{drain}} \tag{1}$$

Accordingly, the heat flux associated with boiling can be calculated using the latent heat of water.

$$\bar{q}''_{2-\text{phase}} = \frac{h_{\text{fg},T_{\text{sat}}} \dot{m}_{2-\text{phase}}}{A} \tag{2}$$

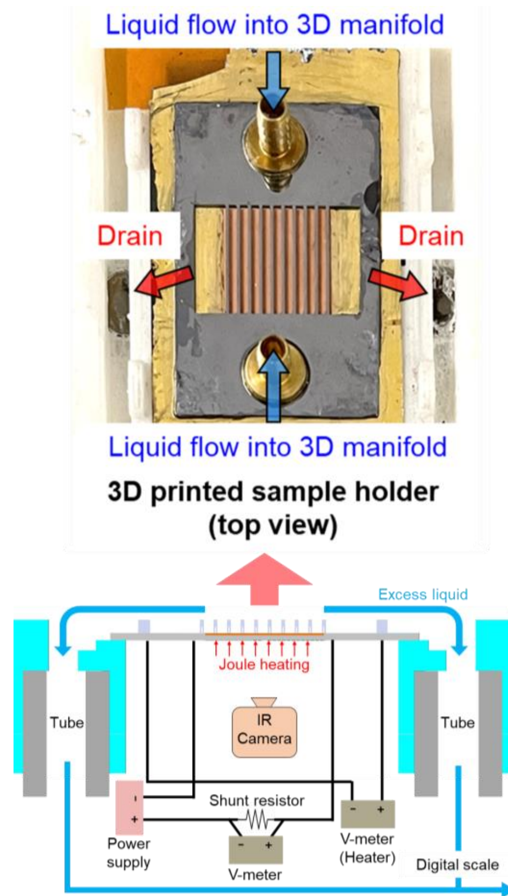

Figure 5. Illustration of micro-cooler with 3D-printed sample holder and experimental apparatus used in the experiment. Please note the pathways for liquid delivery and vapor extraction as well as excess liquid bypass to the drainage slots. The optical image of the micro-cooler on the sample holder is included.

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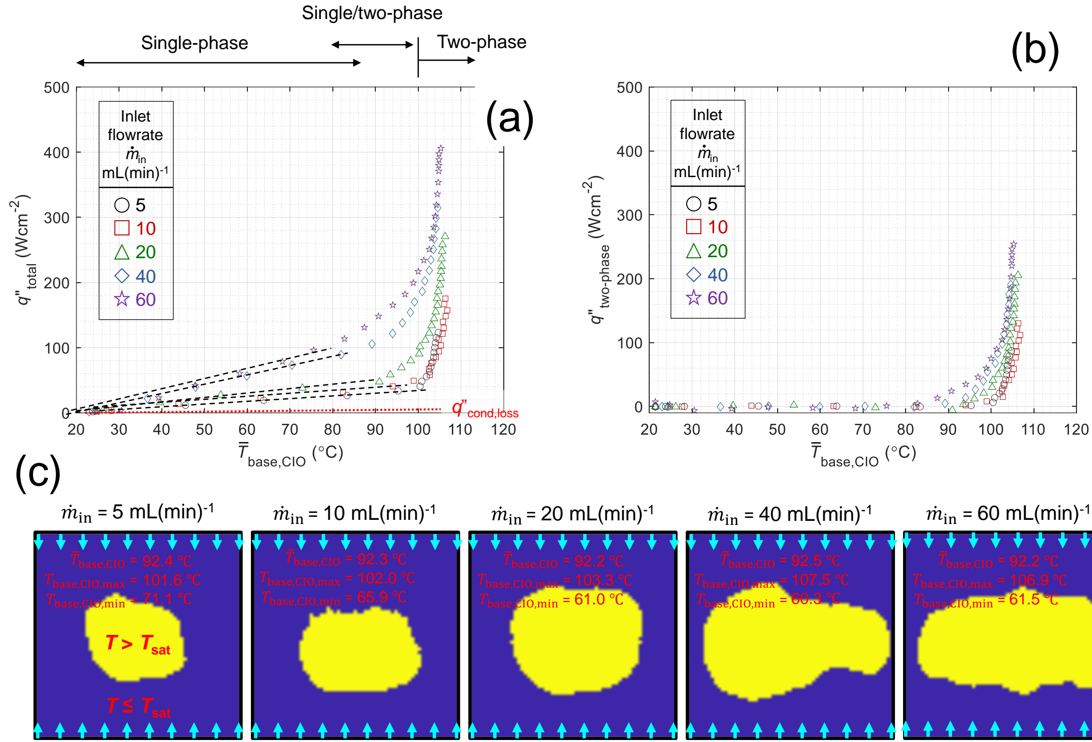

Figure 6. (a) Boiling data (represented by markers) for a micro-cooler at different inlet flow rates of 5, 10, 20, 40, and 60 mL(min)$^{-1}$. The total heat flux applied to the heater is plotted as a function of the average base temperature of CIO derived from IR image over the heater. The measured heat loss due to conduction is also plotted for reference. The dashed line for each set of data represents single-phase contribution as well as a small contribution from heat conduction loss. (b) In this plot, we subtract the contribution of single-phase, corresponding to the dashed line in Figure 6(a), from each data set for a given flow rate. (c) For $\bar{T}_{base,CIO}$ ~ 92 °C at each inlet flow rate, the region where the temperature of the CIO is larger than water saturation temperature is plotted.

TABLE I. Thermal performance near CHF for different flowrates.

$\dot{m}_{in}$ mL(min)$^{-1}$	$\dot{m}_{drain}$ mL(min)$^{-1}$	$\dot{m}_{2-phase}$ mL(min)$^{-1}$	$\bar{q}''_{total}$ Wcm^{-2}	$\bar{q}''_{2-phase}$ Wcm^{-2}	x_e	$\bar{T}_{heater}$ (°C)	$\bar{T}_{base,CIO}$ (°C)	$\bar{R}''_{2-phase}$ cm^2°CW^{-1}	$\bar{R}''_{overall}$ cm^2°CW^{-1}
5.0±0.1	2.23±0.05	2.77±0.11	123.3±0.1	104.4±16.8	0.554±0.014	115.8±2.0	104.7±2.0	0.035±0.016	0.676±0.001
10.0±0.2	6.22±0.05	3.79±0.21	175.4±0.2	142.6±31.1	0.379±0.008	119.5±2.0	106.4±2.0	0.038±0.014	0.488±0.001
20.0±0.4	14.46±0.05	5.54±0.40	270.5±0.3	208.7±60.7	0.277±0.006	123.0±2.0	106.3±2.0	0.025±0.011	0.313±0.001
40.0±0.8	34.34±0.05	5.66±0.80	314.7±0.3	213.2±120.8	0.141±0.003	126.1±2.0	104.6±2.0	0.017±0.012	0.264±0.001
60.0±1.2	52.61±0.05	7.39±1.20	405.8±0.4	278.4±181.0	0.123±0.002	119.3±2.0	105.3±2.0	0.015±0.012	0.207±0.001

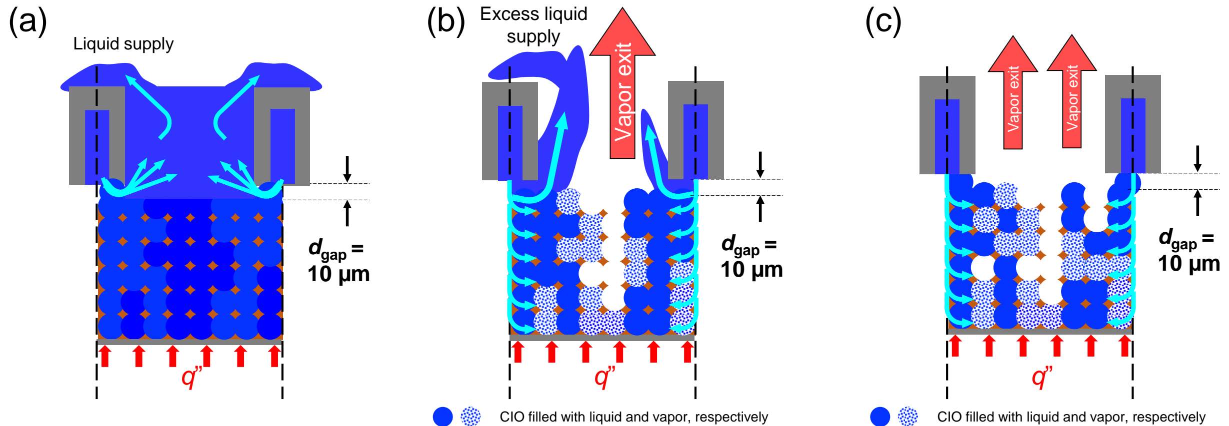

Figure 7. Illustrations for the suggested heat transfer scenarios in the micro-cooler for this study. It depicts three cases: (a) single-phase heat transfer, (b) capillary-enhanced boiling with a shallow pool, and (c) pure capillary-enhanced boiling. The regions colored in solid blue and dotted blue represent the subcooled liquid and vapor, respectively.

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IV. RESULTS AND DISCUSSION

Figure 6(a) presents the measured total heat flux $\bar{q}''_{\mathrm{total}}$ versus the average temperature of the CIO wick base $\bar{T}_{\mathrm{base,CIO}}$, at flow rates ranging from 5 to 60 mL(min)$^{-1}$. The latter is extracted from the measured average temperature of the heater according to Eq. (3).

$$\bar{T}_{\mathrm{base,CIO}} = \bar{T}_{\mathrm{heater}} - \frac{d_{\mathrm{Si}}}{k_{\mathrm{Si}}}\bar{q}''_{\mathrm{total}} \tag{3}$$

There is heat loss through the silicon substrate via heat conduction. To quantify the heat conduction loss, we measure the mean temperature increase of the heater against the applied heat flux. This measurement is conducted on a dry sample to ensure that the temperature rise is exclusively due to conduction. The applied heat flux is found to be linearly proportional to the mean temperature rise of the heater with the proportionality, α = 0.0836 Wcm^{-2}°C^{-1}.

$$\bar{q}''_{\mathrm{cond}} = \alpha(\bar{T}_{\mathrm{heater}} - T_0) \tag{4}$$

As noted before, the power supply is automatically turned off to protect the sample whenever a sudden increase in temperature occurs due to appearance of the local hot spots. Therefore, we call the maximum heat flux, where no hot spots are observed, as the maximum heat flux of nucleate boiling denoted by $\bar{q}''_{\mathrm{NB,max}}$. Increasing the heat flux by an additional 10 ~ 20 Wcm^{-2} leads to the formation of hot spots that eventually grow across the entire cooler area, resulting in dry-out. Therefore, the critical heat flux where the complete dry-out occurs, $\bar{q}''_{\mathrm{CHF}}$ is similar to $\bar{q}''_{\mathrm{NB,max}}$ within 10%.

For all the flowrates and for $\bar{T}_{\mathrm{base,CIO}}$ < 70 ~ 90 °C, there is a linear relationship between the heat flux and CIO base temperature indicating a single-phase regime, which is schematically depicted in Figure 7(a). The cold liquid is squeezed out of the gap between the manifold channels and the CIO, removing heat, and then travels upwards, filling the vapor channel where the liquid is spilled over the microchannels. Finally, the excess liquid is drained to the left and right drainage holes.

The experimental data clearly shows a non-linear relationship as the base temperature of CIO approaches the water saturation temperature ~ 100 °C. For the flowrate range of the present study, the increase in the inlet flow rate from 5 mL(min)$^{-1}$ to 60 mL(min)$^{-1}$ leads to a significant enhancement in $\bar{q}''_{\mathrm{NB,max}}$ up to 400 Wcm^{-2}. The increase in the total heat flux is due to both the contribution of the single-phase sensible and the two-phase heat transfer, as shown in the schematic in Figure 7(b). However, at the higher flow rates, despite the abundance of liquid supply (leading to overflow), no notable increase in superheat is displayed. This observation differs from the results seen in previous studies on pool boiling of CIO layer [14], where the superheat increases monotonically as the input heat flux increases. We postulate a shallow liquid pool, as opposed to a thicker pool, does not significantly affect the superheat. Furthermore, the lateral flow leaking from the gap between the CIO and microchannel sweeps away bubbles emerging from the wick structure facilitating efficient bubble removal, contrasting with the growth of large bubbles comparable in size to the heating element in pool boiling conditions.

To obtain further insight into the contribution of the single- and two-phase heat transfer, it is necessary to quantify the single-phase heat transfer contribution. The heat flux due to sensible heat can be calculated as follows.

$$\bar{q}''_{\mathrm{sens}} = \frac{\dot{m}_{\mathrm{drain}}\rho C_p(T_{\mathrm{drain}}-T_0)}{A} + \frac{\dot{m}_{2-\mathrm{phase}}\rho C_p(T_{\mathrm{sat}}-T_0)}{A} \tag{5}$$

Therefore, to estimate the sensible heat transfer in our system, it is essential to determine the temperature at the drain. However, the cooler is operated at a relatively low inlet flow rate, below 100 mL(min)$^{-1}$, and the excess liquid exiting the manifold is not consistently guided to the outlet, resulting in a highly intermittent flow at the drain. Therefore, a reliable measurement of the exit temperature is not viable.

As shown in Figure 6(b), we subtract the estimated total heat loss due to single-phase liquid flow and conduction, which are represented by the interpolated black dashed lines in Figure 6(a) at each flow rate. It shows that the two-phase components of heat flux increase above the water saturation temperature for the higher flow rates, implying that the data in Figure 6(a) is simply a superposition of single-phase and two-phase heat transfer components for the total heat flux. However, at flow rates exceeding 20 mL(min)$^{-1}$, a non-zero two-phase component of heat flux is observed with the average CIO base temperature remaining below the saturation temperature. We attribute this to the onset of the boiling, occurring when the average temperature of the wick base falls below the water saturation temperature. To confirm this, using the IR imaging results, we plot the region where the local temperature exceeds the water saturation temperature at an average wick base temperature of approximately 92 °C, as shown in Figure 6(c). It is evident that the area where the temperature surpasses the water saturation temperature increases, indicating an expanded region of boiling as the flow rate is increased. This is due to temperature non-uniformity from the inlet to the center.

TABLE I provides additional information on the contribution of the single-phase and two-phase heat transfer rates as well as the vapor exit quality for any given flow rate just below the CHF point. The higher flow rate results in the increase in the CHF, because more liquid flows into the center along the microchannels, preventing the dry-out of the cooler. Consequently, this reduces the thermal resistance of two-phase heat transfer due to the increased heat flux with the similar superheat. The mean thermal resistance over the heated area for the phase change is given by the following equation.

$$\bar{R}''_{2-\mathrm{phase}} = \frac{\bar{T}_{\mathrm{base,CIO}} - T_{\mathrm{sat}}}{\bar{q}''_{2-\mathrm{phase}}} \tag{6}$$

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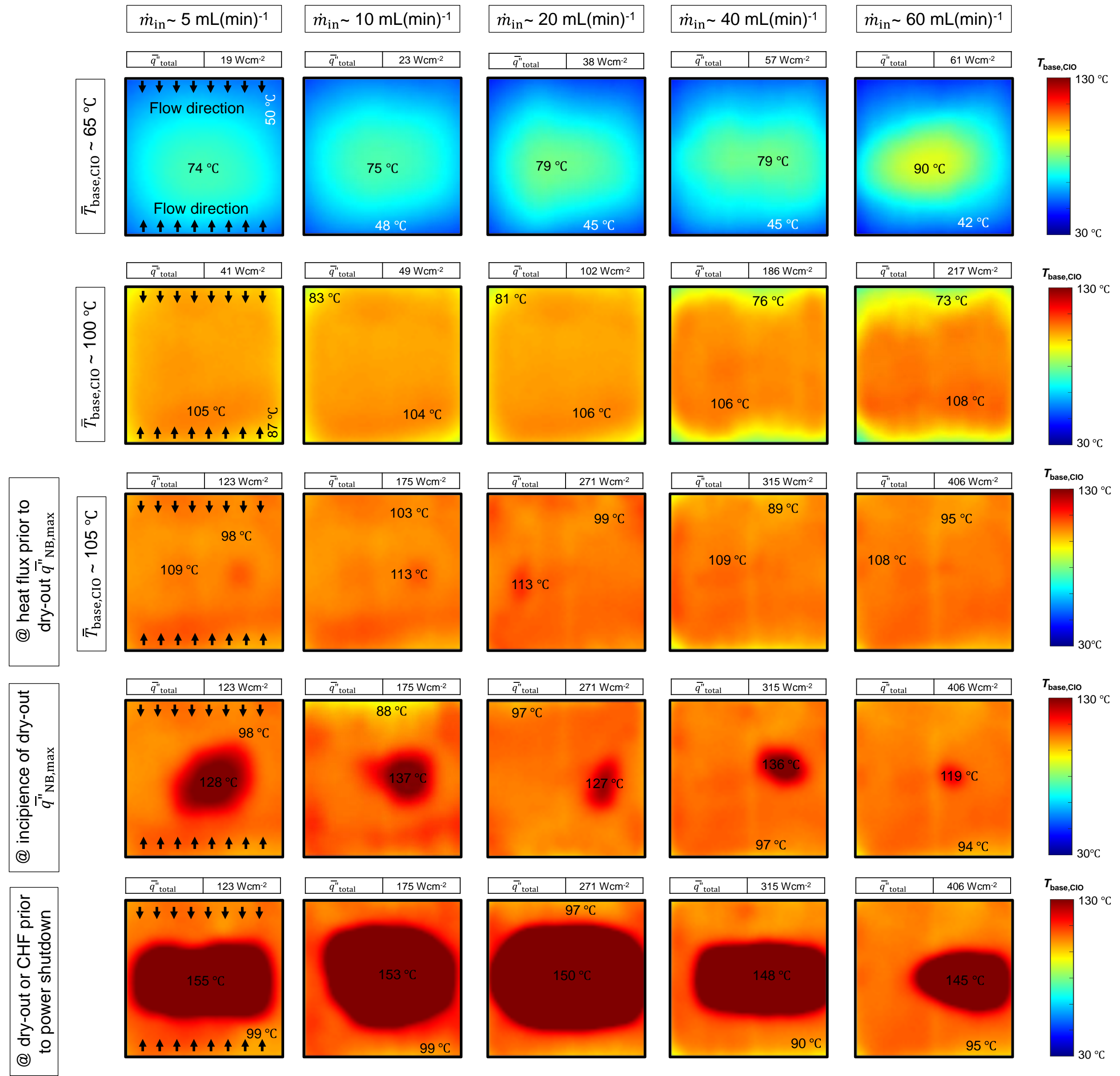

Figure 8?6. 2D temperature profiles of the base (CIO side) that are derived from the measured IR images of the heater. For each flow rate, the heat flux value is chosen at $\overline{T}_{base,CIO}$ ~ 65 °C and $\overline{T}_{base,CIO}$ ~ 100 °C, at the maximum heat flux just before dry-out, at the heat flux where local hot spots begin to form, and the nearly complete dry-out occurs. These correspond to the rows from the first to the fifth, respectively.

The cooling mechanism in the proposed cooler system is a combination of capillary action within CIO and forced flow from the microchannel array of the manifold, rather than relying solely on capillary-fed boiling, for which all the supplied coolant is consumed for the boiling process [5, 15, 16]. Therefore, for the cooler in this study, not all the supplied coolant undergoes boiling and some of it remains in the liquid phase. Accordingly, the exit quality is calculated using the following equation, which is the same definition adopted in the typical flow-assisted two-phase cooler with the closed-loop pump system [17].

$$x_e = \frac{A\overline{q''}_{2-\mathrm{phase}}}{h_{\mathrm{fg},T_{\mathrm{sat}}}\dot{m}_{\mathrm{in}}} \qquad (7)$$

The vapor exit quality drops sharply for the larger flow rates, even though the two-phase component of heat flux is increased. This is because, for the higher flow rate, more liquid leaks through the small gap between the bottom of channel and the top surface of CIO without being vaporized within CIO layer, see Figure 7(b). Furthermore, the increase in the flowrate enhances the single-phase advective cooling contribution of the total heat flux. Owing to the increase in both contributions single- and two-phase heat transfer with the similar superheat value at the higher flow rate, the overall thermal resistance of the micro-cooler is dramatically reduced to 0.18 cm^2°CW^{-1} at 60 mL(min)$^{-1}$.

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To evaluate the overall thermal performance, we define the thermal resistance of the micro-cooler with respect to the inlet liquid temperature.

$$\bar{R}''_{\text{overall}} = \frac{\bar{T}_{\text{heater}} - T_0}{\bar{q}''_{\text{total}}} \quad (8)$$

In our previous study of 5×5 mm^2 micro-coolers [12], for very small flowrates, we noted a completely two-phase capillary boiling regime, where the vapor quality, $x_e \sim 1$, with no excess flow drainage as depicted in the schematic shown in the Figure 7(c). Indeed, the optimal performance for the micro-cooler is achieved at the flowrate corresponding to $x_e \sim 1$ at the expense of lower critical heat flux. For the large-area (10×10 mm^2) micro-cooler, the maximum vapor quality of $x_e \sim 0.55$ was achieved, which is much larger than a typical two-phase microchannel cooling but falls short of the vapor quality ~ 1 that was achieved in our previous study [14].

It is worthwhile to investigate the IR images over the base of the CIO wick, as depicted in Figure 8. For the flow rates used in the experiment, we presented 2D temperature profiles at the average base temperature of CIO ~ 65 and 100 °C, at $\bar{q}''_{\text{NB,max}}$, at the incipience of dry-out, and at the significant dry-out prior to the power supply shutdown, which correspond to the rows from the first to the fifth one. The base temperature profiles are derived from the IR data over the 10×10 mm^2 heater area by subtracting the temperature drop across the silicon substrate at each pixel. At the average base temperature ~ 65 °C where the single-phase heat transfer prevails, the temperature profile is not uniform. This implies the colder regions at the top and bottom of the image correspond to availability of excess cold inlet liquid near the inlet plenums. At the average base temperature ~ 100 °C, where the boiling is expected to begin, the temperature profiles become more uniform compared to when the single-phase heat transfer is dominant. It is noted that at the high flowrate ~ 40 mL(min)$^{-1}$ and 60 mL(min)$^{-1}$, respectively, the temperature profiles near the inlets of the microchannels show lower temperature values than the area near the center due to the significant advective heat transfer near the inlet.

At the $\bar{q}''_{\text{NB,max}}$ (just below the CHF level) as the inlet flow rate is increased from 5 to 60 mL(min)$^{-1}$, no significant increase in the temperature is observed, despite the approximately three-fold increase in the total heat flux. This suggests that capillary-fed boiling over the entire area of the wick exists compared to the single-phase heat transfer by the liquid flow. The temperature profiles in the fourth and fifth rows show the representative snapshots of the local hot-spots (dark red color), followed by the dry-out condition. These small hot spots (the fourth row in the image set) propagate rapidly across the heated area (the fifth row in the image set) before the power supply is automatically turned off. The formation of the hotspots could be due to the presence of large volume of vapor within the CIO that prevents the capillary-fed action and disruption of the liquid supplies within the CIO wick [18].

Furthermore, it is worthwhile to note that for all the flowrates in the experiments, the local dry-out propagates from the center of the cooler. This is attributed to the significant coolant starvation at the center as the liquid leaks out of the gap between the microchannel and CIO surface as the coolant propagates along the microchannel from the inlet to the center over the heated area.

V. Conclusions

Previously, two-phase capillary-based cooling from narrow (200 to 1000 μm) heater bridge copper inverse opal (CIO) wick swith heat flux levels exceeding 1400 Wcm^{-2} with low superheat of ~ 10 °C was demonstrated. Here, we demonstrated the area scaling of the proposed technology to large-area micro-cooler for the high-heat-flux cooling of microprocessors and power electronics. We developed a hybrid single/two-phase micro-cooler that relies on capillary-wicking in a 25-μm-thick CIOs with an open-channel silicon 3D-manifold for liquid delivery and vapor extraction, to achieve a high heat flux of ~ 400 Wcm^{-2} over a heated area of 1 cm^2. For the range of inlet water (21 °C) flowrates from 5 to 60 mL(min)$^{-1}$, we achieved total thermal resistances and vapor qualities of 0.68 cm^2°CW^{-1} to 0.2 cm^2°CW^{-1} and 0.55 to 0.12, respectively. The high heat flux levels are achieved with flowrate that are 10× smaller than conventional single- or two-phase microchannel cooling technology. The corresponding two-phase thermal resistances are in the range of 0.05 to 0.02 cm^2°CW^{-1} with temperature superheat 8 to 6 °C. While the overall performance of the large-area (10×10 mm^2) capillary-based micro-cooler slightly degraded compared to previous demonstrations of the technology over a heated area of 5×5 mm^2, preliminary CFD modeling indicates that an improved 3D manifold design will be able to achieve comparable performance.

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