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Investigation of Static Performances of 1.2kV 4H-SiC MOSFETs Fabricated Using All 'Room Temperature' Ion Implantations

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ABSTRACT Several different designs of 1.2kV-rated 4H-SiC MOSFETs have been successfully fabricated under various ion implantation conditions. Implantation conditions consisted of different P+ profiles and implantation temperatures of both room temperature (25°C) and elevated temperatures (600°C) in order to monitor subsequent lattice damage. Through the use of X-Ray topography, SEM imaging, and electrical measurements, it was shown that room temperature implanted devices can mimic the static performances of high temperature implanted MOSFETs and reduce lattice damage suffered during the fabrication process, when the dose of high energy implants are suppressed.

INDEX TERMS 4H-Silicon Carbide (SiC), MOSFET, 3rd quadrant, design approach, leakage current, breakdown voltage, room temperature implantation, X-Ray topography, SEM-analysis.

I. INTRODUCTION

For high voltage power devices, 4H-SiC offers superior benefits over Silicon due to the material's wide bandgap while simultaneously having comparable electron mobility. The wide bandgap combined with a large critical electric field in 4H-SiC allows the creation of a thin and heavily doped epitaxial drift layer. This results in a device with lower resistance when compared to traditional Silicon power devices at voltage ratings greater than or equal to 600V [1]. Although the material properties of 4H-SiC make it a preferred candidate for high voltage power applications, the material itself presents unique challenges for device processing that is not experienced in traditional Silicon devices. In Silicon device fabrication, the ion implantation process can be performed at room temperature (RT), which allows for a photoresist layer to be used as an implant blocking mask [2]. However, in 4H-SiC processing technology, ion implantation has been performed at elevated temperatures to reduce lattice damage in-situ and prevent Basal Plane Dislocations (BPDs) from forming; the creation of which leads to device degradation under high bipolar current stress [3]. These elevated temperatures (~600°C) used during the implantation process requires the use of an oxide blocking mask as the photoresist layer would not survive the high temperature (HT) process. Therefore, the use of elevated temperatures for ion implantation steps would result in an overall process that is more complex, longer, and costly [4].

Due to the drawbacks of all HT ion implantation processes, there have been studies to integrate full scale room temperature implantations of ions without generating a significant quantity of BPDs. Previously, a critical aluminum dose of $1\times10^{15}\text{cm}^{-2}$ was reported to prevent significant BPD generation while using room temperature ion implantation [5]. Further development from our research group has shown that proper control over the implantation energy and dose

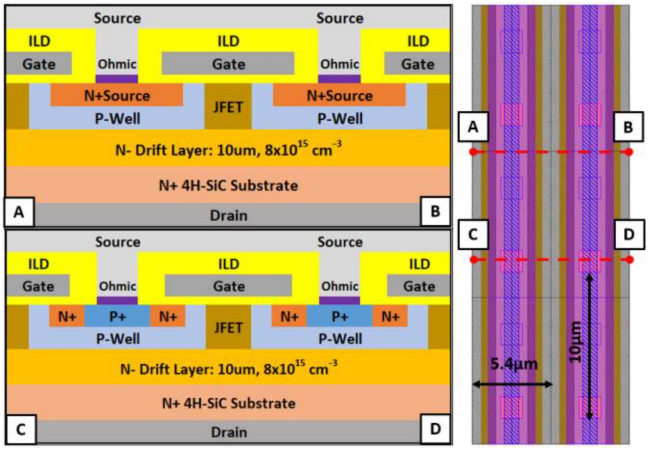

FIGURE 1. Active area cross section and top views of fabricated 1.2kV MOSFETs. P+ source contacts were placed intermittently in the orthogonal direction as indicated by the two cross sectional views rather than a conventional stripe pattern source region. Key regions of the MOSFET cell structure are labeled in each cross section.

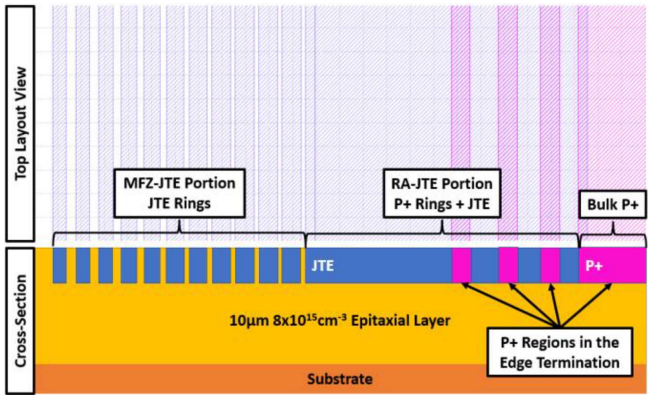

FIGURE 2. Top layout and cross-sectional view of the Hybrid JTE edge termination used to ensure near ideal breakdown voltage and minimal leakage current during the forward blocking operation. P+ implantation regions and P- JTE regions within the hybrid JTE edge termination structure are indicated.

altogether allows devices with an implant dose nearly 10× greater than the previous critical dose, while simultaneously suppressing BPD generation and thus improving device performance and longevity [6]. Although this work can be viewed in simple device structures such as diodes, this method and its effects can be extended to more complex structures such as vertical MOSFETs and their subsequent electrical properties under this process. In this study, the feasibility of all RT implantations for 4H-SiC fabrication was investigated through both physical analysis of the substrate, and MOSFET electrical performance.

II. DEVICE AND EDGE TERMINATION DESIGN

A. ACTIVE AREA DESIGN

Fig. 1 shows a simplified top layout and cross-sectional views of the MOSFET active area cell utilized within this study. For this cell layout, the P+ source contacts were isolated and placed periodically within the orthogonal direction, as opposed to a conventional stripe type P+ contact.

The MOSFET dimensions used in this study were determined through 2-D forward conduction and blocking electrical simulations. For this the optimal dimensions for the JFET width and channel length that resulted in low Specific on resistance ($R_{on,sp}$) leakage current, and high breakdown voltage were determined to be 1.2μm and 0.5μm, respectively. The resulting cell pitch after device optimization was determined to be 5.4μm. Within the JFET region of the device, ion implantation was used to enhance the low background doping of 8×10^{15}cm^{-3} to 5×10^{16}cm^{-3}.

B. EDGE TERMINATION DESIGN

In order to accommodate the 1.2kV blocking voltage rating of the devices, an n-epitaxial drift layer was designed with a thickness of 10μm and a background nitrogen doping concentration of 8×10^{15}cm^{-3}. By doing such a parallel plane blocking voltage of ~1600V was able to be reached while simultaneously minimizing the $R_{on,sp}$ of the MOSFET devices. However, to ensure this near ideal breakdown voltage, the MOSFETs were fabricated with a "hybrid edge termination" structure [8]. This hybrid edge termination structure combines a Ring Assisted Junction Termination Extension (RA-JTE) and a Multiple Floating Zone Junction Termination Extension (MFZ-JTE) into one edge termination structure as observed in Fig. 2. This approach provides a wide range of JTE dose easing device fabrication while simultaneously ensuring high breakdown voltages [7].

The RA-JTE portion can be optimized to consist of spacing between the first P+ ring and the main junction (S_o), followed by incremental spacings between rings (S_i), number of rings (n), and ring width (W), all within the JTE region with a width (W_{jte}). Final dimensions can be described by the equation $S_n=S_o+S_i(n-1)$ where S_n is the spacing between each P+ ring with respect to the ring number. RA-JTE optimized parameters, for S_o, S_i, n, W and W_{jte} are 4, 1, 3, 4, and 60μm, respectively. The MFZ-JTE portion of the edge termination has gradually decreasing JTE region widths, which can be described with the equation $W_n=W_1/\alpha^{(n-1)}$ where n corresponds to the ring number, W_n denotes the n_{th} region width and α denotes a decreasing parameter. MFZ-JTE optimized parameters, for n, W1 and α are 11, 5 μm and 1.05 respectively.

III. DEVICE FABRICATION

Several 10A rated MOSFETs with a blocking voltage rating of 1.2kV were successfully fabricated for this study. To begin the process flow, a heavily doped N+ buffer layer followed by a 10μm thick, 8×10^{15}cm^{-3} n-doped epitaxial layer was grown on 4H-SiC substrates. Ion implantation was applied to form the various dopant regions within the MOSFET structure. For these regions, Aluminum and Nitrogen were used in the formation of the P+/P-well/JTE and JFET/N+ regions, respectively. For the p-well formation,

TABLE 1. Dose and Ion species used in each of the five implantation steps used in the fabrication of each MOSFET split condition.

Implant Step	Ion Species	Net Dose [cm^{-2}]
JFET	Nitrogen	$4.1x10^{12}$
PWell	Aluminum	$5x10^{13}$
N+	Nitrogen	$9x10^{14}$
P+	Aluminum	$1.05x10^{15}$
JTE	Aluminum	$1.8x10^{13}$

an aluminum profile was designed to create an accumulation mode channel. By doing such, a channel with higher mobility was able to be created and thus the overall, $R_{on,sp}$ of the device can be lowered [8]. The implantation steps were performed at both a room temperature of 25°C and at elevated temperatures of 600°C to mitigate the formation of ion implantation induced damage, based on the device split mentioned previously. All implants regardless of implantation temperatures utilized an oxide blocking mask to minimize processing differences. After the ion implantation steps, a carbon capping layer was deposited to reduce lattice damage originating from carbon vacancies, and an activation anneal was performed [9]. For this activation anneal process a temperature of 1650 °C was applied for 10 minutes.

Following the ion implantation and activation anneal processes, a 50nm thick gate oxide layer was created using thermal oxidation. This was followed by the deposition of polysilicon and then both the oxide and polysilicon layers were patterned to create the MOSFET gate. After the gate formation, an interlayer dielectric was uniformly deposited, and then opened to allow the formation of an ohmic contact within the source region and gate contact in the device periphery. Nickel was then deposited, and a silicide was pre-annealed at 750°C for 2 minutes using a rapid thermal anneal (RTA) process to partially form the frontside ohmic contacts and gate contacts. The remaining nickel that did not undergo the silicidation process was then removed. On the backside of the wafer nickel was deposited and then all nickel metal (on the frontside and backside of the wafer) was annealed at 1000°C for 2 minutes. This annealing process forms both the front and backside ohmic contacts of the MOSFET devices. Following the ohmic formation, a thin layer of titanium nitride followed by a 4μm thick aluminum top metal layer was deposited and patterned to form the final source and gate contacts. To finish the process flow, a nitride and thick polyimide layer were deposited and patterned to passivate the frontside of the wafer.

IV. ALL HIGH TEMPERATURE VS ALL ROOM TEMPERATURE ION IMPLANTATION RESULTS

A. IMPLANTATION CONDITIONS

Table 1 shows the net dose and ion species for each implantation step. Each implantation step was performed at either HT (600 °C) or RT (25 °C) depending on the wafer split condition. To mitigate any potential BPD generation of either all HT or RT implantations, the net dose for each implant was limited to the previous critical dose of approximately $1\times10^{15}cm^{-2}$.

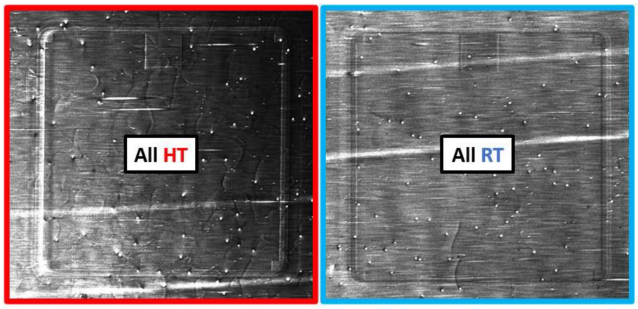

FIGURE 3. X-Ray topography images of the MOSFETs fabricated using all HT (left) or RT (right) implantation. No BPDs or other forms of lattice damage can be observed within both fabricated structures.

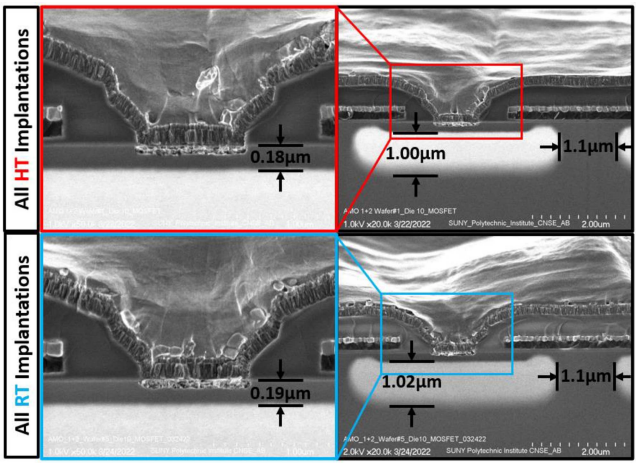

FIGURE 4. Cross sectional SEM images of the N+ source regions within the MOSFETs fabricated using either all RT or HT implantations. No major differences between the two fabricated structures can be observed.

B. PHYSICAL ANALYSIS OF FABRICATED DEVICES

Fig. 3 shows the grazing incidence monochromatic X-Ray topography images of the BPDs generated by both a HT and RT fabricated MOSFET. The X-Ray topography images were performed of the 4H-SiC wafers and recorded on high resolution X-ray films at 1-BM, Advanced Photon Source at Argonne National Laboratory. Prior to the X-Ray analysis the areas above the wafer surface (Top metal, gate poly, oxide, etc.) were striped utilizing a BOE etchant. From these X-Ray topography images, no BPD generation can be observed within both HT and RT fabricated devices.

To ensure the accuracy of the implantations and their effect on device region formations, cross-sectional SEM images were performed after device fabrication as seen in Fig. 4. From these cross-sectional SEM images, no major differences can be observed between the two fabricated structures as indicated by the height, depth, and straggle of the P-Well region in both all HT and RT implanted devices. The absence of any process-induced damage observed within

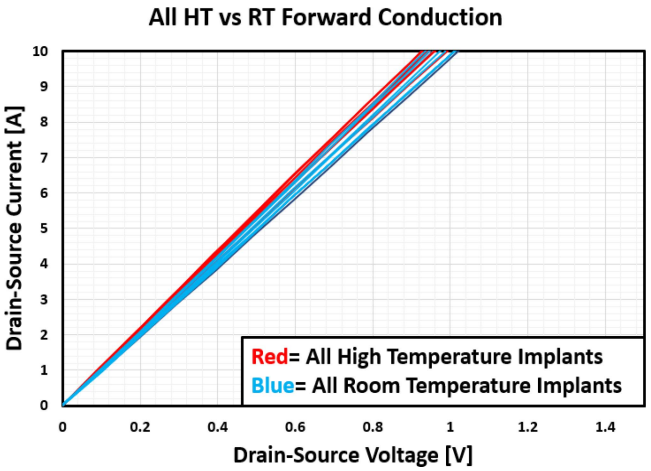

FIGURE 5. Several forward conduction output curves for MOSFETs fabricated using either all room temperature (blue) or high temperature (red) implantations at a gate bias of V_{gs}=20V. All forward conduction measurements were performed on wafer and at 25°C.

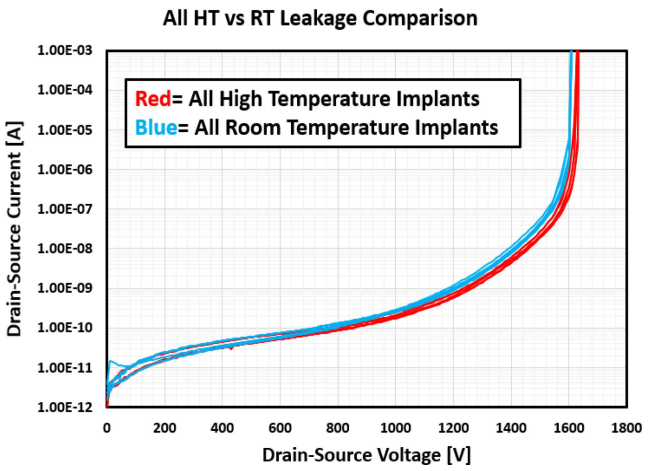

FIGURE 6. Several forward blocking and leakage curves for MOSFETs fabricated utilizing either all room temperature (blue) or high temperature (red) implantations. All leakage curves were performed at V_{gs}=−5V to minimize any potential leakage through the channel.

both structures demonstrates the potential for integration of all RT ion implantation when the net dose for each processing step is lower than the previous critical dose of 1×10^{15}cm^{-2}.

C. STATIC ELECTRICAL CHARACTERISTICS

Although no physical damage could be observed within the HT and RT implanted structures, device electrical performance needs to be evaluated prior to adoption of all room temperature implantation. Fig. 5 shows the typical forward conduction characteristics for the devices fabricated utilizing either all high temperature or all room temperature ion implantation. Average $R_{on,sp}$ between the two fabrication conditions were found to be 4.16mΩcm^2 and 4.37mΩcm^2 with a standard deviation of 0.24mΩcm^2 and 0.17mΩcm^2 for all HT and RT implanted devices, respectively. The RT implanted devices showed slightly higher $R_{on,sp}$ but this small difference is believed to be wafer process variation. The N+ ohmic contact resistances for all HT and all RT implanted devices were found to be 3.27×10^{-4}Ωcm^2 and 3.36×10^{-4}Ωcm^2 respectively, further showing the minimal differences in forward conduction behaviors. Forward blocking and leakage comparison between all RT and HT implanted MOSFETs can be observed in Fig. 6. For these two implanted structures, negligible differences can be observed with both structures maintaining ∼1600V breakdown voltage and a leakage current of ∼0.5nA-0.9nA at a blocking condition of 1200V across several devices. Forward breakdown voltages were determined once the device had reached a drain-source current (I_{ds}) reading of 1 mA. From these forward conduction and blocking results, it can be determined that performing all low dose ion implantations at RT has minimal impact on device performance when compared to HT implanted devices.

The typical 3rd Quadrant output between the HT and RT fabricated devices can be observed in Fig. 7. Minimal differences can be observed when a gate bias was not applied (V_{gs}=0V). However, once the conduction through the channel is limited by applying a gate bias of V_{gs}=−5V, minor differences in 3rd quadrant conduction between the structures can be seen. Average source-drain voltage (V_{sd}) at 10A was found to be 6.80V and 7.03V for both HT and RT implanted devices. This originates from the P+ contact resistance difference of, 0.51Ωcm^2 and 1.78 Ωcm^2 between the HT and RT MOSFETs respectively.

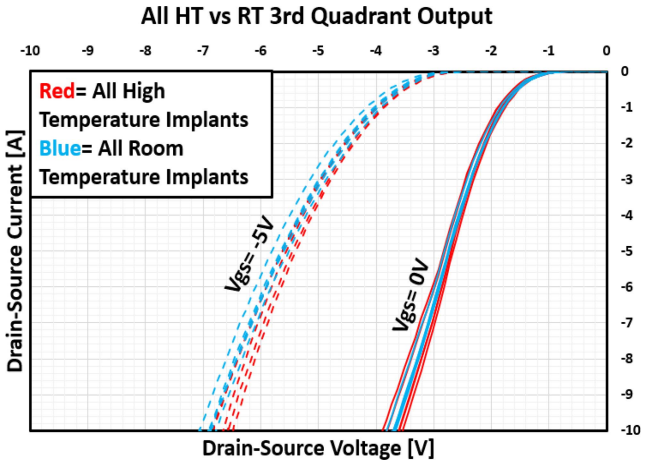

FIGURE 7. Several 3rd Quadrant output curves for MOSFETs fabricated using either all room temperature (blue) or high temperature (red) implantations. The solid and dashed curves are measured at a gate bias of V_{gs}=0V and V_{gs}=−5V respectively.

Unlike the N+ ohmic contacts, the P+ contacts of both HT and RT devices fail to achieve an acceptable contact resistance determined by the non-linear output of P+ measurements as observed in Fig. 8. Thus the net dose for the P+ implant would have to be increased beyond previous 1×10^{15}cm^{-2} critical dose to improve the electrical performances of the devices [6].

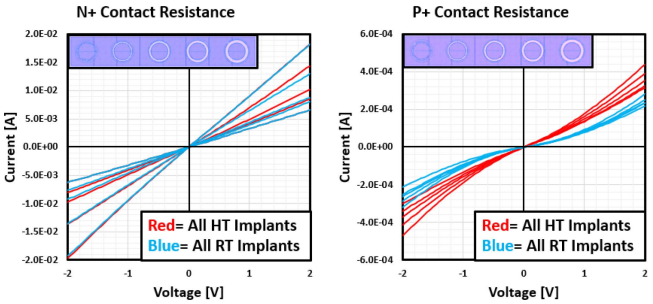

FIGURE 8. Contact resistances extracted for both the N+ and P+ contacts used within this study. N+ contacts formed in this study resulted in linear output curves and therefore resistance can accurately be extracted, however the P+ contacts formed failed to achieve an acceptable linear output.

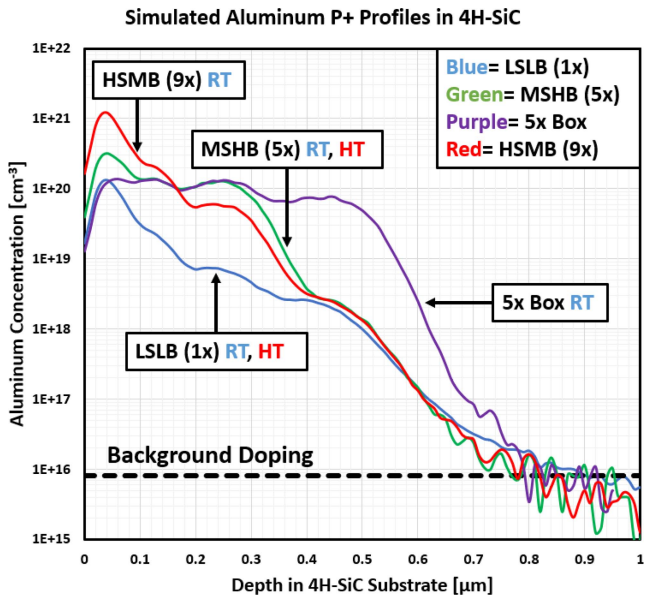

FIGURE 9. Simulated aluminum concentration profiles used in the various P+ source regions and edge termination rings used within this study. It is important to note the creation of this '5x RT Box' profile uses greater doses at its higher energy implants when compared to the other '5x' profiles.

Overall, the differences between all HT and RT implantations and their effects on the static device electrical performance were found to be minimal.

V. PROFILE OPTIMIZATION OF THE P+ IMPLANTATION WITH INCREASED DOSE FOR ALL RT ION IMPLANTED DEVICES

A. P+ IMPLANT PROFILE DESIGNS

The 1×10^{15}cm^{-2} P+ resulted in poor contact resistances and thus device performance was hindered. To further enhance the device output characteristics the P+ implantation dose would have to be increased. However, this elevated dose goes beyond the previous critical dose and thus the profile should be considered to mitigate any potential BPD generation. Fig. 9 shows the four different P+ implantation profiles used in this study, where the profiles are varied with high (H), medium (M), and low (L) in concentration for the surface (S) and body (B) of the junction. The 'LSLB (meaning Low Surface Low Body in doping)' (simply '1x'), 'MSHB' ('5x'), and 'HSMB' ('9x') has a total Al dose of 1×10^{15} cm^{-2}, 5×10^{15} cm^{-2}, and 9×10^{15} cm^{-2}, respectively, while the '5x RT Box' profile has a near uniform surface and body concentration with a total dose of 5×10^{15} cm^{-2}. Table 2 shows the temperatures used for each implantation step during the MOSFET fabrication process. Most implants were performed at RT of 25°C however several implantation splits were conducted at elevated temperatures of 600°C (HT), to compare BPD generation between the various implantation conditions. As a reference, one 'LSLB 1x' split utilizes HT implantation of 600°C for all five implementation steps, and one 'MSHB 5x' split uses elevated temperature solely for the P+ implantation and the remaining implant steps are performed at RT. The remaining implantation conditions were all performed at RT for all five implementation steps.

TABLE 2. Temperatures of each of the five implantation steps used in the fabrication of each MOSFET split condition. Implants performed at elevated temperatures of 600°C and at room temperature of 25°C are denoted by HT and RT respectively.

	1x Low Surface Low Body (LSLB)		5x Medium Surface High Body (MSHB)		5x Box	9x High Surface Medium Body (HSMB)
Implant Step	'1x HT'	'1x RT'	'5x HT'	'5x RT'	'5x RT Box'	'9x RT'
JFET	HT	RT	RT	RT	RT	RT
P-Well	HT	RT	RT	RT	RT	RT
N+	HT	RT	RT	RT	RT	RT
P+	HT	RT	HT	RT	RT	RT
JTE	HT	RT	RT	RT	RT	RT

B. PHYSICAL ANALYSIS OF FABRICATED DEVICES

Fig. 10 shows the zoomed in grazing incidence monochromatic X-Ray topography images of the BPDs generated from each P+ implantation condition. From these images, both 'LSLB 1x'conditions, and the 'MSHB 5x HT' MOSFETs show negligible BPD generation throughout the entirety of the device area. However, BPD generation can be observed starting in the 'HSMB 9x RT' devices and increasing in defect density in the 'MSHB 5x RT' and '5x RT Box' MOSFETs. This BPD generation can be observed around the edge termination and periphery regions of these devices in which the P+ implantation was used. Therefore, this BPD generation is process related as opposed to being native to the 4H-SiC wafer. This is due to the P- JTE regions being subjected to compressive stresses following the ion implantation and activation anneal process [10], [11]. BPD density within the edge termination and periphery region for the 'HSMB 9x RT', 'MSHB 5x RT' and '5x RT Box' were found to be 2.1×10^{3}cm^{-2}, 3.4×10^{3}cm^{-2} and 2.5×10^{4}cm^{-2} respectively.

Although the X-Ray topography images do not show significant BPD generation within the MOSFET active area of each device, after closer examination lattice damage can be observed through X-SEM analysis. Fig. 11 shows the cross-sectional SEM images of the P+ source regions

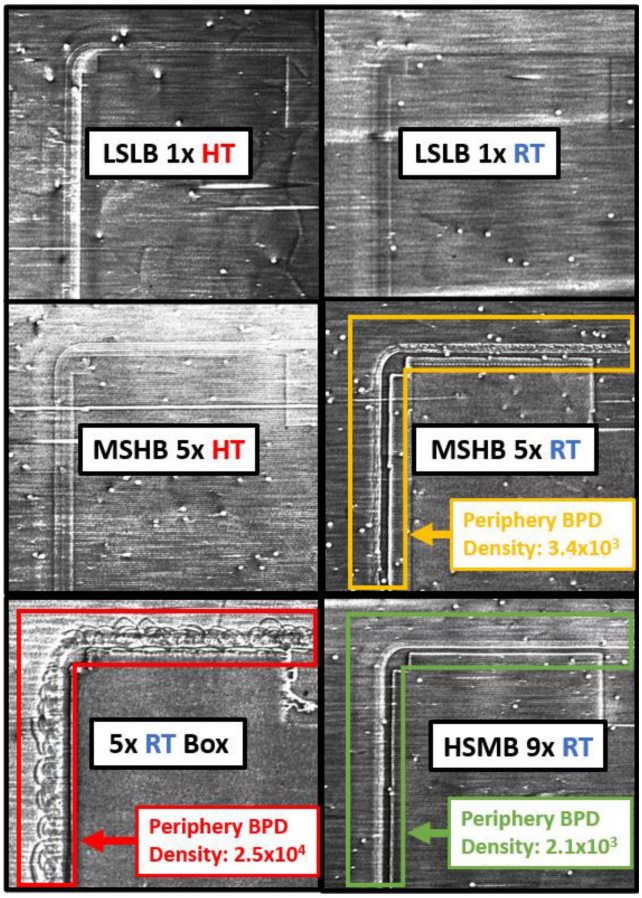

FIGURE 10. X-Ray topography images of the MOSFETs fabricated with various P+ implantation profiles. 'LSLB 1x HT', 'LSLB 1x RT', 'MSHB 5x HT', and 'HSMB 9x RT' all show low levels of damage throughout the active area as well as near the edge termination, however the '5x RT Box' shows a very high density of BPDs near the periphery and edge termination of the device which originated from the high energy and dose implantations to form the P+ regions in those areas. This can also be seen in the 'MSHB 5x RT' condition however to a lesser extent. Both areas of high damage in the '5x RT Box' and 'MSHB 5x RT' condition are highlighted along with their BPD densities. BPD densities were calculated based on the BPD nucleation from device edges and assuming the entire device volume.

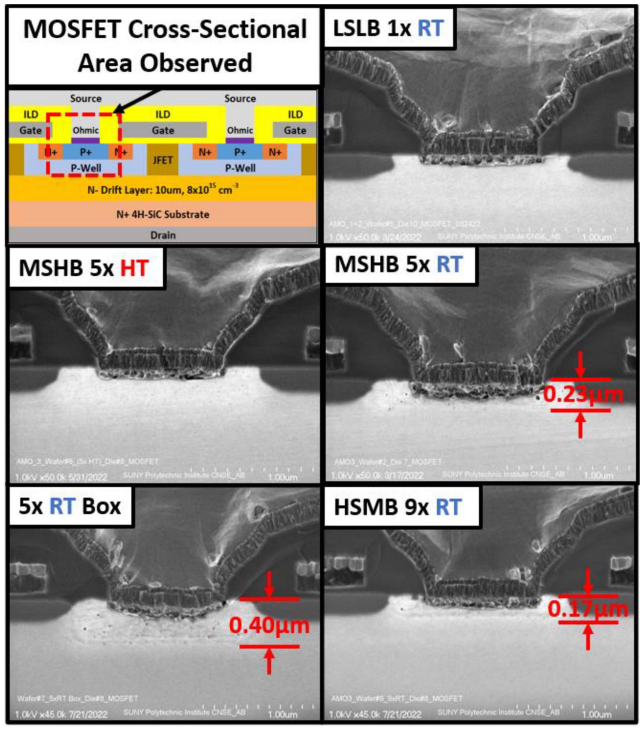

FIGURE 11. Cross sectional SEM images of the P+ source regions within the MOSFETs fabricated with various implantation conditions. Unlike the X-Ray topography images, a damaged lattice and voids can be observed within the active area for the 'HSMB 9xRT', 'MSHB 5xRT', and '5x RT Box' conditions. Depth of the implantation damage are given for each structure.

TABLE 3. Average and standard deviation of the specific on resistances of the MOSFETs with various implantation conditions. Large variations in the specific on-resistance ($R_{on,sp}$) can be observed in the 'RT Box' implanted MOSFETs indicating a large amount of lattice damage suffered during this implantation conditions when compared to the various other conditions. $R_{on,sp}$ was determined at a gate bias V_{gs}=20V, and a drain-source current (I_{ds}) of 0.1A.

	'LSLB 1x HT'	'LSLB 1x RT'	'MSHB 5x RT'	'MSHB 5x HT'	'5x RT Box'	'HSMB 9x RT'
Average Ron,sp [mΩcm²]	4.16	4.37	4.56	4.26	7.55	4.15
Std.Dev Ron,sp [mΩcm²]	0.24	0.17	0.54	0.36	1.74	0.37

within the various MOSFET structures. From these images, voids, and a damaged lattice can be observed within the P+ implanted regions for the 'HSMB 9x RT', 'MSHB 5x RT' and '5x RT Box' devices. Depth of the damaged lattice extends to 0.17μm, 0.23μm, and 0.40μm for the 'HSMB 9x RT', 'MSHB 5x RT' and '5x RT Box' P+ implantation conditions respectively.

In both the X-Ray Topography and X-SEM analysis, the 'HSMB 9x RT' condition showed the least amount of BPD generation and shallowest lattice damage respectively for non 'LSLB 1x' or HT implanted conditions. This can be attributed to the profile shift of 'HSMB 9x' condition. While this profile contains nearly two times the total dose as the 'MSHB 5x' conditions, the 'HSMB 9x' profile uses higher doses at its lower energy implants while simultaneously reducing the dose at higher energy implants [6]. This consideration of the dose at higher energies resulted in an overall lower ion bombardment damage. This concept can further be seen when comparing the 'MSHB 5x' condition to the '5x Box' profiles. Even though the two profiles have the same net dose, the greater dose at the higher energies used in the formation of the '5x Box' profile resulted in greater BPD generation and deeper lattice damage when compared to is 'MSHB 5x' counterpart.

C. FORWARD CONDUCTION OUTPUT

Fig. 12 and Table 3 shows the typical forward conduction and statistical values of the various MOSFETs fabricated under different implantation conditions respectively. Both 'LSLB 1x' conditions, the 'MSHB 5x HT' and 'HSMB 9x RT' devices showed average $R_{on,sp}$ values all within a 5% difference from each other and contain relatively low

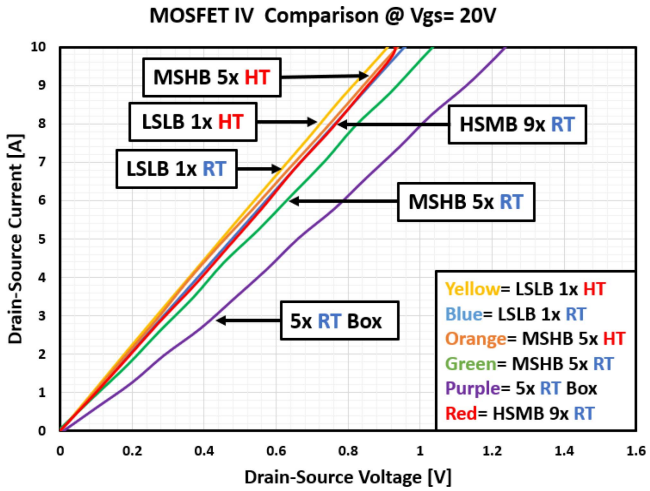

FIGURE 12. Typical forward conduction comparison of the various MOSFETs with various P+ implantation profiles at a gate bias of V_{gs}=20V. Non-linear pinching behavior can be observed in the '5x RT Box' implanted devices, and 'MSHB 5x RT' implanted device sto a lessert extent. This causes higher Ron,sp when compared to other implantation conditions. All forward conduction measurements were performed on wafer and at 25°C.

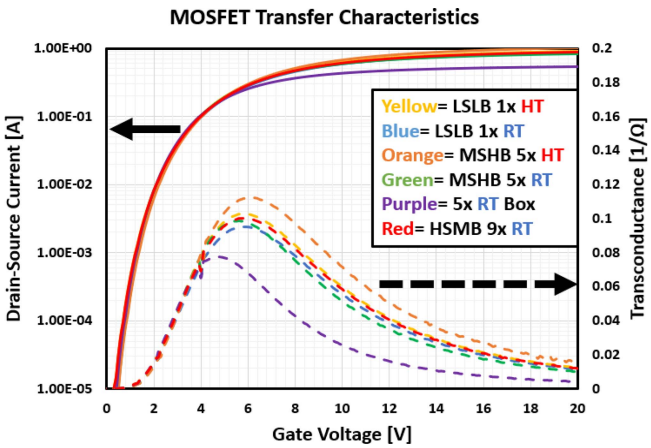

FIGURE 13. I_d-V_g Transfer characteristics (solid lines) of the MOSFETs with various P+ implantation profiles along with the corresponding transconductance curves (dashed lines). A V_{ds} of 0.1V was applied and all curves were measured on wafer and at 25°C.

variation. However, the same cannot be seen for the 'MSHB 5x RT' and '5x RT Box' devices. Devices implanted under these conditions showed non-linear pinching behaviors, and higher degrees of $R_{on,sp}$ variation. This pinching behavior and $R_{on,sp}$ variation are more prominent in devices fabricated utilizing the '5x RT Box' implant condition. Transfer characteristics of the '5x RT Box' MOSFETs are also impacted by this damaged lattice, constricting current flow resulting in lower saturation currents as observed in Fig. 13. As a result, MOSFETs fabricated under this implantation were significantly hindered, making it inferior to the other various conditions.

Obviously, the forward conduction output characteristics of the MOSFET devices are affected by the high lattice damage generation during the ion implantation process.

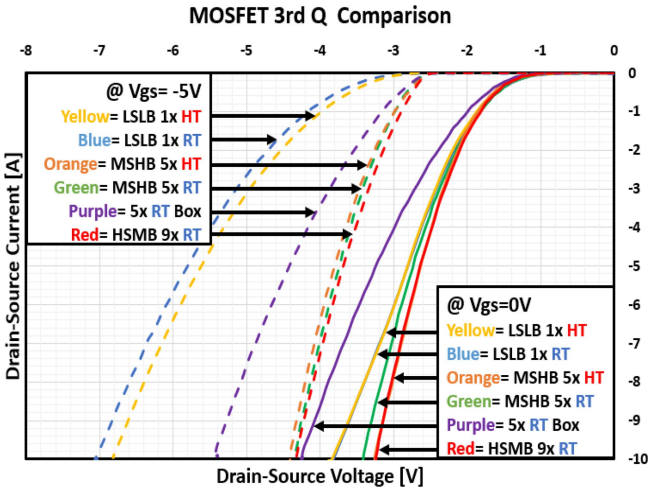

FIGURE 14. Typical 3rd quadrant comparison of the MOSFETs with various P+ source implantation profiles. The solid and dashed curves are measured at a gate bias of V_{gs}=0V and V_{gs}= −5V respectively.

Interestingly, this hindered performance is in the form of non-linear pinching and not a shift in the threshold voltage even though the P+ implantation is directly connected to the P-body contact. It is important to note that even though the 'HSMB 9x RT' implanted devices showed a slightly damaged lattice within the X-SEM images, no pinching behavior can be observed within these structures.

D. 3RD QUADRANT OUTPUT CHARACTERISTICS

The typical 3rd quadrant output characteristics for MOSFETs with various implantation splits can be seen in Fig. 14. When a gate bias of V_{gs}=−5V was applied (thereby closing off conduction through the channel), both the 'MSHB 5x' conditions and the 'HSMB 9x RT' offered near optimal performances. Unlike the forward conduction, both '1x' conditions suffered due to a lack of current flow at the same Drain-Source bias (V_{ds}) when compared to the higher P+ implantation MOSFETs. As seen in Fig. 15, these 3rd Quadrant device performances follow a similar trend to the P+ contact resistance for each implantation condition. P+ implantation conditions with lower doping concentrations near the surface result in a higher ohmic contact resistance [6], and thus greater overall resistances within the 3rd Quadrant of operation. Overall, the switch to all RT implantation has minimal effect on the 3rd quadrant MOSFET performance if the P+ profile is sufficient to minimize the contact resistance.

However, this trend is broken when examining the '5x RT Box' devices. This can be attributed to the severely damaged lattice within the P+ source regions. As observed in Table 4, the variation within the '5x RT Box' condition is ∼6x greater than the low damage devices which is evident of random defects limiting current flow [6], [12]. Although, this damaged lattice is still observed within the 'MSHB 5x RT' and 'HSMB 9x RT' implanted devices, the overall damage suffered is much less, and has minimal effects on

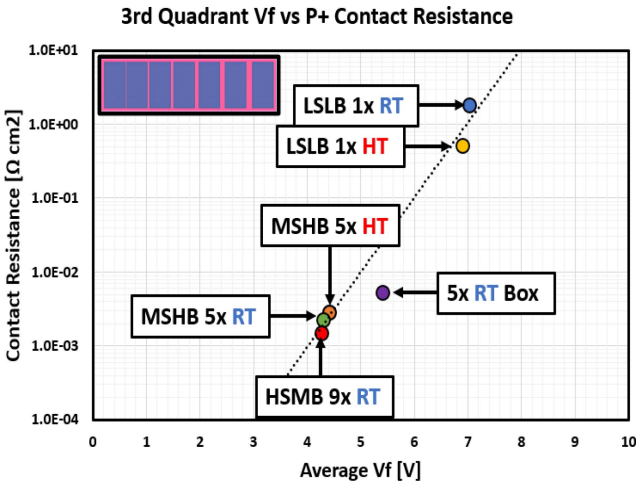

FIGURE 15. Contact resistance of the various P+ implantations used for the MOSFET source regions. Trends seen within the contact resistance for the various implantations mimics the trends observed in the 3rd quadrant output, with exception of the '5x RT Box' implantation condition.

TABLE 4. Average and standard deviation of the Source-Drain voltage drop (V_{sd}) of the MOSFETs fabricated with various implantation conditions. Large variations in the V_{sd} can be observed in the 'RT Box' implanted MOSFETs indicating a large amount of lattice damage suffered during this implantation conditions when compared to the various other conditions. V_{sd} was determined at a gate bias V_{gs}=−5V, and a drain-source current (I_{ds}) of 10A.

	'LSLB 1x HT'	'LSLB 1x RT'	'MSHB 5x RT'	'MSHB 5x HT'	'5x RT Box'	'HSMB 9x RT'
Average Vsd [V]	6.80	7.03	4.31	4.41	5.24	4.28
Std.Dev Vsd [V]	0.05	0.05	0.11	0.04	0.34	0.09

3rd Quadrant performances. Therefore, utilizing this 'MSHB 5x RT' and 'HSMB 9x RT' P+ implantation results in a device matching the 3rd quadrant electrical performances as an elevated dose and temperature implanted MOSFET.

E. FORWARD BLOCKING CHARACTERISTICS

Fig. 16 shows the representative forward blocking behavior of the MOSFETs fabricated under the various P+ implantation conditions. Both 'LSLB 1x' profiles, the 'MSHB 5x HT' and 'HSMB 9x RT' profiles show near ideal forward blocking behaviors with and breakdown voltage of ∼1600V, accompanied by low leakage currents at the blocking rating of 1200V. Although the 'MSHB 5x RT' implanted MOSFETs showed the same ideal breakdown voltage, the leakage current for these devices significantly increased by ∼100x at 1200V. The '5x RT Box' implanted MOSFETs showed no forward blocking capabilities unlike the other conditions, resulting in the 1mA compliance below V_{ds}=10V. Therefore, this lack of blocking capabilities in the '5x RT Box' devices and increased leakage current in 'MSHB 5x RT' devices when compared to the remaining conditions can be attributed to the increased amount of lattice damage observed in the MOSFET structures.

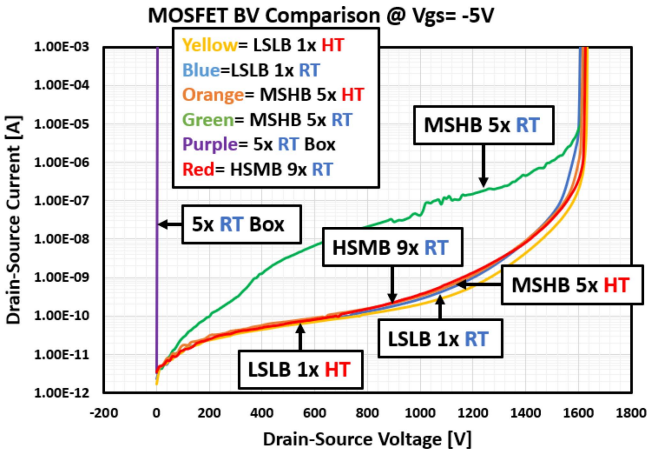

FIGURE 16. Forward blocking comparison of the various MOSFETs with various P+ source implantation profiles. A hybrid edge termination structure was employed to ensure a near ideal breakdown voltage and to minimize the leakage current. All leakage curves were performed at V_{gs}= −5V to minimize any potential leakage through the channel. All curves are representative and were measured on wafer and at 25°.

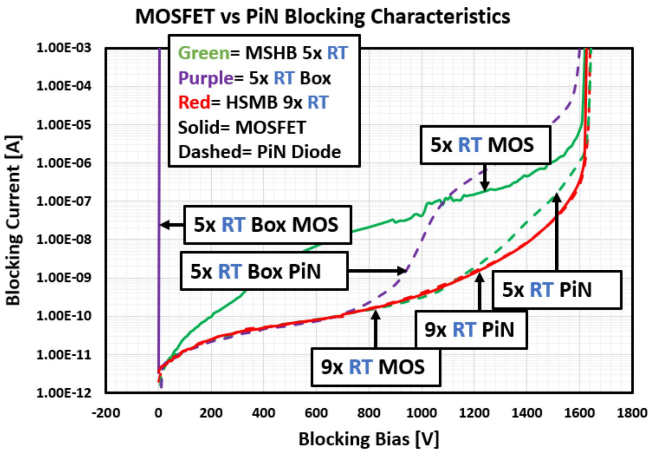

FIGURE 17. Forward blocking comparison of MOSFETs and reverse characteristics of PiN diodes fabricated with the 'MSHB 5xRT', 'MSHB 5x RT Box' and 'HSMB 9xRT' P+ impanation conditions [6]. Both PiN diodes and the MOSFETs were fabricated using the hybrid edge termination structure with the active region being the primary difference between the two devices. MOSFET leakage curves were performed at V_{gs}= −5V to minimize any potential leakage through the channel and provide the current flow solely through the body diode instead. All curves are representative and were measured on wafer and at 25°.

This is apparent when the MOSFETs fabricated with BPD generating P+ implantation conditions ('HSMB 9xRT', 'MSHB 5xRT', and '5xRT Box') are compared with their PiN diode counterpart in Fig. 17 [6]. Both PiN diodes and the MOSFETs were fabricated using the hybrid edge termination structure with the active region being the primary difference between the two devices. The 'HSMB 9xRT' devices showed the same blocking characteristics therefore resulting in the hybrid edge termination being the limiting factor in leakage current. However, for both the 'MSHB 5xRT' and '5x RT Box' leakage current for the MOSFETs increases significantly from its PiN Diode counterpart. Therefore, this

lack of blocking capabilities in the '5x RT Box' devices and increased leakage current in 'MSHB 5x RT' devices when compared to the remaining conditions can be attributed to the increased amount of lattice damage and BPD generation observed in the active area of the MOSFET structures.

Apart from severe BPD generation caused by profiles using high energy and dose implantations ('MSHB 5xRT', and '5xRT Box'), the use of all RT implantation had negligible effects on the forward bocking device performance. Therefore, it is vital to have proper control over the P+ implantation to mitigate BPD and other forms of lattice damage generation as seen in the 'HSMB 9x RT' structures.

VI. CONCLUSION

Several 1.2kV MOSFETs fabricated under various implantation conditions were successfully fabricated to determine the validity of all room temperature implantation. Static performances of the MOSFETs, applying RT implantation for the JFET, P-Well, N+ and JTE resulting in negligible differences when compared to HT implantation counterparts. When it came to the formation of the P+ regions, it was shown that implantation dose higher than $1\times10^{15}\text{cm}^{-2}$ was required for reasonable contact resistance which resulted in BPD and lattice damage when implanted at room temperature. It is confirmed that this high dose and energy of Al ion implantation at RT generates large amount of defects and lattice damage, which hinders the MOSFET electrical characteristics. However, RT P+ implantation profiles that utilized high dose at lower energy implantations (i.e., 'HSMB 9x RT') reduced the BPD generation, lattice damage, and therefore showed negligible effect on MOSFET static performances. Although there is still process induced lattice damage and BPD generation observed, this profile control over the P+ implantation is believed to be the right step in mitigating BPDs, and other subsequent lattice damage generated from the ion implantation process. This can be accomplished while simultaneously ensuring optimal device performance and reducing processing time, energy, cost, and complexity of the MOSFET fabrication process.

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