VREL

Power Electronics Materials and Bonded Interfaces – Reliability and Lifetime

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OVERVIEW

- Project start: October 2018
- Project end: September 2024 (90% completion)
- Total project funding (to date): \$1,000,000; DOE share: \$1,000,000; funding for FY24: \$150,000
- Technical barriers addressed: cost, size and weight, performance, reliability and lifetime.

RELEVANCE

- Wide-bandgap devices such as silicon carbide and gallium nitride enable low-cost, lightweight, and power-dense automotive power electronics; however, these technologies are currently limited by power electronics packaging.
- It is critical that the packaging design and materials withstand the high-temperature operational environment introduced by the wide-bandgap devices; bonded interfaces must be reliable under extreme thermal stress conditions.
- The main objective of this project is to evaluate the reliability and study the failure mechanisms of bonded interface materials for high-temperature power electronics applications.

COLLABORATIONS

- CuNex GmbH: technical partner on the synthesis of sintered copper samples and reliability evaluation study.
- Rogers Corporation: AMB substrates
- NoMIS Power: silicon carbide MOSFET supplier
- Microchip: silicon carbide MOSFET supplier
- Georgia Tech, Oak Ridge National Laboratory, Ames Laboratory, and Sandia National Laboratories: technical guidance and discussion.

SUMMARY

- Samples with sintered Cu as the substrate-attach layer were fabricated and subjected to a thermal profile of -40° C to 200° C.
- Samples with a 3-mm-thick baseplate were found to be reliable, with crack percentages estimated at approximately 5% even after 1,000 cycles.
- We implemented a domain-transfer technique to quickly estimate the crack percentage from C-SAM images; additional filtering techniques will be investigated to improve the accuracy of this technique.

APPROACH

Sample Fabrication

- The Cuprum 80 paste from Cunex GmbH is composed of surface-enhanced microscale flake-type particles in an organic binder capable of reducing Cu oxides in situ during the sintering process.
- nonconformities on the baseplate, the substrate, and Sample configuration consists of a Cu baseplate the printed paste. (approximately 50 mm x 50 mm) and an AMB substrate (0.3-mm-thick Cu, 0.25-mm-thick Si3N4, and After sintering, the samples were cooled down at a rate 0.3-mm-thick Cu) obtained from Rogers Corporation. of 50° C/min, which is essential to control the warpage and thermomechanical stress buildup in the samples.



Cu paste stencil-printed on the baseplates (top) and the corresponding C-SAM images after sintering (bottom); bond patterns are stripe (left), grid (center), and a full-area print (right). Photo by Rodolfo Saccon, THI

ACCOMPLISHMENTS AND PROGRESS

Crack Growth

- After 1,000 cycles, crack growth in samples with the 3-No significant difference can be observed between the mm-thick baseplate was measured at 5%. two bond patterns (3-mm-thick baseplate data)
- We could not observe any distinctive differences between the 4- and 5-mm-thick cases, mainly due to the high variability among the individual samples of each case.



Crack percentages of sintered copper samples as a function of thermal cycles.

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Sintering Profile

- Sintering was performed in an inert atmosphere, within a Budatec SP300 sinter press at 275° C for 5 minutes under 15 MPa of bonding pressure.
- A 250-µm-thick Teflon sheet was used to ensure uniform pressure distribution and compensate for any



Thermal Shock Profile



Sample temperature under thermal shock

| Name | Cold End | Hot End | Ramp rate | Dwell time |
|---------|----------|---------|-----------|------------|
| | (°C) | (°C) | (°C/min) | (mins) |
| Profile | -40 | 200 | >25 | - |

Cu: copper, AMB: active-metal-bonded, C-SAM: C-mode scanning acoustic microscope, SEM: scanning electron microscope

Failure Mechanisms

- To investigate the failure mechanisms within the sintered Cu joint, we cross-sectioned a sample along the diagonal and obtained high-resolution scanning electron microscope images
- The dominant failure mechanism is adhesive fracture. mostly occurring at the interface between the bond layer and the Cu baseplate.



Cross-sectional scanning electron microscope images of a sintered Cu joint.

- The high variability among 4- and 5-mm-thick cases could be due to slight variations in the joint density introduced through the manual stencil printing process.
- Neither the grid nor the stripe pattern resulted in arresting the crack growth and cracks propagated continuously across the individual bond pads.



C-SAM images of a sample with grid pattern (top) and stripe pattern (bottom) at 0 cycles (left), 500 cycles (center), and 1,000 cycles (right).

ACCOMPLISHMENTS (contd.)

Image Denoising

- To calculate the crack percentages, we manually edited the raw C-SAM images to hide the patterns, but this is a time-consuming process.
- An alternative technique is to transfer the image from its spatial domain to frequency domain, filter out the high frequencies, which typically represent the noise (stencil patterns), and transfer the image back to spatial domain.





Crack percentages of a single sample estimated through two different techniques.

FUTURE WORK CHALLENGES AND BARRIERS

- Continue the thermal shock experiments of sintered copper.
- Conduct power cycling experiments with sintered copper bonded between silicon carbide MOSFETs and AMB substrates.
- Power cycling experiments could result in multiple failure mechanisms such as wire bond lift off. It is critical to design the experiment in such a way that failure occurs in the die-attach layer.

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Any proposed future work is subject to change based on funding levels.