IEEE Electronics Packaging Society Emerging Technology Technical Committee Meeting

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Researcher III
National Renewable Energy Laboratory (NREL)
Advanced Power Electronics and Electric Machines (APEEM) Group

June 27, 2024

Childhood

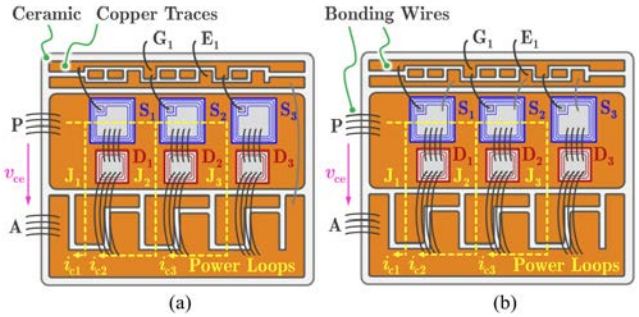
Childhood

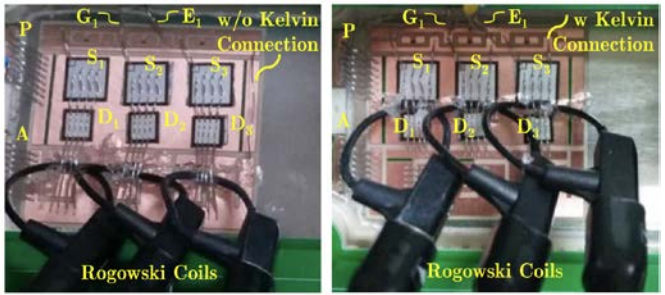
M.S.: Electric vehicle (EV) power modules

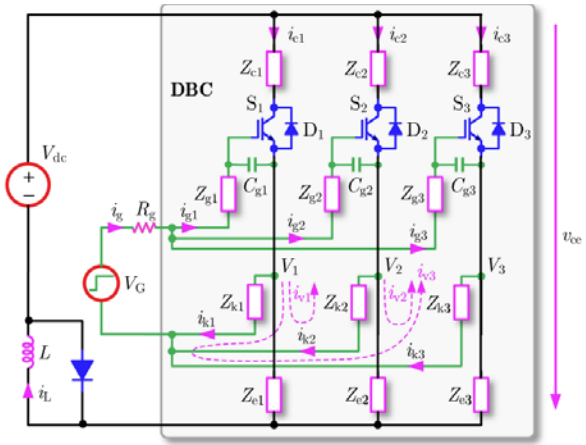
UK-China Silicon Carbide (SiC) Power Electronics Lab; electrical engineering advisor: Dr. Li Ran

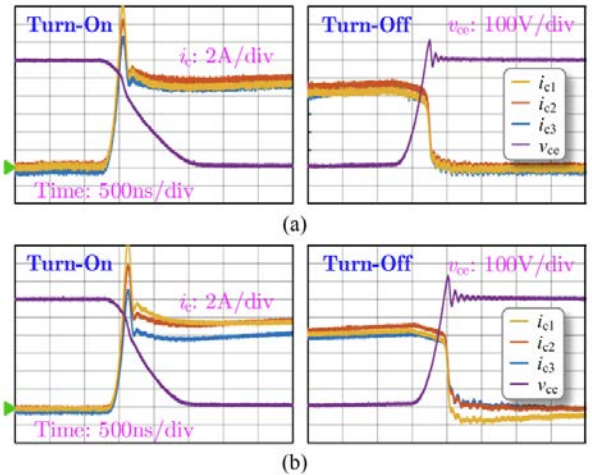
- Electrothermal profile of multi-chip SiC modules for EV applications.
- Condition monitoring of Si insulated-gate bipolar transistors (IGBTs).

❖ Multi-Chip Power Modules for EV Applications









Z. Zeng, X. Zhang, and **X. Li**. 2019. "Layout-Dominated Dynamic Current Imbalance in Multichip Power Module: Mechanism Modeling and Comparative Evaluation." *IEEE Transactions on Power Electronics* 34 (11): 11199–11214.

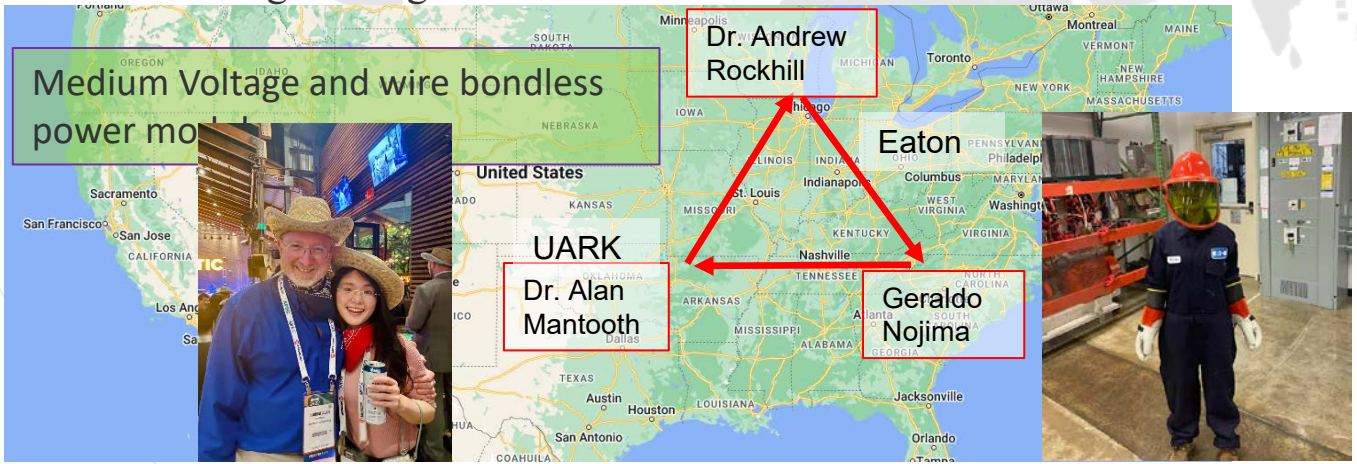
Childhood

M.S.: EV power modules

B.S.: Renewable energy

High-Density Electronics Center (HiDEC), University of Arkansas

Electrical engineering advisor: Dr. Alan Mantooth



- 10-kV SiC metal-oxide-semiconductor field-effect transistor (MOSFET) power module with optimized electric field distribution and electromagnetic interference (EMI) performance (National Science Foundation).
- Integrated reduced-expansion microchannel cooling for SiC power converter (Navy Small Business Technology Transfer).

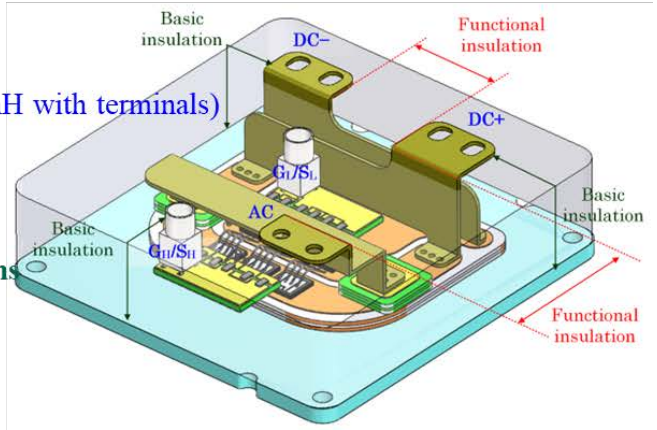
A 10-kV SiC MOSFET Power Module With Optimized System Interface and Electric Field Distribution

■ Main Specifications

Parameter	Value
Rating	10 kV/60A
Configuration	Half-Bridge
Dimensions	97mm x 99mm x 44mm
DC-link voltage	6 kV – 7.2 kV
Line-line AC voltage (rms)	4.16 kV
Overvoltage Category	3
Pollution Degree	2
Altitude	≤ 2000m
Housing material CTI	> 600
Required Impulse Withstand Voltage	18.6 kV

External Insulation-Module-system Interface

- **Low inductance**
  - **Electric-potential-oriented module-system interface concept**
  - Power-loop: 5.3 nH with integrated decoupling capacitors (16.4 nH with terminals)
- **High Voltage Capability**
  - Middle layer patterned multilayer substrates
  - reducing the maximum E-field by **38.6%**
  - Enable sufficient partial discharge inception voltage **≥ 16.8 kVrms**
- Improved EMI performance
  - Parasitic capacitance reduction, **down to a record-low 28 pF.**
  - Surface flashover: 32 kV DC and 25 kV AC



A 10-kV SiC MOSFET Power Module With Optimized System Interface and Electric Field Distribution

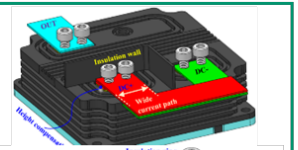
Active Gate Driver

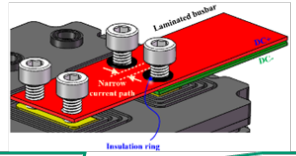
Develop improved gate drivers with

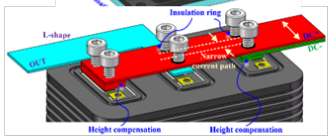
- Balanced current sharing
- Current sensor
- Protection capabilities

Laminate Busbar

Line to ground 7.2 kVrms

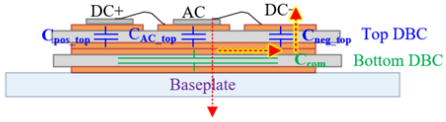






Power Module Packaging

- MV insulation
- Partial discharge
- Parasitic parasitic L
- Common mode C



System Performance

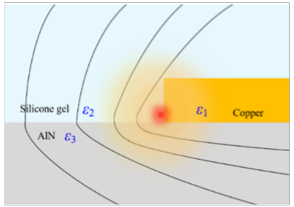
• EMI • Thermal management • System level insulation

X. Li, Y. Chen, H. Chen, R. Paul, X. Song, and H. A. Mantooth. 2024. "A 10 kV SiC MOSFET Power Module With Optimized System Interface and Electric Field Distribution." *IEEE Transactions on Power Electronics* 39 (8): 9540–9553.

➢ Patterned Middle-layer Stacked Substrate: Partial Discharge Inception Voltage

Partial Discharge occurs when the electric field > insulation material's critical dielectric strength

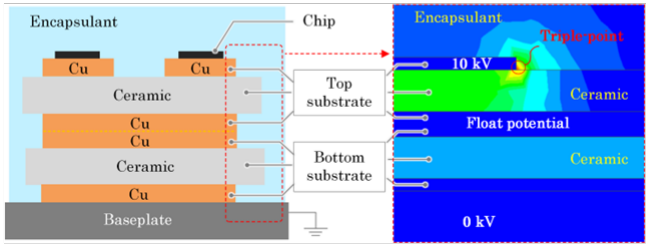
Triple Point - copper-ceramic-gel junction



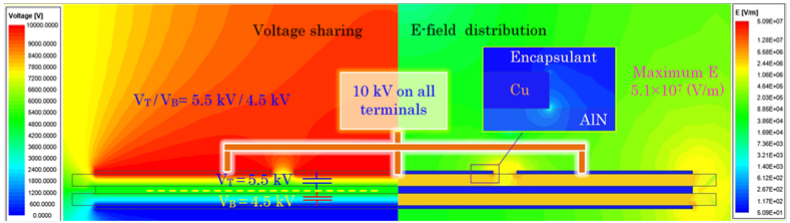
$$\varepsilon_1 E_{n1} = \varepsilon_2 E_{n2} = \varepsilon_3 E_{n3}$$

$$E = -\nabla\varphi$$

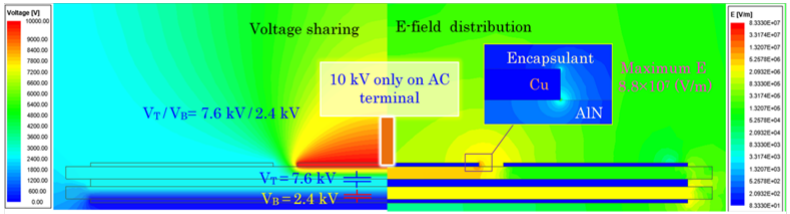
Stacked substrates



Optimize φ in stacked substrates → Reduce the maximum E-field



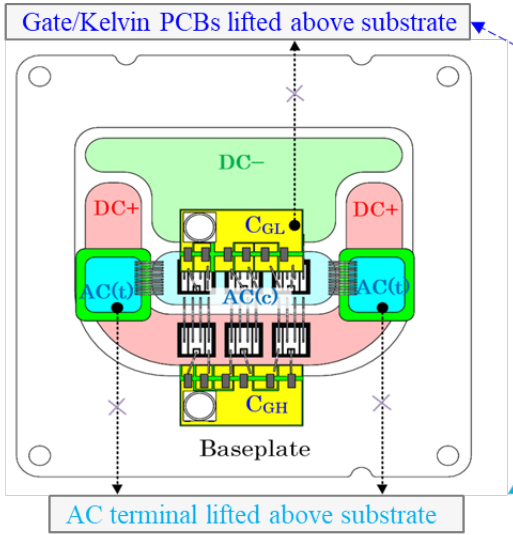
Lumped terminals

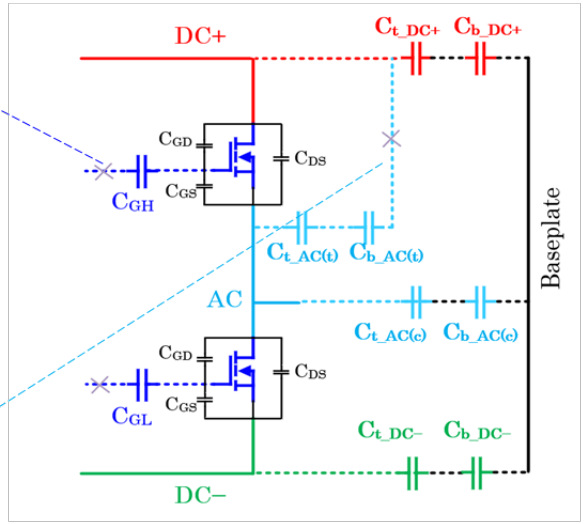


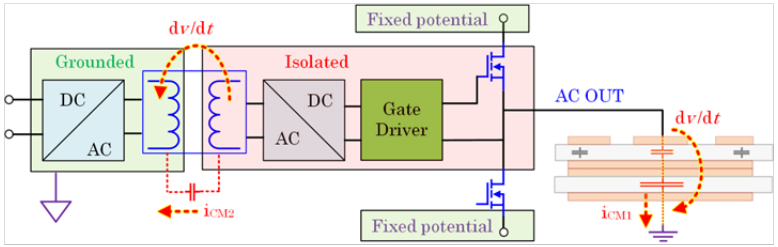
Designated terminal

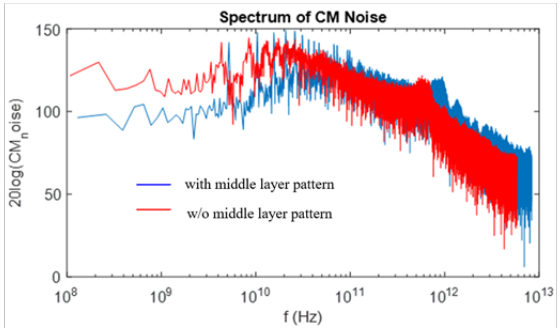
For solid middle-layer stacked substrates, the lumped terminal connection results in overestimated PDIV

➢ Patterned Middle-layer Stacked Substrate: EMI



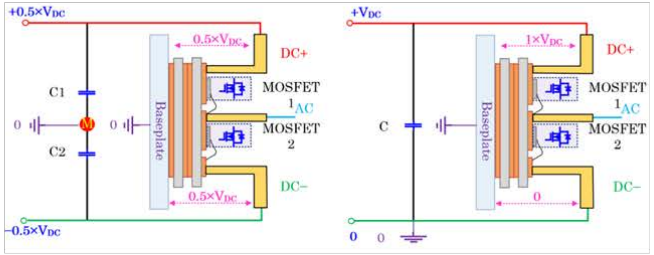


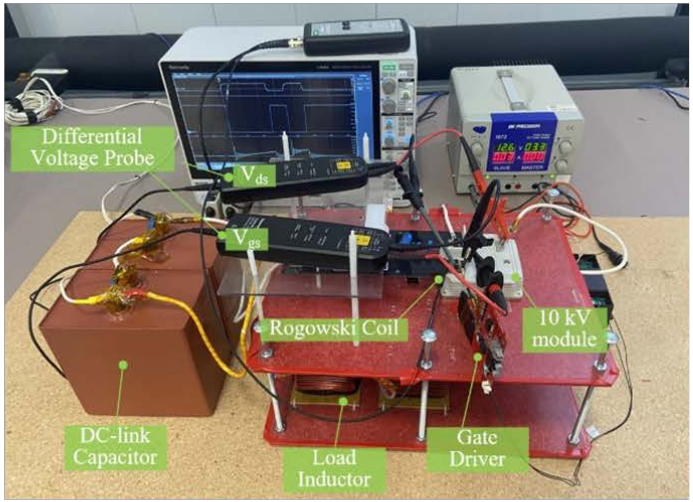




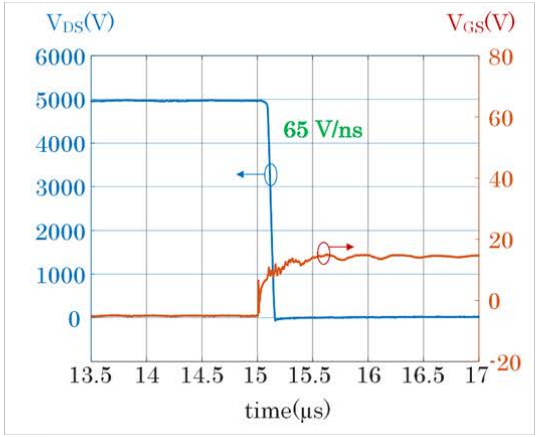
A 10-kV SiC MOSFET Power Module With Optimized System Interface and Electric Field Distribution

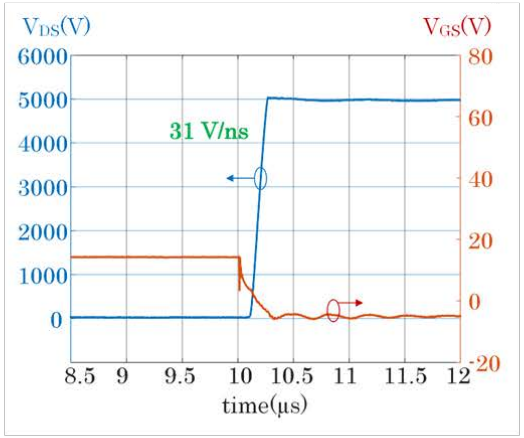
❖ Double-pulse Test





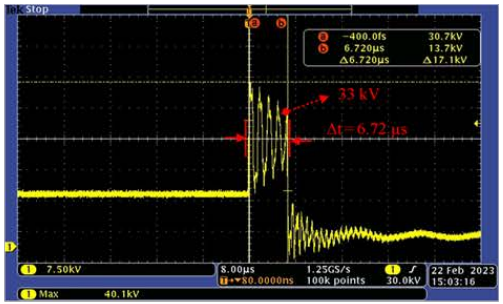
Double-pulse test setup



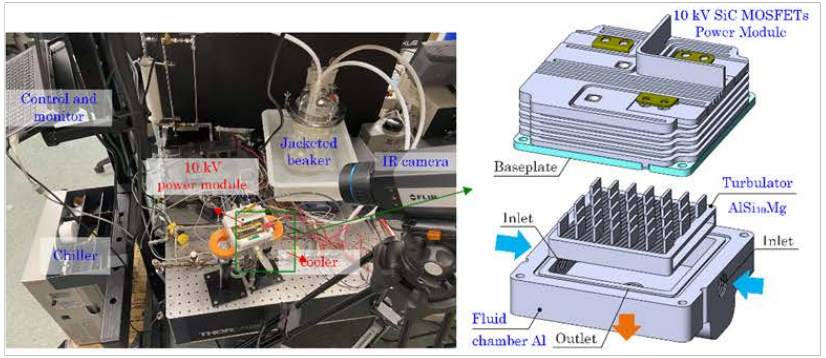


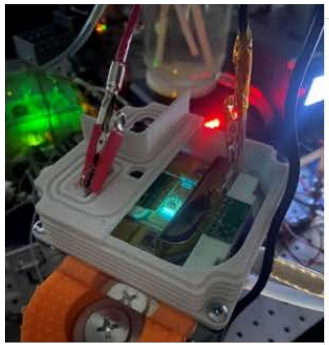
A 10-kV SiC MOSFET Power Module With Optimized System Interface and Electric Field Distribution

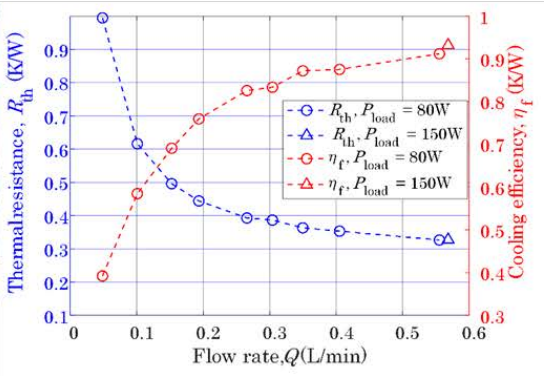
❖ Surface Flashover Test



❖ Thermal Test with Multi-tier Cooler







Childhood

M.S.: EV power modules

B.S.: Renewable energy

APEEM Group
Manager: Dr. Sreekant Narumanchi

U.S. Department of Energy Laboratories

Office of Science Laboratories

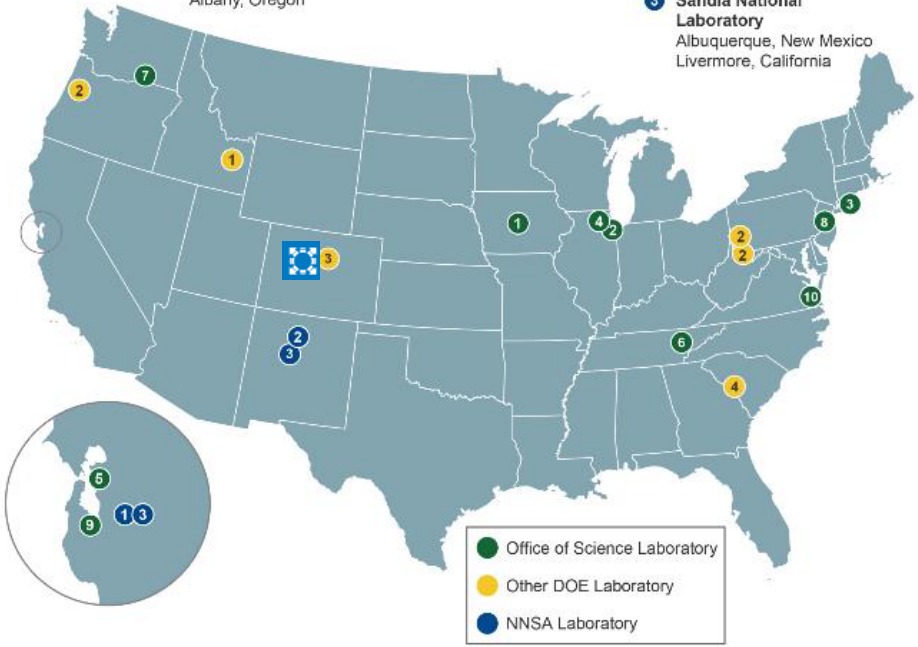
1. **Ames Laboratory**
   Ames, Iowa
2. **Argonne National Laboratory**
   Argonne, Illinois
3. **Brookhaven National Laboratory**
   Upton, New York
4. **Fermi National Accelerator Laboratory**
   Batavia, Illinois
5. **Lawrence Berkeley National Laboratory**
   Berkeley, California
6. **Oak Ridge National Laboratory**
   Oak Ridge, Tennessee
7. **Pacific Northwest National Laboratory**
   Richland, Washington
8. **Princeton Plasma Physics Laboratory**
   Princeton, New Jersey
9. **SLAC National Accelerator Laboratory**
   Menlo Park, California
10. **Thomas Jefferson National Accelerator Facility**
    Newport News, Virginia

Other DOE Laboratories

1. **Idaho National Laboratory**
   Idaho Falls, Idaho
2. **National Energy Technology Laboratory**
   Morgantown, West Virginia
   Pittsburgh, Pennsylvania
   Albany, Oregon
3. **National Renewable Energy Laboratory**
   Golden, Colorado
4. **Savannah River National Laboratory**
   Aiken, South Carolina

NNSA Laboratories

1. **Lawrence Livermore National Laboratory**
   Livermore, California
2. **Los Alamos National Laboratory**
   Los Alamos, New Mexico
3. **Sandia National Laboratory**
   Albuquerque, New Mexico
   Livermore, California



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National Renewable Energy Laboratory

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3,700 employees with world-class facilities

Campus is a living model of sustainable energy

Sponsored by the U.S. Department of Energy

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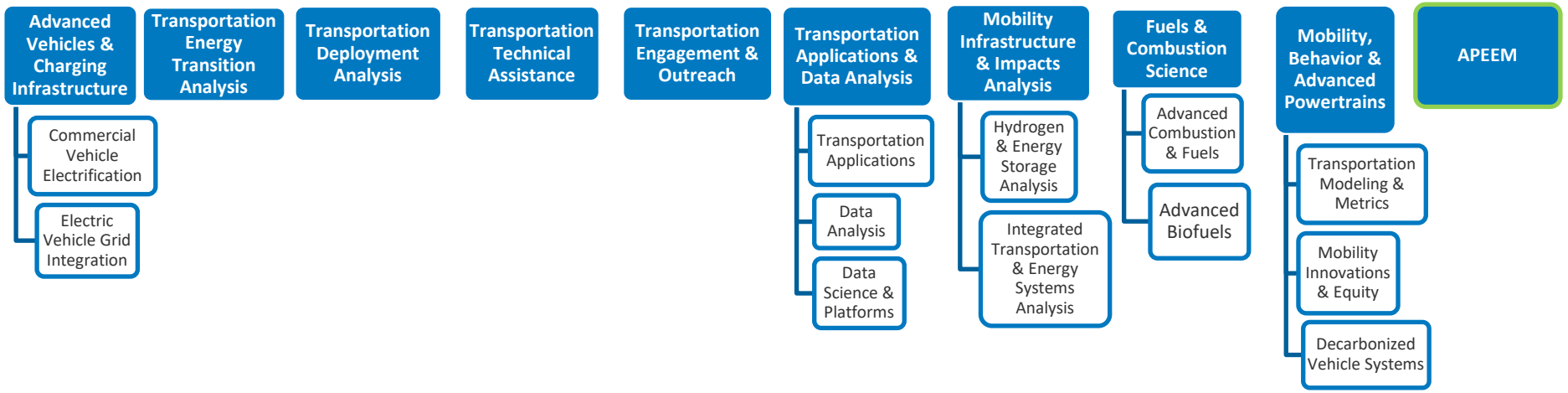


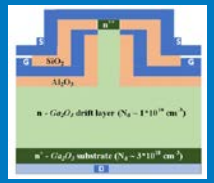
Center for Integrated Mobility Sciences

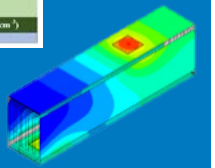
APEEM group manager: Sreekant Narumanchi

Fifteen staff members involved in electrothermal, thermal-fluids, thermomechanical, and reliability research activities.

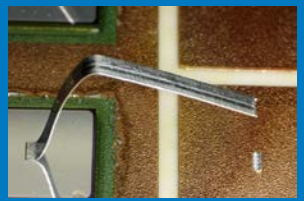
NREL APEEM Group Research Focus Areas

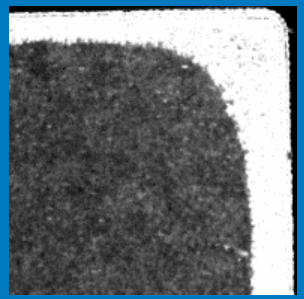
Power Electronics



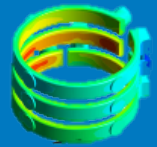


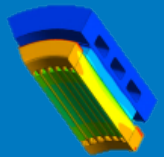
Advanced Packaging Reliability





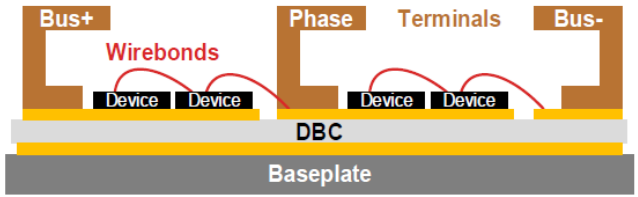
Electric Motors



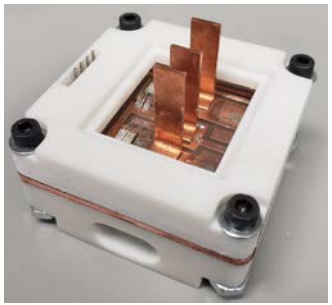


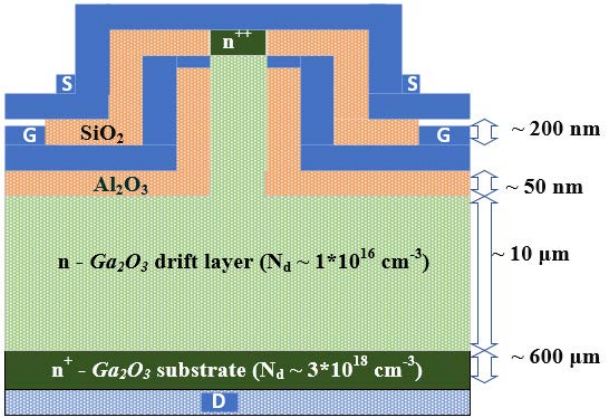
Power Electronics: Semiconductor Device and Package Research

- Semiconductor modeling research for wide-bandgap (WBG) and ultrawide-bandgap (UWBG) devices.
- Electrical and electromagnetic design for power electronics packages.
- Develop new packaging technologies.

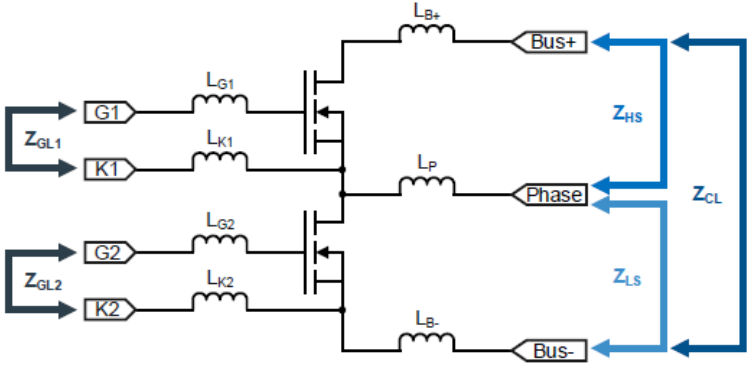


Multi-chip power module





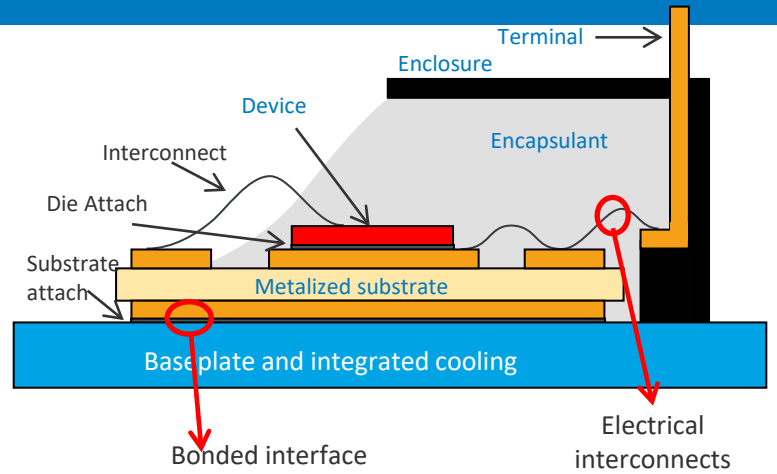
Micro-/nanoscale device modeling

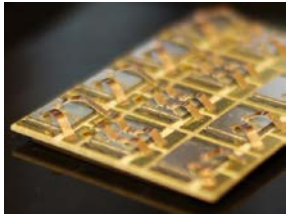


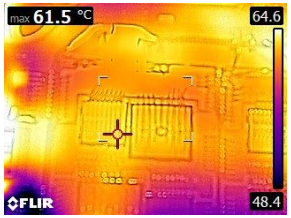
Equivalent circuit of extracted package

Advanced Power Electronics Reliability

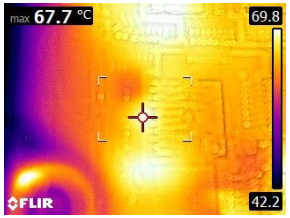
- Improve reliability.
- Develop predictive and remaining lifetime models.
- State-of-health estimation.
- Package parametric modeling.



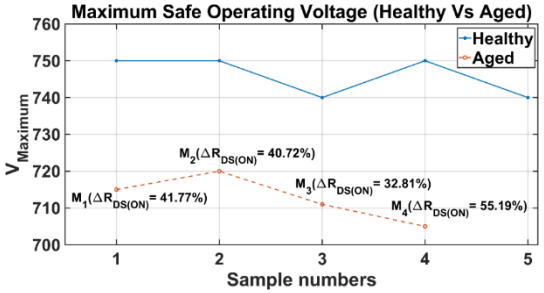




Healthy device



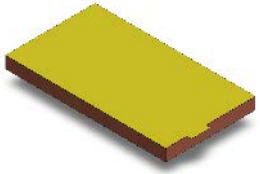
Aged device (hot spot is formed)



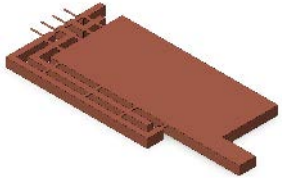
Destructive test results (safe operating area goes down with aging)

Advanced Packaging Incorporating ODBC

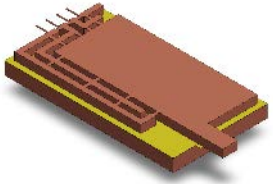
Simplified packaging process has been envisioned with organic direct-bond copper (ODBC) substrates in a double-side-cooled module.



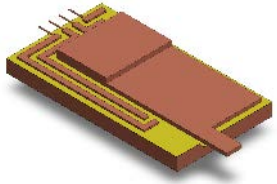
1. *Bond lower Temprion layer to lower cold plate.*



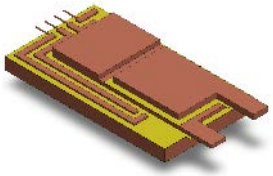
2. *Etch bottom face of drain busbar and traces.*



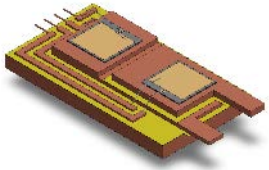
3. *Bond drain busbar and traces to lower Temprion layer.*



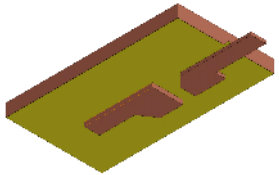
4. *Etch top face of drain busbar and traces.*



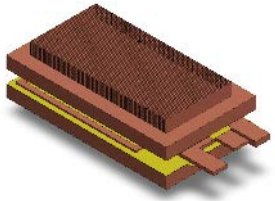
5. *Bond middle Temprion layer and output 2 busbar.*



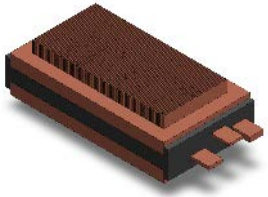
6. *Sinter and wire bond devices.*



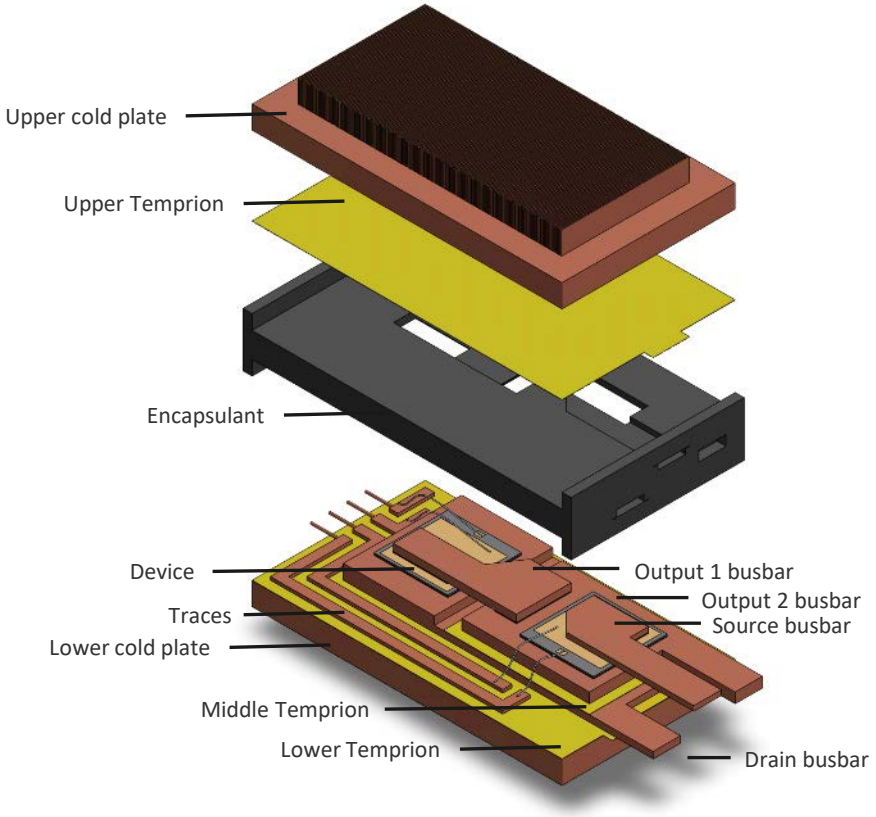
7. *Bond output 1 and source busbars to upper Temprion and upper cold plate.*



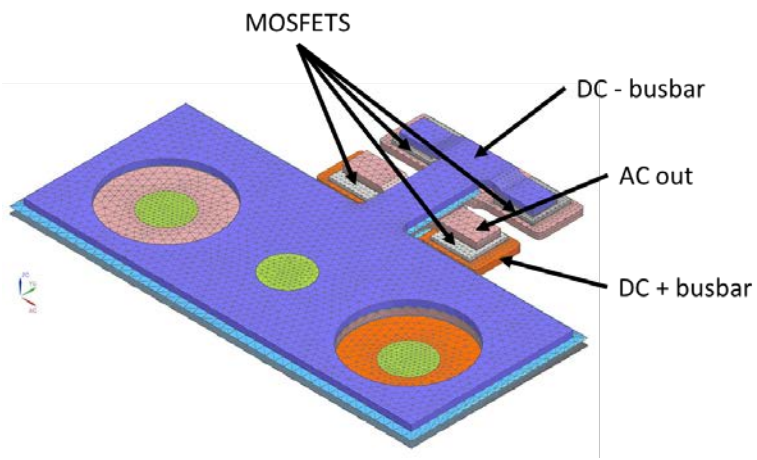
8. *Sinter previous assembly to devices.*



9. *Fill cavity with encapsulant.*



Advanced Packaging Incorporating ODBC



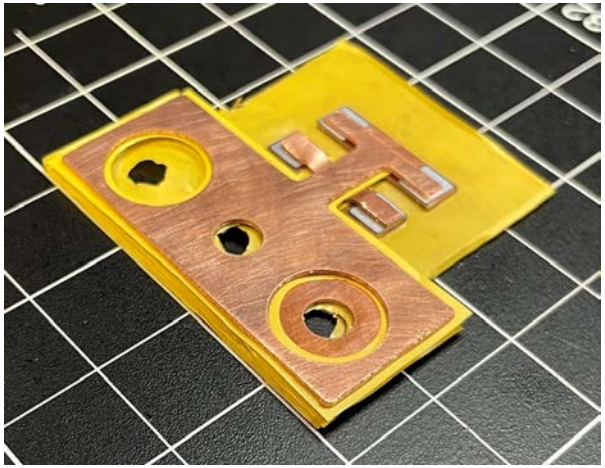
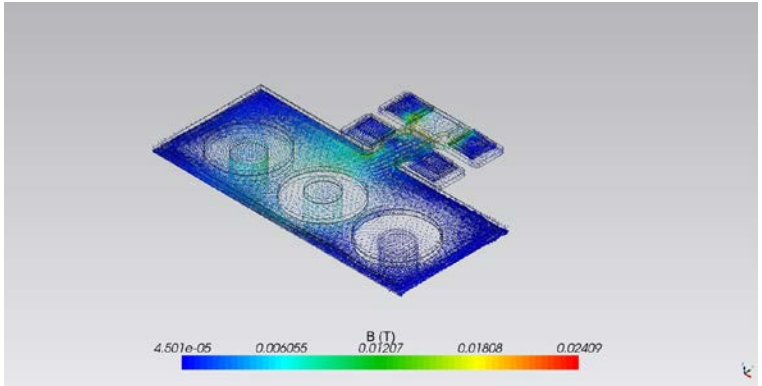
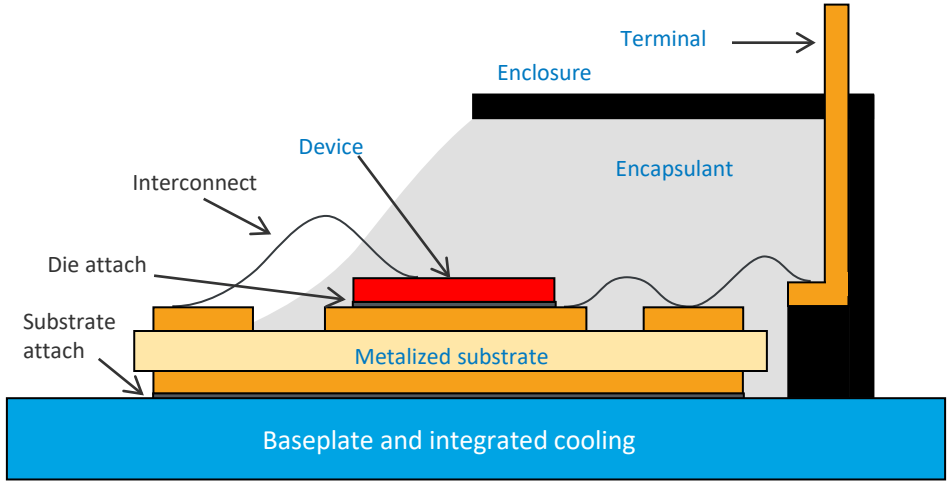


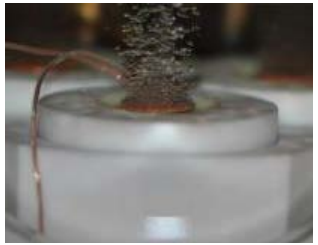
Photo credit: Joshua Major



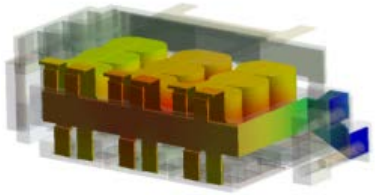
Power Electronics Thermal-Fluids Research

- Compact, power-dense WBG-device-based power electronics
  - Higher-temperature-rated devices, components and materials.
  - Advanced heat transfer technologies.
  - System-level thermal management.





Advanced cooling

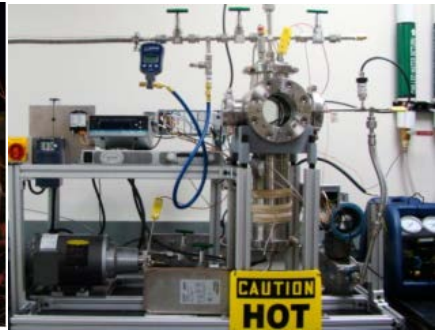


Component-level and system-level heat transfer

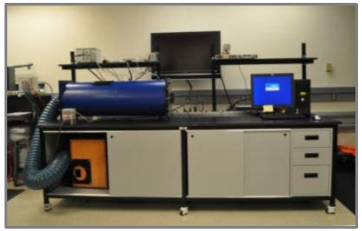
Thermal-Fluids Capabilities

Laboratory Resources

Single-phase liquid loops

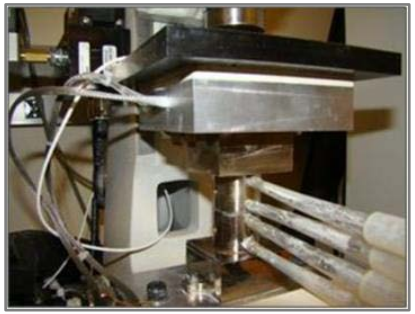


Two-phase liquid loops



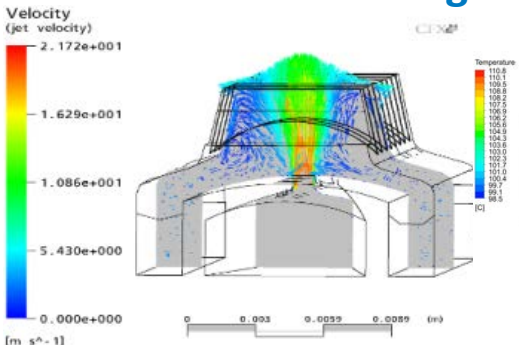
Air cooling loops

Transient thermal tester

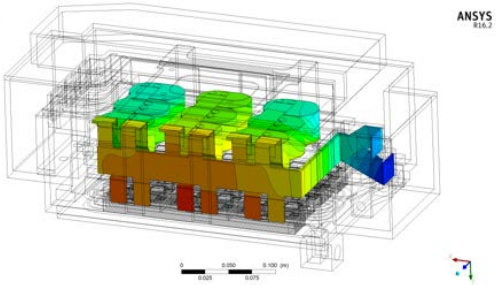


Material thermal resistance characterization

Modeling Capabilities



Computational fluid dynamics

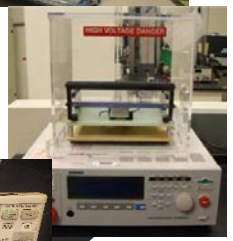


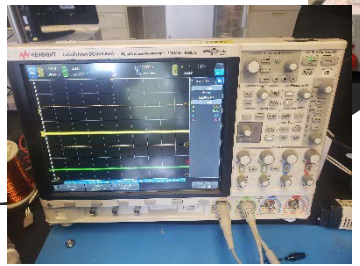
Thermal finite element modeling

Electrical Characterization Capabilities

I/V characterization

High voltage/current

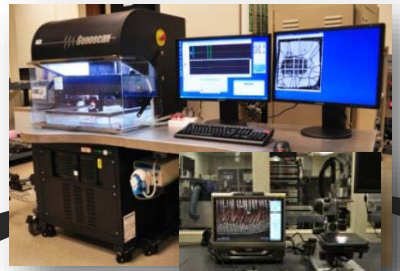




Impedance spectroscopy

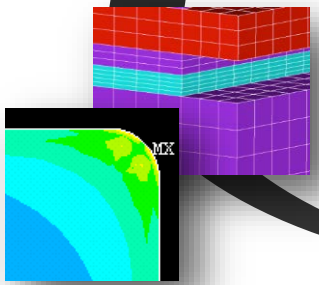
Thermo-mechanical Reliability Capabilities

Nondestructive imaging

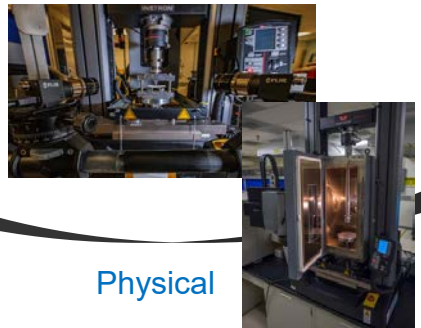


Electrical

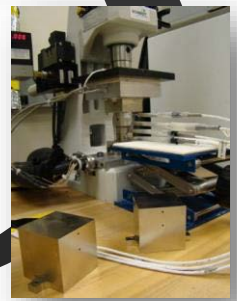
Accelerated testing



Thermomechanical modeling



Physical



Thermal

How To Work With NREL

Visit: www.nrel.gov/workingwithus/technology-partnership-agreements.html

- Shared resources collaboration (U.S. Department of Energy Electric Drive Technologies projects).
- Cooperative research and development agreements (CRADAs)
  - Shared resources
  - Funds-in.
- Strategic partnership projects
  - Interagency agreement
  - Funds-in agreement
  - Technical services agreement.
- Teaming on proposals in response to solicitations.

Thank You!

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Xiaoling.Li@nrel.gov

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