An organic, direct bonded copper, multi-layered, ultra-low inductance package for high-power UWBG MOSFETs

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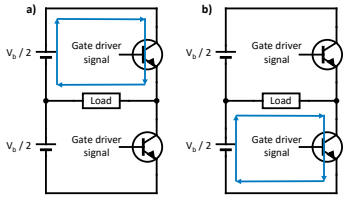
Introduction

Maximizing efficiency in electric vehicles (EVs) is critical to fully replacing gas-powered vehicles. A key focus area for improving efficiency in EVs is in the components responsible for electricity transmission throughout the vehicle, especially the **power inverter.**

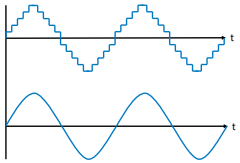
What does an EV inverter module do?

- Converts DC power from the batteries into AC, used by the high-current induction motors.
- One half-bridge inverter module uses at least one pair of transistors, normally Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), to convert battery VDC to VAC.



Current flow through half-bridge inverter circuit when a) the upper and b) the lower MOSFETs are closed, producing an alternating signal at the load.

- The MOSFETs rapidly switch on and off on the to produce a smooth sinusoidal AC signal.



Graphical representation of how a sinusoidal AC waveform can be generated by rapid toggling of MOSFETs.

- A **faster switching speed** improves motor efficiency, but simultaneously introduces harmful parasitic inductance as a result of the rapid changes in voltage and current (dV/dt and dI/dt). [1]
- This unwanted inductance can cause damage to the transistors or other components. Thus, it is critical to **reduce this inductance** as much as possible.

Project Goal

Design a multi-layered power electronics package utilizing a polyimide-based substrate in order to reduce parasitic inductance, increase high-temperature reliability, and reduce time from design to prototype.

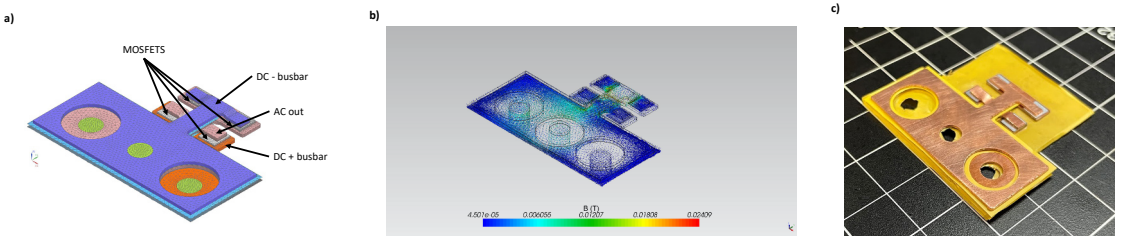
Module Design

Issues with traditional power inverter modules

- 2D layout results in energy density limitations and minimal reduction in parasitic inductance.
- Ceramic substrates are difficult to modify post-production, limiting module design possibilities, and compounded by long lead times for prototype designs.
- For higher temperature applications (>200°C), CTE mismatch will cause high strain-energy density between the ceramic and copper layers resulting in reduced package reliability.

New inverter design

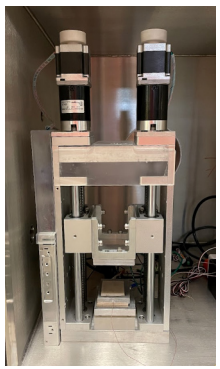
- Replacing ceramic substrate with **Dupont™ Temprion©** electrically insulating film
- Stacked module layout greatly improves energy density and reduces parasitic inductance [2] (based on simulation data)
  - Typical half-bridge module inductance: **20-25 nH**
  - Novel half-bridge module inductance: 2**.2-5.5 nH**
- Improved reliability as the compliance of Temprion© reduces the strain caused by the coefficient of thermal expansion (CTE)



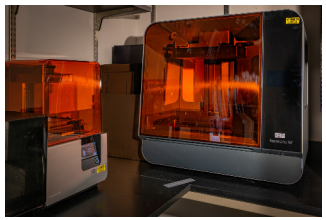
a) 3D CAD drawing of new half-bridge inverter module. b) Magnetic field simulation performed with Simcenter 3D MAGNET. c) Early prototype of polyimide-based half-bridge module.

Rapid Prototyping

Desktop CNC for creating the baseplate, busbars, and electrical traces.



Custom programable hot press



SLA 3D printers for creating cooling fluid manifolds.

Key Features

- Requires only low-cost or custom-built equipment
- No chemicals required for substrate etching
- Fabricate an entire module in less than 3 hours.

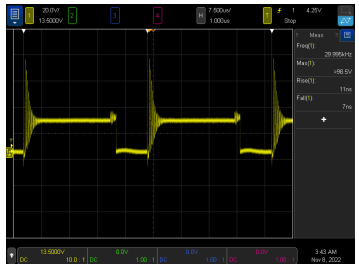
Conclusion

- Organic direct bond copper substrates, utilizing Temprion©, are allowing for next generation power module designs.
- Creating multi-layered power modules helps reduce the package parasitic inductance.
- Fabrication speed of new modules allows for rapid verification of simulation data.
- Relatively inexpensive component costs and ease of fabrication have promising potential for widespread adoption of this material and process into a variety of research areas.

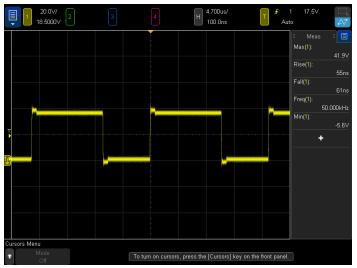
Future Work

- Further optimize the package design to further lower the parasitic inductance
- Fabricate function module once the team receives bare Silicon Carbide (SiC) devices
- Design a "soft" hot press fixture capable of applying different amounts of force along the package to allow for a single-press module fabrication
- Design package to fit the electro-magnetic and thermal management requirements of Ga_2O_3.

Effects of Package Parasitic Inductance



Drain to source overshoot and ringing caused by high parasitic inductance



Reduced drain to source overshoot and ringing achieved by lowering the inductance

- Parasitic inductance caused by rapid dI/dt causes voltage overshoot and ringing that can damage the transistor

Key Takeaways

- Increased switching speeds offered by Ga_2O_3 will require special consideration for parasitic inductance caused by device packaging
- Temprion© based substrates enable multi-layered module design, increased mechanical reliability, and fast prototyping

References

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[2] H. Gui, R. Chen, J. Niu, Z. Zhang, F. Wang, L. M. Tolbert, D. J. Costinett, B. J. Blalock, and B. B. Choi, "Design of low inductance busbar for 500 kVA three-level ANPC converter", in 2019 IEEE energy conversion congress and exposition (ECCE), ISSN: 2329-3748 (Sept. 2019), pp. 7130–7137.

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