Encapsulation Materials Tailored to Perovskite Photovoltaics

Robert Witteck,[1] Brian Habersberger,[2] E. Ashley Gaulding,[1] Joseph M. Luther,[1] and Lance M. Wheeler[1]

1 National Renewable Energy Laboratory
2 Dow Chemical Company

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Technical Report
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Final Report

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h. Report Term or Frequency	*semi-annual*	
i. Principal Investigator (PI)	*Lance M. Wheeler* *Staff Scientist* *lance.wheeler@nrel.gov* *612-424-2828*	

Major Goals and Objectives

The main objective of the proposed work is to establish a perovskite-specific thermoplastic polymer encapsulant for glass-glass modules. We hypothesize polyolefin-based chemistries can be designed to serve this purpose and will rigorously evaluate their suitability.

Impact:

The work combines NREL as the world leader in perovskite and polymeric materials, and teams them up with The Dow Chemical Company, the world leader in commercial production of PV encapsulation materials. The team will design and evaluate encapsulation materials that are tailored to perovskite photovoltaics. Demonstration of polyolefin-based encapsulants for perovskite PV will be impactful for a number of reasons: 1) There is no clear-cut choice for encapsulation for perovskite PV to date. 2) There is high synthetic control of the material properties for future perovskite module designs. 3) Among the candidate materials, they have the highest barrier properties, 4) Polyolefins are the most prevalent (>20 million metric tons consumed in the US alone) and inexpensive (<1.5 $USD/kg) polymers used worldwide. 5) They are recyclable and may play a role in future of circular PV materials. 6) They are manufactured domestically.

Description of work:

Commercialized packaging schemes will require an edge-seal/desiccant material that serves as primary protection to the outside elements (e.g. water vapor). Due to the small scale, it is challenging to encapsulate lab-scale devices (25 mmx25 mm substrates) with both an encapsulant and edge-seal while still being able to electrically test the cells. This work will

establish repeatable methods to seal the edge of a package while retaining electrical access to encapsulated cells.

We identified initial devices to work with and packaging schemes. We chose a PIN architecture due to its known stability in the literature.[1] We use a perovskite absorber layer recently developed by the Luther group (nominally $Cs_{0.17}FA_{0.83}Pb(Br_{0.17}I_{0.83})_3$) at NREL that employs a self-assembled monolayer to change the work function of ITO to form an effective hole transport material (*[4-(3,6-Dimethyl-9H-carbazol-9-yl)butyl]phosphonic Acid) (Figure 1).* The devices exhibit state-of-the-art power conversion efficiency with 21% +/-1% in typical fabrication runs.

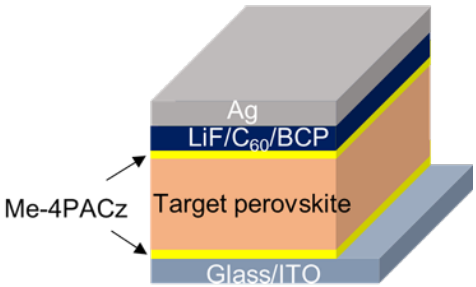


Figure 1: Perovskite device stack investigated in this quarter's work with an efficiency of 21% +/-1% power conversion efficiency. Me-4PACz = [4-(3,6-Dimethyl-9H-carbazol-9-yl)butyl]phosphonic Acid. The target perovskite used here was a triple cation, double halide composition.

We explored a number of different packaging scheme (Figure 2). PACT began with leads soldered directly to the devices and large glass-glass packages, which allow for Ca-coated substrates to be include in the package to evaluate moisture ingress. However, a more robust method has emerged called the "flip chip."[2] In this design, electrodes are evaporated onto a separate cover glass, and electrical connection is made using indium solder at the same time the package is pressed together.

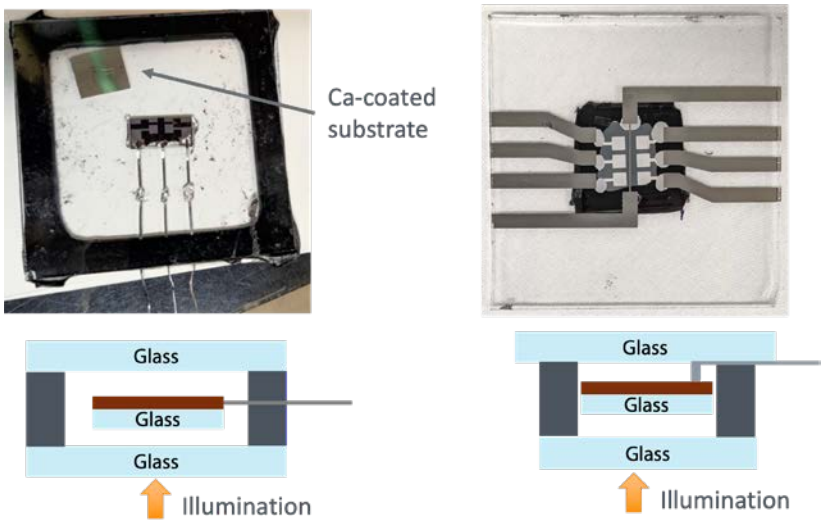


Figure 2: Photographs and accompanying diagrams of the original packaging scheme, featuring soldered leads (left) and the "flip-chip" design, which uses an indium solder connection to leads evaporated onto glass (right).

We evaluated the flip chip for performance losses. Though we were successful in repeated packaging of devices, optical losses decreased the current density of the devices (Figure 3). Though the optical losses could be accounted for in the glass absorption and two extra reflective surfaces, we sought a package that did not suffer from optical loss and was more representative of potential commercial package.

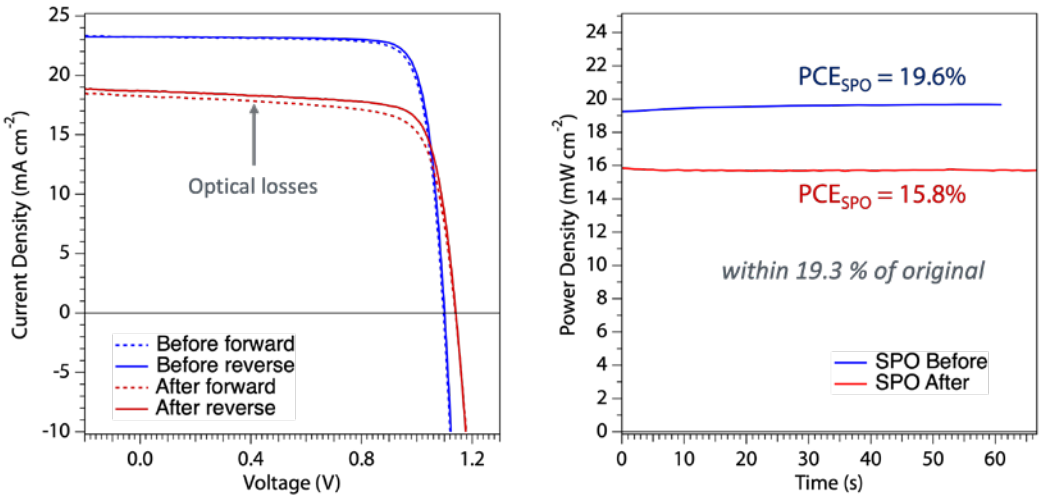


Figure 3: Current density-voltage curves for a perovskite cell before and after lamination in the flip-chip package (left) and stabilized power output the same perovskite cell before and after lamination (right).

Ashley Gaulding has worked with the team to develop a modified flip-chip package that uses the device itself as the laminating glass, much like a CdTe superstrate package (Figure 4). Devices laminated using the superstrate flip-chip avoid optical losses but still degrade during the lamination process. This will be a topic of future study and intend to switch to an ITO back contact to investigate increased durability. Regardless, the device demonstrated power conversion efficiencies based on SPO that were within 7% of the original device, nearly to the 5% metric we set in our milestones.

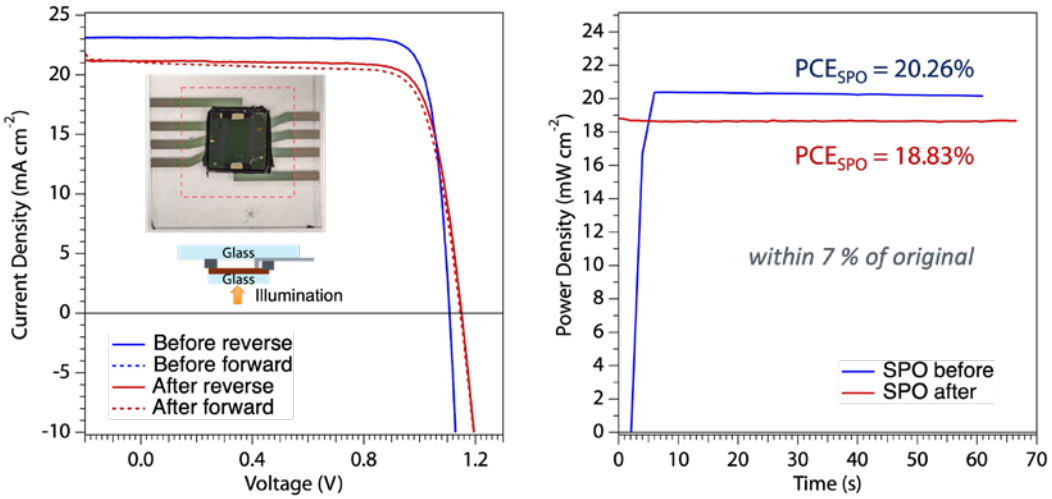


Figure 4: Current density-voltage curves for a perovskite cell before and after lamination in the superstrate flip-chip package (left) and stabilized power output the same perovskite cell before and after lamination (right). Inset shows a photograph and diagram of the superstrate flip-chip.

Vacuum lamination conditions may impact the perovskite cell performance after vacuum lamination with the polyolefin encapsulant. We study the effect of lamination temperature and time on encapsulant adhesion and degradation of the cell. We also study the chemistry of the encapsulant, which will control the melting temperature and elastic modulus. We will also study the effects of lamination conditions and encapsulant chemistry on the power output of the perovskite cell in order to establish lamination regimes where adhesion and cell performance are maximized.

Initial studies resulted in successful lamination, but the cover glass would migrate unpredictably during the vacuum lamination process and cover electrodes to prevent post-lamination measurement. We 3D printed a polyetherimide thermoplastic (PEI) mask to solve this problem. PEI was chosen for its high melting point (180 °C) and chemical compatibility to the encapsulant, which it is likely to come in contact with. Lamination with 3D printed mask prevents wandering during lamination. Vacuum lamination using the mask allowed for consistent lamination of 1-inch by 1-inch devices with access to electrodes (Figure 5).

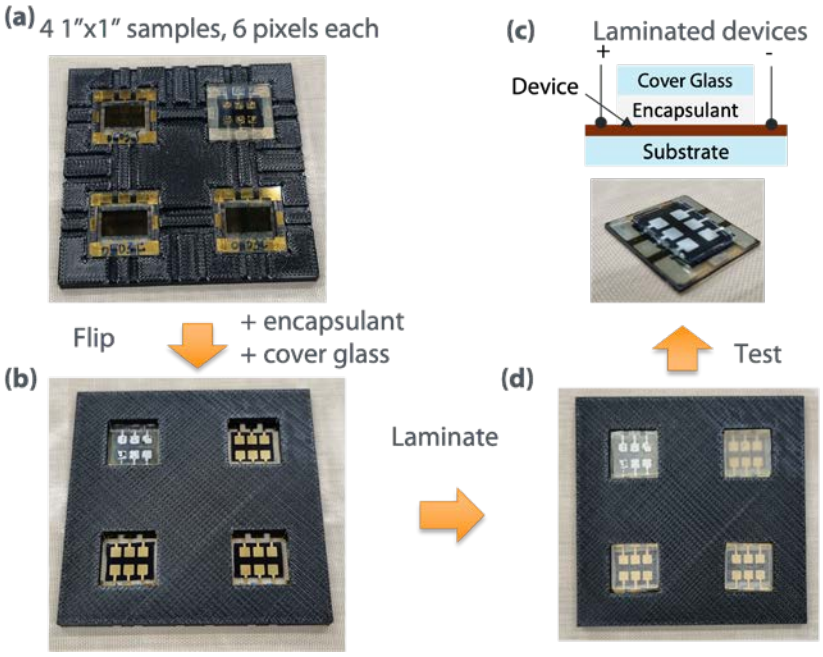


Figure 5: (a-d) Sequence of images showing mask and lamination procedure. Cells are loaded into the custom 3D-printed mask (a), the mask is flipped and encapsulant and cover glass are loaded on the opposite site (b), the device is laminated (d), and tested for current-voltage characteristics.

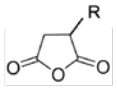
Our goal is to use the masked vacuum lamination process to determine important conditions for effective lamination. We evaluate by lamination by eye to observe any remaining air bubbles remaining in the encapsulant and measuring current-voltage scans to evaluate photovoltaic performance before and after the lamination process. With many interesting variables like lamination temperature, lamination time, lamination pressure, encapsulant mechanical properties (modulus), encapsulant glass linkage chemistry, and type of perovskite solar cell (e.g. PIN, NI, absorber composition, etc.), the parameter space is too large to do a comprehensive study. We decided on a subset that will explore what we hypothesize to be the important variables (Figure 6). Lamination pressure is held constant throughout the study, and each of the variables are explored with a few different variations. The lamination conditions are chosen to resemble current practice in Si photovoltaics with EVA and then decrease time and temperature to values that are closer to known tolerances of the perovskite cells. All laminations are carried out using a Bent River SPL 2860 laminator at NREL.

(a)

Sample Description	Film Code	Estimated Tm (C)	Estimated Modulus (MPa)
Higher crystallinity POE, silane grafted	POE-H-Si	95	20-30
Lower crystallinity POE, silane grafted	POE-L-Si	72	10-15
Higher crystallinity POE, anhydride grafted	POE-H-Ah	95	20-30
Lower crystallinity POE, anhydride grafted	POE-L-Ah	72	10-15
Conventional peroxide-cured POE	POE-L-X	72	10-15
Conventional peroxide-cured EVA	EVA-X	70	10-15

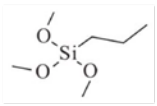
(b)

Anhydride (An)



Byproducts: H_2O

Alkoxysilane (Si)



Byproducts: ROH or H_2O

(c)

Lamination recipe	Lamination code	Time	Temp
Hot short	HS	12	150
Hot long	HL	20	150
Cool short	CS	12	120
Cool long	CL	20	120

(d)

Cell	Lamination	Film
2 replicate cells per type	HS	POE-H-Si
	HS	POE-L-Si
	HS	POE-H-Ah
	HS	POE-L-Ah
	HS	POE-L-X
	HS	EVA-X
	HL	POE-H-Si
	HL	POE-L-Si
	HL	POE-H-Ah
	HL	POE-L-Ah
	HL	POE-L-X
	HL	EVA-X
	CS	POE-H-Si
	CS	POE-L-Si
	CS	POE-H-Ah
	CS	POE-L-Ah
	CL	POE-H-Si
	CL	POE-L-Si
	CL	POE-H-Ah
	CL	POE-L-Ah

Figure 6: (a-d) Definition of sample labels. (a) Table describing definitions of different encapsulants fabricated by Dow Chemical. (b) Chemistry of linking groups and byproducts after reaction with glass (c) Table outlining codes for lamination conditions. (d) Table illustrating experimental design space.

We discovered that using lamination conditions similar to current practice in Si photovoltaics led to degradation of perovskite cells, regardless of encapsulant used. Encapsulation of perovskite cells with peroxide-cured EVA, the same material used in the Si PV industry, led to a nominal decrease in 2-3% PCE when laminating under typical conditions of 150 °C for 20 minutes. We believe the lamination conditions are the issue rather than the encapsulation chemistry itself. A similar decrease in performance is also observed for low-crystallinity POE materials that show promise under different conditions. For PIN perovskite devices, the results are intuitive: perovskites are known to degrade under high-temperature conditions. The hot and long process irreversibly damages the cells. Though the short-circuit current is relatively unchanged, degradation of perovskite interfaces is suggested by reduced open-circuit voltage, increased hysteresis, and increased series resistance (Figure 7).

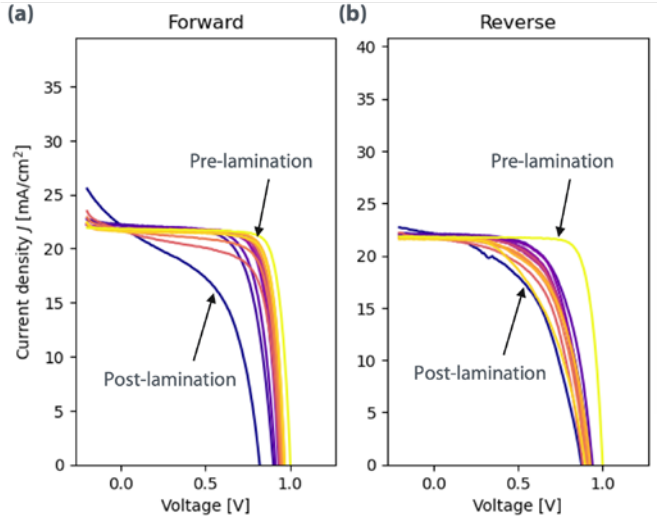


Figure 7: Forward (a) and reverse (b) current-voltage sweeps of PIN perovskite solar cells before and after lamination with low-crystallinity POE with alkylsilane linkage chemistry using 150 °C for 20 minutes.

Peroxide-cured EVA requires 150 °C for linkage chemistry to occur. However, the custom POE materials designed by Dow include alkylsilane or anhydride chemistries, which will undergo sufficient glass interface reactions at 120 °C, which allows us to decrease the lamination conditions while still achieving a strong bond between the perovskite cell and the glass coversheet.

We used PIN perovskite devices for the current study. Future work will also include NIP devices. Intuitively, cooler temperatures (120 °C) and shorter vacuum lamination times (12 minutes) were beneficial for photovoltaic performance. Compared to the control sample (exposed to air during the same times the laminated samples are), perovskite cells that were laminated at 120 °C instead of 150 °C showed less degradation. Similarly, shorter treatment times of 12 minutes instead of 20 minutes maintained better performance. For instance, when held a same temperature (120 °C) the sample held at that temperature for a shorter time maintained better performance (Figure 8, CS = cool, short, CL = cool, long).

There was a smaller dependance on POE crystallinity (modulus). POE-L-Si-CS is the lower modulus material compared to POE-H-Si-CS. Both were evaluated under the same lamination conditions. POE-L-Si-CS showed slightly better performance compared to the control, but there were a small fraction of cells in the POE-H-Si-CS group that also showed nearly no degradation. In fact, the SPO scans show nearly no change after cool, short lamination conditions for both low- and high-crystallinity POE. Future work will expand these findings to POE materials with anhydride linkage chemistry and different perovskite device architectures that have varied amounts of methyammonium and NIP or PIN interfaces.

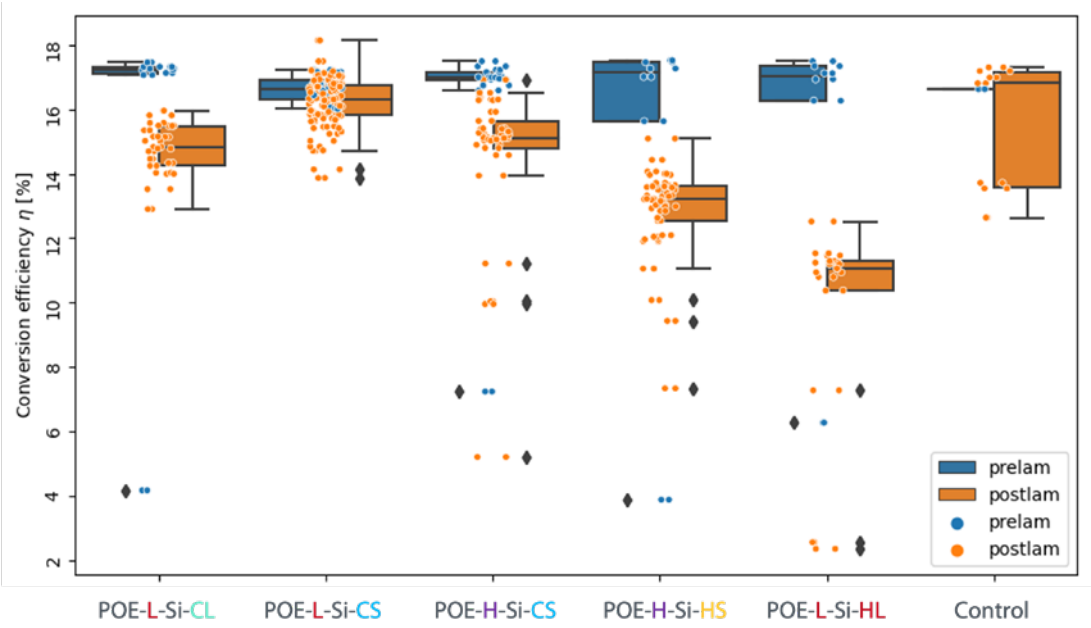


Figure 8: Power conversion efficiency (PCE) as a function of vacuum lamination condition. Lamination condition codes refer to figure 6. All studies were done on PIN perovskite devices with POE functionalized with alkylsilane. Black diamonds refer to outliers.

There were setbacks in the fabrication of NIP devices. The first setback was the solar simulator was down for ~1 month, which delayed device production and characterization for many NREL projects. Subsequent efforts to fabricate NIP devices resulted in PCE<17%, which is stipulated in the TWP. PCE>17% is a necessary metric to ensure we are investigating devices that are relevant for commercialization. We believe it is SPIRO-OMeTAD that is the issue, and we will continue to troubleshoot. We believe we can fabricate NIP devices with PCE>17% for studies in the coming months.

After discussion with SETO during the FY22Q4 quarterly meeting, we decided to focus on PIN devices. We have continued evaluation of POEs with anhydride-based coupling groups (Figure 9). Both sets of devices encapsulated with anhydride-grafted POEs exhibited significant change in performance after lamination. Devices laminated with cold (120 °C, POE-L-Ah-CS) and hot (150 °C, POE-L-Ah-HS) conditions decrease PCE from ~20% to ~10%. It is a similar result to peroxide-cured POE (POE-L-X-HL) and peroxide-cured EVA, which require 150 °C conditions for cross-linking reactions occur. Control devices are carried along during the lamination and measuring process to expose them to the same conditions as the laminated devices except for the actual lamination process (i.e. air exposure, room lights, change in temperature, vacuum for glovebox transfer, etc.).

Perhaps the most interesting observation from these experiments is that devices tend to recover after dropping in efficiency after lamination (Figure 9). When left in a dark, inert (N_2) environment for 1 to 3 days, the perovskite devices recover significantly. Samples that were laminated using 150 °C, regardless of anneal time (codes HS or HL), do not recover to their prelaminated performance. The peroxide-cured encapsulated devices (POE-L-X-HL and EVA-L-X-HL) recover to ~15%, recovering roughly half of what they lost immediately after lamination.

Impressively, the anhydride-grafted, low-crystallinity POE encapsulated device (POE-L-Ah-CS) fully recovers within error of the measurement to return to the initial PCE = 18%.

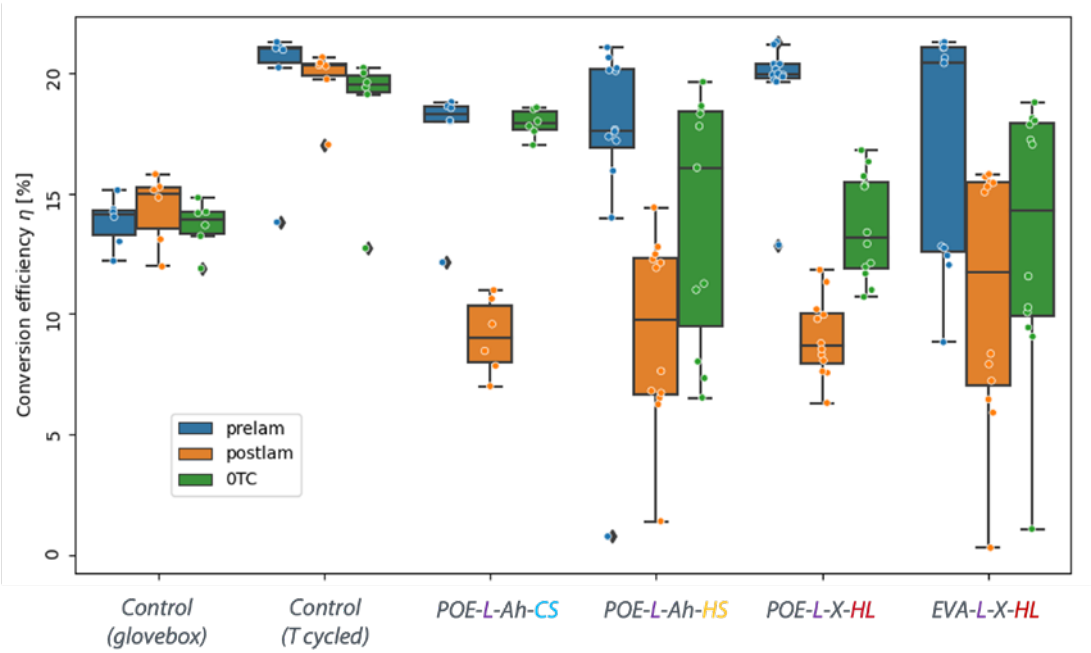


Figure 9: Power conversion efficiency (PCE) as a function of vacuum lamination condition. Lamination condition codes refer to figure 6. All studies were done on PIN perovskite devices. Blue samples are before lamination. Orange samples are after lamination. Green samples characterized before thermal cycling after being stored in a dark inert environment for 1 to 3 days. 0TC = 0 thermal cycles. Black diamonds refer to outliers.

We have begun initial studies to determine the leading cause of device degradation using electroluminescence (EL) and photoluminescence (PL) experiments (Figure 10). In addition to current-voltage studies, EL and PL uniquely allow us to non-destructively evaluate devices after lamination. Our initial results give us confidence that this will be a powerful technique for future studies evaluating thermally cycled samples and those evaluated with fully-packaged damp-heat testing (IEC 61215:2016).

The effects of laminating conditions used here have a clear impact on the luminescent properties of the perovskite devices. Whereas control devices that have not seen lamination conditions exhibit uniform emission under low and high current injection (EL) and illumination (PL), devices that were laminated exhibit significant spatial variation in the emission, which is a clear indication of degradation.

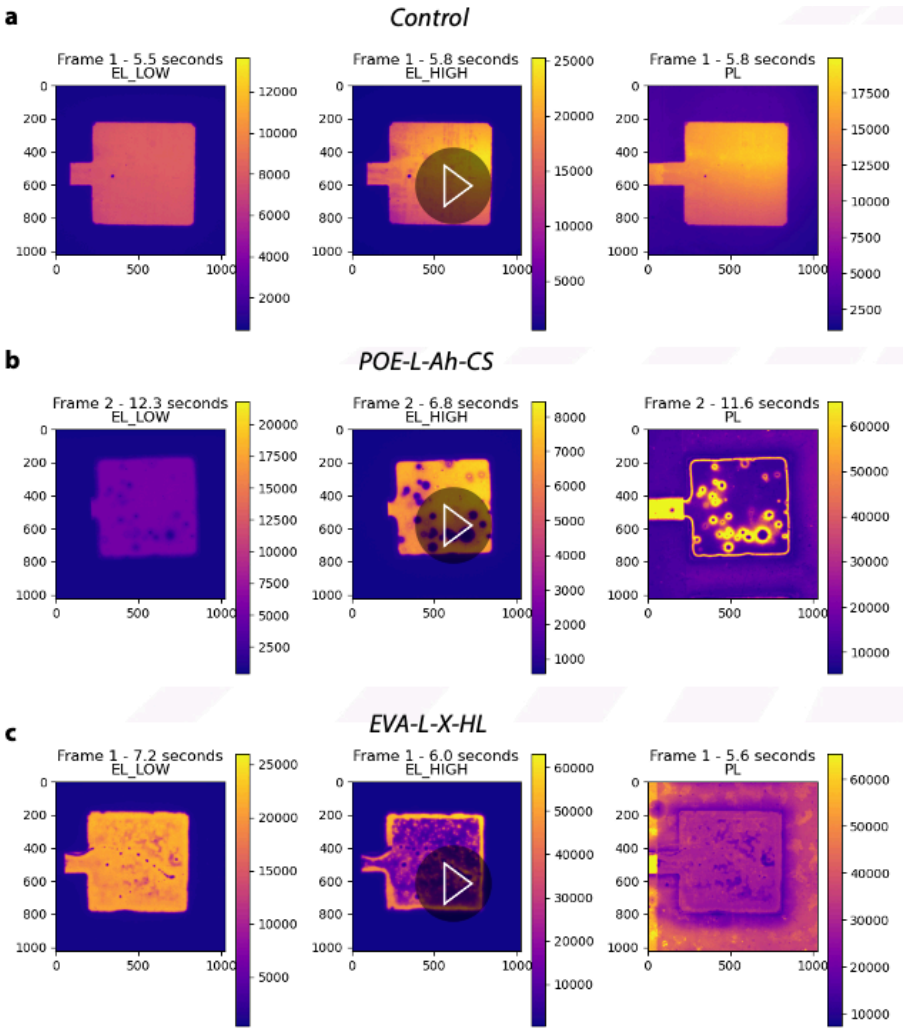


Figure 10: (a-c) Electroluminescence (EL) and photoluminescence (PL) experiments. Left column of images are EL at low injection level, center column of images are EL at high injection level, and right column of images are PL. Each image shown here is a snapshot of a movie that captures kinetics of the emissive behavior for the unencapsulated control sample (a), POE-L-Ah-CS (b), and EVA-L-X-HL (c).

We hypothesize the degradation either occurs within the perovskite film or at a perovskite interface. To test this hypothesis, we fabricated devices with different HTL materials under constant lamination conditions (125°C for 12 min) (Figure 11). The SAM-modified ITO HTL performed the best. 2PACz, MeO-2PACz, and a 50/50 blend of 2PACz and MeO-2PACz each maintained their PCE after lamination within error. The cells with the PTAA HTL show the highest loss in efficiency after lamination, with a median efficiency loss of 23%$_{rel}$. It is unclear if the recovery observed in previous devices will also appear in the PTAA devices.

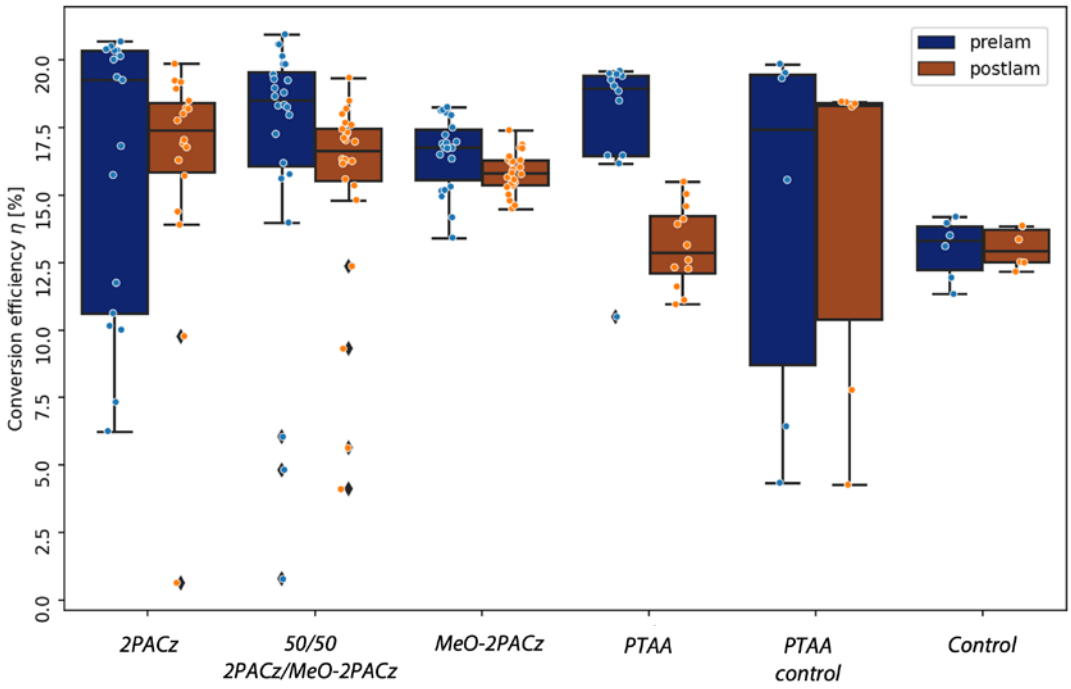


Figure 11: Power conversion efficiency (PCE) as a function of HTL material for constant vacuum lamination conditions (12 minutes at 125 °C). studies were done on PIN perovskite devices with POE functionalized with alkylsilane. Black diamonds refer to outliers.

The last two quarters of research were dedicated to evaluating the chemical compatibility of encapsulants and device durability under thermal stress in an anaerobic environment and in a hot and humid environment when fully packaged (encapsulant combined with edge seal).

We performed thermal cycling analysis of PIN perovskite devices by placing laminated samples into a chamber cycling between -40 °C and 85 °C under an N_2 atmosphere. We use N_2 atmosphere to decouple any effects due to moisture or oxygen ingress. Initial data has validated our initial hypothesis going into the project that lower Young's modulus would lead to good mechanical stability under thermal stress testing. Previous work from the McGehee group shows polyolefin encapsulants from different manufacturers produced different results that roughly correlated to lower Young's modulus as an important property.[1] Materials with higher modulus (>30 MPa) led to delamination under thermal cycling. In our work, we observe no delamination after 100 cycles between -40 °C and 85 °C. Each of the materials from Dow were designed to have a modulus <30 MPa.

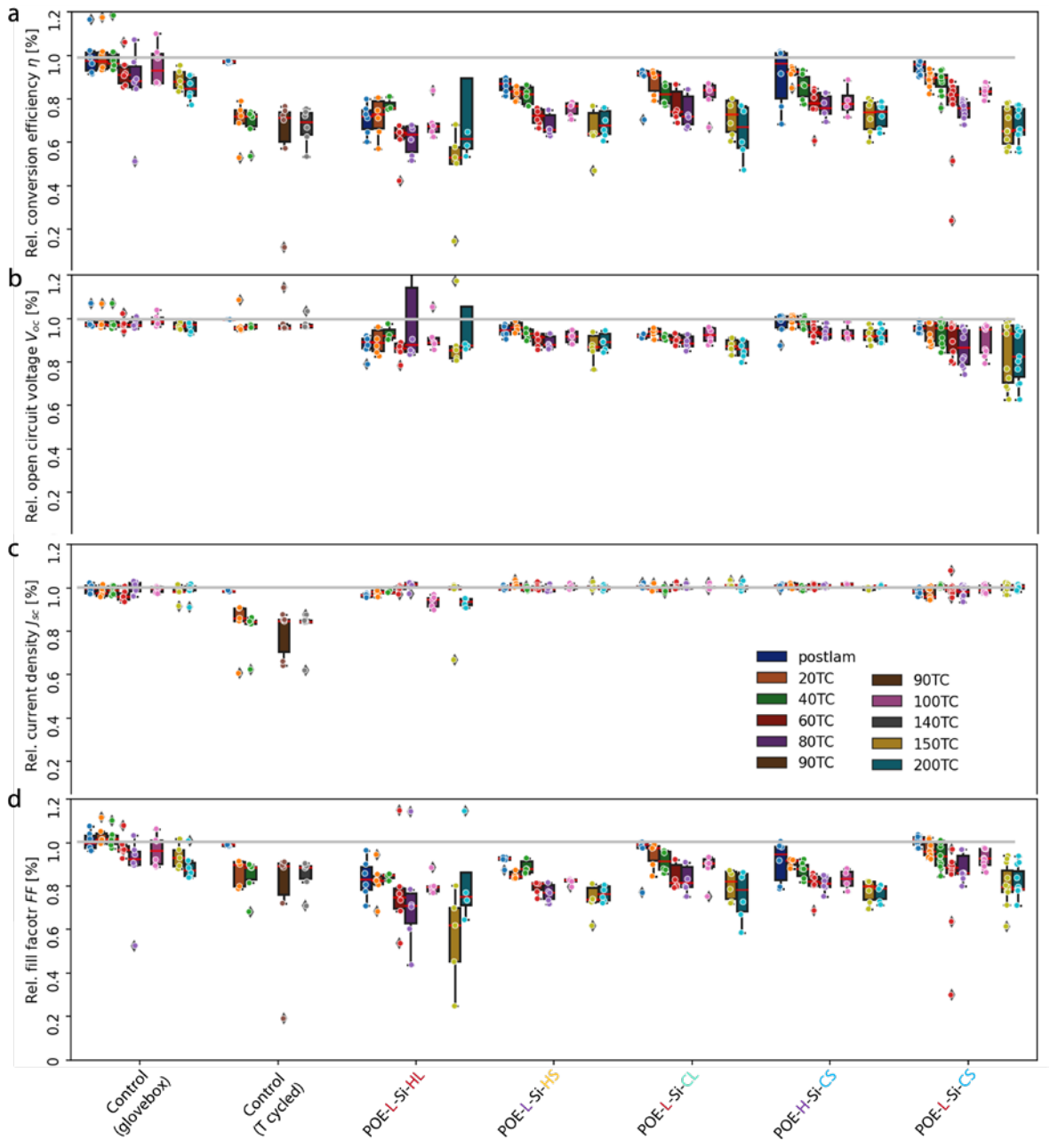


Figure 12: a-d) Power conversion efficiency (PCE) (a), open circuit voltage (b), short circuit current density (c), and fill factor (d) as a function of number of thermal cycles between -40 °C and 85 °C. Sample codes refer to figure 6. All studies were done on PIN perovskite devices with either anhydride grafted POE or peroxide-cured encapsulants. Black diamonds refer to outliers. TC = thermal cycle. Gray line is a guide to the eye at 1.

We completed 200 thermal cycles on the perovskite devices. Perovskite PV devices decrease in PCE as a function of cycle (Figure 12). Each silane-grafted POE-encapsulated perovskite device showed similar behavior. There was a monotonic decrease in PCE through 80 thermal cycles. Of the different encapsulants POE-L-Si-CS showed the smallest decrease, staying within error of the

initial lamination. The same encapsulant (low crystallinity) processed under hot and long conditions showed a decrease from 15% to 12% after 80 thermal cycles. After 100 thermal cycles, each of the device sets showed an increase in PCE, which was an unexpected result. We determined this is because of a longer delay before measurement, allowing the perovskite device to "recover." The mechanism is still unknown.

The remaining 2 measurements at 150 and 200 cycles show a decrease in performance across all encapsulants and encapsulation conditions. Even the control sample that was not temperature cycled and kept in a glovebox did not maintain its original performance. Similarly, the control device that was thermal cycled without encapsulant showed degradation that is similar to the best encapsulated devices (those processed at 120 C for 12 min in the laminator).

We observe degradation in all scenarios. For all encapsulated devices, the main contribution to decreased power conversion efficiency is a decrease in fill factor. Voc and Jsc remain relatively unchanged. Interestingly, the control sample that also shows a decrease in Jsc in addition to the fill factor. Perhaps the encapsulation prevented a mode of degradation.

Because the thermal cycling experiment was performed under inert conditions, we conclude the degradation is not due to exposure to moisture or O_2. The degradation must be due to delamination due to internal stresses in the device or due to an internal degradation mode within the device. Both hypotheses point to issues within the device stack rather than an interaction with the encapsulant. Though discouraging for demonstrating a stable packaged device, we can say the encapsulant did not have further detriment to device performance.

Degradation of our control devices have led us to reevaluate hypotheses that we introduced previously. Our original hypothesis was that the linking chemistry of the encapsulant was the culprit of degradation, either by bonding to the back contact and lifting the layer off or releasing H_2O or MeOH byproducts into the device stack. Dow sent us an encapsulant without linking chemistry included to test this hypothesis. We found devices laminated without the linking chemistry behave the same as the devices laminated with the linking chemistry, indicating it is likely not the byproducts of chemical linking that is at fault here.

We have pivoted to determining which mode of degradation that is introduced during thermal cycling: delamination, internal chemical degradation, or both. We have begun initial studies on distinguishing the different modes. To look for delamination, we have identified C-mode scanning acoustic microscopy (C-SAM) (Figure 13) as particularly promising.[3]

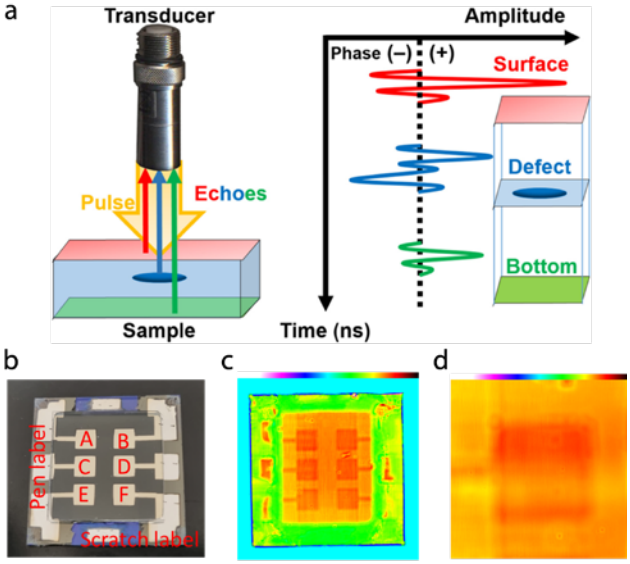


Figure 13: (a) Diagram of C-mode scanning acoustic microscopy (C-SAM) setup and expected signals from a sample. Adapted from ref. 3. (b) Optical photograph of a 6-pixel perovskite device with each pixel labeled (A-F). (c) *A C-SAM image of a 6-pixel perovskite device. (d) A C-SAM image of a pixel "A"of the same device shown in (c).*

C-SAM is a non-destructive imaging technique that is sensitive to imperfections, especially voids, within a stack of materials. The working principle of the technique is based on the reflection that acoustic waves experience at media interfaces and density irregularities. The technique makes use of the high penetration depth of acoustic waves, in comparison to light, to image the internal structure of the specimen. C-SAM is routinely used for quality control, inspection and failure analysis in microelectronics components and materials, which is routinely used for the inspection of plastic encapsulated integrated circuits amongst other systems. Here, we are applying it to an encapsulated perovskite PV for the first time.

Our goal is to correlate optical probes (EL, PL, Figure 10) to the acoustic probe to begin parsing between delamination and chemical degradation modes. C-SAM should highlight delamination. After some effort, we have been able to obtain images of the packaged perovskite devices using C-SAM, though they are devices that we would not expect to find the degradation features observed in EL/PL. However, we conclude the C-SAM may be a valuable tool in the non-destructive evaluation of perovskite devices. Future work will include measurements of samples that have shown degradation in the EL/PL signals.

In parallel to C-SAM measurements, we have performed further analysis on device J-V curves, which suggest an internal chemical mode of degradation is likely. We fit J-V curves to a diode model to extract resistance properties. Though, saturation current density, sheet resistance, and diode ideality show no trends, the mean change in current density and sheet resistance tend to be reduced after lamination (Figure 14). It is similar to the the J-V trend shown in Figure 7. The decrease in shunt resistance is likely not a symptom of delamination, as forcing current to travel further through the absorber or transport layer should instead result in increased series resistance.

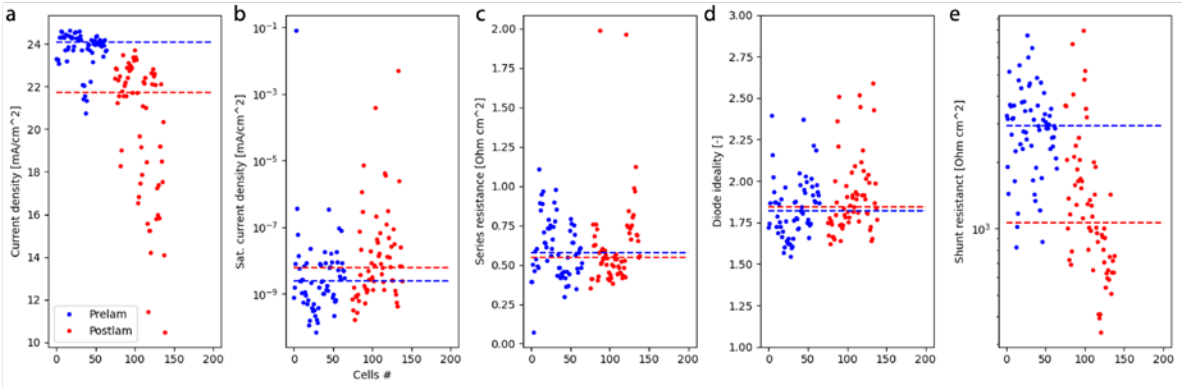


Figure 14: a-d) Short circuit current density (a), Saturation current density (b), sheet resistance (c), diode ideality (d), and fill factor (e) for a large sampling of devices investigated in this study. All studies were done on PIN perovskite devices. Dashed lines are the mean value for pre- (blue) and post-lamination (red)

In addition to any delamination effects, we hypothesize the decrease in shunt resistance is due to diffusion of silver from the back electrode into the device. The phenomenon has been shown in the literature[4]. In order to test this hypothesis, we fabricated devices with SnO_x layers that serve as both and electron transport layer and an internal diffusion barrier. SnO_x replaces the BCP layer in the stack we have been using. There is clear evidence from photoluminescence that the SnO_x barrier layer is effective at mitigating the mode of degradation we observe in the

BCP samples. Whereas dark (non-luminescent) spots form in devices with BCP (Figure 15a), the samples laminated with the SnO_x show no dark-spot behavior (Figure 15b).

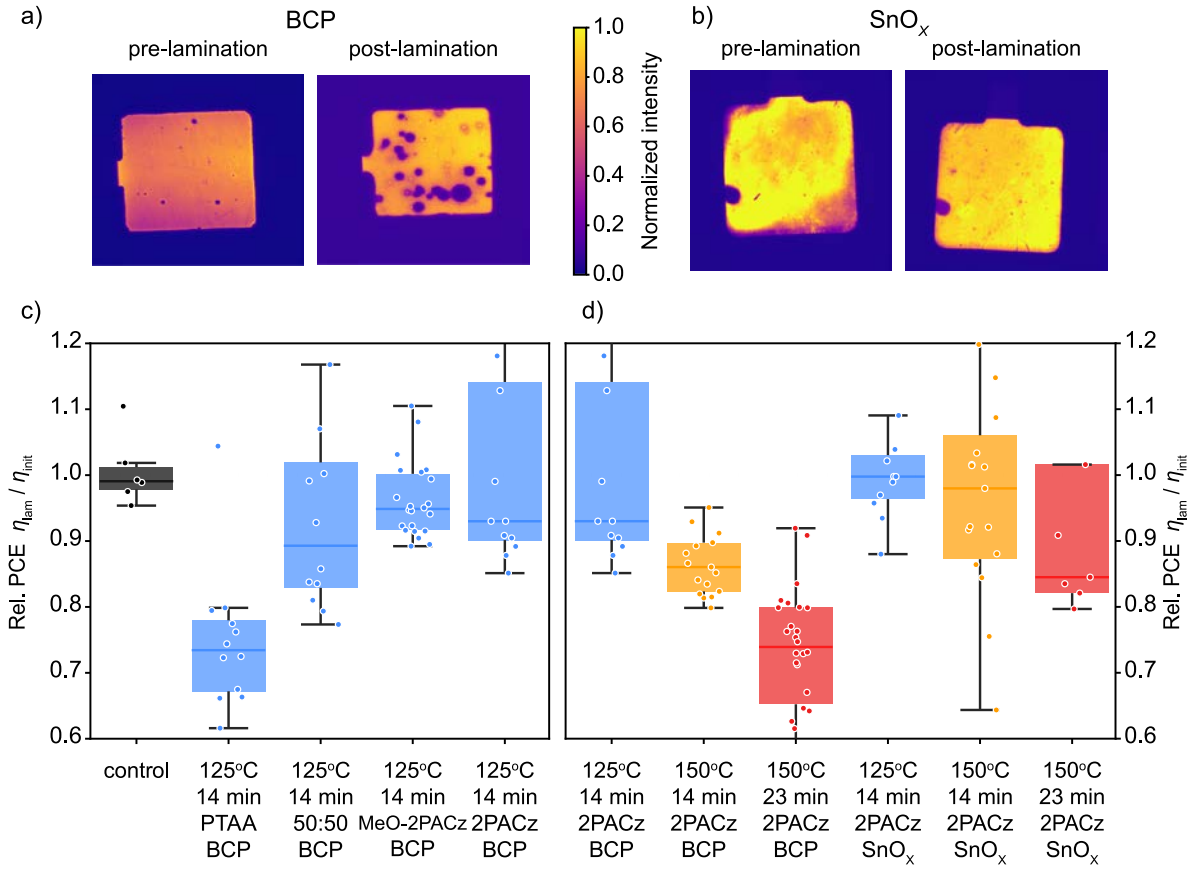


Figure 15: Electroluminescence images at short-circuit conditions of devices pre- and post-lamination with the 150°C/14 min process using different buffer layers of a) BCP or b) SnO_X. Bottom: Relative change in power conversion efficiency (PCE) before and after lamination for devices with c) varying hole transport layer (HTL) and d) buffer layer (BL) laminated with the 125°C/14 min, 150°C/14 min, and 150°C/23 min process.

Devices fabricated with BCP as the barrier layer must have a self-assembled monolayer in order to survive lamination. PTAA degraded to 75% of what it started at when laminated at even low temperatures (125 C, Figure 15c). Devices with SnO_x layers instead of BCP show significantly less degradation after lamination. Whereas BCP devices decrease by 10% and 25% on average after lamination at 150 C for 14 and 23 minutes, respectively, devices with SnO_x show no significant degradation after 14 minutes and 85% degradation on average after 23 min. Within the set of samples, a subset retains 100% of the original PCE even after 23 min (Figure 15d).

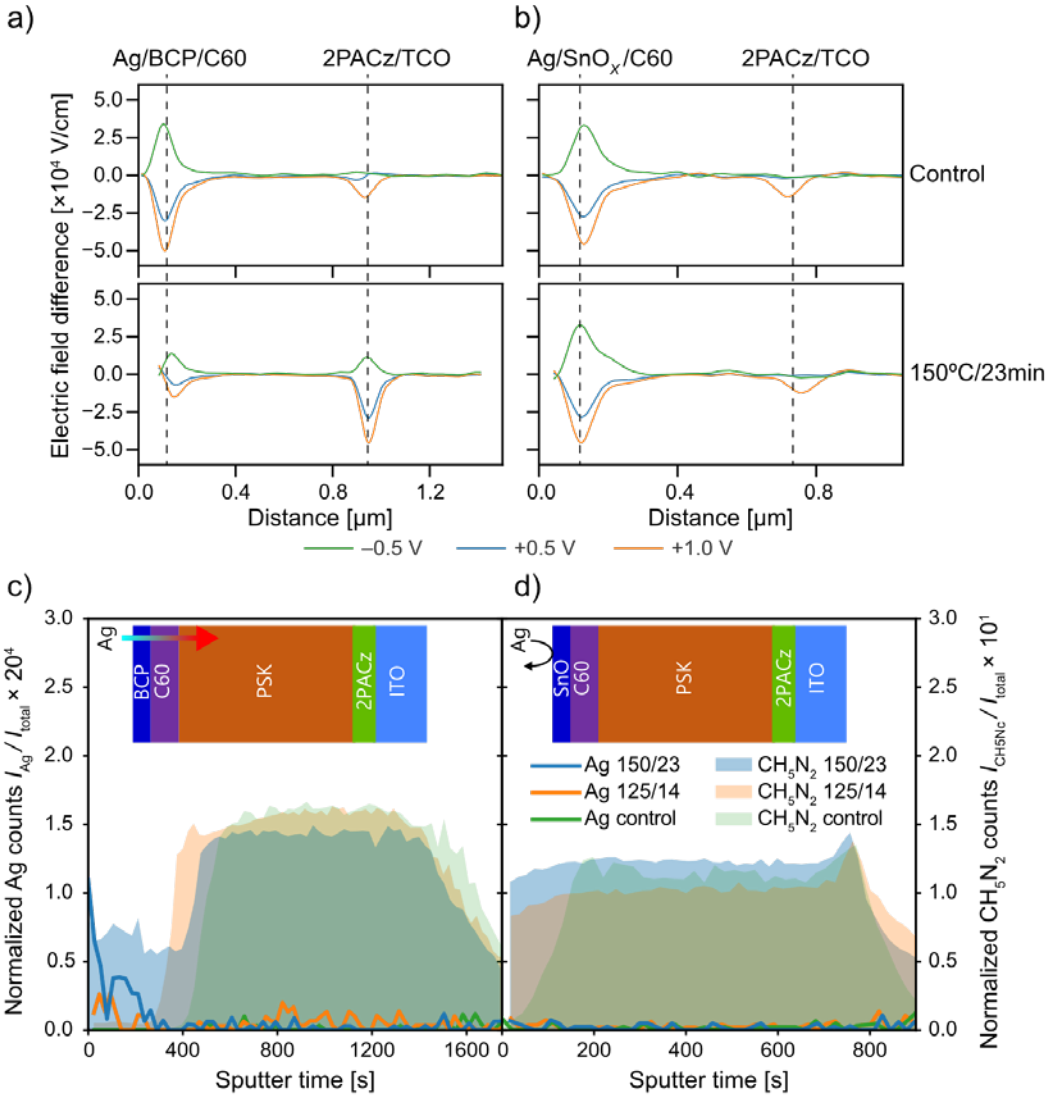


Figure 16: Electric field difference derived from Cross-sectional Kelvin probe force microscopy (cKPFM) measurements of non-laminated control devices and devices laminated with the 150°C/23 min process, incorporating either BCP in a) or SnO_X in b) as buffer layers. Bottom: Depth profiles of Ag and CH_5N_2 from time-of-flight secondary ion mass spectrometry (ToF-SIMS) measurements for devices using BCP in c) or SnO_X in d) as buffer layers. Each profile compares non-laminated control devices to those laminated with the 125°C/14 min and 150°C/23 min processes.

We investigate mechanisms of degradation by correlating cross-sectional cKPFM to observe changes in the device operation with TOF-SIMS chemical analysis. Figure 16a shows the electric field difference (EFD) derived from cKPFM measurements of a non-laminated control device and a device laminated with the 150°C/23 min process, incorporating BCP as buffer layer. Figure 16b shows the same measurements for devices with SnO_X as BL. All samples utilize 2PACz as HTL. For the cKPFM measurements we a apply a bias voltage of -0.5 V, 0.0 V, 0.5 V, and 1.0 V.

The non-laminated control sample with BCP BL in Figure 16a shows an increased amplitude in the EFD signal at the ETL interface relative to the HTL interface. This higher amplitude in the EFD signal suggests either an elevated equivalent resistance at the ETL interface or enhanced

conductance at the HTL interface. However, for the device laminated at 150°C/23 min with a BCP buffer layer, a notable reversal occurs in the EFD signal intensity, which is now higher at the HTL interface compared to the ETL interface. The electric field drops more at the HTL interface, suggesting either an increased equivalent resistance at the HTL interface or enhanced conductance at the ETL interface after the lamination process.

Comparing the measurements of the control device and the device laminated with the 150°C/23 min process with the SnO_X BL in Fig. 17b shows only marginal differences in the EFD signal indicating that the interface is unaffected by the lamination process.

16c shows the depth profiles of the Ag and the CH_5N_2 species from ToF-SIMS measurements on devices with BCP as buffer layers, comparing non-laminated control devices to those laminated with the 125°C/14 min and 150°C/23 min processes. Figure 3d shows shows the same measurements for devices featuring an SnO_X BL. All samples utilize 2PACz as HTL. The CH_5N_2 signal identifies the perovskite bulk. In Fig. 16c we notice an increase in Ag signal at the ETL interface for the samples with BCP buffer layer. The amount of Ag increases with increasing temperature and duration in the lamination process. In contrast, for the samples with SnO_X as BL in Fig. 16d we observe no Ag signal at the ETL side and across the sample. Another observation in Fig. 16c and 16d is that the CH_5N_2 signal becomes more dispersed as the temperature and duration in the lamination process increases, which we interpret as ion migration into the transport layers.

Table 1: Parameters for the drift-diffusion simulations

Parameter	Initial	Degraded	Unit
Temperature	298	298	K
device thickness	5.00E-07	5.00E-07	m
PSK relative dielectric constant	24	24	
PSK conduction band edge	3.82	3.82	eV
PSK valence band edge	5.44	5.44	eV
PSK DOS of conduction and valence bands	3.1E+24	3.1E+24	m^-3
PSK ionised n-doping	0	0	m^-3
PSK ionised p-doping	0	0	m^-3
TCO thickness	1.10E-07	1.10E-07	m
Metal contact thickness	2.00E-07	2.00E-07	m
Electron zero field mobility	6.00E-04	1.93E-04	m^2/Vs
Hole zero field mobility	8.00E-04	3.00E-06	m^2/Vs
Field-dependent electron mobility	0	0	0 : const. mob
Field-dependent hole mobility	0	0	0 : const. mob
Electron field dependence of mob Poole-Frenkel form	0	0	(m/V)^0.5
Hole field dependence of mob Poole-Frenkel form	0	0	(m/V)^0.5
Work function ETL contact	3.85	3.85	eV
Work function HTL contact	5.38	5.38	eV
surface recombination of electrons at ETL contact	1.00E+05	1.00E+05	m/s
surface recombination of holes at ETL contact	1.00E-06	1.00E-06	m/s
surface recombination of electrons at HTL contact	1.00E-05	1.00E-05	m/s
surface recombination of holes at HTL contact	1.00E+05	1.00E+05	m/s

Parameter	Initial	Degraded	Unit
shunt resistance	inf	inf	Ohm m^2
series resistance	0	0	Ohm m^2
thickness ETL layer	2.00E-08	2.00E-08	m
thickness HTL layer	3.00E-08	3.00E-08	m
DOS of ETL layer	5E+25	5E+25	m^-3
DOS of HTL layer	5E+25	5E+25	m^-3
doping in ETL layer	-1E+22	-1.00E+23	m^-3
doping in HTL layer	1E+22	1E+22	m^-3
mobility of ETL layer	5.00E-05	5.00E-05	m2/Vs
mobility of HTL layer	5.00E-05	5.00E-05	m2/Vs
interface transfer velocity ETL layer	1.00E+03	1.00E+03	m/s
interface transfer velocity HTL layer	1.00E+03	1.00E+03	m/s
relative dielectric constant ETL layer	5	4	-
relative dielectric constant HTL layer	15	3	-
conduction band ETL layer	3.82	3.82	eV
conduction band HTL layer	2.21	2.21	eV
valence band ETL layer	6.21	6.21	eV
valence band HTL layer	5.38	5.38	eV
TLs generate electrons/hole	No	No	-
traps in TLs	No	No	-
can ions move into the TLs?	No	Yes	-
concentration of anions	1.0E+21	2.0E+23	m^-3
concentration of cations	1E+21	1.4E+23	m^-3
mobility of anions	5E-11	5E-11	m^2/Vs
mobility of cations	7E-13	7E-13	m^2/Vs
charge separation distance Braun model used	1.00E-09	1.00E-09	m
distribution of a: 1 for delta function 2 for Gaussian	2	2	-
decay rate	1.00E+06	1.00E+06	1/s
direct (band-to-band bimolecular) recombination rate	1.6E-17	1.6E-17	m3/s
Langevin recombination prefactor	1	1	-
trap density (in bulk)	5.04E+20	5.04E+20	m^-3
ETL interface trap density	1E+14	1E+14	m^-2
HTL interface trap density	1.00E+10	1.00E+10	m^-2
number of grain boundaries	0	0	-
grain boundary trap density per grain boundary	1E+13	1E+13	m^-2
capture coefficient for electrons	2E-13	2E-13	m^3/s
capture coefficient for holes	6.77E-14	6.77E-14	m^3/s
energy level of all traps	4.91	4.91	eV
Trap type for the ETL interface*	-1	-1	-
Trap type for the HTL interface*	1	1	-
Trap type for the bulk and grain boundary*	-1	-1	-

*-1: acceptor, 0: neutral, 1: donor

We perform drift-diffusion modeling to enhance our understanding of the degradation mechanisms occurring during the vacuum encapsulation of the PSC. We employ SimSalabim to qualitatively remodel the effect of the vacuum lamination on the *JV* measurements and EFD from the cKPFM measurements. An overview of the modeling parameter is listed in Table 1. It is important to emphasize that the drift-diffusion simulations employ the identical voltage ramp used for the *JV* measurement, as this parameter can influence the observed hysteresis behavior. 17 shows the comparison between measured and simulated *JV* characteristics and EFD. All measurements are for a device with 2PACz as HTL and BCP as ETL buffer layer. 17a shows the *JV* measurement of a device before and after undergoing lamination with the 150°C/23 min process. Figure 17b shows the corresponding qualitative simulation using the drift-diffusion model. Both the measurement and the simulation reveal no noticeable hysteresis in the initial *JV* characteristics. After the lamination the measurement reveals a strong inverted hysteresis, i.e. the *JV* characteristic measured in forward direction exhibits a higher efficiency than in the reverse direction. The same effect is reproduced in the drift-diffusion simulations.

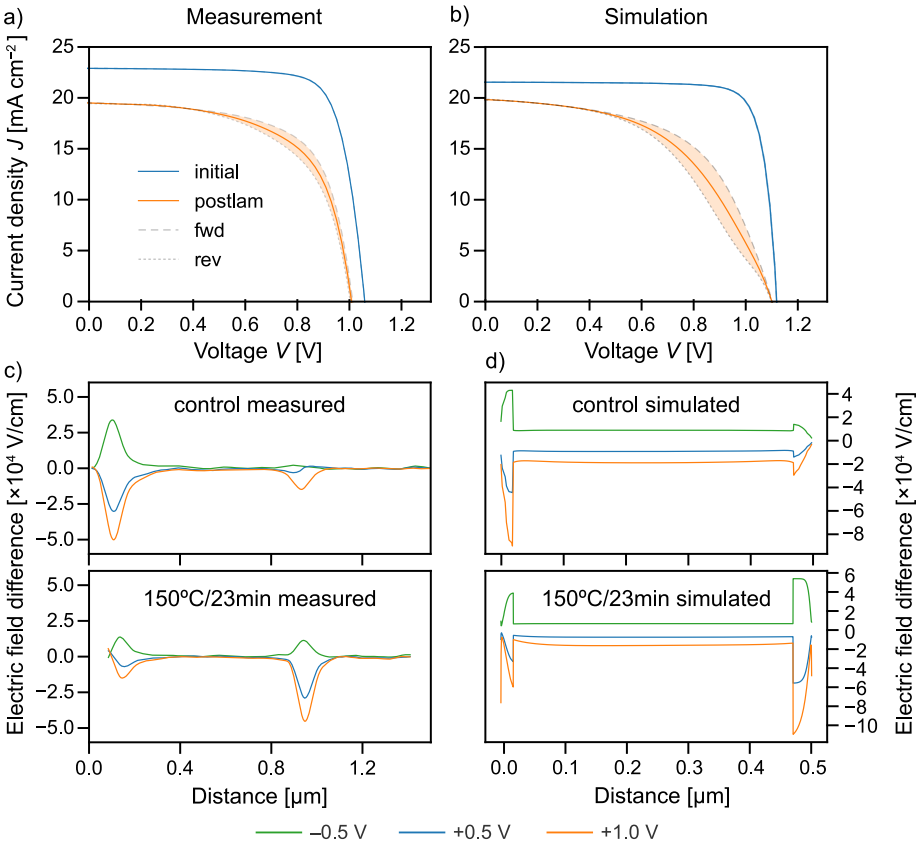


Figure 17: Comparison of measurement and drift-diffusion simulation results. All measurements are for a device with 2PACz as HTL and BCP as buffer layer. a) Measured JV characteristics before and after lamination with the 150°C/23 min process and b) corresponding drift-diffusion model results. c) Electric field difference (EFD) from cKPFM measurements of a non-laminated control and a device laminated with the 150°C/23 min process. d) shows the qualitative drift-diffusion model results.

17c shows the electric field difference (EFD) extracted from the cKPFM measurements of an unlaminated control device and a device laminated with the 150°C/23 min lamination process. 17d shows the corresponding results from the drift-diffusion simulations. Both measurements and simulations reveal a higher amplitude in EFD signal at the ETL interface for the non-laminated device. After lamination the higher amplitude shifts to the HTL interface, which is consistently reproduced in the drift-diffusion simulation. Given the qualitative agreement between measurements and simulations, we can draw conclusions on how the lamination process results in a degradation of the PSC performance.
We realize the modeling of the device degradation during the lamination by varying the following parameters (Figure 18):

1. Increasing the mobile anion and cation density.
2. Allow ions to move into the transport layers.
3. Reducing the mobility of the hole minority charge carriers in the perovskite bulk.
4. Increasing the doping density and decreasing the relative permittivity of the ETL.

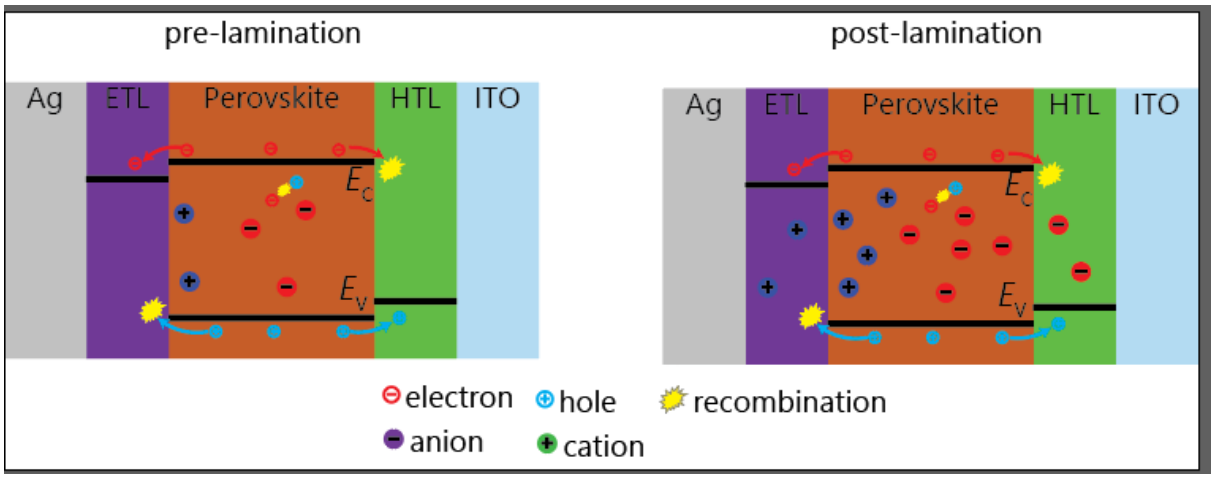


Figure 18: Illustration of mechanisms that lead to changes in pre- and post-lamination current-voltage characteristics based on drift-diffusion modeling.

The rationale for increasing the mobile ion densities is that a higher temperature and duration of lamination process leads to the generation of more mobile ions, a hypothesis that aligns with findings reported in the literature (*30*). This thermal process also facilitates ion migration into the transport layers, which is a crucial assumption for replicating the inverted hysteresis in the simulations and aligns with our observations in the ToF-SIMS measurements. The reduction of the minority charge carrier mobilities is associated to Ag migration into the perovskite. The presence of Ag in the bulk results in an n-type doping of the perovskite (*25*), thereby reducing the hole mobility. The enhanced doping density and decreased permittivity of the ETL stem from replicating the enhanced conductivity of the ETL due to the Ag infiltration. This observation is presumably not reflecting the actual material properties of the ETL but rather arises from reproducing the hysteresis and EFD changes. However, it is important to acknowledge that a decrease in the doping levels of the HTL, which could also account for the observed EFD signals, does not reproduce the observed inverted hysteresis behavior. Further, the penetrating

Ag forming a conductive path through the ETL and the perovskite could be an explanation for the localized shunt formation evident in the luminescent images.

Project Conclusions

We started our work with the hypothesis that the encapsulant chemistry will be critical for achieving durable perovskite devices. We found that the vacuum lamination process resulted in degradation of the perovskite, regardless of the encapsulant chemistry. We htus sought to understand and remedy this effect.

Our investigations into the effects of vacuum lamination on perovskite solar cells (PSCs) reveal that the temperature and duration of the lamination process significantly impacts the PSC performance. Specifically, we observe that a higher process temperature and duration correlates with an increased performance loss, with the 150°C/23 min lamination condition exhibiting the most substantial decrease in PCE, primarily due to reductions in J_{SC} and *FF*. Conversely, V_{OC} is less affected, suggesting that lamination primarily impacts the interfaces between the perovskite and transport layers rather than the perovskite bulk itself. For degraded devices our experiments also highlight a change in hysteresis behavior from normal to inverted hysteresis after lamination, supporting the notion that interface changes are responsible for the post-lamination degradation. Notably, the choice of encapsulation polymer seems to have minimal impact on device performance, possibly since for our tested devices, the perovskite is insulated from direct polymer contact. Future studies with direct contact between perovskite and lamination polymer, e.g. in the scribe lines, must be carried out to verify this hypothesis.

Based on the variations observed in the HTL, our findings indicate that self-assembled monolayers such as 2PACz or MeO-2PACz offer advantages over PTAA. However, it's important to highlight that our study did not include an examination of NiO_X. Given the superior thermal stability of NiO_X, it might offer comparable stability benefits.

The most important finding seems to be that BCP as a buffer layer is less suitable than SnO_X for improving the lamination stability of PSC. Besides *JV* characterization, EL imaging confirms the superior durability of devices with SnO_X buffer layers, demonstrating minimal degradation even under lamination at 150°C. This resilience, combined with observed stability improvements when employing 2PACz or MeO-2PACz as HTL, suggests a pathway to enhancing PSC durability towards processes employed in established PV manufacturing technologies.

After further investigating the underlying degradation mechanism through cKPFM and ToF-SIMS measurements, we hypothesize that SnO_X serves as a more effective diffusion barrier against silver migration than BCP. This finding is further elucidated through drift-diffusion modeling. Our simulations qualitatively reproduce our measurement result, highlighting the role of ion migration and metal in diffusion in PSC performance degradation.

In conclusion, our comprehensive study bridges the gap in understanding the complex interplay between lamination conditions, material choices, and the subsequent effects on PSC stability and performance. It offers valuable insights for refining encapsulation techniques to seamlessly integrate perovskite tandem solar cells within the current photovoltaic production framework and for enhancing the long-term reliability of PSCs under outdoor operation.

The work will result in one paper funded solely by the project and multiple others that were supplemented by work funded in the tandem program and through TEAMUP.

References:

(1) *Cheacharoen, R.; C. Boyd, C.; F. Burkhard, G.; Leijtens, T.; A. Raiford, J.; A. Bush, K.; F. Bent, S.; D. McGehee, M. Encapsulating Perovskite Solar Cells to Withstand Damp Heat and Thermal Cycling. Sustainable Energy & Fuels* ***2018****, 2 (11), 2398–2406. https://doi.org/10.1039/C8SE00250A.*

(2) *Gaulding, E. A.; Louks, A. E.; Yang, M.; Tirawat, R.; Wilson, M. J.; Shaw, L. K.; Silverman, T. J.; Luther, J. M.; Palmstrom, A. F.; Berry, J. J.; Reese, M. O. Package Development for Reliability Testing of Perovskites. ACS Energy Lett.* ***2022****, 2641–2645. https://doi.org/10.1021/acsenergylett.2c01168.*

(3) *Yu, H. Scanning Acoustic Microscopy for Material Evaluation. Applied Microscopy* ***2020****, 50 (1), 25. https://doi.org/10.1186/s42649-020-00045-4.*

(4) *Li, J.; Dong, Q.; Li, N.; Wang, L. Direct Evidence of Ion Diffusion for the Silver-Electrode-Induced Thermal Degradation of Inverted Perovskite Solar Cells. Advanced Energy Materials* ***2017****, 7 (14), 1602922. https://doi.org/10.1002/aenm.201602922.*