Passivated Contacts for Direct Wafer Product: Final Technical Report

David L. Young

National Renewable Energy Laboratory

NREL is a national laboratory of the U.S. Department of Energy
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Technical Report
NREL/TP-5900-91109
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Final Technical Report (FTR)

Cover Page

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h. *Certifying Official (if different from the PI or BC)*	Name Title Email address Phone number	

Signature of Certifying Official *Date*

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3. Executive Summary:

This TCF project developed a thin-oxide (SiO_2)/polycrystalline silicon (poly-Si) passivated contact solar cell on CubicPV's (formally 1366 Technologies, Inc.) Direct Wafer® Product (DWP) kerfless wafers. The project used two NREL-developed technologies described in U.S. Patent No. 9,911,873, *Hydrogenation of Passivated Contacts* and U.S. Patent Application Serial No. 15/890,172, *Doped Passivated Contacts*. The project was motivated by a potential higher efficiency cell (compared to a PERC cell) using passivated contacts on the ultra-low cost kerfless wafers grown using the Direct Wafer process. The hope was to accelerate market adoption of the cell and wafer by delivering the lowest LCOE in the PV industry.

The project tested both n-type and p-type SiO_2/poly-Si passivated contacts grown by thermal oxidation and plasma enhanced chemical vapor deposition (PECVD) of the poly-Si layer on DWP with varying wafer resistivities. Both deposition techniques are industry standards and thus economically viable methods for commercializing the contacts. The results indicated that both n-type and p-type poly-Si passivated contacts can be formed on polycrystalline DWP wafers, but implied open-circuit voltages (iV_{oc}) were limited to below 0.65 mV (compared with ~ 730 mV on n-Cz wafers). Diffusion of H to the Si/SiO_2/poly-Si interface was key to obtaining high iV_{oc} values. In this study, H was diffused from a high-temperature SiN_x layer deposited over the poly-Si layer during a high-temperature firing step, similar to one used for screen-printed metals. The study concluded that poly-Si passivated contacts on DWP wafers passivated the surface of the wafers as well as PERC passivated surfaces, which use a less expensive dielectric layer stack.

The project showed that Direct Wafer Product wafers grown by CubicPV could produce high iV_{oc} values (~0.647 mV), which could produce a cell over 20% efficient with proper processing and metallization. These cells, though not economically viable in 2024 as a stand-alone cell, could be integrated with a wide-bandgap top

solar cell to form a two-junction tandem cell that could be viable under certain circumstances. This is because the bottom cell of a 30%, two-terminal tandem only needs to be a 20% cell under one-sun conditions. Thus, the DWP could be an ideal low-cost wafer for tandems. The project also revealed that a TOPCon type cell could be formed on a p-type DWP wafer using a P-diffused emitter and a p-type poly-Si contact. In fact, the p-type version of the poly-Si contact out-performed the n-type version for a variety of wafer resistivities, from highly doped to lowly doped. This curiosity requires more work to understand because on Cz wafers, the n-type poly-Si contact is of much higher quality than the p-type version.

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- Background
- Project Objectives
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- Path Forward
- Products
- Project Team and Roles
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5. Background:

High-temperature SiO_2/poly-Si passivated contacts are the main driver for the PV industry moving from a PERC cell architecture to a TOPCon architecture.[1] The key improvements are moving from a p-type wafer to an n-type, high-lifetime wafer, and replacing the aluminum back-surface-field point contacts and dielectric passivation scheme of the PERC cell to a full-area SiO_2/poly-Si contact. This significantly lowers the recombination at the back contact and, along with the higher bulk wafer lifetime, raises the V_{oc}, and hence the efficiency of the cell. Some studies have tried a reverse polarity of the TOPcon architecture using p-type monocrystalline wafers.[2] These studies generally show a lower passivation quality than on n-type wafers, but still with respectable iV_{oc} values of ~0.68 V and importantly, the iFF can be as high as ~84.5% for 1 Ohm-cm and 10 Ohm-cm wafers.[2] Mack *et al.* reported a 21.2% efficiency p-type TOPcon device,[3] and the company Longi demonstrated a >25% efficient p-TOPcon cell in 2021.[4] Schindler *et al.* showed a 19.9% efficient multicrystalline n-TOPcon device using a so-called high-performance multicrystalline wafer.[5] CubicPV developed a process to form kerfless multicrystalline wafers directly from a molten bath of silicon. CubicPV calls these wafers "Direct Wafer® Product" (DWP). These wafers have relatively high lifetimes and give efficiencies of 20.5% for a PERC cell architecture using low-resistivity doping. Their high-resistivity wafers have shown lifetimes as high as 1 ms. The one-dimensional current flow of a TOPCon cell (full area back contact) might allow this cell architecture to work well on the high-resistivity, high-lifetime wafers.

6. **Project Objectives:** This project explored forming SiO_2/poly-Si contacts on DWP to make both a p-TOPCon and an all-passivated contact cell. Our objective was to raise the efficiency potential for CubicPV's low-cost DWP wafers. If successful, the new cell designs would lower the LCOE for photovoltaic installations and make the DWP cells a prime candidate for a bottom cell of a two-junction tandem. Table 1 shows the technical tasks and milestones for the project. We first established how to passivate the bulk of the DWP wafers while simultaneously forming and passivating the new contacts. Our milestone was to reach 500 µs bulk lifetime at 1E14 cm^{-3} injection level. Next, we developed n-type and p-type passivated contacts on DWP wafers with milestones of $J_o < 30$ fA/cm^2

Table 1. Tasks and Milestones Gantt Chart

Task	Technical Plan and Milestones	Project Months			SUBTASKS DESCRIPTION	ACCOUNTABILITY
		6	12	18		
Task 1	Advanced bulk and surface passivation of Direct Wafers					
1.1	Update Sinton Lifetime tester calibration for high-resistivity wafers				NREL will have their Sinton Lifetime tester recalibrated for high-resisitivity wafers by a technician from Sinton Instruments.	NREL
1.2	Perform round-robin tests with DWs to ensure calibrated Sinton Lifetime testers at CubicPV Inc and NREL				Perform round-robin tests with DWs to ensure calibrated PCD tools at CubicPV Inc and NREL. NREL PI will ensure that lifetime curves are within 10% of each other between the NREL and CubicPV Inc tools.	CubicPV Inc, NREL
1.3	Measure baseline photoconductive decay(T) and DLTS on DWs to obtain injection-level lifetimes and determine lifetime-limiting defect(s)				Performing defect level characterizations to determine the source of this low injection character of the high-resistivity wafers .	NREL
1.4	Develop advanced passivation process steps for DWs (dielectric growth, anneals, firing steps)				NREL will apply their advanced passivation process steps on DW wafers that have been gettered with CubicPV Inc's phosphorus diffusion/etch-back process.	CubicPV Inc, NREL
	*MILESTONE 1-1-1: Tau effective > 500 µs @ 2E14 cm^-3					
Task 2	Passivated contacts on Direct Wafers					
2.1	Develop p-type passivated contacts on high and low resistivity p-Cz wafers				NREL will provide the wafers, processing and characterization	NREL
2.2	Develop p-type passivated contacts on high resistivity p-DWs				CubicPV Inc will provide phosphorus-gettered p-type DW wafers to NREL. NREL will deposit p-type passivated contacts and measure them.	CubicPV Inc, NREL
2.3	Quantify passivation as a function of grain orientation and in grain boundaries				Use samples from Task 2.2 and have NREL characterization team measure grain orientation by EBSD. Couple results with PL imaging maps.	NREL
	*Milestone 1-2-1: p-type poly-Si/SiO2 contact on DWs (Jo < 30 fA/cm^2, ρcontact < 30 mohm-cm^2)				CubicPV Inc will provide phosphorus-gettered p-type DW wafers to NREL. NREL will deposit p-type passivated contacts and measure them.	CubicPV Inc
Task 3	Passivated contact device on Direct Wafers					
3.1	Develop n-type Si:P emitter on high resistivity DWs (Jo < 130 fA/cm2 and 100-120 Ohms/sq)				CubicPV Inc will provide phosphorus-gettered p-type DW wafers to NREL. NREL and CubicPV Inc will diffuse phosphorus into wafers to form an emitters on the wafers. It is expected that this work will be done at both CubicPV Inc and at NREL labs with knowledge shared between teams.	CubicPV Inc
3.2	Develop compatible processing for front emitter diffusion and rear p-type passivated contacts on DWs				Wafers from Task 3.1 will be used by NREL to develop p-type passivated contacts on one side.	NREL
3.3	Develop compatible metallization process for p-TOPcon on DWs				Metallization will be done at NREL	NREL
3.4	Model device results to perform energy-loss analysis				Modeling will be done at CubicPV Inc start with their current Quokka3 PERC model. Similar modeling will be done at NREL as well.	CubicPV Inc, NREL
	*Milestone 2-3-1: N-type Emitter Rear Passivated Contact cell (P-TOPcon) on Direct Wafers (Eff >20% (4 cm^2))				CubicPV Inc and NREL will work together to accomplish this goal using wafers and knowledged gained from Task 3	CubicPV Inc, NREL
	*Stretch Milestone 2-3-2: N-type Emitter Rear Passivated Contact cell (P-TOPcon) on Direct Wafers (Eff>19% (243 cm^2))				CubicPV Inc and NREL will work together to accomplish this goal using wafers and knowledged gained from Task 3	CubicPV Inc, NREL
Task 4	CRADA final Report				The final report will be written by the NREL PI with input and approval from CubicPV Inc	CubicPV Inc, NREL

and $\rho_{contact} < 30$ mOhm-cm^2. Finally, we developed cells using these contacts with a goal of >20% efficiency over a 4 cm^2 area.

7. **Project Results and Discussion:** Referring to Table 1, Task 1 mainly developed process and measurement protocols for DWP wafers. DWP wafers are unique in many ways compared to standard monocrystalline Cz wafers. Cz wafers have typical saw damage removed chemically etched surfaces or (111) pyramid morphologies, whereas DWP wafers have relatively rough surfaces with randomly oriented grain morphologies. The DWP surfaces required process development to properly clean, grow films on them, and passivate both the bulk and the surface. Additionally, this project was interested in developing cells on high-resistivity wafers because of their higher lifetimes compared with low resistivity wafers. However, to measure minority carrier lifetimes via photoconductance decay (PCD), one must specifically design and calibrate the detection coil for high-resistivity wafers. Task 1.1 required NREL to update calibrations on their Sinton Lifetime testers, and Task 1.2 performed a round robin of samples to ensure that NREL and CubicPV were in agreement on lifetime data. Figure 1 shows a sampling of lifetime as a function of minority carrier density (MCD) data associated with this task. First, the dashed data is from the PCD tool at CubicPV. Second, the bold solid line data are from the

NREL-calibrated PCD tool. Most of the data agrees between the two tools. There may have been some change in the samples as they were shipped between the labs for these measurements. Figure 1 includes data from an uncalibrated PCD tool (thin, solid lines) to illustrate how important calibration of the tool is to these high-resistivity wafers.

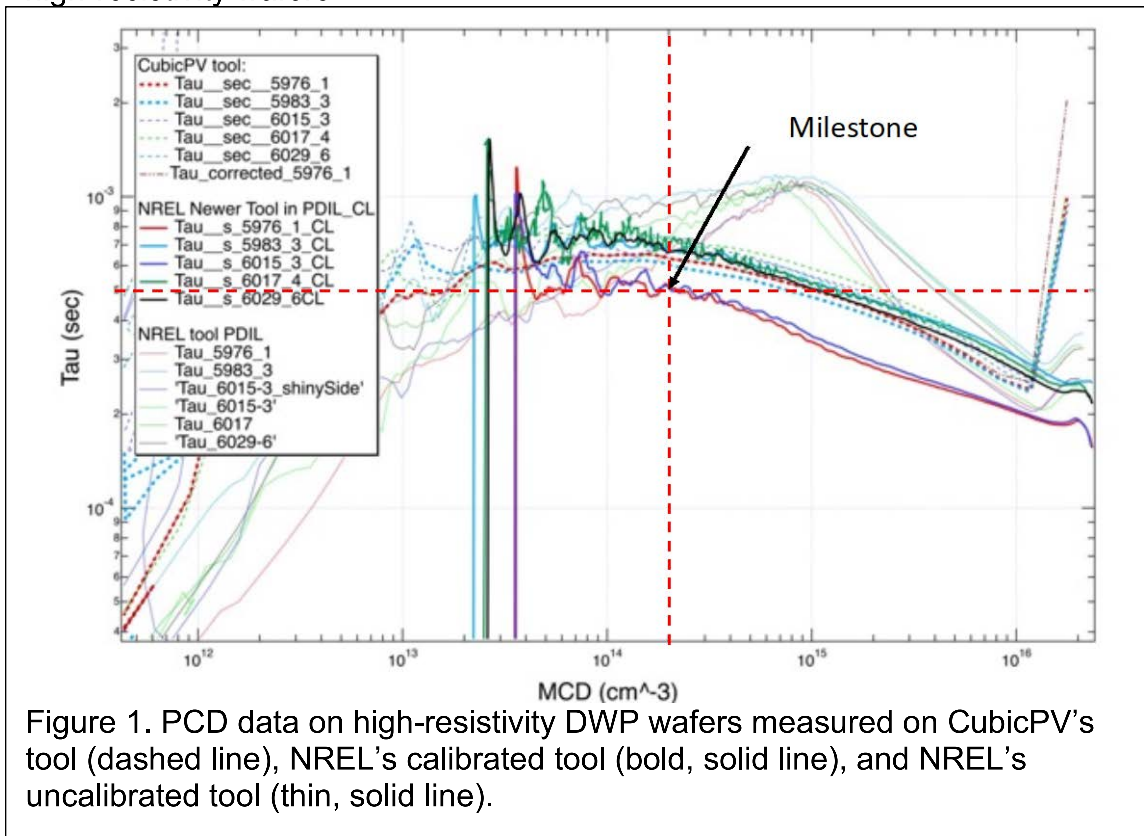

Figure 1. PCD data on high-resistivity DWP wafers measured on CubicPV's tool (dashed line), NREL's calibrated tool (bold, solid line), and NREL's uncalibrated tool (thin, solid line).

Task 1.3 was descoped from this project, as it was determined that CubicPV had already completed a similar study with another partner and would not significantly help our milestones for this project.

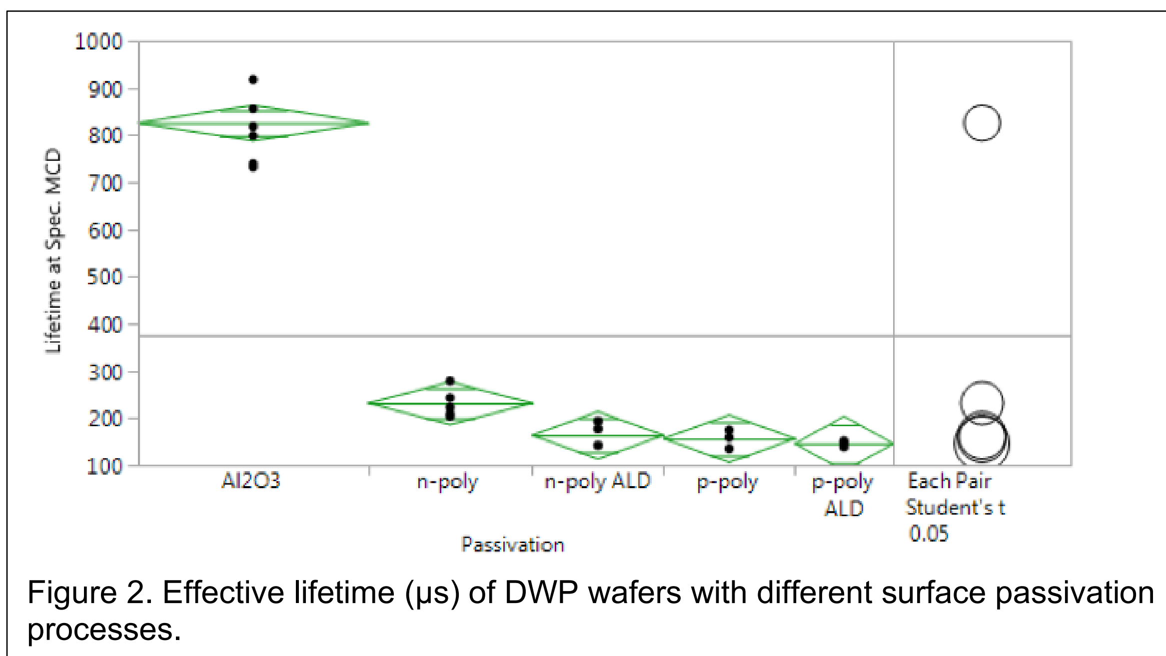

Figure 2. Effective lifetime (μs) of DWP wafers with different surface passivation processes.

Task 1.4 explored different passivation material and processes unique to DWP wafers. Monocrystalline Cz wafers typically do not need passivation of bulk defects to maintain high lifetimes. Usually, when adding a passivation layer or treatment to the surface of Cz wafer, only the surface defects need to be passivated. However, DWP wafers require both passivation of the bulk and the surface defects to achieve high, useful lifetimes. Importantly, the bulk and the surfaces can be passivated with hydrogen (H). H can be diffused into the wafer and to the surface by depositing a hydrogen-containing dielectric layer on the wafer and then annealing the wafer to drive the H into the wafer. Typical annealing temperatures for surface defects are around 400 ˚C. For bulk defects, the temperature needs to be above ~700 ˚C to diffuse the H from the surface to the bulk defect. Surface defects can be passivated with lower annealing temperatures of 400 ˚C when a H-containing dielectric layer provides an "infinite" H reservoir. Significantly, de-passivation of the bulk defects can occur if the temperature is raised above ~600 ˚C without a significant H reservoir layer. Presumably, the higher (700 ˚C) anneal is needed to diffuse H to the bulk defect, but only ~600 ˚C is needed to bond/de-bond the H to the defect. The result is that passivating the bulk and surface needs to be done simultaneously with a single, high-temperature firing step in the presence of a H source. This proved to be challenging for this project as neither lab (CubicPV nor NREL) had the tools to grow passivated contacts and fireable dielectric layers, and to fire the samples. This resulted in samples being shipped multiple times between labs to complete the experiments, as will be explained below in Task 2.

Figure 2 shows effective lifetimes (in μs) by PCD for several different surface passivation processes, illustrating the need to passivate both bulk and surface defects. All samples in Figure 2 underwent a bulk H passivation process (SiN_x film covering both surfaces of the wafer, fired at ~750 ˚C, then the SiN_x film was etched

away) at CubicPV before sending to NREL. NREL then performed standard n-Cz processing on the wafers to passivate the surfaces. The samples marked "Al_2O_3" received an ALD coating of Al_2O_3 and then were annealed in forming gas at ~400 ˚C for 30 mins. As discussed above, this lower temperature anneal in the presence of an infinite H reservoir (Al_2O_3) passivated the surface of the DWP wafer and, importantly, did not de-passivate the bulk defects. The result is a high effective lifetime of ~ 800 μs. However, for samples marked n-poly or p-poly in Figure 2, the bulk passivation was lost during the higher temperature processing steps. For example, the n-poly and p-poly samples were subjected to a high-temperature (~700 ˚C) anneal in an oxygen environment to grow a tunneling oxide. Next, the samples were loaded into a PECVD deposition chamber to grow a ~50 nm thick layer of doped a-Si over the tunneling oxide. Finally, the samples were loaded into a diffusion furnace and annealed at ~850 ˚C for 30 mins to crystallize the a-Si into poly-Si and to diffuse dopants into the wafer surface. Samples marked "n-poly ALD" and "p-poly ALD" were given an additional Al_2O_3 layer over the poly-Si and annealed in FGA for 30 mins at 400 ˚C. As can be seen from the lifetime data, none of the samples processed with the high-temperature poly-Si steps achieved high lifetimes. Presumably, the higher processing temperatures de-passivated the bulk defects which then dominated the recombination in the wafer, swamping any surface passivation benefit the SiO_2/poly-Si treatment may have provided. Note: the processing steps used to form SiO_2/poly-Si contacts would have resulted in > 1 ms lifetimes for n-Cz wafers. Thus, this early experiment in Task 1 revealed that DWP wafers require a different process flow to form passivated contacts while preserving the bulk passivation. Task 2 addressed this challenge by using a single, high-temperature firing step to passivate both the bulk and the surface of the DWP wafers. Milestone 1-1-1 was completed with the data of Figures 1 and 2.

Task 2 focused on developing a process path to form passivated contacts on DWP wafers. Figure 3 shows three DWP wafers that underwent the following processing: 1) POCl diffusion (~850 ˚C) on both sides of the wafer, followed by a wet chemical etch to remove impurities (gettering); 2) a H-rich SiN_x layer deposited on both sides; 3) a firing step to quickly take the sample to ~ 700 ˚C and then return it to room temperature in 10s of seconds (this added H to the bulk of the wafer); 4) chemical stripping of the fired SiN_x layer; 5) growth of SiO_2 by thermal oxidation (~700 ˚C) [note: bulk H was removed during this step]; 6) growth of poly-Si by PECVD and a high-temperature anneal (850 ˚C) [Note: bulk H was removed during this step]; 7) addition of a SiN_x layer; and finally, 8) fire the wafer in a belt-furnace or an RTA furnace (~700 ˚C) [Note: this added H to both the bulk defects and surface poly-Si/SiO_2 layers. Note that steps 5 and 6 were performed at NREL, while the rest of the steps were done at CubicPV. This was necessitated by neither lab having all the tools necessary to complete all of the processing steps.

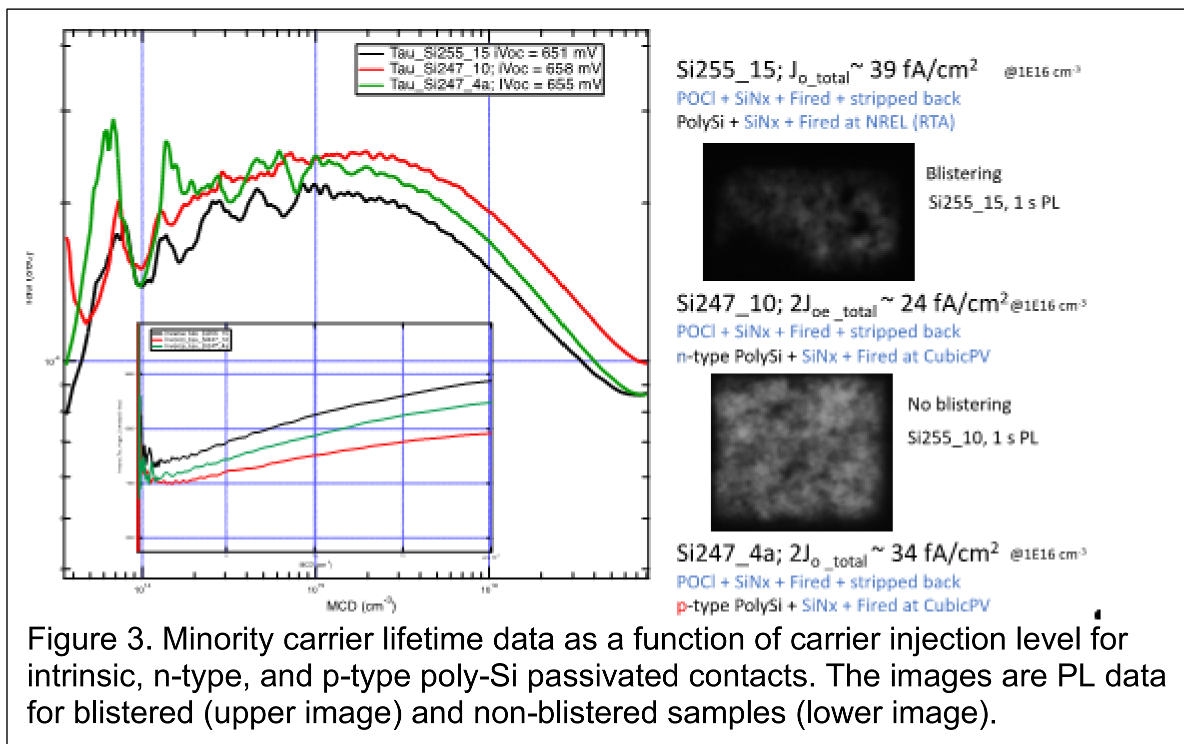

Figure 3. Minority carrier lifetime data as a function of carrier injection level for intrinsic, n-type, and p-type poly-Si passivated contacts. The images are PL data for blistered (upper image) and non-blistered samples (lower image).

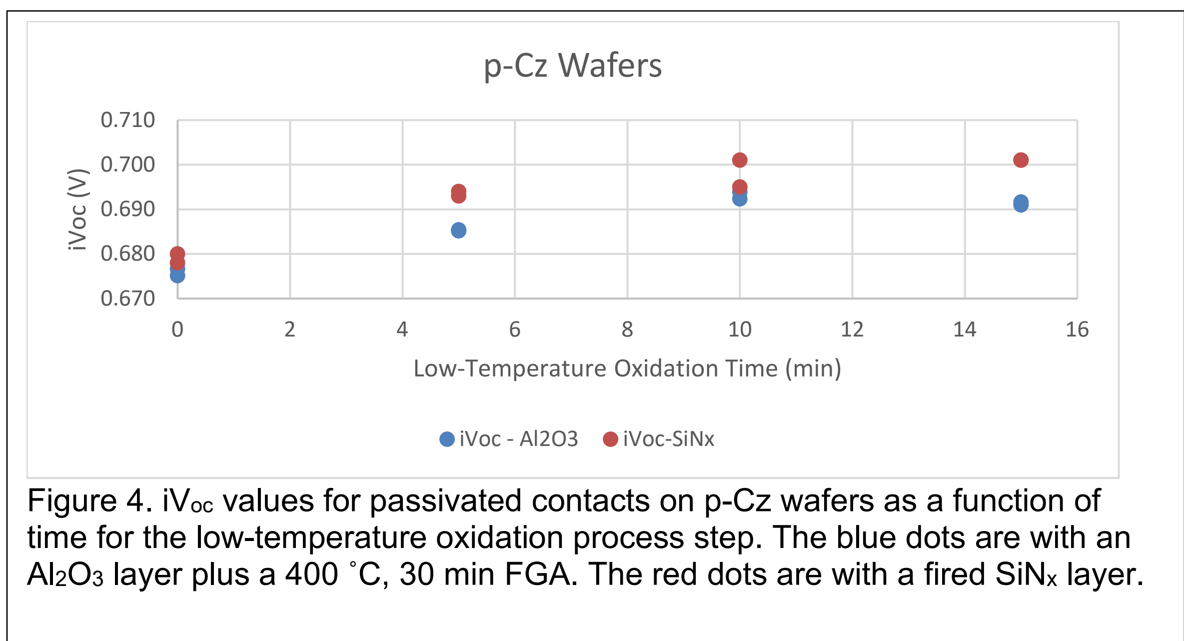

Figure 4. iV_{oc} values for passivated contacts on p-Cz wafers as a function of time for the low-temperature oxidation process step. The blue dots are with an Al_2O_3 layer plus a 400 ˚C, 30 min FGA. The red dots are with a fired SiN_x layer.

Despite the shipping complications, Figure 3 reveals how well the DWP wafers can be passivated with SiO_2/poly-Si passivated contact structures for intrinsic, n-type, and p-type poly-Si. These were all bulk- and surface-passivated using a SiN_x layer as a H reservoir and the firing scheme described above. Note the relatively high iV_{oc} values (> 650 mV), despite the low bulk wafer effective lifetimes ~2E-4 secs. However, the surface recombination parameter, J_o, is quite low for all poly-Si polarities.

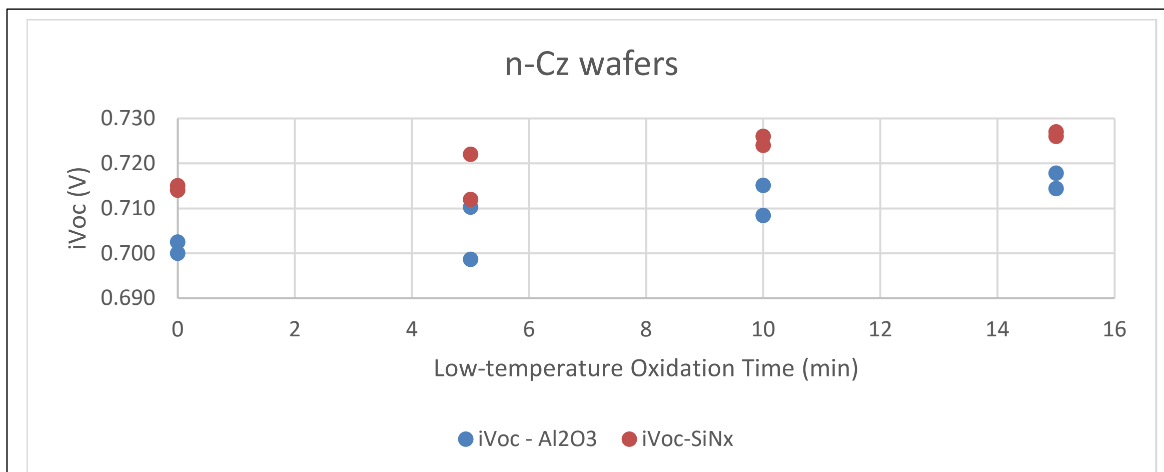

Figure 5. iV_{oc} values for passivated contacts on n-Cz wafers as a function of time for the low-temperature oxidation process step. The blue dots are with an Al_2O_3 layer plus a 400 ˚C, 30 min FGA. The red dots are with a fired SiN_x layer.

Figure 3 also reveals another process issue that had to be overcome, namely H-induced blistering during the firing step. A blister-free solution was found after tests showed they were a function of SiN_x growth recipes, film thickness, firing profiles, and surface morphology of the DWP wafers.

Figure 3 show that using the passivation techniques developed for DWPs with SiO_2/poly-Si contacts, the bulk and the surface can be simultaneously passivated with H from the SiN_x dielectric layer.

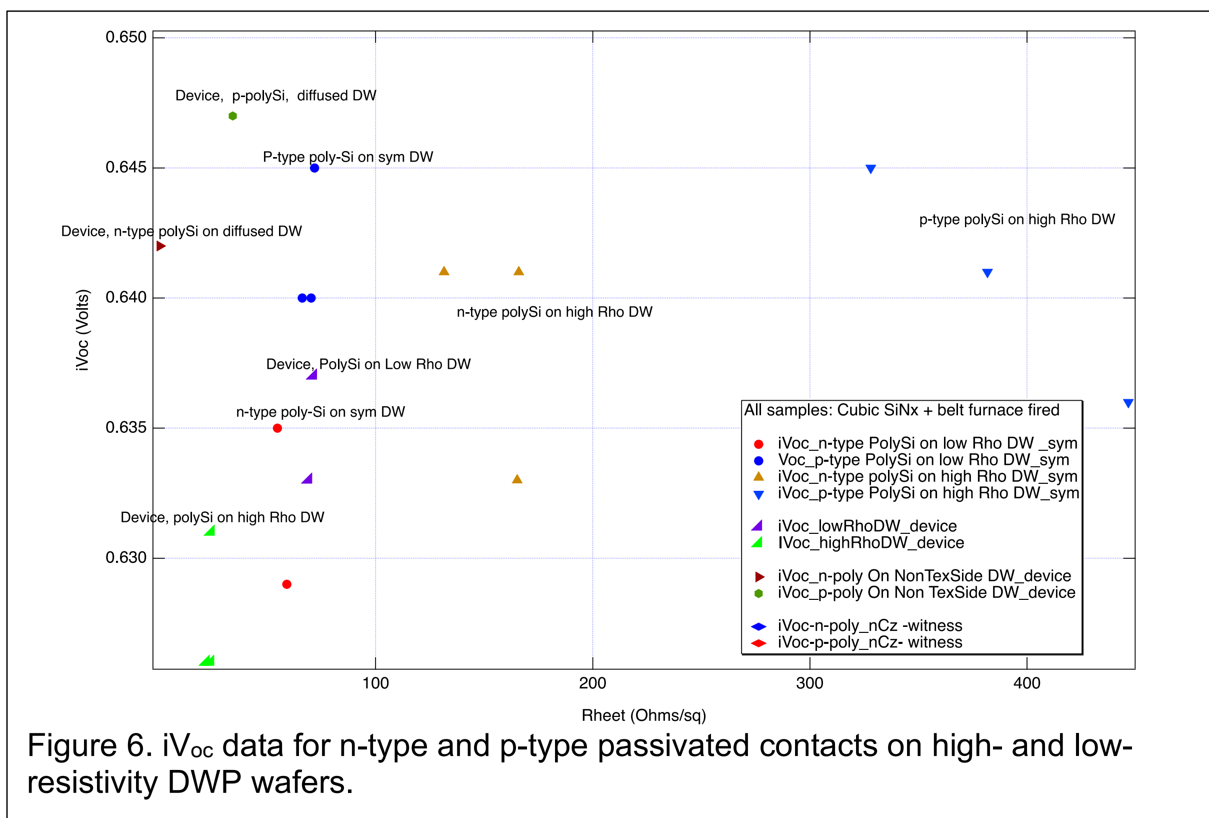

Figure 6. iV_{oc} data for n-type and p-type passivated contacts on high- and low-resistivity DWP wafers.

Task 2.1 developed p-type passivated contacts on p-Cz wafers to establish a baseline and upper limit for the DWP wafers. Figure 4 shows iV_{oc} data on symmetric p-Cz wafers coated with passivated contacts and using either Al_2O_3 layers to passivate (blue dots) or fired SiN_x layers (red dots). The iV_{oc} values are much higher on p-Cz wafers compared with DWP wafers and the fired SiN_x passivation treatment is more effective than the Al_2O_3 plus forming gas anneal (FGA) treatment. Figure 5 shows the same data as Figure 4 but for n-Cz wafers. Here, the iV_{oc} values are even higher than on the p-Cz wafers. Task 2.2 used knowledge from Task 2.1 to develop p-type poly-Si contacts on high-resistivity DWP wafers. The data of Figure 7 show quite low J_o values of the n-poly-Si emitters on p-type DWP wafers. Without AlO_x passivation the J_o value is ~ 22 fA/cm^2. With AlO_x passivation, the J_o value climbs between 30-35 fA/cm^2.

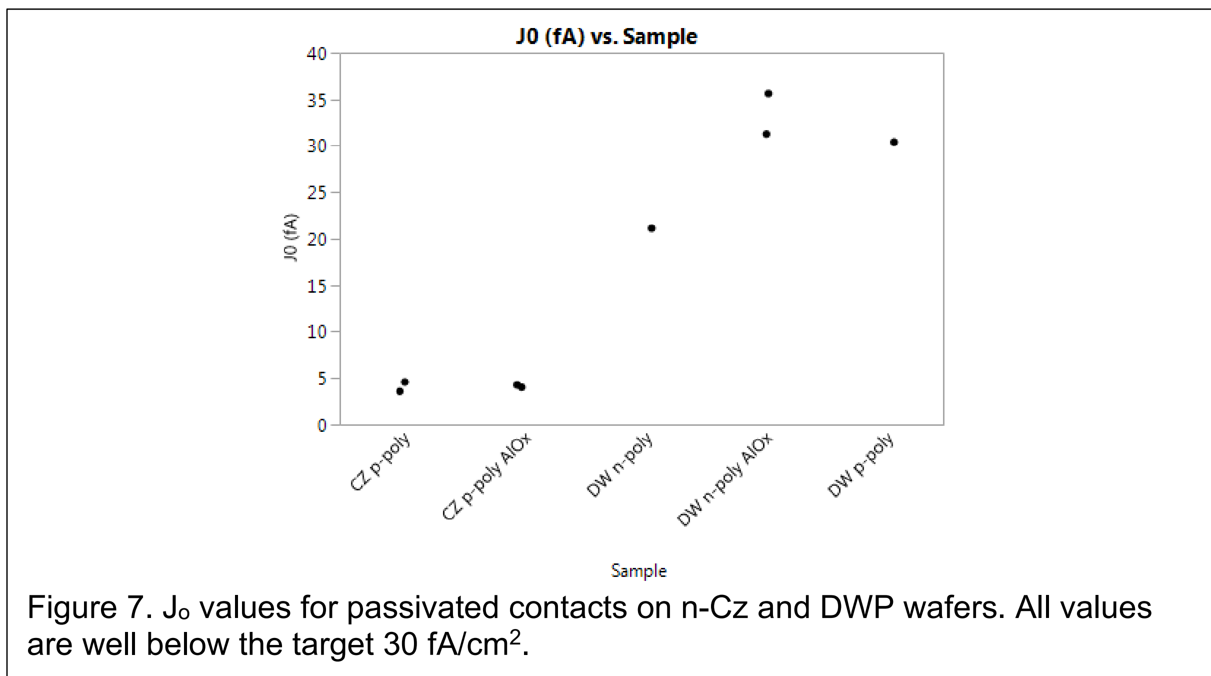

Figure 7. J_o values for passivated contacts on n-Cz and DWP wafers. All values are well below the target 30 fA/cm^2.

Figure 6 shows iV_{oc} data of both n-type and p-type passivated contacts on high resistivity DWP wafers. iV_{oc} values greater than 640 mV were obtained for both polarities. Sister samples to those shown in Figure 3 and 7 with J_o values less than 30 fA/cm^2 were metallized with evaporated silver through a shadow mask to form transmission line (TLM) patterns. The contact resistivity TLM data for n-type and p-type passivated contacts on DWP wafers are shown in Figure 8. All data are less than the milestone target of 30 mOhm-cm^2. Milestone 1-2-1 was completed with the data shown in Figures 3 and 8.

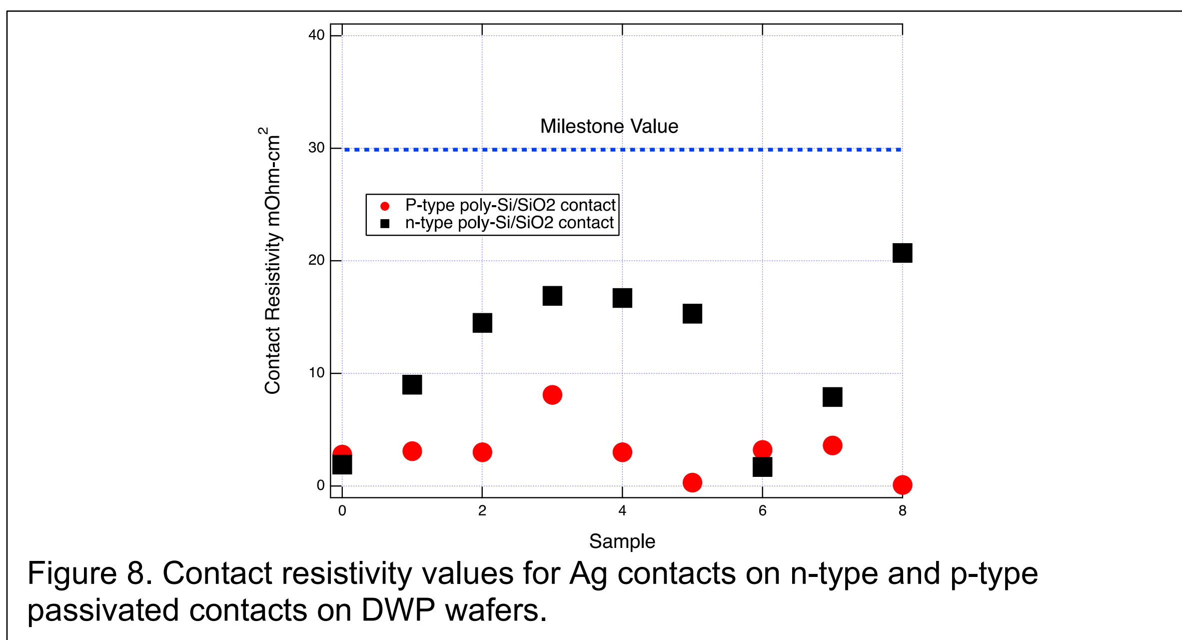

Figure 8. Contact resistivity values for Ag contacts on n-type and p-type passivated contacts on DWP wafers.

Task 2.3 was de-scoped from the project as it related to Task 1.3, which was deemed not necessary for this project due to prior work with a different partner.

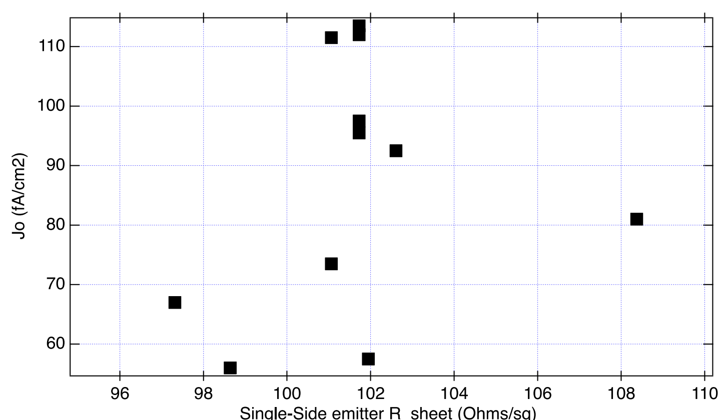

Figure 9. Diffused emitter J_o vs R-sheet on high-resistivity (20 Ohm-cm) DWP wafers.

Task 3 built on of lessons learned from Tasks 1 and 2 and worked towards processing functional p-TOPCon devices on DWP wafers. Task 3.1 developed an n-type passivated emitter on p-type DWP wafers. Figure 9 shows PCD data on symmetric high-resistivity (20-ohm-cm) DWP wafers that were POCl diffused to form an n-type emitter. The data show J_o as a function of emitter sheet resistance. The task's goal was J_o < 130 fA/cm^2 which was easily achieved, with a sheet resistance between 100 and 120 Ohms/sq. Most of the data fall in this range, but there were a few samples with lower sheet resistance.

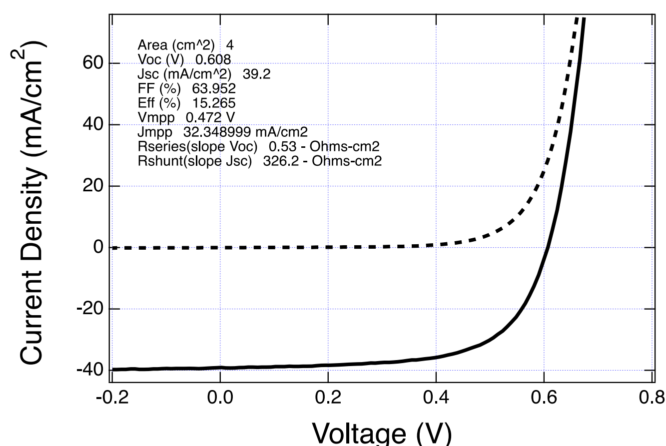

Figure 10. Light and dark JV data for a p-TOPCon device with evaporated Ag grids.

Task 3.2 developed a process to form a front diffused emitter and a rear p-type passivated contact on DWP wafers. The process was described above and the iV_{oc} values for devices are shown in Figure 6 for high- and low-resistivity DWP wafers as

a function of measured sheet resistance. Task 3.3 dealt with metallization of the p-TOPcon devices. Because NREL did not have much experience with screen printing at the time of this project, we decided to use our standard metal evaporation process using shadow masks. This required that the fired SiN_x be removed from the device before the metal could be deposited. Hot phosphoric acid was used to remove the SiN_x layer. This process is selective to SiN_x and does not affect the poly-Si layer when performed on n-Cz /poly-Si samples. However, removing the SiN_x with phosphoric acid on DWP wafers severely increased the surface recombination. The result was that metallized devices using evaporated Ag were never as good as the unmetallized PCD data would predict. Figure 10 shows the light and dark JV data on the best sample from the samples shown in Figure 6. Note the low FF and decreased V_{oc} (~600 mV) compared to iV_{oc} (~ 630 - 645 mV). In retrospect, developing fired, screen-printed metallization would have benefited these samples. Figure 11 shows the Suns V_{oc} data overlayed with the light JV data from Figure 10. Here we see the effects of severe series and shunt resistance on the FF. FF loss analysis showed series and shunt resistance losses were major contributors to the low FF. Milestone 2.3.1 was not achieved, as the best cell efficiency was only 15% (Figure 10). Again, this was mainly due to not metallizing the cells with fired screen-printed pastes due to a lack of experience with this process. Given the very good iV_{oc} values for unmetallized devices, we believe the cells could have achieved >20% efficiency with proper metallization.

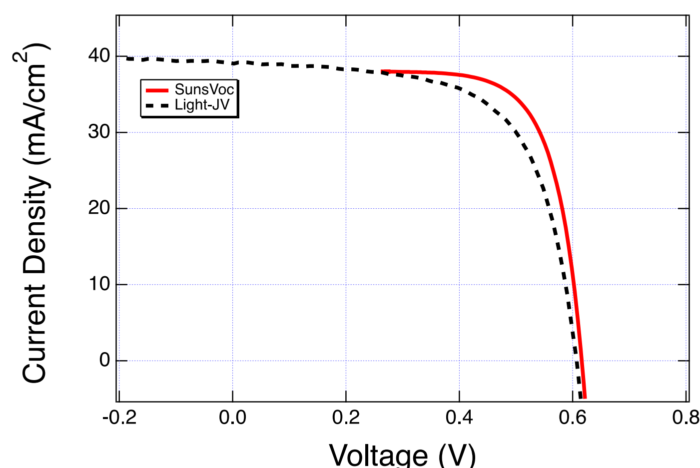

Figure 11. Light JV data and Suns V_{oc} data from the best p-TOPCon on DWP wafer produced in this study.

In summary, the tasks and milestones for this project, shown in Table 1 and described above were completed. The final milestone goal of a 20% device was not achieved in the time allotted for this project. However, we believe the efficiency goal could have been met with proper screen-printing tools and experience. The stretch milestone was not attempted due to poor device results with evaporated metal contacts on the devices.

8. Significant Accomplishments and Conclusions: The main significant accomplishment for this project was developing a process whereby both the bulk and surface passivation of a device using SiO_2/poly-Si contacts on a DWP wafer could be preserved. This process led to iV_{oc} values approaching 650 mV. However, challenges with metallization of the devices due to lack of equipment and experience did not allow the team to achieve the highest efficiencies possible with this passivation scheme. Despite the good work shown on this project, the iV_{oc} values obtained were only on par with those of a PERC passivation process on DWP wafers shown earlier by CubicPV and Q-Cells. Likely, the lower bulk lifetimes and multicrystalline surface of the DWP wafers did not allow the true benefit of the passivated contact structure to be utilized in a p-TOPCon device. This is an important result, as it allows CubicPV to make clear process decisions if they move their DWP wafers into cell production. Again, this project dealt with tool and process challenges that likely contributed to not obtaining the final milestone goal. Having to move samples between Colorado and Massachusetts during the critical process steps was not ideal. Additionally, not having fireable screen-printing capabilities limited the obtained efficiencies of the final devices. As described earlier in this report, some tasks were deemed already covered during previous work and were descoped from this project.

9. Path Forward: Commercialization plans for a p-type TOPCon device using DWP wafers lie solely with CubicPV. There are no technical barriers to commercialization of this product if the proper tools and processes are used. Because the full benefit of the passivated contact does not seem to be able to be realized on the DWP wafers, it may not be economically favorable to build a p-TOPCon device over a PERC device. However, the lower cost of the DWP wafer may lend itself to a viable bottom cell wafer in a tandem structure. Indeed, CubicPV has recently pivoted to this device architecture.

10. Products: No publications/papers, scientific/technical software/data, websites, inventions/patents, or other products were developed or submitted under this award.

11. Project Team and Roles:

David Young – PI (NREL), concept development, experimental design, data analysis, reporting.
Jasmin Hofstetter – co-PI (CubicPV), concept development, experimental design, data analysis.
Adam Lorenz – business and technical contact at CubicPV, concept development, experimental design, data analysis.
William Nemeth – Process engineer (NREL), sample preparation and characterization, experimental design.
Markus Kaupa – Process technician (NREL), sample preparation and characterization.

12. References:

1. VDMA ITRPV Roadmap. https://www.vdma.org/international-technology-roadmap-photovoltaic.
2. Feldmann, F.; Bivour, M.; Reichel, C.; Steinkemper, H.; Hermle, M.; Glunz, S. W., "Tunnel oxide passivated contacts as an alternative to partial rear contacts." *Solar Energy Materials and Solar Cells* 2014, 131, 46-50.
3. Mack, S.; Herrmann, D.; Lenes, M.; Renes, M.; Wolf, A., "Progress in p-type Tunnel Oxide-Passivated Contact Solar Cells with Screen-Printed Contacts." *Solar RRL* 2021, 5 (5), 2100152.
4. Khokhar, M. Q.; Yousuf, H.; Jeong, S.; Kim, S.; Fan, X.; Kim, Y.; Dhungel, S. K.; Yi, J., "A Review on p-Type Tunnel Oxide Passivated Contact (TOPCon) Solar Cell." *Transactions on Electrical and Electronic Materials* 2023, 24 (3), 169-177.
5. Schindler, F.; Schön, J.; Michl, B.; Riepe, S.; Krenckel, P.; Benick, J.; Feldmann, F.; Hermle, M.; Glunz, S. W.; Warta, W.; Schubert, M. C. "High efficiency multicrystalline silicon solar cells: Potential of n-type doping," 2015 *IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, 14-19 June 2015; 2015; pp 1-3.