Final Technical Report: Development of High-Quality, Very Large-Grained Cd(Se,Te) Thin Films for CdTe Solar Modules

Joel Duenow and David Albin

National Renewable Energy Laboratory

NREL is a national laboratory of the U.S. Department of Energy
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Contract No. DE-AC36-08GO28308

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Suggested Citation
Joel Duenow and David Albin. 2025. *Final Technical Report: Development of High-Quality, Very Large-Grained Cd(Se,Te) Thin Films for CdTe Solar Modules*. Golden, CO: National Renewable Energy Laboratory. NREL/TP-5K00-91324. https://www.nrel.gov/docs/fy25osti/91324.pdf.

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NOTICE

This work was authored by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by the U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office. The views expressed herein do not necessarily represent the views of the DOE or the U.S. Government.

Final Technical Report

SECTION I: COVER PAGE

a. Federal Agency	Department of Energy	
b. Award Number	*TCF-21-25048*	
c. Project Title	Development of high-quality, very large-grained Cd(Se,Te) thin films for CdTe solar modules	
d. Recipient Organization	National Renewable Energy Laboratory	
e. Project Period[1]	Start: Oct 1, 2021	End: Sept 30, 2022
f. Budget Period	Start: Oct 1, 2021	End: Sept 30, 2022
g. Reporting Period	Start: Oct 1, 2021	End: Sept 30, 2022
h. Report Term or Frequency	Final Technical Report	
i. Principal Investigator (PI)	David S Albin Senior Scientist david.albin@nrel.gov 303-384-6550	
j. Business Contact (BC)	Bill Hadley Technology Transfer Office b bill.hadley@nrel.gov 303-275-3015	
k. Certifying Official (if different from the PI or BC)	n/a	

Signature of Certifying Official Date

By signing this report, I certify to the best of my knowledge and belief that the report is true, complete, and accurate. I am aware that any false, fictitious, or fraudulent information, misrepresentations, half-truths, or the omission of any material fact, may subject me to criminal, civil or administrative penalties for fraud, false statements, false claims or otherwise. (U.S. Code Title 18, Section 1001, Section 287 and Title 31, Sections 3729-3730). I further understand and agree that the information contained in this report are material to Federal agency's funding decisions and I have any ongoing responsibility to promptly update the report within the time frames stated in the terms and conditions of the above referenced Award, to ensure that my responses remain accurate and complete.

[1] If you have received No Cost Time Extensions (NCTE), please add a note below the table indicating the length of each one and which budget periods were affected.

SECTION II: EXECUTIVE SUMMARY

TCF-21-25048 is a one-year project to quantify the potential attributes of recent NREL inventions where CdTe devices with grain sizes exceeding 100's of microns in lateral dimension can be fabricated using a novel seeded-epitaxial process. A $CdSe_{0.1}Te_{0.9}$ film is evaporated on commercially available transparent conducting oxide (TCO) where the latter surface roughness (R_a) has been reduced to < 1-nm. After NREL's colossal grain growth (CGG) process, the grain size of this "seed" layer is increased to 100-1000 um. CdTe is then deposited epitaxially resulting in a large-grain CdTe device structure without use of $CdCl_2$. As of this report, we have:

- Demonstrated the feasibility of using Tec-15 substrates after surface roughness (R_a) reduction (nexTC).
- Developed reproducible CGG processes for this commercially available substrate.
- Developed a close-spaced sublimation (CSS) process for CdTe epitaxy using these substrates.
- Demonstrated that large-grain CdTe films have less sub-band (band tail) absorption than conventional, small-grain CdTe.
- Demonstrated that large-grain CdTe films (no $CdCl_2$) have carrier lifetimes up to 1.5 ns.
- Demonstrated that carrier lifetimes in epi-CdTe films (no $CdCl_2$) have comparable lifetimes when compared to the best pX-CdTe films (FSLR) treated with $CdCl_2$.
- Started making large-grain CdTe devices using CGG templates and epitaxially deposited CdTe.

Major Goals and Objectives

NREL is working with First Solar (FSLR) to study the application of colossal grain growth (CGG) films in CdTe devices. CGG films are used as templates or "seed" layers upon which NREL deposits large-grain, thin films of CdTe which are then compared with state-of-the-art films supplied by FSLR. NREL's process has the potential to make devices with extremely large CdTe grains without $CdCl_2$.

Technical Progress

This 1-year project required : 1) developing, low surface roughness (R_a) TCO-coated glass substrate to facilitate CGG, 2) developing a reproducible CGG process, and 3) developing a way to epitaxially deposit CdTe on CGG films. The CGG process is based upon the rapid melting, spreading, and solidification of an evaporated $CdSe_{0.1}Te_{0.9}$ (CST) film resulting in a large-grain template upon which the subsequent nucleation and growth of large-grain CdTe films is made possible. Previously, it was determined that the surface roughness of the substrate upon which the CST layer was evaporated needed to be less than approximately 1.0- 1.5 nm. For early demonstration purposes, this roughness could be obtained simply by using a thin, 100-nm layer of alumina deposited on glass. However, for devices, the alumina needed to be replaced by a transparent conducting oxide (TCO). FSLR supplied ITO-coated glass substrates which met the necessary R_a requirement and thus we were able to apply CGG successfully. Unfortunately, the as-received sheet resistance of these films was high (~ 80 ohms/sq) though subsequent processing reduced this to about 30 ohms/sq. In addition, initial device results suggested a "buried" homojunction with possible n-type conversion of the CST due to the possibility of

Indium diffusion at the junction. A better option was to use Tec15 substrates coated with a "smoothing" layer of approximately 500 nm of undoped SnO_2. These substrates were developed through a collaboration made with Cory Perkins (nexTC) who had such a technique using a doctor-blade application. This latter option was preferred since it also demonstrates the viability of using commercially available TCO-coated "Tec" glass from NSG. In addition to low R_a, the sheet resistance was much better at 14-15 ohms/sq and thus became our standard substrate for finishing epi-CdTe devices.

CGG development concentrated on developing a reproducible process to supply large-grain templates for subsequent CdTe epitaxy. As we had noted in our only publication to date of the CGG process [1], grain boundary (GB) imperfections on the surface of CGG seed films cause preferential rapid nucleation and growth relative to bulk regions and non-coherent epitaxy. Previously, this was mitigated by using low levels of oxygen during CdTe epitaxy. We speculated that oxygen effectively increased the rate of bulk nucleation such that bulk growth dominated and coherent epitaxy resulted. In this project we determined that heating of the CGG seed layer during the CGG step and any subsequent heating of the film prior to epitaxy resulted in thermal etching of the seed layer. Morphologically this would manifest in GB and bulk pitting (imperfections) in the CGG film with high R_a values of 10-30 nm. By reducing the time of the CGG anneal step (from 15 m to only 1 m) and using higher ambient pressures of between 50-100 Torr we were able to produce near mirror-like CGG seed layers with R_a values a magnitude lower (1-3 nm). Though considerably smoother, coherent epitaxy without using oxygen was still not possible.

Though not stated definitively in [1], we now believe that CGG occurs by an explosive recrystallization process where the latent heat for melting and subsequent large-grain solidification may be related to the exothermic amorphous-crystalline transition present in Se-Te alloys [2]. Evaporated CST precursor films contain an undetermined amount of amorphous material that can be studied by x-ray diffraction. Increasing the amorphous content of these films is one way to improve CGG reproducibility. This can be achieved by restricting substrate temperature during evaporation to not more than about 400 °C and using higher evaporation rates. During the CGG step, increasing the ramp rate from temperature to the conversion temperature of 550 °C also appears to initiate better heat evolution resulting in more reproducible CGG. Finally, reducing higher melting temperature oxide phases in the film by storing precursors under vacuum as well as using H_2 as the CGG ambient improved reproducibility.

Early experiments at CdTe epitaxy were attempted using vapor transport deposition (VTD) as the technique to deposit CdTe. At first, the observed surface morphology of deposited films suggested successful epitaxy as shown in Figure 1(a). However, subsequent cross-sections of these films using electron-beam back scatter diffraction (EBSD) as seen in Figure 1(b) reveal that epitaxy did not extend the thickness of the CdTe layer, i.e., is not coherent. Rather, epitaxy breaks down during the CdTe deposition due to the changing CdTe vapor flux above the substrate as it moves under the VTD injector. When we switched to a close-spaced sublimation (CSS) process where the substrate is fixed relative to the source, epitaxy improved considerably.

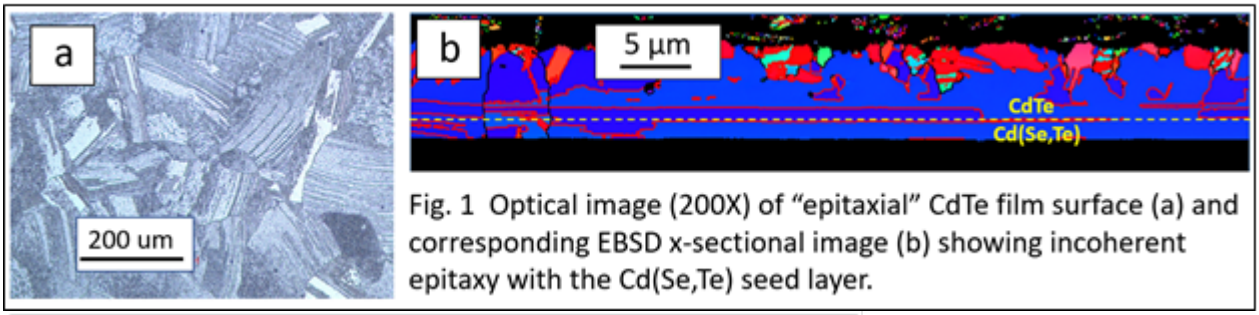

Fig. 1 Optical image (200X) of "epitaxial" CdTe film surface (a) and corresponding EBSD x-sectional image (b) showing incoherent epitaxy with the Cd(Se,Te) seed layer.

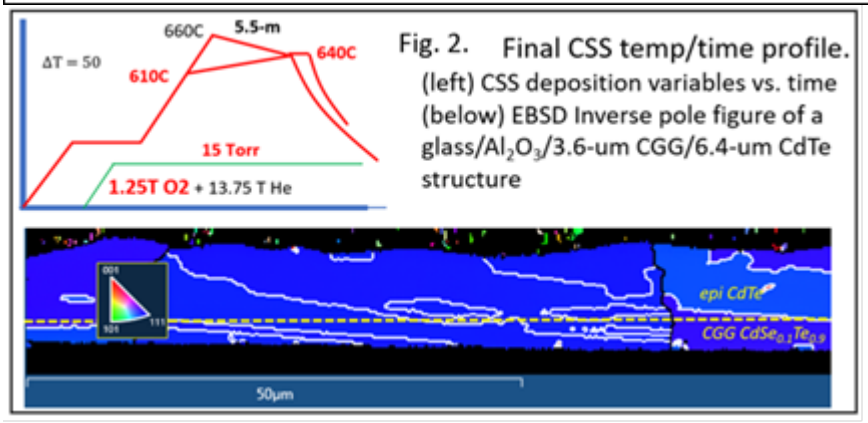

Fig. 2. Final CSS temp/time profile. (left) CSS deposition variables vs. time (below) EBSD Inverse pole figure of a glass/Al_2O_3/3.6-um CGG/6.4-um CdTe structure

CSS variables observed to impact epitaxy significantly included: source-to-substrate distance, O_2 partial pressure, total system pressure, and control of both the CdTe source (T_{src}) and substrate (T_{sub}) temperatures. Again, oxygen was used to suppress GB nucleation and resulting incoherent growth. Without oxygen, films were too rough for thin passivation layers appropriate for PERC and DH structures. One mechanism observed while developing a CSS-epitaxy was that of oxygen-depletion. In CSS, the ambient is typically adjusted at the beginning of the process by filing the CSS chamber with a pre-determined mixture of oxygen to inert (He) gas. During the subsequent deposition, oxygen is consumed somewhat by incorporation in the deposited CdTe film but more by oxidizing the CdTe source itself. The net result is that oxygen levels significantly decrease by the end of the process. Experimentally, the change in the growth ambient due to oxygen depletion effects resulted in changing film morphologies with growth. This was particularly problematic when attempting thicker epi-CdTe films. This effect was notably reduced by tapering off the CSS deposition flux during the latter part of the CSS step as shown in Fig. 2 by reducing $\Delta T = T_{src}-T_{sub}$ during the growth. Fig. 2 also shows a cross-sectional EBSD image confirming coherent registration (epitaxy) between a 6.4-um thick CdTe layer grown on a 3.6-um CGG $CdSe_{0.1}Te_{0.9}$ seed layer.

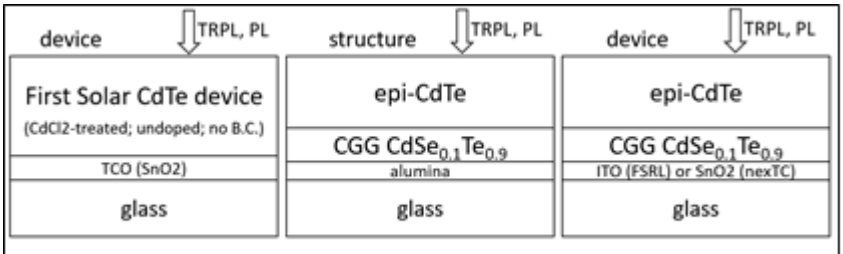

Fig. 3 Structures and Devices used to evaluate back-side TRPL

The Q3 "material qualification" phase produced the *device* and *structures* shown in Fig. 3. Most *structures* were of the single heterojunction (SH) design where no passivation was applied to the back surface. The FSLR *device* was a production, undoped, $CdCl_2$-treated, device film stack with the back contact absent. The NREL "*structure*" resembles this except no $CdCl_2$ was used and the substrate consists of alumina-coated glass. The NREL "*device*" represents the same $CdSe_{0.1}Te_{0.9}$/epi-CdTe structure deposited on transparent conducting oxide (TCO) coated glass (Tec-15) substrates from nexTC where the TCO surface roughness (R_a) was modified to less than 1-nm to facilitate the CGG process step. The device structure was developed to potentially provide another way to compare with FSLR devices.

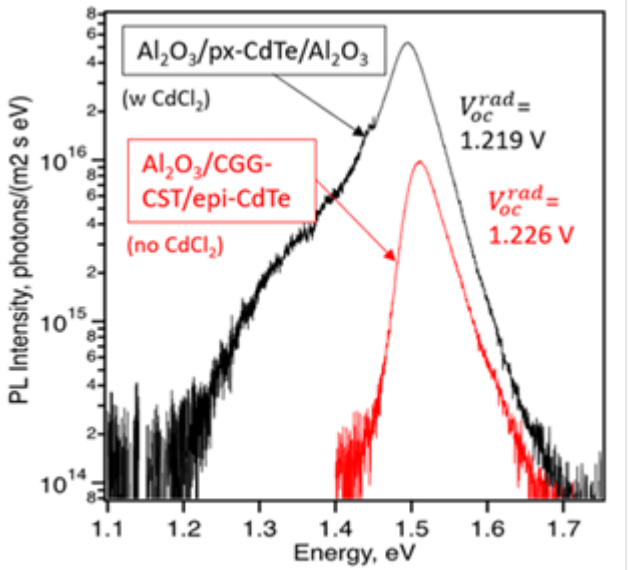

Fig. 4 PL comparison of pX and epi-CdTe structures

One important characteristic of the epitaxial, large-grain CdTe (no $CdCl_2$) structure shown in Fig. 1 is the significant decrease in band tails. Fig. 2 compares the 1-sun absolute PL of the NREL "structure" shown in Fig. 1 with a standard polycrystalline (pX) CdTe double-heterostructure (DH) where greater sub-band absorption in the latter is apparent. In these measurements, the excitation beam was incident on the back side of the structure. $V_{oc,rad}$ averaged over 10 different epi-CdTe samples equaled 1.226 volts relative to a value of 1.219 volts in the pX sample. The pX sample (a better passivated, DH rather than SH structure) did have higher luminescence resulting in a larger photoluminescence quantum yield (PLQY) of 2.3E-06 and thus lower recombination loss of 337 mV relative to the smaller PLQY of the epi-CdTe samples (1.1E-07) and corresponding higher recombination loss of 416 mV. Resulting implied Voc (iV_{oc}) for the $CdCl_2$ treated pX DH and epi-CdTe, non-$CdCl_2$ treated SH were 882 and 809 mV respectively.

TRPL measurements with excitation from the back side (top surface) were made on the two FSLR structures shown in Figure 3: a production film stack without doping, and one with Cu doping. Both structures were $CdCl_2$ treated at FSLR. The average carrier lifetimes for the two FSLR samples were measured as < 250 ps and <50 ps respectively. The lifetimes of the NREL structure (grown on alumina-coated glass and without $CdCl_2$) were higher with values between

0.3 to 1.5 ns. The measured lifetime of a NREL device stack using the low R_a substrates provided by nexTC was comparable to the FSLR samples (230 ps).

Processing		*Device Results*			
Cu	CdCl2	Voc (volts)	Jsc (mA/cm2)	FF (%)	Eff (%)
no	no	0.305	4.8	33.6	0.49
yes	no	0.325	14.1	36.3	1.7
yes	yes	0.558	20.8	26.5	3.1

Table 1 – Preliminary epi-CdTe Devices

Finally, devices were made at NREL using the epi-CdTe device structure shown in Fig. 3. The initial device characteristics are shown in Table 1. Lower J_{sc} may be related to a buried junction due to n-type CdSeTe behavior resulting from the use of H_2 anneals in the CGG process. A buried junction COMSOL model was developed by by Dr. Marco Nardone (BGSU) to better understand what was limited device performance. This simulation suggested that the low performance of these initial devices could be associated with both recombination at the SnO_2/CST and CST/epi-CdTe interface and poor hole transport in the CST layer.

Impact:

Unlike FSLR films, NREL's epi-CdTe films do not need $CdCl_2$ for grain growth. Since the final grain size is quite large (> 100's µm), $CdCl_2$ is also not required for grain boundary passivation. Thus, NREL's approach represents a potential way to make CdTe films and devices without $CdCl_2$. The impact is great since GrV doping (Arsenic) has yet to yield thin film devices with significant boosts in V_{oc} and compensation of As_{Te} acceptors by Cl-defects (e.g. Cl_{Te}) is possible.

Suggested Future Work:

The work performed in this FY22 TCF project is at best preliminary. The benefit associated with reducing the density of GBs is apparent due to the observed luminescence and lifetime seen in CGG/epi-CdTe structures without the use of $CdCl_2$. Device performance is less than stellar but should not represent an inherent obstacle for future development. Very limited device processing was attempted due to the shortage of time. Beyond the apparent need to reduce recombination at the SnO_2/CGG and CGG/CdTe interfaces, COMSOL simulations do emphasize the obvious: the properties of the layer located at the heterojunction, i.e., the CGG layer, needs to be improved. With $CdCl_2$, DHs made using CGG layers have yielded lifetimes up to 65 ns. Without $CdCl_2$, these same DHs yield lifetimes close to instrument response levels. However, we do not believe the program needs another way to make CdTe devices with $CdCl_2$. The primary advantage of the CGG method is that it is the only cost-effective way to make CdTe solar cells *potentially* without $CdCl_2$ which could improve dopant activation in solar cells intentionally doped with GrV dopants like As.

Suggested experiments for any follow-up work (i.e., through a no-cost extension) should concentrate on determining whether alternative processing and anneals can reduce recombination in the CGG layer itself and whether this can be done with no $CdCl_2$ or at least through techniques designed to reduce $CdCl_2$ if indeed it is used. At the same, processing should likely avoid the n-type conversion of the CST layer to improve current collection.

Project Budget Status (as of August 2022):

Actual expenses as of August (YTD $88,391) trail baseline (YTD $139,083) by $50,692. This is due to lower-than-expected costs for EBSD and TRPL/PL measurements. Much of this was due to not providing many samples for TRPL/PL and EBSD measurements, however, both characterization tools were in heavy demand at NREL. At this point, the value of $50,692 can be used as a good estimate of what funds might be left at the end of this contract

Key Personnel Changes: nothing to report
Scope Issues: No scope issues.

SECTION III: TASKS AND MILESTONE PROGRESS

The Q1 milestone (Dec. 31, 2021) finalized test structures, characterization, and sample exchange procedures. The Q3 milestone (covering activities during Q2 and Q3) optimized the properties of epitaxially deposited CdTe films using structural feedback from electron backscatter diffraction (EBSD) and material (electronic) feedback primarily from external radiative efficiency (ERE) and time-resolved photoluminescence (TRPL) decay. Finally, the Q4 milestone is to compare the relevance of NREL and FSLR films in passivated emitter and rear cell (PERC) devices.

Task Number and Title:

Task 1.1 – "Finalize Test Structures, characterization, and sample exchange procedures (due 12/31/2021).
Task 1.2 – "Fabricate DH test and control structures, measure, and rank test performance relative to FSLR controls (due 6/30/2022).
Task 1.3 – "Fabricate PERC test and control structures and rank test performance relative to FSLR controls (due 9/30/2022).
Task 1.4 – "Communicate results to the community of stakeholders (due 9/30/2022).

Planned vs. Actual Activities:

Large-grain CdTe films grown epitaxially on large-grain (CGG) seed templates luminescence even without $CdCl_2$ and have respectable minority carrier lifetimes of up to 1.5 ns. The significantly lower band tails of large-grain films suggest a path forward to reducing radiative voltage losses. The film-side TRPL lifetimes of CdTe grown epitaxially on CGG seed films exceeded the lifetimes of similar device structures provided by FSLR for both un-doped and Cu-doped CdTe films. Though some device structures (using FSLR ITO films) were sent to FSLR, no PERC devices were attempted due to the poor device performance levels obtained.

References:

[1] D.S. Albin, M. Amarasinghe, M. O. Reese, J. Moseley, H. Moutinho, and W.K. Metzger, J. Phys. Energy 3 (2021) 024003
[2] P.A. Vermeulen, J. Momand, and B.J. Kooi, J. Chem. Phys. 141, 024502 (2014).