Adaptive Fault Current-Limiting Control of MMC for Protection of Multiterminal HVDC Systems

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Adaptive Fault Current-Limiting Control of MMC for Protection of Multiterminal HVDC Systems

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Keywords: MMC, HVDC, MTDC, active fault current limiting, fault ride-through

Abstract

A crucial requirement of the protection system for multi-terminal high-voltage DC (MTDC) transmission is that it is capable of selectively isolating the faulty area from the healthy part of the network using DC circuit breakers (DCCBs), while ensuring continuous operation of converter stations in the healthy part of the network. But in the half-bridge modular multilevel converters (HB-MMCs) based MTDC system, since HB-MMCs do not have fault current absorption capability, when a DC fault occurs, the rising fault currents can quickly reach the blocking threshold within a few milliseconds and disrupt the operation of the MMCs in the healthy part. To facilitate fault-ride-through capability of MTDC system, large DC reactors are often considered in series with DCCBs to reduce the rate of rise of the fault current and prevent blocking the MMCs in the healthy part of the DC networks; however, large DC reactors prohibitively increase the cost of the system, introduce stability issues and can create post-fault oscillations. This paper presents an adaptive fault current-limiting control method for MMCs to avoid their blocking and enable the continuous operation of the healthy part of MTDC systems. The method contains two parts: The first part is based on circulating current feedforward control, which emulates virtual reactors in each arm of an MMC, and is immediately activated when the fault current starts to increase to reduce the rate of rise of the fault current. The second part temporarily bypasses all the submodules when the fault current exceeds a preset threshold, complementing the fault current-limiting effect of the first part. Neither part requires fault detection signals, and they are automatically activated during faults. Simulation case studies of a four-terminal bipolar MMC-based high-voltage DC system are presented to demonstrate the effectiveness of the proposed control methods.

1 Introduction

DC Faults in modular multilevel converters (MMCs) based multi-terminal high-voltage DC (MTDC) networks results in significant fault currents due to the discharge of submodule (SM) capacitors and the low number of inductive elements within the DC networks. Half-bridge (HB) MMCs lack the ability to limit and clear fault currents; hence, to protect the insulated-gate bipolar transistor (IGBT) modules in the MMC, its submodules (SMs) are blocked within tens to hundreds of microseconds after a DC fault occurs. On the other hand, the fault interruption time of a DC circuit breaker (DCCB) ranges from 3 to 10 ms [1, 2]. Due to this time difference in the timescales of DCCB operation and MMC blocking, many HVDC converters trip during a DC fault in the HB-MMC-based MTDC system. This contradicts the purpose of selective protection scheme of MTDC system, which aims to maintain continuous operation of the healthy part of a network during a fault; hence, it is critical to limit the fault current increasing until the fault is isolated to protect MTDC networks.

The fault current-limiting methods for HB-MMCs fall into two broad categories: passive methods and active methods. Passive methods limit fault currents by introducing reactors in the network, which not only increase cost and space requirements but also can result in certain drawbacks, such as 1) deteriorating system stability and dynamics; 2) post-fault oscillations [3], which can trigger blocking the MMCs; and 3) higher fault clearing times. As a result, active fault current-limiting control methods have attracted significant interest. Active methods include simulating a virtual DC reactor through control functions [4], and bypassing all or parts of the SMs [1] to prevent the discharge of SM capacitor. Existing control methods emulate virtual DC reactors by modifying the reference for the DC bus voltage control or the active power control, but this is not suitable for the MMC rectifiers controlling the AC bus voltage and frequency in offshore wind applications. Further, existing methods for bypassing SMs present several limitations: 1) The bypassing operation is activated only when the protection detects a DC fault, usually 2 to 3 ms after the fault occurrence, a period when the fault current could still quickly rise and induce SM blocking operation. 2) The scheme of bypassing all the SMs is not necessary for MMCs that are located far away from the fault. 3) Partial bypassing schemes calculate the number of SMs that must be bypassed, which requires knowledge of the

inductance and capacitance in the fault circuit, which is not practical.

This paper presents a novel adaptive current-limiting control method to automatically limit the fault current when a DC fault occurs. It consists of two parts: 1) virtual arm impedance-based control for the main current-limiting function and 2) temporarily bypassing the SMs for supplementary protection if the performance of the former is insufficient. The virtual arm impedance control is based on the feedforward of the circulating current; it emulates a reactor in each arm to limit the rate of rise of the fault current. This control is applicable to both MMC inverters and rectifiers; hence, it can complement the existing virtual DC reactor-based control methods. The former part, although it reduces the rate of rise of the fault current, cannot change the peak value of the fault current. If the peak value cannot be limited within the SM blocking threshold before the fault clearance time (i.e., DCCB operating time), it will still lead to blocking of HVDC converter stations. Therefore, an additional method is needed to limit the peak value of the fault current, which is the second part of the method proposed in this paper. The second part leverages the correlation between the discharge of the energy stored in the SM capacitors and the increase of the fault current; MMC SMs are temporarily bypassed whenever the fault current exceeds a preset threshold. Note that there are no fault detection signals or associated triggering delays in either of the two parts of the proposed method. In addition, both methods have no impact on the normal operation of MMCs.

The rest of the paper is organized as follows. Section II describes the system under study and shows the limitation of using large DC reactors for DC fault ride-through (FRT). Sections III and IV present the two current-limiting functions and their designs. Section V validates the effectiveness of the proposed fault current-limiting method by demonstrating its performance on a four-terminal meshed HVDC test system simulated in PSCAD/EMTDC. Section VI concludes the work.

2 Bipolar MMC-Based MTDC System

2.1 System Under Study

The proposed fault current-limiting control method is demonstrated on the system shown in Fig. 1, which is a bipolar HB-MMC-based four-terminal radial system. The MMC stations 1 and 2 are operated in DC voltage droop control mode, and the MMC stations 3 and 4 are operated in constant power control mode; stations are denoted as C_1 to C_4, respectively. Each station contains two MMC converters, "Cp" and "Cn," one connected to a positive pole and one to a negative. C1 and C3 are connected to each other by a 150-km-long export cable, whereas C2 and C4 are connected to each other by a 225-km-long export cable. C1 and C2 are also connected to each other by a 75-km-long interlinking cable. C1 and C3 are assumed to be offshore stations integrating two offshore wind power plants. They supply power to the onshore stations C2 and C3 through the two export cables. A smoothing reactor of 10 mH is placed in between the converter and the DC bus to filter the converter noise, whereas hybrid DCCBs with constant DC reactors of 50 mH are placed in series at both ends of all the DC cables to limit the rate of rise of the fault currents and slow the voltage collapse. The parameters of the MMC and associated AC systems are presented in Table 1.

Table 1 Parameters of Four-Terminal HVDC Systems

Parameters	$C_{1p,n}$	$C_{2p,n}$	$C_{3p,n}$	$C_{4p,n}$
Rated DC-side voltage (kV)	± 500	± 500	± 500	± 500
Tx primary voltage (kV)	110	110	525	525
Tx secondary voltage (kV)	260	260	260	260
Tx leakage inductance (pu)	0.15	0.15	0.15	0.15
Rated active power (MW)	750	750	1500	1500
Arm reactor (mH)	40	40	40	40
SM capacitance (μF)	15000	15000	30000	30000
# of SMs per arm	100	100	100	100
IGBT blocking threshold (kA)	3	3	3	3

In [5], three HVDC grid FRT scenarios are defined based on different numbers of MMCs allowed to be blocked following a DC fault, and they are termed as “DC-FRTS." DC-FRTS1 requires that none of the MMCs should be blocked after a fault occurs. Under DC-FRTS2, local MMCs can be temporarily blocked during a DC fault, but remote MMCs are not permitted to block and must maintain continuous operation. (Note that a local MMC refers to the MMC that is separated from the fault location by only one cable, one DCCB, and one DC bus; and a remote MMC is defined as the MMC separated from the fault location by at least two cables, two DCCBs, and two DC buses [5].) DCFRTS3 permits the temporary blocking of all MMCs during a DC fault. This work focuses on DCFRTS2, where limiting the rate of the rise of the fault current is crucial to:

- Allow sufficient time for the protection system (such as DCCBs) to detect and interrupt faults on the faulted cable.
- Avoid blocking remote MMCs connected to healthy cables.
- Prevent large fault currents from damaging components, and benefit the design and investment of protection equipment by enabling smaller and lower-rated components.

2.2 DC Reactors for Limiting Fault Currents

Based on the simplified model of a DC fault current provided in [6], the DC fault current of a pole-to-ground fault in a bipolar system can be approximated by:

$$\bar{i}_{dc}(t) \approx \frac{2dNv_c(t_0)}{L_{eq}}t + i_{dc}(t_0) \qquad (1)$$

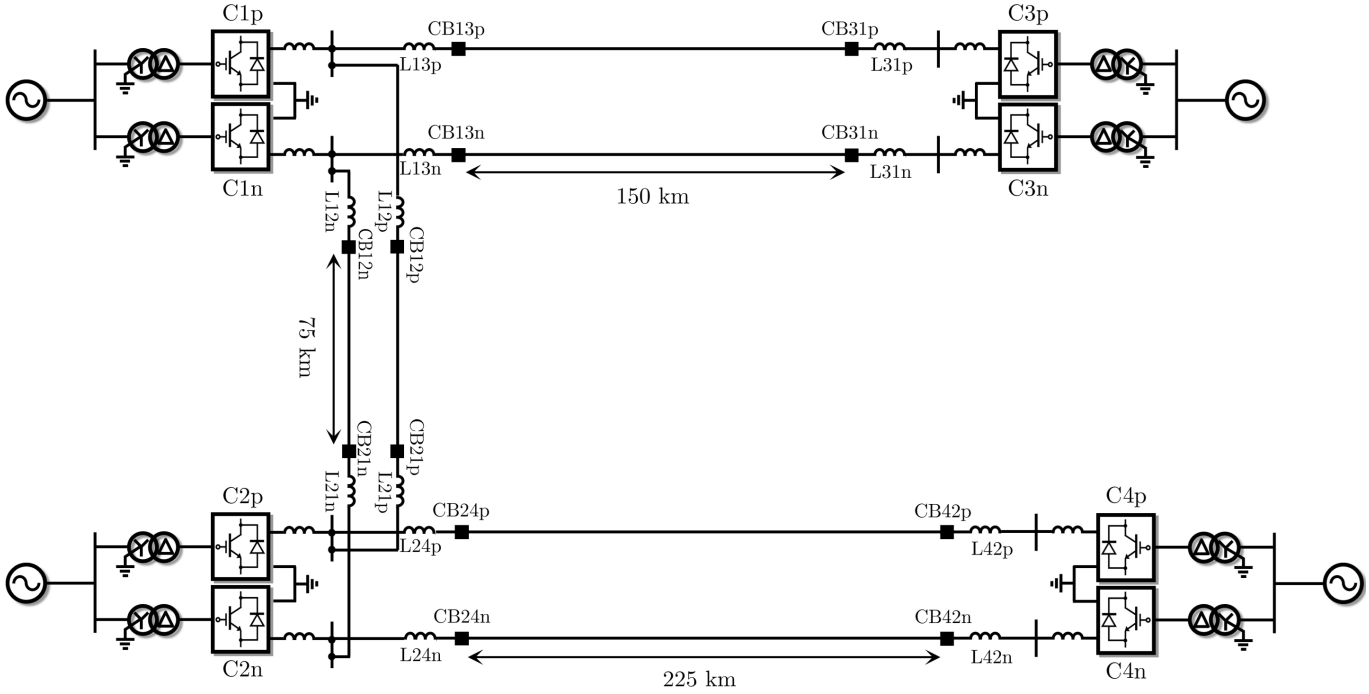

Fig. 1. Diagram of the system under study

where $i_{dc}(t_0)$ and $v_c(t_0)$ are the initial DC current and SM capacitor voltages before the fault occurs, respectively; N represents the total number of SMs per arm; d denotes the duty ratio, which is the ratio between the amount of inserted SMs and the total number of SMs per phase; and L_eq is given by:

$$L_{eq} = \frac{2}{3}L_0 + L_{dc} + L_{lim} + L_{line} \tag{2}$$

where L_0, L_{dc}, L_{lim}, and L_{line} represent the inductance of MMC arm, DC smoothing reactor, current-limiting reactor, and the line between the fault location and the converter station, respectively.

As indicated by (1) and (2), the most straightforward way to limit the fault current is to increase the value of the current-limiting reactor, L_{lim}, included in L_{eq}, which is a commonly used approach in existing MTDC system [7]. For instance, in the Zhangbei HVDC grid in China, a 300-mH current-limiting reactor is employed to prevent MMCs from blocking after a pole-to-ground fault; however, in addition to increasing the land use and investment costs, a large current-limiting reactor can also reduce the dynamic response speed of the system and cause instability [8]. Further, unwanted oscillations can also occur in the voltages and currents after the faulted cable is isolated from the DC network, which are hereafter referred to as post-fault oscillations in this work. The critical issue with these post-fault oscillations is that even though a large current-limiting reactor effectively limits the peak value of the fault current below the SM blocking threshold before the DC fault clearance, the peak value of the post-fault oscillatory currents can still exceed the threshold and block the MMCs.

To better show the post-fault oscillatory behavior of the DC current and its impact on DC FRT, simulation of an illustrative case based on Fig 1 are performed. In the simulation, a permanent positive pole-to-ground fault is applied right after CB13p at $t = 2$ seconds. To ensure FRT, the DC currents of C2p and C4p must be limited to below 3 kA prior to the fault clearance (i.e., CB21p opening). To achieve this, an additional 300-mH DC reactor is installed at the DC outlet of both C2p and C4p. To more clearly illustrate the dynamic behavior of the MMC's DC currents following the fault clearance, CB24p and CB24n remain closed throughout the simulation, and the blocking threshold for converter C2p and C4p is set to 6 kA to prevent them from blocking after the fault clearance. The simulated response of i_{C2p} is shown in Fig. 2.

Approximately 5 ms after the fault occurs, the DC current of C2p begins to decay as a result of the opening of CB21p; however, right after CB21p has fully opened (1 ms later), the current exhibits a damped oscillation,

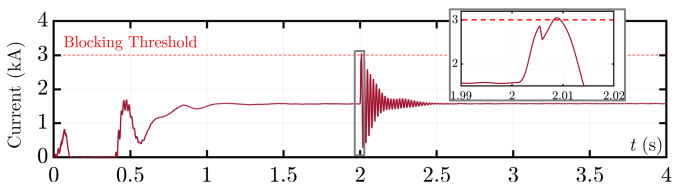

Fig. 2 Illustrative case demonstrating the MMC DC current oscillation after a fault clearance

with the oscillation peak reaching as high as 3.05 kA. In this simulation, if the blocking threshold for C2p is kept at 3 kA, C2p would be blocked after the fault clearance due to the post-fault oscillation, resulting in the failure of the ride-through of the DC fault as well as the loss of the power transfer of both export cables. The root cause of the post-fault oscillation is the LC resonance formed by the DC reactor with large inductance and the DC cable with high capacitance. The frequency and amplitude of this LC oscillation vary with the selected DC reactor and the DC cable capacitance, and such oscillations are generally unavoidable in HVDC systems using cables; therefore, an active fault current-limiting method is required to avoid using large DC reactors.

3 Virtual Impedance-Based Current-Limiting Control

3.1 Basic Principle

Fig. 3 shows the block diagram when a virtual impedance-based current-limiting control (delineated in red) is used in conjunction with circulating current suppressing control (CCSC). The idea of circulating current feedforward is to introduce a term in the output of CCSC that represents a DC voltage drop across a virtual arm inductor. To extract the DC component from the circulating current and to make the derivative term less sensitive to high-frequency components, a first-order low-pass filter with low bandwidth is connected in series with sK_v. The resulting feedforward gain of the circulating current can thus be given by:

$$H_{vi}(s) = \frac{sK_v\omega_c}{s+\omega_c} \tag{3}$$

where ω_c represents the cuttoff frequency of the first-order low-pass filter.

Note that during the steady-state operation of the MMC, the DC component of the circulating current remains virtually constant, making the output of $H_{vi}(s)$ negligible because the derivative of a constant is 0. In other words, this virtual impedance-based current-limiting control does not impact the normal operation of the MMC. When the DC current undergoes a significant change during DC fault, however, the virtual reactance, $sK_v/2$, is immediately inserted into each arm, which resists the rise of the fault current.

As shown in (3), there are two parameters that need to be designed, which will be detailed in the sequel. One is

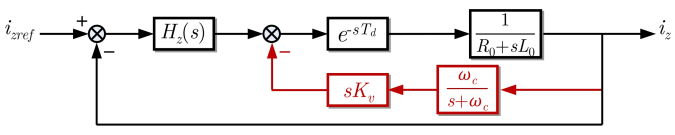

Fig. 3 Block diagram of circulating current feedback and feedforward control

ω_c, which determines the bandwidth of the low-pass filter and the small-signal stability of the MMC's DC side; the other is K_v, which determines the ability of the virtual impedance-based control to limit the fault current.

3.2 Parameter Design of K_v and ω_c

The circulating current feedforward, as depicted in Fig. 3, is equivalent to adding a derivative term to the compensator of the CCSC, which could affect the loop stability of the CCSC. To avoid interference between the feedforward and feedback loops, ω_c can be selected to be a small value (e.g., one-tenth of the bandwidth of the CCSC). By doing so, the design of K_v does not need to account for the impact of the circulating current feedforward loop on the stability of the CCSC. In this work, the bandwidth of the CCSC is 100 Hz; thus, ω_c can be chosen to be below 10 Hz.

For the fault current-limiting performance, the design prefers a large k_v, but k_v is limited by the loop stability. Based on Fig. 3, the loop gain of the circulating current feedforward loop can be expressed as:

$$G_{vi}(s) = K_v\omega_c \frac{1}{R_0+sL_0}\frac{s}{s+\omega_c}e^{-sT_d}. \tag{4}$$

Given specific values for ω_c and T_d, the maximum value of K_v must be set to that corresponding to a phase response of $G_{vi}(s) = -150°$ at the crossover frequency. Consequently, the upper limit of $K_{v,max}$ can be determined by solving:

$$\begin{cases} \omega_{cross} = \mathsf{FindRoot}[G_{vi}(j\omega) = 0] \\ K_{v,max} = \mathsf{FindRoot}[|G_{vi}(j\omega_{cross})| = 1] \end{cases} \tag{5}$$

where FindRoot denotes the solution of the roots of the polynomial, which can be programmed in any available numerical computing environment.

3.3 Effect on System Stability

In the high-frequency range, the low-pass filtering effect of the SM capacitors significantly attenuates the effect of the inherent MMC controller as well as the frequency coupling effect, so the SM of MMC can be treated as an ideal voltage source; therefore, the DC impedance of the MMC with virtual impedance-based current-limiting control can be simply modeled as:

$$Z_{dc}(s) = \frac{2}{3}sL_0 + \frac{2}{3}\frac{sK_v\omega_c}{s+\omega_c}e^{-sT_d} \tag{6}$$

As mentioned before, ω_c is typically set as a relatively small value (e.g., 5 Hz) to avoid loop interference; thus, s and $(s+\omega_c)$ can be cancelled out at high frequencies, which yields:

$$Z_{dc}(s) = \frac{2}{3}sL_0 + \frac{2}{3}K_v\omega_c e^{-sT_d} \tag{7}$$

(7) indicates that the virtual impedance-based current-limiting control results in negative damping on the DC

impedance of the MMC in the frequency range where e^{-sT_d} turns negative. To avoid instability of the MMC, a simple method is to add a second-order low-pass filter in series with the virtual impedance control loop. With the added low-pass filter, the DC impedance of the MMC can be modeled by:

$$Z_{dc}(s) = \frac{2}{3}sL_0 + \frac{2}{3}K_v\omega_c\frac{\omega_b^2}{s^2 + 1.414\omega_b s + \omega_b^2}e^{-sT_d} \quad (8)$$

Fig. 4 plots the DC impedance responses of the MMC with selections of K_v varying between 0.03, 0.05, and 0.1. In this case, the MMC control delay is fixed to 200 μs and $\omega_c = 2\pi 5$. For comparison, the impedance responses with a 1000-Hz (i.e., $\omega_b = 2\pi 1000$) second-order low-pass filter are also included. The results show that after the second-order low-pass filter is applied, the negative damping is limited within approximately 1 kHz, which helps the MMC to avoid system resonance at higher frequencies. On the other hand, the value of $K_v\omega_c$ will determine the amount of negative damping at different frequencies within the negative damping region. As a result, the design of K_v and ω_c as well as ω_b should carefully consider the system resonance conditions.

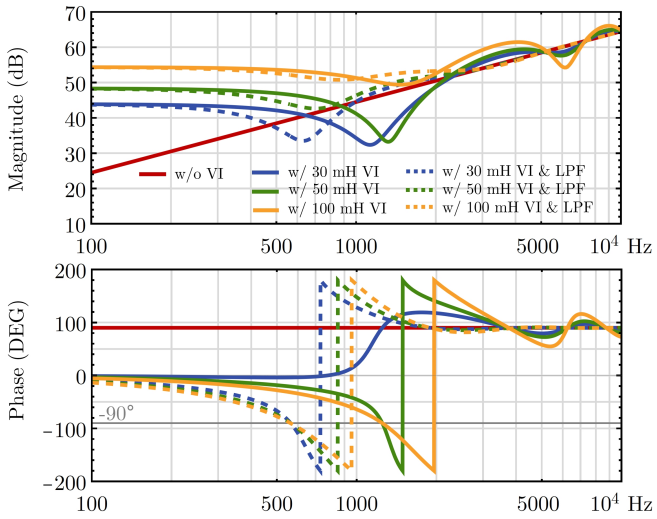

Fig. 4 Effects of virtual impedance control on MMC DC impedance in the high-frequency range

4 SM Bypassing-Based Supplementary Current-Limiting Control

As discussed in Section III, the design and performance of the virtual impedance-based current-limiting control are constrained by the loop stability and the DC system stability. Therefore, relying solely on current limiting based on virtual impedance may not be sufficient to prevent SM blocking in the MMC under certain fault conditions (e.g., a fault occurs very close to the converter station). In addition, virtual arm impedance can only reduce the rate of rise of the fault current and cannot change the peak value of the fault current. Before the fault is cleared (i.e., before the DCCB successfully isolates the faulted part of MTDC system from the healthy part), the fault current may continue to rise and exceed the blocking threshold. As a further enhancement of the DC FRT capability of the MMC, this section proposes a current-limiting method that bypasses SMs, which can be used in addition to virtual impedance-based control when the current-limiting performance of virtual impedance-based control is restricted.

4.1 Basic Principle

Fig. 5 shows the block diagram of the control, where i_{dc} is the DC output current of the MMC; K_d represents the percentage of SMs bypassed, which is between 0 and 1; v_j^* and v_z^* means the reference voltage generated by the AC current/voltage controller and the circulating current controller, respectively; V_c is the rated capacitor voltage per arm; and N_{pj} and N_{nj} indicates the amount of SMs being inserted in the upper and lower arms, respectively.

The proposed method works as follows:

- During startup and steady-state operation, i_{dc} remain below I_{max}, ensuring that the output of the switch block in Fig 5(a) is zero. This results in $K_\triangle$ being zero. Consequently, all SMs will participate in modulation according to the insertion sequence defined by the sorting algorithm.
- When the fault current reaches a level higher than I_{max}, the hysteresis buffer makes the switch block pass through 1; therefore, $K_\triangle$ is determined by (1-K_d), which decreases the number of SMs to be inserted during the modulation process.
- Due to the SMs being bypassed, the fault current will immediately decrease. Once the fault current drops below I_{min}, the fault is considered cleared, and the modulation process returns to normal.

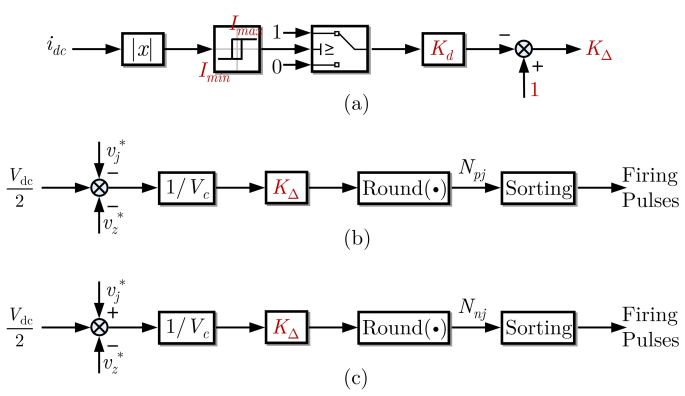

Fig. 5 (a) block diagram of the SM bypassing scheme. Implementation of the bypassing in modulation of: (b) the upper arm and (c) the low arm

- If the fault persists within the system, the MMC will discharge again, causing the fault current to continue rising. Once it exceeds I_{max}, the SM bypassing process will repeat until the fault is cleared.

4.2 Parameter Design of I_{min} I_{max} and K_d

4.2.1 I_{max}: I_{max} determines when the SM bypassing is activated. Because the SM bypassing could lead to a drop in the DC voltage and an overcurrent in the AC side [1], it is preferable to avoid using SM bypassing-based current-limiting control whenever possible; therefore, this control should be activated as late as possible, and the value of $_{max}$ is typically set between 90% and 95% of the IGBT blocking threshold.

4.2.2 I_{min}: I_{min} determines the duration of the SM bypassing state. The smaller the I_{min}, the longer the bypassing process will last. This prolongs the duration of the DC undervoltage and the AC overcurrent, which could trigger DC undervoltage protection and AC overcurrent protection. If the difference between I_{min} and I_{max} is too small, however, the modulation will frequently switch between the normal SM insertion state and the SM bypassing state before the DC fault is isolated from the system by the DCCB. This could potentially increase the switching losses of SMs.

4.2.3 K_d: K_d determines the number of bypassed SMs. The more SMs that are bypassed, the more severe the resulting DC-side undervoltage and AC-side overcurrent; however, if the number of bypassed SMs is insufficient, the current-limiting effect could be weakened, potentially leading to MMC blocking. Because I_{max} is selected to be a value close to the MMC blocking threshold, K_d can be set to 1, ensuring the effectiveness of the SM bypassing-based current-limiting control.

5 Case Study and Simulation Validation

5.1 Simulation Setup

The four-terminal radial HVDC test systems shown in Fig. 1 is used for the simulation validation, in which the development of models for HVDC converters follows the guidelines outlined in [9], whereas the frequency-dependent cable model is modeled following the parameters and configuration given in [3].

To more clearly demonstrate the contribution of the proposed fault current-limiting method to FRT, the simulation is settled as follows: 1) A positive pole-to-ground fault is applied right after CB13p when $t = 2$ seconds, and it is a permanent fault. 2) DCCBs are triggered based on the threshold, with its value set equal to the MMC blocking threshold, which is 3 kA. 3) The modulation delay of the MMC is considered, but the additional control delay and the second-order low-pass filter are ignored. 4) Because the MMC C1P and C3P are blocked after the fault occurs, their simulated responses are omitted. 5) Because the positive and negative poles can operate independently, the simulation results for the negative pole will not be shown. 6) The parameters of the virtual impedance-based and SM bypassing-based current-limiting controls are tabulated in Table 2.

Table 2 Design of Active Fault Current-Limiting Control

Parameter	Symbol	Value
Cutoff frequency of the 1^{st}-order LPF	f_c	5 Hz
Virtual arm reactor per leg	K_v	100 mH
Hysteresis switch-on point	I_{max}	2.8 kA
Hysteresis switch-off point	I_{min}	1.75 kA
Percentage of bypassed SMs	K_d	100%

The simulations are conducted under the following three cases:

- Case 1: No active fault current-limiting control is implemented, and the fault current limitation is solely dependent on the 50-mH DC reactor at the cable terminal.
- Case 2: The virtual impedance-based control is equipped, and the SM bypassing-based scheme is disabled.
- Case 3: Both current-limiting functions are implemented.

5.2 Simulation Results

Fig. 6(a) and (b) show the DC current injected by the MMC C2p into the DC network. As shown, when there is no active fault current-limiting control and only a 50-mH current limiting reactor is placed, the DC current reaches the SM blocking threshold within 2 ms, causing the MMC C2p to block immediately after the SM blocking delay. After the MMC C2p is blocked, the DC fault current continues to increase until it is interrupted by CB21 at approximately 2.0045 seconds. As a result, relying solely on a 50-mH DC reactor does not allow for the DC FRT.

In Case 2, when virtual impedance-based control is employed, the rise in the fault current is significantly suppressed after the fault occurs. In this case, CB21 trips 4.6 ms after the fault occurs. The virtual impedance control effectively limits the fault current to below 3 kA before 2.0046 seconds. As a result, the lower export cable of the four-terminal HVDC system can successfully ride through the DC fault on the upper export cable; however, it is noteworthy that in Fig. 6(b), the peak value of the DC current reaches approximately 2.976 kA, which is very close to the blocking threshold. In practice, any potential disturbance could cause the actual fault current to be greater than the simulated responses in PSCAD, leading to MMC blocking. To ensure a sufficient current margin, supplementary control based on SM bypassing is necessary.

As shown in Case 3, when the fault current reaches the switch-on point of the hysteresis buffer, 2.8 kA, the bypassing function is immediately triggered, which

changes $K_{\triangle}$ from 1 to 0, thereby bypassing all the SMs. By doing so, the DC current decreases to 1.75 kA within approximately 200 μs, and the SMs are then inserted as normal operation. Because the fault location has not been isolated from the system, SMs of MMC C2p discharges again, and the DC current of MMC C2p increases as a consequence. At 2.0031 seconds, however, the DC current starts to decay due to the opening of CB12. Following the disconnection of CB21 at 2.0046 seconds, the DC current starts to return to its steady-state value.

The DC pole-to-ground voltage of the MMC C1p (denoted as V_{C1p} in Fig. 1) is plotted in Fig. 6(c) and (d). It is evident that in Case 3, during the temporary bypassing of all the SMs, there is a significant voltage sag in V_{C1p}.

Due to the logic of the proposed bypassing scheme, the insertion of the SMs switch back to normal when the DC current of MMC C1p drops to 1.75 kA, so the duration of this voltage sag is relatively short; however, this could still trigger the low-voltage protection, and thus it should be evaluated based on the corresponding DC low-voltage ride-through profile of the DC system. As a result, it is important to set the hysteresis switch-off point properly, accounting for the system's allowable minimum DC voltage and the duration of the voltage sag.

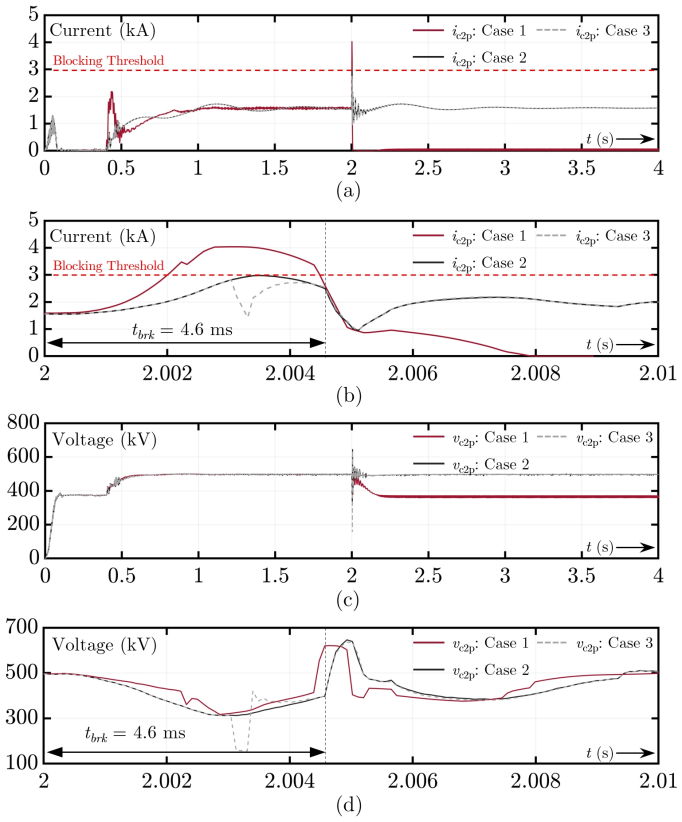

Fig. 6 (a) DC current injected by MMC C2p; (b) zoom-in view of (a) between 2 and 2.01 seconds; (c) positive pole-to-ground voltage measured at the DC outlet of MMC C2p; (d) zoom-in view of (c) between 2 and 2.01 seconds

6 Conclusions

This paper presents a novel adaptive fault current-limiting strategy that includes virtual arm impedance control and submodule temporary bypassing scheme. The former is designed to reduce the rate of rise of the DC fault current, while the latter complements it by preventing the fault current peak from exceeding the MMC blocking threshold. The proposed method offers a reliable solution to prevent the MMCs on healthy parts of the MTDC network from blocking during DC fault, enhancing the MTDC system's ability to ride through DC faults. In addition, it helps MMCs avoid post-fault oscillations that are associated with using large DC reactors to limit fault current. A pole-to-ground fault in a bipolar MMC-HVDC-based four-terminal radial system is simulated in PSCAD/EMTDC, and the simulation results demonstrate the effectiveness of the proposed method in limiting the fault current and facilitating the DC FRT of MMCs in healthy parts of the DC network.

7 Disclaimers and Statements

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