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High-Performance, 0.6-eV, $GA_{0.32}In_{0.68}As/In_{0.32}P_{0.68}$ Thermophotovoltaic Converters and Monolithically Interconnected Modules

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Abstract. Recent progress in the development of high-performance, 0.6-eV $Ga_{0.32}In_{0.68}As/InAs_{0.32}P_{0.68}$ thermophotovoltaic (TPV) converters and monolithically interconnected modules (MIMs) is described. The converter structure design is based on using a lattice-matched $InAs_{0.32}P_{0.68}/Ga_{0.32}In_{0.68}As/InAs_{0.32}P_{0.68}$ double-heterostructure (DH) device, which is grown lattice-mismatched on an InP substrate, with an intervening compositionally step-graded region of $InAs_yP_{1-y}$. The $Ga_{0.32}In_{0.68}As$ alloy has a room-temperature band gap of ~0.6 eV and contains a p/n junction. The $InAs_{0.32}P_{0.68}$ layers have a room-temperature band gap of ~0.96 eV and serve as passivation/confinement layers for the $Ga_{0.32}In_{0.68}As$ p/n junction. $InAs_yP_{1-y}$ step grades have yielded DH converters with superior electronic quality and performance characteristics. Details of the microstructure of the converters are presented. Converters prepared for this work were grown by atmospheric-pressure metalorganic vapor-phase epitaxy (APMOVPE) and were processed using a combination of photolithography, wet-chemical etching, and conventional metal and insulator deposition techniques. Excellent performance characteristics have been demonstrated for the 0.6-eV TPV converters. Additionally, the implementation of MIM technology in these converters has been highly successful.

INTRODUCTION

TPV converters that use low-band-gap, epitaxial $Ga_xIn_{1-x}As$ alloys grown on InP substrates have been under investigation by a number of groups in recent years [1]. Additionally, substantial progress has been made in developing MIMs from similar TPV converter structures [1]. In this paper, we describe recent progress at NREL in the development of both discrete converters and MIMs with a band gap of 0.6 eV.

Low-band-gap (0.5–0.6 eV) $InAs_yP_{1-y}/Ga_xIn_{1-x}As/InAs_yP_{1-y}$ DH TPV converters have been under development at NREL since 1993. The DH converter concept is based on using high-band-gap layers of $InAs_yP_{1-y}$ to effect passivation and minority-carrier confinement when applied to the front and back surfaces of a low-band-gap $Ga_xIn_{1-x}As$ p/n-junction absorber. A full description of this concept, and the experimental demonstration of its utility, are given elsewhere [2]. The DH structure provides higher photovoltaic (PV) performance because it reduces minority-carrier recombination and, thus, results in both a higher quantum efficiency and lower reverse-saturation current density for the converter. Similar DH designs have been used to produce high-efficiency solar PV converters in III-V materials that have high surface-recombination velocities (e.g., solar cells based on the lattice-matched combinations $Ga_{0.52}In_{0.48}P/GaAs$, $Al_xGa_{1-x}As/GaAs$, and $InP/Ga_{0.47}In_{0.53}As$). At 300 K, $Ga_{0.47}In_{0.53}As$ is lattice matched to InP and has a band gap of 0.74 eV. Therefore, TPV converters using $Ga_xIn_{1-x}As$ epilayers grown on InP require mismatched epitaxy in order to produce the lower band gaps (0.5–0.6 eV) necessary for optimal conversion efficiency. The problems that arise from the lattice mismatch between the substrate and the converter epilayers are mitigated by including intervening compositionally graded layers in the converter structure. In the past, continuous, linearly graded regions of $Ga_xIn_{1-x}As$ have been used to produce converters with excellent performance characteristics [2, 3]. In the recent work described here, we have found that properly designed $InAs_yP_{1-y}$ step-graded regions give even better results.

To a good approximation, the band gap (E_g) of $Ga_xIn_{1-x}As$ as a function of x at 300 K is given by the following expression [4],

$$E_g(x) = (0.555x^2 + 0.505x + 0.356)\text{eV}, \tag{1}$$

which yields x = 0.35 for E_g = 0.6 eV. Our experience with $Ga_xIn_{1-x}As$ epilayers shows that this value of x is somewhat high; experimentally, we have found that x ≈ 0.32 is the correct value to attain E_g = 0.6 eV (2067 nm). The lattice mismatch (M) between a $Ga_xIn_{1-x}As$ epilayer and an InP substrate is given precisely by [2]

$$M(Ga_xIn_{1-x}As/InP) = \left(\frac{-0.378 + 0.810x}{11.927 - 0.405x}\right). \tag{2}$$

Thus, M = -1.01% for x = 0.32, where the minus sign indicates that the $Ga_xIn_{1-x}As$ epilayer experiences biaxial compression, a condition that maintains the integrity of the $Ga_xIn_{1-x}As$ (i.e., no microcracking within the epilayer). The lattice-matching condition for epilayers of $InAs_yP_{1-y}$ and $Ga_xIn_{1-x}As$ is expressed exactly by [2]

$$y = 1 - 2.143x. \tag{3}$$

This equation yields y ≈ 0.32 for x ≈ 0.32. We have found close lattice-matching between the $Ga_xIn_{1-x}As$ and $InAs_yP_{1-y}$ epilayers to be of paramount importance, particularly when $InAs_yP_{1-y}$-graded layers are used. Otherwise, microcracks in the epistructure have been observed, which occur, presumably, as a result of the strain between the two ternaries. The band gap of $InAs_yP_{1-y}$ at 300 K is best expressed as [5]

$$E_g(y) = (0.320y^2 - 1.315y + 1.351)eV, \quad (4)$$

which gives E_g = 0.96 eV for y = 0.32.

The above parameters define the 0.6-eV $InAs_{0.32}P_{0.68}/Ga_{0.32}In_{0.68}As$ DH TPV converter design concept. Further details of the actual converter structures are outlined in the sections that follow. It should be noted that the basic $InAs_yP_{1-y}/Ga_xIn_{1-x}As$ DH converter design can be used to achieve a wide range of band gaps; recently, we demonstrated high-performance 0.5-eV converters using this concept. In the remainder of this paper, we describe the results obtained from fabricating 0.6-eV discrete converters and MIMs.

EPITAXIAL GROWTH and DEVICE FABRICATION PROCEDURES

The APMOVPE process used in this work employs an NREL-built gas-handling system and a specially designed, vertically oriented reactor vessel [6] that yields highly uniform epilayers. InP substrates (prepared with an "epi-ready" surface), which were oriented (100) 2° toward (110), were loaded directly into the reactor for growth as received from the vendor. Discrete converters were grown on polished/etched S-doped InP substrates, and MIM structures were grown on double-side-polished (DSP), Fe-doped InP substrates. Ethyldimethylindium, triethylgallium, arsine, and phosphine were used as the primary reactants, and diethylzinc and hydrogen sulfide were used to dope epilayers p- and n-type, respectively. Epitaxial growth was performed in a purified hydrogen ambient at a temperature of 620°C. The deposition rates were 0.1 $\mu mmin^{-1}$ for $Ga_{0.32}In_{0.68}As$ and 0.07 $\mu mmin^{-1}$ for $InAs_{0.32}P_{0.68}$. A detailed description of the APMOVPE system and growth process is given elsewhere [2].

Conventional procedures were used to process devices. Selective wet-chemical etching was performed using 3 H_3PO_4 : 4 H_2O_2 : 1 H_2O to dissolve $Ga_{0.32}In_{0.68}As$ and concentrated HCl to dissolve $InAs_yP_{1-y}$. Electroplated Au was used to form the metallizations on the discrete converters. Our general approach to fabricating MIMs has been described previously [7]. The insulator used in MIM fabrication is SiO_2 (~200 nm) deposited by a chemical-vapor-deposition process. The metallization used for the MIMs is an electron-beam-evaporated multi-metal stack consisting of Cr (30

nm), Pd (20 nm), Ag (4 μm), and Pd (20 nm). The optimized back-surface reflector (BSR), which is applied to the back surface of MIM converters, consists of MgF_2 (130 nm), Ti (2.5 nm), and Au (150 nm). The characteristics of front and back electrical contacts used in the MIMs are discussed in a companion paper given at this conference [8].

DISCRETE CONVERTERS

Discrete converters were fabricated using the epistructure shown in Figure 1. From the substrate up, the basic components of the structure include an $InAs_yP_{1-y}$ step-graded layer, the 0.6-eV DH converter layers, and a contact layer to facilitate contacting the front surface. Details of the composition, doping level, and thickness for each of the component layers in the structure are given in the diagram. Design rules derived from a previous study of lattice-mismatched $GaAs_{1-z}P_z$/GaAs structures [9] were used to guide the design of the graded layer used in the present TPV converters. The $InAs_yP_{1-y}$ graded layer consists of 10 equal compositional steps, which results in a lattice mismatch of -0.1% at each step interface. The grade is terminated with a layer of constant composition ($InAs_{0.32}P_{0.68}$) that is 1 μm in thickness. This thicker layer allows the final network of misfit dislocations arising from the last compositional step to evolve fully, leaving only a relatively low density of threading dislocations to propagate into the active converter layers above. As shown later, this grading technique results in converter layers with excellent electronic characteristics. For the reasons that follow, the total thickness of the $Ga_{0.32}In_{0.68}As$ p/n junction layers of the DH converter (2.3 μm) is about half the thickness required for complete absorption of above-band-gap-energy photons. Firstly, the converter structure is designed for eventual use as a MIM, where a BSR is available to reflect unabsorbed near-band-gap-energy photons back through the converter layers for a second pass. Secondly, thinner p/n-junction layers result in lower reverse-saturation current densities, which, in turn, result in higher converter voltages (~18 mV higher for half the thickness, at 300 K). Finally, thinner layers require less growth time, which is a potential manufacturing advantage. A range of thicknesses (0.1–0.3 μm) have been used for the p^+-$Ga_{0.32}In_{0.68}As$ emitter layer in the DH converter.

The microstructure of the 0.6-eV converters was characterized using atomic-force microscopy (AFM), cross-sectional transmission electron microscopy (XTEM), and electron-beam-induced current (EBIC) techniques. To the naked eye, the surface of the structure appears to have a fine, orthogonal, biaxial crosshatched morpology, which is typical of single-crystal, lattice-mismatched III-V epilayers grown on substrates with a near-(100) orientation [9]. Detailed examinations of the surface topography by AFM show that a three-dimensional ripple morphology is superimposed on the crosshatch. The root-mean-square roughness of the surface is ~23 nm. XTEM examinations show that the structures exhibit extensive misfit dislocation networks in the vicinity of the compositional steps in the graded region.

At the top of the grade, threading dislocations were observed to propagate into the DH converter layers above. Plan-view EBIC was performed on discrete devices to assess the degree of minority-carrier recombination at dislocations within the converter layers. The EBIC studies showed that carrier recombination was not occurring to any measurable degree; the threading dislocations could not be resolved as dark lines or spots. The above result has been corroborated by minority-carrier lifetime measurements, as we have observed minority-carrier lifetimes of several μs in undoped 0.6-eV DH structures [10]. The above results indicate that the grading technique used in the 0.6-eV DH structure produces converter layers with superior properties; the usual deleterious effects of threading dislocations are almost nonexistent.

Spectral quantum efficiency (QE) and reflectance (R) data for a discrete 0.6-eV DH converter without an antireflection coating (ARC) are given in Figure 2. The figure shows R, active-area absolute external quantum efficiency (AAAEQE), and internal quantum efficiency (IQE) data for a representative high-performance 0.6-eV converter. The IQE data show that the carrier collection efficiency over the bulk of the response range is excellent (~90%–100%), a result of excellent bulk-material quality and low interfacial recombination at the outer edges of the p/n-junction absorber. Again, these results corroborate the abovementioned observations made with EBIC and carrier lifetime studies. However, near the band edge of the converter, the IQE rolls off, which is a result of the thin absorber layers discussed previously. As shown later, the near-band-edge QE improves markedly when the converter structure is used in a MIM configuration with a BSR.

In Figure 3, current-voltage data for a representative discrete 0.6-eV converter under high-intensity illumination are given. The typical photovoltaic performance parameters [open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), and fill factor (FF)] are listed. For a band gap of 0.6 eV, the values of FF (73.4%) and the voltage factor (defined as V_{oc}/E_g, 0.59 V/eV) are excellent. Typical ranges for the diode ideality factors and reverse-saturation current densities for these converters [derived from $V_{oc}(J_{sc})$ analyses] are 0.95-1.05, and 5-10x10^{-7} Acm^{-2}, respectively, at a temperature of 25°C. These data illustrate that high-performance TPV converters are realized using the aforementioned design concepts.

MONOLITHICALLY INTERCONNECTED MODULES

As shown in Figure 4, the converter structure grown for MIM fabrication is virtually identical to the structure used for discrete converters, with four exceptions: 1) The InP substrate is DSP and semi-insulating (SI) (i.e., Fe-doped and transparent to sub-band-gap-energy photons); 2) The $InAs_yP_{1-y}$ compositionally graded layer is undoped (making it transparent to sub-band-gap-energy photons); 3) A 0.3-μm-thick n^+/p $InAs_{0.32}P_{0.68}$ cell isolation diode (CID) is included as part of the 1-μm-thick

$InAs_{0.32}P_{0.68}$ layer above the graded layer; 4) The thickness of the p^+-$Ga_{0.32}In_{0.68}As$ emitter layer is fixed at 0.1 μm to reduce free-carrier absorption of sub-band-gap-energy photons (empirically, we have found that p-type layers have a higher sub-band-gap-energy, free-carrier absorption coefficient). At this thickness, the p^+-$Ga_{0.32}In_{0.68}As$ emitter layer has a sheet resistance of ~1600 ohms per square. We have investigated CIDs for MIMs for the last 2 years. In the present structure, the CID serves two important functions, as follows: 1) Electrical isolation of the component cells in the MIM is achieved by etching a trench through the CID n^+/p junction with the reverse-bias characteristic of the CID preventing inter-cell shunting; 2) The depth of the isolation trench is minimized because the CID is disposed directly beneath the DH converter. This feature improves the characteristics of the cell interconnections on the MIM. In fact, the n^+-$InAs_{0.32}P_{0.68}$ layer of the CID is designed to serve several important functions, as follows: 1) It is the back-surface confinement layer for the DH converter; 2) It works as a stop-etch layer for device processing, which ensures correct placement of the back contact within the MIM structure; 3) It is also the back-contact, lateral-conduction layer for the MIM (the sheet resistance of the layer is ~50 ohms per square, which results in negligible Joule losses; 4) It is the emitter layer for the CID. In an effort to reduce free-carrier absorption of sub-band-gap photons in the MIM structure, the p-$InAs_{0.32}P_{0.68}$ layer of the CID is grown just thick enough to support the space-charge region. Overall, the CID technique has been extremely helpful in implementing MIM technology in these lattice-mismatched converter structures.

Spectral AAAEQE data (no ARC) are shown in Figure 5 for a MIM structure both with and without a BSR. The improvement in the near-band-gap response is quite significant. These data demonstrate that the BSR serves the intended purpose of improving the long-wavelength QE of optically thin DH converters.

Current-voltage data for a representative 0.6-eV, four-cell MIM operated under high-intensity illumination are given in Figure 6. The value of V_{oc} for the MIM (1.546 V) gives an average V_{oc}/cell of 0.387 V, which yields a voltage factor of 0.64 V/eV. These data also show that the CID provides excellent electrical isolation between the component cells in the MIM. The FF value (66.1%) can probably be improved somewhat through an optimization of the epistructure/metallization design. If we assume that the IQE data shown in Figure 2 are a good approximation to the AEQE of this MIM with an optimized ARC applied, then the data shown in Figure 6 correspond to operation of the MIM under an ideal blackbody radiator at a temperature of 1027°C. Under these conditions, the maximum power density generated by the MIM is 1.07 Wcm^{-2}, which is an excellent level of performance.

High-reflectance BSRs are necessary for efficient recuperation of sub-band-gap-energy photons in order to achieve high TPV system-conversion efficiencies. Full details of BSR optimization and fabrication are given in a companion paper at this conference [8]. Additionally, sub-band-gap energy free-carrier absorption within the

MIM structure must be as low as possible to maintain efficient recuperation. Long-wavelength, spectral total reflectance data for an as-grown, 0.6-eV MIM structure (no metallization) with an optimized BSR are shown in Figure 7. The data show that high reflectances (80%–90%) are achieved for wavelengths ranging from 2 to 12 μm, which indicates that the BSR has a high reflectance and that the free-carrier absorption of sub-band-gap energy photons is low.

CONCLUSION

A 0.6-eV, $InAs_{0.32}P_{0.68}/Ga_{0.32}In_{0.68}As$ DH TPV converter structure has been described that employs an $InAs_yP_{1-y}$ step-graded layer to produce converter layers with superior electronic properties. The DH design yields TPV converters with high quantum efficiencies and low reverse-saturation current densities. High-performance, 0.6-eV discrete converters and MIMs have been demonstrated with this structure.

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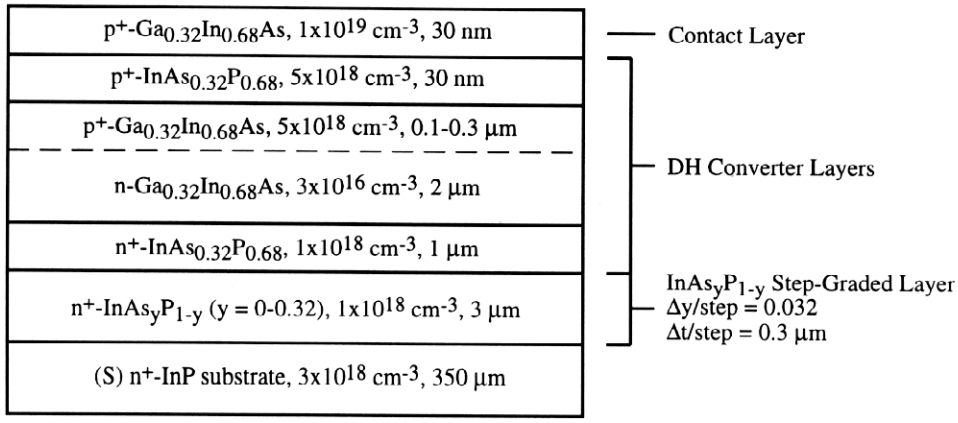

FIGURE 1. Schematic cross-sectional diagram of the epistructure used for the fabrication of discrete 0.6-eV TPV converters.

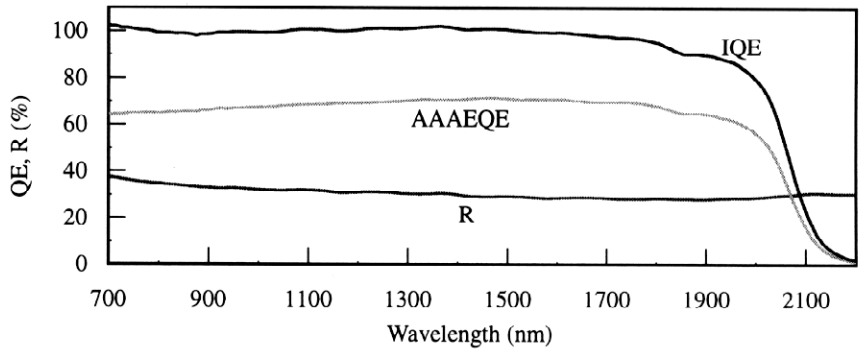

FIGURE 2. Spectral quantum efficiency and reflectance data for a discrete 0.6-eV TPV converter.

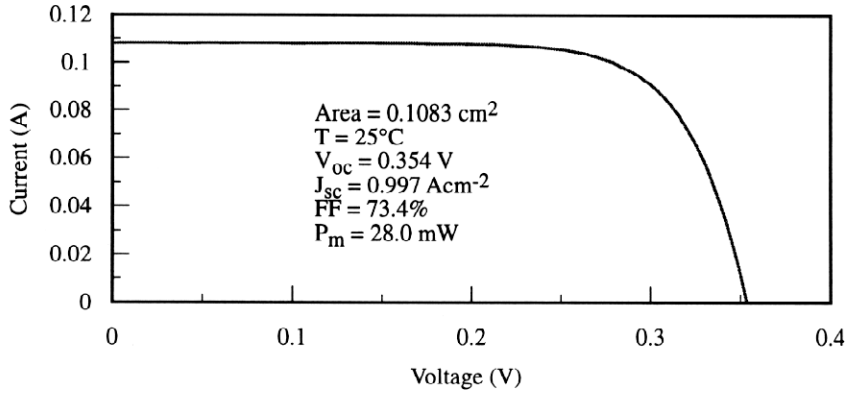

FIGURE 3. Current-voltage data for a discrete 0.6-eV TPV converter under high-intensity illumination.

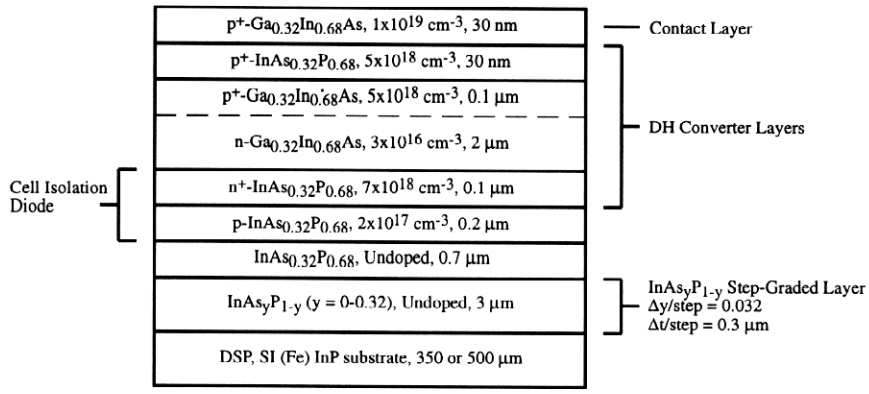

FIGURE 4. Schematic cross-sectional diagram of the epistructure used for 0.6-eV MIM fabrication.

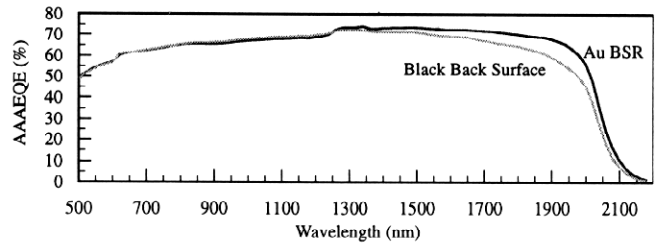

FIGURE 5. Spectral AAAEQE data for a 0.6-eV MIM both with and without a BSR.

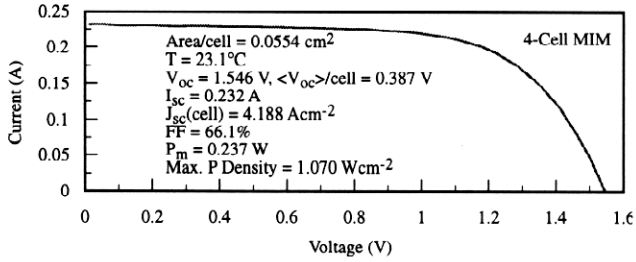

FIGURE 6. Current-voltage data for a 0.6-eV MIM under high-intensity illumination.

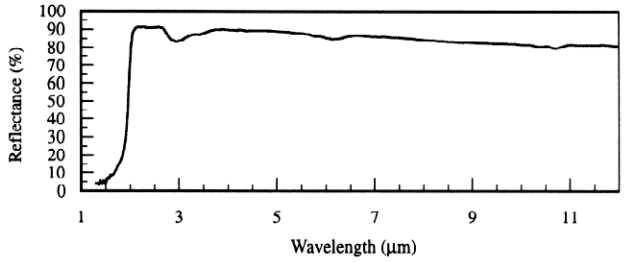

FIGURE 7. Long-wavelength spectral reflectance data for a 0.6-eV MIM converter structure with a BSR.