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Development of a Thin-Film Crystalline-Silicon Solar Cell

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Abstract. A new design for a single junction, thin film Si solar cell is presented. The cell design is compatible with low-temperature processing required for the use of a low-cost glass substrate, and includes effective light trapping and impurity gettering. Elements of essential process steps are discussed.

INTRODUCTION

Thin-film Si solar cells offer many advantages, including a lower cost, potential for high efficiency with lower material quality, and use of smaller quantities of silicon, compared to a wafer-based cell of the same material quality. The major advantages of a thin Si cell come from a reduced recombination of carriers in the bulk that leads to a higher open-circuit voltage (V_{oc}) and a higher fill factor (FF). To fully exploit the advantage of the low recombination, the material quality must be such that its minority-carrier diffusion length is at least twice the cell thickness. Meeting these advantages creates several challenges for both the cell design and its fabrication. The reduced optical absorption accompanying the thinner Si, can be offset by employing an effective light-trapping scheme in the cell structure. Furthermore, the structure and processing techniques for the cell fabrication must be compatible with the low-cost device.

Several approaches are being followed to make thin Si solar cells; these will be reviewed in detail in a forthcoming paper (1). One of the potentially valuable approaches is to use a polycrystalline Si film on a low-cost substrate such as glass. Early attempts at fabricating cells with Si films in the thickness range of 1–3 µm have shown excellent current densities (J_{sc}'s) that reached near-theoretical values (2,3). However, the V_{oc}'s and the FF's of such devices are quite low, which could be attributed to factors such as very small grain size, the high density of intra-grain defects, and high interface recombination velocities (4,5).

The objective our work is to design a low-cost, thin-film Si solar cell capable of yielding high efficiency, and develop a fabrication process for the cell using a glass substrate. This paper describes a new, single-junction, thin Si cell structure and proposes some processing methods for its fabrication.

CELL DESIGN

Because a thin-film solar cell must meet a host of requirements related to the material properties and process conditions, the cell design and fabrication processes must be considered together. Of particular interest is the choice of the substrate. A low-cost substrate is apt to have properties that may not be compatible with the high temperatures required for typical Si processing. For example, low-cost soda-lime glass is not thermally well matched to Si, has a softening point below 550°C, and is likely to degas at elevated temperatures, causing diffusion of undesired impurities into the Si film. Hence, it is essential that appropriate solutions to these problems be included in the cell design itself. Other issues for consideration are that the Si deposition process, the formation of PN junction, and metallization technique must conform to the low-cost technologies.

In addition to the considerations for processing compatibility, the cell design must address other items that include: (i) the nature of textured interface(s) to improve the light-trapping efficiency, (ii) high-reflectivity back contact, (iii) the grain size and quality of the active-layer material, (iv) the junction parameters, and (v) proper AR coating (materials, thickness).

Figure 1 shows the proposed design of our cell. It consists of a metallized, low-cost glass substrate on which a thin layer of either amorphous or fine-grain poly-Si is deposited. The Si film can be deposited by any of the variety of low-temperature processes such as sputtering, PECVD of a-Si or μc-Si, and the hot-wire technique. This film, typically p-type, acts as the base region of the cell. The as-deposited film is then grain enhanced, as described later, to produce a grain size about 10 times the thickness of the base region. An N/P junction can be formed either by a low-

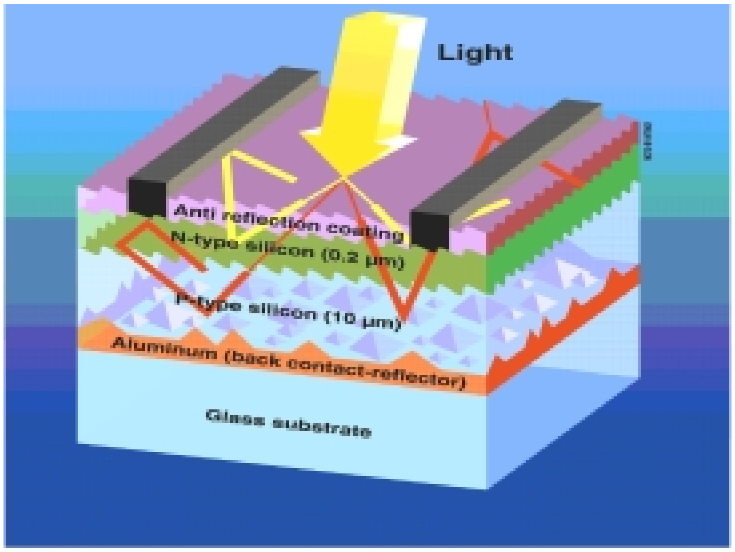

FIGURE 1. A schematic of the thin film Si cell showing major features of the cell design.

temperature deposition of an n-type layer or by some new type of a diffusion at low temperature. The other features shown in the figure are self-explanatory.

This structure realizes a host of important, high-efficiency, features. These include: (i) textured interfaces at the front and the back sides of the cell, (ii) highly reflective back contact, (iii) a built-in gettering layer of Al to minimize impurities in the Si film, (iv) a large grain size to minimize junction shunting, and (v) a stress-relief layer of Al on glass that obviates need for thermal matching between glass and Si film. It should be pointed out that having a back reflector directly in contact with thin Si will lead to an optical loss arising from metal absorption (6). This metallic loss increases with a reduction in the cell thickness. Hence, a compromise should be made between the minimum thickness needed for light trapping and the metallic loss. We have performed calculation using *PV Optics* to determine this thickness (7). Some of the results are shown in Figure 2. This figure compares maximum achievable current density (MACD), obtainable with the cell configuration of Figure 1, as a function of the cell thickness, for three different interface structures. The interface shapes, illustrated in the figure, consist of texture front/planar back, texture front/texture back, and planar front/texture back. This figure shows that, for small thicknesses, texture front/texture back is the optimum configuration. Furthermore, it is possible to obtain about 35 mA/cm^2 in a 10-µm-thick cell. To show the accuracy of our calculations, we have plotted the experimental data from Kaneka (8); an excellent agreement is observed.

An important issue for a thin-film Si cell is the grain size required to achieve high V_{oc}'s and FF's. Our calculations and experimental results show that the grain size needed to reach 16% – 20% range of efficiency, is about 50 µm. The grain size can be considerably smaller if an effective passivation of the grain boundaries can be performed. However, if the film has a high density of intragrain defects, the grain size needs to be larger. A number of processes, including metal induced recrystallization (9,10), zone melting recrystallization (11), Laser induced crystallization (12), and grain enhancement by optically-assisted defect injection, GEOADI (13), can achieve the large grain size. We will briefly describe the results of GEOADI, which verify the

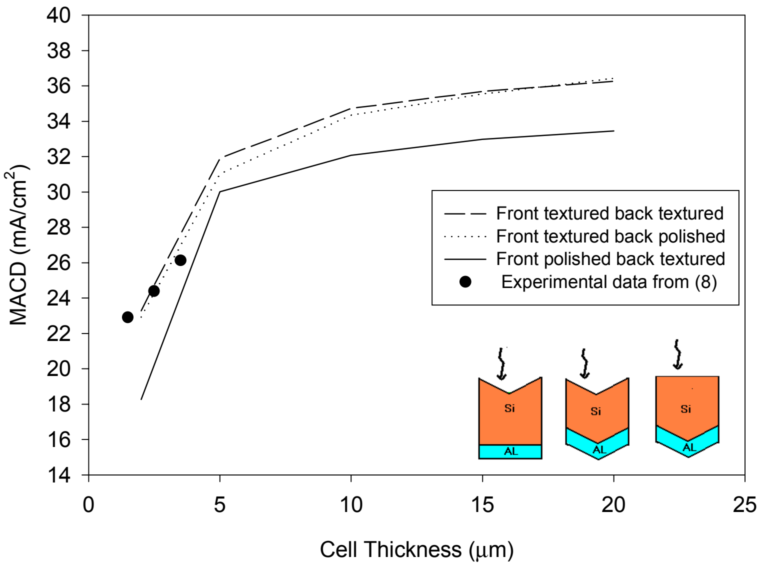

FIGURE 2. Calculated maximum achievable current density (MACD) as a function of thickness for three different cell configurations.

TABLE 1. Summary of Various Crystallization Techniques

Method	Processing Temp. (°C)	Processing Time	Metal Contamination
Annealing	500	20-40 hours	Low
ZMR	1200	Short	Low
MIC	<500	Medium, ~ hours	Severe
LIC	>1000	Short	Low
GEOADI	<600	Short	Superior to MIC

ZMR = zone melt recrystallization, MIC = metal induced crystallization
LIC = laser induced crystallization,
GEOADI = grain enhancement by optically-assisted defect injection.

feasibility of fabricating such a cell by a low-temperature and a low-cost, process. Further details of this process are given in reference (14).

GRAIN ENHANCEMENT OF AN A-SI FILM USING OPTICAL PROCESSING

It is well known that an a-Si film can be crystallized by a thermal treatment. However, thermal crystallization alone requires long times or high temperatures, and can only yield small grain size. Many techniques have been tried to accelerate this process and lower the process cost. Table 1 compares properties of the films produced by several grain-enhancement methods. This table includes the characteristics of our technique for grain enhancement, GEOADI. The apparatus and procedures of the processing have been described elsewhere (13). Here we only present some results of this process.

Because our composite substrate includes a metal layer, it promotes crystallization of a-Si even at a very low deposition temperature. This feature can be seen in Figure 3, which reveals the morphologies of a sputtered a-Si film, deposited on a glass substrate, with and without an Al layer under the Si film. It is seen that the non-Al part of the Si film is amorphous, while the film on Al has columnar grains, typically about 0.1 µm in size. The substrate was not intentionally cooled during sputtering; as a result the substrates acquired a temperature of about 70°C. It is thus clear that the presence of Al results in a nucleation of grains during the deposition. A further increase in the grain size can be produced by GEOADI — a process step in which this film is illuminated with light from tungsten-halogen lamps. Figure 4 is an SEM picture of a sample after processing with 5 W/cm^2 for several minutes, showing that grain sizes up to several microns are formed by the process.

FORMATION OF HIGHLY REFLECTING INTERFACES

In our cell design, the Al back contact also acts as the back reflector, requiring this interface to have a high optical reflectance. We have previously described a process

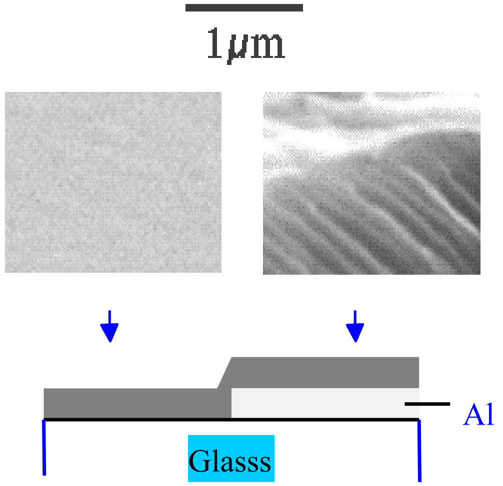

FIGURE 3. Illustration of the effect of Al on the Si grain growth, and the SEM photographs comparing grain size with and without Al.

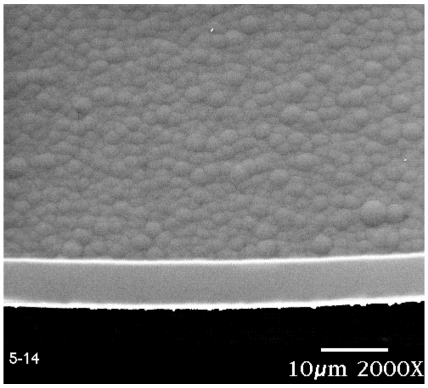

FIGURE 4. An SEM photograph showing grain morphology of a thin Si film after grain enhancement

for forming an ohmic contact with such properties using optical excitation (14). Figure 5 shows the reflectance of Si-Al samples after different processing conditions. It can be seen that under certain conditions, the reflectance of processed Si-Al alloy interface can be very close to the unprocessed Si/Al interface. This feature is manifested as high reflectance for wavelengths larger than 1.1 µm. Such a contact also has very low contact resistivity, as required for high-efficiency solar cells.

Another important feature in our design is the textured back contact. We have previously developed a technique for forming a texture at the Si-Al interface of a single crystal and multicrystalline wafers using a process very similar to the one described above for grain enhancement (15). The texture formation occurs because the diffusivity of Al in Si is different along the different lattice directions. A similar process is expected to occur at the small-grain Si/Al interface.

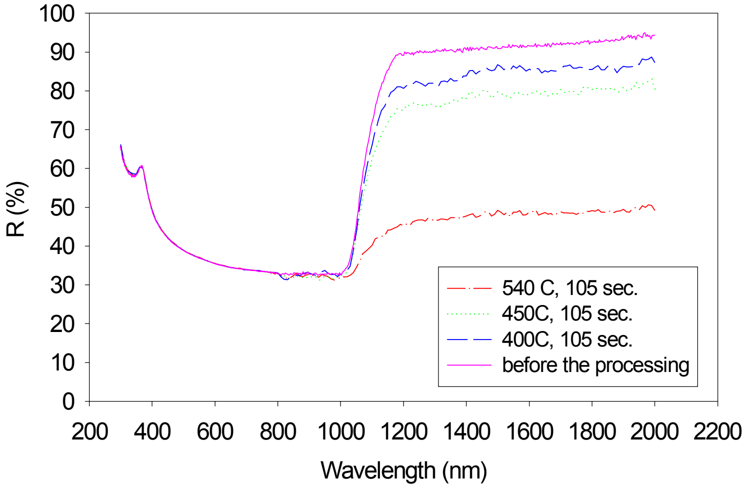

FIGURE 5. Reflectance of a Si/Al sample processed by Optical Processing under different conditions showing changes in the interface properties by the reflectance for wavelengths larger than 1.1µm.

CONCLUSION

We have briefly discussed a new cell structure that offers a promise of being able to yield high efficiency. This structure embodies major features needed for low-cost, low-temperature cell processing. Our calculations predict this structure is capable of generating MACD of 35 mA/cm^2, and a V_{oc} of 600 mV, with a 10 μm thick film of a reasonable grain size. We have verified essential process steps such as grain enhancement at low temperatures, formation of Si/Al back reflector, and our metal layer acting as a stress-relief buffer.

ACKNOWLEDGEMENTS

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