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Subcontractor Report

Polycrystalline Thin-Film Cadmium Telluride Solar Cells Fabricated by Electrodeposition

Final Technical Report
20 March 1995 – 15 June 1998

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EXECUTIVE SUMMARY

Objectives

One of the objectives of this project is to develop improved processes for the fabrication of high-efficiency CdTe/CdS polycrystalline thin film solar cells. The technique we use for the formation of CdTe, electrodeposition, is a non-vacuum, low-cost technique that is attractive for economic, large-scale production. The other objective was to study cell degradation, using stability tests under stress conditions and analysis of possible degradation mechanisms.

Technical Approach

Our research and development efforts have focused on several steps that are most critical to the fabrication of high-efficiency CdTe solar cells. These include the optimization of the CdTe electrodeposition process, the effect of pre-treatment of CdS substrates, the post-deposition annealing of CdTe, and back contact formation using Cu-doped ZnTe. Systematic investigations of these processing steps have led to better understanding and improved device performances of the CdTe-based solar cells.

Stability tests under enhanced temperature showed that cell efficiency degradation is due mainly to an increase in "series resistance". Therefore the degradation processes studies were focused mostly on revealing and explaining the changes that occur in the back-contact region and in the bulk CdTe due to the ZnTe:Cu back contact presence. These changes were studied by means of detailed analyses of the cell I-V characteristics, the C-V profile in the CdTe, and compositional changes in the back-contact region. When discussing possible mechanisms of degradation, the compensation phenomena and charged impurities electromigration were taken into account.

Major Results and Conclusions

<u>CdS thin films prepared by chemical bath deposition. Film growth and structure.</u>

The structural properties of the films and the growth mechanisms were studied by investigating CdS samples prepared at different deposition times. A duplex structure with an inner compact layer and an outer porous layer and three growth stages can explain our data. The measurement of refractive index as a function of deposition time provides a simple way to determine the transition point from compact layer growth to porous layer growth, which is important for the optimization of CdS growth conditions in photovoltaic applications. Careful XRD analyses allowed unambiguous determination of crystal properties.

<u>Electrodeposited CdS Thin Films and their application.</u>

Electrodeposition is a non-vacuum technique and is compatible with our CdTe deposition process. It offers excellent control over the properties of the thin films through the influence of deposition potential, bath temperature, pH, and composition of reactants. In

this project preliminary studies were performed on the electrodeposition of CdS and its application in fabricating CdTe/CdS solar cells. The influence of deposition conditions on the film deposition rate, composition and morphology was studied. CdTe/CdS cells using electrodeposited and physical vapor deposited CdTe on electrodeposited CdS were prepared and characterized. Moderate cell efficiencies were obtained in this preliminary study. Modification of our standard post-deposition treatment led to a considerable increase in cell efficiency. Although it was still lower (8.7%) than for the CBD CdS, it became clear that there is room for the further improvement of the cell performance by means of post-deposition treatment optimization and also by selection of a proper TCO material for the front contact. The latter greatly influences the CdS film morphology and adhesion.

CdTe - CdS interdiffusion.

Post-deposition heat treatments of CdS and CdTe/CdS thin films with $CdCl_2$ coating are very important steps in our processing procedure leading to considerable improvement of the cell performance. Recrystallization and interdiffusion processes at the annealing with $CdCl_2$ are much more pronounced in CBD CdS and electrodeposited CdTe (low-temperature deposition processes) than in "high temperature" deposited films (e.g., deposited by the close space sublimation method). Our cell efficiency increases considerably as a result of the CdS and CdS/CdTe post-deposition treatments and there are indications that there is room for the further improvement of the cell performance through post-deposition steps optimization. In this project we studied diffusion processes and also their influence on the electronic properties of the films. Because of the finite solubility of CdS and CdTe within each other, and interdiffusion between the CdS and CdTe layers, a CdTe-rich ternary phase ($CdTe_{1-x}S_x$) is formed in the CdTe layer. A CdS-rich ternary phase ($CdS_{1-y}Te_y$) may also be formed in the CdS layer. The degree of these interdiffusion processes is affected by the $CdCl_2$ treatment of CdS films and was quantitatively measured in our study by monitoring the change of line shape of XRD patterns. Photoluminescence measurements were also used to study S diffusion into the CdTe. The results of the studies were as follows.

(1) While only a negligible portion of the CdS is converted to $CdS_{1-y}Te_y$ for the $CdCl_2$-treated CdS, it is fully converted to the ternary phase when as-deposited CdS is used. The y value was estimated to be 4.4% in $CdS_{1-y}Te_y$.

(2) In CdTe annealed at temperature $>400^0$C, two phases coexist: pure CdTe located at the central part of the grains, and a ternary phase $CdTe_{1-x}S_x$ concentrated at the grain boundary region. The content of S in the ternary phase is defined by the solubility limit for the annealing temperature used. The total amount increases with annealing temperature. It was found that annealing at 410^0C for 45 min (our standard procedure) leads to thinning of the CdS by 60-70 nm. That imposes a lower limit on the initial CdS film thickness.

Electronic properties of CdS films treated under different conditions were also studied. It was found that annealing at 450^0C for 50 min increases the bandgap by 60-70 mV bringing it close to the bulk CdS bandgap value. Conductivity of as-prepared films is very low and its temperature dependence is characterized by an activation energy of about 0.7 eV. The films reveal very high photoconductivity with characteristic times of decay

achieving hours. Both effects (the activation character of the dark conductivity temperature dependence and high photoconductivity) could be attributed to the influence of the potential barriers for the majority carriers located at the grain boundaries. Annealing with $CdCl_2$ decreases significantly the role of these barriers.

By means of optical transmission, differential optical absorption and photoluminescence measurements we demonstrated the strong influence of annealing, especially with $CdCl_2$, on the types of defects and their density in CdS thin films. There was some indication that at least some of the defects are reconstructing centers, that is with the thermal and optical ionization energy values different from each other. Measurement of radio-frequency photoconductivity decay on CdS films containing different amounts of Te showed that Te impurities in CdS act as effective recombination centers.

ZnTe:Cu/Metal back contact.

Because of the rather high work function of CdTe and the difficulty of achieving high doping levels in p-type CdTe, a low-resistance ohmic contact cannot be formed by a simple metallization. ZnTe, which has a small valence band discontinuity with CdTe and can be doped degenerately with Cu, has been used as an intermediate layer between the high-resistivity CdTe and the metal contact. We studied the effects of Cu concentration, ZnTe:Cu layer thickness, substrate temperature at deposition, ZnTe post-deposition annealing conditions, and contact material to the ZnTe on the photovoltaic performances of CdTe/CdS solar cells. Concurrently with the ZnTe back contact studies we also investigated ZnTe thin films on glass substrates prepared with the same processing procedure. That helped us to study and better understand the electronic properties of the ZnTe interlayer and to optimize dopant concentration and post-deposition conditions.

It was shown that a short anneal at temperature of about 250^0C and higher activates the Cu dopant and provides a hole concentration in ZnTe in the range 10^{18}-10^{20} cm^{-3} which is supposed to be sufficient for obtaining low-resistance contacts. This anneal also eliminates irreversible changes in electric properties of the ZnTe thin films and decreases considerably intergrain resistances. The optimized processing procedure for the ZnTe:Cu back contact interlayer included: etching of the CdTe surface in the diluted Br_2-Methanol solution for some tens of seconds followed by rinsing and drying; ZnTe and Cu coevaporation on the CdTe surface held close to room temperature (film thickness ~50 nm, Cu concentration in ZnTe ranging from 2 to 6 at.%); short post-deposition annealing at T=250-270^0C. Back contact formation is completed with metal deposition. Using of Au, Ni, and Co metallizations provided almost the same efficiency of about 12% and series resistance lower than 1 W-$cm^{2.}$. The best results for Au metallization were: η=12.9%, R_{se}<0.1 Ω-cm^2.

Cell performance improvement.

Based on studies described above we have increased the efficiency of the cells with the electrodeposited CdTe and CBD CdS by 3% on average (~30 relative %). The improvement came from:

1. Optimization of CdS initial thickness taking into account CdS consumption by CdTe during the CdTe/CdS post-deposition treatment; optimization of CdS post-deposition treatment with $CdCl_2$ aimed at prevention of Te diffusion into CdS and improvement

of the CdS film morphology and electronic properties. That led to a considerable increase in short circuit current, by 13 % on average.

2. Optimization of CdTe thickness and post-deposition treatment which led to a significant increase in V_{oc} , by ~70 mV. The highest V_{oc} obtained exceeded 800 mV.
3. Development of a ZnTe:Cu/Metal back contact processing procedure which included selection of optimal Cu content, deposition regime and post-deposition treatment conditions.

As a result, back contact resistance as low as $0.1\Omega\text{-cm}^2$ was obtained. Preliminary studies of some new approaches to improvement of CdS/CdTe structure were conducted.

Cell degradation studies.

Cells with the ZnTe:Cu/Au back contact were subjected to the long-term stability tests in the vacuum oven at enhanced temperature (140 and 110^0C), in dark. It was found that degradation of cell efficiency was caused mostly by the increase in "series resistance". Analysis of the dynamic resistance, R= dV/dJ, as a function of current and voltage on the basis of a two-diode model, showed that the degradation of the cells with the ZnTe:Cu/Au back contact is due to a decrease in the saturation current of the back contact Schottky diode. A strong correlation was observed between increase in the Schottky barrier resistance and decrease in doping level in the CdTe. The latter increases the Schottky barrier height and width and hence decreases its transparency for holes. It was demonstrated by special experiments that Cu dopant in ZnTe not only provides a low resistance back contact but also is responsible to a great extent for the cell degradation. Discussion of the experimental data led to the conclusion that Cu acceptors in CdTe are highly compensated by donors (not certainly identified yet) and that significant changes in carrier concentration observed under stress tests were caused by a very small (probably, not more than 1%) increase in compensation degree.

Using the XPS and AES measurements, compositional changes in the back contact region were studied. A considerable diffusion of Au into and through the ZnTe layer was observed as well as a significant consumption of Cu and Te by the Au layer. It was concluded that these processes can influence significantly not only series resistance degradation but also changes in the bulk CdTe and CdTe/CdS junction. No composition changes of this kind were found for the Ni metallization. This may explain, at least partially, the difference in degradation processes for these two metallizations. Increase in "series resistance" was more significant for Au while decrease in the "shunt resistance" was more rapid for Ni.

Stress stability tests with forward and reverse biases applied to the cells revealed some peculiarities in cell degradation that were qualitatively explained on the basis of a possible influence of Cu electromigration. Comparative theoretical analysis of diffusion and electromigration of Cu in different parts of the CdTe cells showed that electromigration can play a dominating role in Cu migration and degradation processes under real cell operating conditions. When discussing the results of tests under different stressed conditions, one must consider changes in electric field magnitude and distribution over the cell thickness. For example, it should be realized that illumination itself may cause greater and more important changes in electric field within the absorber layer than reverse bias or reverse bias in combination with light.

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1. INTRODUCTION

1.1 Background

Polycrystalline thin-film CdTe has attracted a great deal of interest for low-cost, high-efficiency photovoltaic energy conversion applications. Among the various techniques that are available for CdTe thin film deposition, electrodeposition is a non-vacuum technique and has the advantage of low cost, efficient utilization of raw material, and scalability for high-volume production. At the same time, additional research is still needed to improve upon the process reproducibility and performance levels achieved to date. Among the significant issues are interface carrier recombination and top-layer photon absorption which presently limit the short-circuit current, junction recombination which limits the open-circuit voltage, and series-resistance losses which suppress the fill-factor.

The objective of the CSM contract was to improve certain processing steps of the cell fabrication and to further our knowledge of these polycrystalline thin film materials. Improved efficiencies, high-quality film growth techniques, materials analysis, device fabrication and characterization have all been of particular interest in our work. We also were focused, especially in Phase III of the project, on stability issues. Using tests under various stress operating conditions, we tried to clarify mechanisms of cell degradation.

1.2 Cell Fabrication Procedure

The solar cell we investigate has a CdTe/CdS/SnO_2/glass structure. The standard cell fabrication procedure includes:

1. Chemical bath deposition (CBD) of CdS layers (typical thickness of 0.2 μm) in an alkaline solution containing cadmium acetate, ammonium acetate, ammonium hydroxide, and thiourea (see Section 2.3 for the solution composition).
2. Annealing of the CdS films at 450°C for 50 min in a N_2 atmosphere. A $CdCl_2$ coating is applied to the CdS surface prior to annealing, using a mist generator containing a 1.2 M $CdCl_2$ aqueous solution.
3. The electrodeposition of CdTe (typical thickness of 2 - 3.5 μm) using a system composed of four electrodes: Cd and Te anodes, a Ag/AgCl reference electrode, and a cathode (sample substrate). The typical electroplating conditions are: pH, 2; temperature, 80°C; 1.2 M $CdCl_2$; deposition current between 0.26 and 0.40 mA/cm^2; deposition potential, -600 mV (vs. Ag/AgCl electrode); and anode current ratio close to 2.0.
4. Annealing of CdTe/CdS films at 410°C for 40 min in dry air. Prior to annealing, a $CdCl_2$ coating was applied to the CdTe surfaces using the same procedure as used for the CdS layers.
5. Etching of the CdTe surface in a 0.1% Br-MeOH solution for 10 s and back contact formation using either evaporated Au or Cu-doped ZnTe followed by Au evaporation.

1.3 Thin Film and Device Characterization

A wide variety of thin film and device characterization techniques was used to characterize our material. X-ray diffraction (XRD) measurements were performed on a Rigaku x-ray diffractometer using Cu-Ka radiation. Scanning electron microscopy (SEM) measurements were performed using a JOEL Model 840 instrument. Optical transmission and reflection measurements were performed using a CARY 5E UV-VIS-NIR spectrophotometer equipped with a PTFE integrating sphere. Film thicknesses were measured using a Dektak 3 surface profiler and later a Tencor P-10 Profiler. Hall effect and mobility in a temperature range were measured using a Bio Rad Hall system. For studies of low-temperature luminescence spectra of CdTe/CdS structures (not completed cells) the following combination of instruments was used: (1) Double-grating spectrometer Spex-1301; (2) GaAs photomultiplier(as a detector); (3) Ar-Ion Laser Spectra Physics / 2000 and He-Ne Laser Melles Griot (as excitation sources). For the study of structural and optical properties of the CdS films after CdTe deposition and final annealing processes, the CdTe layers were removed either mechanically or by chemical etching. Auger electron spectroscopy and x-ray spectroscopy studies were performed using PHI 600 and Kratos-HSI systems, respectively. The finished cells were characterized using current-voltage, capacitance-voltage, and spectral response techniques.

1.4 Material Presentation in the Report

The results of studies performed in the first two years of the project (Phases I and II) were described in detail in our Annual Technical Reports: March 1995 to March 1996 and March 1996 to March 1997 , and also in some publications. Therefore in this Final report we will present briefly and summarize these results referring when necessary to the annual reports mentioned above and publications. Studies conducted in the third year of the project (Phase III) are presented in more detail. The titles of the corresponding sections are supplied with the index (III), e.g. "4. CELL DEGRADATION UNDER STRESS CONDITIONS (III)". The references to our technical reports to NREL (see Appendix B) are supplied with the superscript ®, e.g., [2®], the references to our publications (see Appendix A) with an asterisk, e.g., [3*], and references to other sources (see Sec. 6, REFERENCES) have no special signs.

2. CdS/CdTe THIN FILM STUDIES

CdS is commonly used as an n-type window layer in CdTe solar cells. Different techniques are used for thin film CdS preparation. Among them, chemical bath deposition (CBD) is a simple and low-cost method and produces uniform, adherent, and reproducible films. This method is what we use for the CdS layer deposition in our standard cell fabrication procedure. However, CBD has the disadvantage of low material utilization and high volume waste production. It is also less compatible with the vacuum-based CdTe deposition technologies. As such, other techniques have been studied to produce CdS films of comparable (with CBD) quality. In this project, in addition to CBD, we also studied

electrodeposition of the CdS layer and properties of the cells with both CdS and CdTe layers prepared by electrodeposition.

The treatment of the CdS thin film prior to the deposition of CdTe and CdTe/CdS postdeposition treatment are critical steps in the fabrication of polycrystalline CdTe/CdS solar cells. In this section we present and discuss in detail structural, compositional and electronic properties of CdS and CdTe thin films and their dependence on preparation conditions, in particular due to interdiffusion between the CdTe and CdS. Our efforts aimed at optimization of the CdS/CdS structure and processing procedure with respect to the cell performance were based on these studies.

2.1 CdS Thin Films Prepared by Chemical Bath Deposition. CdS Film Growth and Structure

(See also [1®])

There have been several publications [1-5] on the mechanism of CdS growth via CBD as it relates to the optimization of CdS film properties. It is well known that, depending on the deposition conditions, an "ion-by-ion" growth process results in compact and adherent films while a "cluster-by-cluster" process or colloidal growth yields porous films [1,5]. Chemical bath deposition of CdS proceeds in three main stages [2]: an induction stage, a compact layer growth stage and a porous layer growth stage. The induction stage corresponds to the formation of nucleation sites on the substrate and growth of a compact layer that is usually completed at a thickness between 100 and 200 nm [1,3]. Afterwards, a porous layer is formed for longer deposition time. Finally, the solution species are exhausted and the CdS film growth ceases. If CdS film growth proceeds into the porous layer growth stage, a duplex layer structure, which consists of an inner compact layer and an outer porous layer with some surface particles, will be formed.

We studied CdS films of various thicknesses corresponding to the termination of the growth at different deposition stages. CdS thin film samples were prepared on glass slides by CBD from an ammonia-thiourea aqueous solution. The chemicals and their concentrations in the solution were: $CdAc_2$ ($1x10^{-3}$ M), NH_4Ac ($20x10^{-3}$ M), and $(NH_2)_2CS$ ($5x10^{-3}$ M). Ammonia was used to adjust the initial solution pH to a value between 9 and 10. The chemical bath was kept at a temperature of 85^0C. The substrates were immersed in the solution and taken out at different deposition times. The mechanism of CdS growth, the structural properties of these films and the compactness of the films were then analyzed using XRD, ellipsometry and other measurements.

Studies of the evolution of the refractive index provided us with a simple quantitative method to determine the transition point from compact layer growth to porous layer growth. The refractive index, as a function of deposition time, was obtained from optical reflection and transmission measurements. In the compact layer growth region, CdS does not fully cover the substrate. This contributes to an artificially smaller refractive index in comparison to that of bulk CdS. Near the transition point from the compact layer growth to the porous layer growth, the refractive index is close to that of bulk CdS (2.40) and

reaches its maximum value (2.35). As porous layer growth starts, the refractive index decreases. Refractive index values measured from ellipsometry show qualitatively the same trend. In order to obtain dense CdS films, the substrates need to be removed from the bath just prior to porous layer growth (35 min in our experiments).

The grain size was determined from XRD line widths using the Scherrer equation. The grain size is linear with the film thickness and still increases during the porous layer growth which corresponds to film thickness above 150 nm for our deposition conditions. It was concluded that the "ion-by-ion" growth process continues in the porous layer growth stage, even though the "cluster-by-cluster" growth process becomes more important, i.e. there is not a sharp transition in growth mechanisms.

The CdS surface roughness increases significantly as a function of CdS film thickness, t : from 20 nm for t=100 nm to 150 nm for t=250 nm. The roughness is mainly due to height difference of CdS surface particles adsorbed from solution. In the compact layer growth region, the amount and size of adsorbed CdS surface particles are relatively small. In the porous layer growth region, on the other hand, the roughness is relatively large and increases quickly.

The results of numerous studies of the structural properties of CdS films prepared by CBD are scattered over a wide range [5-9] because of different deposition conditions used in various laboratories. Because high quality as-deposited CdS films have only one preferred orientation, corresponding to either cubic (111) or hexagonal (002), it is difficult to distinguish these two phases based on the XRD peak position [5,6]. According to [1] the "ion-by-ion" process results in compact films which have pure hexagonal or a mixture of hexagonal and cubic phase, while the "cluster-by-cluster" process gives rise to porous layers with pure cubic phase . This point of view influenced other authors' assumptions on the phase of as-deposited CdS [4].

We have analyzed the XRD patterns for CdS films obtained in the compact layer and porous layer growth stages. In order to determine the phase unambiguously we performed also XRD studies of CdS powders collected from the solution, as well as the powders obtained by scraping CdS films from the glass substrates. XRD patterns of CdS films obtained in the compact layer growth stage and in the porous layer growth stage are similar. The positions and relative integrated intensities of several peaks were used to determine the CdS phase. Both peak positions and relative integrated intensities are closer to those of the cubic phase than those of the hexagonal phase. The strongest evidence against any hexagonal phase is the absences of the hex (100) and (101) peaks. Therefore it was concluded that the CdS films are purely the cubic phase, even for films grown dominantly by the "ion-by-ion" process in the compact layer growth region. This is contrary to what was reported earlier [1].

2.2 Electrodeposited CdS Thin Films and Their Application in CdS/CdTe Solar Cells

(See also [2®] and [13 *])

The electrodeposition of CdS was done in a system that consisted of a glassy-carbon anode, an Ag/AgCl reference electrode, and a cathode (sample substrate). The experimental conditions used in our study were: pH from 2.0 to 3.0; temperatures of 80° and 90°C; $CdCl_2$ concentration of 0.2 M; deposition potential from -550 to -600 mV vs. Ag/AgCl electrode; [$Na_2S_2O_3$] concentration between 0.005 and 0.05 M. Either HCl or H_2SO_4 was used for adjusting the pH. Typically, a film of 200 nm can be grown in less than 1 hr. The films exhibit a yellow color typical of pure CdS, in contrast with the orange color commonly shown by chemical bath deposited CdS.

The electrodeposition rate of CdS was studied as a function of the solution temperature, sodium thiosulfate concentration, pH, and the acid used. The deposition rate increases with increase of the thiosulfate concentration and decrease of solution pH. This dependence can be understood based on the known dissociation of thiosulfate ions:

$$S_2O_3^{2-} \leftrightarrow S + SO_3^{2-}$$

and the overall electrode reaction:

$$Cd^{2+} + S_2O_3^{2-} + 2e^- \leftrightarrow CdS + SO_3^{2-}$$

With decreasing pH and increasing thiosulfate concentration, the dissociation rate increases, leading to an increased deposition rate of CdS on the electrode. The high deposition rate observed at high solution temperature may be caused by both an increased reaction rate at the electrode and the increased thiosulfate dissociation rate. We also observed that the acid used to adjust the pH has a large impact on the deposition rate. The deposition is faster in a hydrochloric solution than in a sulfuric acid solution. The lower the pH the lower the Faradaic efficiency. This is caused presumably by the hydrogen evolution at low pH which contributes to the reduction current. In both cases, the Faradaic efficiency was much lower than unity.

The morphology of electrodeposited CdS was studied using SEM. Films consist of agglomerates of small crystallites. The agglomerates size was of the order of 1μm. The crystallites that compose these agglomerates had a typical size of about 50 nm. In terms of film uniformity and cell fabrication, deposition in a hydrochloric acid solution at 80°C is preferred. The improved uniformity can be related to the slow growth rate obtained under such conditions. We have also investigated the effects of substrate materials. Films deposited on ITO substrates are much more uniform than films deposited on tin oxide substrates under the same deposition conditions.

X-ray diffraction measurements indicated that the electrodeposited CdS is a mixture of hexagonal and cubic phases. This is different from the chemical bath deposited film which, according to our previous study, exhibited only cubic phase.

The composition of the electrodeposited CdS was analyzed using Auger electron spectroscopy. The ratio of Cd and S concentrations is close to the stoichiometric value for films deposited at a pH of 3.0. At lower pH, the films are more Cd rich.

CdTe/CdS cells prepared using electrodeposited CdS films had considerably lower efficiency than those with the CBD CdS films. Electrodeposited CdS films have poor adhesion to the tin oxide substrates and flake off easily during CdTe deposition or post-deposition annealing. This problem is especially severe when the CdTe films are thick or when the CdS films are not annealed prior to CdTe deposition. When our standard CdTe/CdS annealing procedure was used, cells made with electrodeposited CdS exhibited a low open-circuit voltage and a low shunt resistance. We have modified the post-deposition annealing procedure in order to improve the adhesion. Significant improvement was obtained in terms of V_{oc}, R_{sh}, and the resulting cell efficiency. The open-circuit voltage of 0.65 V and efficiency of 7.7 % obtained with a CdS film thickness of 125 nm are comparable with what we obtained with CBD CdS of a comparable thickness. However, at larger CdS thicknesses, the efficiency of cells fabricated with electrodeposited CdS is much lower than what we obtain typically (upper 700 mV range) with CBD CdS.

Cells were also made using physical vapor deposited CdTe on electrodeposited CdS. The cell performances are shown in Table 2.2.1 for two CdS deposition conditions. The fractions of pinhole area of the CdS are also listed. We can see that the V_{oc} of the cells correlates well with the pinhole density.

Table 2.2.1. Cells with physical vapor deposited CdTe on electrodeposited CdS.

CdS deposition conditions	**η (%)**	**V_{oc} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**R_s (Ω-cm^2)**	**Fraction of pinhole area (%)**
pH=3.00; 90^{0}C	8.7	705	21.4	57.9	6	$5x10^{-6}$
pH=2.65: 80^{0}C	8.4	629	20.6	64.8	4	$3x10^{-5}$

2.3 CdTe-CdS Interdiffusion Studies

Post-deposition heat treatments of CdS and CdTe films with preliminary $CdCl_2$ coating are very important steps in our processing procedure leading to the considerable improvement of the cell performance. Recrystallization and interdiffusion processes upon annealing with $CdCl_2$ are much more pronounced in CBD CdS and electrodeposited CdTe (low temperature deposition processes) than in "high-temperature" deposited films (e.g., those deposited using close space sublimation). Cell efficiency increases considerably as a result of the CdS and CdS/CdTe post-deposition treatments and there are indications that

there is more room for the further improvement of the cell performance through the optimization of post-deposition steps. Unfortunately, not all the mechanisms of post-deposition treatments influences on the electronic properties of the cell are clear. We consider the clarification of the problem as a very important part of our studies of CdTe/CdS solar cells. It is reasonable to consider the diffusion processes and compositional changes in the CdS and CdTe layers prior to the discussion of electronic properties.

2.3.1. XRD Studies of CdTe Annealing and CdTe-CdS Interdiffusion

(See also [1®, 3*, 6*])

Because of the finite solubility of CdS and CdTe within each other, interdiffusion between the CdS and CdTe layers occurs during the final annealing of CdS/CdTe films. As a result, a CdTe-rich ternary phase ($CdTe_{1-x}S_x$) is formed in the CdTe layer. A CdS-rich ternary phase ($CdS_{1-y}Te_y$) may also be formed in the CdS layer. The degree of these interdiffusion processes is affected by the $CdCl_2$ treatment of CdS films and can be quantitatively measured by monitoring the change of line shape of the XRD patterns.

Both the as-deposited and annealed CdTe films exhibit lattice parameters larger than that of commercial CdTe powder, indicating an in-plane compressive stress in the films. For both the pure CdTe powder and the 350°C-annealed thin film, the XRD pattern is characteristic of a single-phased material. For CdTe films annealed at 410°C, a noticeable change in the XRD lineshape was observed. The XRD pattern is composed of two sets of peaks. One set of peaks (lower angles) corresponds to pure CdTe under compression. The second set, characterized by a smaller lattice parameter and growing in intensity with annealing time, indicates the formation of $CdTe_{1-x}S_x$.
Indeed, the good agreement between the measured lattice parameters of the powder collected from the thin film and that of commercial CdTe powder is a clear indication that the first set of peaks is associated with pure CdTe phase, rather than $CdTe_{1-x}S_x$ with low S content. Our result also indicates that the larger lattice parameter we observed with the thin films is related to residual stress introduced by the different thermal expansions between the thin films and glass substrate. Based on the observed difference in lattice parameters derived from the two sets of peaks and the known lattice constants of CdTe (0.6481 nm) and CdS (cubic, 0.5818 nm), we estimate the content of S in $CdTe_xS_{1-x}$ to be $x = 0.03$.

It has been found that S diffusion along grain boundaries proceeds at a rate several orders of magnitude higher than that in bulk CdTe [10]. Therefore, it was suggested that the pure CdTe exists mainly near the center of the grains. The nonuniformity of S diffusion is in the lateral direction, i.e., from grain boundaries to grain centers. The concentration gradient of S along the direction normal to the film is less significant. This is verified by comparing the XRD lineshape of the film and the scraped powders.

The dependence of XRD lineshape on $CdCl_2$ treatment and annealing conditions was investigated. For CdTe/CdS structures that were treated with $CdCl_2$ and annealed at a relatively low temperature (350°C), little interdiffusion was observed. For a higher

annealing temperature (410°C), the relative intensity of the S-alloyed component increases with the amount of $CdCl_2$ that was sprayed on the CdTe prior to annealing, indicating that $CdCl_2$ is effective in promoting the interdiffusion. The separation between the two peaks corresponding to CdTe and $CdTe_xS_{1-x}$ remains unchanged, indicating a constant x value in the alloy. The observed S content is expected to be limited by the solubility of S in CdTe at the annealing temperature.

A broad tail was also observed at the high angle side of the main $CdTe_xS_{1-x}$ peak indicating the existence of an alloyed region with S content higher than 3%. Such a broad peak indicates either a continuous distribution of S content in the $CdTe_xS_{1-x}$, or that the S-enriched regions are highly localized so that the diffraction peak is broadened. We are inclined to the second explanation and associate the S-enriched region with the grain boundaries and the small crystallites that exist at the CdTe/CdS interface.

The diffusion of Te into CdS and the formation of $CdS_{1-y}Te_y$ were also investigated by monitoring the XRD pattern of the hexagonal CdS (103) peak. For this measurement, the bulk CdTe layer was removed chemically in a Br_2-MeOH solution in order to enhance the XRD intensity of the CdS peak. For CdS/CdTe films prepared with $CdCl_2$-treated CdS, the CdS (103) XRD peak yields a lattice spacing characteristic of pure CdS. For films prepared with as-deposited CdS, on the other hand, the XRD pattern shows a significant shift of the peak position toward low diffraction angle, indicating an increased lattice spacing and the formation of an alloyed phase. This indicates that while only a negligible portion of the CdS is converted to $CdS_{1-y}Te_y$ for the $CdCl_2$-treated CdS, it is fully converted to the ternary phase when as-deposited CdS is used. Based on the known values of the (103) lattice spacing for CdS (0.1898 nm) and hexagonal CdTe (0.2115 nm), we estimate the y value to be 4.4% in $CdS_{1-y}Te_y$. This large difference in the extent of Te diffusion into CdS is expected to originate from not only the differences in grain size, but also the difference in defect density in the two types of CdS films.

For CdTe/CdS films prepared with as-deposited and $CdCl_2$-treated CdS, the sulfur content in the Te-rich ternary phase was found to be identical. The proportion of the ternary phase relative to the binary phase was found to be slightly higher for films prepared with as-deposited CdS, based on relative x-ray intensities of the two components.

2.3.2 Sulfur Diffusion in CdTe. XRD and Photoluminescence Studies (III)

(See also [5®,15*])

For CdTe/CdS films prepared with $CdCl_2$-treated CdS, two peaks at 2.54 eV and 2.08 eV were observed in the photoluminescence spectra, corresponding to a near band gap transition and a deep transition of pure CdS. For films prepared with as-deposited CdS, only a broad peak, at 1.74 eV energy, was observed [3*,6*]. This transition is characteristic of the $CdS_{1-y}Te_y$ ternary phase [11] and is presumably related to deep levels introduced by Te in CdS. The photoluminescence results therefore confirm the results obtained from XRD, i.e., $CdCl_2$-treated CdS remains pure CdS while non-treated CdS is fully converted to ternary phase during the final annealing step. In this section the recent studies of S diffusion

in CdTe are presented based on investigation of the depth profile of photoluminescence in $CdCl_2$ -treated CdTe/CdS structures annealed at different temperatures.

Experimental procedures

CdTe/CdS structures on soda-lime glass substrates (Nippon Sheet Glass) were prepared using our standard processing procedure (See Sec. 1.2). The only deviations were the variations in temperature of the CdTe postdeposition annealing and $CdCl_2$ amount applied to the CdTe surface prior to annealing. No back contact was deposited onto the CdTe.

X-ray diffraction (XRD) and photoluminescence (PL) measurements were used to characterize S diffusion into the CdTe layers. XRD was performed on a Rigaku X-Ray diffractometer using Cu-Kα radiation. PL measurements were performed at low temperature (15 K) under CW excitation using the 458 nm line of an argon ion laser. The luminescence was dispersed through a double pass grating spectrometer and detected at the exit slit using a cooled GaAs photocathode photomultiplier tube.

Profiles of the S concentration as a function of depth were obtained by sequentially removing the CdTe layer using a Br-methanol etch (0.025-0.1%). For PL measurements, a sequence of steps of various heights was etched into a single sample. A surface profiler was used to determine the step heights. Spectra were then obtained as function of depth. Since XRD measurements require a larger area than PL, profiling was accomplished by thinning the entire CdTe layer between XRD measurements.

AFM measurements (University of Oklahoma) of the CdTe surface topography were made to confirm that the etching process thinned the sample without preferentially etching grain boundaries or creating pinholes which might expose material deeper into the CdTe layer than the average etch depth. Fig. 2.3.1a shows an AFM image of the unetched CdTe surface. Fig. 2.3.1b shows an image obtained after etching close to the CdS interface. It is clear that the etch smoothes the surface without creating pinholes.

Results

X-ray Diffraction

We have previously used XRD measurements (see Sec.2.3.1) to detect the presence of $CdTe_{1-x}S_x$ in the CdTe layer and to show that anneal temperature and $CdCl_2$ treatment have a strong influence on the degree of interdiffusion. Now we have used XRD in conjunction with sequential
etching to profile the S concentration across the CdTe layer. Fig.2.3.2 shows a series of XRD patterns taken on a 5.3 mm thick CdTe film which was annealed at 410^0C. A high angle diffraction peak of CdTe (531) was chosen to improve resolution and minimize alignment effects. The etch times of 5 and 10 minutes correspond to regions in the middle of the CdTe layer while 20 minutes of etching exposes CdTe very near the CdS interface.

Two peaks corresponding to the $CuKa_1$ and $CuKa_2$ lines are visible in the unetched spectrum. As the CdTe layer is thinned, additional structure forms in the XRD pattern at higher angles indicating the presence of a $CdTe_{1-x}S_x$ phase. After the 5 and 10 minute etches this structure is visible as a shoulder on the pure CdTe peak. After 20 minutes the $CdTe_{1-x}S_x$ peak has shifted further (indicating an increase in S concentration) and it has become the dominant feature in the spectrum. Using the lattice constants of CdS and CdTe, peak fitting techniques, and taking into account residual stress in the films as previously discussed in Sec. 2.3.1 we find the S content of the $CdTe_{1-x}S_x$ for the measurement near the CdS surface to be x=0.053.

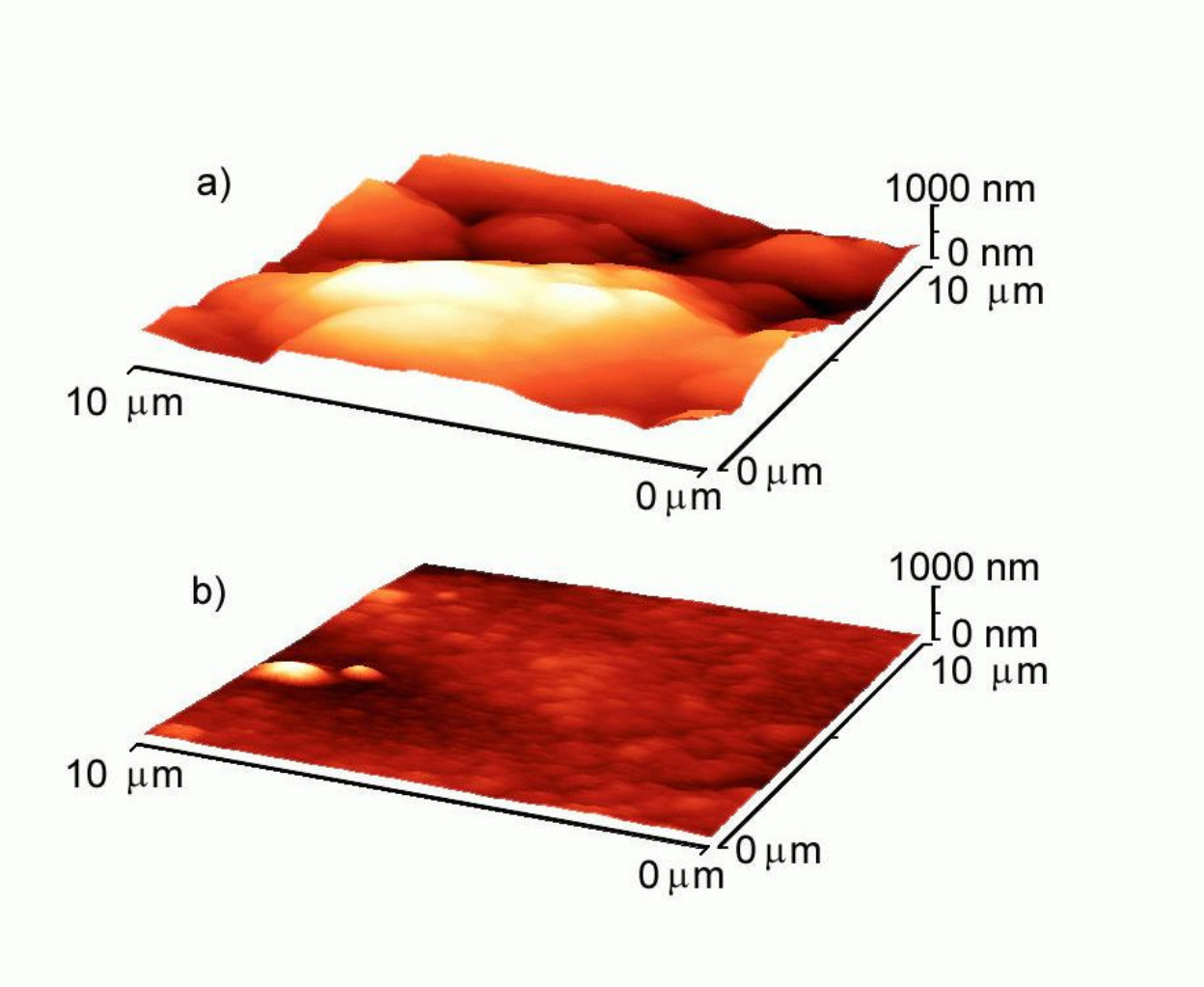

Fig. 2.3.1 a) AFM image of unetched CdTe surface.
b) Topography after etching into region near the CdS interface

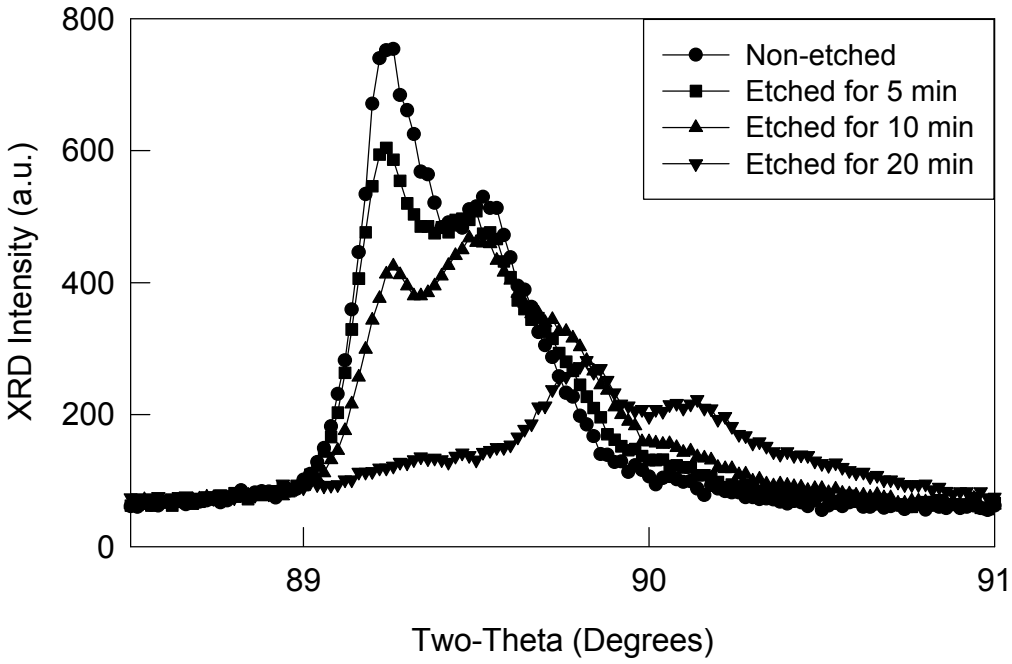

Fig. 2.3.2 XRD pattern of the CdTe 531 peak as a function of etch time

Photoluminescence

For $x < 0.2$ the band gap of $CdTe_{1-x}S_x$ decreases as S content increases [11,12]. In this study we used low temperature PL to monitor the shift in the band gap caused by the S diffusion. Using the relationship between energy gap and S content given in [12] and our PL measurements of the shift in the band gap as a function of depth, we were able to depth profile S content in the CdTe layer under various annealing conditions.

Fig. 2.3.3 shows an etch profile for a sample which was annealed at 350^0C and the band edge PL spectra obtained at various depths into the layer. The band gap of CdTe at low temperature (4.2K) is 1.606 eV. Excitonic luminescence (free and bound) in crystalline material tends to occur in the range of 1.585 to 1.596 eV while donor-acceptor luminescence is typically 30 mV or more lower in energy. These are 4.2 K values, however, at 15 K the band edge is only about 1 meV lower in energy [14]. The PL spectrum obtained from the thickest region of the sample in Fig. 3 (position e) has a peak energy of 1.581 eV. There is some sample to sample variation in the position of this peak with it occurring at

energies as high as 1.585 eV. It is also quite broad as generally observed for polycrystalline material. Based on the excitonic energies given above, we tentatively assigned this peak to excitonic luminescence. The presence of a small S content, residual strain, and even internal electric fields can all contribute to variation in the peak position and to a peak energy which is slightly lower than typical of bound excitons in crystalline material. In analyzing the S content, the origin of the band edge luminescence is less critical than its shift in position.

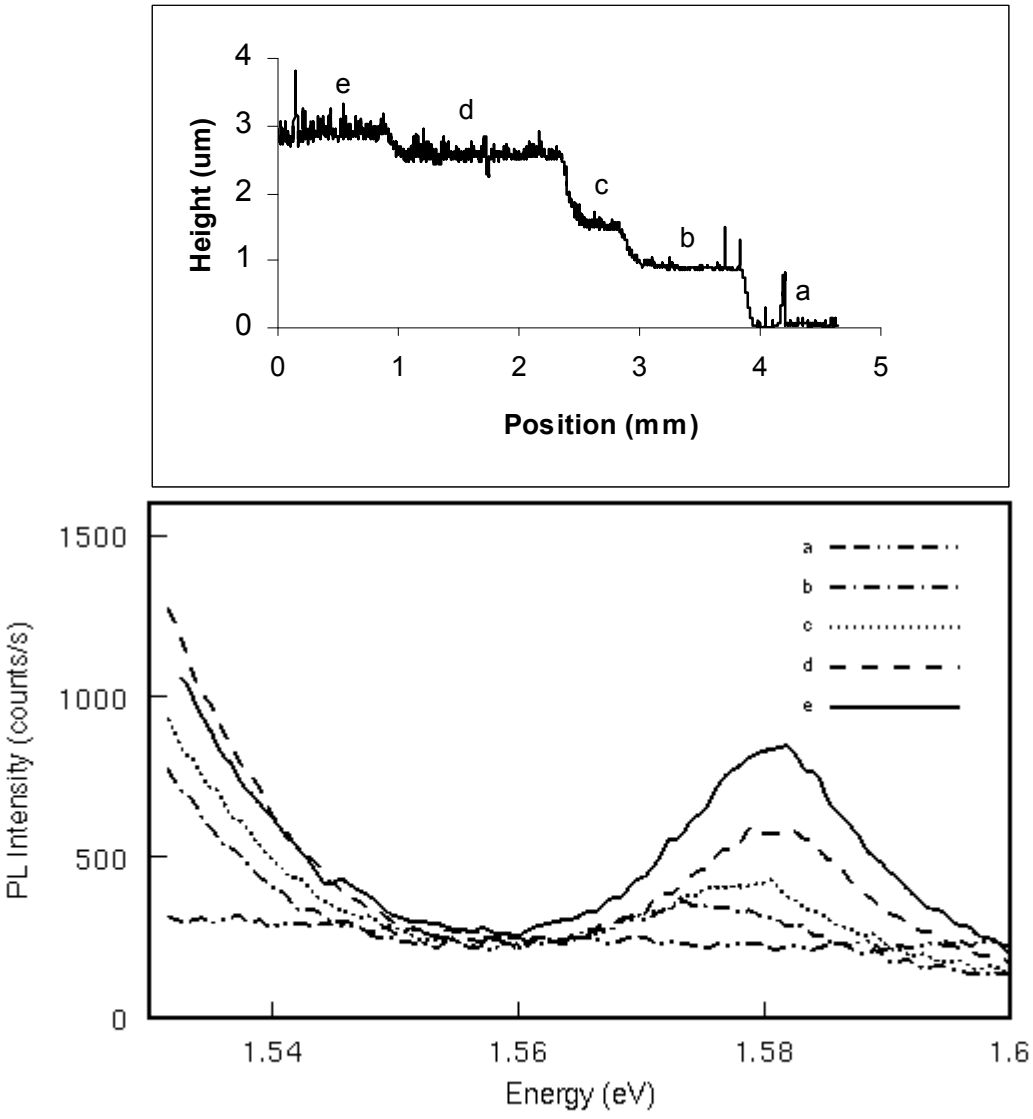

Fig.2.3.3 Etch profile and band edge PL spectra for a 350^{0}C anneal

The luminescence in Fig. 2.3.3 shifts to lower energy as measurements are made closer to the CdS interface, ending up about 7 meV lower in the region closest to the CdS. This shift can indicate increasing S content. Based on Ref. 3, however, a 7 meV shift would only correspond to an increase in S content of 0.7% which suggests the S concentration is quite low across the entire layer after a 350^0C anneal when compared to anneals at 410^0C and 450^0C as discussed next.

Fig. 2.3.4 shows PL spectra for a ample annealed at 410^0C. The spectrum obtained from the thickest region of the sample (the unetched surface) shows two distinct peaks. Most measurements we have made on material annealed at 410^0C exhibit this two-peak structure. As measurements are made closer to the CdS interface, the higher energy peak drops in amplitude (possibly decreasing slightly in energy), while the second peak shifts to lower energy indicating it arises from a ternary phase with a S concentration which increases with depth. The position of the higher energy peak near 1.584 eV is close to the peak energy after the 350^0C anneal and to excitonic energies in pure CdTe. We associated this feature with the presence of nearly pure CdTe. The coexistence of CdTe and a ternary $CdTe_{1-x}S_x$ phase is consistent with the XRD observations above, although in PL coexistence was only observed near the unetched surface, while in XRD it was observed throughout the layer. The energy difference between the CdTe and ternary peaks can be used to estimate the S concentration of the ternary phase as a function of depth. For curves shown in Fig. 2.3.4 we estimate S to vary from 1.5% at the surface to 4% near the CdS interface.

PL studies of the unetched CdTe surface were also made as a function of $CdCl_2$ treatment. We found in general that increasing the $CdCl_2$ exposure time increases the amplitude of the ternary peak relative to the CdTe peak (Fig. 2.3.5) in agreement with the view that $CdCl_2$ promotes interdiffusion. [3*,15].

PL measurements were also performed at room temperature (Drs. D.H. Levi and R.K. Ahrenkiel, NREL) on a sample annealed at 410^0C. A shift of the PL to longer wavelength with increasing depth was observed. The size of the shift was the same as found at low temperature. Room temperature PL arises from the band to band transitions rather than bound levels which makes it a more direct measurement of band gap energy. This supports our conclusion that the decrease in PL energy with depth is associated with a decrease in band gap and, therefore, with an increase in S concentration. Room temperature lifetime measurements gave a decay time of 300 ps. which did not vary significantly with depth.

PL spectra for a sample annealed at 460^0C are shown in Fig. 2.3.6. The PL peaks occur at an energy corresponding to the highest S content in the 410^0C anneal indicating that S has diffused throughout the film. The S concentration near CdS interface is estimated to be 5%. Fig. 2.3.7 summarizes the S concentration depth profiles determined by PL measurements on the samples annealed at 350, 410, and 460^0C.

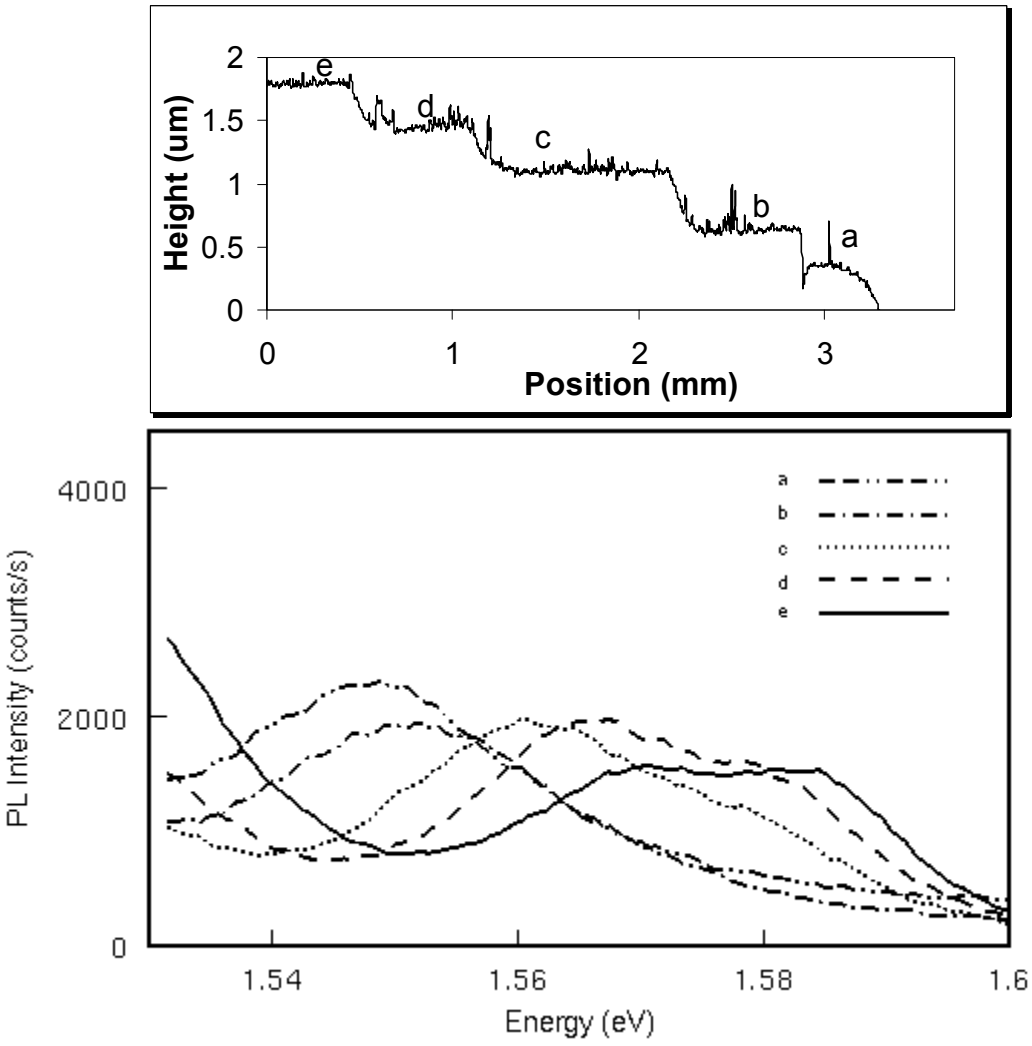

Fig. 2.3.4 Etch profile and band edge spectra for a 410^0C anneal

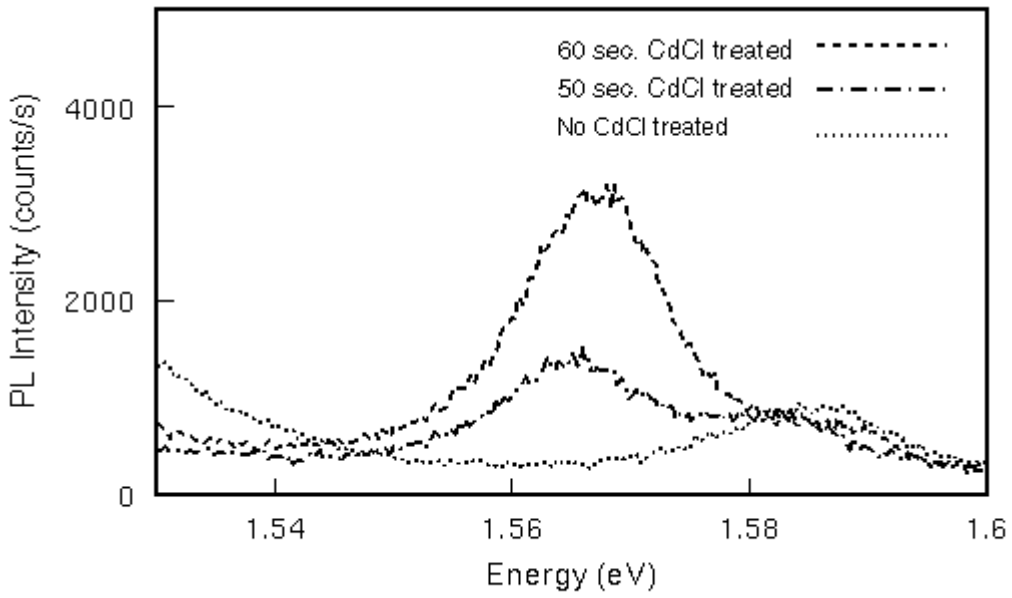

Fig. 2.3.5 Dependence of band edge PL on $CdCl_2$ treatment

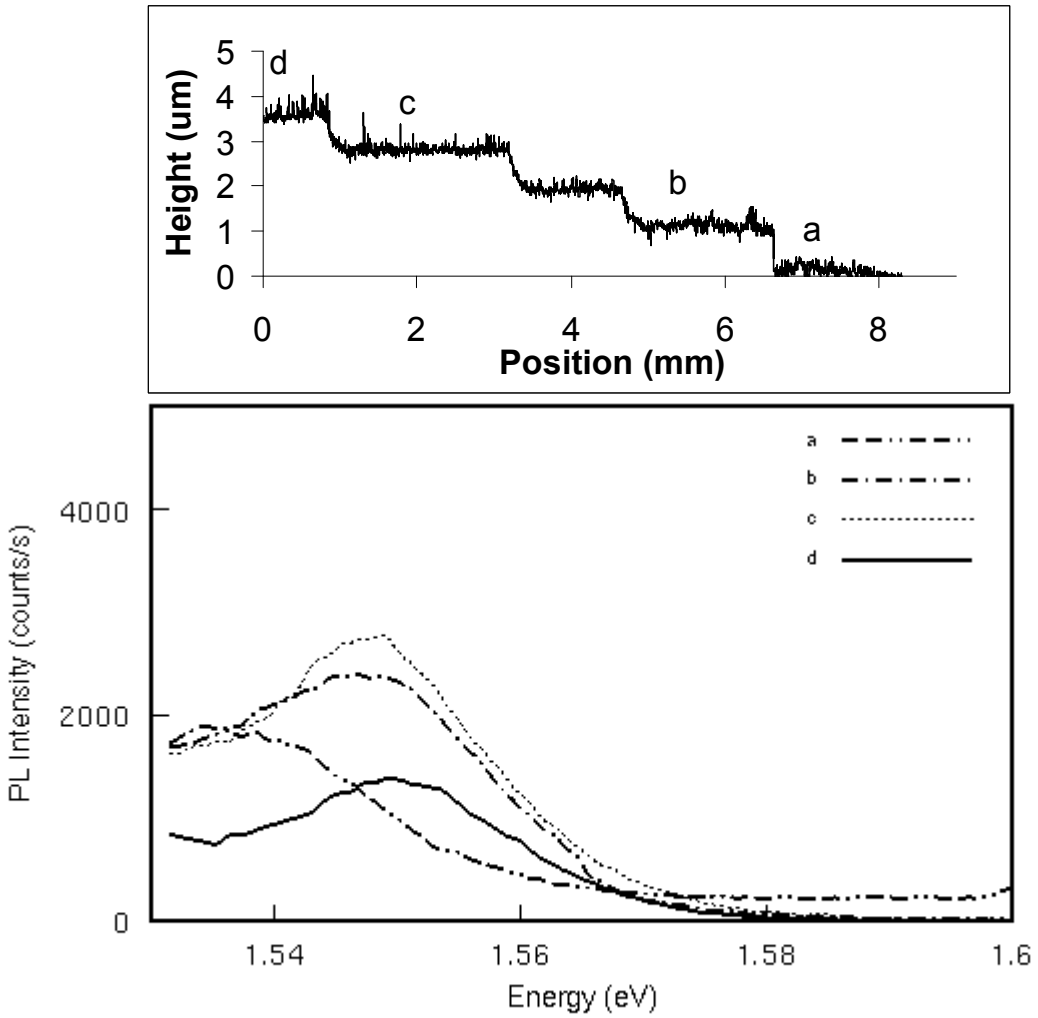

Fig. 2.3.6 Etch profile and PL spectra for a 460^0C anneal.

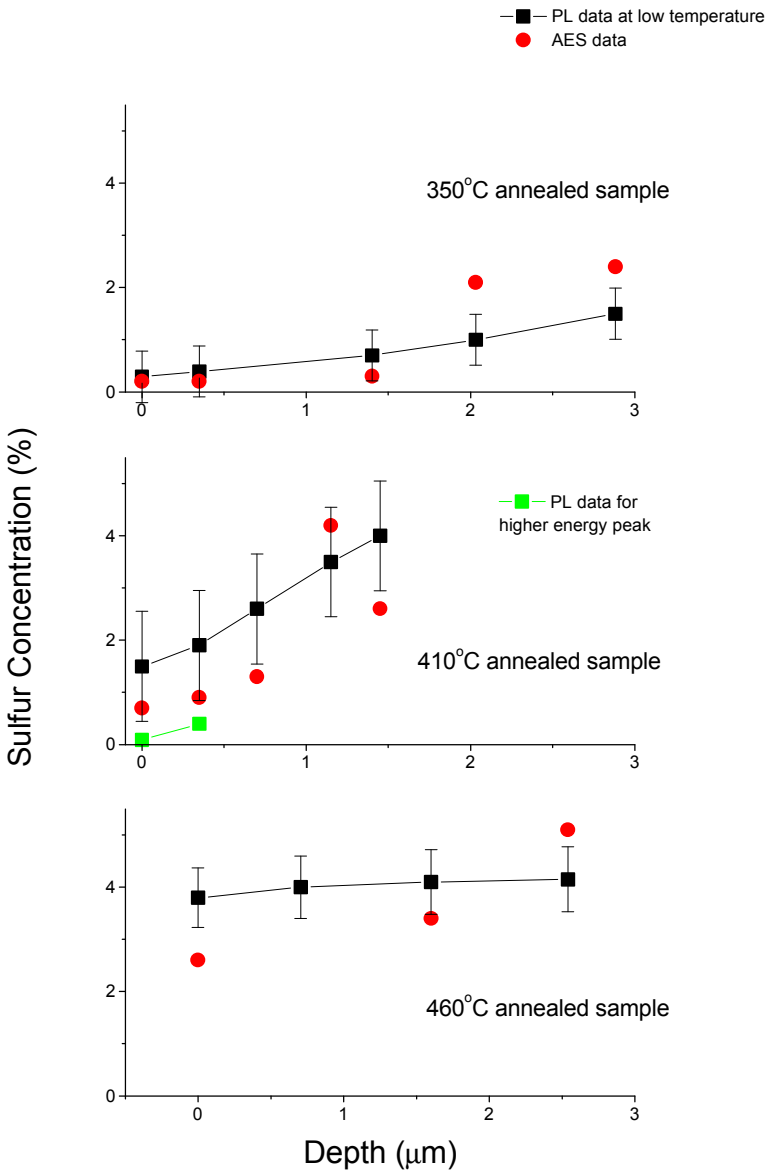

Fig. 2.3.7 Sulfur composition as a function of depth for various annealing temperatures

Discussion and Conclusions

(1) The agreement between XRD and PL results is really quite good considering some of the differences between the two techniques. For example, the x-ray penetration depth is estimated to be 2.5 μm which indicates XRD measurements, while weighted toward the top of the film, are sampling a large fraction of the film. The optical absorption length for 458 nm PL excitation is much smaller (less than 0.5 μm). However, carriers can move distances comparable to the minority carrier diffusion length before recombining to give off light. If a large and small band gap regions are within a diffusion length of one another, the PL measurements will be heavily skewed toward the lower bandgap region. In addition, the S compositions estimated from PL are dependent on our choice of the PL peak position in pure CdTe which could lead to an error of up to one percent in composition. With this in mind we obtain the following general conclusions:

- The amount of S which diffuses into the CdTe layer changes substantially between 350^0C and 460^0C.
- After a 410^0C anneal, nearly pure CdTe and $CdTe_{1-x}S_x$ coexist. The S content of the $CdTe_{1-x}S_x$ phase varies from 1% or less near the back contact to 4-5% near the CdS interface (for the 2μm thick sample used in this study).
- For all annealing temperatures studied here, the maximum S concentration is observed to be around 5% which is quite close to the S solubility limit at 415^0C of 5.8% reported in [16].

(2) The presence of distinct CdTe and $CdTe_{1-x}S_x$ phases within the film after 410^0C anneal is quite interesting. There is no reported evidence that phase segregation occurs for S compositions less than the 5.8% solubility limit. We might, therefore, expect diffusion to lead to a broad distribution in S composition and to one broad peak instead of two distinct sets of peaks in PL and XRD. S diffusion into the CdTe layer undoubtedly occurs preferentially along grain boundaries. Diffusion of S into individual crystallites can then occur from grain boundary as well as from the CdS layer itself. The grain regrowth which occurs during the anneal will also influence the S distribution [1*]. Several possibilities then exist for obtaining inhomogeneous S distributions. If S penetration along grain boundaries varies from boundary to boundary, the S concentration within individual crystallites will also vary. S diffusion into the grain from the grain boundary surface will lead to variation in S content across the grain. PL measurements might be more sensitive to grain-to-grain inhomogeneity than to variations in S content across the grain due to minority carrier diffusion as discussed above. Our XRD results in Fig. 2.3.2 indicate two phases are present across the entire film thickness, while in PL we only detect pure CdTe near the unetched surface. Based on this reasoning one can made the following presumable conclusion:

Pure CdTe and $CdTe_{1-x}S_x$ are separated further spatially, perhaps in separate crystallites, near the unetched surface.

2.4. Physical Properties of CdS Films Treated Under Different Conditions

(See also [1®, 3®, 6*, 14*])

2.4.1 Electrical Properties

The dark and light resistivity of CdS films grown by CBD using two different recipes (listed in Table 2.4.1) were investigated. The first recipe is characterized by a high solution concentration and a fast growth rate. The second recipe is characterized by a dilute solution and a slow growth rate. Films in their as-deposited state and those annealed at 450°C in nitrogen ambient, with and without $CdCl_2$ treatment, were studied. The results are summarized in Tables 2.4.2 and 2.4.3. The activation energy was determined from the slope of ln(ρ) vs. 1/T plots measured in the temperature range of 20 - 100°C. The energy bandgap obtained from optical absorption measurements is also listed.

One can notice several features from these data:

(1) The bandgap of as-deposited CdS is comparable for films grown with either method and is 60 - 70 meV smaller than the bandgap of single crystal CdS. After $CdCl_2$ treatment and annealing, the bandgap increases in both cases, approaching that of single crystal CdS (2.42 eV). For annealing without $CdCl_2$, however, variations of bandgap in opposite directions were observed for films deposited with the 2 different recipes. A large decrease of bandgap was observed for films deposited with the slow growth recipe, whereas a small increase was observed for films deposited with the fast growth recipe.

(2) The dark resistivity of as-deposited films differs significantly, by more than 5 orders of magnitude, for films deposited with the two different recipes. The fast-growth recipe yielded very high dark resistivity and the slow-growth recipe yielded relatively low resistivity.

Correspondingly, the activation energy is also much smaller in the latter case. After annealing, the dark resistivity reaches comparable values for both types of films.

(3) Films deposited by slow growth and annealed with $CdCl_2$ treatment showed the lowest resistivity under illumination (60 Ω-cm) and the highest dark-to-light resistivity ratio (4.7×10^5). The high conductivity under illumination and high dark-to-light resistivity ratio suggest a long lifetime of photogenerated majority carriers.

(4) For both as-deposited films and those annealed without $CdCl_2$ treatments, the photoconductivity decay is very slow. In some cases, several hours are required for the dark resistivity to reach a stable value. Such a slow decay of photoconductivity indicates the existence of a high concentration of traps. For films annealed with $CdCl_2$ treatment, the photoconductivity decay is very fast, with a time constant of the order of seconds. This indicates that the $CdCl_2$ treatment eliminated effectively the deep trapping centers.

Table 2.4.1. Recipes for chemical bath deposition of CdS

	$CdCl_2$ or $Cd(Ac)_2$	**Thiourea**	**NH_4Cl or NH_4Ac**	**pH**	**deposition rate (A/min)**
recipe#1	0.002 M	0.15 M	0.005 M	11	100
recipe#2	0.001 M	0.005 M	0.02 M	9.5	20-40

Table 2.4.2. Electrical Properties of CdS films prepared by fast growth (recipe 1).

	Dark ρ (Ω-cm)	**Light ρ (Ω-cm)**	**ρ_{dark}/ρ_{light}**	**Activation Energy (eV)**	**Bandgap (eV)**
As-deposited	2.0×10^9	3.3×10^5	6.0×10^3	0.70	2.36
Annealed w/o $CdCl_2$	5.6×10^7	2.0×10^3	3.0×10^4	0.54	2.39
Annealed with $CdCl_2$	1.6×10^7	1.1×10^3	1.5×10^4	0.50	2.42

Table 2.4.3. Electrical Properties of CdS films prepared by slow growth (recipe 2).

	Dark ρ (Ω-cm)	**Light ρ (Ω-cm)**	**ρ_{dark}/ρ_{light}**	**Activation Energy (eV)**	**Bandgap (eV)**
As-deposited	9.5×10^3	6.5×10^1	1.5×10^2	0.19	2.35
Annealed w/o $CdCl_2$	3.2×10^7	7.8×10^2	4.1×10^4	0.67	2.26
Annealed with $CdCl_2$	2.8×10^7	6.0×10^1	4.7×10^5	0.55	2.39

2.4.2 Optical Absorption and Photoluminescence (III).

CdS films were prepared by the CBD method on SnO_2-coated glass substrates and subjected to various post-deposition treatments:

A. No treatment;
B. Coating with $CdCl_2$ with following anneal in N_2 at 450^0C for 50 min;
C. Anneal in N_2 at 450^0C for 50 min. without $CdCl_2$ application.

Optical transmission spectra were studied using the Cary 5G UV-Vis spectrophotometer in our Laboratory. The spectra are presented in Fig.2.4.1. The dependence of transmission spectrum on treatment conditions is easily observed. Sample B ($CdCl_2$-treated) demonstrates the sharpest onset of transmission at the wavelength corresponding to the CdS bandgap (500 nm). The onsets for the two other samples are less steep and shifted toward lower photon energies. The differences in optical properties of the films subjected to different treatments are seen clearly in *differential absorption spectra* (DAS) measured by Dr. R.K. Ahrenkiel and his colleagues at NREL (Fig.2.4.2). The DAS peak for the sample B is the narrowest and located close to λ=500 nm. This peak is reasonable to attribute to band-to-band electron transitions. The peak for the non-treated sample, A, is the broadest one. Its maximum is located at 507 nm. We are prone to attribute this peak also to band-to-band absorption. As to its shift from 500 nm and broadening, we consider various possible explanations. The first one is that there exist high residual stresses in the as-deposited film. The bandgap depends on the stress type and value. These stresses are expected to be inhomogeneous. The stress averaged over the film area defines the maximum of the peak position; the fluctuations of stress define its broadening. Another explanation is that there are significant tails of density of states in the bandgap due to highly imperfect structure of unannealed films. These tails diminish the optical bandgap leading to the peak position shift. Defect density is heavily inhomogeneous in fine grain polycrystalline material, which causes the peak broadening. The sample annealed without $CdCl_2$ application (sample C) has a peak broader than sample B ($CdCl_2$-treated) and located at 535 nm (photon energy is by 160 mV lower than the CdS bandgap).

A possible explanation for this subband peak is some level (or narrow band) within the bandgap. If so, one has to conclude that the defects responsible for this peak are much less pronounced in un-treated or $CdCl_2$-treated films. As to the latter, basing on DAS, one can conclude that $CdCl_2$ treatment is much more effective than annealing itself in minimizing the density of the levels within the bandgap. Still we face a problem why we do not see band- to-band absorption in DAS for the sample C which was annealed without $CdCl_2$.

Room temperature *PL spectra* measured on the same films (Dr.Ahrenkiel et al. at NREL) are different from DAS (see Fig.2.4.3). Only the $CdCl_2$-treated sample B has a PL peak (510 nm) close to the DAS one (500 nm) but it has also two broad peaks at longer wavelengths: 610 nm and 750 nm. The unannealed sample, A, has two peaks in the studied wavelength range: 548 nm and 686 nm. The sample annealed without $CdCl_2$ has a well pronounced and rather narrow peak at 555 nm and a broad one at λ>750 nm. Similar

discrepancies between PL and differential absorption (DA) spectra were observed and discussed also in [17] for the CdS films prepared by different methods or subjected to different treatments as compared to our films.

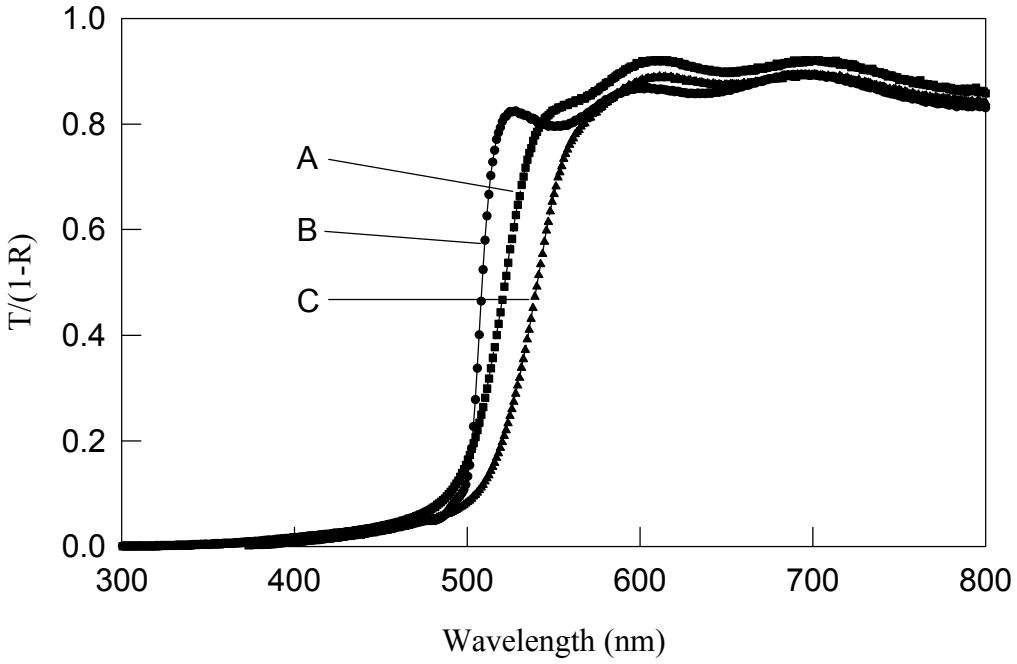

Fig. 2.4.1 Optical transmission spectra of thin-film Samples CdS/SnO_2/Glass subjected to different post-deposition treatments: A- unannealed; B and C - annealed in N_2 at 450^0C for 50 min with (B) and without (C) preliminary $CdCl_2$ coating

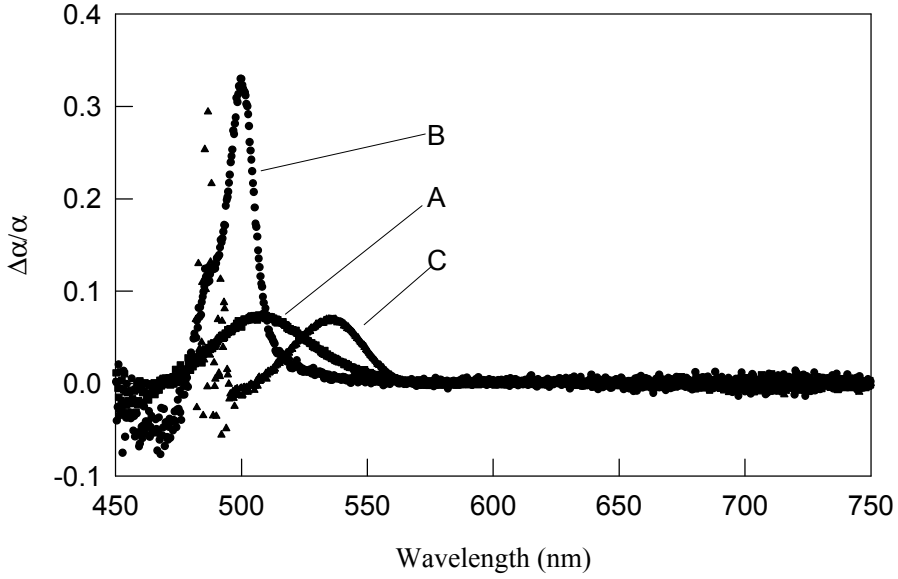

Fig. 2.4.2 Differential absorption spectra of the samples as at Fig. 2.4.2

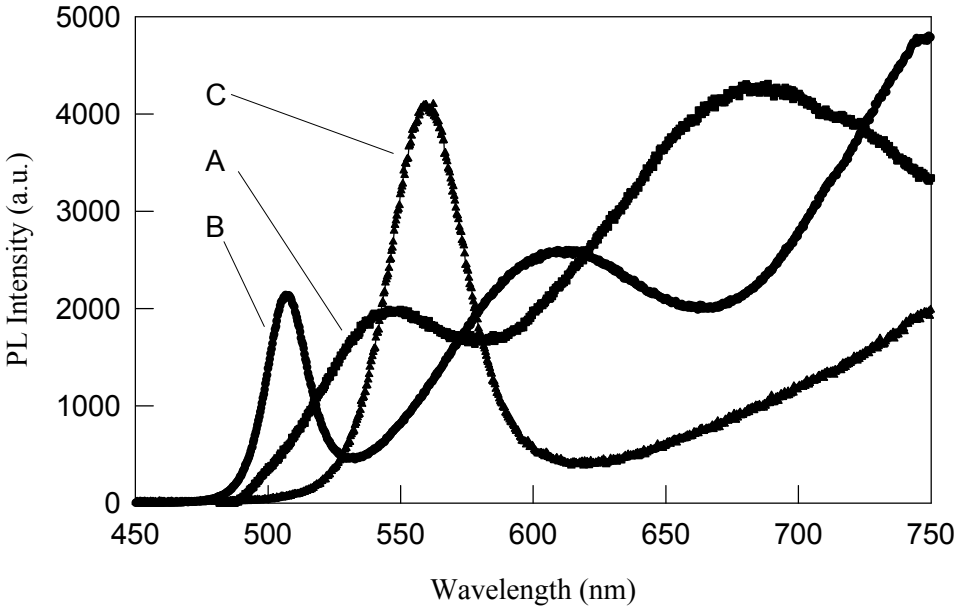

Fig. 2.4.3 Photoluminescence spectra of the samples in Fig. 2.4.1

One of the possible explanations proposed in [17] for the complete absence of PL where the DAS shows a peak (e.g., the peak in DAS close to 500 nm for our sample A) is that only one type of charge carrier remains in energy states at or near the band edge. There would still be a signal in DAS because of occupation of either the initial or final state involved in the absorption process. On the other hand, there would be no PL because radiative recombination requires both electrons and holes. Since CdS is n-type, one must conclude that the hole lifetime in the valence band is very small , e.g., due to the hole recombination with the majority electrons through the recombination centers. It seems to be a reasonable explanation for the most defective unannealed sample A. For the $CdCl_2$-treated sample B, which is believed to be the most perfect, we have a PL peak close to that in DAS. A small shift toward lower photon energies can be ascribed to the excitons.

A second discrepancy discussed in [17] is the absence of the DA signal where there is a strong PL signal (as regards our samples, that is an issue for all the PL peaks with wavelengths greater than 535 nm). This will occur if either the initial or final state involved in the PL transition is not available for an absorption transition. The authors of [17] consider the *Franck-Condon effect* as a probable reason for this situation. They suggest that after photoexcitation the holes are very rapidly captured by deep traps. These transitions produce the PL observed in a long-wave range. Due to the occupation of the level by the hole the defect center reconstructs, which means a change in crystallographic surrounding of the center. It may be the Coulomb polarization of the lattice due to the additional positive charge acquired by the center (center-symmetric deformation) with a corresponding decrease in the energy of the charged center. It also may be non-symmetric deformation which splits the degenerate level and in this way decreases the energy of the defect occupied by the carrier (similar to the Jahn-Teller effect for molecules). In both cases the final energy of a system "defect+carrier" due to the lattice relaxation is lower than that immediately after hole capturing. Therefore, to excite the captured hole from the reconstructed center to the valence band one needs a photon of higher energy (shorter wavelength) than that emitted at the capturing of a hole by the deep trap (PL). According to this concept the PL peak for some defect must be shifted to the longer wavelengths with respect to the corresponding DAS peak.

The Franck-Condon effect due to polarization is well pronounced in the II-VI semiconductors because of their highly ionic lattice structure [18], hence the explanation above seems quite probable. That means that in principle it is possible to relate each peak in the PL spectra to some peak in DAS or vice versa. If one is successful in doing that, this could be the way to bring us closer to the localized electronic states identification and better understanding of their nature. Right now it does not seem possible for our films, because for each film (A, B, and C) we have at least two PL peaks that should be related to some localized states in the bandgap, while among the peaks detected by DAS only one (535 nm, sample C) can be related to some level in the bandgap for certain. As discussed above, two other peaks in DAS in Fig. 2.4.2 (500 nm for sample B and a broad peak shifted a little bit from 500 nm for sample A) may be identified as corresponding to band-to-band transitions. Nevertheless, this direction of studies may be fruitful and deserves to be continued.

2.4.3 Photoconductive Lifetime (III)

Annealing of CdTe/CdS structure leads to considerable interdiffusion that affects significantly the electronic properties of both layers. Interdiffusion studies (see Sec.2.3.1) performed on the cells fabricated at CSM showed that $CdCl_2$ application before CdS annealing (pre-treatment stage) minimizes Te diffusion into the CdS [6*]. If CdTe is deposited on the as-deposited CdS, the latter is fully converted to $CdS_{1-y}Te_y$ (y estimated to be 0.045) after the final anneal of the CdTe/CdS structure. However, only a negligible portion of the $CdCl_2$-treated CdS is converted to the ternary phase. A radical reduction of Te concentration in the CdS is beneficial for the reason that the bandgap in the ternary phase decreases as y increases [12]. Indeed, the spectral response of the cells fabricated with $CdCl_2$-treated CdS shows a sharp increase at the wavelength corresponding to the CdS bandgap (500 nm) and a very high quantum efficiency between 500 and 600 nm. Probably, the increase of photon flux reaching the CdTe layer is the major reason for the short-circuit current (J_{sc}) increase of about 13.5% in comparison with the cells using CdS which did not receive the $CdCl_2$ treatment.

There might also be other mechanisms which in principle lead to the J_{sc} increase. One of these is the suppression of recombination in the CdS due to minimizing of the concentration of recombination centers. The heat-treatment in the presence of $CdCl_2$ promotes grain growth of the CdS films, hence reduces the density of deep electronic states connected with the grain boundaries. The recombination rate can also be diminished due to decreasing Te concentration in $CdCl_2$-treated CdS. It was found in [17] that "... Te defect centers act as radiative recombination centers and shorten the lifetime of holes in n-CdS." To check this conclusion with respect to our processing procedure *the photoconductivity decay rate* was studied in CdS films subjected to various treatments. Measurements of *radio-frequency photoconductive decay* (RFPCD) were performed by R. Ahrenkiel et al. at NREL on the CdS films A and B described above and also on CdTe/CdS films. The latter will be represented below by two samples that were processed in different ways:

Sample D: CdTe was deposited on as-deposited CdS layer (on sample A above); the CdTe/CdS structure was coated with $CdCl_2$ and annealed in air at 410^0C for 45 min (Te diffusion into CdS should be well pronounced according to Sec. 2.3.1);

Sample E: CdTe was deposited on a CdS layer pre-treated with $CdCl_2$ (on sample B above); the CdTe/CdS structure was treated as for sample D (only a negligible amount of Te in the CdS).

Films were illuminated from the CdS side using the tripled YAG wavelength of 335 nm as the excitation source. The TCO layer is transparent for this radiation. The absorption coefficient of CdS is higher than 10^5 cm^{-1} for this wavelength [17]. Thus, practically all the light is absorbed in the CdS layer. That is confirmed by transmission spectra in Fig.2.4.1.

The RFPCD response V(t) for films A and B is shown in Fig. 2.4.4. There is no significant qualitative difference between untreated (A) and $CdCl_2$-treated (B) films. This kind of decay is usually considered as evidence of trap-limited response of fine grain polycrystalline materials [5].

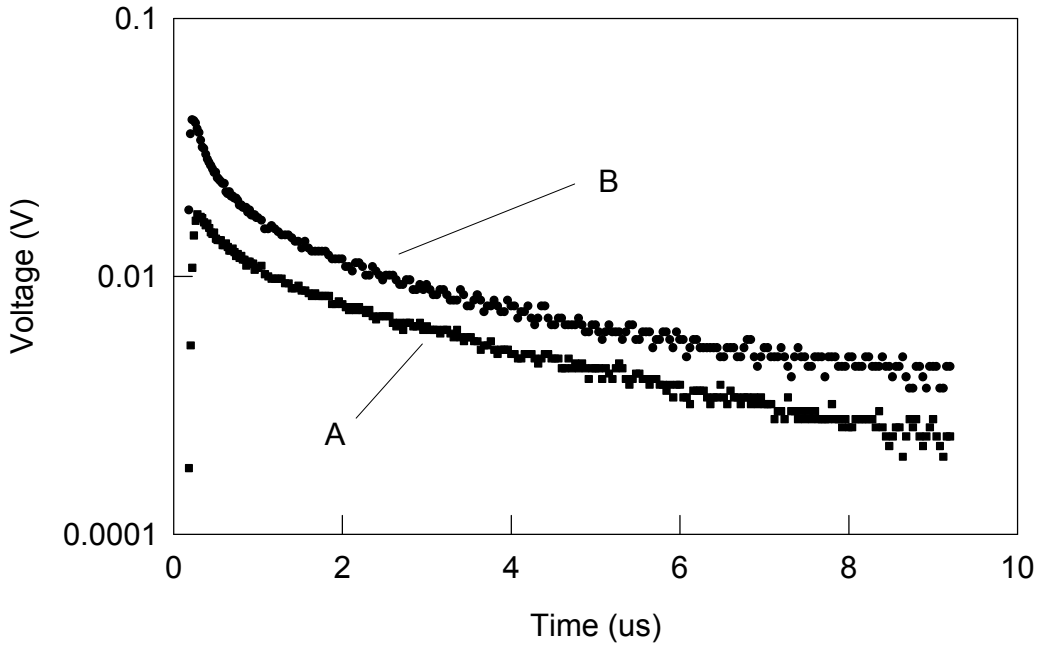

Fig. 2.4.4 RF photoconductive decay (RFPCD) response for two CdS films: A and B are the same as in Fig. 2.4.1

An instantaneous relaxation time (decay time), τ, defined from V(t) dependence using the expression:

$$\tau=-(d\ln V/dt)^{-1} \quad ,$$

is presented in Fig. 2.4.5 for the films of A and B types of a thickness 120 nm.

Initial decay time is about 1 μs for the untreated sample A, and about 0.4 ms for the $CdCl_2$ -treated sample B. The value of τ increases with time of observation, *t,* achieving approximately 7 μs at *t*=8 μs for sample A and about 12 ms for sample B. Probably, the curves in Figs.2.4.4 and 2.4.5 represent a transition region between photoconductivity limited by carrier recombination (fast decay) and photoconductivity limited by emission of holes captured by shallow traps in n-CdS (slow decay). Unfortunately, we are not able to determine the recombination time because there is no portion of the curve with constant slope. At the same time the initial RFPC signal is considerably larger for the treated sample B than for the untreated A. That can be attributed to a higher concentration of

recombination centers in the as-prepared, non-treated sample A. The time of observation was too short for achievement of saturation of the $\tau(t)$ dependence. Thus we were not able to define the real hole emission rate from traps which is helpful for distinguishing different types of traps.

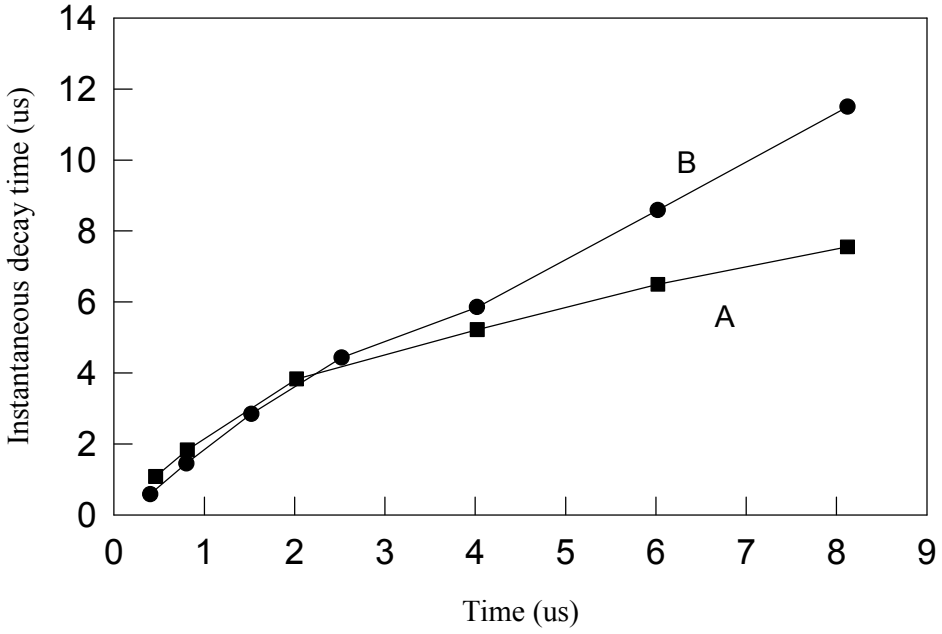

Fig. 2.4.5 Instantaneous (momentum) decay time for A and B samples calculated from the data in Fig.2.4.4

Fig. 2.4.6 shows the RFPCD response for sample D (CdS was not pre-treated before CdTe deposition). The measured RFPC signal is rather small, not exceeding the noise level at t>10 μs. There is no evidence of any fast decay at the initial portion of the curve. The decay time τ is constant (about 6 μs) over the whole range of the observation time t=1-18 μs (see Fig. 2.4.7). One can suppose that trap-limited recombination dominates in this film and t=6 μs is defined by the hole emission rate from traps. RFPCD response is quite different for the sample E (Fig. 2.4.6). Like samples A and B we see here a transition from a region of band-to-band recombination (radiative or through recombination centers) to a trap-limited region. But contrary to A and B, sample E demonstrates saturation in its τ(t) dependence. The long-term decay time is about 40 μs. This is about 7 times higher than for sample D which can be explained by a different nature of the defects responsible for traps in these two samples. Another impressive distinction is a much higher (almost by 2 orders of magnitude) RFPC signal in sample E. That can be explained by a much slower

recombination rate in this sample, that is a much lower concentration of recombination centers.

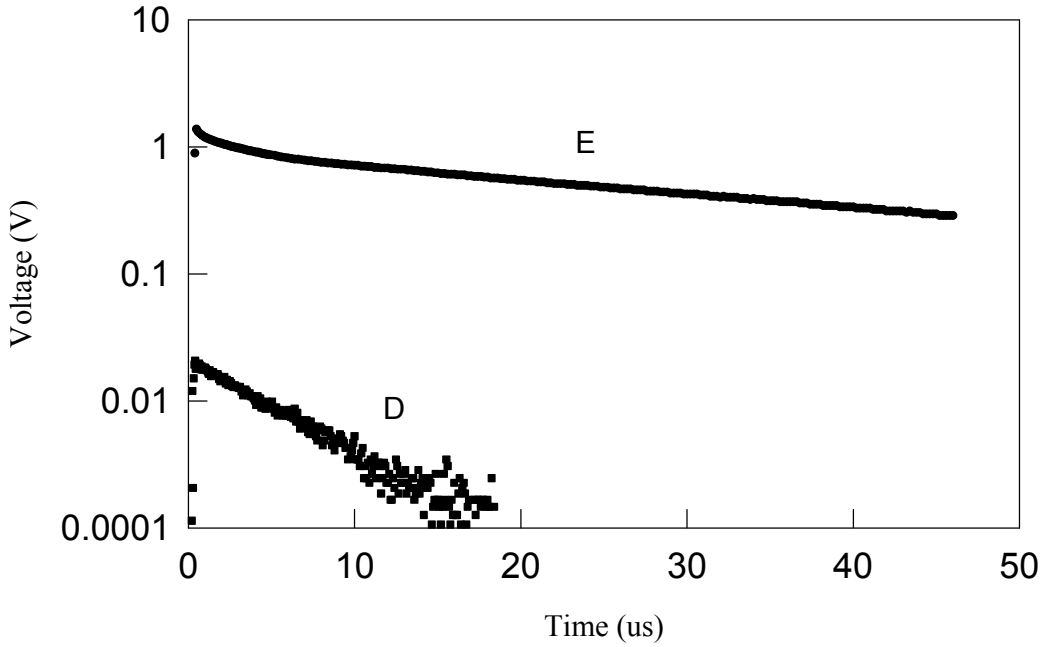

Fig. 2.4.6 RFPCD response of CdS films coated and annealed with CdTe (air, 410^0C, 45 min), D - untreated and E - treated before CdTe deposition (coated with $CdCl_2$ and annealed in N_2 at 450^0C for 50 min).

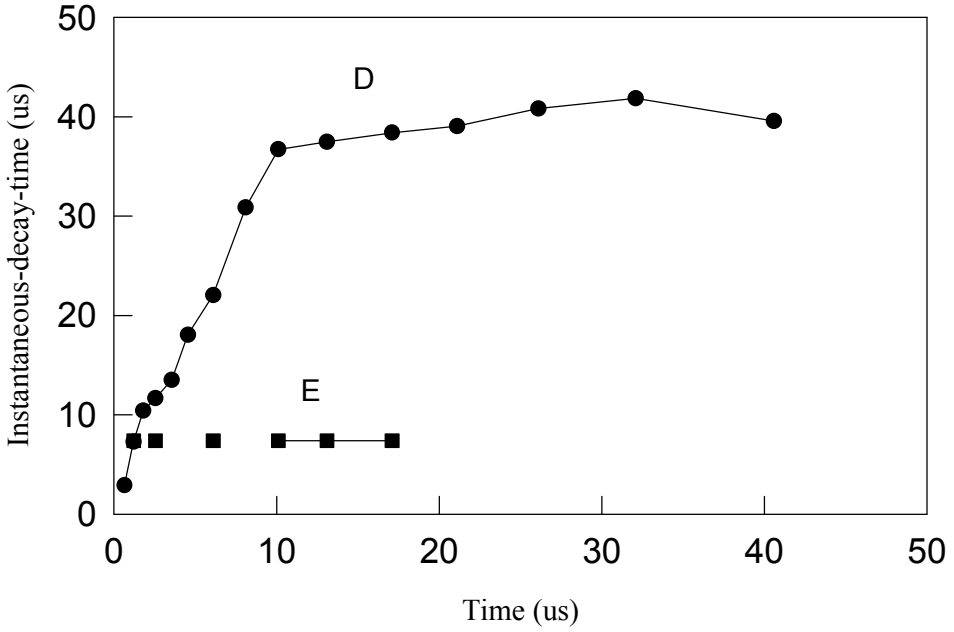

Fig.2.4.7 Instantaneous decay time for samples D and E (the same as in Fig. 2.4.6)

Comparing samples D with a high concentration of Te and E supposedly with a small Te amount, one can conclude:

1. The density of recombination centers is much lower for sample E.
2. The recombination centers in sample D (with a high amount of Te) may be attributed to Te- related defects because their density is lower by orders of magnitude in sample E where the Te amount is negligible.
3. The traps are different in nature for samples D and E which follows from the significant difference in the hole emission rates. Maybe the traps in sample D are Te-related.
4. The nature of traps in sample E is unclear. It can not be excluded that they are of the same nature (but, probably, not of the same density) as in samples A or B that were not coated with CdTe and therefore did not contain Te. Unfortunately, RFPCD was measured in these two samples in much narrower range of time (t=0-8 μs) than in sample E (0-45 μs). But in the same range of t the decay times are comparable.

Thus minimization of Te concentration in the CdS layer by $CdCl_2$-pre-treatment increases the lifetime of the light-generated carriers in the CdS and can contribute to the observed increase in J_{sc}. In the cell fabricated on sample D, J_{sc}=20.5 mA/cm^2 and on sample E, J_{sc}=23.2 mA/cm^2. Unfortunately, we are not able yet to separate this contribution from the increase in bandgap due to elimination of the ternary phase.

2.5 Optimization of CdTe/CdS Structure

2.5.1 Effect of the CdS and CdTe thicknesses
(See also [1®])

The high proportion of the ternary $CdTe_xS_{1-x}$ phase in the CdTe layer implies significant consumption of the CdS layer. Based on the relative intensity of XRD peaks corresponding to the binary and ternary phases, approximately 70% of the CdTe is converted to $CdTe_xS_{1-x}$. This would predict a decrease of CdS film thickness of ~60 nm for the CdTe film thickness used (3.4 μm). Indeed, after the CdTe layer was removed after the annealing and interdiffusion process, the CdS film thickness was found to have decreased from 240 nm to 165 nm, representing a 75 nm reduction. The large reduction of CdS film thickness can also be noticed when we compare CdTe/CdS cells fabricated with electrodeposition and with closed-spaced sublimation (CSS). CSS is known to produce CdTe films with large grains and better crystallinity, which lead to less interdiffusion and less CdS consumption. On the other hand, electrodeposition and other low temperature processes produce CdTe films with much smaller grains, which lead to more significant interdiffusion and CdS consumption. This high CdS consumption caused by CdTe-CdS interdiffusion is expected to play a critical role in determining the smallest CdS thickness that can be employed in CdTe/CdS solar cells fabricated with low temperature processes.

We investigated the effect of the CdS and CdTe thicknesses on the photovoltaic performance of CdTe/CdS cells. The results are shown in Tables 2.5.1. and 2.5.2. As expected, J_{sc} of the cells decreases monotonically with increasing CdS thickness because of the increased absorption in the window layer. However, high V_{oc} and efficiencies were obtained only for CdS thicknesses above 1500 Å. Cells with very thin (700 Å) CdS exhibit low efficiency, caused mainly by a low V_{oc}. The highest efficiency was obtained for a CdS thickness of 1500 Å. The CdTe thickness was varied from 2.2 μm to 5.3 μm. A CdTe thickness of 2.2 μm, typical of most studies using electrodeposited CdTe, yielded V_{oc} values in the low 700 mV range. An increase of CdTe thickness to 3.4 μm led to a significant improvement in V_{oc}, by ~70 mV. The highest V_{oc} obtained at this CdTe thickness exceeded 800 mV. Further increase of the CdTe layer thickness to 5.3 μm, however, resulted in low shunt resistance and low efficiencies of the cells.

Table 2.5.1. Effect of CdS thickness on the photovoltaic performance of CdTe/CdS cells.

CdS thickness (Å)	Voc (mV)	Jsc (mA/cm^2)	FF(%)	η (%)	Rsh (Ω-cm)
700	645	24	54	8.3	550
1500	780	23	72	12.9	1800
2300	775	22	69	12	2500
2500	765	21.5	70	11.6	2200

Table 2.5.2. Effect of CdTe thickness on cell performances.

CdTe thickness (μm)	V_{OC} (mV)	J_{SC} (mA/cm^2)	R_{sh} (Ω-cm)
2.2	708	22.9	890
3.4	775	22.8	800
5.3	757	22.8	210

SEM measurements were performed on CdTe films of various thicknesses after $CdCl_2$ treatment and annealing. The average CdTe grain size was larger for the thicker CdTe films. This increase of grain size may explain the improved V_{oc} obtained with 3.4 μm CdTe. The deteriorated cell performance obtained with 5.3 μm CdTe is caused by the poor adhesion of CdTe on the substrate and the formation of shunting paths in the CdTe layer during the post-deposition annealing.

Our systematic investigation and optimization of the processing conditions has led to consistent improvement of the efficiency of CdTe/CdS/ZnTe cells we fabricate (our studies of ZnTe/Metal back contact are presented in Sec. 3). An efficiency as high as 12.9% was measured at NREL for our cell with an area of 0.1 cm^2. The cell yielded a V_{oc} of 0.778 V, a J_{sc} of 22.4 mA/cm^2, and a FF of 74.0%. In terms of individual parameters, we have obtained V_{oc} values over 0.8, and FF values of 76%.

2.5.2 Other approaches to the further improvement of CdTe/CdS processing (III)

(See also [3®])

Studies briefly described below were aimed at optimization of the CdTe/CdS post-deposition treatment. Although some results are indicative, these studies must be considered as only the first steps; they must be continued and extended.

(1) SEM images of CdTe/CdS structures before and after anneal at 410^{0}C for 45 min with a preliminary coating with $CdCl_2$ (our standard postdeposition treatment) show that a CdS layer that is rather uniform in thickness before anneal becomes significantly non-uniform after anneal. That means that, although due to interdiffusion the average thinning of the CdS is 60 nm for our standard procedure, initial CdS thickness should be significantly higher to prevent shorts between the CdTe and TCO layers. An alternative way is to decrease the duration of the post-deposition anneal which will lead to smaller CdS consumption and, supposedly, to less non-uniform thickness of the rest of the CdS layer.

To investigate this alternative way, cells were prepared with a CdS initial thickness of 130 nm (typical thickness is 200 nm). The back contact was produced by a simplified procedure: Au was deposited on the surface of the CdTe without a ZnTe interlayer. After CdTe electrodeposition, the structure was coated with $CdCl_2$ and annealed in air at 410^{0}C for various times. In agreement with our expectations it was found that shortening of the anneal time led to an increase in V_{oc} and shunt resistance. Indeed, our standard anneal

duration of 45 min. resulted in V_{oc}=510 mV and R_{sh}=120 Ohm-cm$^{2.}$. For a 15 min. anneal, both V_{oc} and R_{sh} were considerably higher: 635 mV and 160 Ohm-cm^2, respectively. One should not pay much attention to low cell parameters which were caused by the small CdS thickness and absence of a ZnTe interlayer. Thus shortening of the post-deposition treatment minimizes the deteriorative influence of CdS consumption by the CdTe. But we face another problem. This short anneal can lead to an insufficient degree of S diffusion into the CdTe. To check this assumption and also to inquire into alternative approaches to S diffusion control, additional experiments were performed.

(2) The cells were fabricated using a non-standard processing procedure for CdTe/CdS structure preparation. A thin CdS layer was deposited by CBD on the top of the CdTe. This "sandwich" structure (CdTe layer between two CdS layers) as usual was coated with $CdCl_2$ and annealed at 410^0C in air. Before back contact application, the top CdS layer was removed. The cells were completed by Au back contact as before. This new procedure was expected to provide greater sulfur content in the CdTe and more uniform distribution. It can be seen from Table 2.5.3 that the new procedure leads to a considerable improvement of the cell parameters.

Table 2.5.3. Comparison of the cells fabricated with a single CdS layer and "sandwich structure"

CdS/CdTe structure	**Anneal time (min)**	**η (%)**	**V_{OC} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**R_s (Ω-cm^2)**	**R_{sh} (Ω-cm^2)**
standard	15	5.3	635	17.7	47	20	160
sandwich	15	8.75	722	21.5	56	8.9	200
sandwich	22	9.4	771	20.8	58.5	7.9	250

Based on material of this section one can conclude that there really exists some room for further cell improvement by optimization of the CdS/CdTe processing.

3. ZnTe:Cu/METAL BACK CONTACT ON CdTe/CdS SOLAR CELLS

The formation of stable, low-resistance contacts to p-type CdTe is critical for the achievement of high efficiency and long-term stability of CdTe thin-film solar cells. Because of the rather high work function of CdTe and the difficulty of achieving high doping levels in p-type CdTe, a low-resistance ohmic contact cannot be formed by a simple metallization. Chemical reactions between CdTe and some of the high work function metals (e.g., Au) also make it difficult to form a stable ohmic contact by metal deposition. ZnTe, which is expected to have a small valence band discontinuity with CdTe and can be doped degenerately with Cu, has been used as an intermediate layer between the high-resistivity CdTe and the metal contact [20, 21]. Incorporation of a thermally evaporated Cu-doped ZnTe contact in CdTe/CdS cells yielded an efficiency of 11.2% [20,21], a record efficiency for thin-film solar cells at that time. Subsequently, other groups have investigated the deposition and properties of ZnTe thin films in relation to their application in thin-film CdTe solar cells [22-24].

We studied the effects of Cu concentration, ZnTe:Cu layer thickness, ZnTe post-deposition annealing temperature, and contact material to the ZnTe on the photovoltaic performances of CdTe/CdS solar cells. ZnTe films doped with Cu were deposited by vacuum co-evaporation. The ZnTe and Cu deposition rates were measured by separate thickness monitors. The typical deposition rates of the ZnTe were 5-10 Å/s. The deposition rate of the Cu was adjusted to a value between 0 and 0.2 Å/s to obtain the desired Cu atomic concentration in the ZnTe, varying between 4 and 10%. During vacuum deposition, the substrates were held at room temperature.

Concurrently with the ZnTe back contact studies we also investigated ZnTe thin films on the glass substrates prepared with the same processing procedure. That helped us to study and better understand the electronic properties of the ZnTe interlayer and optimize dopant concentration and post-deposition conditions.

3.1 Study of Cu Doped ZnTe Thin Films

(See also [2®, 4®, 5*, 11*, 12*]

The study involved the crystallographic structure, morphology, electrical and optical properties of vacuum evaporated ZnTe:Cu thin films. For application as an interface layer in the back contact, low temperature processing would be preferred, so our study of the film properties was limited to temperatures below 450^0C.

3.1.1 Crystallographic Structure, Morphology and Composition

The structure of the Cu doped ZnTe films prepared by our vacuum evaporation system was studied with XRD. The films were deposited on cleaned micro-analysis glass slides (soda-lime glass); the film thickness was of 800 nm. The crystalline phase of ZnTe

showed a dependence on Cu doping level, [Cu]. As-prepared ZnTe films without Cu showed cubic (zincblende) structure with a preferred orientation of <111>. As-prepared films with low [Cu] (<6 at. %) exhibited a mixture of cubic and hexagonal (wurtzite) phases. The lower the Cu concentration the lower the total amount of hexagonal phase in the films. Cubic phase dominated in the films with 2 at.% Cu, whereas hexagonal phase dominated in the films with 6 at.% Cu. When [Cu] exceeded 6 at.% (up to 13 at.%), only hexagonal phase was detected.

Phase transformation under anneal took place in the films where hexagonal phase existed. The amount of hexagonal phase decreased with increasing annealing temperature. After annealing at 350 ^{0}C, films with low Cu content retained a zincblende structure. The grain size grew as indicated by sharper diffraction peaks. In films with high Cu contents, the cubic phase dominated after annealing and only a very small amount of the hexagonal phase remained. Films with smaller thicknesses (250 and 80 nm) showed the same phase transition processes. However the temperature of hexagonal to cubic phase transformation was lower for thin films. For films of 80 nm thickness and high [Cu] only the cubic phase was observed after annealing.

There have been reports for the vacuum evaporated ZnTe films without Cu doping that these films exhibited cubic or hexagonal phases depending on the Zn and Te ratio, which is determined by deposition conditions, such as substrate temperature, Zn and Te partial pressure, and film thickness [25]. It was found for the first time in our study that the formation of cubic and hexagonal phases depends also on Cu concentration.

The grain size of ZnTe calculated from the linewidth of the XRD peaks was in a range of 20 to 50 nm. Thicker films, lower deposition rates, and higher substrate temperatures led to larger grain size. Post-deposition annealing increased the grain size. The grain size and morphology of the films with different Cu concentrations and annealing temperature were studied closely by Atomic Force Microscopy (AFM). A well pronounced effect of aggregation at T>350-400^{0}C has been observed. This effect is undesirable for the ZnTe back-contact interlayer. When the latter is applied to the top of the CdTe, aggregation of the ZnTe leaves some portion of the CdTe surface uncoated, that is in a direct contact with the metallization. The contact resistance in these uncoated area would be higher. To avoid this phenomenon, post-deposition treatments of the ZnTe must be conducted at not too high temperature (<350^{0}C).

Wavelength-dispersive electron spectroscopy (WDS, Cameca model MBX electron microprobe) was used for compositional analysis. The analysis was performed on a series of ZnTe:Cu films with nominal Cu concentrations (detected by rate monitors) ranging from 1 at. % to 8 at. %. Films were deposited on conductive SnO_2-coated glass. The WDS technique requires ZnTe films with thicknesses close to or larger than one micron to obtain accurate results. Films with 800 nm thickness were used for the study. Cu concentration detected by WDS was somewhat higher than the nominal value. It was found that at low Cu concentrations (< 6 at. %), there is a deficiency of cations, $(C_{Zn} + C_{Cu}) / C_{Te} < 1$; at Cu concentrations higher than 6 at. %, the cation concentration exceeds the anion

concentration, $(C_{Zn} + C_{Cu}) / C_{Te} > 1$. Combined with the XRD results, these data lead to the suggestion that hexagonal phase is associated with anion deficiency whereas cubic phase is associated with cation deficiency. This is similar to the case of ZnTe films without Cu doping. The fact that the ratio of cation to anion increases as the Cu concentration increases is consistent with the observation of reducing lattice constant with increasing Cu concentration. The atomic size of the cation (Zn and Cu) is smaller than that of the anion (Te).

3.1.2 Electrical and Optical Properties

Electrical resistivity (r) of the films in the lateral direction was measured using the two-probe method or van der Pauw four points method along with the Hall effect measurement. Measurements of the temperature dependence of resistivity with increasing ($T\uparrow$) and decreasing ($T\downarrow$) temperature indicated that some irreversible changes in electrical properties of as-prepared film occur during the first temperature run. The results of $\rho(T\uparrow)$ and $\rho(T\downarrow)$ measurements for the second and subsequent runs in the same temperature range were identical and quite reproducible. That indicates that irreversible effects are eliminated by the first increase of temperature (short anneal).

Hall effect measurements were conducted on films with a thickness of 800 nm. We were not able to perform these measurements on the films with 50 nm thickness , which is typical for the ZnTe interlayer used in our back contact fabrication, because the sheet resistance of such films is too high for our Hall system. Although electrical properties depend on the film thickness, we hope that some basic trends observed for the thick ZnTe films will also be in effect for the thinner ones.

Table 3.1.1 lists some results of the Hall coefficient measurements conducted at room temperature on the films annealed at different temperatures in the N_2 environment. Cu concentration in the films was measured by WDS. As indicated by this table, hole concentration (n_h) depends on both Cu concentration and annealing temperature. For the lowest [Cu] (~0.5 at.%), the n_h value did not exceed 5×10^{17} cm^{-3} for the whole range of annealing temperatures. For higher [Cu] values, hole concentrations as high as 10^{18}, 10^{19} and even more than 10^{20} cm^{-3} were achieved. An annealing temperature T_{ann} of about 300^0C provided these high hole concentrations. Increasing the temperature of anneal up to 450^0C resulted in a significant decrease in n_h (see samples with [Cu] »7 and 10 at.%).

The maximum hole concentration achieved increases with Cu concentration. Thus, in agreement with literature reports, Cu in ZnTe acts as an acceptor. However, the hole concentration is always lower than [Cu] by an order of magnitude or even more. This suggests that a considerable portion of Cu exists in some electrically inactive state, or donor defects are present in our films in an amount comparable to that of the Cu in acceptor states. Cu acts as an acceptor when occupying the Zn site in the ZnTe lattice (Cu_{Zn}). For the samples with high [Cu] where an excess of cations was observed, one can suggest the existence of Cu_2Te-like electrically inactive configurations. Another possibility is that a

considerable fraction of the excess cations (Zn or Cu) are located in interstitials, where the cations easily lose a valence electron and act as donors that compensate Cu_{Zn} acceptors. Te vacancies are also believed to act as donors. If we accept the idea of a high-degree compensation as a major reason for the low Cu doping activity, it is reasonable to expect that even a relatively small change in compensation degree changes significantly the hole concentration. In turn, annealing at temperatures higher than that of the film deposition leads to changes in the film structure, morphology, residual stresses, defect and complexes amount and arrangement, which should inevitably cause changes in compensation degree and irreversible changes in hole concentration.

Table 3.1.1 Dependencies of film resistivity and carrier concentration of ZnTe on Cu concentration and post-deposition annealing temperature.

Cu Concentr. (at.%)	**Ann. Temp. (0°C)**	**ρ (Ω-cm)**	**Hall Concentr. (cm^{-3})**
0.48	250	3.8×10^{4}	$2\ x10^{13}$
	300	6.4	$2\ x10^{17}$
	350	0.72	$5\ x10^{17}$
	400	1.2	$3\ x10^{17}$
	450	14	$3\ x10^{16}$
2.35	250	3.8	$1\ x10^{19}$
	300	0.32	$7\ x10^{18}$
	350	0.14	$5\ x10^{18}$
	400	0.29	$2\ x10^{18}$
	450	0.55	$8\ x10^{18}$
6.8	300	0.24	$8\ x10^{19}$
	350	0.1	$5\ x10^{19}$
	450	1.8	$2\ x10^{18}$
9.8	250	2.7	$2.2\ x10^{18}$
	300	0.012	$3.8\ x10^{20}$
	350	0.04	$1.5\ x10^{20}$
	400	0.08	$1.3\ x10^{20}$
	450	0.055	$4.9\ x10^{19}$

To clarify the mechanisms that influence electrical charge transport along with free carrier concentration, the temperature dependencies of conductivity were measured and discussed for the films with stabilized properties, i.e., those which were annealed and did not manifest irreversible effects. (The resistivity-temperature behavior is repeatable in the temperature range below the temperature of anneal.) The temperature dependencies of the conductivity for increasing and decreasing temperature scans were conducted with the two-probe method on the films with thickness of 80 nm deposited on soda-lime glass. When interpreting the electrical properties of these films, we will base some of our

conclusions on some results of the Hall effect measurements, although the latter were measured on much thicker films. Plots of ln $\sigma(1/T)$ for all studied films were represented by straight lines. Activation energies for these films derived from the slope of $\ln\sigma(1/T)$ dependencies are presented in Table 3.1.2

Table 3.1.2 Activation energy of dark conductivity of ZnTe films as a function of Cu concentration and post-deposition annealing temperature.

Cu Concentr. (at %)	**Ann. Temp. (^{0}C)**	**Activation Energy (eV)**
1	145	0.45
	235	0.5
	305	0.41
2	140	0.4
	230	0.45
	300	0.3
3	140	0.42
	225	0.32
	305	0.22
4.5	145	0.25
	190	0.21
	310	0.22

The question is what is responsible for the fast conductivity rise with temperature: increase in carrier concentration, mobility, or both. Let us start with hole concentration. No irreversible changes and no hysteresis were observed for the repeated $\sigma(T\uparrow)$ and $\sigma(T\downarrow)$ measurements. That allows us to suppose that no changes in acceptor concentration or in the compensation degree occur. Thus, if the increase in conductivity were due to an increase in hole concentration, the latter would be provided by thermal ionization of some acceptor centers. Based on the Hall effect data (see Table 3.1.1), we can conclude that in our films with higher [Cu] values, after annealing at 300 ^{0}C, the free hole concentration at room temperature should be on the order of 10^{19}-10^{20} cm^{-3}. Now suppose that such a high hole concentration and its exponential growth with temperature with an activation energy E_a is provided by thermal ionization of some acceptor levels. If so, the concentration of the acceptors (N_a) must exceed the hole concentration at least by the Boltzman factor, $\exp(E_a/kT)$. For $n_h = 10^{19}$ cm^{-3}, E_a= 0.3 eV and T = 300 K, that brings us to $N_a > 10^{23}$ cm^{-3}. This number is not only greater than the total concentration of Cu in ZnTe, but also greater than the total number of ZnTe lattice sites per one cubic centimeter, which is unphysical.

Thus we have to conclude that an increase in carrier concentration cannot contribute substantially to the observed increase in conductivity, and the most likely explanation could be an exponential increase in mobility with temperature. Confirmation was obtained from

the resistivity and Hall effect measurements on a film with high Cu concentration, 8 at.%. This film was annealed at 200^0C, and the hole concentration was about 4×10^{18} cm^{-3}. Measured hole concentration did not change in the temperature range of 370-440 K, while mobility changed considerably with an activation energy about 0.2 eV. The observed very sharp mobility rise with temperature cannot be explained by any usual bulk scattering mechanism, such as phonon scattering or impurity ion scattering. The only possible explanation for the exponential increase in conductivity is the so-called "grain boundary scattering". If the grain boundary region dominates the total resistance of the sample (contribution of the grain boundaries exceeds that of material inside the grains), then measured conductivity is proportional to $\exp(-E_b/kT)$, where E_b is an effective potential barrier height. E_b is a real barrier height for the thermionic emission mechanism of barrier transmission. It is lower than the barrier height for the field-thermionic emission (thermally-assisted tunneling), which is probably the case for our heavily doped films. The barrier transmittance usually increases (effective barrier decreases) with an increase in doping level of material inside the grain. This can explain why activation energy, which should be close to the effective barrier height, decreases with the Cu content in the films. Our experimental data are not sufficient to discuss the problem in more detail.

The optical absorption of as-prepared ZnTe films and films after anneal was studied as a function of Cu doping concentration ([Cu]=2, 4, 6 and 8 at.%). The transmission spectrum of the glass substrate was quite smooth at the photon energy range of the absorption edge of ZnTe and used as a correction baseline. It was found that the direct band gap varied from 2.25 eV for [Cu]=2 at.% to 2.30 eV for [Cu]=8 at.% (as-prepared films). After annealing at 270^0C the bandgap increased approximately by 0.03 eV for all [Cu] values. Our optical experiments did not reveal any relationship between direct bandgap and phase. After annealing, high [Cu] films changed phase from hexagonal to cubic, while low [Cu] films were predominantly cubic even before annealing and remained cubic after annealing. However, bandgaps for both high and low [Cu] films increased after annealing by the same amount.

3.2 Fabrication of High Efficiency Devices with ZnTe/Metal Contacts.

(See also [1®, 2®, 7*, 9 *, 11*, 12*])

The studies of ZnTe thin films described in Sec.3.1 helped us to get some knowledge about the properties of thermally co-evaporated ZnTe:Cu thin films and understand better the nature of the processes that occur under the post-deposition treatment. The most important conclusions regarding the back-contact ZnTe interlayer processing were as follows.

1. Using thermal coevaporation with the substrate kept at room temperature and post-deposition anneal, it is possible to obtain ZnTe films with properties that can provide a high quality back contact to the CdTe.
2. Doping activity of Cu in ZnTe in our films is much less than unity, however sufficiently high hole concentrations ($>10^{18}$ cm^{-3}) can be obtained if the Cu concentration in the film exceeds 1 at%.

3. Post-deposition anneal is a necessary step in processing which stabilizes properties of the film, provides high carrier concentration and decreases considerably the film resistivity;
4. To achieve all these results we need only a short (~min) anneal at not too high annealing temperatures. T_{ann} as high as 250^0C and even some lower are sufficient to achieve $n_h > 10^{18}$ cm^{-3} if [Cu]³1 at%. Higher temperatures usually do not provide higher carrier concentrations but even can lead to lower ones.
5. High annealing temperatures, e.g., 400-450^0C cause undesirable changes in the film morphology, namely aggregation, which can make a considerable area of the CdTe surface uncoated with ZnTe and therefore increase the back contact resistance.

These conclusions were made based on the studies of ZnTe films deposited on glass; usually the thickness of these films was greater than that of the back contact interlayer. As we developed the back contact processing with the ZnTe interlayer we were able to check, correct and adjust the conclusions above with respect to much thinner ZnTe films on the CdTe surface. The influence of the CdTe substrate with different preparation procedures and properties on the formation of back contacts was investigated. The effects of the substrate temperature during ZnTe deposition, ZnTe thickness, Cu concentration, and post-deposition treatment conditions were studied and optimized with respect to the photovoltaic performance of CdS/CdTe/ZnTe/Metal cells. Metals with high work function, such as Au, Ni, and Co, were chosen as the candidates for the contacting electrode.

3.2.1 CdTe Substrate and CdTe Surface Etching Effects

The back contact studies were carried out by us on three different types of CdTe samples:

1. CdTe prepared by the CSM laboratory using electrochemical deposition (ED). After annealing with a $CdCl_2$ coating, the CdTe films have grain size of about 1-2 nm. The grains are columnar and normally are rather compact. Under proper preparation conditions, the films can have a very small pinhole density.
2. CdTe samples fabricated by Solar Cell, Inc. (SCI) using a Vapor Transport deposition (VTD) method . VTD CdTe had larger grain size (2-4 nm). However, these films were not as compact as those prepared by ED.
3. For the purpose of comparison and as a part of our CdTe team activities, ZnTe/Metal back contacts were applied to samples provided by Golden Photon, Inc. (GPI) prepared by spray pyrolysis.
4.

For different CdTe samples, it was found necessary to use different CdTe etching and back contact preparation conditions in order to achieve high efficiency and high stability solar cells.

In order to examine the etching effects on device quality, cells fabricated with and without an etching procedure were prepared and compared. To prepare etched cells, the

etching conditions used were: 0.015 vol.% Br_2-methanol solution, 25 second etching followed by a 2 minute rinse in methanol. For unetched cells, a two minute rinse in methanol was used. The performance of the two sets of cells is shown in Table 3.2.1. Both sets of cells show large shunt resistance. The fact that the shunt resistance of unetched cells is lower and the short circuit current density is higher than those of etched cells could be partially due to the smaller area of unetched cells. It is known that edge collection of current is more significant in cells of small size. We can also see that the etching procedure improved the fill factors. Figure 3.2.1 demonstrates the dynamic resistance (R=dV/dJ) vs bias (V) . For unetched cells there could be seen a significant increase and peak in R(V) dependence at V> 0.6-0.7 V. This is an evidence of a Schottky diode dominating resistance of the back contact. (see Section 4.4). For etched cells, manifestations of the back contact Schottky diode are much weaker and the increase in resistance near V_{oc} is one order of magnitude smaller than for the unetched cells. Thus one can conclude that the etching procedure is essential for reducing the contact resistance.

Table 3.2.1 Performance of the ED CdTe cells with and without CdTe surface etching. Values are the average over more than 4 cells. All measurements were made at CSM.

Etch condition	**Area (cm^2)**	**η (%)**	**V_{OC} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**R_s (Ω-cm)**
unetched	0.08	13.3	819	22.5	72.2	840
etched	0.2	13.4	831	21.3	75.4	2415

For porous CdTe or CdTe with large pinholes, the Br_2-methanol etching can create extra shunting paths along the CdTe grain boundaries. It was found in our study that by varying the Br_2 concentration in methanol as well as the etching time, the shunting effect could be significantly limited for the CSM and SCI samples. However the shunting effect could not be avoided for the porous GPI samples using the Br_2-methanol etching. High Br_2 concentration in methanol would lower the shunt resistance dramatically for CdTe samples from SCI, while it did not show much effect on CdTe samples prepared by CSM, which were more compact. It may be suggested that shunting comes from preferred etching along grain boundaries. There was a report [26] that Br_2 penetrated down the grain boundaries even to the TCO layer.

It is known that the excess Te in CdTe provides p-type conductivity. One can suppose that the etching procedure, which creates a Te-rich layer [27], increases the doping density in the CdTe region close to the CdTe/ZnTe interface which leads to the decrease in the back contact Schottky barrier. Indeed, Dark (C-V) profiles measured on cells from Table 3.2.1. detected a higher CdTe doping level close to the ZnTe interface for the etched cells than for unetched ones. That could be considered as evidence that the etching procedure created a Te-rich region at the surface of the CdTe. However we cannot exclude another possible reason for the increase of the CdTe doping level in etched cells. Namely, it

is an increased concentration of Cd vacancies at the interface region and therefore enhanced occupation of Cd sites by Cu diffused from the ZnTe [28]. The higher V_{oc} in etched cells may also be a result of the higher doping in CdTe due to the etching procedure, since higher doping increases the built-in voltage of the junction.

3.2.2 Deposition and Post-Deposition Treatment of ZnTe:Cu Layer

The typical deposition rates of the ZnTe we used for the ZnTe layer fabrication were the same as for the ZnTe/glass samples, i.e.,5-10 Å/s. The deposition rate of the Cu was adjusted to a value between 0 and 0.2 Å/s to obtain the Cu atomic concentration in the ZnTe up to 10%. An optimal ZnTe thickness of about 50 nm was established which provides both high efficiency and high stability of the cells. Experiments showed that the ZnTe:Cu deposition on substrates kept at low temperature yielded the highest performances. Indirect heating caused by the thermal radiation from evaporation sources led to significant fluctuations in the performance of the resulting cells. By careful arrangement of the configuration of the deposition system and adding insulators to the sample supporter, radiation heat was reduced and the substrate temperature was kept close to room temperature. The quality of the back contact was improved and also became more reproducible.

Based on the ZnTe:Cu thin film studies (see Sec. 3.1) we have varied the temperature of post-deposition treatment of the ZnTe interlayer in a range 200-350 ^{0}C to provide high hole concentration and low resistivity in the interlayer. After performing a series of annealing experiments, the optimized annealing conditions for different Cu concentrations were found. For example, 270^{0}C was found to be an the optimal annealing temperature for [Cu]= 2 at.% (see Table 3.2.2).

Table 3.2.2. Effect of ZnTe annealing temperature on cell performance. SCI CdTe/CdS samples were used. The ZnTe:Cu film parameters: [Cu]=2 at.%, thickness ~50 nm, the cell area = 0.1 cm^2. Values are averaged over the 5 best cells for each set.

Anneal Temp. (^{0}C)	**η (%)**	**V_{OC} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**$R_s=(dV/dJ)_{V_{oc}}$ (Ω-cm)**
200	1.8	532	9.4	36	20.1
270	13.3	796	23.9	70	4.5
280	12.1	763	23.2	68	4.75
350	7.08	678	20.7	50	18.8

Annealing temperatures in a range 240-270^{0}C were found to be optimal for cells with Cu concentrations in the ZnTe up to 6 at%. Our study of post-deposition treatment of ZnTe:Cu/glass samples indicated a strong dependence of the film resistivity and hole concentration on the annealing temperature. As to the length of anneal, it was found that steady state is achieved (and all the irreversible changes are eliminated) in a short time, on the order of a minute. This conclusion was confirmed also with respect to cell performance using a back-contact ZnTe interlayer. It was found that a total time of 2 min. during the sample is held at T>200^{0}C is sufficient to provide high cell performance, while longer anneal (say, tens of minutes) leads to performance degradation. A typical temperature - time profile we use for the ZnTe/CdTe post-deposition anneal is presented in Fig. 3.2.1.

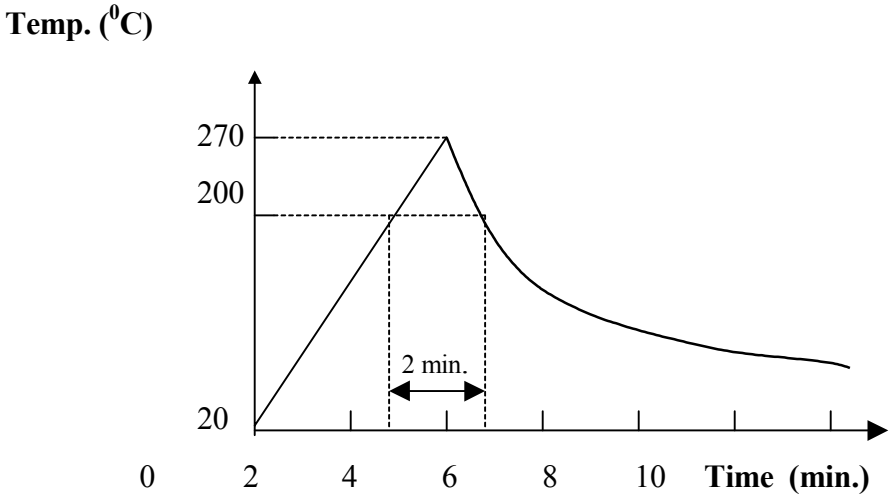

Fig. 3.2.1 Typical Temperature - Time profile for ZnTe postdeposition heat-treatment

3.2.3 Effect of Different Contact Metals

Metals with high work functions were tested as contacts: Au, Ni and Co. Au films were deposited by vacuum thermal evaporation, while Ni and Co were deposited by e-beam evaporation. ED CdTe prepared by CSM (Table 3.2.3) and VTD CdTe prepared by SCI (Table 3.2.4) were used for these studies.

Table 3.2.3 Comparison of cells with different metal electrodes. CSM CdTe material. Interlayer parameters: ZnTe thickness ~60 nm, [Cu]=6 at.%. Cell size is 0.08 cm^2. Values are averaged over 5 cells for each group.

Metal	**η (%)**	**V_{OC} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**$(R)_{V=Voc}$ (Ω-cm^2)**	**R_{sh} (Ω-cm^2)**
Au	12.0	763	22.7	69.3	5.2	1191
Co	11.7	734	23.9	66.9	4.9	574
Ni	12.7	733	26.0	66.6	5.3	530

Table 3.2.4. Performance of Au- and Ni- contacted cells made on SCI material. Cell area = 0.2 cm^2, ZnTe thickness~50 nm, [Cu]~4 at.%.

Metal	**η (%)**	**V_{OC} (mV)**	**J_{sc} (mA/cm^2)**	**FF (%)**	**$(R)_{V=Voc}$ (Ω-cm^2)**	**R_{sh} (Ω-cm^2)**
Au	13.0	821	21.2	75.0	4.2	1335
Ni	12.3	800	21.4	72.2	4.6	1586

It is seen from the tables that for all the metallizations used the series resistance (defined as dV/dJ at $V=V_{oc}$) is almost the same and low enough. The efficiencies of the cells do not depend significantly on the type of metallization. The fill factors and open circuit voltages of Au-contacted cells are somewhat higher than those of Ni- and Co-contacted cells. It may be supposed that the higher J_{sc} values for the CSM material, especially for the Ni-contacted cells, were due to the higher edge collection for small area cells. Saturation current and diode quality factors for Au- and Ni-contacted cells were deduced from the dark J-V curves. They had exactly the same values for both kinds of cells: A=1.55 and $J_0=1.0\times10^{-11}$ A/cm^2. Thus no difference takes place in the number of defects that influence recombination processes and transport mechanisms through the junction. Thus, based on the data for as-prepared cells it is difficult to decide what type of metallization (Au or Ni) is preferable.

The dynamic resistance R=dV/dJ was analyzed in a wide range of forward biases for Au- and Ni-contacted cells. No manifestation of the back-contact Schottky diode was found, such as increase in the R magnitude with increasing V or peak in R(V) dependence. At the same time, the R value at high forward bias, where R(V) is close to saturation, which represents a real contact resistance, is considerably lower for Au-contacted cells than for the Ni-contacted, both in dark and light. For the Au-contacted cells this value in light was usually within the range of 0.1-0.3 Ω-cm^2, while for the Ni-contacted it was in the range of 0.5-1.0 Ω-cm^2.

3.3 Improvement of Cell Performance by ZnTe/Metal Back Contact.

Based on the studies presented above in Sec. 3, the following conclusions can be formulated:

- Application of a thin ZnTe:Cu back-contact interlayer deposited by thermal evaporation and properly annealed, improves cell performance due to considerable decrease in series resistance. Indeed, back contact specific resistance at a high forward bias, R_c, lower than 0.1 Ω-cm^2 was obtained for Au/ZnTe/CdTe/CdS solar cells as compared to $R_c \geq 2$ Ω-cm^2 for Au/CdTe/CdS cells.

- The work function value of the contacting metal (Au, Ni or Co) does not influence considerably the series resistance value (defined as dV/dJ at $V=V_{oc}$) as long as a high hole concentration in ZnTe is provided by doping with Cu and post-deposition heat treatment. The choice of metal may have a small effect on the V_{oc} values obtained in the completed cells.

- Based on the comparative studies of as-prepared cells it is difficult to decide what kind of metallization among studied is preferable. A more conclusive decision should be made based on studies of cell degradation under various stress conditions.

Light J-V dependence (measured at NREL) of a CdS/CdTe/ZnTe/Au cell with area of 0.1 cm^2 is shown in Fig. 3.3.1. Cell efficiency is 12.9%; the Fill Factor is 74%.

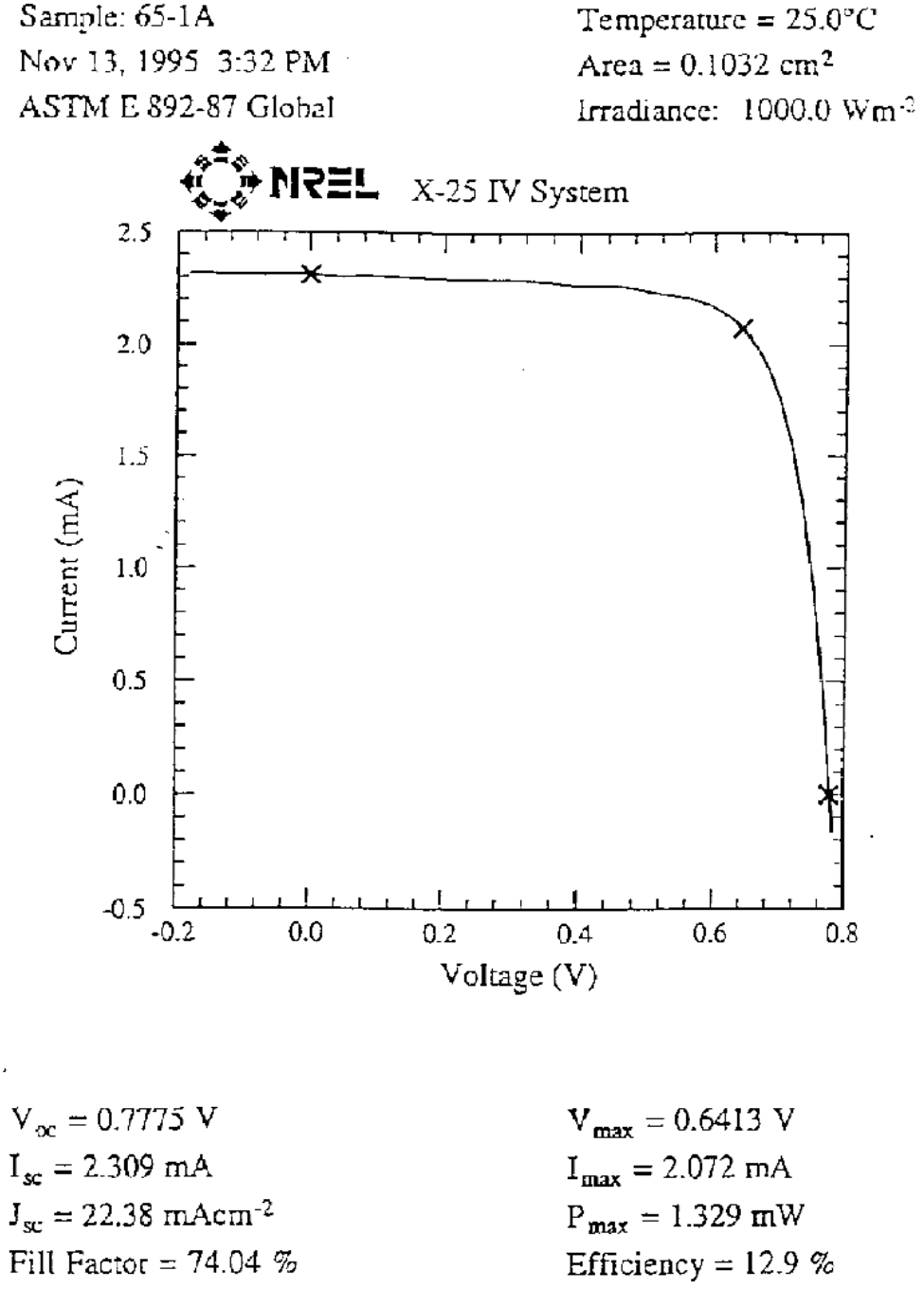

Fig. 3.3.1 Light J-V curve (measured at NREL) of a CdS/CdTe/ZnTe/Au cell showing 12.9% efficiency

4. CELL DEGRADATION UNDER STRESS CONDITIONS (III)

(See also [3®, 4®, 6®,12*]

The studies presented in this section were aimed at revealing and identifying the degradation processes occurring in the cells with ZnTe/Metal back contacts. The objectives were as follows:

(i) To separate the degradation processes taking place in the back contact region from those occurring in other parts of the cell.
(ii) To study and explain changes in electrical properties of the back contact, in particular, degradation of the back-contact Schottky diode.
(iii) To study compositional changes in the back-contact multilayer structure and their possible influence on degradation processes.
(iv) To reveal and analyze changes in the main diode region caused by the presence of the ZnTe:Cu/Metal back contact.
(v) To clarify the role of the Cu dopant in ZnTe in degradation processes.
(vi) To compare degradation processes in cells with different metallizations and explain the difference if there is any.

To achieve these objectives we tried to combine experimental studies with some new approaches to the interpreting the results, including analyses of the dynamic resistance of the cell in a wide bias range and analyses of the possible influence of impurity/defect electromigration. We also tried to estimate the possibilities for selective acceleration of different degradation processes (in different parts of the cell) which may be helpful in the development and optimization of an accelerated test procedure for the prediction of cell lifetime.

4.1 Cell Degradation under Enhanced Temperature. Experiment.

Cells for these studies were fabricated on the base of CdTe/CdS structures supplied by SCI. ZnTe:Cu/Au back contacts were applied using our routine processing procedure. There were two sets of cells with different Cu concentrations in ZnTe: [Cu]=2 at.% and 5 at.%. A ZnTe thickness of 50 nm was used for both sets of cells. Stability tests were conducted in a vacuum oven at temperatures of 140^0C (for 165 hours) and 110^0C (for 683 hours). Both sets of devices had initial efficiency of about 12%. The efficiency (η), fill factor (FF), and series resistance (R_s) changes over testing time are presented in Figures 4.1.1, 4.1.2, and 4.1.3, respectively.

The degradation rate at 140^0C was unexpectedly considerably higher for the cells with [Cu]=2 at% as compared to those with [Cu]=5 at.%. However, the difference in degradation rates for the two [Cu] values was much smaller at 110^0C. The major part of the degradation occurred in the first 100 hours. Then the rate of degradation decreased considerably. Even some recovery in efficiency can be seen in Fig. 4.1.1 after 300 hours of stressing for [Cu] = 5% and after 550 hours for [Cu] = 2%. V_{oc} and J_{sc} decreased, but these changes were not significant for both sets of cells.

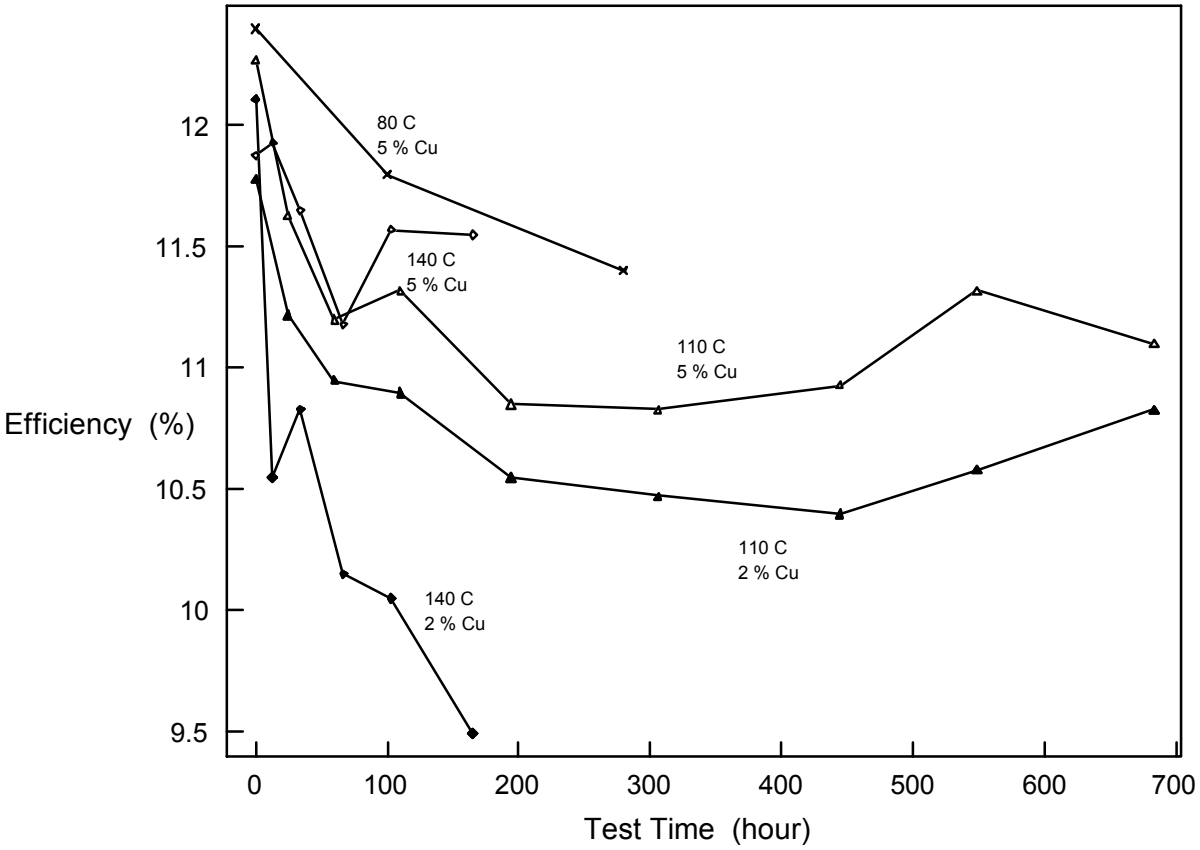

Fig. 4.1.1 Cell efficiency as a function of stress testing time. The testing temperature and Cu concentration in ZnTe are indicated at each curve. All the data are averaged for not less than 6 cells. Cell area is 0.08 cm^2.

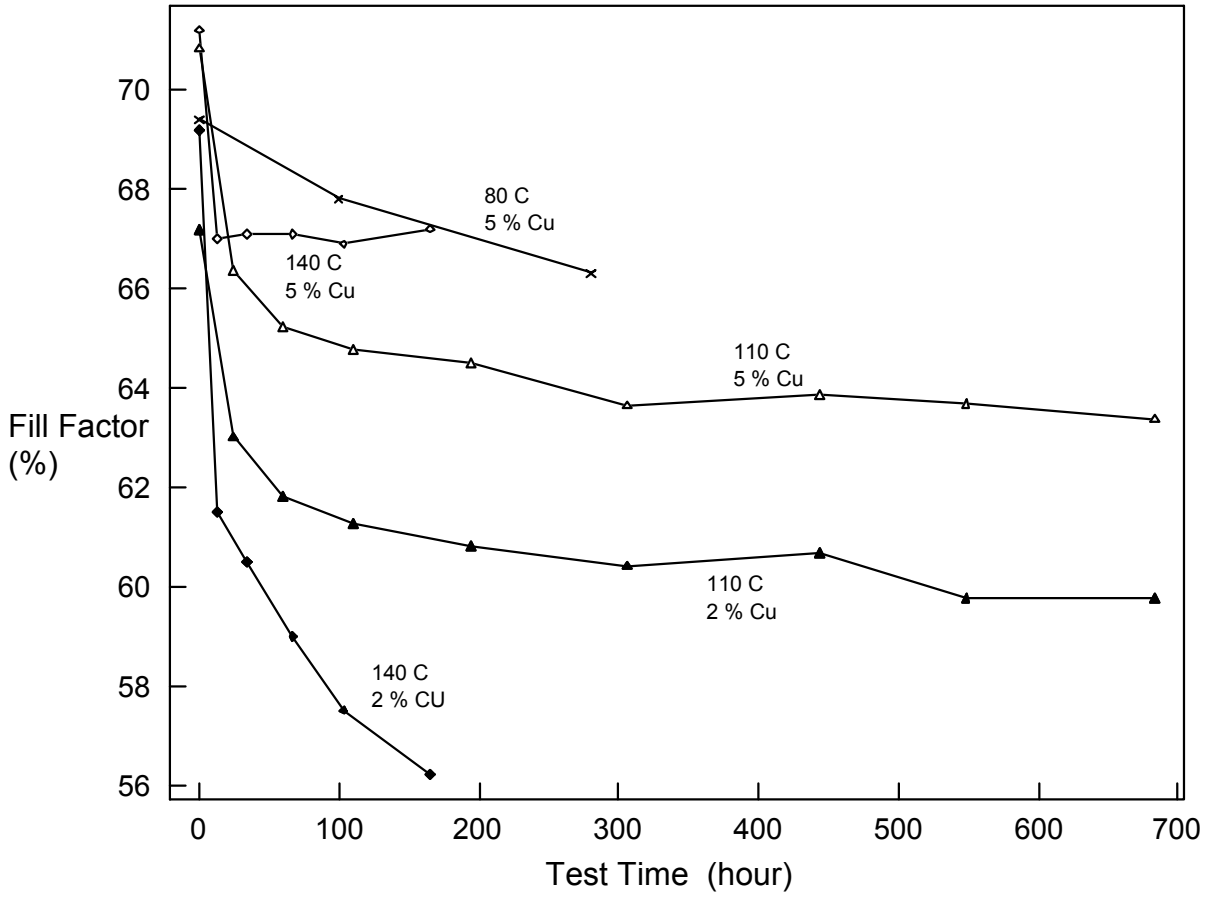

Fig. 4.1.2 Fill factor as a function of stress testing time. The same cells and tests as in Fig. 4.1.1.

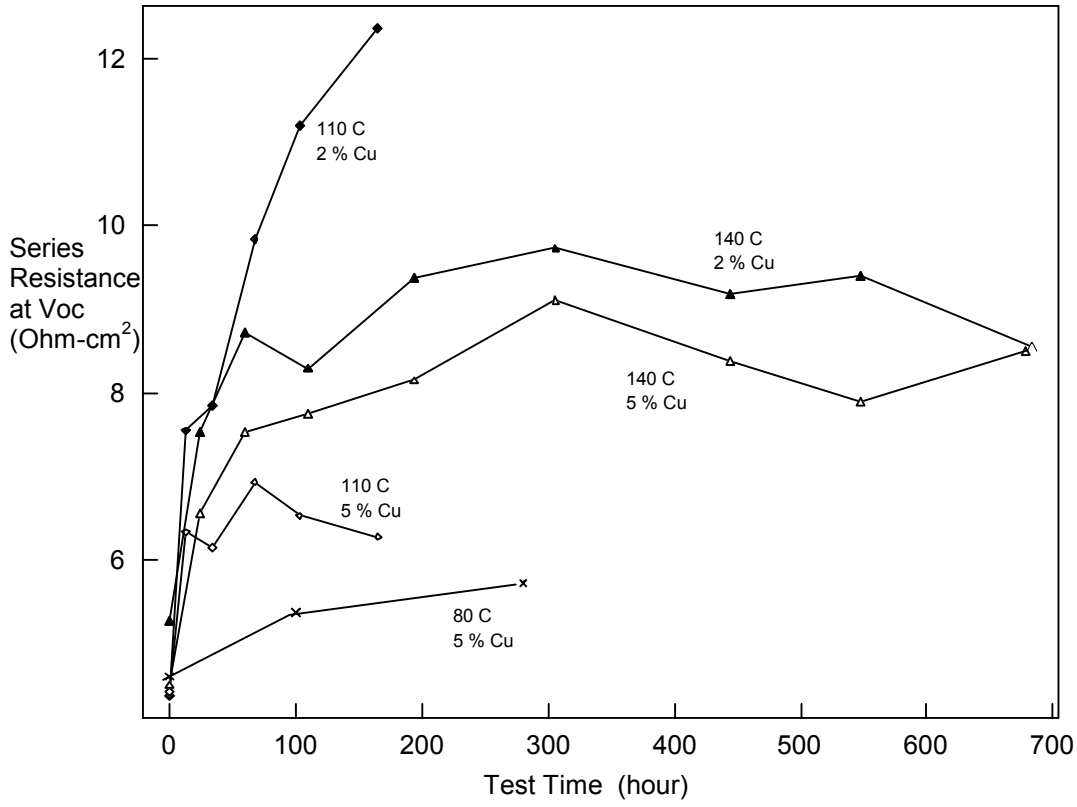

Fig. 4.1.3 Series resistance as a function of stress testing time.
Series resistance is defined as dV/dJ at $V=V_{oc}$.
The same cells and tests as in Fig. 4.1.1.

The most significant change was the increase in series resistance. Besides Fig. 4.1.3, this can be seen in Fig. 4.1.4 where J-V dependencies measured in dark are presented for as-prepared and degraded cells. A great change in the slope of the graph at high forward bias for the degraded cells indicates considerable increase in series resistance. Some specific features of the J-V dependencies can be seen better from Fig. 4.1.5 where the dynamic resistance, R= dV/dJ, as a function of bias is shown. A low magnitude of R indicates a high quality semi-ohmic back contact in the as-prepared cell. All other curves demonstrate well pronounced minima and maxima in the R(V) dependencies. The R magnitude in the high voltage range is highest for the cell with [Cu]=2at% after stress temperature testing for 683 h. It is higher than that for the cell with [Cu]=5 at.% subjected to the same stress test. The cell exposed to the air at room temperature for 6 months demonstrates an R magnitude intermediate between these two cells and the as-prepared one. But the peculiarities mentioned above (minimum and maximum in R(V) dependence) are manifested clearly. The same features can be seen in all the degraded cells.

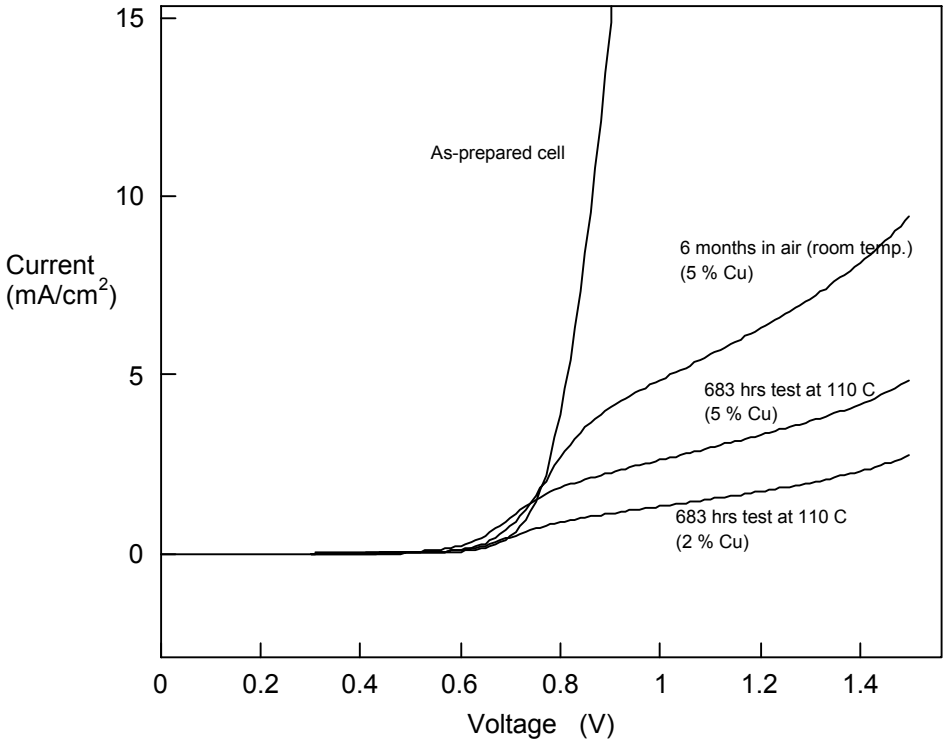

Fig. 4.1.4 Dark J-V curve for as-prepared and degraded cells. Degradation conditions and Cu concentration in the ZnTe for each cell are indicated in the graph.

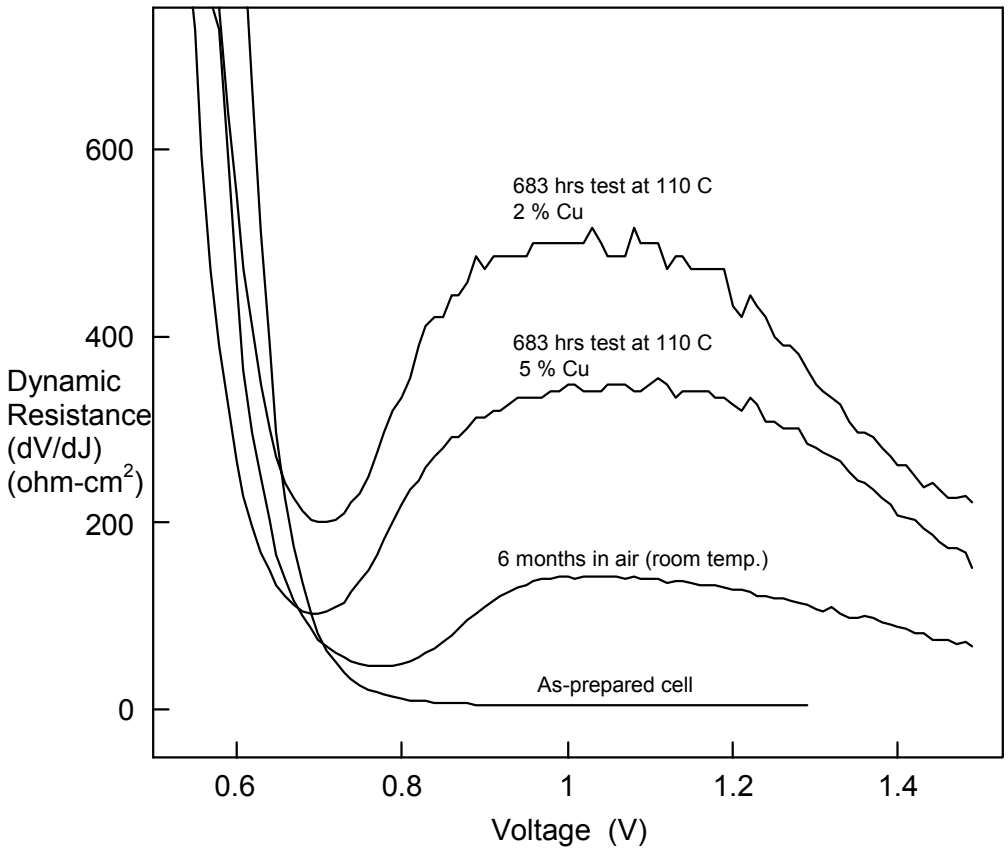

Fig. 4.1.5 Dynamic resistance (dV/dJ) as a function of voltage applied derived from the data in Fig. 4.1.4. dV/dJ(V) dependencies for all the degraded cells demonstrate well pronounced minima and maxima.

The initial drop in resistance with the forward bias increase is quite understandable: it is determined by the behavior of the main diode (CdS/CdTe p-n hetero-junction) under forward bias increase, namely by the exponential dependence of current on voltage. The subsequent increase in R can be attributed to the presence of a Schottky diode at the CdTe/ZnTe interface. The reverse bias applied to this diode increases with an increase in forward current through the cell which leads to the R increase. Theoretical analysis and modeling of J-V curves for a Schottky diode showed that at a sufficiently high reverse bias its resistance may drop with applied voltage. The sharpness of the maximum and its position on the V scale depends on the dominant mechanism of carrier transport (thermionic emission, tunneling, etc.). For the degraded cells the behavior described above becomes more pronounced which means degradation of the Schottky diode properties. The influence of the back-contact Schottky diode on the R(V) characteristics of a cell will be discussed in more detail in Sec.4.2.

Changes in doping level in the CdTe were also studied using C-V profiles (Figs. 4.1.6 and 4.1.7). The changes after the stressing are considerable over the entire voltage/depth range, achieving an order of magnitude and even more at depths of 2.5-3.5μm. We do not think that these curves can supply us with exact information on the space charge density especially in the region close to the CdTe/ZnTe interface. But it is likely that at least the trend of changes in doping level resulting from stress temperature tests could be derived from these data. Definite correlations were found between changes in efficiency and R_{se} on one hand and the doping level in the CdTe layer on the other (see Fig.4.1.8). Because of the increasing errors as the applied voltage increases, the doping level data presented in the figure correspond to V=0, i.e., to the edge of the depletion layer in the CdTe. It is seen that an increase in R_{se} is always followed by a doping level decrease. Moreover, after a few hundred hours temperature stress test, a slight decrease in R_{se} took place, and some recovery of the doping level was also observed. We were not able to determine the doping level close to the CdTe/ZnTe interface, but it is likely that it changes in the same direction over the entire CdTe layer. A decrease in doping level in the CdTe adjacent to the interface (which should lead to an increase in the height and width of the Schottky barrier) can be considered as a possible reason for the increase in Schottky diode resistance.

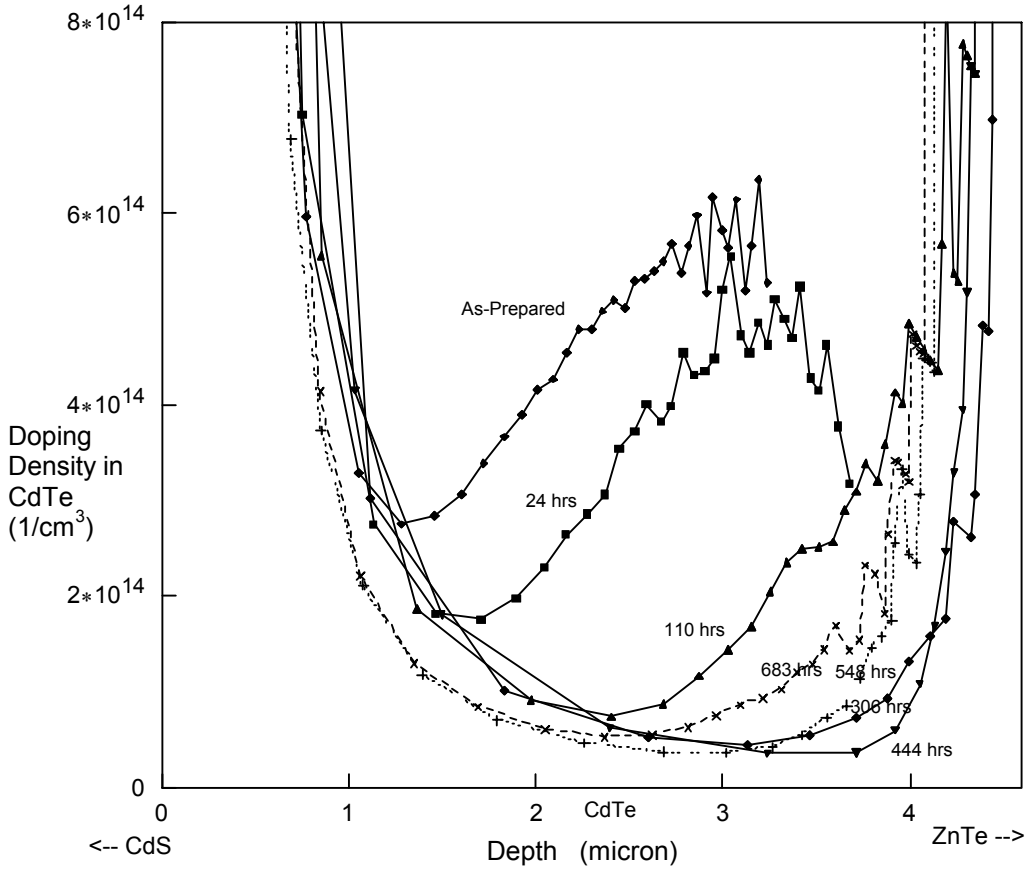

Fig. 4.1.6. Distribution of CdTe doping density derived from dark C-V profiles. Cu concentration in ZnTe is 2 at.%.

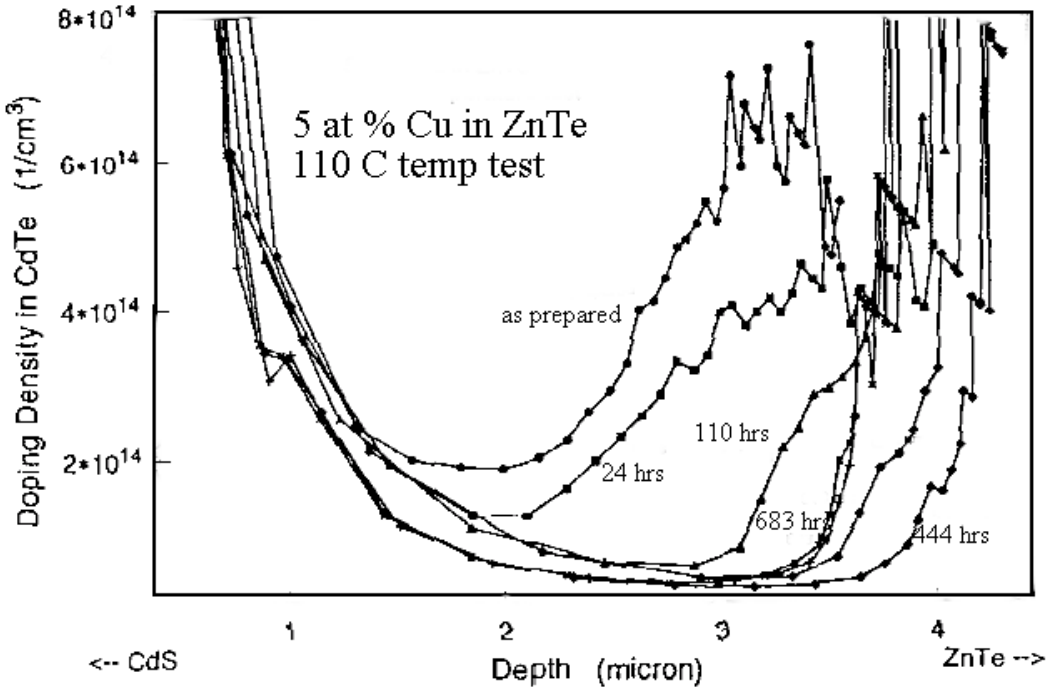

Fig. 4.1.7 Distribution of CdTe doping density derived from dark C-V profiles. Cu concentration in ZnTe is 5 at.%.

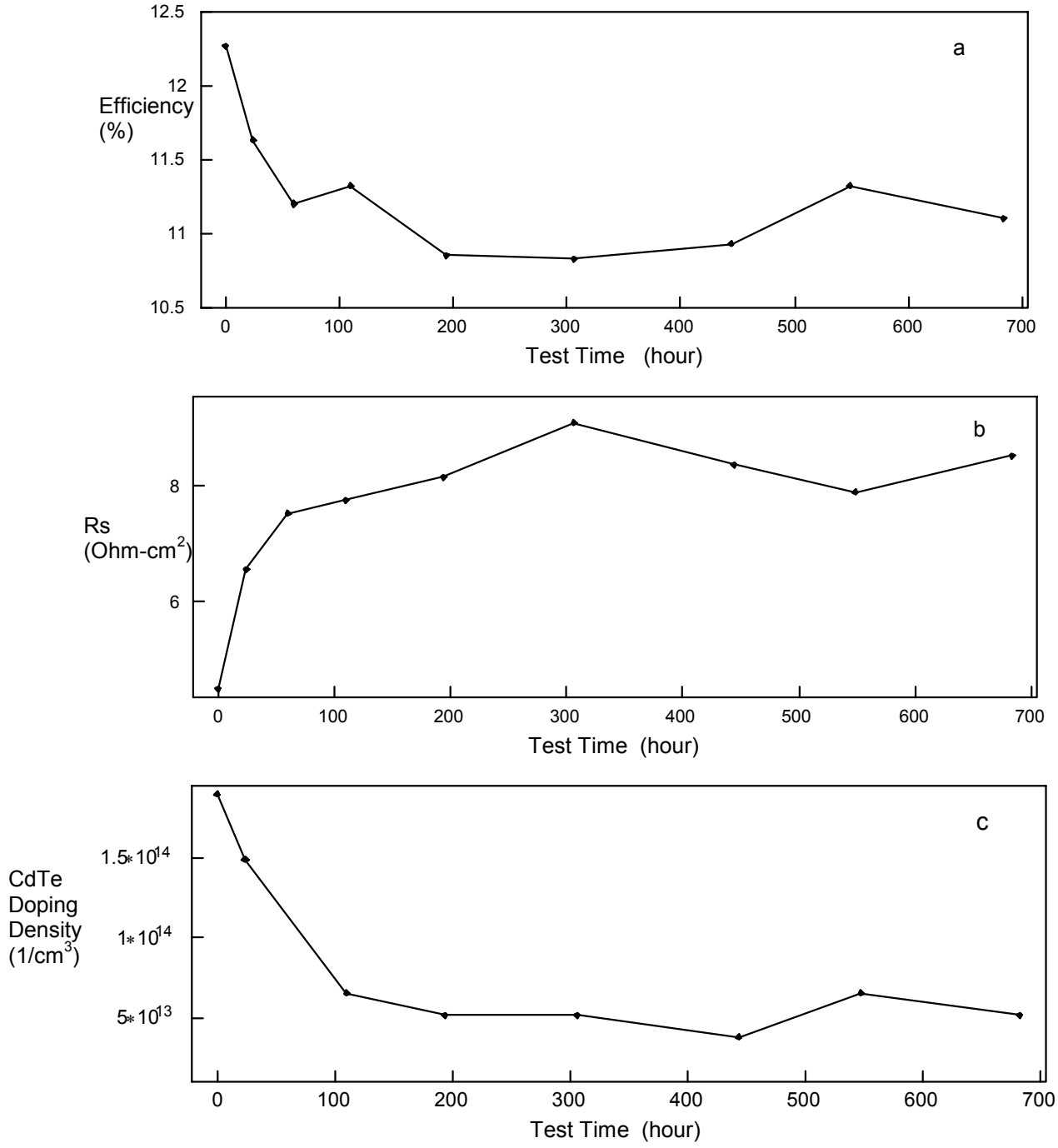

Fig. 4.1.8 Efficiency (a), resistance (b), and CdTe doping density (c) of CdS/CdTe/ZnTe/Au cells upon temperature stress testing at 110 ^{0}C. Cu concentration in ZnTe is 5 at.%.

4.2 Influence of Cu on Degradation Process

To understand better the role of Cu in cell degradation, cells with three different types of back contact were prepared: ZnTe/Au, ZnTe:Cu/Au, and Cu/Au - and tested before and after 20 hours annealing at 110^0C. The results of these studies were as follows (see Figs. 4.2.1 and 4.2.2.):

(1) As-prepared cells with Cu involved had a very small series resistance and practically the same doping level-depth profile with a maximum value $3x10^{15}$ cm^{-3}. The as-prepared cell with the ZnTe/Au contact, without Cu, had series resistance an order of magnitude higher and also the well pronounced Schottky diode behavior discussed above . The doping level for this cell was about 10^{13} cm^{-3}.

(2). After annealing, the cell with the ZnTe:Cu/Au contact demonstrated a significant increase in R_s, especially in the dark, a well pronounced Schottky diode behavior, and a decrease in doping level to $2\text{-}5x10^{14}$ cm^{-3}. In the case of the ZnTe/Au, the doping level did not change and the dark resistance increased less than 30%. For the Cu/Au sample, the doping level decreased by a factor of 3, and the resistance even decreased.

From these measurements, we conclude that the Cu dopant plays a significant role not only in cell initial performance but also in the degradation process. The atomic-scale mechanism of the Cu influence is not well understood yet. One might suggest (as was done in our last annual report for NREL) that an additional Cu amount diffuses into the CdTe from the back contact during the long-term stability test. However there are some reasons for this suggestion to be doubtful:

(1) Cu diffusivity in CdTe is very high, even at room temperature. According to [29] the diffusion coefficient of Cu, D_{Cu}, in single crystal CdTe at T=300 K is about $3x10^{-12}$ cm^2/s. That means that the diffusion length $L_D=(D_{Cu}\cdot t)^{1/2}=5$ μm for the diffusion duration t=24 h. For t=500 h $L_D=23$ μm. The diffusion coefficient for 110^0C should be significantly higher, suggesting that the Cu concentration gradient in the CdTe adjacent to the ZnTe becomes small in a short time and no considerable additional diffusion of Cu into CdTe can take place in the following tens and hundreds of hours. Thus it is hard to expect a change in Cu concentration in the vicinity of the CdTe/ZnTe interface which can influence considerably the Schottky barrier properties.

(2) The Cu dopant is known as an acceptor providing p-type conductivity in CdTe. It should be expected that an increase in Cu concentration will increase the doping level whereas in our experiments annealing resulted in a considerable lowering of the doping level.

(3) The doping level in CdTe:Cu is much smaller than the Cu concentration not only in our experiments. For example, studies of Cu diffusion from a Cu/Au back contact [30] showed that Cu concentration in CdTe can be as high as 10^{18} cm^{-3} while the doping level determined from the C-V profile is in the range of 10^{15} to 10^{16} cm^{-3}.

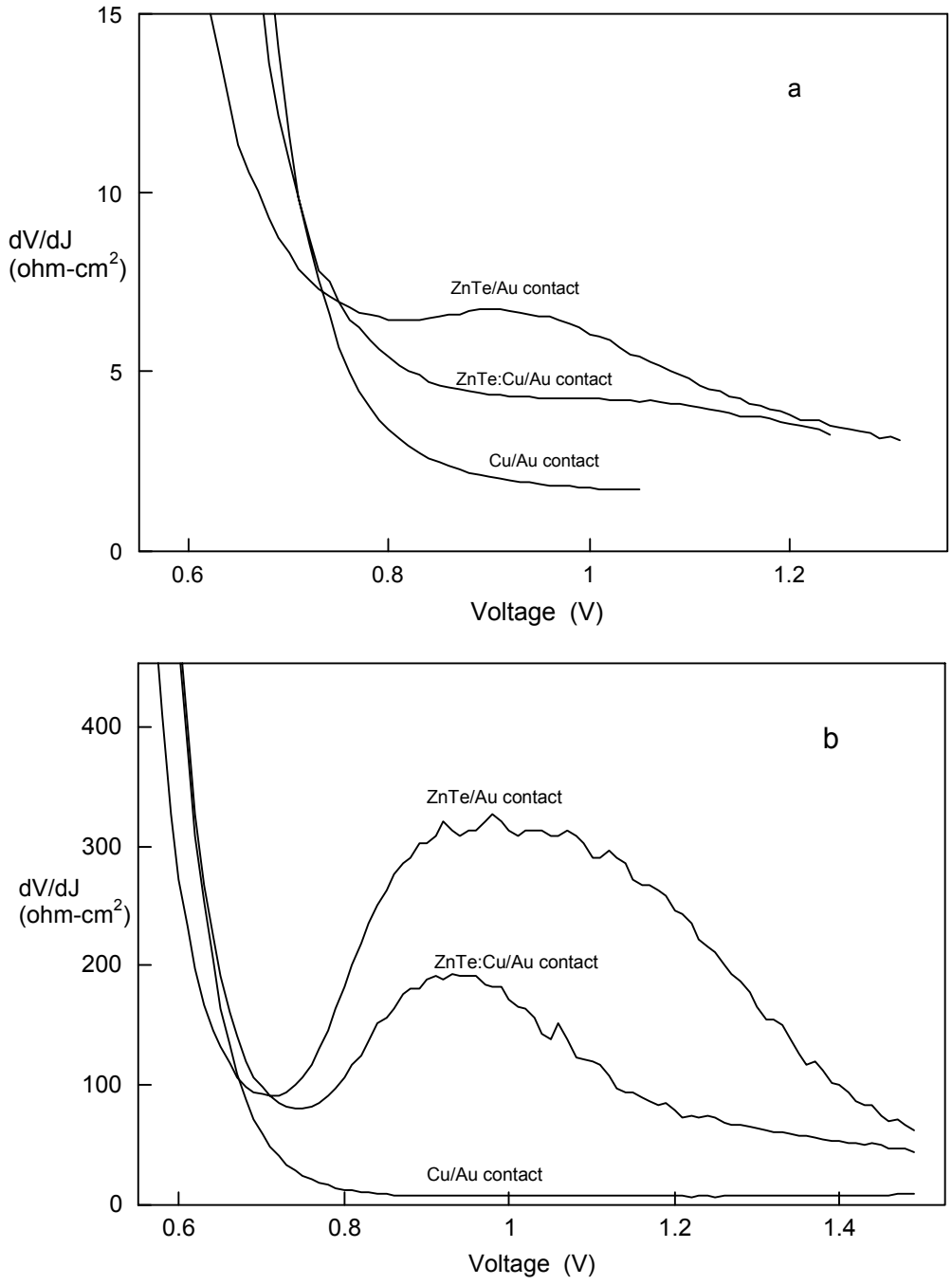

Fig. 4.2.1. Dynamic resistance of cells with different back contacts. (a) as-prepared cells, (b) cells after 20 hours temperature test at 110 ^{0}C.

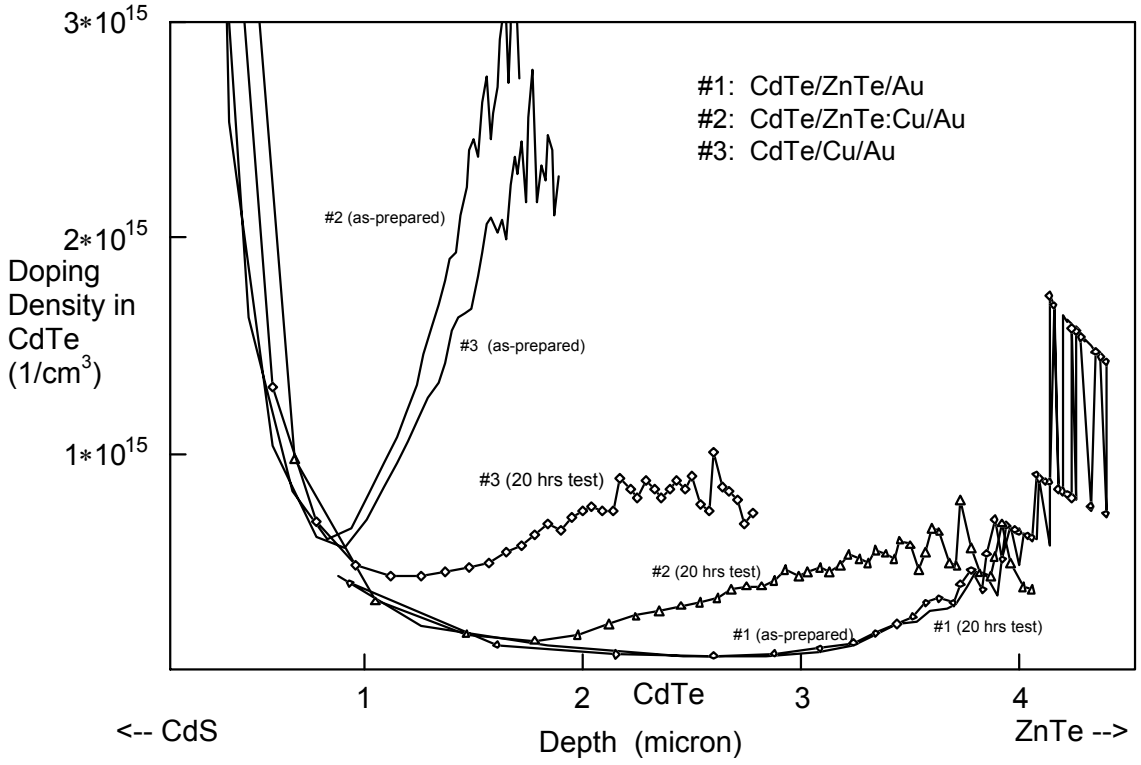

Fig. 4.2.2 Distribution of CdTe doping density derived from the dark C-V measurements for the differently contacted cells. Solid lines represent the as-prepared cells, and dots represent the cells after 20 hours test at temperature 110 ^{0}C.

All the facts above lead to the conclusion that we must look for degradation mechanisms other than Cu-doping of the CdTe. The one which seems the most probable is based on the concept of compensation of acceptors induced by Cu. Cu introduced into CdTe can produce a few types of defects. Among them are a shallow donor, Cu_i^+, and a deep acceptor, Cu_{Cd}^-,[7-9]. Besides this, there is an evidence that copper forms complexes such as $[Cu_iCu_{Cd}]$ and $[Cu_iV_{Cd}]$ [10]. The latter is believed to act as an acceptor. Among these species only Cu_i^+ is thought to be mobile at room temperature and responsible for the high diffusivity of Cu. If so, it should be suggested that a considerable portion of the Cu should exist in CdTe in the interstitial form and that the compensation of Cu-induced acceptors can come from these interstitial Cu ions that act as donors. This is not the only possibility. Cu acceptors can also be compensated by donor- type native defects such as Cd_i or V_{Te}. It is well known that the self-compensation phenomenon is pronounced in II-VI semiconductors such as CdTe. Thus we have grounds to propose a high degree of compensation in CdTe. This means that the hole concentration as well as the space charge density in the depletion region (derived from the C-V profile) is much smaller (maybe orders of magnitude) than the total density of charged impurities and

defects. If so, even a minor change in the degree of compensation caused by the enhanced temperature in our stability tests can provide a considerable change in the measured doping level as well as in hole concentration. The latter, if it occurs in the vicinity of the ZnTe/CdTe interface, can lead to the observed changes in the Schottky diode resistance.

4.3. Compositional Changes in the Back Contact

CdTe/ZnTe:Cu/Au cells were studied using AES and XPS after annealing at 140^0C for 165 hours. Auger element maps (Fig. 4.3.1) showed some small islands (~1 μm) on the Au surface containing considerable amounts of Te. XPS depth profiles indicated considerable Cu diffusion from the ZnTe to the Au layer. The Cu concentration in Au was about 4 at.% in the cells made with 5 at.% Cu in the ZnTe. The same tests of Ni-contacted cells revealed no detectable diffusion of Te and Cu into the Ni metallization.

In order to reduce the influence of the roughness, primarily due to the CdTe, metal/ZnTe:Cu structures were grown on the smooth surface of a polished Si wafer. To intensify diffusion and chemical reactions the samples were annealed at the elevated temperature of 230^0C for 2 hours in vacuum. As before, considerable amounts of Te (see Fig. 4.3.2) and Cu were detected in the Au layer, which confirmed the results on real cells. Cu content in the Au layer was comparable to that in the ZnTe. In addition, dots containing over 15 at.% Au were found on the top surface of the ZnTe. No traces of interdiffusion were detected in ZnTe:Cu/Ni structures.

Based on the evidence that significant compositional changes caused by interdiffusion or, perhaps, reactive diffusion, occur in Au-contacted cells while no phenomena of this kind were detected in Ni-contacted cells, one might suppose that Ni-contacted cells should be more stable and exhibit slower degradation. Indeed, in Ni-contacted cells R_{se} increased slower and the decrease of doping level was considerably smaller than in the Au-contacted cells with the same Cu concentration in the ZnTe (5 at%). However, the efficiency of the Ni contacted cells degraded faster, which was mostly due to the faster decrease in shunt resistance. Low shunt resistance was also observed for our Au-contacted cells with high Cu concentration in the ZnTe (as well as for cells with a Cu/Au back contact with a thick Cu layer [5]). Excessive Cu may diffuse to the CdTe/CdS interface and form additional shunt paths. Based on the above results, we can propose that the amount of Cu that is able to diffuse into CdTe during the long-term tests is limited by the consumption of a considerable portion of Cu by the Au layer. This effect does not take place in Ni-contacted cells. This could be one of the possible explanations of the different stability of Au- and Ni-contacted cells.

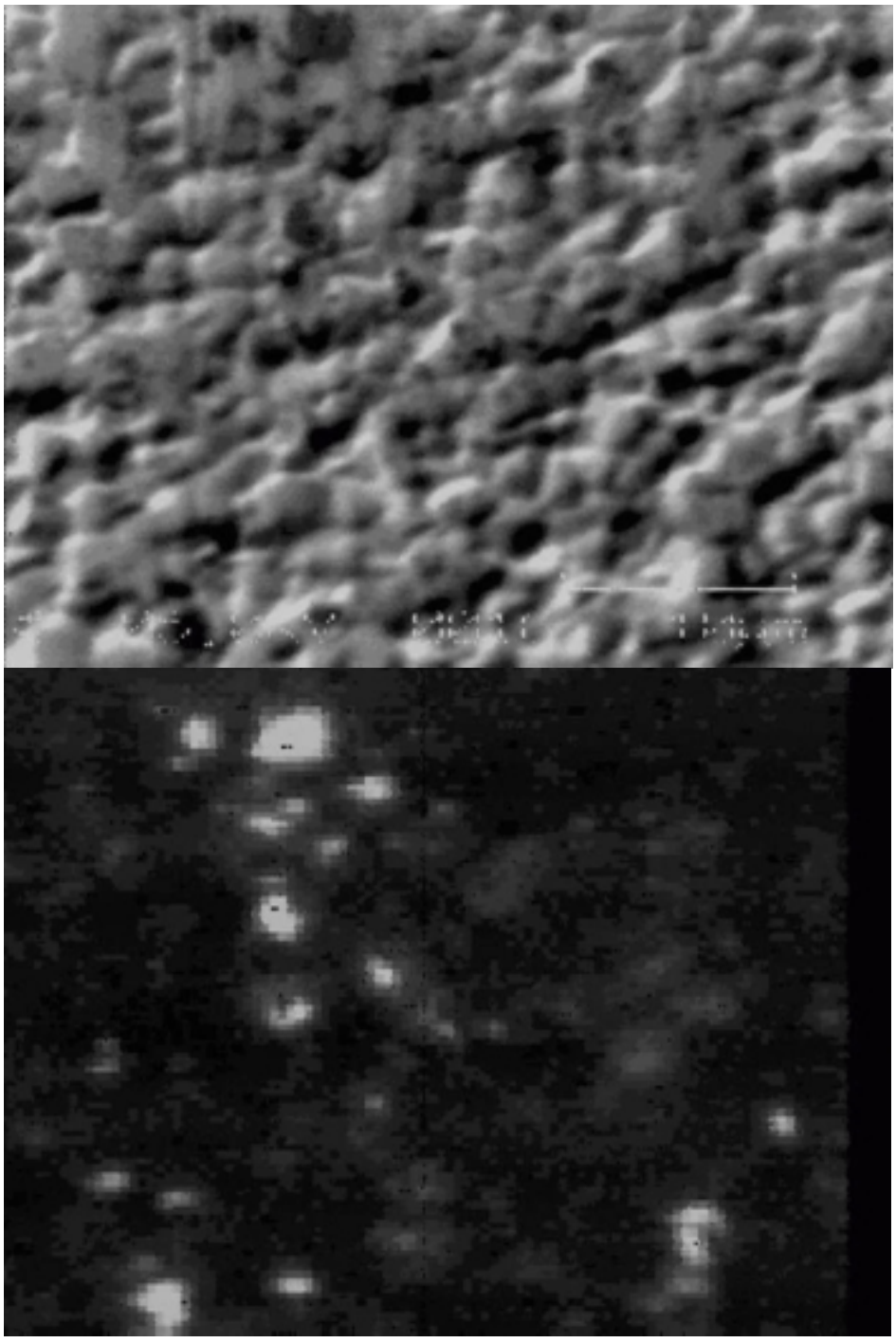

Fig. 4.3.1. (a) SEM image of Au surface of CdTe/ZnTe/Au cell after 165 hours testing at 140^0C.
(b) AES Te element map of the same area as (a). Te out-diffusion into the Au layer took place after temperature stress testing.

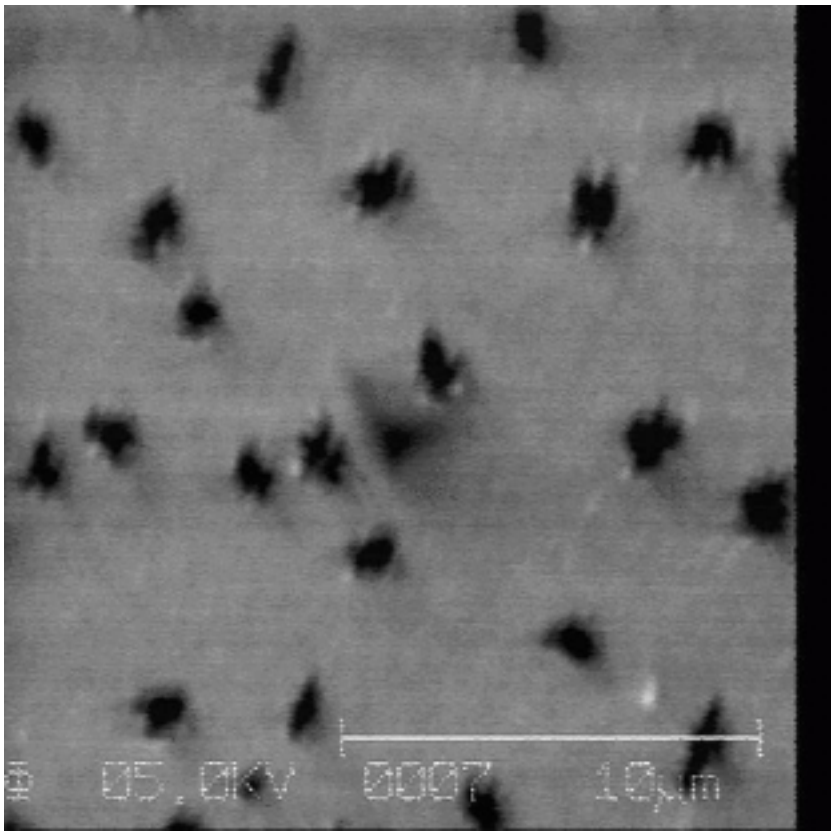

Fig. 4.3.2 SEM image of Au layer in the sputtering crater of Si/Au/ZnTe:Cu sample. Lighter background corresponds to pure Au, and dark dots contain Te and Au. Te diffused into the Au after annealing.

4.4 Analysis of J-V and R-V Dependencies Based on the Two-Diode Model.

4.4.1 General Description and Explanation of the R(V) Specific Features

Usually the J-V characteristics of cells with enhanced series resistance display evidence of a reverse diode presence which can be attributed to the back contact. It is better to analyze not the J-V characteristic itself , but the so called "dynamic resistance", R=dV/dJ, which emphasizes specific features of the J-V characteristic, makes them more observable, and sometimes even helps to understand better their nature. This is well seen from the comparison of Figures 4.1.4 and 4.1.5 that present J(V) and R(V) dependencies measured in the dark on as-prepared and degraded cells.

The specific features we are focused on are:

- as the magnitude of forward bias applied to the cell increases, the dynamic resistance first decreases quickly, but then, at some V value, the derivative dR/dV changes its sign, and R starts to rise; the appearance of a minimum in the R(V) curve is a typical feature of the cells with enhanced series resistance;
- at some higher voltage, the R(V) curve exhibits a maximum and then drops; to observe this clearly the voltage range of measurements should be extended to V>+1V.

Both these features can be attributed to the back-contact Schottky diode. Indeed, the main diode (MD) resistance decreases rapidly with increase of the current through the cell, J. At the same time, a positive sign of J corresponds to the reverse direction for the back contact Schottky diode (SD). If the saturation current for the SD is low enough (as in degraded cells), then, at some achievable current density, these two resistances become equal to each other. As J increases further, the SD resistance exceeds the MD resistance more and more. The total resistance of the cell increases. Thus, at some current density /applied voltage, the measured resistance should have a minimum. As to the appearance of a maximum , the decrease of a Schottky diode resistance at some high enough voltage can be explained when examining major factors that influence the SD saturation current.

For the simplest Bethe thermionic emission theory

$$J=J_{sat}\cdot[\exp(qV/kT)-1];\ \ J_{sat} \propto \exp(-q\phi/kT) \qquad (4.4.1)$$

where f is the Schottky barrier height. Due to the well known Schottky effect (the image-force-induced lowering) the potential barrier height decreases with increase of the reverse bias applied to the diode. Calculations, not presented here, show that, if the Schottky effect is taken into account, there should be no current saturation. Moreover, starting from some reverse V value, the increase in J_{sat} in Eq. 4.4.1 is sharper than the decrease in the second factor, so that the resistance, dV/dJ, decreases. In the framework of the combined Thermionic Emission+Diffusion theory the effect is even more pronounced because an electric field applied to the barrier region increases the drift velocity of carriers that transit the region, and, hence, the current. The sharpest manifestation of the effect takes place when the dominating mechanism of transport is tunneling or thermally-assisted tunneling (thermionic-field emission). Indeed, the Schottky effect leads not only to the lowering of the potential barrier but also to its thinning, which also increases the barrier transparency for carriers. Calculations show that the R(V) dependence for the Schottky diode has a maximum; its position on the bias axis and its sharpness depend on the dominating mechanism of transport. In the progression: Thermionic emission-Thermionic Emission+Diffusion - Tunneling, the sharpness of a peak in dV/dJ increases and its location on the V axis shifts toward lower V magnitudes (in the MD bias scale).

Leaving aside further discussion of the maximum, we will now analyze in more detail the minimum in R(V) dependence. As will be shown below, the R_{min} magnitude , as well as its location on the current and voltage axes, J_{min} and V_{min}, can lead to some

worthy conclusions about the properties of the degraded cell. The simplified model we use is based on the following assumptions:

1. The cell electric circuit contains only two diodes connected opposite to each other: the main diode (MD)-CdS/CdTe junction, and the Schottky diode at the back contact (SD). Some additional resistance, R_0, can be also connected in series with the two diodes which is supposed to be ohmic. Shunt resistance is supposed to be high enough, so that the current flowing through it can be neglected in comparison with that through the MD in J- and V- ranges of interest.

2. The MD J-V characteristic is described by the equation:

$$J_1=J_{01}[\exp(qV_1/A_1kT)-1] -J_L, \qquad (4.4.2)$$

where J_L is a photogenerated current magnitude (J_L=0 under Dark conditions), and J_1, V_1, and A_1 are the current density, voltage applied, and the diode quality factor for the MD, respectively.

3. A forward direction of the current for the MD is simultaneously a reverse direction for the SD and vice versa. In our consideration positive signs of the current density through the cell, J, and the total voltage drop, V, will correspond to the forward direction for the MD. Therefore a J-V equation for the SD can be written as follows:

$$J_2=J_1=J=-J_{02}\,[\exp(-qV_2/A_2kT)-1], \qquad (4.4.3)$$

where J_2, V_2, and A_2 are current density, voltage applied, and a diode quality factor for the SD, respectively. Properties of the SD are supposed not to be influenced by light.

4.4.2 Resistance minimum

Resistance minimum in Dark

In this case we put J_L=0 in Eq. 4.4.2. If in addition to the Schottky diode we have also some ohmic resistance (R_0), then the total voltage across the cell is:

$$V=V_1+V_2=(kT/q)\{A_1\cdot\ln(1+J/J_{01})+A_2\cdot\ln(1-J/J_{02})\}+J\cdot R_0 \qquad (4.4.4)$$

The dynamic resistance of a cell is:

$$R=dV/dJ=kT/q\{A_1/(J+J_{01}) +A_2/(J_{02}-J)\}+R_0 \qquad (4.4.5)$$

The location of the minimum dynamic resistance (R_{min}) on the current axis (J_{min}) obtained from the condition dR/dJ=0, is the same as for zero ohmic resistance (R_0=0):

$$J_{min}=J_{02}[1+(A_2/A_1)^{1/2}]^{-1} \qquad (4.4.6)$$

When deriving this equation, a supposition was made: $J_{01}/J_{02}«1$, which is valid even for degraded cells. With the same approximation the R_{min} value is given by:

$$R_{min}=(1/J_{min})\cdot(kT/q)\cdot A_1\cdot[1+(A_2/A_1)^{1/2}]+R_0 \qquad (4.4.7)$$

It is seen from Eqs. 4.4.6 and 4.4.7 that in the case of $R_0=0$,

$$R_{min}\cdot J_{min} =(kT/q)\cdot A_1\cdot[1+(A_2/A_1)^{1/2}] \qquad (4.4.8)$$

An important conclusion: *if all the cells under consideration have A_1 and A_2 values that do not vary considerably, then $R_{min}\cdot J_{min} \approx$ constant for the given temperature.*

If R_0 is of a considerable value (comparable to the measured R_{min}), then the product $R_{min}\cdot J_{min}$ is not a constant. Moreover, there can be expected a considerable spread in the product values for various cells subjected to different stress tests (temperature or duration), because there is no reason for R_0 to be the same for all the cells.

Location of the minimum R on the voltage axis is defined by

$$V_{min}=(kT/q)\cdot A_1\cdot\{\ln(J_{02}/J_{01})+Z(A_1,A_2)\}+J_{min}\cdot R_0, \qquad (4.4.9)$$

where

$$Z(A_1, A_2)=[(A_2/A_1)-1)\cdot\ln[1+(A_2/A_1)^{1/2}]-1/2(A_2/A_1)\cdot\ln(A_2/A_1)$$

The amendment Z value varies in a narrow range for a reasonable range of the A_2/A_1 ratio:

$\mathbf{A_2/A_1}$	0.25	0.5	1.0	1.5
Z	-0.131	-0.094	0	+0.096

It is seen that the major contribution to V_{min} comes from the ratio of saturation currents of the SD and MD, J_{02}/J_{01}, if $R_0<<R_{min}$.

When neglecting Z and R_0 in Eq. (4.4.9), one obtains

$$V_{min}=(kT/q)\cdot A_1\cdot\ln(J_{02}/J_{01}) \qquad (4.4.10)$$

Thus, if two parameters are known, e.g., A_1 and J_{01}, then the third parameter (e.g., J_{02}) can be estimated from V_{min}. If J_{02} is estimated from R_{min} and J_{min} analysis, then one

can use Eq. (4.4.10) to evaluate J_{01}. Unfortunately, the derived value of J_{02}/J_{01} depends exponentially on the $(qV_{min})/(A_1kT)$ value, and therefore is very sensitive to the inaccuracy of A_1.

Resistance minimum in Light

Now we must use equations (4.4.2) and (4.4.3) with $J_L>0$. Using the same approaches as in Sec. 4.4.2 we obtain the equations for J_{min} and R_{min} as follows:

$$J_{min}=J_L\cdot(\alpha+\beta)/(1-\beta)\{1-[1-(\alpha^2-\beta)(1-\beta)/(\alpha+\beta)^2]^{1/2}\}, \qquad (4.4.11)$$

where $\alpha\equiv J_{02}/J_L$ and $\beta\equiv A_2/A_1$.

$$R_{min}=(kT/q)\cdot A_1\cdot(1/J_L)\cdot[(1+J_{min}/J_L)^{-1}+\beta(\alpha-J_{min}/J_L)^{-1}]+R \qquad (4.4.12)$$

Conclusions

- Comparison of the experimental and calculated data on the $R_{min}\leftrightarrow J_{min}$ relation can help check to what extent the back-contact SD is responsible for the high series resistance in initially poor or degraded cells.
- As a first step for checking the validity of the model, we can examine the magnitude of the product $R_{min}\cdot J_{min}$ defined experimentally. According to Eq. 4.4.8, this value in Dark depends on temperature and also on the diode quality factors and for the reasonable range $1\le A_1, A_2\le 2$, at room temperature, it should be confined to the interval $0.05V \le R_{min}\cdot J_{min} \le 0.1V$. If, due to some degradation processes, the diode quality factors increase, then the product will increase too. For example, for $A_1=A_2=4$ (we do not discuss whether or not it is possible) the product value is 0.2 V.
- If the model proposed is valid, then monitoring of the minimum dynamic resistance of the cell (R_{min} value and its location on the J and V axes) allows one to obtain information on some basic parameters of the cell and their changes under cell degradation. For example, if the MD quality factor, A_1, can be obtained by some independent method, then data on R_{min}, J_{min}, and V_{min} are sufficient to estimate a saturation current of the back-contact SD, J_{02}, the saturation current of a main diode, J_{01}, and the diode quality factor of the SD, A_2.
- Analysis of the $R_{min}\leftrightarrow J_{min}$ relation for the Light J-V cell characteristics allows one in principle to estimate the SD saturation current in Light. Also some information can be obtained on trends of A_2 and A_1 "Dark - Light" changes. Comparison with the Dark data can help to understand better the influence of illumination on properties of both diodes. (We do not discuss here the complicated procedure of V_{min} analysis).

4.5 Discussion of the Experimental Data for the Cells Subjected to the Temperature-Stress Test

In this section experimental data on Cell degradation at enhanced temperature (see Sec 4.1) will be discussed on the basis of the two-diode model using the analysis presented in Sec.4.4.

4.5.1 Data Obtained in Dark

First, let us check whether the two-diode model fits our experimental data. It was shown in Sec. 4.4 that for this model the R_{min} value and its location on the J-axis, J_{min}, are totally determined by the SD saturation current density, J_{02}, and by diode quality factors for the MD (A_1) and the SD (A_2) (see Eqs. 4.4.6 and 4.4.7). There is an important relation between R_{min} and J_{min}.

$$R_{min} \cdot J_{min} = (kT/q) \cdot A,$$

where

$$A = A_1 \cdot [1 + (A_2/A_1)^{1/2}]$$

Thus for the two-diode model the product $R_{min} \cdot J_{min}$ value should not vary considerably from cell to cell even if the R_{min} and J_{min} values themselves vary in wide ranges. For T=300K, $R_{min} \cdot J_{min} = A \cdot 0.0258$ V and in a reasonable range of A_1 and A_2 variation (from 1 to 2) one obtains:

$$2 < A < 4,$$

$$R_{min} \cdot J_{min} = 0.0516 \text{ V} \quad \text{for } A_1 = A_2 = 1,$$

$$R_{min} \cdot J_{min} = 0.1032 \text{ V} \quad \text{for } A_1 = A_2 = 2$$

Significant deviations of measured values of $R_{min} \cdot J_{min}$ beyond these limits must be considered as evidence that the two-diode model does not work well and that there exists some series resistance different from the SD resistance and/or some low-resistance shunts connected in parallel with the MD and/or SD. In this case we should also expect a significant spread in the product values for different cells because there is no reason for these additional resistances and shunts to be quite the same for different cells.

Table 4.5.1 presents data for several cells with different conditions of preparation or degradation. Beside R_{min}, J_{min}, and their product, the V_{min} values are also presented that indicate the R_{min} location on the V-axis.

Table 4.5.1 Minimum R characteristics for the cells with different conditions of preparation or degradation (from J-V characteristics measured in Dark). All the cells were degraded in Dark under open circuit conditions, except #7 and #8. The latter were degraded in Dark under reverse bias V=-1V

Cell #	Conditions of degradation	Rmin [Ω/cm2]	Jmin [mA/cm2]	Vmin	Rmin·Jmin
1	As-prepared w/o etching CdTe surface	27	3.1	0.79	0.084
2	Air, room 6 months	17	5.2	0.78	0.088
3	Vac., 1100C 22 hours	79	1.1	0.79	0.087
4	Vac.,1100C 683 hours	105	0.85	0.7	0.089
5	Vac., 1400C 20 hours	155	0.55	0.7	0.085
6	Vac., 800C open circuit 100 hours	61	1.4	0.75	0.085
7	Vac., 800C, rev. bias, 100 hours	28	4.2	0.82	0.12
8	Vac., 800C, rev. bias 280 hours	220	0.8	0.67	0.18

It is seen from the Table that R_{min} and J_{min} vary over wide ranges of magnitude. At the same time the product $R_{min}\cdot J_{min}$ is surprisingly constant for the first six cells: 0.087 ± 0.002. The obtained experimental value of the product is well within the calculated range: 0.0516-0.1032 V for T=300K and $1\leq A_1, A_2\leq 2$. These results may be considered as strong evidence of the validity of the two-diode model with respect to the cells #1 through #6. Cells #7, #8 with a $R_{min}\cdot J_{min}$ product value that differs considerably from 0.087 V, are included in the table on purpose, to demonstrate that not always are the experimental data in such a good agreement with the two-diode model theory. These cells were degraded under applied bias simultaneously and in the same chamber as cell #6. Probably, the degradation processes under bias differ from those under open circuit conditions. Degradation in the biased cells will be discussed later, but now let us come back to the cells that match the two-diode model predictions. It should be mentioned that we are able to present much more data matching the model with practically the same $R_{min}\cdot J_{min}$ values, but these have not been included to avoid overloading the table.

Now, if there is evidence of the validity of the two-diode model for many cells with enhanced series resistance, let us try to derive more information from the R(V) or R(J) analysis. The first step will regard the diode quality factors. The coefficient $A=A_1[1+(A_2/A_1)^{1/2}]$ can be derived using the formula $A=(R_{min}\cdot J_{min})/(kT/q)$. From the data in Table 4.5.1 we find that $A\approx 3.4$.This value depends on both diode factors. Thus to define one of them, we need some independent information about the other, or at least, some reasonable estimation of the other. Let us suppose that $A_2=1$ which is reasonable for a Schottky diode. Then from the A value we find $A_1=1.95$. If $A_2=2$ is supposed, then $A_1=1.75$. The difference between these two A_1 values is small (about 13%). An average $A_1=1.85$ is not in a bad agreement with the A_1 value (1.6) obtained by traditional method from $\log(J+J_L)$ vs. V analysis.

Based on A_1 and A_2 estimations and using Eq. 4.4.6., one can determine the saturation current density of the Schottky diode:

$$J_{02}=J_{min}\cdot B;\ \ B=1+(A_2/A_1)^{1/2}. \qquad (4.5.1)$$

For our estimations above of the A_1 and A_2 values, we have the following B values:

$A_2=1$, $A_1=1.95$ -> $B=1.71$

$A_2=2$, $A_1=1.75$ -> $B=2.06$

Again, the difference between these two values is small (about 15%) and we will use for the saturation current estimations an average value B=1.89. The results of the calculations are presented in Table 4.5.2.

According to Eq. 4.4.10, the location of R_{min} on the V-axis, V_{min}, depends on the quality factor of the MD and also on the ratio of saturation currents of the two diodes:

$$V_{min}=(kT/q)\cdot A_1\cdot\ln(J_{02}/J_{01}) \qquad (4.5.2)$$

Thus, J_{01} can be estimated using the formula

$$J_{01}=J_{02}\cdot\exp[-(qV_{min})/(A_1kT)] \qquad (4.5.3)$$

Assuming $A_1=1.85$ and using the data on J_{02} from the second column in Table 4.5.2, we obtained the J_{01} values presented in the last column in Table 4.5.2. It should be mentioned that the accuracy in defining J_{01} in this way is not too high. Indeed, an error in definition of the R_{min} location on the V axis of 0.01 V leads to an error in J_{01} of 23%. Another source of error is an inexact knowledge of the diode factor. With this fact in mind, one can consider the J_{01} values in the Table for different cells as practically the same (with the exception of cell#3) or, at least, differing little from each other. An average J_{01} value (excluding #3) of 6×10^{-10} A/cm^2 is of the same order of magnitude as that for the as-prepared cells defined with traditional methods.

Table 4.5.2 Schottky diode and Main diode saturation current densities derived from R(J) and R(V) experimental dependencies. Cell numbers are the same as in Table 4.5.1

Cell #	**J_{02}, 10^{-3} A/cm^2**	**J_{01}, 10^{-10} A/cm^2**
1	5.9	4.0
2	9.8	8.0
3	2.1	1.5
4	1.6	7.4
5	1.0	4.6
6	2.6	6.0

An analysis presented above leads us to the following conclusions:

- In the cells degraded at enhanced temperature, in Dark and under open circuit conditions, back contact degradation is due to changes in the properties of the back contact Schottky diode, namely due to decrease in the Schottky diode saturation current. The higher the temperature and the longer the stress testing, the lower the saturation current.

- With respect to the saturation current, the main diode degrades less than the back contact Schottky diode.

- There is no indication of any changes in the diode quality factors for both diodes which indicates no changes in the transport mechanism during the stress tests performed.

The results of the experiment presented below can be considered as a straight confirmation of the conclusion that the main diode degrades only a little, while degradation of the SD is significant under High Temperature, Dark, Open Circuit conditions. CdTe/CdS structures without back contacts were annealed in a vacuum chamber at 110^0C for 40 hours in dark. Then the back contacts were applied to the cells using our routine procedure and the cells were subjected again to the same stress conditions at open circuit. Figures 4.5.1 and 4.5.2 show J-V and R(V) dependencies measured in Dark on one of these cells before (curves C) and after (curves D) a second annealing. For comparison the same dependencies are shown for cells fabricated with the usual procedure before (curves A) and after stress testing (vacuum, Dark , open circuit, 110^0C, 40 h) (curves B). The as-prepared cell fabricated on annealed material (C) demonstrates just the same properties as the as-prepared cell fabricated on non-annealed material (A). That means that no degradation of the CdTe/CdS structure takes place if there is no back contact. After this cell (C) was stress tested, the changes were observed to be typical of the case of the back contact degradation (compare curves D and B).

As to the possible mechanism of the SD saturation current decrease (increase in the back contact SD resistance), we discussed this issue in Sections 4.1 and 4.2. Based on the observed strong correlation between R_{se} increase and decrease in doping level in the CdTe adjacent to the ZnTe interface (derived from C-V profile measurements), we concluded that the major reason for the SD degradation is strengthening of the Schottky barrier. The latter is due to a decrease in doping level which leads to increase in both barrier height and width.

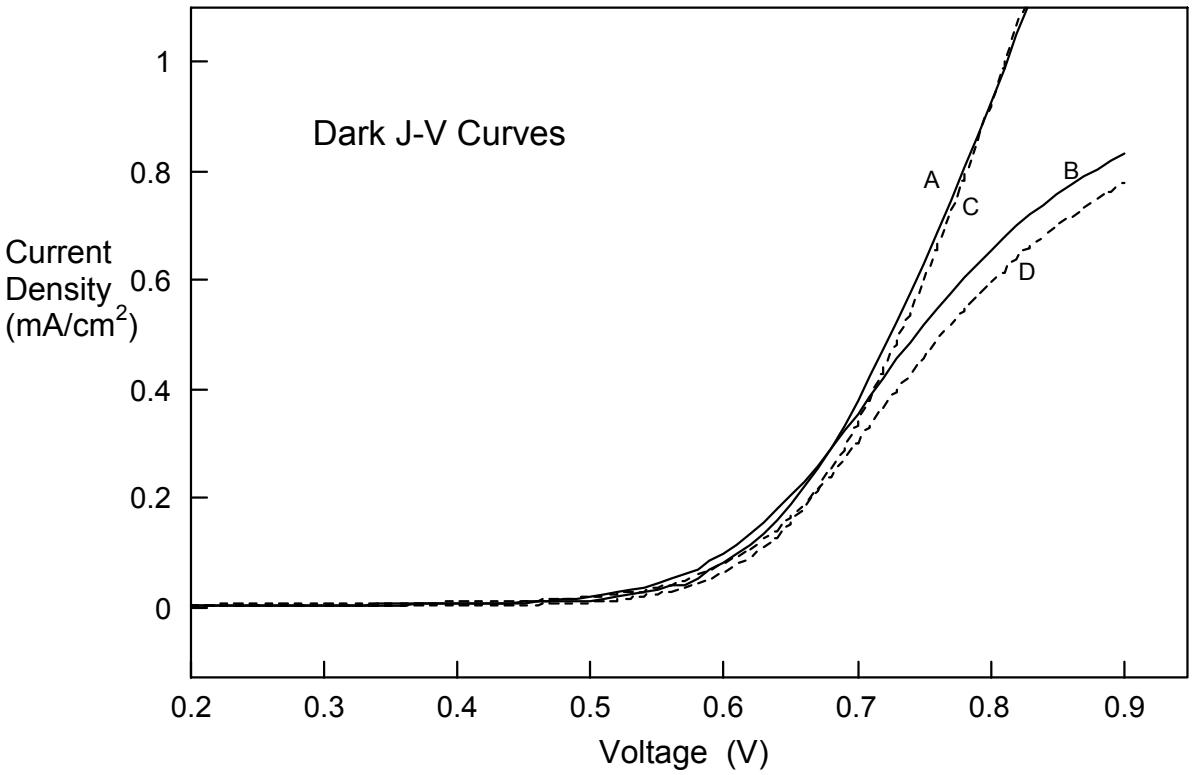

Fig. 4.5.1 Dark J-V curves for cells with different conditions of ZnTe:Cu/Au back contact application.
A - back contact was applied to the CdTe/CdS substrate supplied by SCI;
C - SCI CdTe/CdS substrate was annealed at 110^0C for 40 hours before back contact application;
B - completed cell A was annealed for 40 hours at 110^0C
D - completed cell B was annealed for 40 hours at 110^0C

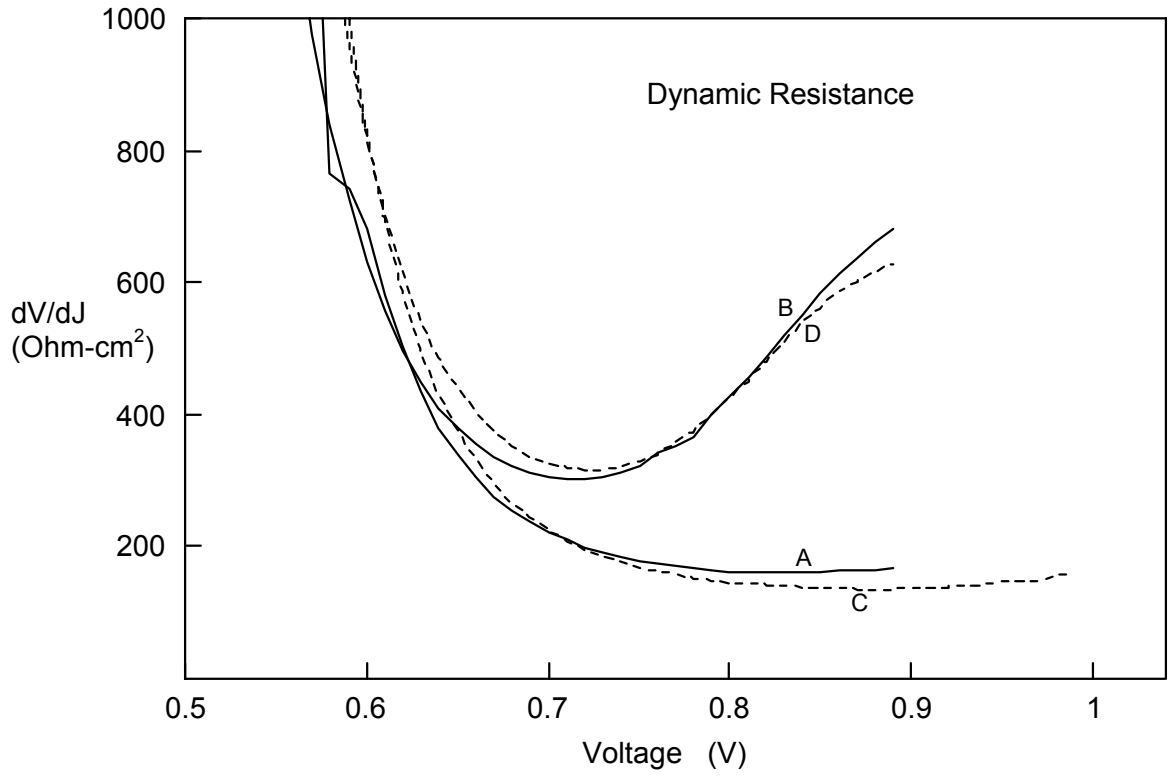

Fig. 4.5.2 Dynamic resistance as a function of bias for the cells presented in Fig. 4.5.2

4.5.2 Analysis of J-V and R(J) Dependencies Measured in Light

R(V) dependencies measured in light manifest minima and maxima less clearly than those measured in Dark. The accuracy in their location on the J- and V-axes is also lower. Therefore we will apply to these data some simplified analysis to reveal and discuss the differences between parameters derived from the Light and Dark measurements.

To simplify the analysis we put in Eqs. 4.4.11 and 4.4.12 $A_2=A_1$ and $J_L=J_{sc}$ which brings us to

$$J_{min}=(J_{02}-J_{sc})/2 \qquad (4.5.4)$$

$$R_{min}=(2kT/q)\cdot A_1\cdot(J_{min}+J_{sc})^{-1} \qquad (4.5.5)$$

$$J_{02}=J_{sc}+2J_{min} \qquad (4.5.6)$$

At T=300K $R_{min}\cdot(J_{min}+J_{sc})=0.0516\cdot A_1$

In Table 4.5.3 the measured and calculated data for several cells degraded under different conditions are presented. For all the cells J_{sc} was around 20 mA/cm^2.

Table 4.5.3 R_{min} parameters obtained from the Light J-V dependencies, and J_{02} and A_1 values calculated with Eqs. 14 and 15. $J_{sc}\approx 20$ mA/cm^2

V_{min} (V)	R_{min} (Ω-cm)	J_{min} (mA/cm^2)	$R_{min}\cdot(J_{min}+J_{sc})$ (V)	J_{02} (mA/cm^2)	A_1
0.75	8.5	2.3	0.19	25	3.7
0.82	6.5	4.1	0.16	28	3.1
0.82	5.2	7.4	0.14	35	2.7
0.75	6.8	0.5	0.14	21	2.7
0.76	7.5	2.4	0.17	25	3.3
0.89	3	32	0.16	84	3.1

It is seen from the table:

- according to the theory prediction, the product $(J_{min}+J_{sc})\cdot R_{min}$ does not vary much for all the cells although J_{min} and R_{min} variations are rather significant;
- saturation current of the Schottky diode in Light, J_{02}, is much higher than that in Dark (see Table 4.5.2);
- the diode quality factor is higher in Light than in Dark

It should be mentioned that more exact calculations based on Eqs.4.4.11 and 4.4.12. If our approach to the data treatment is correct (no serious errors in the model and approximations), then one can conclude:

- the transport mechanism in the diode/diodes in Light differs from that in Dark as indicated by the significant increase in the diode factor;
- the saturation current of the SD increases considerably in Light.

The last conclusion needs to be checked thoroughly, but if it is valid, we have to explain the mechanism of illumination influence on the SD behavior. Can it be explained by the direct influence of the light having photon energy below the CdTe bandgap which is not absorbed by the CdTe layer, or we should discuss some other possibilities? In any case, along with the checking of the validity of the model we used, we are going to perform some additional experiments that may help us to clarify the problem.

4.5.3 Conclusions

• Stress testing at enhanced temperature under Dark and Open circuit conditions accelerates cell efficiency degradation mostly through the decrease of FF and increase of R_{se}. The latter is caused by strengthening of the ZnTe/CdTe Schottky barrier due to a decrease in the CdTe doping level.

• A simple Two-Diode model describes successfully the J-V characteristics of the degraded cells. Analysis of a minimum dynamic resistance magnitude together with its location on the current and voltage axes allows us to estimate diode quality factors and saturation currents for both diodes. Hopefully, this approach can be useful for the clarification of degradation mechanisms.

• Analysis of the experimental data based on the Two-Diode model revealed significant changes in saturation current and diode quality factor caused by illumination not only for the main diode but also for the back contact Schottky diode.

4.6 Bias-Stress Test. Possible Influence of Defect Electromigration on Cell Degradation

As was shown in Sec. 4.5, the cells subjected to temperature-stress tests degraded mostly due to degradation of the back contact Schottky diode. Properties of the bias-stress-tested cells could not be explained in the framework of the simple two-diode model. That indicated that the degradation processes in this case could be more complicated than under enhanced temperature only. In this section we present some preliminary results of degradation studies under bias and discuss them on the base of possible influence of electromigration of electrically active defects.

4.6.1. Experiment

In order to reduce the temperature effect on the device during bias test, a lower temperature of 80^0C was applied while cells were under bias testing. Tests were conducted in vacuum and in the dark. Three bias conditions were used: forward bias (+0.5 V), reverse bias (-1.0 V), and open circuit. The Cu concentration in ZnTe was 4 at.%. Devices were characterized after each period of time testing. The change of performance is summarized in Table 4.6.1.

The cells stress-tested under open circuit conditions demonstrated small changes in performance after 280 hours testing. (See also cell #6 in Table 4.5.1). The degradation mostly came from an increase in R_{se}, which was not too high and led to a decrease of fill factor only from 69.4% to 66.3%. The diode quality factor and saturation current did not show any change compared with as-prepared cells, which means that the quality of the main junction remained unchanged under such stress test at open circuit conditions.

Table 4.6.1 Cell performance under stress-bias testing.

Bias	Time (hours)	η (%)	V_{OC} (mV)	J_{sc} (mA/cm^2)	FF (%)	$(R)_{V=Voc}$ (Ω-cm)	R_{sh} (Ω-cm)
Reverse	0	12	818	21	69.6	5.25	917
	100	11.6	830	20.9	67	6.09	2660
	280	8.25	747	19.5	57.4	9.2	436
Forward	0	12.1	807	21.4	69.9	4.47	700
	100	10.6	803	21.3	61.5	7.76	490
	280	6.9	757	19	48.1	8.2	189
Open Circ.	0	12.4	812	22	69.4	4.59	510
	100	11.8	813	21.4	67.8	5.36	582
	280	11.4	796	21.6	66.3	5.72	611

There was much larger degradation for cells under forward and reverse bias. Under forward bias efficiency degraded faster than under reverse bias. The degradation under forward bias stress test mainly came from the detriment of the main diode, which is indicated by the low shunt resistance R_{sh} and low open circuit voltage (V_{oc}). Increase in R_{se} is also responsible to some extent for the efficiency degradation. It is interesting to notice that the shunt resistance of cells under reverse bias increased considerably at the first 100 hours of testing; simultaneously some increase in V_{oc} and R_{se} was observed. Longer annealing (280 hours) led to the R_{sh} drop (though not as significant as for the forward bias), V_{oc} decrease and R_{se} increase. The fill factor dropped significantly: from 67 to 57%. Thus, applying an external electric field accelerated some processes that led to the degradation of the main junction besides possible degradation of the back contact.

To understand better the degradation mechanisms of cells under bias stress, we must analyze the diffusion and drift processes of the most mobile electrically active defects/ impurities in the cells.

4.6.2 Comparison of Diffusion and Electromigration

Two mechanisms of electromigration of charged impurity species should be taken into account: (1) "electron wind", or drag of ions by electron/hole current, (2) drift of ions in an electric field.

Electron Drag

If the same electric field causes the ion drift and the electron drift, then the ion drag by electrons can be taken into account by introducing an effective ion mobility [35]:

$$\mu_{ieff}=\mu_{i0}\,(1-n_e\cdot l_e\sigma_i), \qquad (4.6.1)$$

where μ_{io} is an ion mobility, n_e is a concentration of electrons, l_e is an electron mean free path length, and σ_i is the electron scattering cross section of ions.

We have in the cell an electric field that varies considerably over the cell thickness and even has opposite signs in different parts of the cell structure. The free electron and hole concentration is essentially non-uniform spatially (and generally is different from the equilibrium value). Finally, the electron/hole current in the solar cell is defined not only by the applied voltage but also by illumination intensity. Under some conditions (e.g., at $V<V_{oc}$) the current direction is opposite to the voltage across the cell. For all these reasons it should be better to express the electron drag contribution to the ion current through the electronic current density which is the same in all parts of a cell.

Based on Eq. 4.6.1 we have derived another equation that allows us to estimate the ratio of ion current density caused by the drag effect (J_2) to that due to ion drift in the electric field (J_1):

$$J_2/J_1=q(l_e/\mu_e)\sigma_i\cdot(j_e/E), \qquad (4.6.2)$$

where μ_e and j_e are electron/hole mobility and current density, respectively, and E is the electric field strength.

To estimate the possible influence of a drag effect in p-CdTe, we used the following
hole parameter values : $m_h\leq 100$ cm^2/Vs at room temperature and $m_h^*\sim m_0$, which leads to $l_h\leq 10$ nm. Based on [35], one can assume a hole scattering cross-section of ions in CdTe, $\sigma_i\leq 10^{-12}$ cm^2. With these parameter values, we obtain for p-type CdTe:

$$(J_2/J_1)\leq 0.1\cdot[J_e,\ \text{A/cm}^2]/[E,\ \text{V/cm}]$$

This formula is correct only for the material parameter values assumed. For different semiconductors, especially heavily doped and at low temperature, the electron drag effect might be much higher. But for p-CdTe this is not a bad estimation.

In the depletion layer in the CdTe, the electric field is of the order of 10000 V/cm. Thus, the drag effect can be neglected until the electron/hole current density is as high as 1000 A/cm^2 which seems impossible for our cells. It is seen that the relative role of the drag effect at the given current density increases as the electric field decreases. That means that the drag contribution to the total electromigration can become considerable in CdTe beyond the depletion layer where the electric field strength is orders of magnitude smaller than within the depletion layer. But in this region, the field is so small that electromigration itself can be neglected as compared to ion diffusion.

Conclusion**:** *Electron drag effects can be neglected when considering electromigration of ions in CdTe solar cells.*

Ion Drift in Electric Field in Comparison to Diffusion

To estimate approximately what dominates (drift or diffusion), one can use the ratio of two characteristic lengths:

Diffusion length $L_{dif}= (Dt)^{1/2}$ and

Drift length $L_{dr} =\mu Et$,

where D is an ion diffusion coefficient, μ is an ion mobility, and t is a time of the process duration.

Based on the Einstein relation [$\mu=D(q/kT)$] it is easy to see that

$$L_{dr}/L_{dif}=E\,(q/kT)\,(Dt)^{1/2} \qquad (4.6.3)$$

Thus, in a long enough time L_{dr} inevitably becomes greater than L_{dif}. The higher the diffusion coefficient and electric field the shorter this time:

$$L_{dr}/L_{dif} \geq 1 \text{ at } t \geq t^*, \qquad (4.6.4)$$

where

$$t^*= [(kT/q)^2]/[E^2 \cdot D] \qquad (4.6.5)$$

and t* is a convenient time scale unit. At t=t* the drift and diffusion lengths are equal to each other. The ratio L_{dr}/L_{dif} can be expressed via the duration time of the process, t, measured in t* units:

$$L_{dr}(t)/L_{dif}(t)=(t/t^*)^{1/2} \qquad (4.6.6)$$

For numerical estimations we have chosen the following diffusion coefficient values: $D=10^{-12}$, 10^{-14}, and 10^{-16} cm^2/s. Even the highest of these values is somewhat lower than the diffusion coefficient for fast Cu diffusion (through the interstitials) in CdTe at room temperature ($D\sim 3x10^{-12}$ cm^2/s) [29]. Lower D values are closer to the common diffusion coefficient values, especially for diffusion through vacancies. The electric field is assumed to be E=10000 V/cm and temperature $T=100^0C$.

D	**t***	**(L_{dr}/L_{dif}) for t=100 h**
10^{-12} cm^2/s	~10 sec	~190
10^{-14} cm^2/s	~10^3 s »17 min	~ 19
10^{-16} cm^2/s	~10^5 s »28 h	~ 1.9

It is seen that electromigration dominates diffusion for all these diffusion coefficient values for process durations even shorter or much shorter than the usual stress-test duration. As to the real conditions and duration of the cell operation, it is clear that electromigration should dominate diffusion even if diffusion coefficients are as low as 10^{-20} cm^2/s.

Conclusion: *Electromigration of the charged defects should be taken into account when considering degradation mechanisms in the cells due to defect migration. For the stress testing it can influence results even if the testing time is of the order of several days or even hours.*

4.6.3 Some Possible Effects of Electromigration in CdTe Solar Cells

As an example, the problem will be discussed with respect to Cu diffusion and electromigration. The back contact in our cells is a two-layer structure, ZnTe:Cu/Au. There is evidence that Cu diffused from the ZnTe dopes the CdTe. It was shown that the Cu presence is essential not only for the small initial series resistance but also for the degradation (see sec.4.2) The Cu diffusion constant in single crystal CdTe is very high, about $3x10^{-12}$ cm^2/s [29] at room temperature. It is believed that the high diffusivity is due to the motion of interstitial Cu. The ionic radius of Cu^+ is close to that of Cd^{++}, making substitution Cu_{Cd} easy [36]. Cu_{Cd} acts as an acceptor with an energy level of 0.3-0.35 eV above the valence band [37].

Electric Field in the CdTe

In the absence of external applied voltage and illumination, the built-in potential in the CdS/CdTe cell is about 1V and almost totally applied to the CdTe, namely to its depletion layer with the thickness W~1000 nm. Thus an average electric field is: $\langle E\rangle\sim 10^4$ V/cm. If the space charge density is constant over the depletion layer width, then $E(x)=E_{max}(1-x/W)$ $(W>x>0)$, and $E_{max}=2\langle E\rangle$. The electric field is directed from the CdS

to the CdTe pushing positive ions from the depletion layer to the neutral portion of the CdTe and pulling negative ions from the neutral region into the depletion layer (toward the CdS interface).

Application of forward bias reduces the magnitude of the electric field and makes narrower the region where the field is non-zero (the depletion layer width). In principle, for high enough forward bias (≥1V), the electric field can be reduced to a negligible level.

Reverse bias application provides the opposite effect. For high reverse voltages applied, the depletion layer can, in principle, occupy the whole CdTe layer thickness. The electric field magnitudes, both E_{max} and <E>, increase, but stay in the same range (~10^4 V/cm).

Illumination under open circuit conditions can reduce the built-in potential significantly.
One-sun intensity reduces it by ~0.8 V. Thus, the electric field strength and the depletion layer width decrease considerably, reducing the influence of electromigration. It is important to notice that application of some reverse bias (e.g., V_m) reduces the light influence restoring partially the built-in electric field.

We do not discuss here the electric field in the vicinity of the CdTe/ZnTe interface.

Possible Cu Migration (Diffusion and Electromigration)

We assume that before the back contact application, the main diode is formed in the CdS/CdTe system and there exists an electric field as described above. When ZnTe:Cu is deposited at room temperature and then annealed at T= 250-270^{0}C, a considerable diffusion of Cu into the CdTe occurs with diffusion length L~0.1-1μm. Probably, diffusion continues also after the cell is cooled. The diffusion length increases with increasing time as $t^{1/2}$ and in tens or hundreds of hours the calculated diffusion length becomes greater than the total CdTe thickness.
But, when the diffusion front of Cu (we assume that Cu diffuses mostly through the interstitials being positively charged) reaches the depletion layer edge, the electric field prevents deep penetration of Cu into the depletion layer. This is beneficial for the cell performance, because it prevents an increase in doping level in the vicinity of the CdS/CdTe interface and hence keeps the depletion layer thick enough to provide the collection of almost all photogenerated electrons by the p-n junction. This stopping of Cu-ion flow in the direction of the p-n junction prevents also the development of current paths due to an excess of Cu in the junction vicinity (decrease in shunt resistance).

Let us consider the influence of the bias applied in *Dark.*

Forward bias leads to a decrease in the built-in potential. The consequences are: (1) the depletion layer edge shifts toward the CdS interface, hence the Cu distribution front shifts in the same direction; (2) the magnitude of the electric field decreases, hence the force pushing Cu_i^+ ions back decreases. Thus, one can expect: a decrease in R_{sh}, J_{sc}, and, probably, V_{oc}.

Reverse bias increases the electric field in the depletion layer and its width. Expected changes in the Cu distribution are opposite to those for the forward bias. In particular, one can expect even an increase in R_{sh}.

So far we have not taken into account another mechanism of Cu diffusion. It is believed that Cu in Cd sites (Cu_{Cd}) acts as an acceptor. In this position Cu is charged negatively. Indeed, we must consider the sign and magnitude of electrical charge for the substitutional Cu atom with respect to the Cd ion it replaces. The latter manifests in CdTe a valency close to 2 and its effective charge is close to +2. We do not have definite data on the valency of Cu_{Cd} in CdTe. If it is bi-valent, its charge with respect to the Cd sublattice should be zero. If it is single-valent (which is more probable, see [3]) its effective charge is -1.When accepting an electron from the valence band of CdTe (acceptor action), the Cu ion acquires an additional charge of -1.

Drift of negatively charged Cu_{Cd} ions in an electric field occurs in a direction opposite to that for Cu_i in the interstitials. The number of Cu_{Cd} is greater than that of Cu_i. The substitutional Cu diffusivity (D_s) should be much lower than that of interstitial Cu (D_i). We do not have any reliable information on Cu diffusivity through Cd vacancies, that is through Cd sites. Suppose that $D_s \sim 10^{-16}$ cm^2/s for the diffusion through sites. It can be even lower. For T=100 C and $E=10^4$ V/cm, t*~30 h. In this time both L_{dif} and L_{dr} reach ~ 30 nm value, which is only a small portion of the depletion layer width. Thus, one can not expect considerable effects due to Cu_{Cd} diffusion and drift. A significant influence should be expected when the Cu front penetrates a considerable portion of the depletion layer. For example, it will take 300 hours (if $D_s=10^{-16}$ cm^2/s) for the Cu front to drift by 300 nm toward the interface; ~900 h to drift by 1000 nm. For $D=10^{-15}$ we have for the same T and E: t*=9.04 h; drift by 1000 nm in 280 hours.

Thus, because diffusion through sites (vacancies) occurs much slower than through interstitials, it may happen that first we will see an increase in R_{sh} after reverse bias application, due to the positive interstitial-Cu ions outdrift from the depletion layer to the neutral CdTe. But later, in a considerably longer time, the opposite effect will take place due to the negative site-Cu ions much slower diffusion and drift into the depletion layer. Something like that was observed in our bias-stressed degradation studies (see Sec. 4.6.1).

4.6.4 Conclusions

- There exist high electric fields in some portions of the CdTe solar cell which may influence considerably the defect migration even without external bias or light application.

- The analysis above enables us to explain, at least qualitatively, some peculiarities of the results of our bias-stress tests performed in Dark.

- When analyzing defect migration under real cell operation conditions or under stressing one must consider the electric field magnitude and distribution changes. Illumination itself may cause even greater changes in defect migration than illumination in combination with reverse bias.

5. AKNOWLEDGEMENTS

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7. APPENDICES

7.1 List of Publications from this Research:

1*. "Effect of Annealing on Microstructure, Residual Stress, and Photovoltaic Characteristics of Electrodeposited CdTe Films", D. Kim, B. Qi, D.L. Williamson, and J.U. Trefny, *Proc. 24th IEEE PVSC*, 338 (1994).

2*. "Polycrystalline Thin Film CdTe Solar Cells Fabricated by Electrodeposition", D. Kim, S. Pozder, Y. Zhu, and J.U. Trefny, *Proc. 24th IEEE PVSC*, 334 (1994).

3*. "Interdiffusion in Polycrystalline Thin Film CdS/CdTe Solar Cells", D. Mao, L.H. Feng, Y. Zhu, J. Tang, W. Song, R. Collins, D.L. Williamson, and J.U. Trefny, *13th NREL Program Review Meeting, AIP Conf. Proc.* **353**, edited by Harin S. Ullal and C. Edwin Witt, (AIP, New York, 1995) p.352.

4*. "Effect of Annealing on Microstructure, Residual Stress, and Photovoltaic Characteristics of Electrodeposited CdTe Films", B. Qi, D. Kim, D.L. Williamson, and J.U. Trefny, *J. of Electrochem. Soc*. **143,** 517 (1996).

5*. "The Structural, Optical, and Electrical Properties of Vacuum Evaporated Cu-doped ZnTe Polycrystalline Thin Films", L.H. Feng, D. Mao, J. Tang, R. Collins, and J.U. Trefny, *J. Electron. Materials* **25**,1433 (1996).

6*. "Effect of $CdCl_2$ Treatment of CdS Films on CdTe/CdS Solar Cells", W. Song, D. Mao, L. Feng, Y. Zhu, M.H. Aslan, R.T. Collins, and J.U. Trefny, *Mater. Res. Soc*. *Symp. Proc.* **426**, 1996, pp. 331-336.

7*. "Study of ZnTe:Cu Back Contacts on CdTe/CdS Thin Film Solar Cells", J. Tang, L. Feng, D. Mao, W. Song, Y. Zhu, and J.U. Trefny, *Mater. Res. Soc*. *Symp. Proc.* **426**, 1996, pp. 355-360.

8*. "Chemical Bath Deposition of CdS Thin Films: Growth and Structural Studies", Y. Zhu, D. Mao, D.L. Williamson, and J.U. Trefny, *Mater. Res. Soc*. *Symp. Proc.* **426**, 1996, pp. 227-232.

9*. "The Properties and Optimization of ZnTe:Cu Back Contacts on CdTe/CdS Thin Film Solar Cells", J. Tang, D. Mao, L. Feng, W. Song, and J.U. Trefny, *Proc. 25th IEEE Photovoltaic Specialists Conference,* 1996, pp. 925-928.

10*. "Fabrication of CdTe Thin Film Solar Cells Using Electrodeposition", W. Song, D. Mao, Y. Zhu, J. Tang, and J.U. Trefny, *Proc. 25th IEEE Photovoltaic Specialists Conference,* 1996, pp. 873-876.

11*. "Effect of Cu Doping on the Properties of ZnTe:Cu Thin Films and CdS/CdTe/ZnTe Solar Cells", J. Tang, D. Mao, and J. U. Trefny, *Proc. 14th NREL Photovoltaic Program Review Meeting,* 1996, pp.639-646.

12*. "Properties of ZnTe:Cu Thin Films and CdS/CdTe/ZnTe Solar Cells", J. Tang, D. Mao, T.R. Ohno, V. Kaydanov, and J.U. Trefny, *Proc. 26th IEEE Photovoltaic Specialists Conference*, 1997, pp. 439-442.

13*. "Electrodeposited CdS Thin Films and their Application in CdS/CdTe Solar Cells", Figen Kadirgan, D. Mao, A. Balcioglu, B.E. McCandless, W.Song, T.R. Ohno and J.U. Trefny, *Proc. 26th IEEE Photovoltaic Specialists Conf.,* 1997, pp.443-446.

14*. "Photoconductive Lifetime of CdS used in Thin-Film Solar Cells", R.K. Ahrenkiel, D.H.Levi, S. Johnston, W. Song, D. Mao and A. Fisher, *Proc. 26th IEEE Photovoltaic Specialists Conference*, 1997, pp. 535-538.

15*. "Sulfur Diffusion in Polycrystalline Thin-Film CdTe Solar Cells", M.H. Aslan, W.Song, J.Tang, D. Mao, R.T. Collins, D.H. Levi, R.K. Ahrenkiel, S.C. Lindstrom, M.B. Johnson, *Mater. Res. Soc. Symp.*, Fall 1997, in print.

7.2 List of the CSM to NREL Technical Reports Cited in the Text

Technical Reports on the project "Polycrystalline Thin Film Cadmium Telluride Solar Cells Fabricated by Electrodeposition" prepared by the CSM for the National Renewable Energy Laboratory under Subcontract No. XAF-5-14142-11 (U.S. Department of Energy Prime Contract No. DE-AC02-83CH10093):

1® Annual Technical Report, March 20, 1995 to March 19, 1996, NREL/SR-520-21927 (4197).

2® Annual Technical Report, March 20,1996 to March 19, 1997, NREL/SR-520-23994 (1198).

3® Quarterly Technical Status Report, for Quarter Ended June 30, 1997 (unpublished).

4® Quarterly Technical Status Report, for Quarter Ended September 30, 1997 (unpublished).

5® Quarterly Technical Status Report, for Quarter Ended December 31, 1997 (unpublished).

6® Quarterly Technical Status Report, for Quarter Ended March 31, 1998 (unpublished).

7.3 Personnel

Many individuals contributed to this work. Their names, titles, and representative responsibilities are summarized below. Those who have been envolved during just a portion of the project period are noted.

John U. Trefny, Professor of Physics: Project coordinator.

Duli Mao, Research Assistant Professor: Photovoltaic Development, Principal Coinvestigator (left CSM 06/97).

Victor Kaydanov, Research Professor: Electron Transport Phenomena, Photovoltaic Development, Co-Principal Investigator (since 06/97).

Timothy R. Ohno, Associate Professor of Physics: Surface Physics, Photovoltaic Development.

Don L. Williamson, Professor of Physics: XRD.

Reuben Collins, Professor of Physics: Electronic and Optical Properties of Semiconductor Materials.

Tom. E. Furtak, Professor of Physics: Optical Properties of semiconductors.

Lianghuan Feng, Visiting Professor: ZnTe Back Contact and Cell Fabrication (left 08, 1995).

Figen Kadirgan, Visiting Professor: Electrodeposition of CdS (1996).

Yuming Zhu, Graduate Research Assistant: CdS Chemical Bath Deposition (defended PhD thesis 1996).

Jian Tang, Graduate Research Assistant: ZnTe Back Contact, Cell Fabrication and Stability (defended PhD thesis April 1998).

Wenjie Song, Graduate Research Assistant: CdTe Elecrodeposition, Characterization and Cell Optimization.

Ahmed Al Kaoud, Graduate Student: Tranparent Conducting Oxide.

M. Hasan Aslan, Graduate Student: Photoluminescence, Interdiffusion Studies.

Esam Alarfaj, Graduate Research Assistant: CdTe Electrodfeposition (defended MS thesis 1996).

Troy Berens, Graduate Research Assistant: Thin Film Solar Cell Fabrication (defended MS Thesis 1997).

Brian Egaas, Graduate Research Assistant: Thin Film Solar Cell Fabrication.

Wendi Batchelor, Graduate Research Assistant: Thin Film Solar Cell Fabrication.

Yoxa Mahthongdy, Graduate Research Assistant: CdTe Solar Cell Processing.

Don Morgan, Graduate Research Assistant: Degradationof CdTe Solar Cells.

7.4 Laboratory Improvements

1. A major laboratory renovation project was finished in 1996-1997. This laboratory renovation project was supported by the Infrastructure Program of National Science Foundation with matching funds from the School of Mines. The total investment of NSF and CSM in this new facility exceeded $800,000 and provided a new 2,200 sq. ft. thin film processing laboratory with 3 more filtered fume hoods, a class-1,000 clean room, ample lab space, and other hardware related to the safety of staff members and students. During the renovation, efforts were made to minimize the disruption of the construction work to the CdTe project.

2. A proposal for the "Acquisition of Characterization Instrumentation for Advanced Materials Research" to the Infrastructure (Instrumentation) Program of NSF was granted. This allowed us to acquire 4 pieces of equipment that are critically important for our thin film research: a Tencor P-10 surface profiler with three-dimensional imaging capability, a Cary 5G UV-Vis-NIR spectrophotometer with diffuse reflection accessory, a variable temperature Hall effect measurement station, and a three-wavelength (633, 830, 1300 nm) ellipsometer. In addition, Professor Ohno has acquired an x-ray photoemission spectroscopy system, also sponsored by the Infrastructure (Instrumentation) Program of NSF. These new instruments have all arrived and are functioning.This helps to greatly facilitate our thin films research.

For the infrastructure projects listed above, the Colorado School of Mines has provided about $800,000 in matching funds, demonstrating clearly its strong commitment to thin films and photovoltaics research.

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13. ABSTRACT *(Maximum 200 words)*
This report summarizes work performed by the Colorado School of Mines Department of Physics under this subcontract. Based on the studies conducted, researchers increased the efficiency of the cells with electrodeposited CdTe and CBD CdS by 3% on average (~30 relative %). The improvement came from 1. Optimization of CdS initial thickness taking into account CdS consumption of CdTe during the CdTe/CdS post-deposition treatment; optimization of CdS post-deposition treatment with $CdCl_2$ aimed at prevention of Te diffusion intoCdS and improvement of the CdS film morphology and electronic properties. That led to a considerable increase in short circuit current, by 13% on average. 2. Optimization of CdTe thickness and post-deposition treatment which led to a significant increase in V_{oc}, by ~70 mV. The highest V_{oc} obtained exceeded 800 mV. 3. Development of a ZnTe:Cu/Metal back contact processing procedure that included selection of optimal Cu content, deposition regime and post-deposition treatment conditions. As a result, back contact resistance as low as $0.1\Omega\text{-cm}^2$ was obtained. The cell stability was measured on exposure to accelerated stress conditions. Preliminary studies of some new approaches to improvement of CdS/CdTe structure were conducted.

14. SUBJECT TERMS
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