June 1999 • NREL/SR-520-26663

Subcontractor Report

Photovoltaic Cz Silicon Module Improvements

Final Subcontract Report
9 November 1995 — 8 November 1998

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Siemens Solar Industries
Camarillo, California

National Renewable Energy Laboratory

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Contract No. DE-AC36-98-GO10337

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NREL Technical Monitor: R.L. Mitchell

Prepared under Subcontract No. ZAF-5-14271-12

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Preface

This report describes work done by Siemens Solar Industries (SSI) from November 9, 1995 to November 8, 1998 during Phases I, II and III of a three-phase Photovoltaic Manufacturing Technology (PVMaT 4A) subcontract from DOE/NREL. The work focuses on improvements in the cost per watt of Cz silicon photovoltaic modules through detailed understanding of their cost structure, module design to minimize cost per watt, measures to improve manufacturing yield and productivity, and manufacturing control systems to improve module reliability. The overall project goal has been a reduction of Cz silicon module cost per watt of 18% at the end of the three phases of the subcontract.

Acknowledgments

Many people have contributed to the work under this contract. Thanks are due especially to Rick Mitchell, NREL technical monitor, to Ruben Balanga, Dave Bender, Eberth Covarrubia, Heinrich Eichermüller, Chet Farris, Bryan Fickett, Jean Hummel, Dave Jeffrey, Waltraut Klein, Greg Mihalik, Alex Mikonowicz, Jeff Nickerson, Ken Sandland, Maria Tsimanis, Elena Woodard, and others in the Engineering, Quality, Manufacturing, and Finance groups at SSI.

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Summary

Work focused on reducing the cost per watt of Cz silicon photovoltaic modules under Siemens Solar Industries' DOE/NREL PVMaT 4A subcontract is described in this report. New module designs were deployed in this contract, improvements in yield of over 25% were realized, and implementation of Statistical Process Control was achieved. Module configurations representing a 17% cost reduction per watt were implemented in production. Yield improvements are described in detail, and the deployment of SPC in critical process steps is reported on here. The sum of all improvements resulted in greater than a 17% cost per watt reduction in manufacturing.

Table i. Program Summary Results

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
New module designs to reduce $/W	6% reduction in module $/W ***Complete***	12% reduction in module $/W ***Complete***	18% reduction in module $/W ***17% Reduction***
Improvement of yields and reduction of labor	5% improvement in module mfg. yield 5% increase in module mfg. productivity ***Complete***	10% improvement in module mfg. yield 10% increase in module mfg. productivity ***Complete***	15% improvement in module mfg. yield 15% increase in module mfg. productivity ***Complete***
Improvement of module reliability	Implement SPC on 50% of appropriate mfg. processes ***Complete***	Implement SPC on 100% of appropriate mfg. processes ***Complete***	Assessment of SPC protocols, areas for improvement ***Complete***

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Introduction

Program Goals

The Photovoltaic Manufacturing Technology (PVMaT) project is sponsored by the U.S. Department of Energy (DOE) through the National Renewable Energy Laboratory (NREL) in order to assist the photovoltaics industry in improvement of module manufacturing and reduction of module manufacturing cost. The objective of the DOE/NREL PVMaT subcontract with Siemens Solar Industries (SSI) is to continue the advancement of Siemens Solar Industries' photovoltaic manufacturing technology in order to achieve an 18% reduction in module cost per watt at the end of three phases of work. Each phase lasts a year as shown in Table 1. Phase I of this subcontract began in November 1995. The approaches for reaching the cost reduction goal have been to analyze existing module cost structure and explore new module designs and materials, investigate the reduction of labor and improvement of yield, and to implement statistical process control (SPC) in module manufacturing.

Table 1. Goals of Siemens Solar Industries' PVMaT 4A Subcontract from DOE/NREL.

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
New module designs to reduce $/W	6% reduction in module $/W	12% reduction in module $/W	18% reduction in module $/W
Improvement of yields and reduction of labor	5% improvement in module mfg. yield 5% increase in module mfg. productivity	10% improvement in module mfg. yield 10% increase in module mfg. productivity	15% improvement in module mfg. yield 15% increase in module mfg. productivity
Improvement of module reliability	Implement SPC on 50% of appropriate mfg. processes	Implement SPC on 100% of appropriate mfg. processes	Assessment of SPC protocols, areas for improvement

Approaches

The first step toward reducing the cost per watt at the module level was to gain a thorough understanding of the present factors which dominate cost during Phase I of this contract. Armed with this knowledge, the cell and module designs were optimized to minimize the costs of ingot, wafering, cell, and module fabrication, as described in the following sections. The design of larger cells, larger modules, and match of wafer shape to ingot cross-section have shown to be simple but effective means of reducing the cost per watt of silicon photovoltaic modules during Phase II of the program when the designs were released to production. Phase III was the full deployment of the module designs in manufacturing.

In many process steps, yield loss is the greatest single contributor to the module cost per watt. Unlike other types of cost components, such as direct materials, yield loss is not an intrinsic cost of the process, and thus this cost can potentially be driven to zero. Yield loss comes in many forms, such as lost crystal

structure, off-spec resistivity, wafer thickness variation, insufficient wafer cleaning, cell breakage and its dependence on wafer thickness and other parameters. Improvement of yield across the various sources of yield loss, and focusing resources on only the most serious yield loss mechanisms was the approach taken in this contract.

Four strategies to increase manufacturing productivity at SSI have been deployed further during all three phases: 1) use of automation; 2) development of relationships with vendors to provide pre-assembled parts or improved materials; 3) critical evaluation of staffing requirements of various process steps; and 4) improved efficiency of the internal logistics of material supply. This strategy, combined with yield improvement of over 25% has allowed SSI to meet it's productivity goals.

The approach taken to improve SSI Cz silicon module reliability continues to be one of increased control over manufacturing systems, including design and material procurement, in addition to manufacturing process parameters. Statistical process control of key steps in the fabrication sequence is a cornerstone of this strategy. Many of the steps required for certification under the ISO 9001 quality system directly address the issues of manufacturing control: written documentation of procedures and work instructions; training and certification of operators; measurement of process capability factors; calibration of measurement instrumentation used to control fabrication processes; and internal and external quality audits of manufacturing compliance. SSI received ISO 9001 certification during Phase I of this contract, and passed additional surveillance audits during Phase II and Phase III of the contract, showing compliance and improvement in this focus of control and manufacturing stability. Deployment of SPC in all critical manufacturing steps has been completed during the three phases of the contract.

Module Cost Reduction

Module Cost Drivers

This section gives examples of the cost structure of module manufacturing at SSI. Once the most significant costs are known, strategies for reducing them were formulated and discussed. Finally, specific module designs that address these cost issues were developed. These improvements in module configuration have been introduced into production in the SSI Camarillo plant during the contract

Figure 1 shows the division of cost per watt at the module level among the four major process segments of wafered silicon solar cell fabrication: ingot growth; wafering; cell fabrication; and module fabrication. Module fabrication has the largest cost of these, and so is a reasonable area on which to focus efforts to reduce the overall cost per watt. However, costs in the other areas are also very significant contributors to the cost per watt at the module level, and must be addressed as well.

The costs in each process area in Figure 1 are divided to show the costs due to yield loss, the costs that would be incurred even if the yield were 100%, and manufacturing overhead costs. Yield loss in a given process area requires that upstream processes increase their production volume, in order to make up for the lost material. Yield loss in the cell fabrication area, for instance, requires that more cells be produced to make up for the loss, and requires greater production volumes in the wafer and ingot areas as well, to provide raw materials for those cells. So yield loss in a given process increases the costs residing in the upstream processes as well. This is shown in Figure 1.

If the yield were 100% in each process area, the production volume in each area could be reduced while maintaining the same overall plant MW/year output. The costs in each process area would then be the height of the bars labeled *100% yield case* in Figure 1, plus *Mfg. overhead*. The items summed under the 100% yield case are costs which increase if equipment is added to increase plant capacity (for instance, to make up for yield loss in downstream processes), in addition to material and labor costs that increase with increased production volume. These items are: direct material; indirect material; direct labor; indirect labor and fringe benefits; depreciation on capital equipment; maintenance of equipment; and building rent and utilities. *Mfg. overhead* consists of those costs which do not, to first order, increase when production volume is increased, but which are nevertheless directly associated with manufacturing. These items include the costs of manufacturing management, and the logistics, health & safety, and quality assurance departments. Functions not directly related to manufacturing, such as the marketing & sales, or finance departments, are not included in *Mfg. overhead*.

Figure 2 shows an alternate way to group the costs of yield loss. Rather than group them in the process area which must bear the burden of increased volume to make up for lost production, as in Figure 1, Figure 2 lumps the yield loss costs in the process area for which the yield loss was incurred. Thus the cost of yield loss in the module area includes not only the cost of module fabrication, but also the costs of ingot, wafer, and cell fabrication required to replace the cells in the lost modules. The *100% yield case* and *Mfg. overhead* values remain as they were before in Figure 1. This is the convention followed for the cost of yield loss in the rest of the figures.

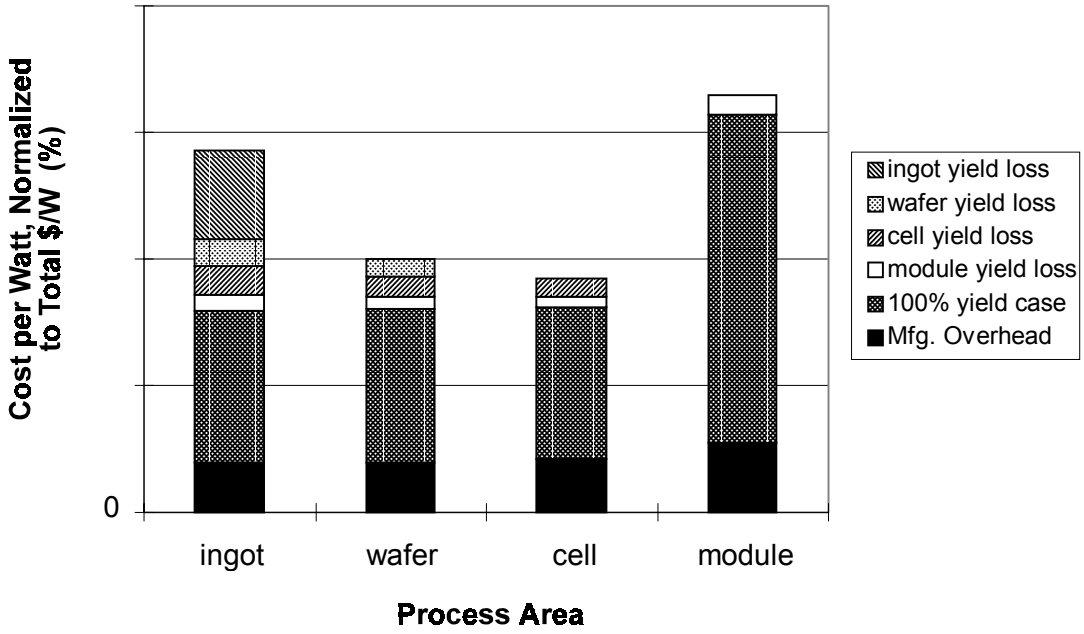

Figure 1. Cost/watt by process area, normalized to total $/W, with cost of yield loss allocated to process area in which production must be increased in order to make up for yield loss.

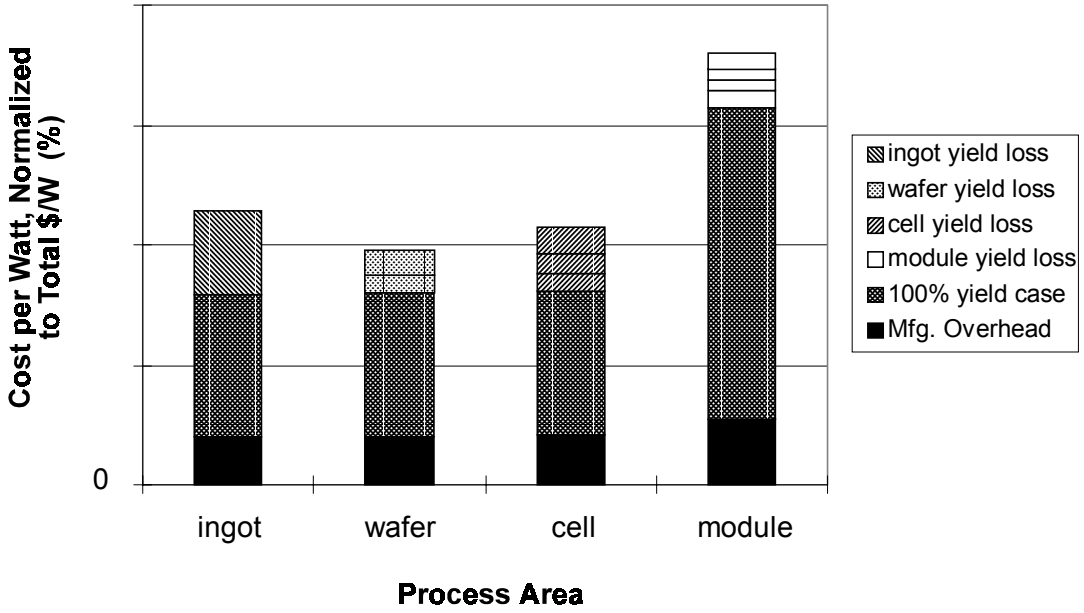

Figure 2. Cost/watt by process area, normalized to total $/W, with cost of yield loss allocated to area in which yield loss occurred.

It is instructive to break the *100% yield case* down into its component parts and compare the magnitude of these constituent costs with the cost of yield loss. This is done in Figure 3-Figure 6. In the ingot growth area, yield loss is by far the dominant contributor to cost per watt at the module level, as can be seen in Figure 3. Significant steps have been taken to combat this loss, for example, specification and procurement of an acid cleaning line for silicon feedstock used in crystal growth at the end of Phase I and a thorough study and understanding of feedstock yield effects done during Phase II. These are covered in more detail in the yield and productivity improvement sections of this report. The magnitude of the yield loss cost is followed by direct and indirect materials costs in the ingot area. Indirect materials include such parts as quartz crucibles and graphite heaters. Although Si crystal growing is an energy-intensive process, the costs of utilities have been held fairly low in comparison to other cost components, due largely to the consolidation of crystal growth operations in Vancouver, WA where electricity rates are much lower than at the Camarillo, CA site.

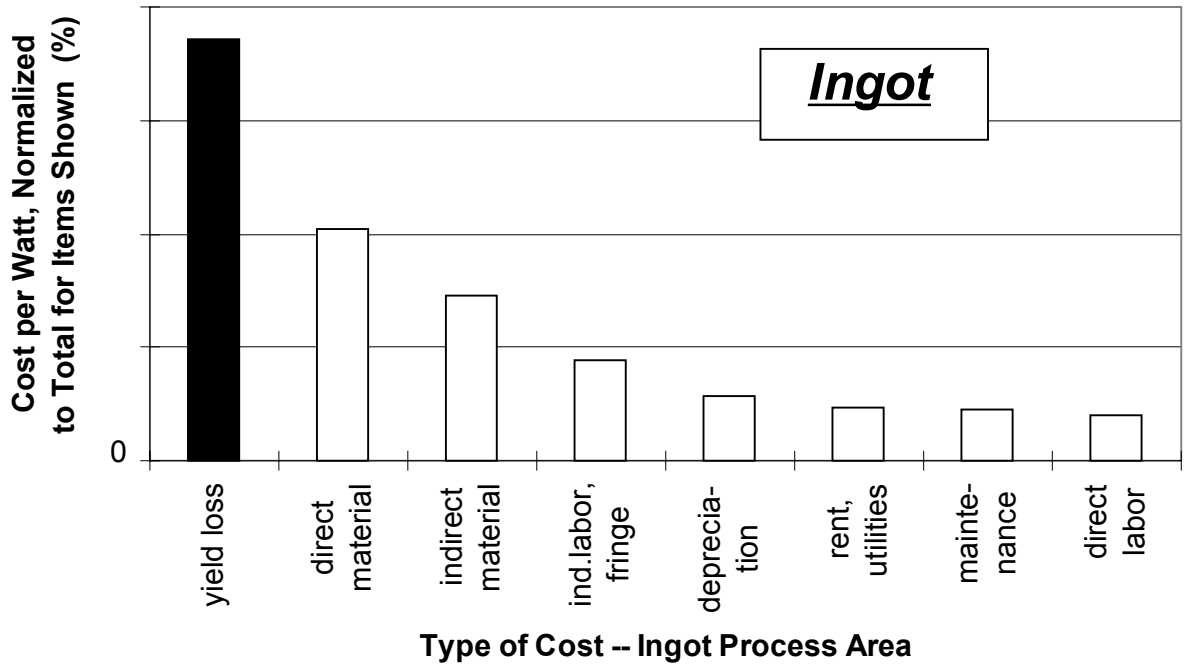

Figure 3. Ingot manufacturing costs per module watt for the case of 100% yield and the cost/watt of ingot yield loss.

Systematic exploration of wire saw parameters, such as wire tension and speed, and characterization of the properties of the silicon carbide and oil that make up the cutting slurry, have resulted in vastly improved understanding of the wire sawing process and correspondingly low yield loss. As shown in Figure 4, indirect materials, such as wire, carbide, oil, and solvent used to remove the slurry, are dominant costs in the wafering process area. Measures to reduce use of these indirect materials, such as cutting a greater number of wafers per wire saw run are covered later in this report.

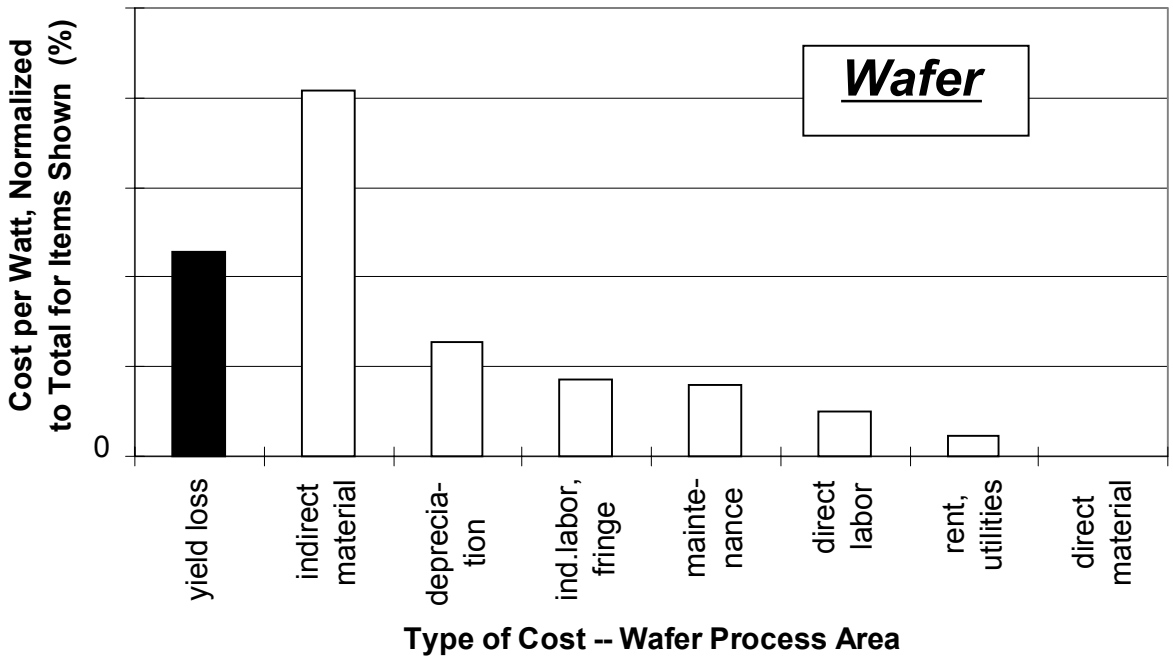

Figure 4. Wafer manufacturing costs per module watt for the case of 100% yield and the cost/watt of wafer yield loss.

In the cell fabrication area, yield loss stands out as the largest contributor to cost per watt, as can be seen in Figure 5. During Phase I the dominant cause of this yield loss was wafer breakage in the multiple automated and manual handling steps in the cell fabrication sequence. Therefore, the emphasis in Phase I, Phase II and Phase III centered on improved handling of cells through the process line and on increasing the yield of cells in the module assembly process. The technique deployed to combat this loss was to identify the fabrication steps in which breakage was greatest, strengthening feedback on mechanical yield to the operators who handle the wafers, and on understanding the dependence of force required to break a wafer on substrate and surface properties. Among the remaining costs per module watt in cell fabrication, the six next largest are fairly comparable in magnitude.

Direct materials such as glass, frames, interconnect ribbons, etc. are by far the largest component of cost per watt in the module fabrication area, as shown in Figure 6. Yield loss is the next largest cost; although the percentage of yield loss in the module area is fairly low, the costs of ingot, wafer, and cell fabrication are all folded into the yield loss cost per watt in the module area, elevating this cost. Indirect and direct labor are the two next largest cost components in the module area. While smaller than the cost of module direct materials, the yield and labor components are important factors to reduce overall.

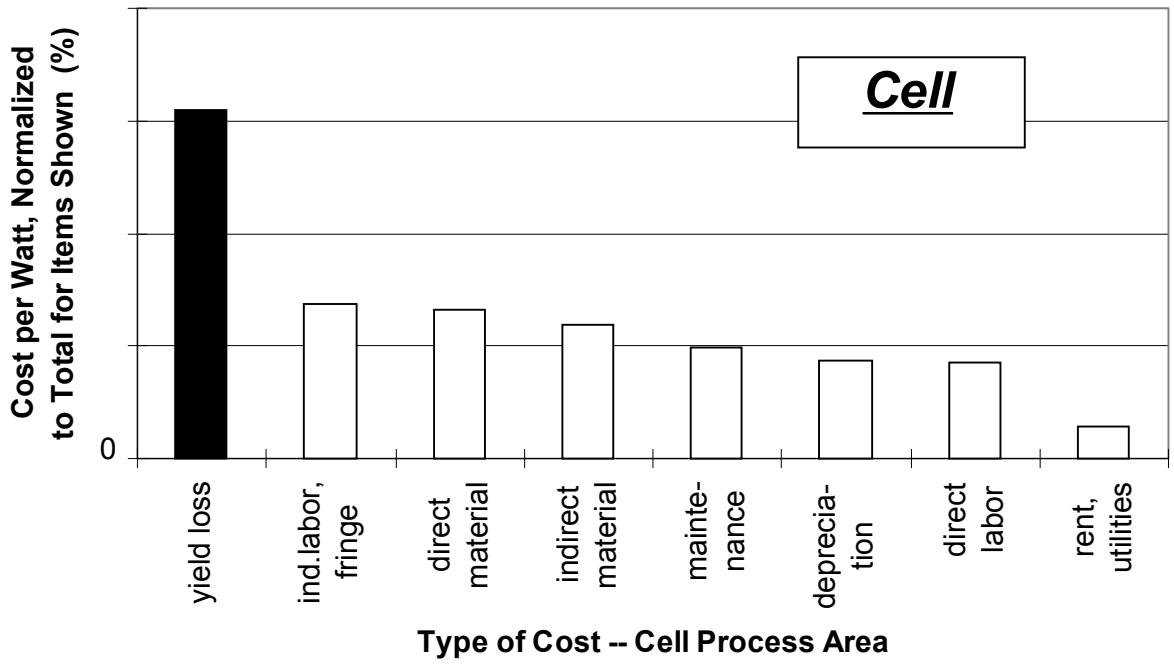

Figure 5. Cell manufacturing costs per module watt for the case of 100% yield and the cost/watt of cell yield loss.

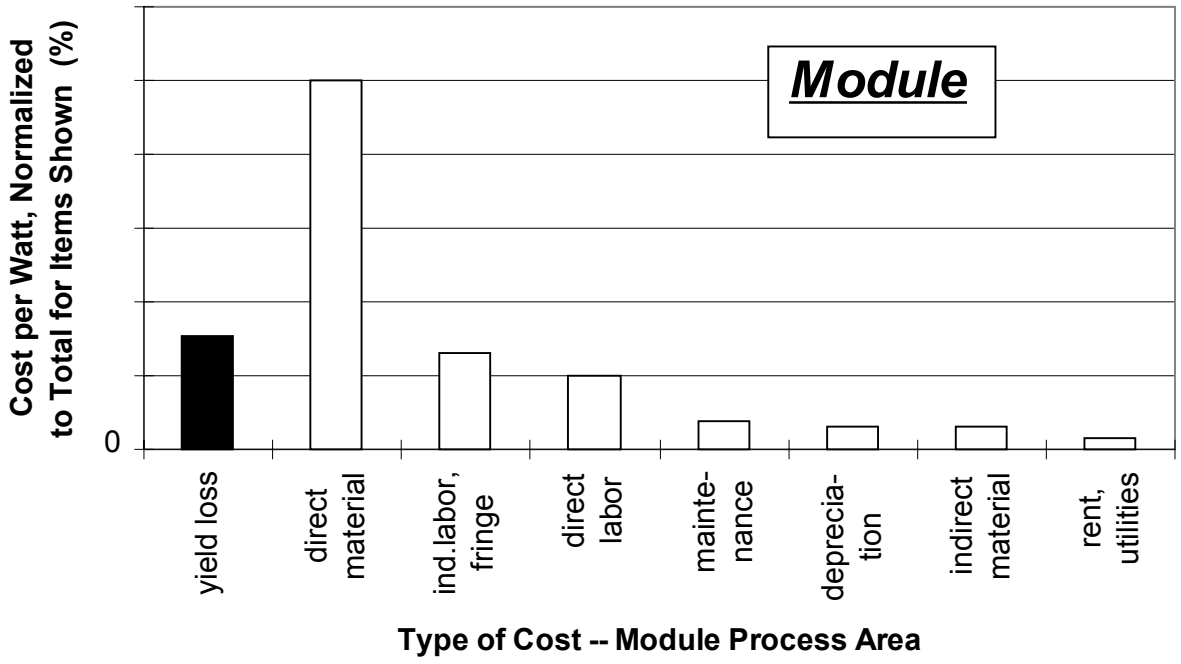

Figure 6. Module manufacturing costs per module watt for the case of 100% yield, showing the large contribution of direct materials, and the cost/watt of module yield loss.

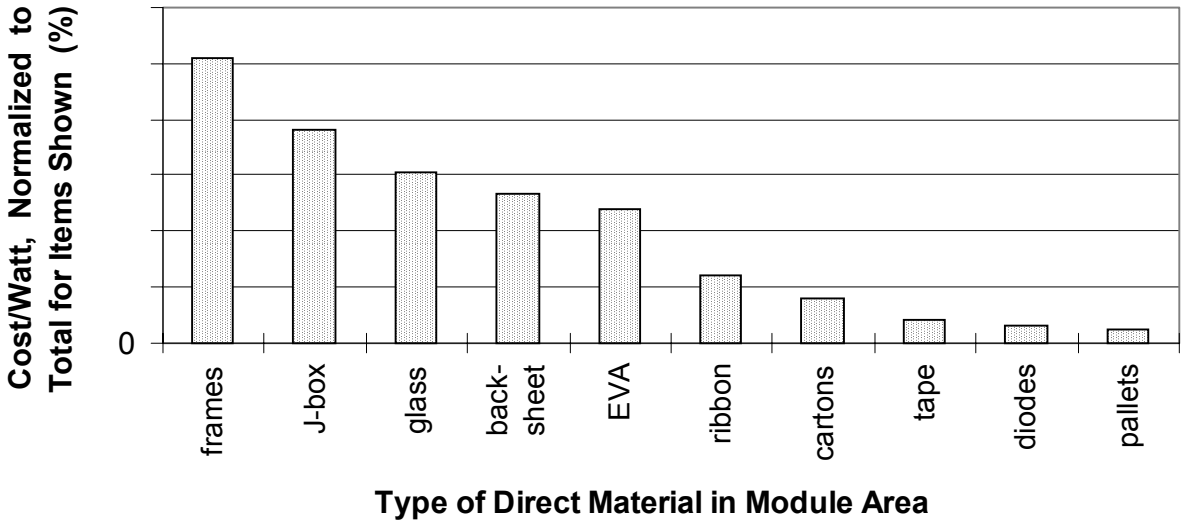

Figure 7. Cost/watt for direct material in the module fabrication area.

Resolving the detail in the module direct material costs, we see in Figure 7 that there are many contributors, but that the frames and junction boxes are the greatest module direct material costs. The next three largest cost components are proportional to the area of the module: glass, backsheet, and the ethylene vinyl acetate (EVA) sheets used to encapsulate the cells. Since the two direct materials with the largest cost, frames and junction boxes, do not scale with the module area, their contribution to module cost per watt can be reduced by increasing module size as described in the next section and by changing their fundamental designs.

Solutions to Module Cost

Methods for reducing the cost per watt at the module level can be divided into at least three categories of reductions in: the cost of cells that go into the modules, the cost of module direct materials, and the cost of module manufacturing labor. Starting with the cost of cells, a principle used to great advantage in the integrated circuit industry is to increase the substrate size, thus producing a greater amount of the desired output (watts for solar cells) for each part processed. Another lesson from integrated circuit fabrication lines, as well as other types of manufacturing, is that yield is tremendously leveraging, particularly in processes with as many steps as there are between silicon feedstock and finished photovoltaic modules.

Several other issues are important for reducing cell cost. The cell shape should conform to the ingot in order to make the best use of the grown silicon. For Cz Si, this promotes round substrates. Decreasing cell material usage is a straightforward way to reduce cell costs, e.g., through the use of thinner wafers. Increasing the cell power, e.g., by reducing resistive losses, lowers the $/W by increasing the denominator of this ratio.

The themes of using larger cells and increasing yield are quite general and apply to modules as well. With regard to the cost of module direct materials, increasing the module size lowers the perimeter-to-area ratio, thus reducing the $/W contribution of the frames. Similarly, the cost of junction boxes can be spread out over a greater wattage by using larger modules. Simply finding less expensive materials and vendors for frames and junction boxes is always a valid method for reducing cost. The use of glass,

backsheet, and EVA scale with the module area. As always, yield is highly leveraging for reducing direct materials costs.

For manufacturing direct labor, increased module size reduces the $/W of all processing steps whose costs scale with the number of parts processed rather than with the module area. Automated assembly, e.g., the Spire automatic soldering equipment developed under another PVMaT subcontract, and semi-automated fixturing is important for managing the costs of a labor-intensive process like module fabrication. Once again, maintaining high yield is necessary for maximizing operator productivity and holding manufacturing labor costs low.

All of the above strategies for reducing the cost per watt of Cz Si photovoltaic modules have been employed during this contract.

Model of Cost-per-Watt Dependence on Module Size

Based on the observation that many module material and labor costs do not increase as rapidly as the module area when the module is made larger, a model was developed to quantify these cost savings available through module design. Costs of the component materials and of the module fabrication labor were plugged into the model to calculate the cost per watt as a function of module size. This allows the module designer to see clearly at which point it is advantageous to increase module size, and at which point further size increases have diminishing returns. This analysis separates the benefits of increasing module size from the further benefits achievable with increased cell size and cell shape matched to the ingot cross section.

The module direct materials and direct labor components can be divided into three categories: costs which are proportional to the module area; costs which vary with the linear dimensions of the module; and costs which are constant with respect to module size. The model described here uses module aspect ratio (γ = module length/module width) as a parameter, so that in terms of the module width w, module length is γw, the perimeter length is $2(1 + \gamma)w$, and module area is γw^2 .

Most photovoltaic modules include some inactive region around the module perimeter made up of the lamination materials without cells, to provide room for the circuit layout or for the framing scheme. The cost of the lamination materials used in this perimeter region scales with the length of the perimeter, since the width of the perimeter region is approximately constant with respect to module size. The size, shape, and spacing between cells in the module define a unit cell of module area. The area of this unit cell times the number of cells gives the area of the active region of the module, as opposed to the perimeter region. The module area, width, and length discussed above refer to the dimensions of this active region. The cost of lamination materials (glass, backsheet, and EVA) required to cover the active region of the module increases proportionally to module power as the module is made larger, and so increasing the module size does not affect this component of the cost/watt. Similarly, in this treatment with constant cell size, the costs of cell interconnect ribbon and solder are also proportional to the area of the active region, and therefore to the module power.

Module direct material costs which scale with the linear dimensions of the module are: the lamination materials in the perimeter region discussed above; the circuit busbars used to connect series strings of tabbed cells; the sealant material around the laminate perimeter; and the module frames. Since the cost of these items increases more slowly than the module area and the module power, larger modules will tend to decrease the contribution of these items to the cost per watt. Based on purchase price data, the cost of frames has a component which is proportional to length, and a component which is constant with

respect to length. Finally, the junction box (including diodes, sealant, etc.), material used for circuit busbar isolation near the junction box, and the module label are independent of module size, so that an increase in module size has the greatest impact on these components of the cost/watt.

For the direct labor required to make modules from cells, the module fabrication sequence was divided into two major portions: 1) soldering cells into strings; and 2) assembling the module circuit from cell strings, lamination, and module finishing operations such as framing and testing. When considering a change in module size while keeping cell size constant, larger modules require that the number of cells to be soldered be increased in proportion to the module area. The cost of direct labor is assumed to be a constant times the length of soldered cell strings required, and for constant cell width, the length of strings is proportional to the area of the module. So the cost of direct labor required for cell stringing scales with the module area in this model, and therefore there are no reductions in soldering direct labor cost/watt as a result of increasing module size only. Note that if cell size is increased, then the cell width is larger, and more soldered cell area is gained per unit length of string soldered. So for an increase in cell size, the cost/watt of soldering is decreased.

For the remainder of the module fabrication process (circuit assembly, lamination, and module finishing), it is probably too optimistic to assume that the direct labor costs will be proportional to the number of modules handled, regardless of the module size. However, many direct labor costs increase more slowly than the module area as the module size increases. As an approximation, the direct labor costs in this area are taken to be proportional to the linear dimensions of the module, which increase more slowly than the area. When considering such operations as soldering tabbed cell strings to the circuit bus bars, attaching the module frames, or transporting modules down a linear assembly line, this approximation of linear dependence on module dimensions seems plausible.

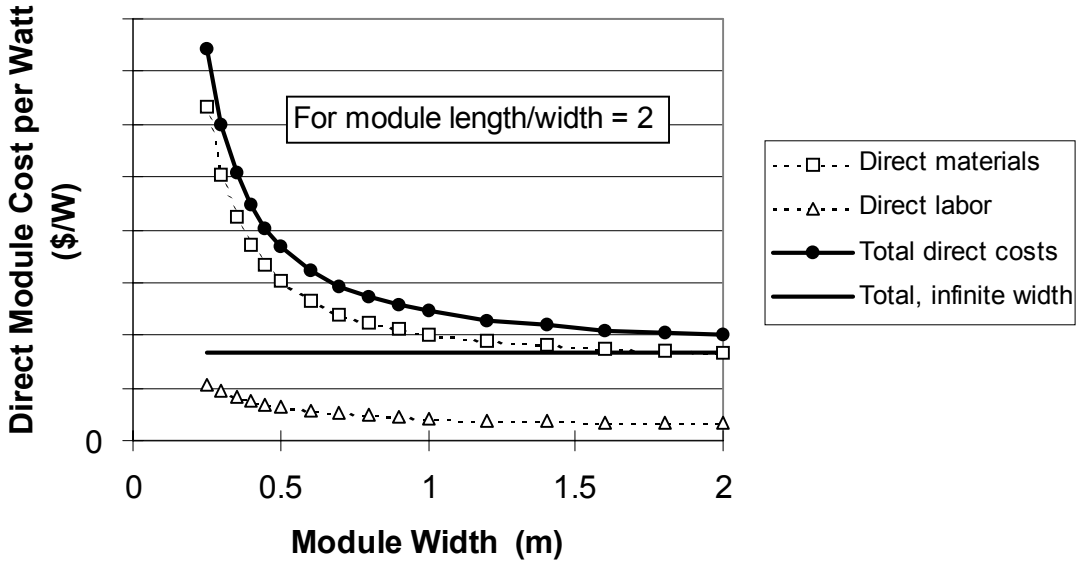

Figure 8. Dependence of module direct material costs and direct labor costs, for a module aspect ratio of 2, and the assumptions described in the text.

Figure 8 shows the dependence of direct materials and direct labor costs on the module width, calculated according to the guidelines described above, for a module aspect ratio of length/width = 2. Other aspect ratios can be readily plugged into the model. The total direct cost/watt in the module area decreases rapidly as the module width is increased from ~0.25 to 0.5 m, undergoes a gradual decline from about 0.5 to 1.0 m, and changes only slowly for larger module widths. The asymptotic value of the module direct cost/watt as the module width becomes infinite is also shown on the graph. SSI modules are evolving from a width of ~0.33 m to nearly 0.6 m, primarily due to the issues represented by the above model.

Specific Module Designs

The strategy of building larger modules with the same size cell was used in manufacturing during Phase I of this contract. Figure 9 shows a schematic of an SM110 module with 72 103-mm semi-square cells, rather than the more usual 36. This type of laminate began production in the SSI Camarillo plant in August 1996. The larger module size and power (110 W) lower the $/W components from the frames, junction box, module manufacturing labor, etc., resulting in a 4% reduction in module $/W relative to 36-cell modules.

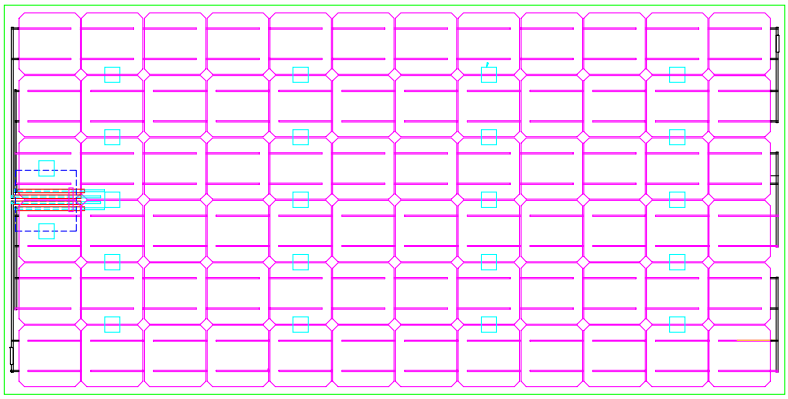

Figure 9. SM110 module with 72 103-mm semi-square cells reduces $/W contribution of the frames and the junction box.

Figure 10 shows a new module configuration that uses 150-mm round cells in a 36-cell package. Prototypes of this module have been built during Phase I of this contract and shipped to NREL. Much of the effort to reduce the cost/watt at the module level in Phase II focuses on the implementation a new product line based on 150-mm round cells in production. The cost per watt is significantly lower for this type of module for a variety of reasons. The larger cell substrates used translate to an increase in surface area per wire saw run, and a reduction of wafer handling and cell fabrication equipment costs per watt for a given MW/year production level. The round shape of the 150-mm cell makes more efficient use of the Cz ingot by eliminating slabbing of the ingot. As described above, the large module size also means that module direct materials, module direct labor, and equipment costs per watt will be reduced for a given MW/year production level.

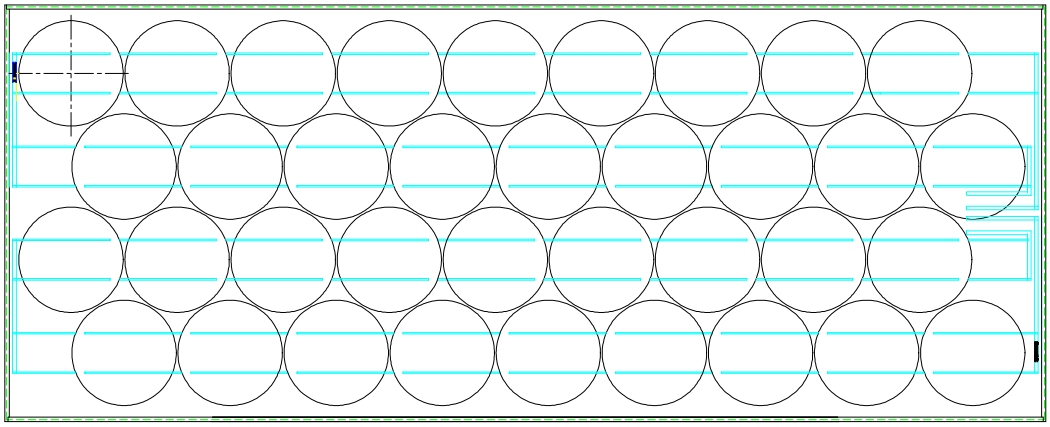

Figure 10. Large-area SR100 prototype module using 150-mm-diameter cells has a reduced cell contribution to $/W, as well as reduced frame and junction box $/W components.

Specific Improvements in Material Procurement and Utilization

A straightforward and highly effective way to reduce the module cost per watt is through improved design or manufacturing of the component parts. Another clear but often overlooked form of cost/watt savings is through improved vendor relationships which allow greater efficiency for both the vendor and the photovoltaics manufacturer, *e.g.*, fewer defective parts, streamlined return policy, lowered need for receiving inspection of component materials, reduced work in procress (WIP), etc.

As a result of consolidating SSI Cz crystal growth operations in the Vancouver, WA facility, electricity costs for Si ingot production were sharply reduced in Phase I. The energy-intensive process of Cz Si ingot growth had been split between the Vancouver, WA site, and Camarillo, CA, where the price of a kWhr from the electric utility is much higher than in the Pacific Northwest. Consolidation of the crystal growing operations in Vancouver was completed in early 1996.

Due to the polysilicon feedstock shortage that impacted the Si photovoltaics industry during Phase I, both the cost of feedstock and the availability of normal types of feedstock were adversely affected. Using alternative forms of feedstock when more traditional types were no longer available increased costs through greater crystal growing yield loss, since the procedures for growing with the different feedstock types had not yet been developed. Boron dopant schedules were developed to expand the usable range of Si feedstock to either p- or n-type with resistivity greater 1 Ωcm. Procedures were also developed to use small pieces of Si feedstock in the mm size range, rather than the preferred size of several cm. These measures helped to hold the cost increases in crystal growing due to the Si feedstock shortage to a lower level than they would otherwise have been. Studies of feedstock material type vs. yield are described later in this report.

In the wafering area, cost reductions resulted from the implemention of lower-cost wafer cleaning solvent in production, development of improved solvent recovery by distillation, and design and construction of a water-based scrubber for the exhaust from an acetic acid solution. In addition, a thinner wire process was

developed which drastically reduces the ingot loss to kerf, while improving yields due to reduced wafer taper.

Analysis of the power lost due to resistance in the back screen-printed metallization and comparison to the cost of the back paste led to a reoptimization of the back metallization pattern. The previous back pattern used too little metal paste, and so although paste direct material costs were held low, the power lost in the back metal resistance was high, resulting in a higher cost/watt than necessary. Calculating the optimum grid line spacing, width, and grid line taper options results in significantly lower cost/watt for both 103-mm and 125-mm cells. A back metallization pattern with higher coverage fraction on 125-mm cells was implemented in production in May 1996. Although the amount spent on back metal paste is greater with the new pattern, the module power is greater by 1.5 Watts translating to a net reduction in module cost/watt.

Working with interconnect ribbon manufacturers led to the use of ribbon formed by rolled wire, which resulted in a 25% cost reduction for ribbon, and fewer rejects. Negotiations with our glass vendor resulted in a new set of glass specifications which reflect the vendor's process capability, a formalized procedure by which to return defective material, and a 5% reduction in glass cost.

Module Design and Manufacturing for Lower Cost

As described in the previous sections, Module Assembly costs, from soldered cells to finished boxed modules represented the largest contribution to total dollar per watt in the four major categories of cost. Figure 11 shows this relationship again as a simple bar chart. The work on design and manufacturing changes to address these costs are discussed specifically in this section.

The first step to cost reduction involved yield improvement to fully reduce the costs associated with manufacturing processing. Figure 7 and Figure 7 show the yield of soldering, lamination and module processing combined over Phase I and Phase II timeframes. Figure 7 shows the 103 mm (M line) product results, and Figure 7 shows the 125 mm (P line) product results. These figures show a raising and stabilizing of yields to ensure the lowest cost contribution to module dollar per watt.

The second area worked to reduce the contribution to dollar per watt in the module area has been to deploy more watts in a module through a larger cell design. Figure 7 shows the SR100 module which has been produced in small scale production during Phase II of the contract. By the use of thirty six (36) large cells, 100 watts is produced, using virtually the same labor and equipment as thirty six smaller cells. The module assembly labor is also leveraged with this design as the assembly and lamination of these larger cells using the Spire solder machine is comparable to the labor used in both SM55 and SP75 modules produced at Siemens Solar. An SM55 and SP75 module shown in Figure 7 and Figure 7 respectively require approximately the same labor on the stringing level as the SR100 module shown in Figure 7 The layup and lamination labor is size related with the SM55 module requiring 10% less labor than an SP75 module and approximately 25% less labor than an SR100. This labor is a small contributor to the overall dollars per watt. With the module framing and j-box labor comparable on all three designs, the SR100 has the least cost per watt on the module level.

A new junction box design that features greater versatility for photovoltaic module users and lower cost entered production for this SR100. A schematic of this new junction box, called the PowerMax J-box, is shown in Figure 7. The bypass diodes are pre-assembled in this junction box, allowing logistics savings

and increased productivity. The lower cost of this J-box translates to a savings of 0.05 $/W for present module sizes.

The third area which was focused on during Phase II and III of the contract was in the reduction of module cost components. Figure 18 shows the cost/watt for direct material in the module fabrication area, with frames and j-boxes contributing over 50% to the materials totals. During Phase II of the contract, a new SR50-Z module was designed and produced in small scale which further reduced the junction box and frames costs. The new SR50-Z module is shown in Figure 19, with the j-box and frame shown in Figure 20 and 21 respectively. The new junction box for the SR50-Z allows for ease of installation and a cost savings of over 50% per j-box per module. The new frame design eliminates end caps, screws and taping when compared to the traditional SSI module designs and saves over 25% in the framing cost of modules. The overall reduction in $/W total module cost is 17% with the SR50-Z design when compared to SSI's standard M55 module.

The combination of yield improvement in the module area, larger cells and watts in a module, and the new framing and junction box, allowed for a greater than 17% cost per watt advantage, coming close to the 18% contract goal.

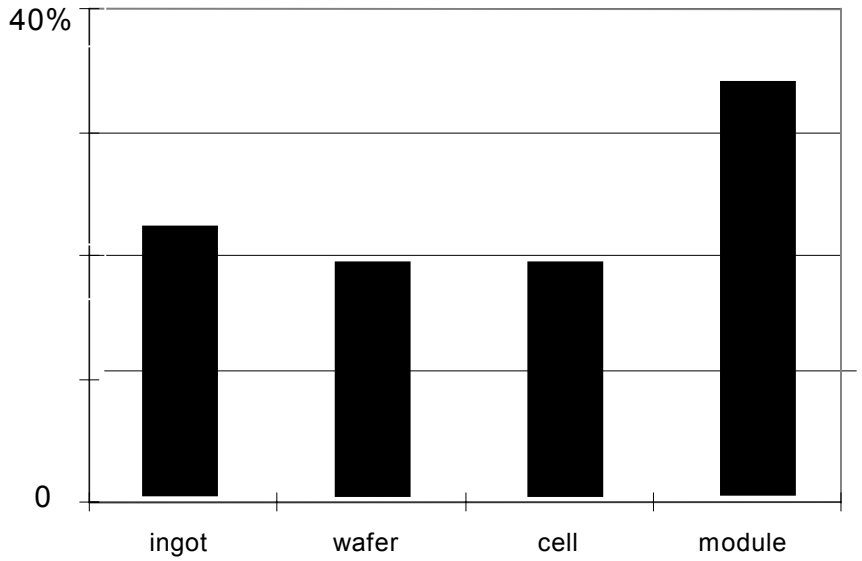

Figure 11. Cost per Watt

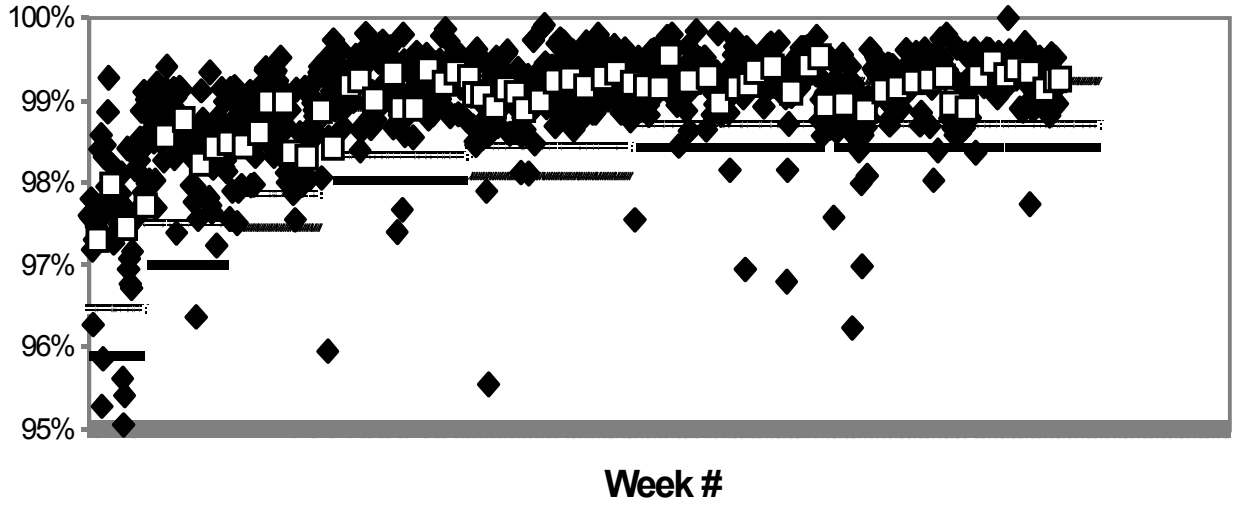

Figure 12. Module Yield for M-line

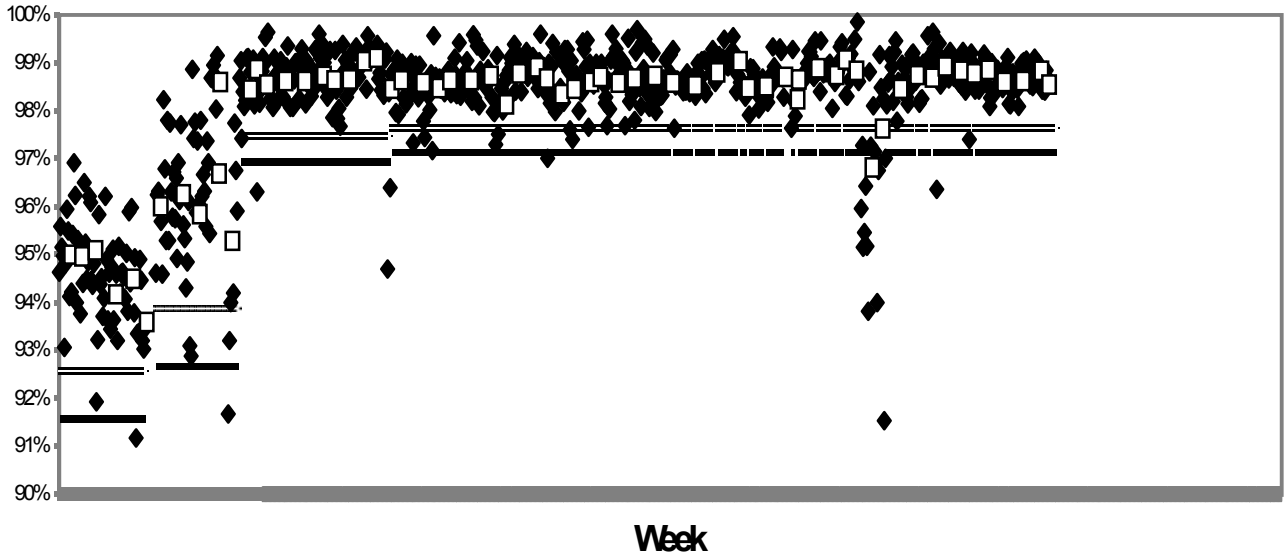

Figure 13. Module Yield for P-line

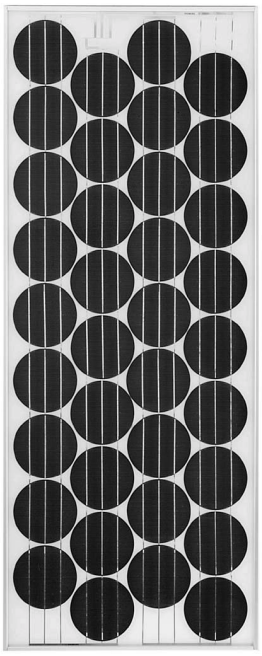

Figure 14. SR100 Module with 150mm cells

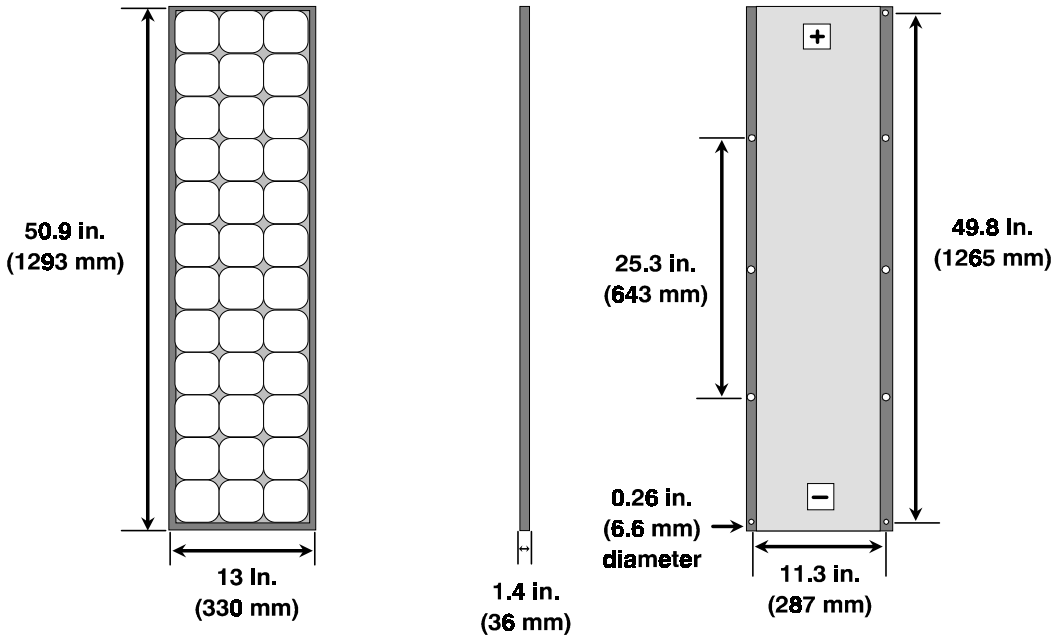

Figure 15. SM55 Module

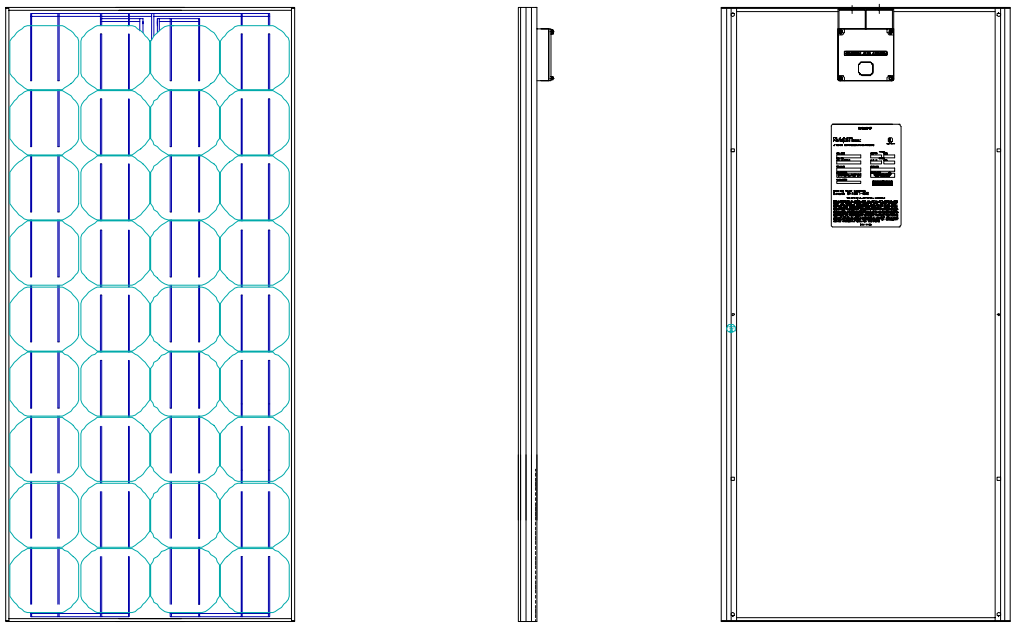

Figure 16. SP75 Module

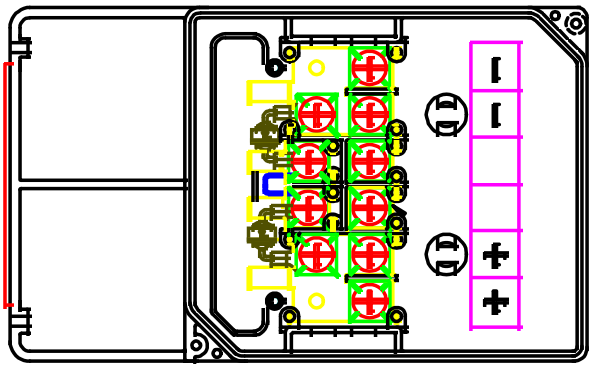

Figure 17. Schematic of new junction box combining improved flexibility of use and lower cost per module for SR100.

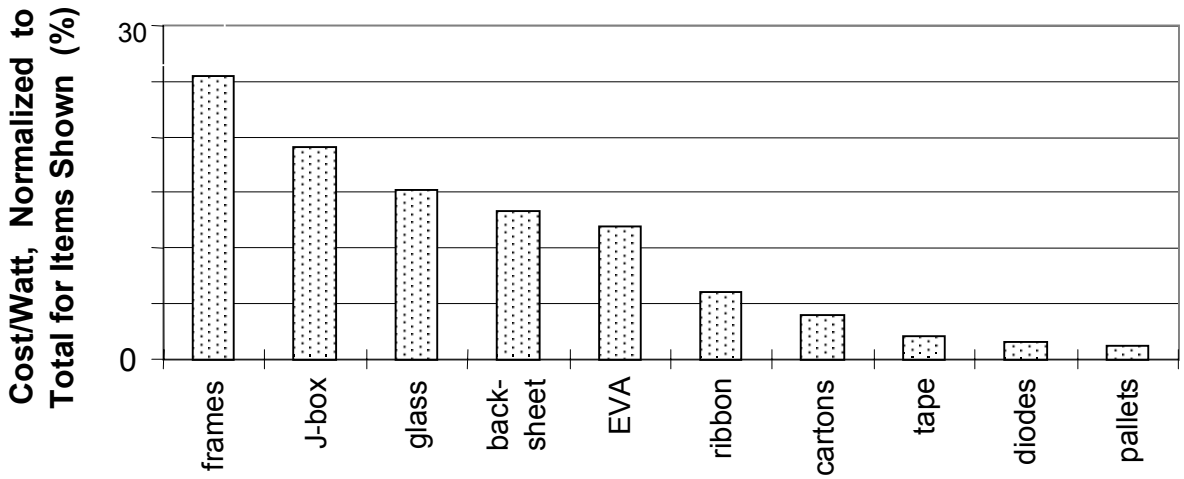

Figure 18. Direct Material Contribution in Module

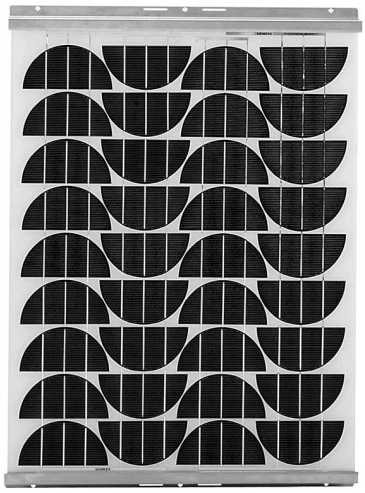

Figure 19. SR50-Z Module

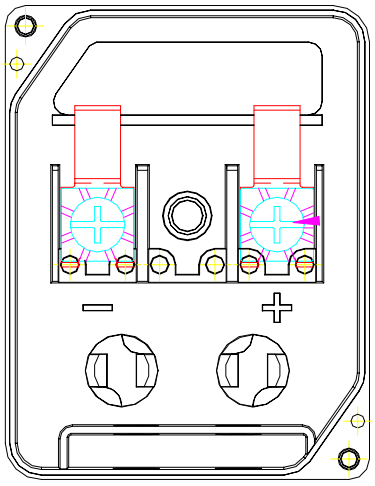

Figure 20. New Junction box for SR50-Z

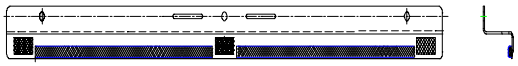

Figure 21. SR50-Z Frame

Yield and Productivity Improvements

Types of Yield Loss

In the discussion of cost in a previous section, yield was found to impact nearly all types of potential cost reductions. Figure 22 plots the relative yield loss for the three process areas of wafering, cell fabrication, and module fabrication. Yield loss in the ingot fabrication area is not included in this chart, it is covered in a separate section on crystal growth yield improvements. The contribution of ingot yield loss to the overall cost/watt can be seen in Figure 2. Among the three process areas considered in Figure 22, the yield losses for the wafer and cell areas are the highest. However, a given yield loss in the module fabrication area is especially costly due to the high cost per watt at this final point in the process. In Figure 23, the various types of yield loss in the line are plotted. Mechanical breakage is clearly the dominant type of defect causing yield loss. Accordingly, most efforts at improving the yield have been aimed at reducing mechanical breakage.

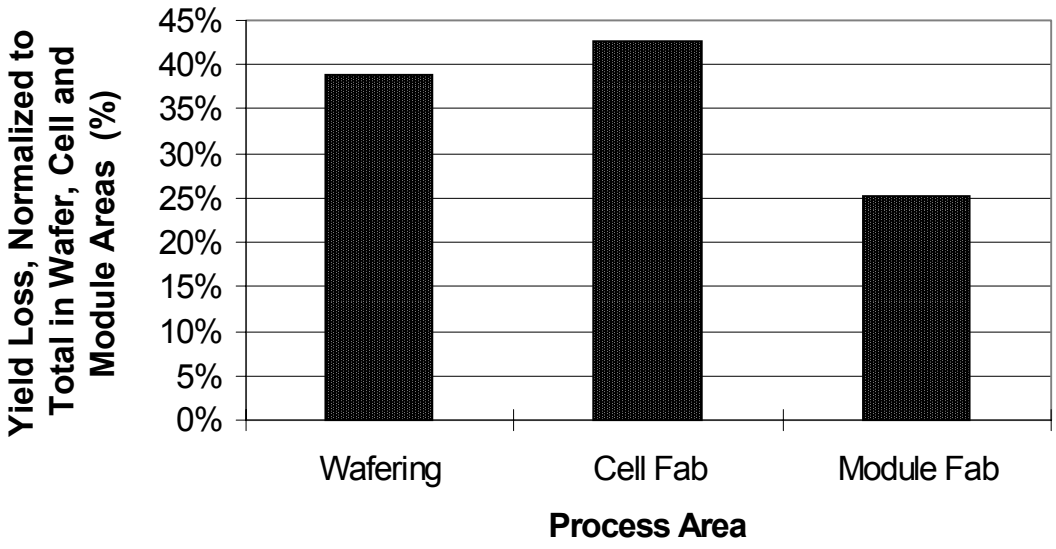

Figure 22. Yield loss by process area. Due to the value added at each step in the process, yield loss in the module area is especially costly.

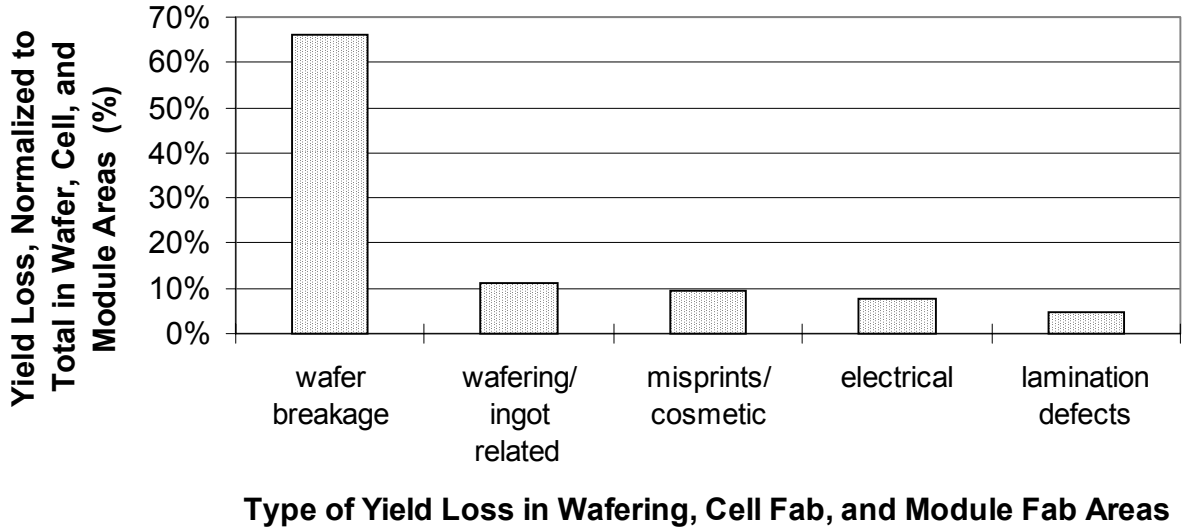

Figure 23. Yield loss by type of defect. Wafer breakage is by far the dominant loss mechanism for the wafering, cell fabrication, and module fabrication areas.

Breakage Force Studies

In order to provide more information about the root causes of wafer breakage, the average breakage force of wafers was measured by a stylus lowered at a controlled rate in the center of the wafer resting on two horizontal rails. The force required to break wafers in this configuration was measured for multicrystalline-Si (mc-Si) wafers and for single-crystal SSI Cz wafers, at 6 different points in the cell fabrication sequence, from as-sawn wafers to finished cells. Although standard SSI Si solar cells are single-crystal Cz, mc-Si wafers were evaluated for comparison. The data is shown in Figure 24. Each bar represents the average of breakage force measurements on 25 wafers, except for after Step 4, where the data set was only 10 wafers. The error bars indicate ± one standard deviation. These breakage force measurements may not highlight precisely the same mechanisms that cause breakage in the manufacturing line, but do provide a relative measure of wafer strength that can indicate major effects of wafer processing, and of different silicon materials.

Throughout the cell process, the breakage force of mc-Si is fairly similar to that of single-crystal SSI Cz. As sawn, the wafers are 50-60% weaker than after texture etching (after Step 1), and the mode of breakage is qualitatively different for the single-crystal Cz. Before etching, the Cz wafers tend to cleave into quarters, while after etching the wafer shatters into a larger number of small pieces. One explanation is that microfractures or other irregularities on the as-sawn wafer surface can serve as nucleation sites for larger fractures when the wafer is stressed during the breakage force measurement. The fracture nucleation sites on the as-sawn wafer are likely to be removed or their density decreased by the wet etching solutions.

For most of the cell process after etching, the breakage force stays fairly constant within the experimental uncertainty. On printed and fired cells (after Steps 5-8), however, the average breakage force drops by ~35% for both types of material. This could be due to the surface imperfections caused by the metal contacts. It is interesting to note that for all of the process steps after wet etching, the standard deviation

of the breakage force measurements was higher for the mc-Si wafers than for single-crystal SSI Cz, perhaps due to the variation in crystal orientation in mc-Si.

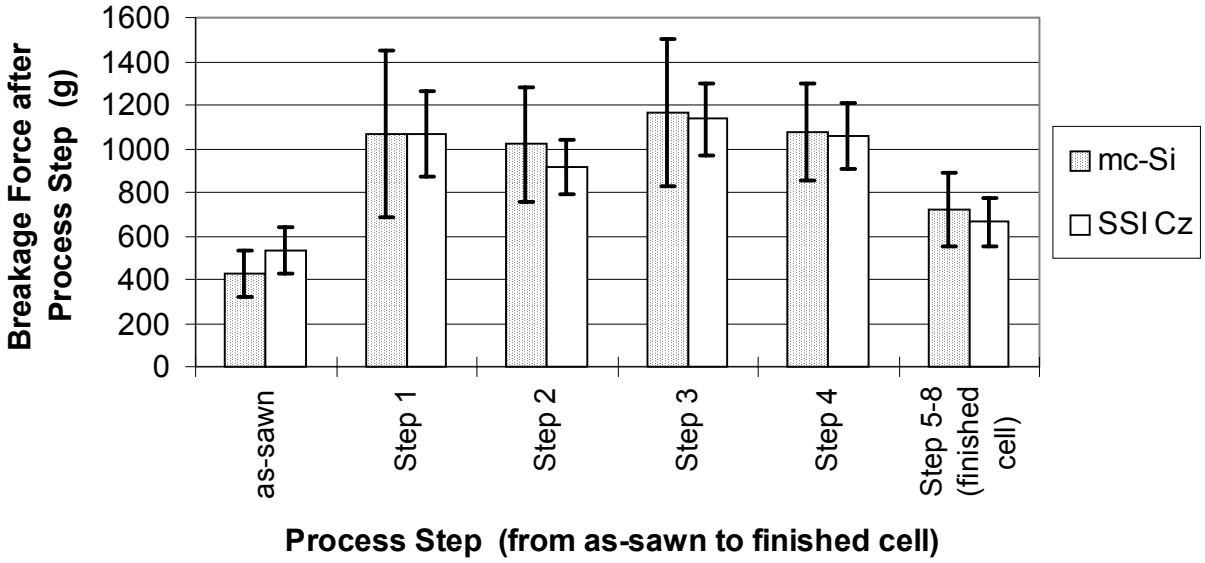

Figure 24. Wafer breakage force of multicrystalline-Si (mc-Si) and SSI CZ Si, as measured by a stylus for wafers resting on two horizontal rails. The error bars indicate ± 1 standard deviation in the data.

Mechanical Yield Experiments

The mechanical yield and electrical performance of multicrystalline-Si (mc-Si) substrates through the SSI cell fabrication line were also measured in order to evaluate the use of mc-Si wafers in addition to or instead of the single-crystal Cz Si normally used at SSI. Multicrystalline-Si ingots from two vendors (A and B) were wire sawn at SSI. A standard format for tracking mechanical yield was developed, in which the wafer breakage is recorded at 43 steps in the cell process to identify problem areas, for both the type of wafer under test and for standard SSI Cz Si processed at the same time. The number of wafers in each group is 875 at the start of cell processing.

Figure 25 shows the mechanical yield for mc-Si from Vendor A, lumped into 8 major process areas from as-sawn wafers to finished cells. The overall mechanical yield through SSI cell processing in this experiment was 92.0 % for the mc-Si, compared to 99.0 % for standard 103-mm SSI Cz wafers. The low yield for mc-Si in this run is attributable in part to an improper fit of the square mc-Si wafers in the wafer carriers in diffusion, as noted for Step 2 in Figure 25. For Steps 4, 6, and 7, the mechanical yields were somewhat lower than for SSI Cz. Factors contributing to this lower yield could be damage at the corners of the mc-Si from contacting the wafer carriers in diffusion, the square shape of the wafers causing problems at other wafer handling steps, or an intrinsic difference in the susceptibility of this type of mc-Si to breakage in the SSI line compared to SSI Cz.

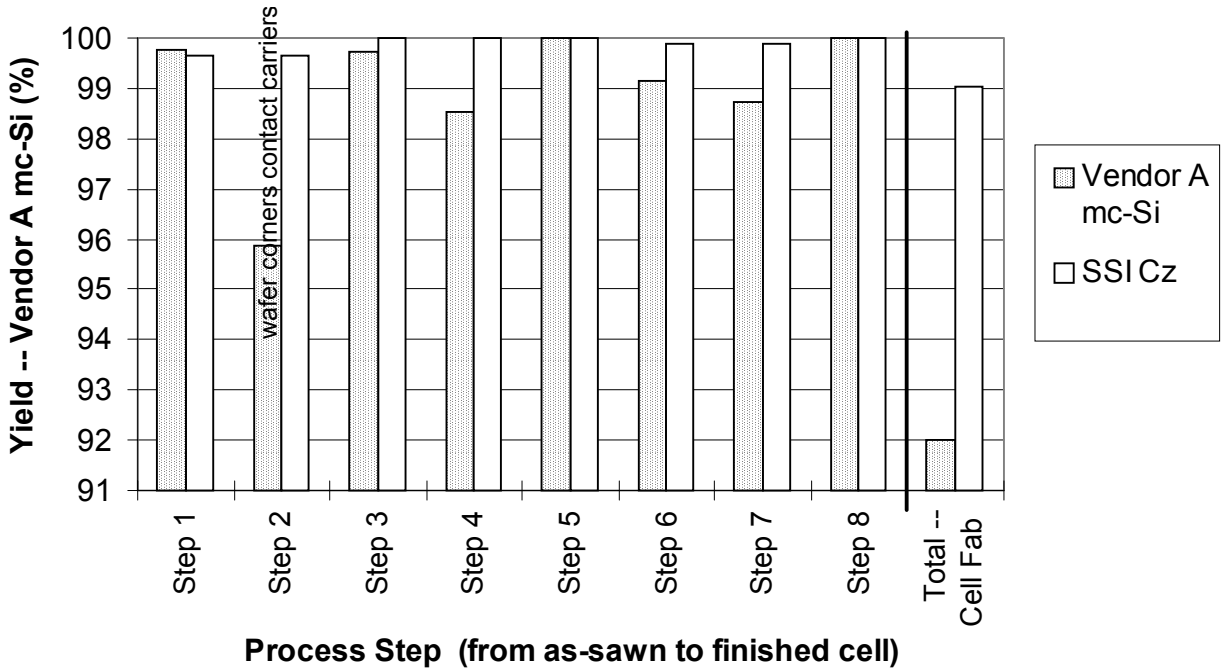

Figure 25. Mechanical yield of multicrystalline-Si (mc-Si) afers from Vendor A, in SSI cell fabrication process.

These mc-Si cells from Vendor A ingot were assembled into strings for module fabrication on an automatic soldering machine, and the yield was tracked in a similar way. Mechanical yield was 99.8% for the mc-Si and 99.3% for SSI Cz. For the SSI Cz, all breakage occured during the thermal and mechanical stress at the time of soldering, while for the mc-Si, no breakage occured during the actual soldering.

The mechanical yield of mc-Si from another vendor (Vendor B) was also tracked through SSI processing in the same way, as shown in Figure 26. The largest difference between mc-Si from vendor B and SSI Cz was in back printing and firing area (Step 7), with breakage of 1.3 % for the mc-Si and 0.0% for standard SSI Cz. Breakage in Step 2 was lower for the mc-Si than for SSI Cz. New wafer carriers designed to clear the square corners of the mc-Si wafers were used in this run. Overall mechanical yield for the cell fabrication process at SSI was 96.7 % for mc-Si from Vendor B and 98.2 % for SSI Cz in this test.

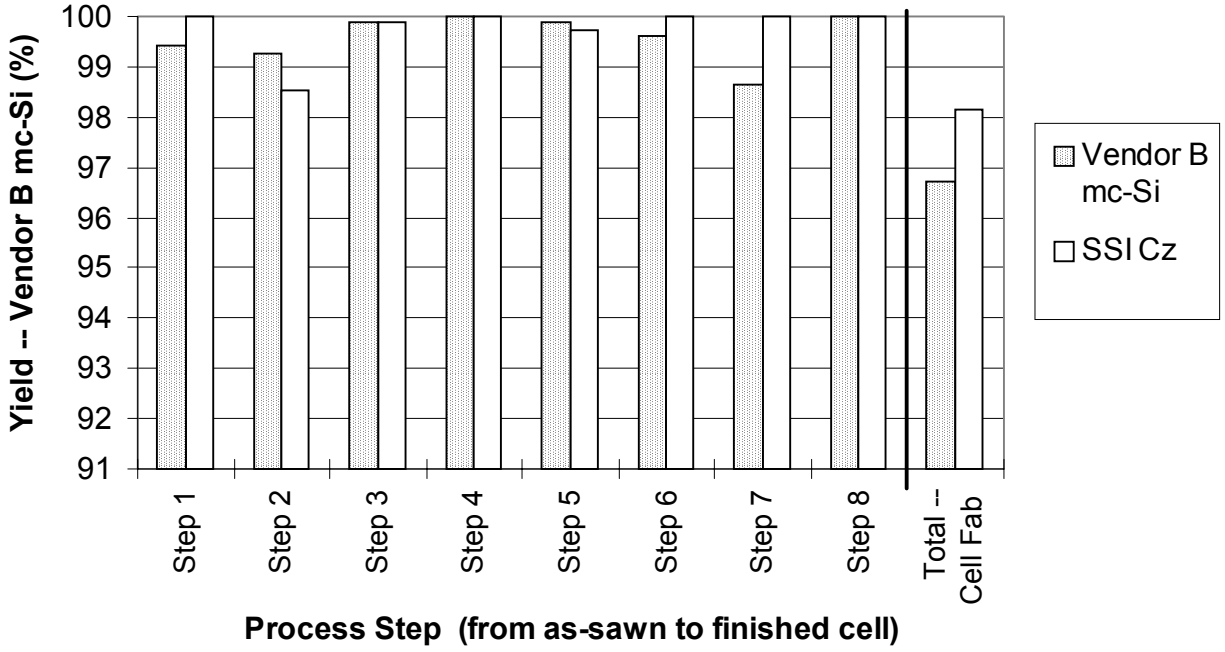

Figure 26. Mechanical yield of multicrystalline-Si (mc-Si) wafers from Vendor B, in SSI cell fabrication process.

Figure 27 shows the cell electrical distribution for mc-Si from Vendors A and B, and for SSI Cz in these experiments. The cells are binned according to I_{vr} , defined to be the cell current at a rated voltage of 0.484 V. The cell performance for both mc-Si materials is similar, with an electrical distribution much lower than that of the single-crystal Cz substrates. The SSI cell process is not optimized for mc-Si, so it is possible that this electrical performance could be improved by tuning some of the fabrication processes for mc-Si. Figure 28 shows the cell performance of the mc-Si relative to SSI Cz, broken down into the electrical parameters V_{oc} , I_{sc} , and FF, and the combination of these in the cell efficiency. The mc-Si shows low I_{sc} values of 83-85 % that of the SSI Cz, uncorrected for the larger area of the mc-Si cells (both mc-Si and SSI Cz were 103 × 103 mm substrates, but the SSI Cz wafers have rounded corners). Part of the current loss on mc-Si relative to SSI Cz results from the incomplete texturing on mc-Si, due to the random grain orientation, and part from the lower bulk lifetimes typically seen in mc-Si substrates. The mc-Si V_{oc} was 95-98 % that of SSI Cz, and the FF was 96-99 % of the average value for SSI Cz, resulting in cell efficiency of 77-80% that of the SSI Cz for the mc-Si evaluated in this experiment.

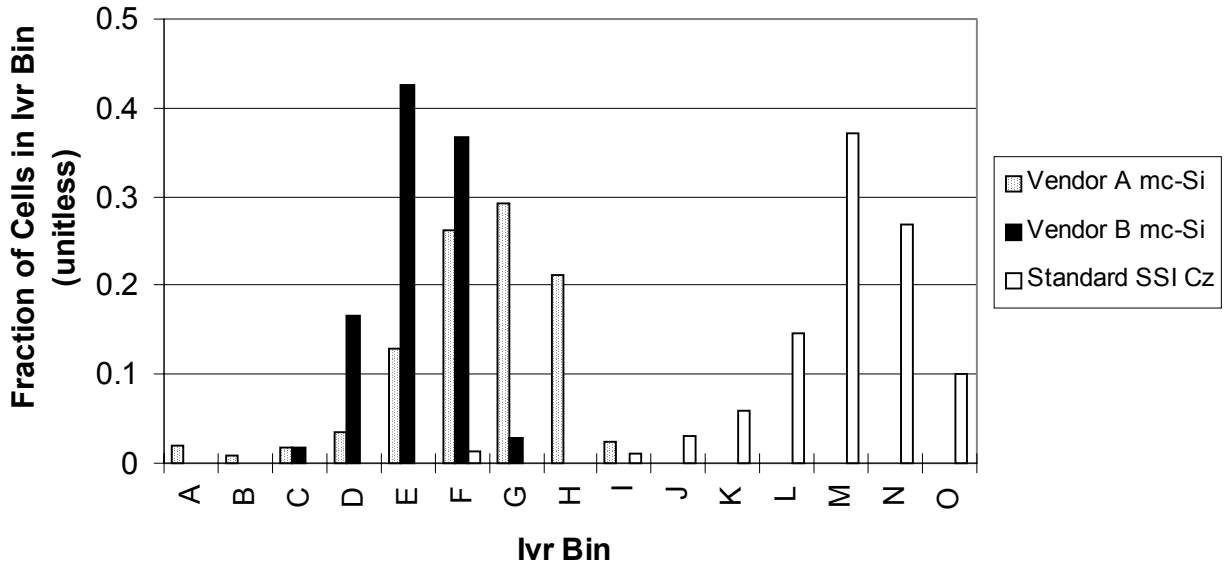

Figure 27. Electrical distribution for SSI Cz and mc-Si substrates. I_{vr} is the cell current at a rated voltage of 0.484 V, and is proportional to the cell power at that fixed voltage.

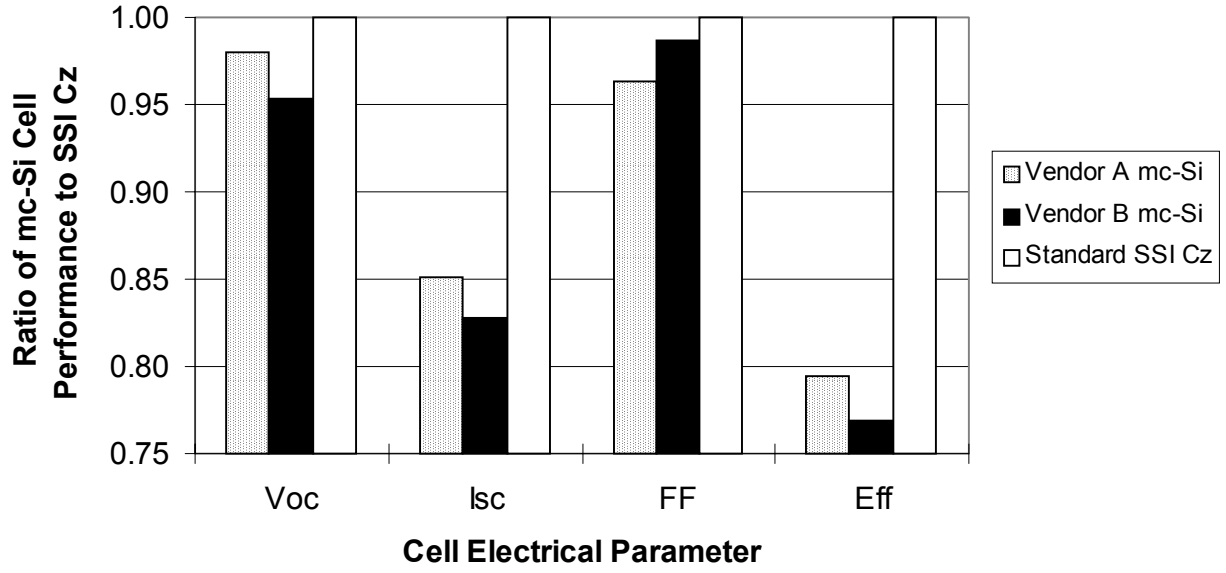

Figure 28. Comparison of cell electrical parameters for multicrystalline-Si and SSI Cz.

Specific Measures to Increase Yield

Wafering

Understanding of the factors which influence yield in wire sawing has increased considerably in Phase I. Sources of yield loss in wire sawing include: wire ruptures, ingot debonding from its support beam, out-of-spec average wafer thickness, excessive thickness variation across a wafer, chip formation on the wafer edge, wafer surface contamination, and, of course, wafer breakage after sawing.

A important capability for feedback to the wire saw process is rapid, accurate, multi-point measurement of thickness across a statistically significant number of wafers from each wire saw run. A new personal-computer-based wafer thickness gauge was introduced in the wafering area. Previously, after wafering an ingot, 25 wafers were selected from various positions throughout the ingot, and the thickness was measured with a manual gauge at five points on each of these wafers. The thickness values were typed individually into a spreadsheet program for data analysis. The new thickness gauge uses a capacitive method to measure thickness on five or more points across each wafer at once, and the data is automatically downloaded to a spreadsheet file. Wafer bow data can also be gathered with this instrument. The distribution of thickness values made with the manual gauge is not smooth and shows spikes in the data, presumably due to variation introduced by the operator. In contrast, the data from the automatic measurement system forms a smooth, gaussian distribution. The automatic data also showed a mean thickness that was 10 μm lower than the average of the manual measurments, possibly due to the broad platform for the wafer on the manual gauge, allowing wafer bow to influence the thickness measurement. A discrepancy of 10 μm in thickness is important to understand, as it impacts wafer strength and breakage through the rest of the process.

The rapidity of the thickness measurement is crucial in order to provide timely feedback to the wire saw operators. Based on the thickness measurements on a sample of wafers from each wire saw run, the probability of incidence of out-of-spec wafers, in terms of either average wafer thickness or thickness variation across the wafer, is calculated and available to the wire saw operator before beginning the next run. This allows the operator to be alerted to non-optimum conditions, and check saw parameters such as wire tension, change cutting slurry, or make other checks to correct the problem.

Feedback on the overall yield of each wire saw run due to all sources of loss, such as wafer breakage, wire rupture, chips, double-thickness wafers, etc. is also important for wire saw operators and engineers to make informed decisions. The parts-per-million loss due to each of these causes is quantified and charted for consecutive runs on each wire saw. The updated charts for each machine are posted daily in the wafering area, to quickly identify problem saws and detect trends in the yields.

A large source of process variation was traced to the silicon carbide abrasive obtained from various vendors for use in the cutting slurry. Analysis of the SiC particles indicates that the shape of the grains influences the uniformity and repoducibility of the wafer thickness. Significant increases in wafering yield were achieved by reducing the variability in the SiC particles associated with one of the vendors.

The epoxy used for mounting the ingots on a support beam was found to stress the ingots, if mixed improperly, resulting in increased wafer breakage. The previous blend of the two-part epoxy had excessive shrinkage, and stressed the ingot more than necessary. Adjusting the blend to result in less shrinkage and therefore less stress can result in long cure times, or in extreme cases, debonding of the ingot from the support beam. An optimum blend was found which has acceptable cure times, holds the ingot securely during cutting, and yet does not subject the ingot to excessive stress, resulting in reduced

wafer breakage. Bead blasting of the support beam was also developed to improve adhesion to the epoxy.

A critical step in wafer fabrication, which is often overlooked, is the cleaning of wafers after sawing. Failure to remove the cutting slurry residues after sawing can cause contamination of the downstream processes, visible surface nonuniformities on the wafer surface, and lower cell electrical output. A new automated wafer cleaning line was developed and installed in Phase I. In combination with the previous wafer cleaning line, the new cleaning machine can increase either the capacity or the thoroughness of the wafer cleaning process. Increasing the capacity of this step can be vital for maintaining high yield, because the slurry becomes extremely difficult to remove with any cleaning step if the wafers are allowed to sit in air for an extended period of time before cleaning. If the cleaning step is a bottleneck, then wafers can build up after boating before they can be cleaned. Another measure implemented to combat this problem is that a maximum of 10 wafer boats are allowed to be waiting after boating and before cleaning. A new method for removing the epoxy strips from the bottom of wafers was also developed and implemented in the automatic wafer cleaning line, resulting in fewer chips on the wafer edge.

Cell Fabrication

When the cell fabrication process steps at which wafer breakage occurs are categorized in terms of 1) machine handling, 2) operator handling, 3) thermal processes, and 4) other, most wafer breakage occurs during operator handling steps. This finding, in addition to the observation that wafers could be handled with greater deliberation and care at some steps, led us to address the issue of operator handling directly. Charts were posted in a prominent location and operators were trained to collect and plot the wafer breakage data at the end of each shift. This has heightened the operators' awareness of the magnitude of wafer breakage in the targeted area of cell fab process steps 1-4, and the effect that they can have on it. By having a frequent feedback mechanism by which the operators can gauge the effect of their efforts to handle wafers more carefully, they have achieved a significant increase in the average mechanical yield. The shift in the average breakage rate that occured in September 1996 when this feedback mechanism was strengthened is shown in Figure 29. The variation in breakage rate has also been tightened, as shown by the decrease in the upper control limit starting in September.

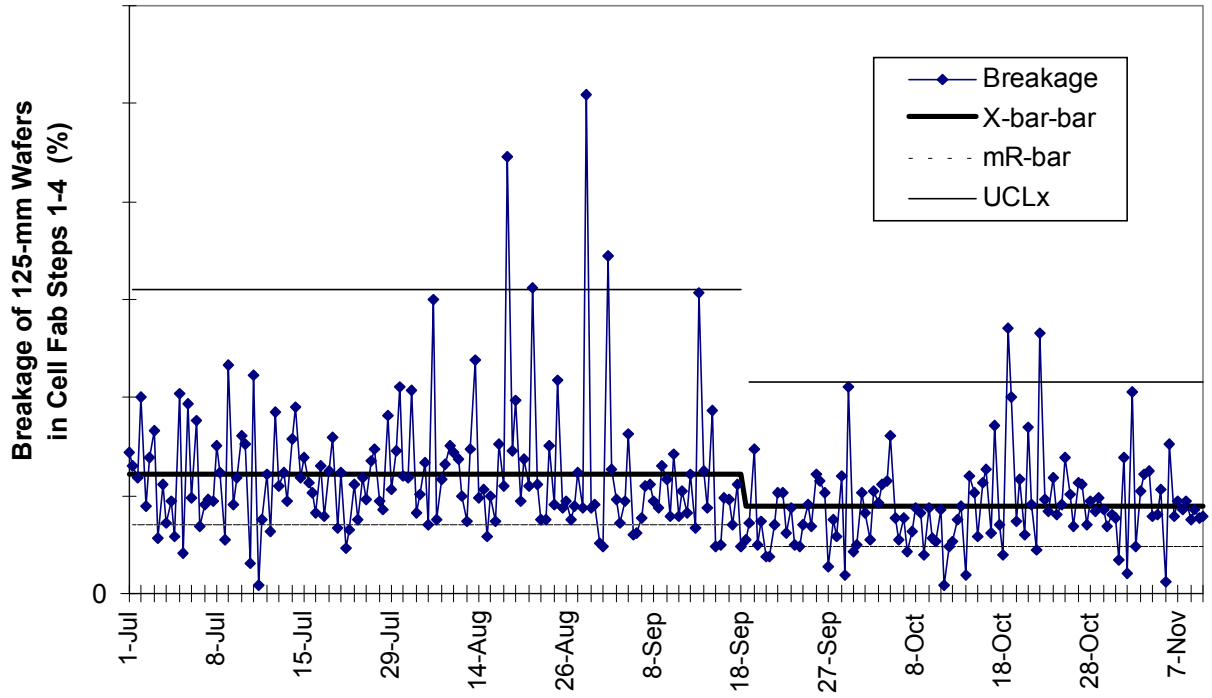

Figure 29. SPC chart of 125-mm wafer breakage in the first four process steps in cell fabrication. The downward jog in average breakage and range coincides with greater operator awareness of the breakage yield problem and greater visibility of the data, as described in the text.

Wafer edge chips constitute a serious type of defect that impacts the mechanical yield in cell fabrication. As discussed above, edge chips are grouped into two classifications: regular chips, which extend through the entire wafer, and; clamshell chips, which do not extend all the way through the wafer. Procedures and work instructions were established to eliminate regular chips at various points in the line, and treat them as a scrapped wafer, the way a broken wafer would be treated. Regular chips are eliminated from the product flow before the 2nd half of cell fabrication, which includes AR coating, front and back printing, contact firing, and cell testing. They are inspected for and removed again before the automatic cell soldering process.

Taking this yield loss early in the cell process has several benefits for yield:

1) A wafer with an edge chip that extends through the wafer is unlikely to make it through the rest of the cell fabrication, soldering, and lamination processes without cracking. This being the case, it is better to be rid of the wafer before more materials and labor are added to the cell, and even more importantly, before the cell has a chance to crack in a laminate, thus causing ~35 good cells to be scrapped along with it.

2) When a relatively large percentage of cells are breaking in automatic wafer handling equipment, such as the automatic soldering equipment and the multitude of wafer loaders and unloaders in the 2nd half of cell fabrication, broken pieces of wafer can cause an avalanche effect, causing the next, defect-free wafers coming through the machine to jam and break also. The productivity of the operators and of the equipment is also severely impacted, because of the need to frequently stop the process to clear the machine of broken wafers.

3) A more subtle effect of a high breakage rate through a piece of process equipment is that operators become acclimatized to poor yield conditions, treating it as the normal course of events. They are then less likely to investigate the root cause of the yield loss and take the steps neccessary to correct yield loss problems, even ones that can be easily remedied.

4) Eliminating regular chips before one process segment clearly allows one to determine how many chips come from upstream processes, and how many chips are generated in the process segment in question. The 2nd half of cell fabrication has numerous wafer stops used to align the cells for loading, unloading, printing, and testing equipment, which can cause edge chips themselves. When the rate of chip generation is made visible, steps can be taken to isolate the machine causing the chips, and realign it or find other means to fix the problem.

For these reasons, inspection and removal of regular chips before the 2nd half of cell fabrication and before automatic soldering has had a dramatic effect on the yield in those two process segments.

A machine vision system for inspecting wafers both before and after front contact printing was developed and installed. Before front print, the vision system can detect wafers with out-of-spec dimensions, such as a corner-to-corner diameter that is too small. Such wafers can cause metal to be printed on the edge of the wafer or on the metal cell chuck, causing yield loss. After front print the system can detect a wide variety of print defects, such as grid line voids, tears in the print screen, double prints, and misaligned prints. Having a machine perform this inspection is valuable for at least three reasons:

1) Immediate feedback on print defects is essential to catch the problem before many parts are ruined with a rejectable defect. The equipment configuration is such that it is difficult for the print operator to see a print problem until many wafers have gone through the printer.

2) Inspection by an operator is far from 100% accurate, due to fatigue, inattention, interpretation of reject criteria, etc. This allows the possibility that some rejectable cells would not be scrapped as they should be, and that conditions such as a screen tear could persist for many printing cycles, causing many cells to be scrapped needlessly.

3) Productivity of the print operator can be increased, since the vision system frees him or her to attend to the tasks associated with running the line other than inspection, to fill in for other operators absent or on breaks, etc.

A key process control point in the cell process is the contact sintering (firing) process after front and back screen printing. This is a dynamic process, which can cause the cell fill factor (FF) to vary from nearly zero up to its maximum values above 75%, through the strong dependence on firing time and temperature profiles. The definitive test of firing condition optimization is the cell fill factor that results. This is the method used in manufacturing to find the best firing temperature. Although this is a direct optimization method, it has a fairly long feedback time of 15 minutes or so, and requires some effort on the part of the operator. Because many factors can influence the optimum firing conditions, such as wafer thickness, furnace loading, ambient air temperature, lamp age, etc., the frequency of this firing temperature tuning was increased, and the data from sequential FF checks posted, resulting in tighter control over this key electrical parameter.

A problem area for wafer breakage during automatic wafer handling is at the station for unloading wafers from the contact firing furnace belt. Vibration of the belt tends to misalign wafers so that they do not descend smoothly down the lanes designed for unloading. Design and experimentation with adjustable lane guides, increased air jet pressure for low-friction transport down the unloader lanes, and measures to

reduce belt vibration have resulted in far less wafer jamming and breakage at this point. Operator productivity is also significantly improved, due to fewer events in which the back print operation must be left to fix a wafer jam in the belt unloader.

Module Fabrication

The foundation of yield improvements in the soldering area is development of accurate tracking and recording of breakage on the automatic cell soldering machines. This is the gauge by which the dependence of a process change on the yield can be measured under actual production conditions. Work instructions formalizing the methods for gathering and posting this data were completed in Phase I of this contract. An example of this yield chart is shown in the section on SPC, in Figure 48. Elimination of chipped wafers prior to soldering had a dramatic effect on yield in this step, through the reasons described above, such as fewer broken pieces in the machine that can break subsequent wafers, easier isolation of the root causes of the edge chips, etc. SPC charting of the yield in various parts of the machine show that the breakage in the lamp-heated zone, in which the cells are subjected to both thermal stress from non-uniform, rapidly changing temperatures, and mechanical stress from the rollers which hold the ribbons, is much greater than in the automatic wafer handling part of the system, in which the cells are picked from a stack and flipped in order to apply solder paste on front and back.

It was also found that the soldering machine yields are strongly dependent on machine setup parameters, such as alignments, roller pressure, lamp power, etc. A detailed troubleshooting list was developed, giving the operator a way to rectify many simple problems on the machines, without the delays and productivity loss associated with waiting for a maintenance technician. The SPC charting of yield provides the operator with an unambiguous way to tell that the machine is causing poor yield; the list of specific action plans for many commonly encountered yield problems offers a way to fix it. Operator training is an essential part of this approach, both to explain the technical aspects of setup and troubleshooting, and to build operator awareness of and greater responsibility for yield.

Finally, yield experiments and confirmation runs showed that the greater yield obtained with thicker 125-mm substrates (nominally 400 μm as opposed to the previous 325-μm thickness) outweighs the fewer number of the thicker wafers that can be cut from a given length of ingot. Standard production 125-mm wafers were switched to the greater thickness in Phase I, resulting in reduced breakage in wafering, cell fabrication, and soldering. 103-mm wafers did not show as strong an advantage for increased thickness, and so standard 103-mm wafers remained at the thinner 325 μm. With improvements to the wafer handling systems throughout the line, it is anticipated that wafer thickness can be reduced while maintaining high yield, but in the present manufacturing environment these thicknesses are close to optimum.

Overall Yield Improvement

Yield Improvements in the Cz Manufacturing line have been a focus at SSI starting with PVMat 2A. In increasing yield, all areas of cost reduction and productivity benefit. A summary of the yield efforts during the contract shows that the yields have improved at SSI over 25% absolute percentage points. The yield gains are shown in Figures 30 and 31 respectively for the M line and P line products over the time frame including PVMat 2A and 4A.

The M-line yield gain has been 25% over the start of the program and P-Line yield gain has been 40% relative to the 94/95 time frame.

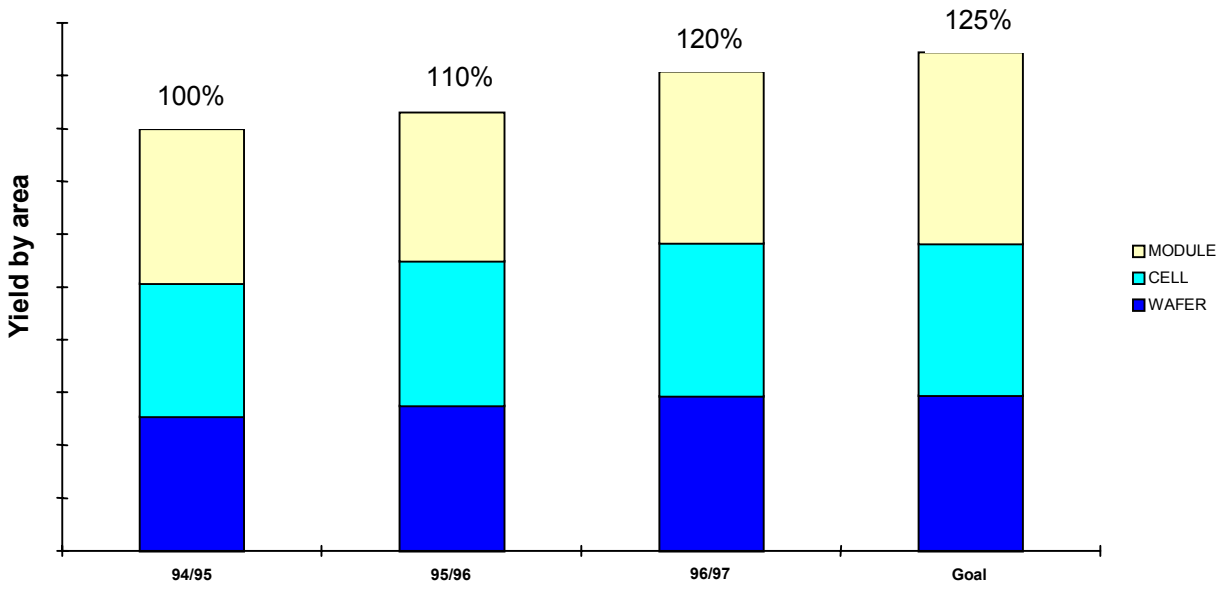

Figure 30. Yield on M-line Product

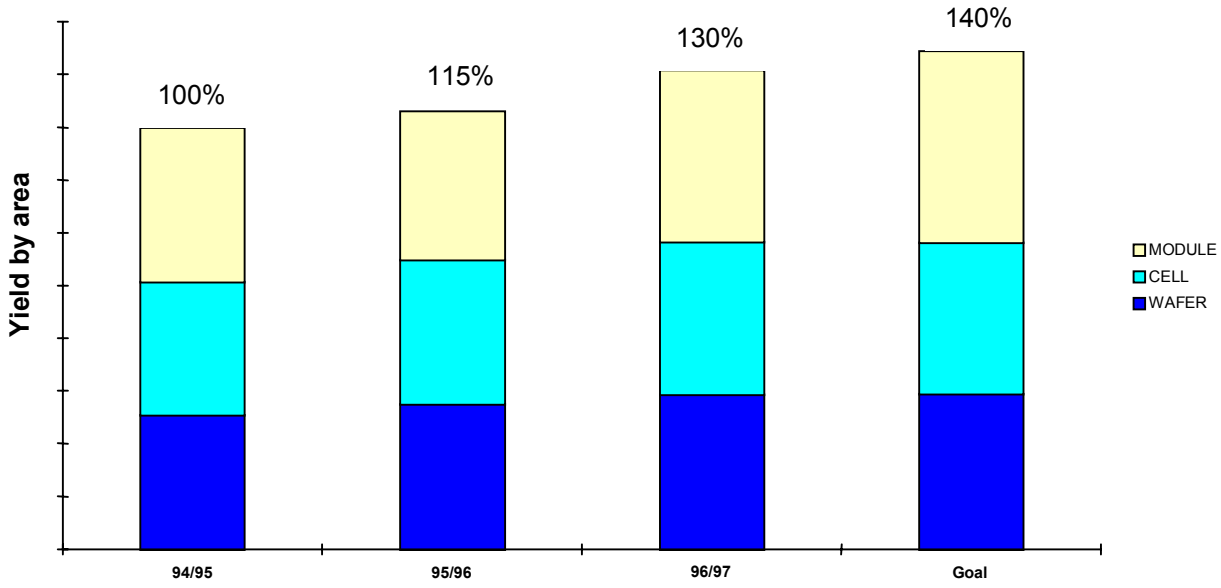

Figure 31. Yield on P-line product

Crystal Growth Yield

Yield in the crystal growth process has been strongly affected by the changes in availability in the polysilicon market. The different types of polysilicon raw material affects growth yields differently. The differences in raw material feedstock and their affect on growth yields are shown in Figure 32, where the "virgin chunk" feedstock gives the highest crystal pulling yields. Remelt polysilicon is shown as the second highest producer, and potscrap the lowest yielding material. All of these growth yields are with the material as received from the supplier.

An improvement in the growth yields have been realized by etching the various types of polysilicon. Figure 33 shows the same materials as shown in Figure 32, with the etching process performed prior to growth. As can be seen in Figure 33, a lot of the variation in the materials can be reduced, with surfaces being etched. This etching process has been adopted as a standard preparation process for polysilicon at Siemens Solar Industries.

The diffusion length of these various materials were measured after growth **1111** and shown in Figure 34. The measurements showed that etched virgin material and remelt gave the highest diffusion lengths both before and after thermal processing in phosphorus diffusion. The solar cells made from these materials showed similar results and the efficiency of these cells vs. material type are shown in Figure 35.

An additional study has been done to look at ingot "lifetime" with a tool developed by NREL. Figure 36 shows the measurements of different types of materials and different locations in the ingot. With the change in diffusion length through the thermal processes in the cell fabrication sequences, no correlation of this measurement to cell performance could be seen.

In addition to the improvements seen by etching the polysilicon, a major development activity has focused on grower performance improvement. There are three types of growers used at SSI, *analog* or manually controlled machines, *digital* or computer controlled machines, and *CG6000* machines which have a camera control system where the melt is monitored continuously and the diameter control is accomplished with a vision system. In total there are 41 crystal growers operating in SSI's Vancouver, Washington plant. To improve the yield in all three machine types a strategy of choosing a reference machine A strategy was adopted where a reference grower of each type was identified and optimized for three parameters:

- Yield (kg out/kg in)
- Total productivity per day (mm/day)
- A section length which is a measure of the first section pulled from the run

In using a reference grower, the population of like growers can be compared to the reference growers and systematically troubleshot to fix problems. An example is shown in Figure 37, where productivity on a reference grower is shown. Figure 38 shows a histogram of the population of growers like the reference grower. As can be seen by the two charts, differences exist and work has been done to make the grower populations emulate the performance of the reference growers. This strategy has been successful and is shown in Figure 39 where the crystal growth yields for the M line ingot have improved dramatically over time, by over 8% absolute. The dark bar is growth yield on analog machines and the light bar is growth yield on the digital machines. Likewise the gains in P line yield are shown in Figure 40.

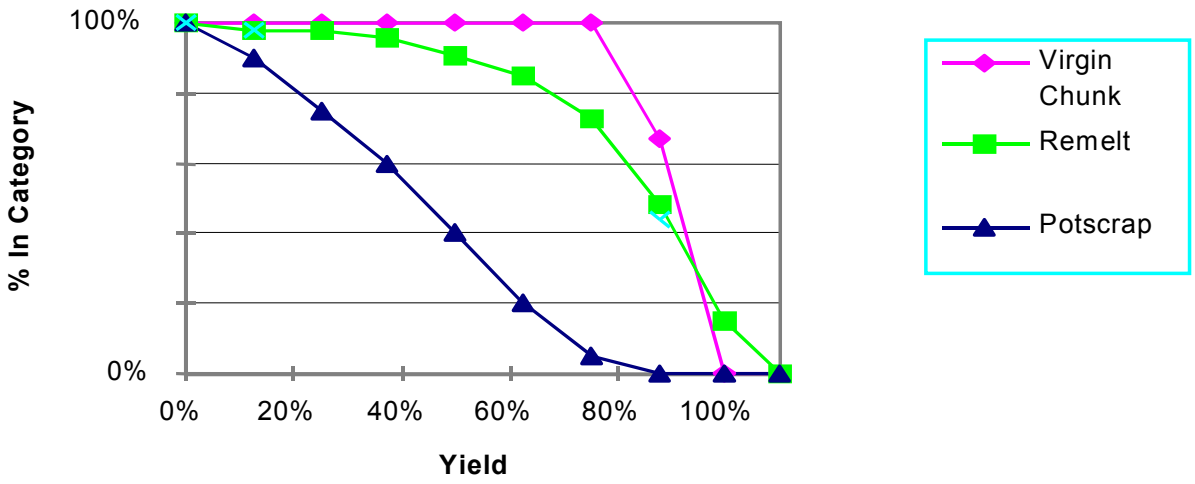

Figure 32. Growth yield by polysilicon type as received from supplier

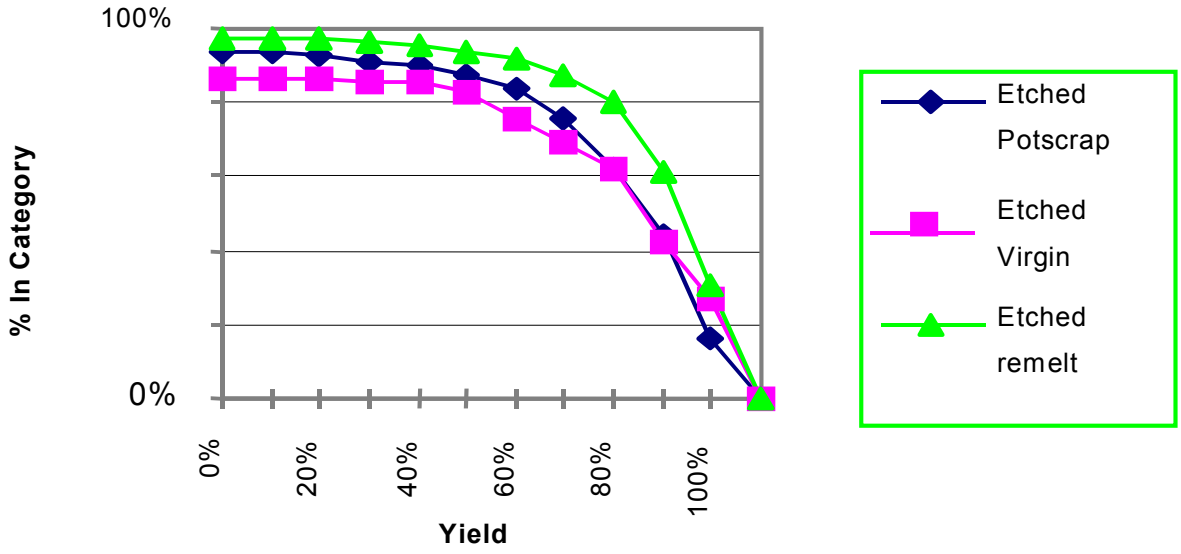

Figure 33. Growth yield by polysilicon type after etching

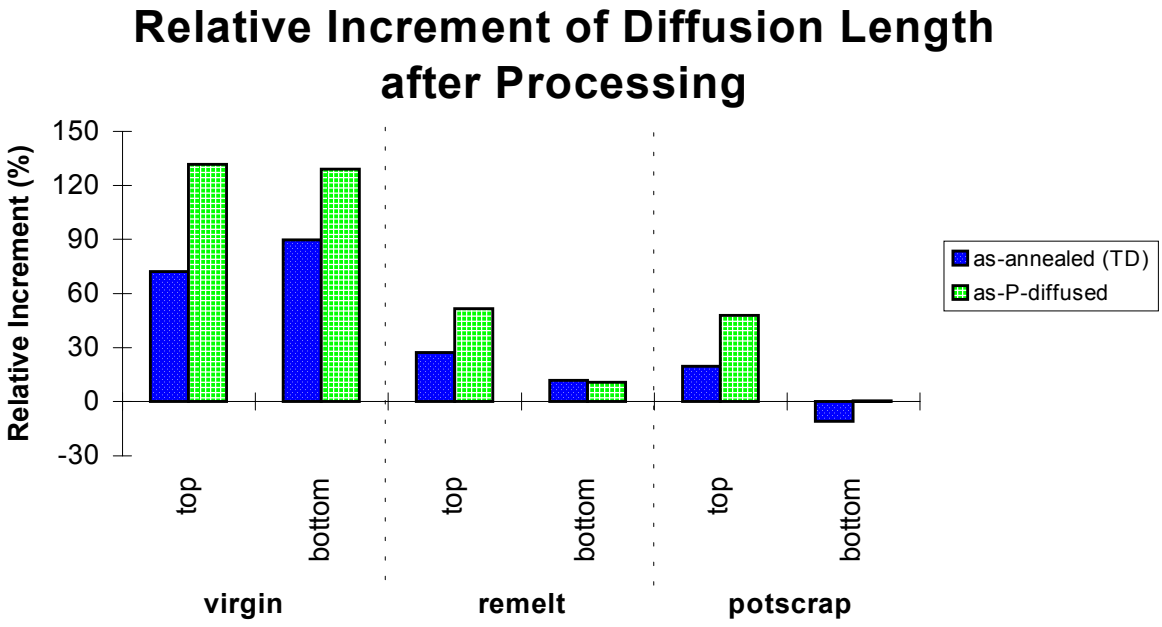

Figure 34. Diffusion Length vs. Material Type

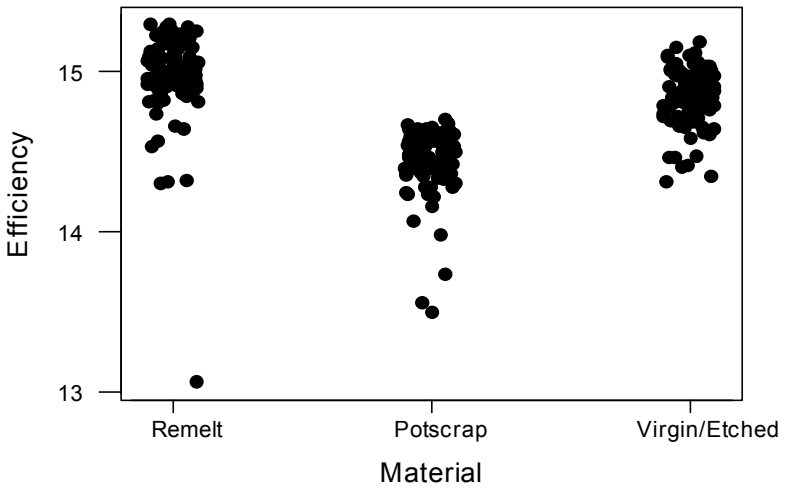

Figure 35. Cell Efficiency vs. material Type

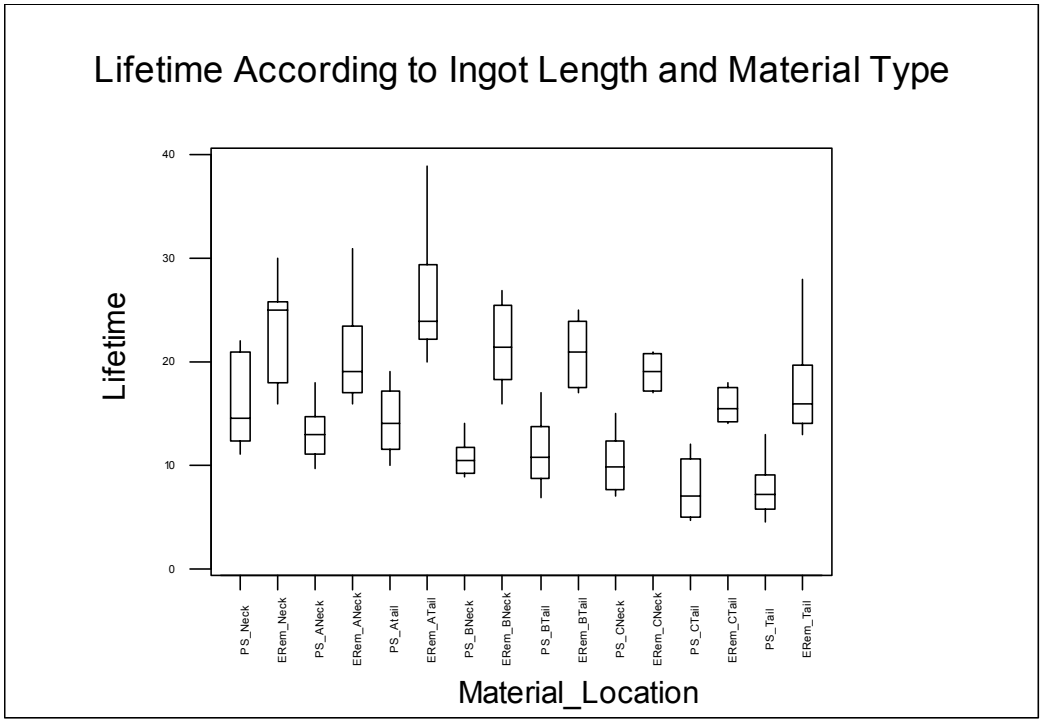

Figure 36. Lifetime vs. Material Type and Ingot Position.

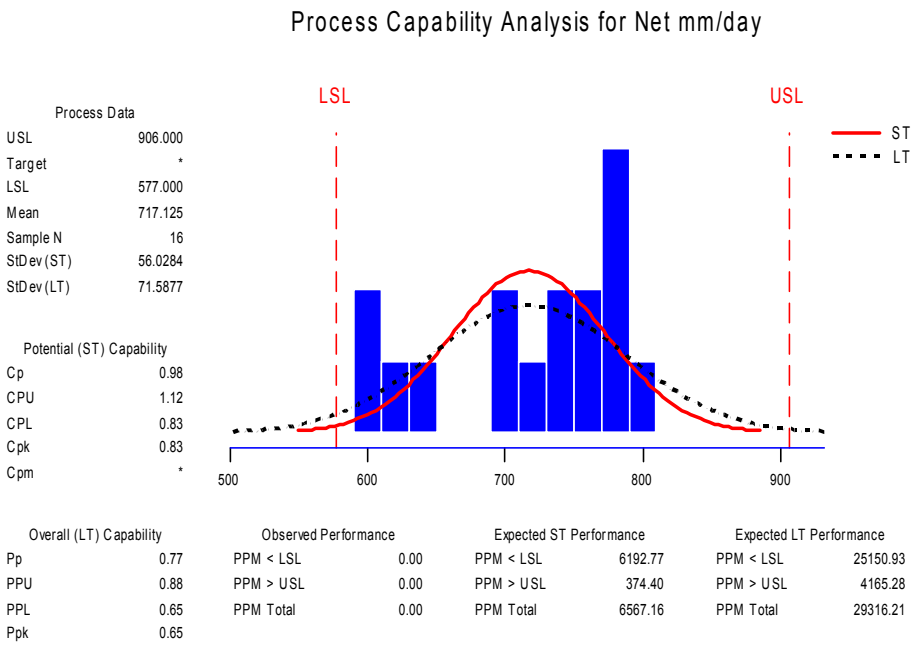

Figure 38. Reference Grower Performance for Net mm/day

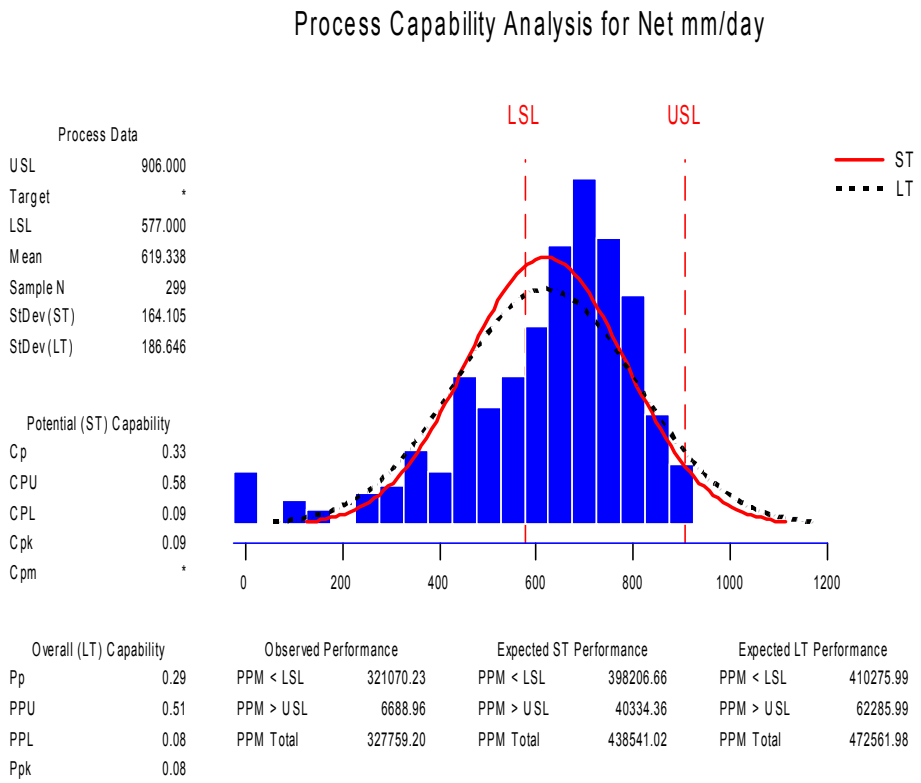

Figure 37. Grower Population Statistics for Net mm/day

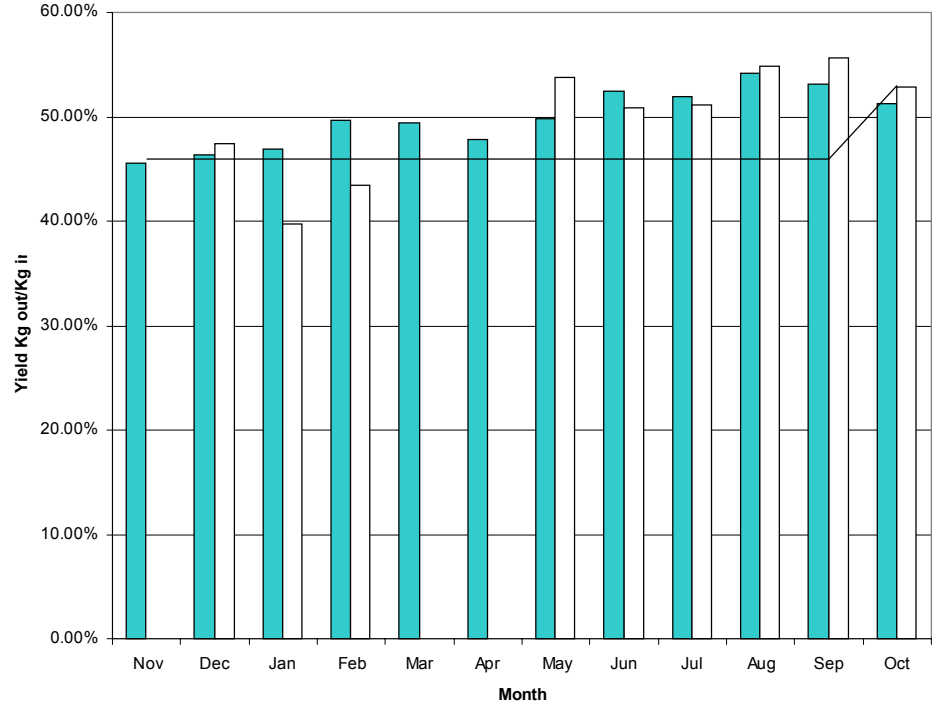

Figure 40. M-line Crystal Growth Yield

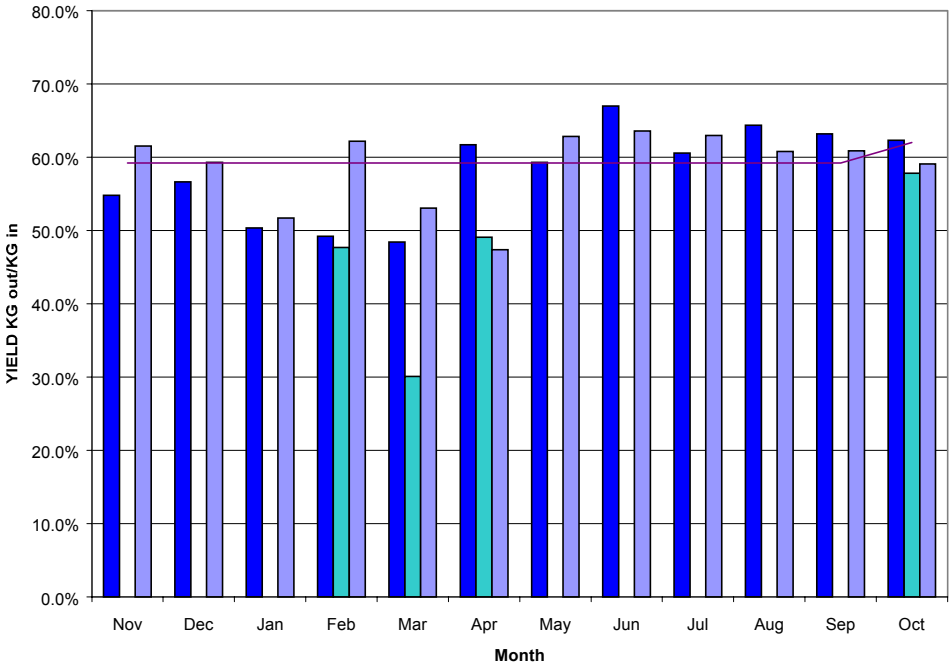

Figure 39. P-line Crystal Growth Yield

Wafer Yield

The wafering area yield and productivity is driven by the number of yielded wafers produced per inch of ingot fed into the process. This can be accomplished by improvement in yield which has been reported on in the previous (PVMat 2) contract summary, and additionally by the wafer thickness sliced including the kerf loss due to the wire. Improvements in wafers produced per inch of ingot is shown in Figure 41 inclusive of gains in PVMat 2 and PVMat 4. The total wafers per inch productivity has improved from 29 to over 50, a gain of over 65% in productivity. In phase two of this program the wire thickness has been reduced from 175 microns to 160 microns, resulting in a 4% gain in productivity in the wafering process. Figure 42 shows the thinner 160 micron wire test data on a population of 200,000 wafers. Based on this data and the supporting yield information, which stayed constant, the thinner wire is being deployed across all wire saws at Siemens Solar. As stated above, this is a 4% productivity gain across all wafer types, a savings of over $500K annually.

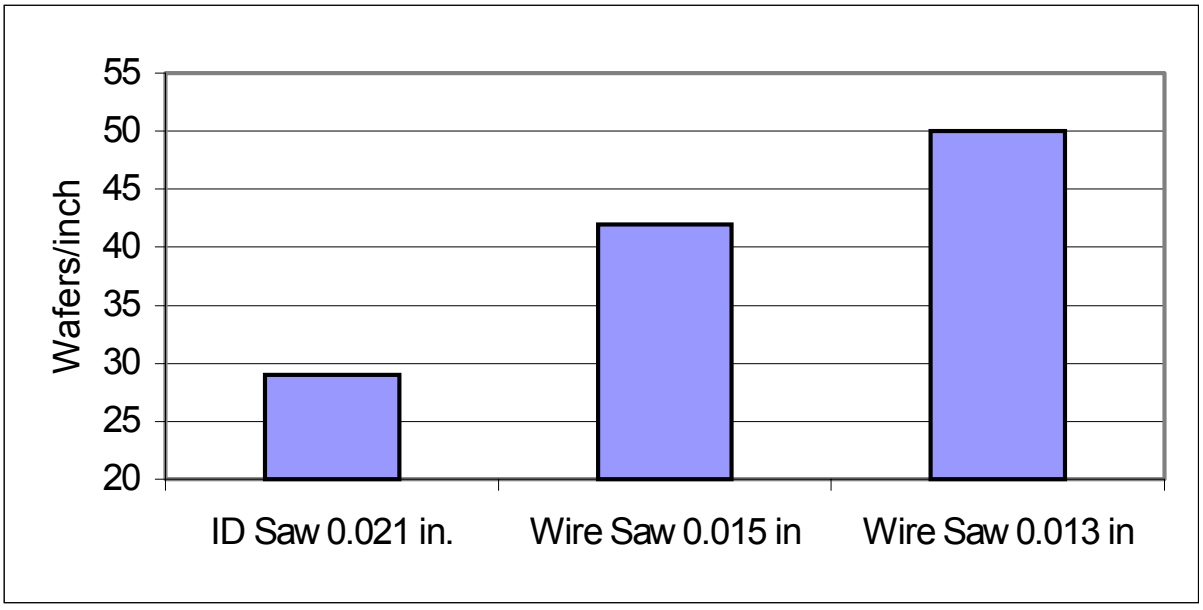

Figure 41. Wafers Per Inch Increase

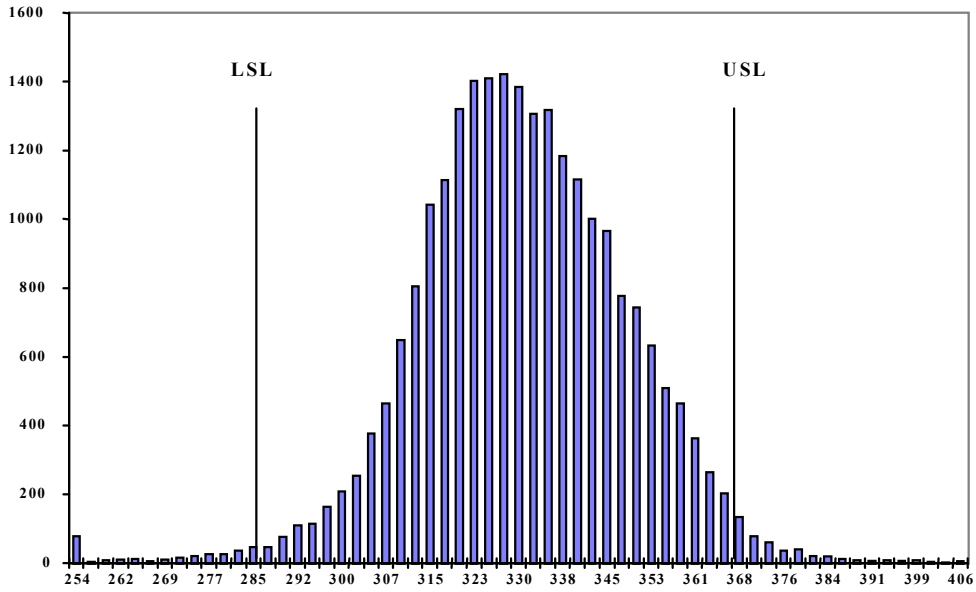

Figure 42. Thin Wire Thickness Test Data

Cell Yields

Cell fabrication yields are highly dependant upon both the mechanical and electrical yields of the process. The electrical yield in Siemens Solar's process is linked directly to the sheet resistance of the diffusion process. Figure 43 shows the reduction in variation implemented in the diffusion process by better profiling and control of the tube to tube thermal calibration. Additional capability studies and improvements are described in the SPC section of this report.

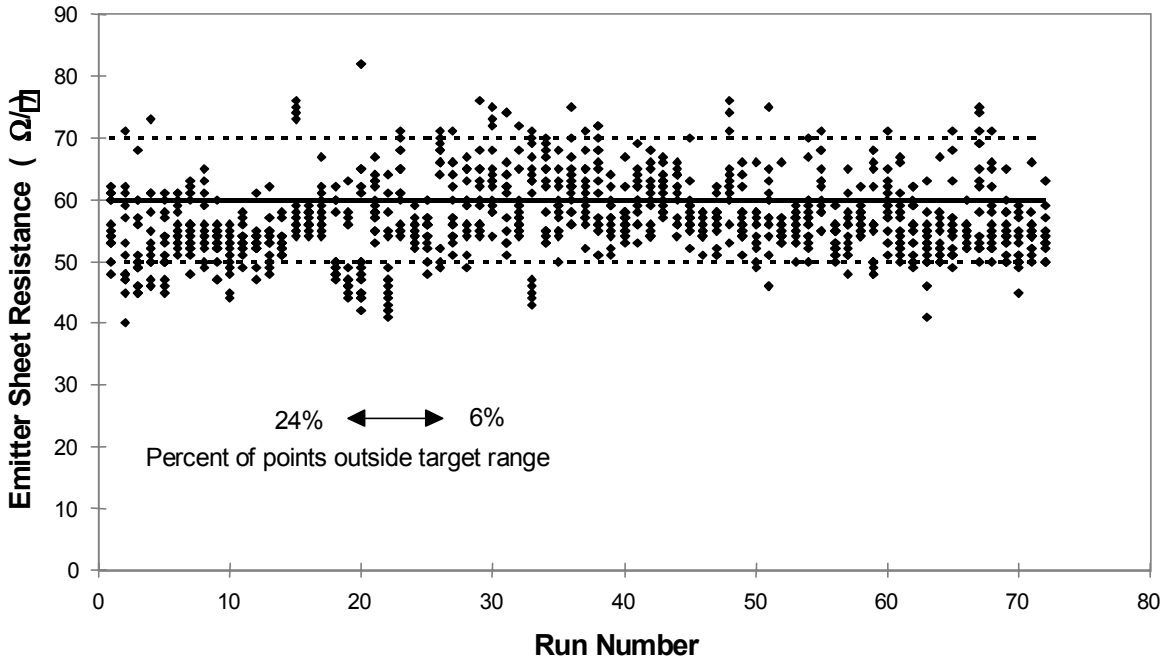

Figure 43. Sheet Rho Improvement in Diffusion Process

Thinner Large Area Wafers and Cells

In increasing yield and productivity and decreasing cost, the overall strategy is to increase the number of watts produced per kilogram of silicon, as in the work on increased growing yield with etching, increasing the number of wafers per inch of crystal as in the thinner wire deployment, and significantly decreasing cost with larger wafers as in the SR100 production. The combination of these three items needs to be done to maximize the benefit of cost reduction potential.

To this end, a series of experiments have been run to test the sensitivity of mechanical yield to wafer size and thickness. The crystal sizes used for the experiment represent the 103 mm, 125 mm, and 150 mm ingots which are standard sizes at Siemens Solar Industries. The wafer thickness used for the experiment ranged from 125 microns to 400 microns.

Figure 44 shows the yield of various wafers sizes at various thicknesses through the wafer slicing process. The x axis of the chart is slicing thickness in microns, the y axis is yield of wafers out divided by wafers in reported in percent, and the lines represent different cell sizes. As can be seen from the graph, the yield of all wafer sizes drops as the thickness is reduced below 200 microns.

This is also evident in the cell yield graph, shown in Figure 45, where cell yield is declining at values lower than 300 microns.

Figure 46 shows the combined effect of the wafering and cell yields, versus the potential productivity gain. As is evident in the chart, the productivity potential by making the wafers thinner is very high, as much as 180% relative to 400 micron slices. As is also evident in the graph, many areas of the production line will need to be modified to produce high yield, large area, thin cells.

This data allowed SSI to move from 400 microns to 315 microns on the M line cell during this program, a gain of 15% in productivity overall. The P line moved from 400 microns to 385 microns a gain of 3% overall.

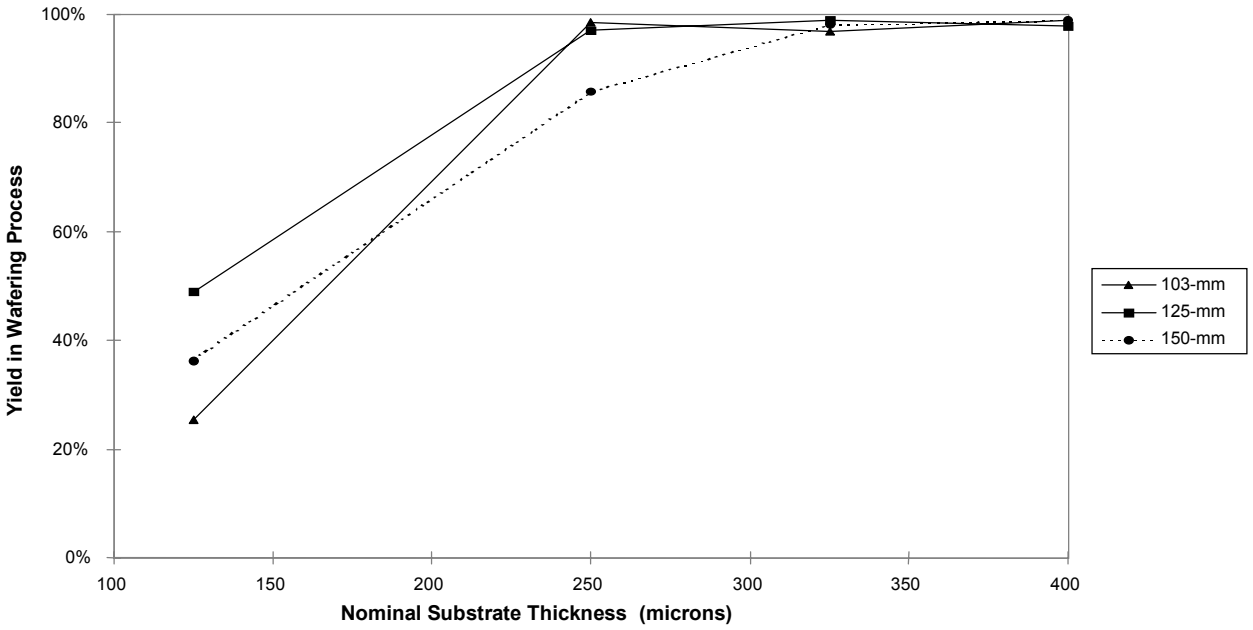

Figure 44. Yield in Wafering vs. Thickness and Size

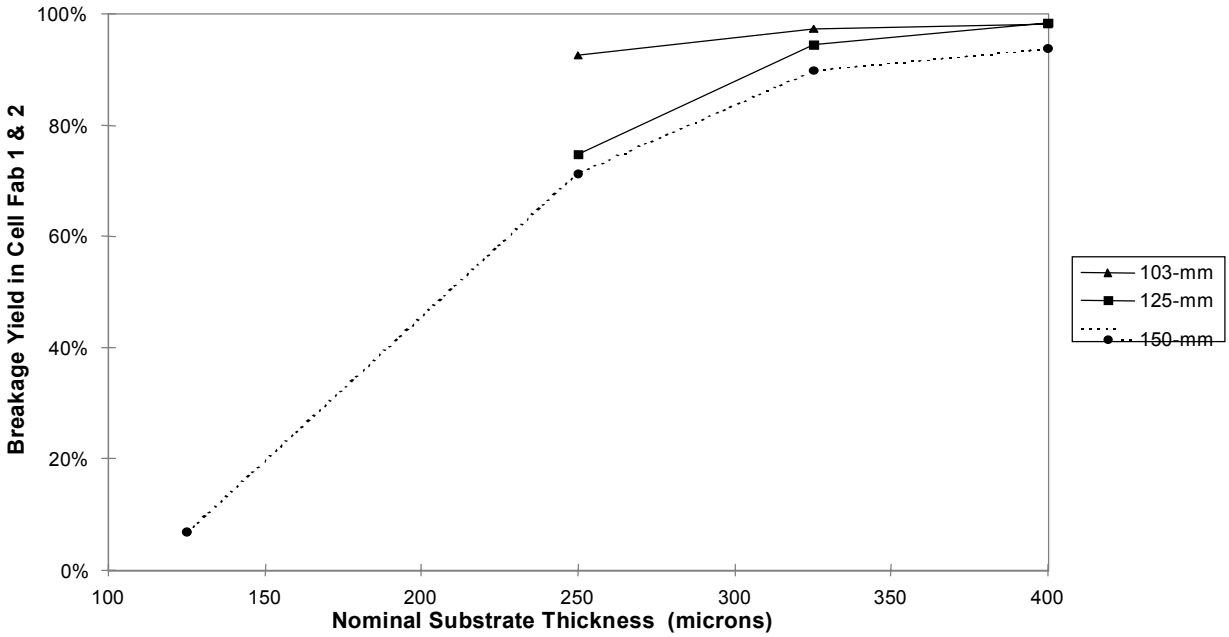

Figure 45. Yield in Cell Fab vs. Thickness and Size

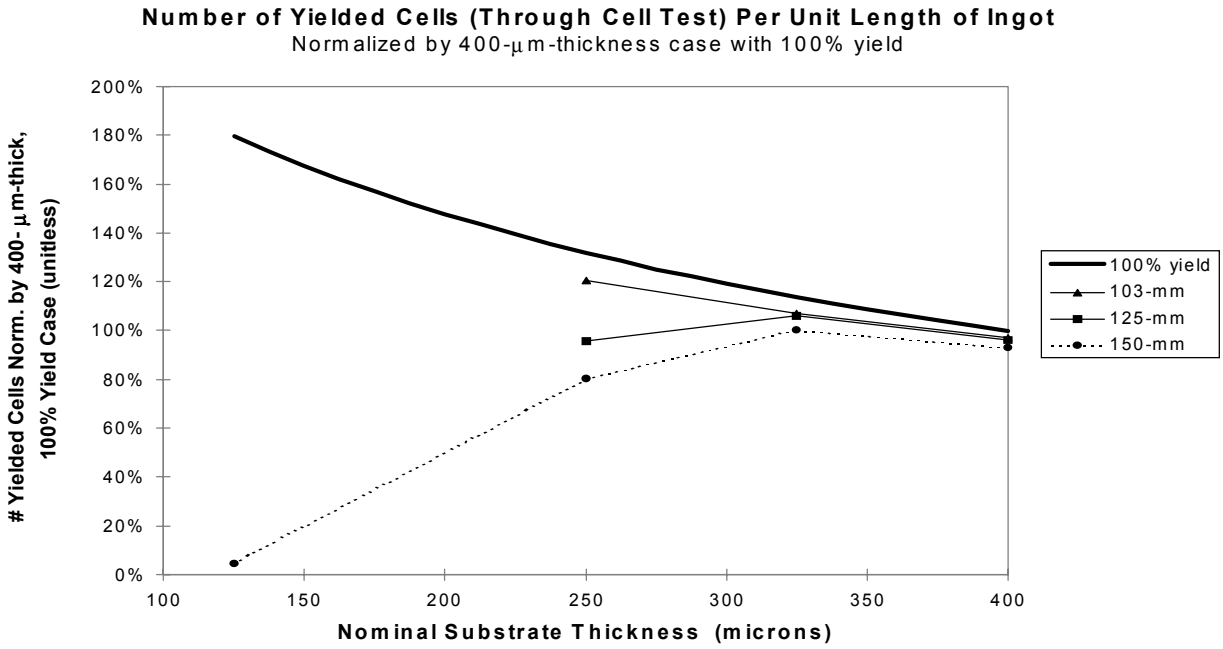

Figure 46. Yield vs. Increase Cell Productivity

Manufacturing Systems to Improve Module Reliability

ISO 9001 Certification

The SSI Camarillo plant received ISO 9001 certification in March 1996. This is a major milestone in the pursuit of quality manufacturing systems, and represents a very substantial effort by the company to establish and document procedures, operator work instructions, maintenance and calibration schedules, conduct operator training, etc. The benefit is a profoundly improved system to ensure manufacturing compliance and control of its processes. It is, however, only a beginning. The follow on support has been successful as SSI has passed additional surveillance audits during Phase II and III.

Statistical Process Control Implementation

In order to maintain reproducible and reliable photovoltaic manufacturing, key process control points, such as wafer thickness variation, emitter sheet resistance, cell fill factor, lamination defects, etc., must be established. Part of the statement of work of this contract is to identify which measurements are suitable for tracking by statistical process control (SPC), and to implement SPC charting on those points by the end of Phase II. SPC methods are now in use at many sites in the plant, baseline data is being gathered, and a feedback mechanism for early detection of out-of-control process conditions exists. Figure 47 shows an SPC chart of emitter sheet resistance after diffusion as an example. The data is characteristic of an in-control process, well-centered on the target value. The regular charting of data by operators fosters greater participation, and provides a way to monitor progress in bringing a process parameter closer to a target value, tightening the distribution of values, or improving yield. Figure 48 gives an example of a shift in the average value of automatic soldering yield, and distribution tightening, coupled to events in the line.

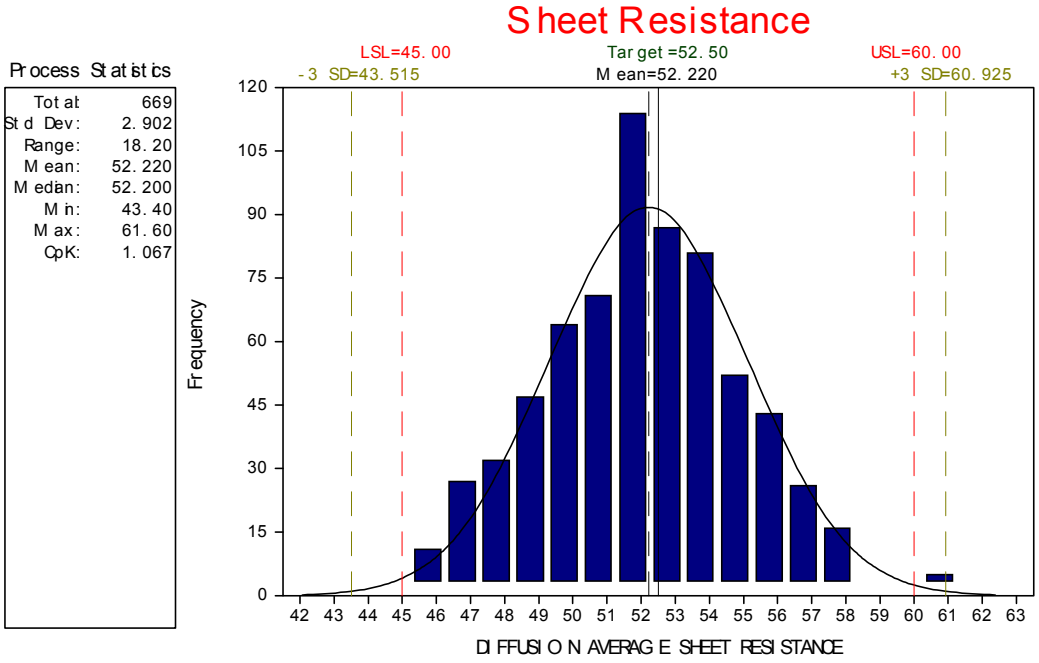

Figure 47. SPC charting of emitter sheet resistance after diffusion.

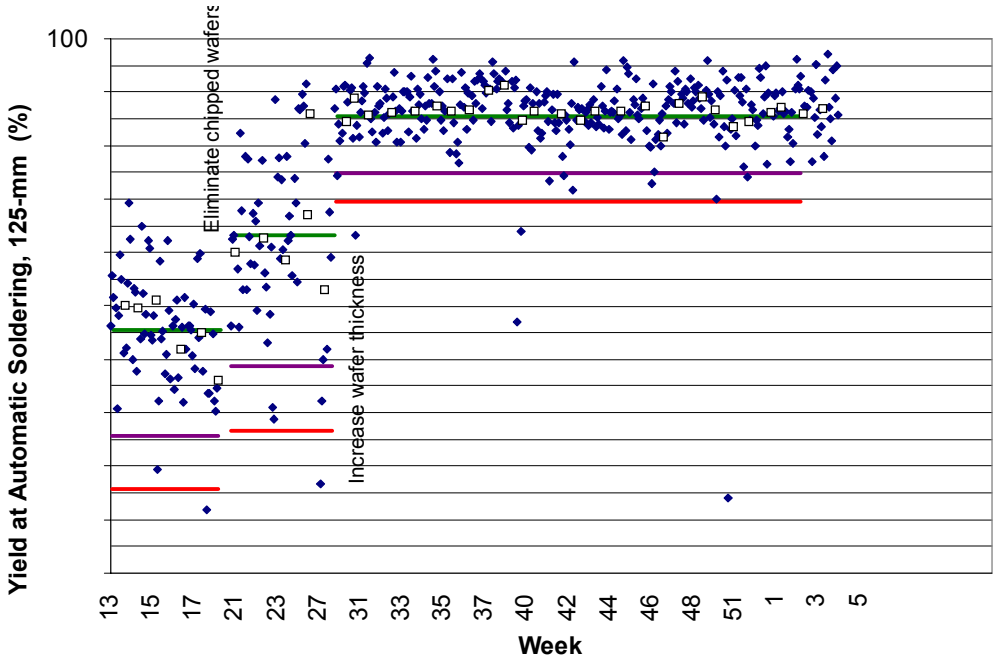

Figure 48. Charting of automatic soldering yield provides feedback mechanism to gauge the effect of process changes.

SPC is best suited for processes in which an operator or engineer has an opportunity to respond to an out-of-control condition, by halting the process before further parts are placed at risk, and following an action plan to ascertain the reason for the loss of control. For other processes, for which the effect of the measured parameter on the end product is not yet well understood, it is appropriate to store the measurements in a database which can be used to determine interactions between several process parameters. For still other processes, for which the emphasis is not on control but adherence to a specification limit still needs to be checked, a simple pass/fail measurement may be appropriate, and uses the least labor resources.

Table 2 shows the measurement points in the SSI photovoltaic manufacturing process which have been identified as useful to track by SPC. These points share the feature that action can practically be taken when the measured value strays from its normal range to bring the parameter back into control, or at least to avoid damaging or misprocessing further parts. Many of the points are tracked by manual charting on the part of the operator. This has the advantage of enhancing the visibility of the data and of trends for the operator, as opposed to entering the data in a computer program, and often manual charting is the most appropriate method. Computer entry of measurements for SPC charting is less time consuming, however, thus improving productivity. SPC has been implemented in all of the points identified as appropriate in Table 2, exceeding the goal of 50% implementation by the end of Phase I. Table 3 shows other measured parameters that are not tracked by SPC, but that are either stored in a database to identify interactions with other parameters, or are used to check manufacturing compliance to documented specifications.

Table 2. Photovoltaic manufacturing control points at SSI appropriate for statistical process control (SPC) tracking.

Process Area	Control Point	Measured Data Charted by SPC Manually	Measured Data Charted by SPC on Computer
Ingot	Base pressure of crystal growth chamber	X	
	A section length	X	
Wafer	Wafer thickness		X
	Thickness variation across wafer		X
	Acetic acid concentration	X	
	Wafer cleaning rewash rate	X	
	Breakage in wafer cleaning	X	
Cell	Reject rate for surface defects after wet etch	X	
	Sheet resistance after diffusion		X
	Sheet resistance after oxidation		X
	Breakage in 1st half of cell fabrication	X	
	AR coating thickness		X
	Cell fill factor after contact firing	X	
	Reproducibility of cell test	X	
	Breakage in cell printing	X	
Module	Breakage yield in automatic cell soldering	X	
	Yield through circuit assembly	X	
	Reproducibility of module test	X	

Table 3. Photovoltaic manufacturing control points at SSI appropriate for check against documented specifications or procedures, and/or for storage in computer database.

Process Area	Control Point	Measured Data Recorded Manually & Checked Against Spec.	Measured Data Stored in Computer Database
Ingot	Meltdown time		X
	Stabilization time		X
	Tail length		X
	Pop diameter at tail		X
	As-grown ingot diameter	X	X
	Bulk resistivity of top of ingot	X	X
	Bulk resistivity of bottom of ingot	X	X
	Conductivity type (p- or n-type)		
	Corner-to-corner diameter	X	
	Flat-to-flat dimension	X	
	Parallelism of flats	X	
	Length of ingot	X	
	Length of full-diameter ingot lost due to: bulk resistivity improper tailing ingot fracture diameter		 X X X X
Wafer	Yield through wire sawing/boating		X
Cell	Breakage in AR coat, printing, contact firing: cell line with manual belt unload cell line with automatic belt unload		 X X
	Cell electrical performance		X
	Yield loss due to low electrical output		X
Module	Solder bond pull strength	X	
	EVA elongation test	X	
	Incidence of laminate defects, by type		X

An area where Siemens Solar is fully deploying the use of SPC charting is in the evaluation of routine monitoring of the reliability of its product. Every month Siemens Solar randomly selects samples of its production product and runs these products through the standard environmental sequence of Thermal and Humidity Freeze (T50 10 HF) cycles, 200 thermal (T200) cycles and 1000 (Damp Heat 1000) hours of damp heat exposure at 85 degrees C, 85% relative humidity. This deployment of SPC in the gathering and analysis of the data, is the baseline which has allowed Siemens Solar to have a 25 year warranted product. As can be seen from the charts which cover the period of 1992-1997, the control is excellent.

Figure 49 shows the performance of Siemens product to the T50 10HF test cycle with all points in the control band.

Figure 50 shows the data from the T200 testing, where a few points are out of the control range. These points were later traced to a simple process fix which could be implemented rapidly to further enhance process control on the production line.

Figure 51 shows the data from the DH1000 testing, showing three recent points out of the control range and a variation in the data starting in the latest time period. This data has shown to be related to the change in humidity resistance of a module component which is now being worked with the supplier of that component. This work has commenced based on this long term statistical information and has been useful in troubleshooting with the supplier, where there has been a change in the supplier's process.

Deployment of this type of SPC analysis continues at Siemens Solar Industries and is invaluable, not only for warranty assessments, but as a very valuable tool to indicate overall process stability and conformance to specifications on Siemens Solar's production line. This maturity in process control is unique to SSI and is a result of both the ISO 9000 effort and PVMat program combined to focus on the elimination of process variation, and the confirmation of that reduction by the use of statistical tools.

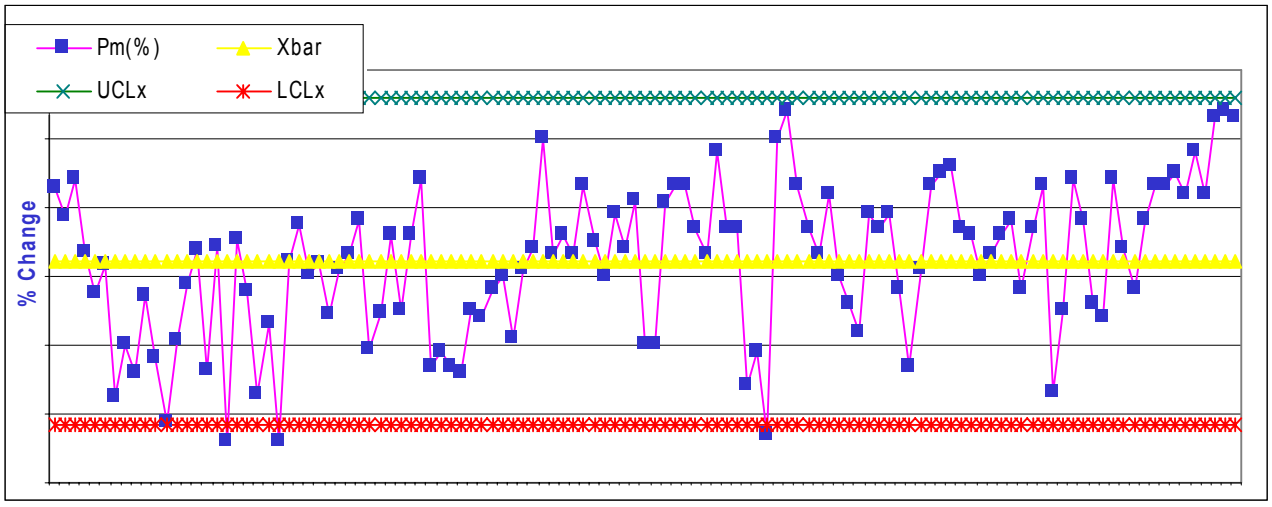

Figure 49. T50 10HF SPC chart for test data

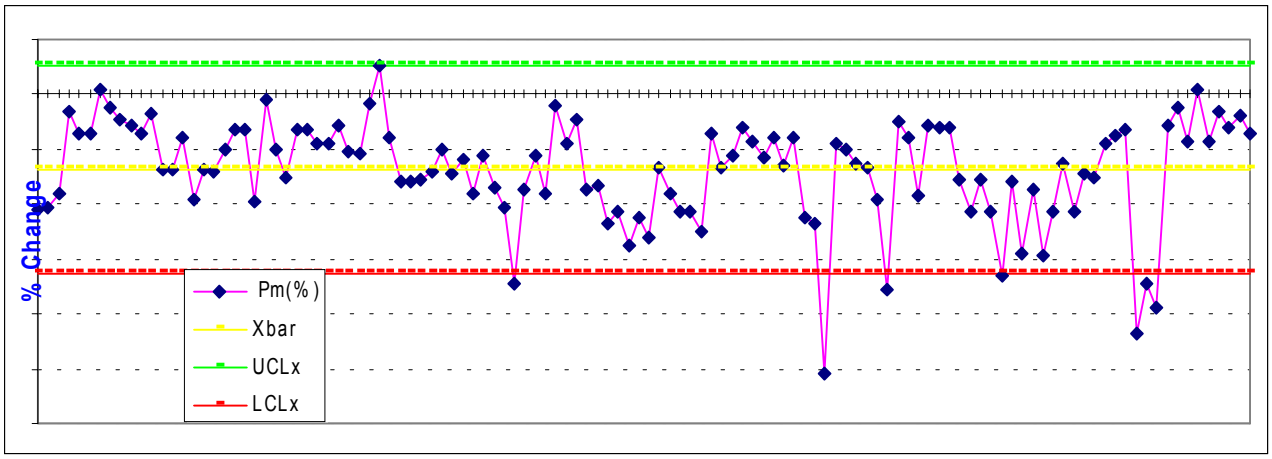

Figure 50. T200 Exposure Data SPC Chart

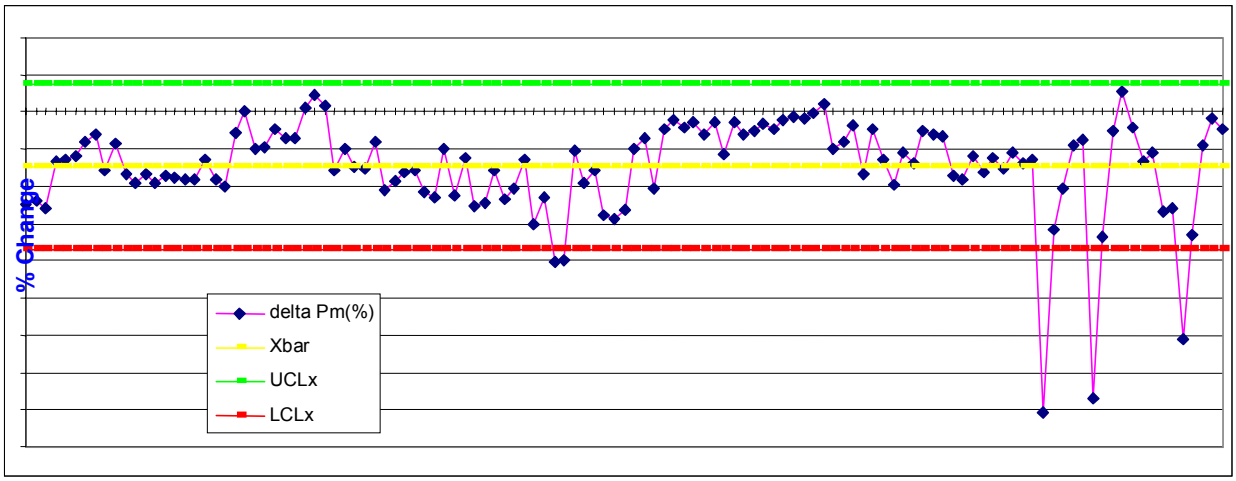

Figure 51. Damp Heat 1000 SPC Data

Conclusions

Cost drivers for Cz Si solar cell modules have been identified. Cost components for existing photovoltaic technology were resolved by process area (ingot, wafer, cell, or module), by direct and indirect materials and labor in each area, and the cost of yield loss in each area was quantified. Cell size and shape, material usage, module size, and cell and module yields have an especially strong influence on cost. A model was developed to show the dependence of module cost per watt on module size, using actual material and labor cost data as inputs. Specific module designs to address cost issues have been implemented, as have numerous other measures to reduce the cost per watt. Broader changes to the module configuration based on the 150-mm-diameter round cell are in progress during Phases II and III.

Wafer breakage is the mechanism which dominates cell yields. Breakage was reduced by investigation of the factors which affect wafer strength, improved tracking of breakage rate in different processes, enlistment of operator involvement, and development of more robust processes. In the wafering, cell fabrication, and module fabrication areas taken as a whole, yield has increased by 8.5 relative % in Phase I, in excess of the 5% goal in the statement of work. The yield in the crystal growth area is not included in this change in yield: the shortage of silicon feedstock during Phase I has forced the use of many non-traditional sources of silicon, most of which seriously compromise crystal growth yield, making it difficult to gauge the effect of efforts to improve ingot yield in this time frame. Productivity measured in terms of kW produced at the module level per direct labor employee has been improved through automation and development of more efficient work practices. Productivity has increased by 6.5% in Phase I, exceeding the goal of 5%. The development of systems to ensure compliance and control of module manufacturing includes ISO 9001 certification received by SSI in March 1996, and the ongoing implementation of SPC methods at key control points in manufacturing. Over 80% of the measurement points identified as appropriate for SPC have been implemented in SSI manufacturing, in excess of the goal of 50% by the end of Phase I.

As a result of yield gains in wafering, cell, and module fabrication, productivity gains throughout the plant, and design and procurement improvements, items directly related to the PVMaT statement of work sum to greater than 8% savings in cost per watt at the module level through the end of Phase I, exceeding the 6% goal for cost reduction. It should be noted that this cost-per-watt savings does not include the negative impact of lower yield in crystal growing in this time frame due to the industry-wide silicon feedstock shortage described above. Module design work and prototyping in Phase I, centered around the cost reduction themes of larger modules, larger cells, and better match of the wafer shape to the ingot cross section, has led to the development of a new, low cost-per-watt module line based on 150-mm-diameter round cells. Implementation and refinement of this module design will be the focus of further cost reductions in Phases II and III. Based on the approach of large modules with 150-mm-diameter round cells, a 19% reduction in module cost per watt is projected, with production beginning in Phase II.

Productivity and yield in every major process area has been achieved. Better pulling yield in crystal growth with an emphasis on material cleanliness has been realized, as well as productivity and yield gains in the large machines deployed in Siemens Solar's Vancouver growth plant. Wafering yield and productivity has been improved by thinner wire implemented for cutting. Cell processing yield has been improved by the reduction in variation in the diffusion process.

SPC deployment is complete in the key process areas throughout the manufacturing line. More work is planned for the less significant process control points through phase III. Full use of SPC in evaluating environmental data is on going.

As a result of yield gains in wafering, cell, and module fabrication, productivity gains throughout the plant, and design and procurement improvements, items directly related to the PVMaT statement of work sum to greater than 17% savings in cost per watt at the module level through the end of Phase II, meeting the 12% goal for cost reduction. Module production of larger modules, larger cells, and better match of the wafer shape to the ingot cross section, has led to the development of a new, low cost-per-watt module line based on 150-mm-diameter round cells. Based on the approach of large modules with 150-mm-diameter round cells, a 17% reduction in module cost per watt is projected, with production fully deployed.

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13. ABSTRACT *(Maximum 200 words)*
This report describes work that focused on reducing the cost per watt of Cz silicon photovoltaic modules under Siemens Solar Industries' (SSI) DOE/NREL Photovoltaic Manufacturing Technology (PVMaT) 4A subcontract. SSI researchers deployed new module designs, realized improvements in yield of more than 25%, and implemented statistical process control (SPC. They have described yield improvements in detail and reported on the deployment of SPC in critical process steps. The sum of all improvements resulted in a greater than 17% cost per watt reduction in manufacturing.

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