September 1999 • NREL/SR-520-26833

Subcontractor Report

Market-Driven EFG Modules

Final Report
14 December 1995—30 June 1999

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SUMMARY

This report describes the progress made in the 3-year program at ASE Americas Inc. in the PVMaT 4A2 Initiative on the development of Edge-Defined Film-Fed Growth (EFG) silicon wafer technology. This program was performed over the period from December 14, 1995 to June 30, 1999. The work focused on advancing EFG manufacturing technology and lowering production costs in three areas:

I. EFG Wafers – through better silicon feedstock utilization, improvements in growth, a wafer thickness reduction from 300 to 250 microns, and a higher bulk wafer electronic quality; additionally, new technology for laser cutting of wafers was demonstrated;

II. Solar Cells - by an increase in solar cell efficiency, and implementation of a new glass etch process;

III. Modules – by lamination cycle improvements, introduction of a new diode housing, and simplification of module construction.

The program will exceed its overall goal of reducing EFG module manufacturing costs by 25%. About 17% of these improvements are already implemented in manufacturing. Technology to achieve an additional cost savings of 11% is in the final stages of introduction into large scale manufacturing. Specific progress in the key tasks are summarized below.

Wafer Manufacturing

New sieving techniques for pelletized silicon feedstock were developed to attain better material utilization, and to reduce the impact of silicon dust on the hot zone. EFG crystal growth furnace components were redesigned to reduce stresses in EFG tubes and increase the average lifetime of graphite dies. The stress reduction was required to maintain yield in the initiative to reduce wafer thickness from 300 microns to 275 microns. The second stage of thickness reduction to 250 microns has been held up due to concern for yield in cell and module manufacturing. Other improvements in the hot zone design have resulted in a doubling of the number of octagons grown from a single crucible. EFG wafer bulk electronic quality was raised through development and implementation of better purification methods for graphite parts used in the crystal growth hot zone which control the impurity contamination of the wafer. Laser technology used to cut EFG tubes into wafers was improved to raise yields of thinner wafers. Lasers with the potential of increasing cutting speed by a factor of four were evaluated. A reduction of labor costs *in wafer production* of 50% is anticipated with eventual implementation of high speed laser cutting technology. Overall wafer manufacturing improvements implemented in this program contributed toward lowering module manufacturing costs by 6%.

Cell Manufacturing

A major thrust in cell manufacturing was to improve average cell efficiency. This was to be accomplished through improvements in cell design, in particular, by optimizing the emitter grid to reduce series resistance, by adding a textured anti-reflection layer to the cell surface to reduce reflectance losses, and through developing Statistical Processing Control (SPC) methods for cell processing. The emitter grid redesign has been completed and has been introduced in the manufacturing line. The textured anti-reflection layer did not deliver the expected improvement, and work on it was stopped. SPC techniques were instituted in cell production. This included the installation of equipment to automate data collection. Application of SPC has started. It is estimated that by tightening the overall distribution of cells produced in manufacturing, it has helped us raise cell efficiencies on average by 0.2%. The SPC system is still in the early stages of development and this will be continued in our next PVMaT program. We anticipate that SPC will continue to provide cost reductions as the system implementation proceeeds. In another cost reduction effort, a new technique for removing phosphorus glass from the cell surface after diffusion was demonstrated. Manufacturing line prototype equipment now has been built and is being evaluated in production. Full implementation of this process will result in reduction in fluoride effluent by more than 98%. Overall cell manufacturing improvements accomplished in the cell area have reduced module manufacturing cost by 7%.

Module Manufacturing

Module lamination cycles were shortened and the construction of the module changed to improve the yield in the lamination step. A new diode housing was developed and tested to reduce construction material costs and to improve functionality for customer benefit. These improvements have resulted in a 4% reduction in the cost of EFG modules to date. Simplification of module designs developed in the program will produce an additional cost reduction of 11% . These designs have gone through the prototype phase, and modules are in the final stages of environmental testing and acceptance qualification. We also have completed an extensive study of new encapsulants. One encapsulant we have evaluated is very similar to that we use, but has shown superior resistance to ultraviolet light degradation. We have completed environmental testing and plan to introduce it into manufacturing soon. Another encapsulant is liquid at room temperature and thus has advantages in encapsulating thinner wafers by allowing higher yields to be realized. Tests of this encapsulant are continuing.

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1.0 INTRODUCTION

The goal of the PVMaT 4A2 program at ASE Americas has been to reduce the manufacturing cost of photovoltaic (PV) modules based on silicon wafers produced by the Edge-defined Film-fed Growth (EFG) method.

In the wafer production area, ASE investigated methods to improve silicon feedstock utilization, growth system improvements to increase material quality and the number of tubes grown per crucible, and effective ways to reduce wafer thickness, not only to reduce silicon materials costs, and ergo wafer costs, but also to increase average cell efficiency. Thinner wafers require thinner EFG tube walls which can lower the yield of laser cutting of tubes into wafers. Thus, laser cutting processes needed to be modified to handle these thinner wafers and were necessary to the success of the thin wafer program. Wafer electronic quality was also improved by optimizing the tube growth process and by reducing contamination of EFG tubes during growth.

Another task in the PVMaT program was aimed at reducing cost per watt by increasing average cell efficiency. Although the average efficiency of the EFG cells manufactured at ASE Americas has been high relative to the efficiencies of mass-produced cells made on multicrystalline silicon by other manufacturers, further increases in efficiency were possible. Improvements were made in bulk material quality, and average wafer thickness was reduced, both of which contributed to increased cell efficiency. In cell manufacturing, the front metal grid was redesigned to improve cell efficiency by reducing series resistance by increasing the number of fingers, while minimizing increased shadowing. Because of the proprietary method used at ASE to metallize cells, this change required reengineering of the equipment used in the metallization process. The maintenance of high cell efficiencies was furthered by the introduction of Statistical Process Control techniques to determine the optimum parameters for every process step and to ensure that each is performed consistently from lot-to-lot and day-to-day. We also reduced cell processing costs by finding a substitute for the conventional process for removing phosphorus glass after emitter diffusion. This development is also of environmental benefit because it reduced acid utilization.

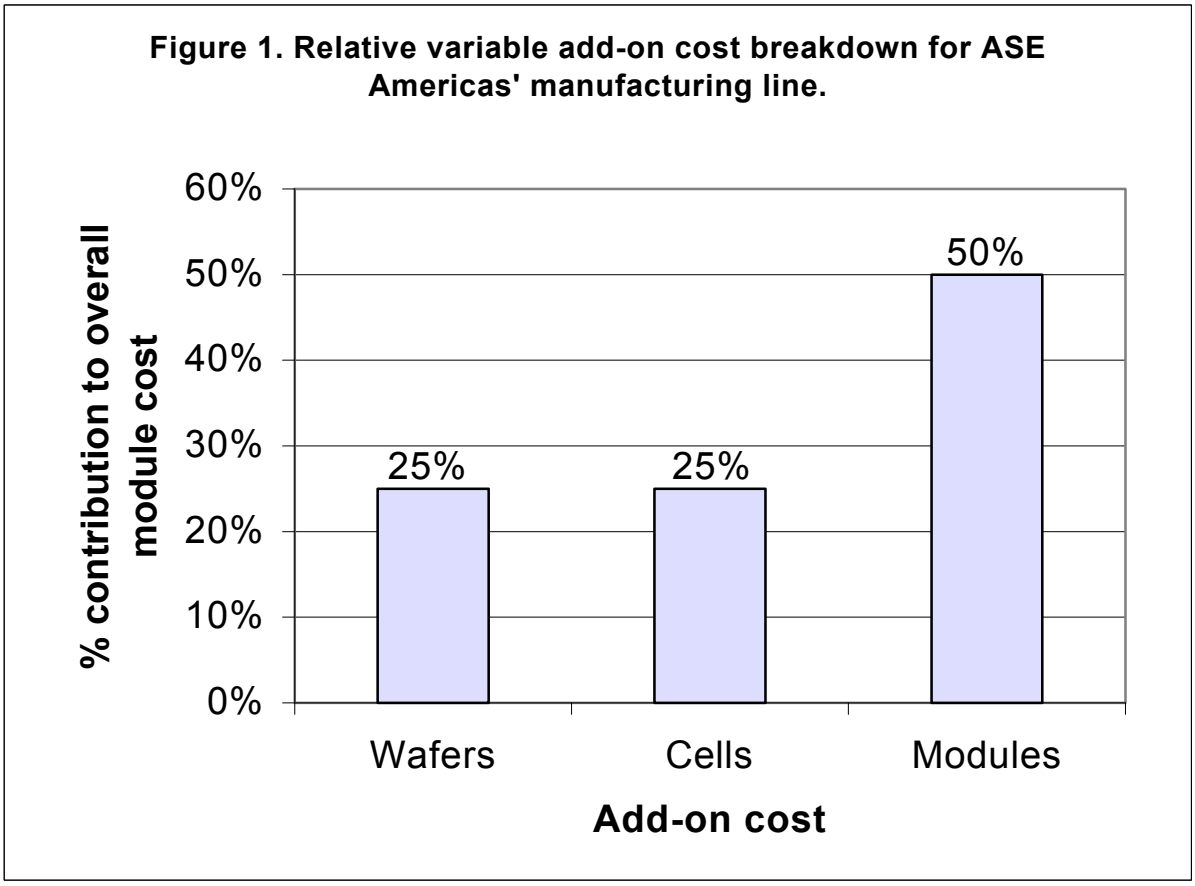
Lamination and module assembly is the most expensive part of the manufacturing process, accounting for almost one-half of the cost of the finished module. Two significant material costs in module assembly are the aluminum frame and the diode housing. Another major cost in module assembly is the vacuum lamination process, which is relatively slow for the high reliability encapsulant used at ASE Americas. During the program, we improved existing technology and developed subtitute processes and materials in all of these areas. We also evaluated new encapsulants for their potential to increase module yields and lifetime in the field.

The goal of the current PVMaT subcontract has been to reduce module cost by 25% by the end of the third and final phase. This report discusses the technology improvements which have been demonstrated. We have implemented technology to reduce module costs by 17% to date. Additional work which has been completed, and which will be introduced into manufacturing in the next 6-12 months, will result in a further 11% module cost reduction. These developments will allow us to exceed the original program goals.

2.0 ASE TECHNOLOGY PRIOR TO THIS PROGRAM

In this Section, ASE's manufacturing process prior to this PVMaT effort is described. Some parts of this process remain unchanged today; improvements made under the program are described in Section 3. An outline of the overall ASE manufacturing process is presented in Table 1; boldface steps have been re-engineered under the PVMaT program. Figure 1 identifies the distribution of costs among the three areas of Wafers, Cells and Modules for which improvements in technology will be discussed. Approximately 25% of total module manufacturing costs are incurred in each of the wafer and cell production areas, and 50% of costs are in module fabrication.

Figure 1. Relative variable add-on cost breakdown for ASE Americas' manufacturing line.



The technology used for manufacturing modules at ASE Americas is based on the EFG method for growing silicon in a closed hollow shape, which is currently in the form of an octagonal tube from which eight ribbons are cut. An 'octagon' EFG tube has a wall thickness of approximately 300 μm and is grown to a length of about five meters. When the desired length is reached, the tube is detached from the die and removed from the furnace. A new seed is then lowered onto the die tip, and growth is resumed. This procedure is repeated until the die deteriorates and must be replaced. A multi-tube run between die replacements is called a 'growth run'. After a run is ended, the furnace is cooled, and the section of the furnace containing consumable parts is removed and replaced. The consumable parts are disassembled and rebuilt for re-use.

Table 1. ASE PV Module Manufacturing Process
(Boldface indicates steps improved as part of this subcontract)

WAFER AREA

Sorting of silicon feedstock

Growth of EFG octagon tubes

Laser cutting of tubes into wafers

CELL AREA

Silicon wafer etch

Phosphorus diffusion

Phosphorus glass removal

Hydrogen passivation

Anti-reflection coating

Metal printing (rear and front) and firing

Cell testing

MODULE AREA

Cell interconnection into strings

Module lay-up

Lamination

Module testing

Framing

Diode housing and external wiring assembly

Safety testing

The growth furnaces are highly automated, so that several furnaces can be operated simultaneously by one operator. One of the features of the equipment that makes this possible is an automatic feedstock replenishment system which monitors the weight of the growing tube and replenishes the melt. In order for this equipment to operate properly all feedstock must be within a certain particle size range. Prior to this program, silicon feedstock was manually sorted through a series of sieves.

The EFG growth furnace itself is largely constructed of graphite. Commercial grades of graphite available for furnace construction can contain harmful impurities, and these must be removed by careful processing of all furnace parts before assembly into a growth furnace. The levels of impurities in EFG wafers are very dependent on the effectiveness of the graphite purification process.

During growth of the EFG tube, the hot portions of the tube are surrounded by an atmosphere of argon to prevent oxidation of both the silicon and the graphite furnace parts. A small amount of carbon monoxide (CO) has sometimes been added to improve the electronic quality of EFG wafers. The mechanism by which CO sometimes improved the wafers is not fully understood; it may be related to the interaction between oxygen and carbon defects in the silicon, the pinning of dislocations, and/or the gettering of metallic impurities. However, the use of CO also has detrimental consequences in high-volume manufacturing. For example, the reaction of CO with silicon can form volatile silicon monoxide (SiO) which condenses to form fibrous deposits on the cooler zones of the furnace.

After an octagon tube is removed from a growth furnace, it is transported to another work station where a Neodymium-doped Yttrium Aluminum Garnet (Nd:YAG) laser cuts each face into square wafers, 100 mm in length and width. The laser pulses generates microcracks at wafer edges, and these cracks can propagate and cause the wafer to break during later processing. Efforts are made to minimize the laser-induced damage during cutting.

Cut wafers are etched in a mixture of nitric and hydrofluoric acids. The etching process is followed by phosphorus diffusion to create an emitter layer. The diffusion process is a continuous operation, as opposed to the batch operations used by other PV companies. After diffusion the phosphorus glass is removed with a second wet chemical process. The glass etch batch process used prior to this PVMaT effort was poorly matched to the continuous diffusion and consumed a significant quantity of chemicals that had to undergo costly treatment before discharge.

After glass etch, cells undergo hydrogen passivation and anti-reflection (AR) coating using proprietary technologies. After the anti-reflection coating is deposited, silver contact pads and an aluminum back surface field coating are applied to the rear of the cell, and the silver grid pattern is printed on the front. The grid consists of a number of 100 μm wide fingers and two bus bars which are bonded to cell interconnect tabs. Computer modeling suggested that the grid design prior to this program, containing 32 fingers, was a source of significant series resistance losses.

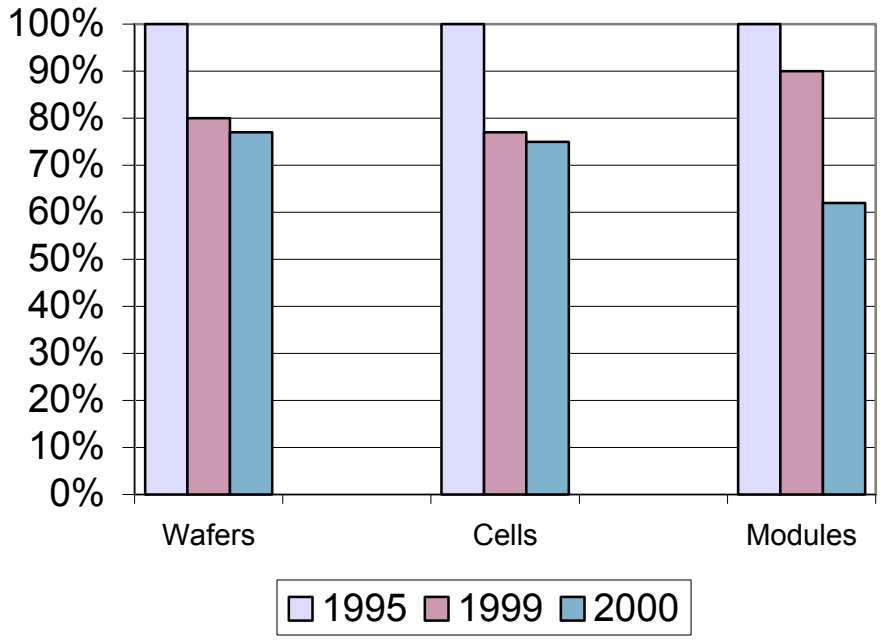
After printing, front and back contacts are co-fired, and each cell is individually tested and binned according to photocurrent at peak power. Cells are interconnected by attaching solder-coated copper tabs by soldering them simultaneously to the front and back of one cell, followed by the feeding out of another length of tabbing and repetition of the process. The sequential nature of the process and the time required to properly heat and cool the solder bonds limit the production rate. Strings of interconnected cells are manually laid-up on a sheet of glass with layers of encapsulant and power bus strips. This lay-up is placed in a vacuum laminator, air is removed, and the encapsulant is melted and reflowed to fill all internal spaces. After removal from the laminator, the ‘laminate’ is tested to ensure that its output power is within specifications.

The module is completed by attaching an extruded aluminum frame, a junction box or diode housing, and electrical cables for connection to other modules. Framing is labor intensive and not readily amenable to automation. The diode housing used on most ASE modules is manually attached to the laminate using an adhesive. The diode housing is a custom-formed part which encloses the protective diodes and dissipates heat generated during their operation. The final step in module assembly is the electrical connection of the laminate to the diode or junction box circuitry, and the attachment of the cables used to connect the modules to one another. The final steps are a power rating test and a high voltage current leakage test.

3.0 PVMaT PROGRAM ACTIVITIES

This Section details the methods used to reduce the cost of ASE modules during the three years of the program, for the process steps identified in Table 1. We first identify the primary accomplishments in the three main areas of Wafers, Cells and Modules here, and then discuss the details in Sections 3.1-3.3 below. Variable (direct) cost reductions accomplished as a result of these technology improvements in the manufacturing of modules are summarized in Fig. 2. Here we break down the module variable cost into add-on costs in each area, and indicate the percent reduction that has been accomplished through technology advances already implemented (year 1999 bar), and those which will be introduced within the next year (year 2000 bar). The baseline cost in 1995, at the start of the program, is normalilzed to 100%. To date, we have implemented variable cost reductions totalling 20% in Wafers, 23% in Cells and 10% in modules. We anticipate that additional reductions of 3% in Wafers, 2% in Cells and 18% in Modules will result by the year 2000 from technology advances made in PVMaT 4A2.

Figure 2. Add-on variable cost reduction for PVMaT 4A2 program by manufacturing area for ASE Americas' modules.



Wafers

Sorting of silicon feedstock. The sorting operation has been converted from a manual operation to an automated process, providing significant savings in labor, an improved level of safety, and a reduction of the potential for contaminating the feedstock.

Growth of EFG octagon tubes. Improvements in the graphite purification process have resulted in an improvement in the electronic quality of EFG wafers. An enclosure to prevent air leaks into EFG growth furnaces was built and tested, but its design was found to be inadequate for use in production. Process variable optimization studies identified the optimal growth speed that balances material quality and production rate. Impurity analyses were developed to provide rapid determination of sources of wafer contamination. Additions of carbon monoxide during crystal growth were terminated after tests showed little improvement in wafer quality. Run length increased after furnace component modifications were made which prevented the accumulation of unmelted silicon pellets and reduced oxidation of the graphite dies. The thickness of typical EFG wafers was reduced from 300 μm to 275 μm, while maintaining similar yield in cell and module fabrication. However, wafer production at the program goal thickness of 250 microns was not implemented because of low yields for these thinner wafers in downstream cell and module processing.

Laser cutting of tubes into wafers. Initial tests with a low-cost, low-maintenance carbon dioxide laser showed promise, but cutting conditions were not optimal. Evaluation of a copper vapor laser indicated that this laser technology is not yet practical for production use. Changes in the optics of the cutting station have been demonstrated which have doubled the current cutting rate on an experimental basis. Experimentation has shown that cutting can be accomplished with much lower levels of edge damage than that produced by the current generation of lasers. A new design of the gas assist nozzle has been successfully tested. This will help to improve yields in cutting 250 micron thick octagons. This technology is undergoing further development.

Cells

Phosphorus glass removal. A new approach to the removal of the phosphorus glass layer remaining after diffusion has been demonstrated both in the laboratory and on the production floor. The new process reduces chemical, waste treatment, deionized water, and labor costs, and streamlines material handling. A prototype unit was built which processed wafers continuously, an improvement over the batch process used previously at ASE Americas. A production unit has now been built and is being evaluated in manufacturing.

Anti-reflection coating. Development work was carried out on a textured anti-reflection (AR) coating. Unlike standard AR coatings used in the PV industry, this coating would be relatively thick and textured to produce a matte surface on multicrystalline silicon surfaces similar to that produced by alkali etching of single crystal silicon surfaces. The coating did not provide any improvement over the standard doubled-layer EFG AR coating, and work on it was discontinued.

Metal printing and firing. Firing conditions for the current metallization pattern have been optimized, resulting in a gain in cell efficiency to over 14% on many production lots. Equipment for increasing the number of fingers in the emitter grid has been tested and shown to provide a benefit in cell efficiency. It is now being evaluated in production. To date, we have not been successful in reducing finger width through work with vendors to develop modified silver pastes for the front metallization. This work is continuing.

Modules

Cell interconnection into strings. Experiments were carried out to increase the cooling rate of solder bonds during interconnection. Throughput improvements of as much as 50% have now been demonstrated.

Lamination. We have successfully implemented a process in manufacturing which reduces lamination time by 30%.

Framing. A mounting system eliminating the standard module frames was demonstrated.

Diode housing. A new diode housing has been developed. All required environmental tests have been passed, and UL certification obtained. It will be introduced into production in 1999.

Module design and encapsulants. A new module design has been developed and demonstrated in which most of the light which falls in between cells in the module is redirected onto the cells. Increases in module power of as much as 20% have been demonstrated for a given cell area. Work on this concept was not finished because of the inability to obtain reflector materials. A number of new encapsulants have been evaluated and two have been chosen for further development and testing.

3.1 IMPROVEMENTS IN EFG WAFER PRODUCTION

3.1.1 Reduction of Wafer Thickness to 275 Microns

Silicon is one of the most costly materials in an ASE module. Reduction in wafer thickness reduces silicon materials content and can also increase cell efficiency by increasing the collection of photogenerated current.

It is challenging to decrease EFG tube thickness. Although tube thickness can be changed by varying the temperature of the tip of the die during tube growth, small changes in temperature can introduce stresses in the growing tube that cause it to buckle. In addition, the thickness of the wall of the octagon tube is not uniform around the perimeter of the tube because of temperature non-uniformities caused by magnetic field asymmetry and variations in hot zone graphite electrical properties. Reducing the average thickness reduces the thickness of the thinnest face to a point where it may cause growth instability, or later leads to mechanical losses when the tube is cut into wafers. Thus, a central part of the program work to reduce average wafer thickness was to improve the thickness uniformity through various modifications of the hot

zone configuration in order to reduce the impact of such effects on yield. At the beginning of this program, EFG octagon tube thickness was nominally 300 microns, and the goal for Phase III was to reduce thickness to 250 microns. We first set an intermediate goal of 275 microns, and planned to stabilize production throughout cell and module fabrication at acceptable yield levels before reducing thickness further. This was done during during Phases I and II. In Phase III, we evaluated 250 micron wafer production and processing.

The initial reduction to 275 micron thickness was achieved in several steps. In the first step, one production EFG furnace was converted to growth of the thinner tubes. An immediate improvement in cell efficiency was observed for material cut from those tubes, with improvements up to 0.5% in absolute efficiency on an individual tube basis. Production yields appeared to be only 1-2% lower throughout wafer and cell manufacturing, but higher breakage rates were observed during cell interconnection. This experiment was continued for three months. During those months, a fuller understanding of the effects of thin material growth was obtained.

With a larger quantity of data, it was found that 275 micron material did have an efficiency advantage of about 0.2% absolute over 300 micron material. Wafer yield losses during crystal growth and laser cutting of wafers due to breakage were no higher for the 275 micron material than at the 300 micron thickness. However, initially the thinner material was not as flat, leading to a 2-3% higher rejection rate than for 300 micron material. However, continued modifications of temperature profiles in the post-growth region reduced this yield deficit for the thinner wafers. Finally, the entire production line was turned over to growth at 275 microns at the end of Phase II. Manufacturing with this thickness of EFG wafer now has been going on for over one year. All of the improvements expected at the beginning of the program have been fulfilled: a reduction in silicon usage combined with an increase in cell efficiency, accomplished without a negative impact on production yield.

Growth and cutting of 250 micron tubes were investigated in detail in Phase III. Yields for this material were often inconsistent due to fracture of the thinner tube faces during laser cutting. On tubes without large circumferential thickness variations, cutting yields were normal, but there was an increase in the number of wafers not meeting pre-set flatness criteria. When larger numbers of 250 micron thick EFG were grown and cut, problems arose in downstream processing, mainly in handling steps and interconnect. These issues are not yet resolved, and have prevented introduction of the 250 micron thick wafers into manufacturing before the termination of this program.

3.1.2 Improvements in the Growth of EFG Octagon Tubes

Development of a Particle Separator for Silicon Feedstock

The silicon feedstock used to replenish EFG furnaces during octagon growth is sorted both to remove silicon particles that are too large to flow smoothly into the die during the replenishment operation and also to remove very fine particles, or dust, which has a tendency to float on the surface of the molten silicon and contributes to the formation of 'mushrooms'. Prior to the beginning of this PVMaT subcontract, the sorting operation was performed manually, using a series of sieves. Over time, the quantity of silicon used for EFG growth had increased greatly, as did the labor requirements. In addition, the relatively small fraction of material that had to be removed according to the starting specification was accumulating, and represented a significant cost of material that was not used for EFG growth. During Phase I, experiments were carried out to determine whether particles in the ranges considered to be out of specification could be tolerated in the growth system if their concentrations were low. This was found to be true, which led to the development of a procedure for blending rejected material back into the feedstock destined for crystal growth, while keeping tight control over the concentrations of particles in the various size ranges. This procedure greatly reduced the amount of material which was not usable in crystal growth, but it required an amount of sieving that became onerous if performed manually. Therefore, a task was begun to design and build a mechanical particle sorting machine that would permit automation of the new procedure.

A consulting engineering firm studied the problem and recommended the purchase of a commercial sieving machine. A sorting machine was first rented and outfitted with appropriate sieves, and the sorted feedstock material was used to grow octagon tubes on one production EFG furnaces to compare it to the standard propduct and to check it for contamination effects. The machine operation was acceptable. Wafers produced from the feedstock material used in the test were processed into cells with efficiencies equivalent to those of cells produced from feedstock which was manually sorted. This initial trial resulted in some design modifications, and the sorting machine was purchased and permanently modified for use in the EFG wafer manufacturing. The more effective sorting performed by the new machine has permitted the use of a higher percentage of silicon feedstock material than was possible using the manual sorting method, while reducing the labor costs associated with sorting.

Improvements in graphite purity

Extensive testing of various grades of graphite from different vendors, and several graphite purification processes, were conducted during Phase I of this program. This testing consisted of both spectroscopic measurement of impurity levels in the various grades, and the fabrication of the purest of these grades into furnace components for correlation of cell efficiency with material type. As a result of these studies, several graphite grades and two purification methods were qualified for production use.

In Phase II, in-depth testing of the purification process was carried out to compare the purification processes of two vendors. Significant differences in cell efficiency were not observed when wafers from furnaces purified by the two different vendors were made into cells. This allowed us to accept a second vendor as a qualified source for purified graphite.

Solar grade silicon

An attempt was made to reduce the cost of EFG wafers by relaxing the specification for the feedstock silicon material from higher grades to the least expensive solar grade. After an initial evaluation that did not show any clear difference in cell efficiency as a result of the use of the less costly grade, a large fraction of production was converted to the use of solar grade material. While this resulted in a cost savings on raw materials, the larger body of data accumulated by the use of solar grade material in full production showed an efficiency shortfall of several tenths of one percent absolute in cell efficiency, which negated the savings on materials cost. As a result, the feedstock was changed back to the higher grades. The information obtained in the experiment will continue to be useful, however, as prices and availability of the various grades of silicon change in the future. Particularly during periods of silicon shortages of higher grade materials, the difference in price between the different grades might justify the use of the lower grade material.

Furnace component improvements

A particularly difficult problem which has affected EFG crystal growth has been the problem of unmelted silicon feedstock in the central portion of the EFG die/crucible, called ‘mushrooms’ from their appearance after solidification. The presence of mushrooms in the crucible disturbs the thermal uniformity of the melt, causing some faces of the octagon tube to grow thinner than others, and can eventually cause ‘voiding’ of the growth, where one of the faces separates from the die tip. Then growth must be stopped. The growth of mushrooms eventually leads to unacceptable temperature variations around the perimeter of the die, the termination of a growth run, and the need to replace the die.

A number of modifications of the EFG furnace aimed at reducing the mushroom problem were tested in our PVMaT program. A substitution was made for the material of one of the furnace components in contact with the silicon melt, in order to reduce the tendency of semi-molten feedstock material to stick to it. In addition, the mechanism that disperses feedstock into the melt during replenishment was changed to reduce the tendency of feedstock to accumulate on one of its components. As a result of these changes, improved die designs were demonstrated, and the length of growth runs was increased by 50%. This has contributed significantly to improved productivity in the crystal growth area

Engineering of an Enclosure for EFG Furnaces

Wafer quality is affected not only by the purity of materials intentionally placed inside the furnace, but also by impurities that infiltrate into the furnace from the ambient air. Exposure of EFG tubes to the environment can cause other problems as well, e.g. tube nonflatness due to air disturbances and incorporation of air into the growth furnace where it leads to oxidation of graphite parts. Protection of the furnace and growing tube from the environment would improve the quality and consistency of EFG wafers.

During Phase I an enclosure for EFG growth furnaces was designed. A prototype enclosure was constructed and tested in Phase II. There were initial problems with tracking of the bellows enclosure and with completely purging the air from the system. After these problems were fixed, air was still found to leak into the system from several points, and the growth conditions were not improved over those without the enclosure. Octagon tubes grown in the enclosure were not of higher quality than tubes grown without the enclosure. Since benefits were not demonstrated, testing of this concept was terminated.

3.1.3 Research into Laser Cutting of Tubes into Wafers

One of the major causes of breakage of EFG wafers thinner than 250 microns is the presence of cracks caused by the laser cutting process by which the octagon tubes are converted into wafers. There are two aspects of the cutting process that cause these cracks. The first is the mechanical force exerted on the tubes during the cutting operation by the assist gas jet which is directed at the cut to eject the material melted by the laser. The second is the thermal stress induced in the vicinity of the cut by laser heating and by the resolidification of silicon in the region of the cut, which produces microcracks. While both of these problems affect the yield of EFG wafers of any thickness, they cause much greater difficulties with thin wafer growth. Therefore, these problems need to be addressed in order to be able to make thinner wafer production viable .

The first part of this work was focussed on reducing the mechanical stresses on the wafers caused by the assist gas. A number of design studies were carried out on the gas flow in the nozzle supplying the gas to the cut area. These have led to radical new configurations for the nozzle which have produced improvements in the cutting process. These improvements allow new laser technology to be evaluated which previously could not be used with the old nozzle designs.

One important goal of the laser program was to increase cutting speed. Speed can be increased by using more powerful lasers, but such lasers are more expensive than the lasers currently in use, and the increased power can lead to an increase in the extent of microcrack formation in the region of the cut. Another approach is to improve laser beam focussing. Experiments were carried out on this approach by introducing a new lens system to modify the laser beam. In tests conducted at a laser vendor's facility, this new lens led to a doubling in cutting speed with no degradation in cut quality. This increase in cutting speed would result in a throughput increase of 25-30% after accounting for time to position the tube and remove cut wafers. Other lens designs were demonstrated which have the potential of increasing the cutting speed by a factor of four.

We plan to continue evaluating the new approaches to laser cutting technology which have been opened up by these developments beyond the end of this program.

Work was also conducted on the task of locating a robust laser which could produce a higher quality cut, with a minimum of microcrack formation in the edge of the cut wafer. This is an important goal, because currently ASE Americas chemically etches all wafers to blunt the cracks caused by laser cutting, and the elimination of this step would result not only in a large cost savings, but also a large reduction in consumption of etch chemicals. A number of experiments were performed with a laser which was expected to produce higher quality cuts than the Nd:YAG lasers in current production. The new laser, which uses shorter pulses at higher power densities, was shown to produce cuts with much less edge damage. Although micro-cracks were still formed, they were much shorter, and could be blunted with much less chemical etching. At the completion of testing of the new laser, it was concluded that it was not yet practical for use in a manufacturing environment, but the testing had identified pulse parameters which were necessary to achieve the desired results. This information has been used identify and acquire a short pulse length laser for future experimentation.

3.1.4 Strengthening of EFG Wafers Without Chemical Etching

In lieu of reductions in chemical etching that might be possible with improved laser cutting, wafer strengthening was attempted using mechanical lapping of the wafer edges using an abrasive slurry of the type used to commercially polish silicon wafers. Several methods which were tried did not show promise, and this work was terminated.

3.2 IMPROVEMENTS IN EFG CELL PRODUCTION

3.2.1 Evaluation of Textured Anti-reflection (AR) Coatings

One of the disadvantages that multicrystalline silicon materials such as EFG face when compared with monocrystalline silicon as a substrate for photovoltaic cells is the inability to texture the surface by chemical means. Work was performed during this program to attempt to produce the benefits of a textured surface on multicrystalline EFG wafers by applying a textured coating to the surface of the wafers. An attempt was made to reproduce the results achieved in a study at Sandia National Laboratories, in which cells coated with textured layers of zinc oxide (ZnO). For the ASE Americas study, a number of cells were coated with the same material at the laboratory of Professor Roy Gordon at Harvard University. The cells in the ASE study were not improved significantly by the addition of the coating, although improvements of as much as 0.5% absolute were reported under similar conditions in the Sandia study.

As part of the effort to explain the lack of improvement in the ASE cells, a number of cells produced in the study were sent to Harvard and Sandia for analysis, where the reflectance and transmittance of the ZnO films were measured, the texture of the ZnO film texture was observed by scanning electron microscopy, and modeling was carried out to determine the reflectance

levels which would be expected for the observed texture. The conclusion from the tests was that the textured film was performing as expected, but its performance was not appreciably better than that of the standard ASE AR coating, because ASE's standard coating was unusually effective. Thus, it was concluded that further work in this direction would not be productive, and the study was ended. It was further concluded that the difference between the ASE results and those obtained in the earlier work at Sandia was due to the poorer performance of the titanium dioxide AR coating used as a control in the Sandia work as compared to that of the ASE AR coating.

The project on development of the textured coating had been a major part of the planned effort on this subcontract to increase cell efficiency to the order of 15%. In order to be able to meet projected cost decrease goals for the program without it, it was necessary to redirect resources budgeted for this work toward the development of an alternate technology which promised increases in cell power. We therefore initiated modeling work on a new module technology. The modeling indicated that a flat-plate concentrator module design which had been under consideration would provide enhancements in module power. Work on that project is described in Section 3.3.6 of this report.

3.2.2 Optimization of Cell Processing

As part of an ongoing program of product improvement at ASE Americas, cell samples were sent to laboratories at Georgia Institute of Technology (GIT) and University of California at Berkeley (UCB) for analysis of the levels of impurities in EFG wafers at various steps in the production process. Initial tests indicated a measurable increase in the level of impurities after processing, suggesting that wafers were being contaminated. Further tests revealed that the impurities accumulating in the wafers were primarily iron and nickel.

The problem was addressed by a two-pronged approach: an effort to develop new processes and equipment that would not require wafers to contact metal components, and an attempt to find substitute materials for the components suspected of causing the contamination in the standard production equipment. One candidate for a new process was the use of Rapid Thermal Processing (RTP), based on encouraging results obtained in an ongoing development program at GIT, including the production of 1 cm^2 EFG cells with efficiencies of 16%. As a result of this encouraging work, we are planning to continue investigation of RTP in the future.

Meanwhile, a search had been initiated for new materials for the standard process equipment. Samples of several candidate materials were obtained and exposed to temperatures typical of the highest temperature processes to evaluate any tendencies for the materials to change from this exposure. Analysis was performed to determine whether the material producing the lowest contamination would have the mechanical properties at high temperatures required in order to use it as a direct replacement for the metal components in the standard equipment. This analysis was encouraging and we have started to evaluate process equipment components made from several of the candidate materials we have identified for future testing. This work was not completed as of the end of this program.

3.2.3 The Development of a New Process for Phosphorus Glass Removal

As is typical for any diffusion process on silicon wafers, the diffusion process at ASE Americas leaves the wafer surface coated with a silicate/phosphate glass, which must be removed prior to any further processing. At ASE, this has traditionally been accomplished by wet chemical etching of the wafers, which are held in carriers in an acid bath. The need for the use of carriers presents a handling difficulty, since neither preceding nor following process steps require the use of carriers. In addition, although little acid is consumed by chemical reaction during the process, the bath must be replaced periodically. The disposal of the spent acid is costly, since it requires treatment before it can be discharged, and removal of the fluoride that it contains is expensive.

ASE developed a concept of an alternative process based on the use of acid vapor, which could be carried out on wafers as they are transported by belt from one processing area to another, eliminating the need for carriers and a great deal of manual handling. The task of studying the feasibility of designing such a process and developing equipment to carry it out was subcontracted to an outside vendor. They demonstrated the effectiveness of the method by successfully processing a number of EFG wafers coated with phosphorus glass, using bench-top apparatus which demonstrated the principles that could be used in a machine capable of continuous processing. As a result, the decision was made to build a prototype unit capable of continuous processing at the rate required to match the throughput of the cell line at ASE Americas. Test results with the prototype indicated that the vapor etch process was working as expected, but that major improvements would be needed in the rinsing process to remove all of the etch residue. Those early tests indicated that cells processed in the new unit had slightly lower efficiencies than those processed in the standard equipment on the ASE Americas production line, a problem which was attributed to inadequate rinsing. Chemical consumption was found to be reduced by even more than the 98% which had been projected for the unit, indicating an extremely high efficiency in the utilization of the hydrofluoric acid etchant. A number of design improvements in the original vapor etch concept were worked out. A pilot unit was built and is undergoing testing in a production environment at this time. This work was not completed as of the end of this program. We expect that full benefits from this new concept will be realized after the pilot testing is completed in the next 4-6 months.

3.2.4 Optimization of Metal Printing and Firing

<u>Optimization of the Front Grid</u>

The width of the silver fingers used in the front grid pattern on the cells currently manufactured at ASE Americas is approximately 100 μm; the narrowest fingers achieved in developmental engineering work at ASE is approximately 60 μm. If those narrower fingers could be produced consistently on the manufacturing line, the resultant reduction in shadowing would increase cell efficiency by about 0.2% absolute. A computer study showed that if, in addition, the number of fingers in the grid pattern were increased from 32 to 40 or more, the reduced spacing between the fingers would reduce series resistance losses in the cell emitter and raise efficiency by an additional 0.1-0.2%.

The difficulty in achieving this overall objective lies mainly in the flow properties of commercially available thick film silver pastes designed for use on PV. During the course of this program, ASE Americas discussed the necessary changes with several manufacturers of silver paste. Unfortunately, while some of the sample pastes provided to ASE by commercial vendors to date have produced good results in developmental work, they not been consistent enough to use in manufacturing. At this point, the pay-off in cost reductions with this aproach is still attractive and we are still continuing to work on this problem .

In parallel, a grid modeling program was obtained from Sandia National Laboratories and used to model the standard ASE Americas design, and the results obtained from the new model indicated that an efficiency improvement of about 0.2% absolute should be achievable by increasing the number of grid fingers without changing line width. This allowed the problem to be approached as two independent steps, a change in line width and an increase in the number of fingers, which could be carried out in any order.

In order to test a grid with a larger number of fingers, it was necessary to machine a new printing head for the ASE machine, and run tests on the production line itself. In the first of those tests, over 4,000 cells were printed with the new grid design. The test showed an improvement for the new grid, but it was only about one-half of that predicted by the model, apparently because the additional contact area caused an increase in reverse leakage. Introduction of the new grid was therefore not undertaken for the current cell line. However, we have recently started to manufacture larger area cells with 40 fingers, for which the increased grid coverage is essential to maintaining parity in efficiency with the smaller area cells.

3.2.5 Statistical Process Control

During the course of this PVMaT subcontract it became apparent that improvements in average cell efficiency would be difficult to achieve without first putting into place better methods to analyze variations in cell performance on the production line and relate them to production conditions. Accordingly, it was decided to implement a program of Statistical Process Control (SPC), under which data would be collected at each process step and fed into a database for analysis.

As a first step in implmenting SPC, we acquired software permitting cell test results to be accessed by all members of management and the engineering staff from the ASE personal computer network. As another component of the system for collecting information, bar code printers and readers were installed in both the crystal growth and cell fabrication areas. In the crystal growth area, this allowed the collection of critical information on furnace components, such as the reactor used for purification and purification date, for every growth run. This data was then made available for correlation between such variables as purification process and cell efficiency. In the cell area, the use of bar code readers permitted cell processing data, such as sheet resistivity, to be recorded immediately in digital form, instead of on paper. This eliminated the need for tedious searching through paper records to follow trends in production data.

A second step in the SPC program was development of a format and structure with which to carry out Design of Experiments (DoE) matrices and analysis for cell processing. A consultant was used to set up and direct large-scale optimization experiments. We have carried out several of these on the program and are learning which process variables have the most impact on cell efficiency in order to help us to raise cell performance. This work will continue beyond the end of this program in order to implement SPC methodology throughout the ASE manufacturing line.

3.2.6 High Efficiency Program

As a result of incremental improvements in the production line, cell efficiency has been improved over the course of the three years of the program. One of the largest improvements was seen as a result of reducing average wafer thickness to 275 μm, which raised average efficiency by 0.2% absolute. Improvements in the purity of the silicon available for crystal growth also has helped. Lots of EFG cells now are being produced at average efficiencies of 14.1-14.2%. About 30% of the cells in those lots have average efficiencies equal to or greater than 14.35%. We estimate that overall cell improvement in the course of the program which has been implemented in manufacturing is about 0.5% absolute.

3.3 IMPROVEMENTS IN ASE MODULE PRODUCTION

3.3.1 Increases in Lamination Throughput

One of the goals of this subcontract was to achieve a reduction in the time required for module lamination, which would reduce the need for expensive capital equipment and its associated floorspace requirements. The need for this improvement arose from differences in flow properties between the proprietary encapsulant material used at ASE Americas and the EVA material used by other manufacturers. Although the ASE encapsulant has been demonstrated to possess better resistance to degradation during outdoor exposure than EVA, it burdened ASE with a competitive disadvantage in the form of lower throughput in the lamination process.

At the beginning of Phase I of this subcontract, work was carried out to investigate a number of alternative materials and processes which might permit faster lamination cycles. While some new processes and methods were evaluated, it was found the financial risk involved in purchasing new equipment for production use were too high. As a result, renewed attention in the program was focussed on improving the throughput of ASE's current equipment and materials before making the large expenditures required to pursue the new ones. This has been very succesful. A process for producing 50-watt modules first was demonstrated, which shortens total lamination time by 30%. The process next was adapted and implemented for production of the 300-watt module.

3.3.2 New Encapsulants

In addition to the work described in the previous section, we carried out investigations on new and modified encapsulants on this program. Our search had two purposes. First, we wanted to raise the yield of thinner cells in module fabrication by reducing stresses on the cells during lamination; second, we wanted to extend prospective module lifetime in the field to greater than 20 years. The latter involved for a search for an encapsulant that could improve on the one we presently use.

The first of these programs involved an investigation into the use of liquid encapsulants which would harden through the application of high temperatures or light. Such encapsulants were commonly used by manufacturers of photovoltaics twenty years ago, but their use was largely discontinued once vacuum lamination using EVA became standard practice in the industry. Because of the anticipated costs of adding more vacuum laminators as production volume increases, which would not be necessary using this process, and the broad range of new materials developed in the polymer industry during the past two decades, it was considered prudent to reinvestigate this approach.

Work was subcontracted to a consultant to develop a number of test formulations of liquid-based encapsulants to determine the properties of these materials. Sample coupons were prepared using EFG cells and a variety of test formulations. As a result of extensive testing in this area, we located a liquid encapsulant which appears to have the stability we require under UV exposure. We next developed methodology and procedures with which to make 50 W modules. Several of thse have been made for this program and are undergoing reliability testing. We plan to continue to work with this encapsulant in order to test its compatiblity with other module materials and solar cells, and develop approaches with which to reduce process costs in large scale manufacturing.

In parallel with the work on the liquid encapsulants testing was also conducted on variants of ASE's standard encapsulant material. One of these was shown to be very attractive. The two major improvements offered by this new material are higher clarity, with lower haze, and improved resistance to loss of light transmission during exposure to UV light. Test samples of the new material were prepared and result of this testing have now shown conclusively that the new material shows a high level of stability and a lower transmission loss than all other materials tested, and clearly superior to ASE's proprietary encapsulant and EVA. Modules manufactured using the new material were placed in outdoor testing in Florida to attempt to confirm these results, and as of the end of the program results received on these modules are consistent with the results of the accelerated indoor testing. We have secured access to production quantities of this new material in the meanwhile, and plan to introduce it into manufacturing.

3.3.3 Reduction in Materials and Labor Costs of Module Framing

During Phase I an effort was made to identify frame constructions which would be less expensive than the industry-standard frames made of extruded aluminum and at the same time reduce the time required for assembling frames to modules. The most promising alternative construction found during this search was one in which the frame is made of roll-formed metal, rather than extruded metal. Only one of the proposed designs was found to be sufficiently stiff for ASE's large 300-watt module. However, a cost advantage in switching to the new design was not demonstrated, so this approach was not pursued further.

Another approach to achieving a substantial cost reduction over conventional frames is the concept of eliminating the standard configuration. The logic of this approach is that good structural engineering practice dictates that no structure should contain multiple load-bearing elements that carry the same load. The frames of PV modules are generally designed to provide support for all of the wind loads to which the modules are subjected, but the support structure to which the frames are mounted must carry exactly the same loads. That being the case, small mounting brackets which transfer wind loads from the module to the underlying structure perform the same function as the large frames, but at much lower cost. Initial design work has been carried out to engineer several designs: in one case, a mounting bracket that would be compatible with ASE modules, and would provide mounting locations compatible with standard ASE frames; in another case a glue-on frame to attach only to the back sheet of the module. Prototypes of frameless modules have been fabricated and have performed with very promising results in preliminary testing. We are carrying on this work and are in the process of developing final manufacturing concepts for these new designs

3.3.4 Reduction in Cost of Diode Housing

The large 300 W module manufactured by ASE Americas is most commonly supplied with electrical quick connectors to provide connections between modules. Therefore, it does not require a junction box *per se.* However, it does require diode protection to minimize problems associated with hotspot heating due to uneven illumination. The protective diodes are mounted on a circuit board enclosed in a housing on the rear of the module. A large part of the housing cost arises because of the use of an extruded and machined aluminum cover on the housing, which provides a heat sink which dissipates the heat generated by the diodes during the rare instances when they are operating.

A reevaluation of this design was called for in response to new customer demands. This prompted a review of the diode assembly, which resulted in the discovery of an opportunity to change the configuration so as to reduce the heat load. The new design was tested both indoors and outdoors and found to function as predicted, while meeting all requirements for certification. Due to the reduction in heat load, the requirements for heat dissipation using this design were reduced as well. This permits the elimination of the aluminum radiator, to provide a substantial reduction in the cost of such a design. All environmental testing and certification of the new diode housing have been completed, and plans for immediate introduction into manufacturing are being formulated.

3.3.5 Replacement for Module Back Glass

One of the most expensive materials in the standard ASE double glass module configuration is the sheet of back glass. Its cost is escalated by a hole drilled in the back to provide an exit for the wires. We have alternatively used an aluminum sheet, which bonds very well to our proprietary encapsulant, in the standard ASE 50 Watt module design. However, this had not been practical to use in the larger ASE 300 Watt module. In this program, we undertook to find low cost options to the back glass. One composite soft backskin material has been developed and shown to have compatibility with other aspects of module construction. It has been structurally and environmentally tested in both the 50 W and the 300 W configurations and has passed all requirements. We are planning to introduce it into manufacturing in the near future.

3.3.6 New Flat-Plate Concentrator Design

As was described in section 3.2.1 of this report, an effort was made during Phase I to develop a textured coating that would enhance the collection of light at the cell surface, and this effort was ultimately unsuccessful. As a redirection of the program in order to replace the loss of this avenue for cost reduction at the end of Phase 1, a new concept was developed for reducing cost of the module. This addressed improvement of the collection of light, but on the module level, rather than the cell level, by allowing the efficient collection of light from the spaces between cells in the module. We determined that the new module concept had the potential to increase the amount of current collected by a given number of cells by as much as 50% or more, depending on the size and geometry of the cells. Accordingly, the resources that had been earmarked for the completion of the cell texturing work were redirected toward the new module design, which has been designated a Flat-Plate Concentrator (FPC).

The principle of the FPC is that light that strikes in between cells is reflected by a highly reflective surface, and the redirected light rays then strike the interface between the glass and the surrounding air, which reflects them once again, this final time in the direction of a nearby solar cell. The advantage of the new FPC design over older, similar, proposals, is that it collects light from a distance of 20 millimeters or more, and at a much higher efficiency than is possible with conventional backskin materials.

One problem with early trials of the concept was that it was not possible to eliminate all air bubbles from the laminates. However, even with those defects, the large improvements expected for the FPC design were clearly demonstrated. A first series of coupons exhibited improvements in collected power of an encapsulated cell of as much as 22% over that obtained with the same cell before encapsulation. In the second series, the improvements ranged up to 25%. A number of small modules were then made for demonstration purposes, and were shown to potential customers, who responded enthusiastically to the new design.

The major task in reducing the FPC concept to practice in module manufacturing was in locating a supplier who could produce the required reflective material in the form of large sheets. Such a supplier was eventually located, and work was carried out to design and build the tooling for producing module-scale sheets of reflector material. This tooling was successfully completed on schedule. However, the material produced on that tooling exhibited poor bonding to ASE's encapsulant during pre-testing, and application of the final reflective coating was delayed while a solution to the adhesion problem was sought. Unfortunately, that solution has not yet been found as of the end of this program. ASE is, however, continuing to develop the FPC module, and plans to incorporate it into its future product line.

4.0 SUMMARY AND CONCLUSIONS

The three-year program at ASE Americas under the PVMaT 4A2 Initiative has been successful in achieving the cost reductions anticipated at the start of the program. The cost reductions result from the achievements made in each of the manufacturing areas of the company: Wafer Manufacturing, Cell Manufacturing, and Module Manufacturing.

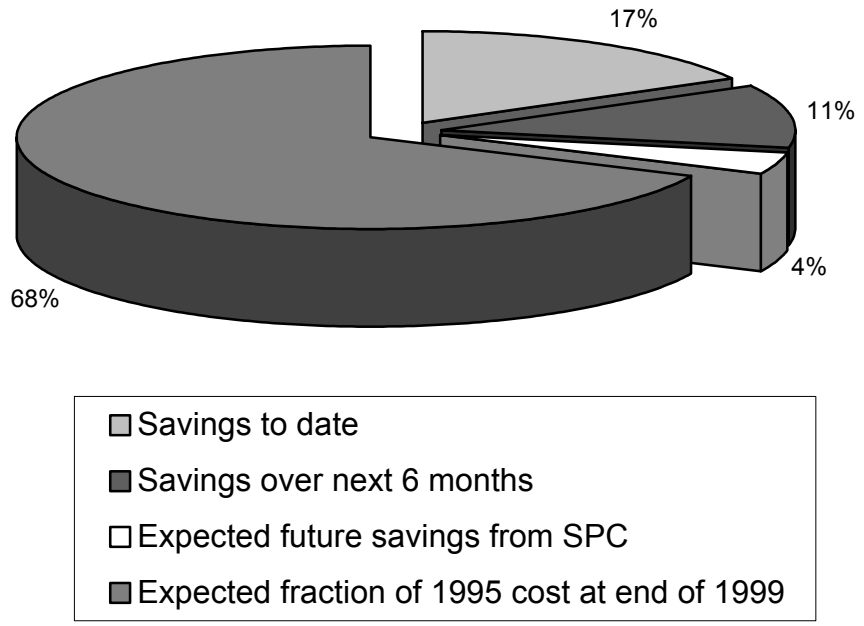
In Wafer Manufacturing, the cost reductions result from a doubling in the length of growth runs, leading to a reduction in the cost of furnace components, and also to an even more valuable increase in the uptime of this capital equipment. The introduction of an automated silicon sieving process has resulted in an improved utilization of silicon feedstock material, and a reduction in labor costs. Most importantly, the reduction in EFG wafer thickness from 300 microns to 275 microns resulted not only in a reduction in silicon cost, but in a measurable improvement in average cell efficiency. In total, the combined cost savings from these three improvements amounts to 20% of the add-on wafer cost at the beginning of the program, which is equivalent to 6% of module cost.

In Cell Manufacturing, cost reductions resulted from an improvement in cell efficiency of 0.5% absolute on cells using the standard grid design, and a further improvement of 0.2% on 150 mm^2 cells using the new 40-finger grid design. Further cost reductions have resulted from the use of the new vapor etch process for removing the phosphorus glass after diffusion, and from an increase in cell yield due to improvements made due to the introduction of SPC monitoring of production processes. In sum total, these savings represent an add-on cost reduction in the cell manufacturing area to date of 25%, which represents 7% of module cost.

Finally, in Module Manufacturing, costs have decreased to date by about 14% due to the introduction of the improved diode housing and the improvements in lamination, which have increased both production throughput and manufacturing yield. This amount represents 4% of the total cost of producing modules, when wafer and cell costs are included.

Thus, the improvements already implemented on the ASE manufacturing line total about 17% of the cost of module production at the beginning of the program. This amount is shown in Figure 3 on the following page, along with other savings detailed below. The value of 17% is somewhat lower than the original goal of 25%. However, this does not include all of the improvements which are ready for manufacturing, nor the further cost reductions which will result from programs initiated under this program, but which will reach the production floor in the time frame of 6 months to one year in the future. The most immediate of these further cost reductions will occur due to the production of modules with adhesively bonded mounting supports instead of conventional aluminum frames, and the introduction of large 300 W modules which use a composite backskin instead of glass as the back element in the module construction. Development on both of these products is complete, and modules using the new designs have been sampled to customers and installed in the field. The products have now completed all environmental testing, and all certifications (UL, IEEE, IEC) from testing laboratories have been received. When these products are introduced, they will incorporate a reduction of a further 11% in overall module cost. That will bring the total reduction in module cost resulting from this program to 28%, exceeding the original goal of the program.

Figure 3. Variable Cost Reductions Resulting from the PVMaT 4A2 Program



In addition, several programs will have payoffs which will not be felt for more than six months. The sum total savings resulting from these programs will be significant. A further decrease in EFG wafer thickness to 250 microns is still planned, along with improvements in the wafer-cutting lasers to make this goal possible. Those laser improvements will also incorporate an increase in cutting speed, reducing wafer cost still further. The full introduction of SPC in the Wafer Manufacturing area is also expected to improve yield significantly, particularly as a result of improved flatness. Further reductions in Cell Manufacturing cost will also accrue from the further implementation of SPC and a change in the diffusion equipment which is expected to produce a considerable savings in labor cost. The sum total of all of these improvements is expected to result in a module cost reduction of 4-5%.

Finally, a large reduction in module cost is anticipated from the future introduction of the Flat Plate Concentrator (FPC) module in production. This module is at this point fully designed, but problems arose in the manufacturing of the essential reflector material, preventing its demonstration before the end of the program. It is likely that those problems can be overcome sufficiently to permit the production of demonstration modules during the next few months. However, the amount of time required to solve basic materials issues, such as adhesion, may still be considerable, and such a completely new product will not be introduced without extensive testing. We do not expect to introduce the FPC module as a standard product earlier than six months from the end of this program. When it is introduced, however, this module is expected to reduce costs by a full additional 10% beyond the improvements shown in Figure 3.

Publications and Patents

Publications

1. J. Cao, R. Gonsiorawski, M. Kardauskas, J. Kalejs, C. O'Brien, M. Prince and E. Tornstrom, "EFG Manufacturing Line Technical Progress and Module Cost Reductions Under the PVMaT Program", in *Conference Record of the Twenty-Sixth IEEE Photovoltaic Specialists Conference - 1997,* IEEE, New York, 1997, pp. 1077-1080.

2. M. Kardauskas, J. Kalejs, J. Cao, S. Ebers, R. Gonsiorawski, B. Piwczyk, M. Rosenblum, and S. Southimath, "New Technology and Cost Reductions in the Phase 4A2 and 5A2 PVMaT Programs of ASE Americas", in *NCPV Photovoltaics Program Review,* M. Al-Jassim, J. P. Thornton, and J. M. Gee, editors, AIP, Woodbury, New York, 1999, pp. 686-692.

Patents

Patent applications have been filed for improvements in EFG die design and for the flat plate concentrator module.

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13. ABSTRACT *(Maximum 200 words)*

This report describes the progress made in the 3-year program at ASE Americas, Inc., in the Photovoltaic Manufacturing Technology 4A2 Initiative on developing Edge-Defined Film-Fed Growth (EFG) silicon wafer technology. The work performed under this subcontract focused on advancing EFG manufacturing technology and lowering production costs in three areas:

- EFG wafers – through better silicon feedstock utilization, ASE realized improvements in growth, a wafer thickness reduction from 300 to 250 microns, and a higher bulk wafer electronic quality; additionally, new technology for the laser cutting of wafers was demonstrated;
- Solar cells – by an increase in solar cell efficiency and by implementing a new glass-etch process;
- Modules – by lamination cycle improvements, introducing a new diode housing, and simplifying module construction.

The program will exceed its overall goal of reducing EFG module manufacturing costs by 25%. About 17% of these improvements are already implemented in manufacturing. Technology to achieve an additional cost savings of 11% is in the final stages of introduction into large-scale manufacturing.

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