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Ninth Workshop on Crystalline Silicon Solar Cell Materials and Processes

Extended Abstracts and Papers

Workshop Chairman: B. L. Sopori

Program Committee:
J. Gee, J. Kalejs, T. Saitoh, R. Sinton, M. Stavola, D. Swanson, T. Tan, E. Weber, J. Werner and B. L. Sopori

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National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

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9th Workshop on
Crystalline Silicon Solar Cell Materials and Processes

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R&D Challenges and Opportunities in Si Photovoltaics

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Since 1997, the PV sales have exceeded 100 MW/yr with > 85% of the production coming from silicon photovoltaics (Si-PV). As the PV demands increase in the new millennium, there will be a host of challenges to Si-PV. The challenges will arise in developing strategies for cost reduction, increased production, higher throughput per manufacturing line, new sources of low-cost Si, and introduction of new manufacturing processes for cell fabrication. At the same time, newer thin-film technologies, based on CdTe and CIS, will come on board posing new competition. With these challenges come new opportunities for the Si-PV—to detach itself from the microelectronics industry, to embark on an aggressive program in thin-film Si solar cells, and to try new approaches to process monitoring.

The PV industry has already begun to address the use of thinner Si wafers, dropping from 400 μm toward 200 μm. Such a reduction in the wafer thickness is expected to conserve Si usage with an added advantage of higher cell efficiencies. The test production lots, fabricated with thin wafers, have verified such improvements in the device performance with a reduction in wafer thickness. However, the yield of thin cells is far lower than that of its thicker counterparts. It is expected that automation can mitigate part of this problem. However, it is necessary to investigate the basic mechanisms of wafer breakage. In particular, factors such as sawing, texturing, and warpage by the asymmetric metal patterns, which cause a propensity to breakage, need to be well understood. The final frontier of the thinner cells, the thin-film Si solar cell, is already above the horizon. The transition of this laboratory device into production is a strong challenge.

Process monitoring will be an important issue in the future. The current monitoring approaches are reminiscent of the microelectronic technology and are not well suited for PV. New methods that can yield meaningful results on large-area, textured wafers and cells are needed for process control and monitoring.

On the research side, continued work is needed toward understanding the role of defects and impurities. This understanding is apt to culminate in the fabrication of very-high-efficiency (about 20%) cells using low-cost material. This knowledge is also needed to deal with thin-film cell issues, such as the effects of impurities and defects becoming considerably more important. Other issues are related to metallization and processing that can achieve many conventional processes in one step so as to minimize the number of process steps for solar cell fabrication.

The 9th Workshop on Crystalline Silicon Solar Cell Materials and Processes will address these issues in a number of sessions. In addition to covering the usual topics of impurity gettering, defects, passivation, and solar cell processing, we have included sessions on poly feedstock, mechanical properties of Si, metallization, and process monitoring.

Production of Solar Grade (SoG) Silicon by Refining Molten Metallurgical Grade (MG) Silicon

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ABSTRACT

Pyro-metallurgical refining techniques are being developed for use with molten metallurgical grade (MG) silicon so that directionally solidified refined MG silicon can be used as solar grade (SoG) silicon feedstock for photovoltaic applications. The most problematic impurity elements are B and P because of their high segregation coefficients. Refining processes such as evacuation, formation of impurity complexes, oxidation of impurities and slagging have been effective in removal of impurities from MG silicon. Charge sizes have been scaled up to 60 kg. Impurity analysis of 25 kg charge after refining and directional solidification has shown reduction of most impurities to <1 ppmw and B and P to <10 ppmw.

INTRODUCTION

The photovoltaic (PV) industry passed the 100 MW per year production milestone during 1997, and has been growing rapidly toward GW per year production at an annual growth rate of approximately 25%. Most of the commercial production is based on crystalline silicon which is likely to be the mainstay for the near future. One of the stumbling blocks in this scenario is the availability of silicon feedstock at a reasonable cost. At the present time, the PV community uses existing capacity, rejects and scraps from the semiconductor industry. Demand for silicon feedstock has increased while supply has decreased, resulting in shortages. Recently the semiconductor industry was in slow-down mode and the PV industry had feedstock available at low cost, but the upturn of integrated circuit (IC) manufacturing is bound to put pressures on supply and price of the silicon feedstock. Arguments about the silicon feedstock crunch for the PV industry have shifted from whether there will be one to when it will happen. Now that the industry has grown, the crunch will hurt more; still there is no solar grade (SoG) silicon feedstock available specifically for the solar industry.

During the late 1970's, the Department of Energy (DOE) funded several options to produce solar grade silicon for the photovoltaic industry, which were ultimately developed to supply semiconductor silicon. In addition to programs funded by the DOE, several options were also pursued in other countries and in the industry. However, none of these options resulted in commercial production of solar grade silicon.

The proposed approach is to develop SoG silicon feedstock by upgrading metallurgical grade (MG) silicon. Previous approaches to upgrading MG silicon to produce higher purity silicon from the arc furnace or to purify in the solid state using metallurgical techniques were not commercialized. The thermo-chemical reactions of the proposed approach have been proven in laboratory scale experiments[1-3]; however, the scale-up of process steps remains to be demonstrated. The simplicity of approach and the few processing steps required suggest that the final product will be low cost.

BACKGROUND

It was postulated that SoG feedstock silicon could be developed using either a chemical approach or a pyro-metallurgical approach. In both cases, the starting point was metallurgical grade (MG) silicon and the target was to produce a high purity silicon feedstock for production of high performance devices.

The semiconductor industry used the chemical approach as it recognized that to achieve purities in the ppba range, MG silicon had to be converted into a gaseous or liquid chemical (e.g. tricholorosilane, silane, etc.), which is then put through multiple distillations for purification and finally reduced via gaseous phase reactions. The resultant product is high purity polysilicon, which is left with B and P at levels less than 1 ppba and all other impurities even lower. The residual elements, B and P, are the most difficult elements to remove from silicon.

With the metallurgical approach for purification of silicon, it is possible to achieve sub-ppma levels of impurities, but this approach cannot achieve low ppba levels. Refining of MG silicon involves upgrading reactions in the molten phase of silicon where reaction rates are more rapid and complete compared to solidstate. The molten silicon with low B, P and SiC concentration must be directionally solidified to remove other metal impurities. If the refining approach works to upgrade MG silicon to levels where it can be used as feedstock for the photovoltaic industry, then there can be an ample supply of SoG silicon. In addition, it is recognized that the cost of production and quantities of SoG silicon using the refining approach will meet the requirements of the photovoltaic industry.

The photovoltaic industry produces solar cells, and these devices are more tolerant of impurities compared to the devices produced in the semiconductor industry. At the present time, the PV industry relies on silicon scraps from the semiconductor industry as feedstock. Almost all commercially produced solar cells utilize B-doped (p-type) silicon wafers in the 1 ppma range, and these devices rely on a p-n junction which is produced by incorporating a thin P-doped (n-type) layer on the p-type wafers. While there are differences in requirements for different solar cell processing sequences, almost all commercial operations require the wafers to be >0.5 ohm-cm, p-type (0.2 ppma B) resistivity. Typical B concentration in MG silicon is 20-60 ppma. This means that the photovoltaic industry reduces this B concentration to less than 1 ppba level and then puts back 0.2 ppma B during the production of wafers. Several studies[4,5] document the effect of impurities in silicon on the degradation of solar cell performance. It is concluded that almost all impurities have to be less than 1 ppma level, and, in some cases, in the ppba level. Elements that degrade performance in the ppba range have segregation coefficients in the 10^{-8} range and can therefore be removed to this level by controlled directional solidification.

The cooperative effort between Exxon and Elkem demonstrated[6] that it is possible to upgrade MG silicon in the arc furnace and use it as feedstock for photovoltaic applications. Several approaches to upgrading MG silicon[7] were pursued in Germany to upgrade in the arc furnace, but these efforts were curtailed without commercialization. Similarly, other approaches[8-20] did not result in a product.

Upgrading MG silicon is currently being supported in Japan. This work has shown[21] that it is possible to upgrade MG silicon for photovoltaic applications, and Kawasaki Steel Corporation is setting up a pilot production facility to demonstrate the full processes under funding from NEDO. High purity MG silicon is first reduced in P concentration under vacuum, followed by reduction in Al and Fe levels by a first directional solidification step. B is then removed from the surface by reaction with Ar plasma and water vapor, and finally a second directional solidification produces SoG silicon. Laboratory results are encouraging, but vacuum processing, two directional solidifications and treatments in Ar plasma make it difficult to produce SoG cost effectively.

The proposed approach is different from the Elkem and the Kawasaki approaches. However, it addresses the essential components of both these approaches and is based on laboratory results[1,2] which have shown that each of the impurities in MG silicon can be reduced to less than 1ppm level (including B and P) by carrying out purification of molten silicon. The initial purification approaches were developed by Crystal Systems using commercially available MG silicon as feedstock and the Heat Exchanger Method (HEM™) for purification. These laboratory experiments were carried out with approximately a 3 kg charge and involved stirring the melt by blowing it with moist argon, slagging and volatilization in the molten state of silicon followed by directional solidification. Based on encouraging laboratory results, experiments were carried out in an MG silicon production plant where molten MG silicon from a standard production furnace was poured into a ladle and laboratory-developed procedures were used prior to solidification of the silicon. These experiments were carried out on a tap charge of approximately 1,200 kg, and the purification experiments were limited to less than one hour duration prior to solidification of the charge. It was demonstrated that significant purification of the charge was achieved. However, it is essential that the purification approaches be utilized for longer periods of time to produce SoG silicon.

REFINING OF MG SILICON IN MOLTEN STATE

A review of the typical impurity analysis of MG silicon shows that most of the impurities can be removed by directional solidification as most impurities have a low segregation coefficient in silicon. The problematic elements are B and P, which cannot be removed effectively from silicon by directional solidification. Therefore, in the development of SoG silicon directional solidification from the molten state has to be a key refining step; in addition, it is necessary to develop other refining procedures which are focussed on removing B and P from molten silicon prior to directional solidification. It is desirable that all impurities including B and P be reduced from MG silicon as much as possible prior to directional solidification so that the yield of SoG silicon from the ingot is high. In view of these features, emphasis was placed on developing refining procedures and evaluating their effect on all impurities in MG silicon. This study used several simple refining procedures to upgrade molten MG silicon and follow the refining step with directional solidification.

Evacuation. The simplest refining step is to remove volatile elements from MG silicon; heating MG silicon in molten stage under vacuum can enhance this. Table I shows the elements that can be removed under vacuum. A major advantage of this refining step is that the impurities are

removed from MG silicon and, therefore, do not have to be dealt with for their residual effects. Vacuum processing of molten silicon has been shown to be effective for reducing P concentration in MG silicon.

Formation of volatile species. If the impurity elements can be reacted to form volatile species, further refining can be achieved. Table I also tabulates the elements that after reaction can be removed through the vapor phase. Volatile products of impurities can be formed by reaction with solid powders or gases. The solid powders could be added to the initial charge of MG silicon prior to melting, or to the molten charge with the reactive gas.

Oxidation of impurities. Impurity elements in MG silicon can be oxidized to form other species and separated from MG silicon in a slag. In this case the species formed has to be more stable than the element staying in MG silicon. Therefore, thermodynamic analyses are necessary to predict if this is possible, and then experimental conditions have to be developed conducive to forming the impurity oxide species. Table I shows the oxidation potential required to remove impurities, and Table II shows the species that were studied for refining of impurities.

Development of a thermodynamic database and model to delineate kinetic from equilibrium effects was prepared using a database in HSC modified to include thermodynamic data and solution models. HSC is a commercially available thermodynamic modeling package that incorporates an extensive database, allows extensive modification of the database and solution models by the user, and includes several powerful Gibbs Free Energy minimization routines. Overview thermodynamic calculations were performed initially with this database in the system Si-B-P-H2O-Ar, starting with 1 mole of Si(l) containing 30 and 40 ppm of B, and P, respectively. The calculations were performed to simulate the addition of up to 20 moles of gas to the system. This system was expanded to include Ca and Al as well, and slag calculations incorporated the Na-Ca-K-Al-Si-O system.

Removal of impurities from liquid silicon requires (a) reaction, such as oxidation, to form an impurity phase, and (b) partitioning of this phase from liquid silicon into a second phase. For example, B in Si (l) can react with H(g) and SiO(g) to form HBO(g); therefore, B reacts to form HBO and is removed by partitioning to the vapor phase and removed from liquid silicon, or

$$B_L \rightarrow HBO\ (g)$$

Partitioning of the impurity phase can also be into a liquid phase such as slagging, or into a solid phase such as directional solidification.

A large number of species were considered[22]; the species used in the calculations are listed in Table II. Preliminary analysis of the thermodynamics of the process indicates that the observed removal of B and P during steam blowing cannot be explained in terms of reduced B and P species volatilities. Under equilibrium conditions, less B and P are partitioned to the vapor phase than silicon, resulting in increasing concentrations of B and P in the residual silicon liquid

Slagging. If an impurity can be reacted to form a non-volatile species, it may be possible to incorporate the species or a combination of species to form a second phase, thereby sequestering the impurity away from MG silicon into this "slag" phase. This slag phase can either float on the

Table I. Refining approaches for removing impurities from liquid MG Silicon.

Atomic #	El.	Volatilization (L-V)		Slagging (L-L) (all require some oxidation potential)	Sequestering (L-S)	Segregation (L-S)
		Elemental	Complexed			Log Seg. Coeff. (Lower is better)
3	Li	High	LiCl(g)	Moderate (Acid)		
5	B	V. Low	HBO (g) (HBO2 at very high PO2)	Moderate (oxidized, basic)	Potentially good in Si3N4	-0.1
9	F	High	NaF(g)	Good (basic or acidic)		
11	Na	High	NaCl	Moderate, (Acid)		
12	Mg	High	MgCl, MGCl2	Moderate, (Acid)		-5.5
13	Al	Moderate	AlCl, AlCl2, AlCl3	Good, (acid or basic; moderate to high fo2)		-1.5
14	Si		SiCl4, SiO			
15	P	Moderate	HPO (modest), also PH2, (PH, PH3)	Good at high fo2, basic, or extremely low fo2, basic		-0.5
16	S	High	SiS, H2S, HS, SiS2, S2	Good (basic, low fo2, or basic, extremely high fo2)		
17	Cl	High	NaCl	Extemely basic, low fo2		
19	K	High	KCl	Moderate (Acid)		
20	Ca	High	CaCl2	Good (Acid)		
21	Sc	Low	ScCl2			
22	Ti	V Low	TiCl4	Acid, high fo2		-5.7
23	V	V. Low	TiCl4,			-5.4
24	Cr	Low		high fo2		-4.9
25	Mn	high		high fo2		-4.9
26	Fe	V. Low	FeCl2	high fo2		-5.2
27	Co	V. Low	CoCl2	high fo2		-4.7
28	Ni	V. Low	NiCl2	high fo2		-3.9
29	Cu	Moderate	CuCl2	NO		-3.1
30	Zn	V. High	ZnCl2	NO		-5.0
31	Ga	High		Good (basic or acid, moderate to high fo2)		
32	Ge	Low		Good Moderate fo2	GeO2 (solid)	
33	As	High				
34	Se	V. High				
37	Rb	V. High	RbCl	Moderate - Acid, high fo2.		
38	Sr	V. High	SrCl2	Good, (acid and high fo2)		
39	Y	V. Low				
40	Zr	V. V. Low				-7.8
41	Nb	V. Low				-6.4
42	Mo	V. V. Low	MoO			-7.3
47	Ag	High		NO		-4.8
48	Cd	High		NO		
50	Sn	Moderate	SnO			-1.5
51	Sb	V. High				
56	Ba	V. High (?)	BaCl2			
57	La	V. Low		?Phosphate rich slag		
58	Ce	V. Low		?Phosphate rich slag		
59	Pr	Low				
60	Nd	Low				
62	Sm	V. High (?)				
63	Eu	V. high (?)				
64	Gd	V. Low				-6.4
65	Tb	V. Low				
66	Dy	High (?)				
74	W	E. Low				-7.8
82	Pb	V. High				
83	Bi	V. High (?)				
90	Th	V. Low				

Table II. Species used in initial thermodynamic analysis of Ar + H2O addition to Si bath with B, P impurities. The highlighted species are stable.

#	Phase	Species	#	Phase	Species	#	Phase	Species
1	gas	Ar(g)	22	gas	HBO2(g)	43	gas	P4O9(g)
2	gas	H2O(g)	23	gas	H3BO3(g)	44	gas	P4O10(g)
3	gas	B(g)	24	gas	(HBO2)3(g)	45	gas	Si(g)
4	gas	B2(g)	25	gas	HPO(g)	46	gas	Si2(g)
5	gas	BH(g)	26	gas	O2(g)	47	gas	Si3(g)
6	gas	BH2(g)	27	gas	OH(g)	48	gas	SiH(g)
7	gas	BH3(g)	28	gas	P(g)	49	gas	SiH2(g)
8	gas	B2H6(g)	29	gas	P2(g)	50	gas	SiH3(g)
9	gas	B5H9(g)	30	gas	P3(g)	51	gas	SiH4(g)
10	gas	B10H14(g)	31	gas	P4(g)	52	gas	Si2H6(g)
11	gas	BO(g)	32	gas	PH(g)	53	gas	SiO(g)
12	gas	BO2(g)	33	gas	PH2(g)	54	gas	SiO2(g)
13	gas	B2O(g)	34	gas	PH3(g)	55	solid	B2O3
14	gas	B2O2(g)	35	gas	PO(g)	56	solid	H3PO4
15	gas	B2O3(g)	36	gas	PO2(g)	57	solid	P2O5
16	gas	B(OH)2(g)	37	gas	P2O3(g)	58	solid	SiO2
17	gas	B2(OH)4(g)	38	gas	P2O4(g)	59	solid	BP
18	gas	(BOH)3(g)	39	gas	P3O6(g)	60	liquid	B(l)
19	gas	H(g)	40	gas	P4O6(g)	61	liquid	P(l)
20	gas	H2(g)	41	gas	P4O7(g)	62	liquid	Si(l)

surface of molten silicon or sink to the bottom of the crucible and be easily removed. A synthetic slag can be added to the charge for refining or formed as a result of reactions with impurity elements. It is important that the components of the slag do not contribute impurities to silicon. MG silicon contains alkali and alkaline earth elements that are slag formers. An analysis was carried out to review the impurity elements and evaluate their propensity to go into the slag phase. This tendency is dependent on the acidity/basicity of the slag as well as the oxygen partial pressure. Table I shows the results of this analysis. Once again, refining by slagging is dependent on several parameters, viz., reaction kinetics, diffusion of impurities, partitioning coefficients, etc.

Gas blowing. During refining of molten MG silicon gases can be purged through the melt. These gases can be of reactive nature to react with the impurity elements, or neutral to promote stirring of the melt. An advantage of a stirred melt is that it may promote reaction chemistry. Different gases have been used to promote reaction chemistry as well as promoting conditions for slagging and oxidation conditions. The gases have also been used to carry solids (slags), liquids (moisture) or gases (gas mixtures) to react with molten MG silicon and promote refining.

Simultaneous reactions. Theoretical analysis of the above refining processes indicate different experimental conditions for refining different impurity elements and cannot explain the purification achieved by isolated processes. A combination of the refining processes has shown even better results as compared to the sum of the individual processes. This may be explained by the fact that vigorous stirring of the "melt", "slag", "impurities" and "impurity species" are intimately mixed, thereby promoting reactivity and "tying up" the impurity rather than be limited by diffusion-limited and thermodynamic factors. Similarly, impurities may be trapped in an oxidized state in the slag and thereafter be removed by evaporation. Simultaneous reactions may allow complex, local equilibrium steps to happen sequentially which could otherwise not happen.

EXPERIMENTAL RESULTS

Commercially available MG silicon, as received from the supplier and without any cleaning or surface treatments, was loaded in a fused silica crucible and placed in an experimental reactor or a modified Heat Exchanger Method (HEM) furnace for refining experiments. Initial experiments used about 1 kg MG silicon charge in the experimental reactor; later experiments were with 10 to 60 kg charge in the HEM furnace. Besides the capability of using larger charge sizes, the HEM furnace was set up with an improved vacuum capability and directional solidification. Refining experiments were carried out using different parameters, e.g.,

- degrees of vacuum as well as slight overpressure,
- blowing of different gases,
- incorporating different moisture content in gases and at different flow rates,
- adding slag components to the charge initially or to the molten MG silicon,
- changing experimental conditions with time as well as the order in which the parameters were changed, etc.,
- lance diameter and height above bath,
- water content of gas,
- H_2 content of gas

A typical experiment involved heating the charge under vacuum until molten, stabilizing the melt at 1450°C, extracting the first sample, carrying out various refining steps with samples extracted after each step, evacuating the chamber after completion of refining steps, and directional solidification of the charge. Samples were extracted from molten MG silicon during refining using suction cups in a fused silica tube immersed under molten silicon. Samples were also extracted from the directionally solidified ingot corresponding to initial solidification stage and towards the end. These samples were analyzed using glow discharge mass spectroscopy. The results showed some problems due to the sample extraction technique, ability to sample clean melt, entrapment of gases and secondary phases, inhomogeneities, etc. However, trends of refining with various parameters could be deduced from the data. The initially solidified sample always showed a lower level of impurities and samples toward the last solidified material showed considerably higher level of impurities. Some of the conclusions that can be drawn at this stage, based on refining for about 6 to 8 hours of total refining with steps of about 1 to 3 hours each, are as follows:

- Best B reduction was achieved with a 1 kg charge in the experimental reactor, using reactive gas loaded with moisture blowing through the charge and using a slag during refining,

- Evacuation, slagging, moist argon gas blowing through the melt carried out separately did not effectively reduce the impurities in MG silicon; however, in combination significant reduction of impurities was achieved,

- P reduction by evacuation of molten MG silicon at 1450°C was not effective but with other refining steps P was reduced significantly,

- Charge sizes up to 60 kg were refined without any problem but most of the development was carried out at 25 kg charge size,

- Refining steps were effective for reducing impurities in MG silicon as the difference in the last-solidified and initially solidified samples cannot be explained by directional solidification alone,

- Impurities up to 5 orders of magnitude were refined in experimental batches with the most problematic elements, B and P, showing refining by up to factors of 50.

Figure 1 shows the impurity analyses of several samples taken during development of refining processes. In this experiment (#MG3-7), a 25 kg MG charge was refined. The data was normalized to the first sample taken after meltdown of the charge. All elemental impurities except B and P are shown on a logarithmic scale, whereas B and P are shown on a linear scale on the right side. Significant refining was achieved. The directionally solidified silicon sample from this experiment is tabulated in Table III along with a similar sample for a 1 kg refined MG silicon charge. The data shows that the 25 kg MG silicon sample, after refining, measures impurity levels similar to the 1 kg sample; the refining times for both experiments were quite similar.

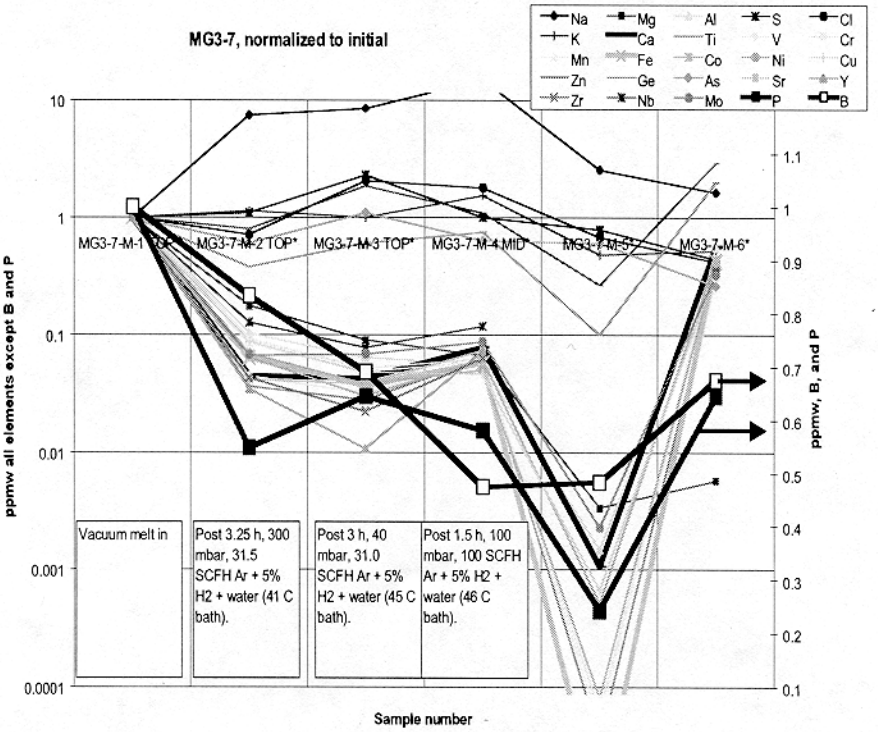

Figure 1. Impurity analyses of several samples taken during development of refining processes.

Table III. Impurity analysis (ppmw) of MG silicon after refining followed by directional solidification.

Element	1 kg Charge CSI-003	25 kg Charge MG3-7-M-5	Element	1 kg Charge CSI-003	25 kg Charge MG3-7-M-5	Element	1 kg Charge CSI-003	25 kg Charge MG3-7-M-5
Li	0.01	0.011	Mn	0.11	0.015	Ag	<0.5	<0.5
B	0.68	5.8	Fe	23	0.11	Cd	<0.3	<0.3
Na	0.1	0.17	Co	0.07	0.004	Sn	<0.05	<0.05
Mg	0.019	0.007	Ni	0.21	0.021	Sb	<0.05	<0.05
Al	2.5	2.5	Cu	0.12	0.04	Ba	0.14	<0.01
Si	Major	Major	Zn	0.029	0.02	La	<0.01	<0.01
P	13	7.5	Ge	1	0.2	Ce	<0.01	<0.01
S	0.2	0.041	As	0.58	0.18	Pr	<0.01	
Cl	0.66	0.21	Se	<0.5		Nd	<0.01	
K	0.75	0.029	Sr	<0.01	<0.01	W	0.062	<0.01
Ca	0.31	0.084	Y	<0.01	<0.01	Pb	<0.05	<0.05
Ti	0.05	0.008	Zr	<0.01	<0.01	Th	<0.005	<0.01
V	0.079	0.003	Nb	<0.01	<0.01	U	<0.005	<0.01
Cr	0.045	0.008	Mo	0.022	0.013			

CONCLUSIONS

Pyro-metallurgical techniques have been developed to refine molten MG silicon to reduce the level of impurities and thereafter directionally solidify the charge so it can be used as SoG silicon feedstock. A combination of vacuum operation, reaction with impurities to form volatile species, or oxidation of impurities that can be vaporized, sequestered or slagged to remove impurities from MG silicon has been used as a refining technique. The experimental parameters for each processing step and each impurity vary. However, it is demonstrated that the best refining step is achieved when a combination of refining techniques is used. The most problematic impurities for refining are B and P as these elements have a high segregation coefficient. Therefore, focus for refining has been to reduce B and P, and after refining directionally solidify the charge. Initially using a 1 kg sample, B and P were reduced to 0.68 ppmw (1.77 ppma) and 13 ppmw (11.9 ppma), respectively. The charge size was scaled up to 60 kg. An experiment using a 25 kg MG silicon charge, after refining for approximately 8 hours followed by directional solidification, reduced the B and P concentrations to 5.8 ppmw (15.1 ppma) and 7.5 ppmw (6.8 ppma), respectively. The proposed approach of using simplistic refining procedures simultaneously while blowing moist argon through the melt followed by directional solidification has been effective in reducing all impurities from molten MG silicon including B and P. It is intended to optimize the processing steps and scale up the charge sizes to produce low-cost solar grade silicon using this approach.

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Status of Technology Development of SOG-Si Materials using NEDO Melt Purification Process

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Abstract ; The 60 tons / year scale pilot plants of NEDO MP-Process has been competed till the end of 1998 and MG-Si has been successfully purified to solar-grade impurity level. The technology development of the pilot plant operation is planned to carry out in 1999-2000.

1 Introduction

In recent years, there has been a large expansion of the solar cell market. In 1998, the world production of solar cells amounted to about 150 MWp. As regards the feed stocks, the solar cell industry has been dependent on the off-spec silicon supplied by microelectronics industries. However, a serious shortage of feed stock in near future is predicted in view of the expected growth of the market. One of the answers to this problem is to provide another feed stock source.

From this point of view, Kawasaki Steel Corp. has been engaged in developing a pyro-metallurgical process to produce solar grade silicon (SOG-Si). Historically, from 1986 to 1992, its efforts were focused on a so-called NEDO Direct Reduction Process on a basis of the carbothermic reduction of silica of high purity.[1] In 1993, the objective of the research was switched to the refining of metallurgical-grade silicon (MG-Si) with a result that fundamentals of a new process of melt-purification (NEDO-MP Process) was developed on an experimental plant with a scale of 20 kg silicon.[2] In 1996, aiming at the extension of the NEDO-MP Process to the mass production technology, seven Japanese companies established SOG-Si Technology Research Association (SOGA). Since then, SOGA has been engaged in the construction of a pilot plant with a capacity of 60 tons / year and the development of its operation technology as well.

2 Outline of NEDO-MP Process

The flow diagram of NEDO-MP Process is shown in figure 1, and the outline of the plant is shown in figure 2. With this plant, MG-Si is fed as the raw material. Its purification is completed through double melting process. In the first melting process, dephosphorization of silicon and the first-step directional solidification are carried out successively in an electron beam vacuum furnace. Proceeding to the second melting process, a plasma melting of the silicon in an oxidizing atmosphere eliminates the impurities of boron and carbon. Subsequently, the molten silicon is directly subjected to the

second-step directional solidification. Thus, SOG-Si is usually produced as ingot or crushed block.

Targets of this development has been determined as follows. The content of impurities in SOG-Si must be less than 0.1 ppmw for phosphorous, iron, aluminum and titanium, 0.1 to 0.3 ppmw for boron, less than 5 ppmw for oxygen and carbon. Its resistivity shoud be in a range of 0.5-1.5 Ωcm with the polarity of p-type. The target production cost is 2300 yen / kg-silicon at the production scale of 1000 tons / year. In the on-going project, a pilot plant of 60 tons / year scale was originally scheduled to be constructed till the end of 1998, and the technology for its operation is planned to be developed in 1999 - 2000.

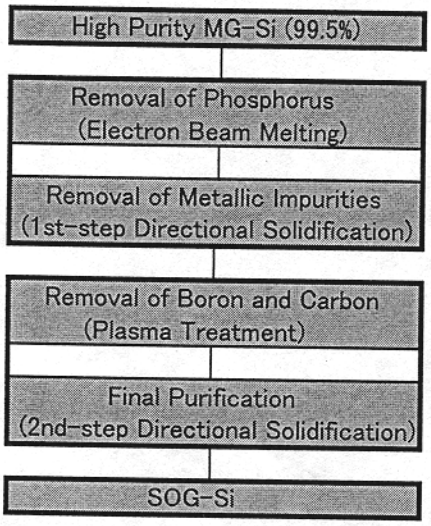

Fig.1 Flow diagram of NEDO MP Process

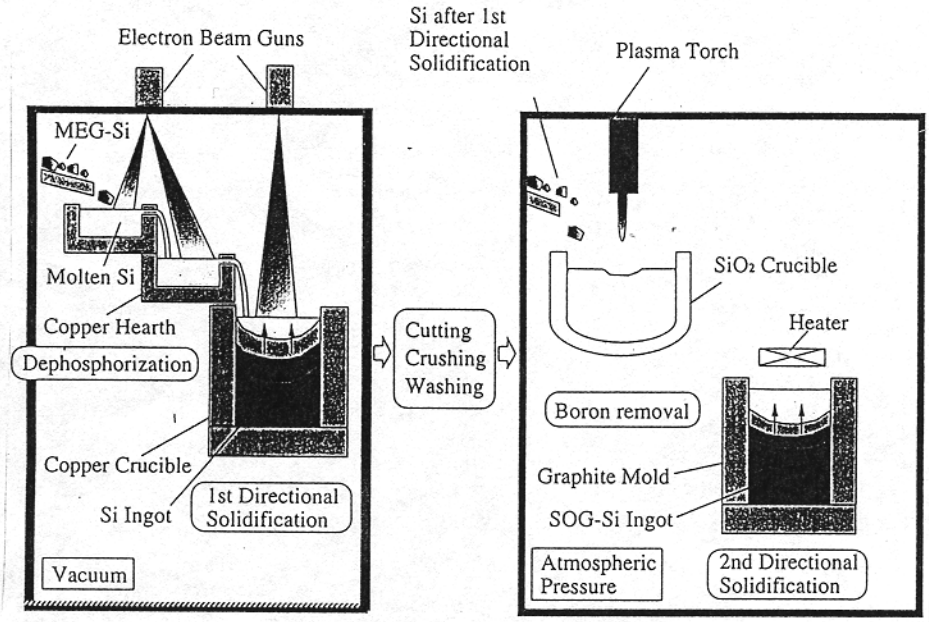

Fig.2 Outline of the plants of NEDO MP Process

3 Present Status

The main part of the pilot plant has been already completed at Mizushima Works of Kawasaki Steel Corp. The facilities for first melting process were installed in March, 1998. The specifications are listed in table 1. An electron beam furnace is composed of two electron beam guns with output power of 750 KW, a copper hearth for melting silicon and a water cooled copper mold for directional solidification. With this furnace, the MG-Si is fed continuously and into the copper hearth and melted. The impurity of phosphorous in silicon is removed by evaporation from the surface to the level

Table 1 The specifications of facilities for the first melting process

Melting Chamber	φ2100 × L4500 mm
Feeder	10～100 kg／h
EB Gun	750kW × 2
Copper Hearth	W1500×L800×H150mm
Copper mold	φ750×H300mm
Ingot Weight(max)	150 kg

Table 2 The specifications of facilities for the second melting process

Plasma Torch	1200kW × 1
Induction Heater	800 kW
Silica Crucible	φ630 mm
Max. Melting Size	300 kg
Graphite Mold	650×650×300mm
Mold Heater	500 kW

below 0.1 ppmw. The dephosphorized silicon overflows from hearth to the copper mold for the directional solidification. This furnace is capable of approximately 150 kg-silicon by one cycle.

The facilities for the second melting process were installed at the end of 1998. Their specifications are shown in table 2. They comprise a plasma melting furnace and a casting furnace with graphite mold. The former is equipped with a non-transfer type plasma torch for purification and an induction heater for melting in a crucible made of silica. The silicon purified through the first melting process is charged in the melting furnace. The temperature of silicon melt is in the range of 1500 to 1700 ℃. The impurities of boron and carbon in molten silicon is eliminated by oxidation with the plasma of argon and hydrogen gas containing water vapor. When the resistivity of silicon monitored by sampling reaches the target range, the deboronization treatment is finished, and the melt is poured into the graphite mold for the second-step directional solidification. The maximum ingot size of the directional solidification is 650×650×300mm and its weight is approximately 300 kg.

Figure 3 displays the sequence of impurity contents in silicon with NEDO MP Process. The concentrations of major impurities in MG-Si are listed in the figure. It is important to note that only phosphorous is removed in the first melting process and only boron in the second process. Metallic

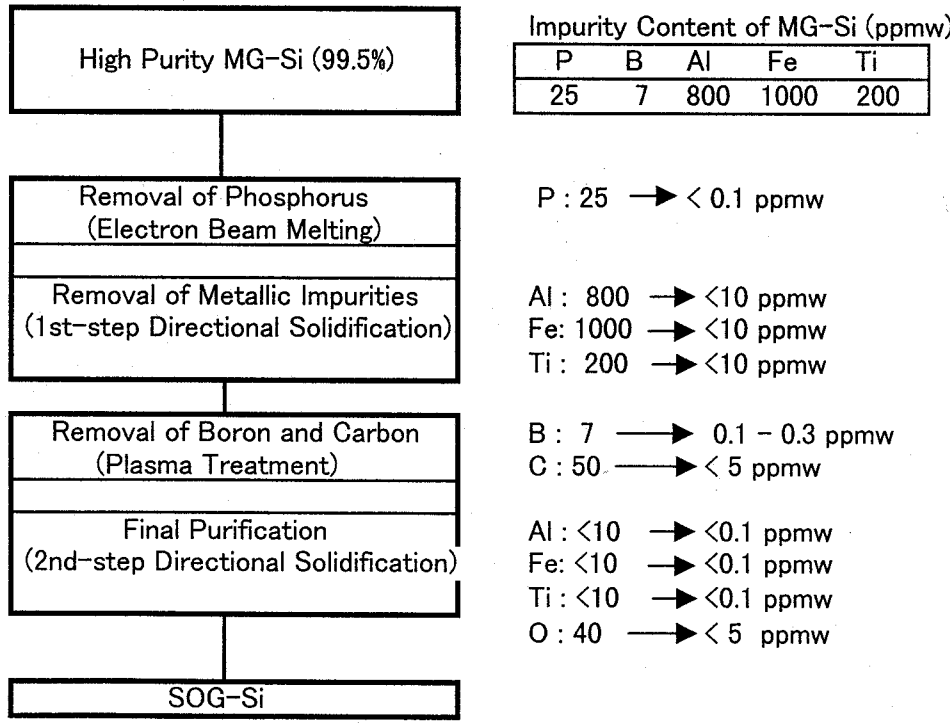

Fig.3
Change in impurity contents of silicon with NEDO-MP Process.

Table 3 Impurity contents of SOG-Si produced with the pilot plant (ppmw)

	Fe	Al	Ti	C	O	resistivity
SOG-Si produced	<0.05	<0.01	<0.01	<10	<5	0.5-1.1
(target)	<0.1	<0.1	<0.1	<5	<5	0.5-1.5

Table 4 Cell efficiencies using electro-magnetic cast wafers from the SOG-Si

silicon	Mean cell efficiency(%)
Present SOG-Si	13.6
"off-spec silicon"	13.2

impurities in silicon after the first directional solidification is less than 10 ppmw. In the process shown in figure 3, the first melting process is capable of processing the silicon by about 50kg／h. And in the second melting process, in which deboronization is carried out, purification of silicon is processed by the rate of 45 kg／h.

Table 3 shows the impurity contents in SOG-Si ingot produced with this pilot plant. The resistivity of this silicon is in a range of 0.5 – 1.1 Ωcm. It has turned out that impurity level satisfy the target. The quality of the SOG-Si produced by this process was compared with that of off-spec silicon used commercially for solar cells by preparing solar cell from the electro-magnetic cast wafers. The results is shown in table 4. The cell efficiency of the SOG-Si was found to be 13.6% comparable to 13.2% obtained with the off-spec silicon. This result demonstrate the technological utility of NEDO-MP Process for the commercial production of SOG-Si. The technology for the operation of this pilot plant operation is developed on the basis of the experiences obtained with the previous small-scale experimental equipment in 1993-1996. [3)]

4 Summary

The 60 tons / year scale pilot plants of NEDO MP-Process has been competed till the end of 1998. The technology development of the pilot plant operation is carrying out and MG-Si has been successfully purified to solar-grade impurity level. This year, improvement in the facilities and technology development for quality control and plant operation are under way, and test operation on manufacturing SOG-Si will be continued for process evaluation conducted in next year.

Acknowledgements

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Physics of iron in silicon: how much do we know after 35 years of research?

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1 Introduction

Iron is one of ubiquitous metal impurities in silicon, detrimental for both IC and PV devices. In photovoltaics, iron contamination introduces recombination centers, which reduce the minority carrier diffusion length and consequently the solar cell efficiency. The maximum dissolved interstitial iron concentration which does not significantly affect solar cell efficiency is approximately 10^{13}-10^{14} Fe/cm^3 [1]. However, interstitial iron and FeB pairs is not the only iron-related defect, detrimental for the lifetime. Iron may decorate extended defects, making them extremely recombinative active [2]. Precipitation of iron and other metal impurities in areas of high defect densities in polycrystalline solar cells leads to regions of low minority carrier diffusion lengths. In terms of the solar cell efficiency, these local regions act as shunts for power generated in neighboring regions, and result in unproportionally lower cell performance [3]. It was observed that gettering is very inefficient in increasing the lifetime in areas containing defect clusters, and it was speculated that this may be due to the strongly bound chemical state of transition metals at intragranular defects [4, 5]. Unfortunately, the data on the fundamental physical properties of iron in silicon, available from the literature, are essentially limited to interstitial iron and iron-acceptor pairs, and do not include much information on other possible states of iron. Surprisingly, even some basic properties of iron are still debated in the literature. In this article, we will discuss the physics of iron in silicon, and will show that many of the issues, which are generally believed to be resolved, are in fact poorly understood and need further research.

2 Interstitial iron in silicon

2.1 Electrical properties of interstitial iron

Although numerous experimental data, obtained on intentionally and unintentionally iron-contaminated samples [6-20] suggested that the level at E_V+0.40 eV is associated with iron, it took about 20 years of research starting from the pioneering work of Collins and Carlson [21] to prove that this level is indeed the level of interstitial iron. The ultimate evidence for this was obtained by Feichtinger *et al.* [22], who diffused iron in *n*- and *p*-type silicon with different resistivities and plotted the intensity of the EPR signal of Fe_i^0 as a function of the calculated Fermi level position. He found that the charge state of Fe_i changes from Fe_i^+ to Fe_i^0 as the Fermi level crosses the level at E_V+(0.375±0.015) eV [22]. These studies were done at cryogenic temperatures.

The temperature dependence of the position of iron level in silicon received increasing attention in the last several years due to its importance for modeling of segregation-type gettering in p/p^+ epitaxial wafers. The experimental data reported in [23-25] indicate that the energy levels of iron, as well as of manganese and cobalt, are strongly temperature dependent at high temperatures. McHugo *et al.* [24, 25] and Gilles *et al.* [23] concluded from their neutron activation analysis (NAA) and Mössbauer spectroscopy studies, respectively, that the position of the iron level at T=800^{0}C coincides with that measured by DLTS and Hall effect at low temperatures, whereas at T>900^{0}C the iron level dives towards the valence band and nearly merges with it at T>1100^{0}C. Their experimental data are presented in Fig. 1.The absence of experimental data between the temperatures where the DLTS and Hall effect data were obtained, and 800^{0}C, makes the interpolation of the iron level position over the whole temperature range difficult. One can imagine three substantially different simple curves for a temperature dependence of the iron level in the

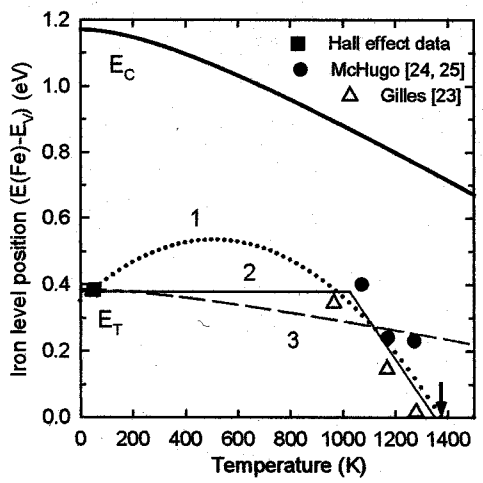

Fig.1. Temperature dependence of the position of the donor level of iron in the band gap with respect to the valence band edge. The symbols represent the experimental data for the iron level position obtained in numerous DLTS and Hall effect studies at low temperatures (filled square) and as reported by McHugo *et al.* [24, 25] (filled circles) and Gilles *et al.* [23] (open triangles). A data point measured by McHugo *et al.* [24, 25] at 1373 K corresponded to the iron level merging with the valence band and is shown in this figure by an arrow. The lines represent attempts to fit the temperature dependence of the iron level by three different functions: a parabolic fit (curve 1, dotted line)), a step-like function (curve 2, solid line) and a proportional fit $E_{Fe}(T)/E_g(T)=const$ (curve 3, dashed line). The temperature dependence of the band gap width $E_g(T)$ is shown by the thick solid line "E_C". This dependence does not take into account an additional band gap shrinkage due to heavy doping.

intermediate temperature range, as indicated in Fig. 1: a parabolic fit to the experimental data (curve 1), a step-like function (curve 2) and a smooth curve given by $(E_{Fe}(T)-E_V)/E_g(T)=const$ (curve 3), where $E_g(T)$ is the temperature-dependent band gap width. The parabolic dependence is the only curve of the three, which is smooth and fits well the experimental data. Although it would be premature and speculative to conclude that the temperature dependence of the iron level position in the band gap is described by this parabolic function, we want to attract attention of the scientific community to this possibility. Experimental studies at T<800^{0}C are required to determine which of the three models provides a better description for the temperature dependence of iron in silicon.

2.2 Diffusivity of interstitial iron in silicon

The diffusion coefficients of transition metals in silicon depend on the charge state of the metal since the ionic radii of the neutral and ionized species and the degree of the electronic density overlap of the diffusing atoms with surrounding silicon matrix are different for the ionized and neutral charge states. Migration enthalpies and preexponential factors of the largest of *3d* ions can be astonishingly accurately calculated as a difference in the elastic energies at the tetrahedral and the hexagonal interstitial sites using a hard-sphere model, as suggested by Utzig [26]. However, this model fails for *Cu, Ni, Co* and *Fe*, which have the smallest ionic radii from the *3d* row. For instance, no prediction could be made for Fe_i^+ using the model of Utzig [26] since the ionic radius of positively charged iron is too small to distort the lattice. Obviously, the diffusion barrier of interstitial iron is determined primarily by a strong interaction of iron valence electrons with up to a hundred of surrounding silicon atoms, as it was observed in EPR and ENDOR studies [27-29]. Theoretical calculations which would take into account such interactions for neutral and positive charge states of iron are lacking. In the following discussion, we will show that even experimentalists do not agree if the positive or neutral iron diffuses faster.

The charge state of iron in *n-Si* and *p-Si* at different temperatures can be easily calculated from the position of the $Fe_i^{0/+}$ level with respect to the Fermi level. The temperature dependencies of the fraction of ionized iron in *p-Si* and *n-Si* for the temperatures from 300 K to 1400 K are presented in Fig. 2. The calculations took into account the temperature dependence of the band gap width and possible temperature dependencies of the position of the iron level with respect to the valence band, discussed above. At room temperature, Fe_i is predominantly positive (and paired with boron) in *p*-type silicon and neutral in *n*-type silicon. At temperatures above approximately 100 to 200^{0}C, *FeB* pairs dissociate and the Fe_i^+ concentration increases. At sufficiently high temperatures (above 600 K) the Fermi level moves to the midgap position, and iron becomes mostly neutral in both *n*-type and *p*-type silicon. The fraction of ionized iron depends on the function chosen to

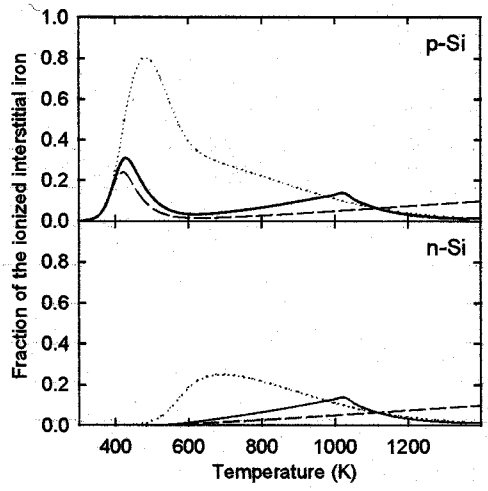

Fig. 2. The equilibrium fraction of ionized interstitial iron in *n*- and *p*-type silicon for different assumed temperature dependencies of the energy level of interstitial iron. The simulations were made for a doping level of 10^{15} cm^{-3} and for an iron contamination level much lower than the boron (phosphorus) doping. The dotted line (see curve 1 in Fig. 1), the solid line (curve 2 in Fig.1), and the dashed line (curve 3 in Fig. 1) corresponds to the parabolic, step-like, and proportional temperature dependencies of the interstitial iron energy level. The calculations for *p-Si* also take into account iron-boron pairing, although the concentration of *FeB* pairs is not shown in the figure. A peak in the Fe_i^+ plot at about 400 K in *p-Si* is due to the dissociation of *FeB* pairs in *p-Si*. Almost all the ionized iron is paired with boron in *p-Si* at temperatures below 350 K.

describe the temperature dependence of the iron level position. Parabolic and step-like functions (curves 1 and 2 in Fig.4, dotted and solid lines in Figs. 1,2) result in the fraction of ionized iron decreasing with increasing temperature from 10% at 1000 K to 1.5% at 1400 K in both *p-Si* and *n-Si*. On the contrary, the proportional model (dashed lines in Figs. 1,2) predicts a gradual increase of the fraction of ionized iron from 5% at 1000 K to 10% at 1400 K.

The predominantly neutral charge state of iron at elevated temperatures does not necessarily imply that the diffusion coefficient of iron at high temperatures is determined by the diffusivity of neutral iron. While about 95% of iron is neutral at T>1000 K in moderately doped silicon (see Fig. 2), the small fraction of ionized iron may significantly change (or even determine) the apparent diffusivity of interstitial iron, if the diffusion coefficient of the ionized iron is much higher than that of the neutral iron. This will be discussed below.

At low temperatures, the charge state of iron is better defined. It is assumed that iron is neutral in *n-Si* and in the depletion region of reverse-biased Schottky diodes made on *p-Si*, and is positive (and paired with boron) in *p-Si*. However, generation of electron and holes by iron (see, e.g., [30]) may make small fractions of iron ionized in the depletion regions of *p-Si* Schottky diodes, and neutral in the depletion regions of *n-Si* Schottky diodes, as pointed out by Heiser *et al.* [31].

After the report of Weber [32, 33], based on experimental results of Struthers [34], Kimerling *et al.* [35], and Shepherd *et al.* [36], more than 10 research groups reported their results on iron diffusivity [11, 23, 31, 34, 36-56]. Their data are plotted in Figs. 3,4. The diffusivity data were plotted separately for the high-temperature and the low-temperature range to make the plots more legible. We want to point out that the horizontal and vertical scales of Figs. 3,4 are identical (so that the readers may combine them into a single oversized graph by cutting and pasting) and a single line is fitted through both graphs.

Analysis of the literature data, presented in more detail in our recent review [57], shows that there is a significant scatter from 0.49 eV to 0.92 eV in the iron diffusion barriers reported by different groups, which can partly be ascribed to the narrow temperature range of each study. Additionally, there is no agreement whether ionized or neutral iron diffuses faster. While most of the authors that compared diffusivities of Fe_i^0 and Fe_i^+ agree that neutral iron has a higher diffusion barrier than Fe_i^+ [31, 43, 51, 58], Koveshnikov *et al.* [50] came to the opposite conclusion. Heiser *et al.* [59] suggested that this contradiction can be partly explained as a consequence of *FeB* pairing, i.e., that Koveshikov *et al.* [50] measured the *effective* diffusion coefficient of the ionized iron, affected by pairing with boron. Unfortunately, the data on the pairing constants of iron with boron remain ambiguous, thus hampering accurate evaluations of the effect of pairing.

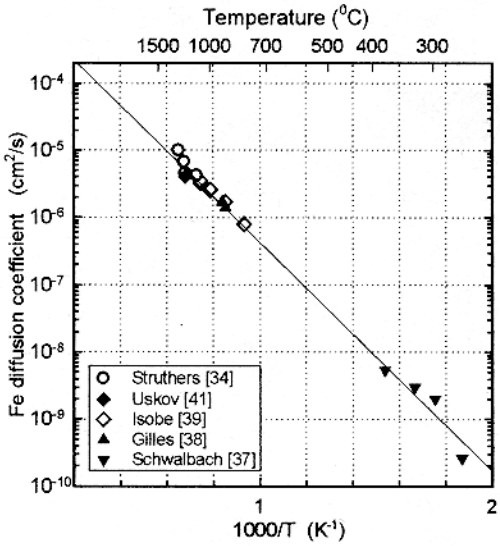

Fig. 3. Diffusivity of iron in silicon at temperatures above 250°C. The solid line represents the fit given by Eq. (1). The fit was made using data from both this figure and Fig. 4.

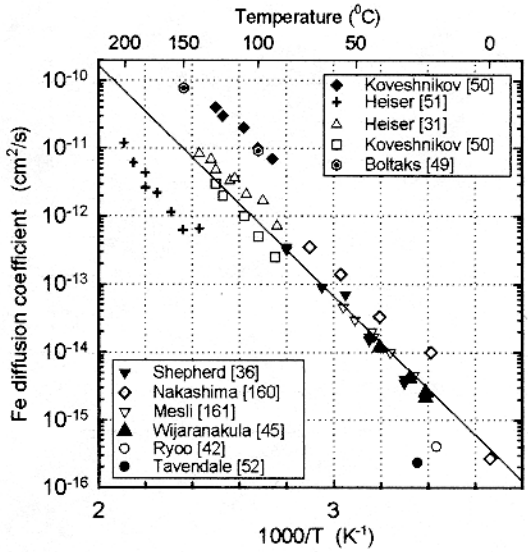

Fig. 4. Diffusivity of iron in silicon at temperatures below 250°C. Solid line represents the fit given by Eq. (1). The fit was made using data from both this figure and Fig. 3. The filled diamonds and open squares are the data obtained by Koveshikov *et al.* [50] for neutral and ionized iron, respectively.

It is clear that an accurate value for the height of the diffusion barrier for neutral or ionized iron can be obtained only by using experimental data in a wide temperature range under the conditions when ionized or neutral iron is the only diffusing species. Unfortunately, this is difficult, if not impossible, since iron usually co-exists in both neutral and ionized charge states. The apparent diffusion coefficient of iron diffusing in two charge states is given by $D_{app}(Fe_i)=fD(Fe_i^+)+(1-f)D(Fe_i^0)$, where f is the fraction of ionized iron, and $D(Fe_i^+)$ and $D(Fe_i^0)$ are the diffusion coefficients of ionized and neutral iron [23]. For example, if we assume that the diffusivity of Fe_i^+ at a temperature T is much higher than the diffusivity of Fe_i^0, then the apparent diffusion coefficient $D_{app}(T)$ will be determined by the diffusion barrier of Fe_i^+ despite the relatively low fraction, f, of the ionized iron. However, the pre-factor in the diffusion coefficient will be reduced by the value of coefficient f, which is, in turn, temperature dependent. The consequence of the temperature dependence of f is that neither the diffusion barrier of Fe_i^0 nor that of Fe_i^+ can be straightforwardly extracted from the temperature dependence of $D_{app}(Fe_i)$.

Despite the lack of understanding of the charge state of diffusing iron, the experimental data points for both Fe_i^0 and Fe_i^+, all plotted in the same plot, can be fitted by a single straight line (Figs. 3,4) with a slope corresponding to the diffusion barrier of $E_m(Fe_i)=0.67\pm0.02$ eV. The majority of experimental data points can thus be described by the equation

$$D(Fe_i) = (1.0^{+0.8}_{-0.4}) \times 10^{-3} \exp\left(-\frac{0.67 \mp 0.02 \ \ eV}{k_B T}\right), \quad cm^2/s \qquad (1)$$

It is worth noting that this expression agrees within the error limits with the one previously reported by Weber [32, 60], $D(Fe_i)=1.3\times10^{-3}exp(-(0.68\ eV)/k_BT)\ cm^2/s$. Although almost all data points in Figs. 3,4 are fitted by Eq.(1), we would not conclude from this result that the diffusion barrier of iron does not depend on its charge state. We believe that this agreement actually confirms the difficulties with the analysis of iron diffusivity due to co-existence of iron in both charge states in all or almost all imaginable experiments. Since we can assign Eq.(1) to the diffusivity of neither ionized nor neutral iron, we will call it the "effective diffusion coefficient of iron". Yet, the physics of iron diffusion can not be understood without further experimental and theoretical studies.

3 Pairing of interstitial iron with other impurities

3.1 Iron-boron pairing

Since a noticeable fraction of interstitial iron is ionized in *p-Si*, diffusion of iron will be affected by its pairing with shallow acceptors. Recent studies of diffusivity of copper in *p*-type silicon [61] revealed the importance of taking the pairing effects into account. The correct pairing constants are absolutely necessary to reliably model the processes of diffusion and segregation gettering of iron. Iron is believed to be the best studied transition metal in silicon, and it is assumed that the pairing behavior of iron with boron, characterized by the equilibrium binding energy E_b, diffusion barrier of interstitial iron E_m, and potential barrier for dissociation of FeB pairs E_{diss}, was established years ago. However, analysis of the literature data suggests that this is not quite the case.

The equilibrium binding energy E_b can be obtained from the analysis of the temperature dependence of the equilibrium fraction of Fe_i, paired with boron, as it follows from the law of mass-action:

$$\frac{N(FeB)}{N(Fe_i^+)\times N(B_s^-)} = \frac{Z}{N_i}\times \exp(\frac{E_b}{k_B T}), \qquad (2)$$

where N_i is the density of interstitial sites in the silicon lattice (5×10^{22} cm^{-3}), Z is the number of possible orientations of the pair with the same symmetry around one acceptor atom (4 for the tetrahedral symmetry), and $N(FeB)$, $N(Fe_i^+)$, and $N(B_S^-)$ are the concentrations of *FeB* pairs, ionized interstitial iron, and negative boron acceptors, respectively.

The temperature dependence of the equilibrium fraction of paired iron was studied by Kimerling *et al.* [54, 55], Lemke [46, 62], Reiss *et al.* [63], and Wunstel *et al.* [64]. The reported binding energies vary from 0.45 eV [55] and 0.53 eV [64] to 0.6 eV [62, 63] and 0.65 eV [46, 54]. Wijaranakula [45] calculated a binding energy of 0.58 eV from the experimental data reported earlier by Nakashima *et al.* [44]. A scatter in the binding energies reported by different groups can be partly ascribed to interaction of iron with other impurities, unintentionally introduced in silicon during studies, and by narrow temperature range in which the studies were made. A careful re-examination of the pairing data using state-of-the-art silicon material and modern cleanroom facilities is required to obtain the binding energy with a better accuracy. While the scatter by 0.1 eV is not very important from the point of view of fundamental physics of semiconductors, it is unacceptable for the task of prediction of gettering in real devices.

A similar, if not greater, uncertainty was found in the reported association and dissociation energies of *FeB* pairs. The association kinetics of *FeB* pairs can be described [36, 65] using the theories of diffusion-limited precipitation/trapping, developed by Ham [66]. It can be shown [65] that the association rate of *FeB* pairs is given by the following expression:

$$\tau_{ass} = (4\pi D(Fe_i) N_A R_C)^{-1}, \qquad (3)$$

where R_C is the capture radius of iron by acceptors. Inserting the approximation of R_C for moderately doped samples into Eq.(3), one easily obtains [35, 54, 56, 65]:

$$\tau_{ass} = \frac{\varepsilon\varepsilon_0 k_B T}{q^2 N_A D(Fe_i)} \approx \frac{566.7\times T}{D(Fe_i)\times N_A}, \qquad (4)$$

This equation was extensively used for determining the diffusion barrier of ionized iron at low temperatures. These studies, discussed in detail in our recent review [57], yielded strongly scattered values for the diffusion barrier from 0.58 eV to 0.81 eV, which is certainly not accurate enough for the purpose of predictive modeling.

The dissociation kinetics of *FeB* are determined by the potential barrier E_{diss} for a jump of the Fe_i ion away from the first closest neighbor position to the boron atom. The dissociation time constant is given by:

$$\tau_{diss}^{-1} = \nu \times \exp(-\frac{E_{diss}}{k_B T}) \quad (5)$$

where ν is the attempt frequency. Although it is quite straightforward to determine the dissociation barrier E_{diss} from the temperature dependence of dissociation reaction, we are aware of only two values reported in the literature: E_{diss}=1.17 eV ($\nu=1.8\times10^{10}$ s^{-1}) [67], and 1.2 eV ($\nu=5\times10^{10}$ s^{-1}) [68].

It is important to note that the association or dissociation energies of the pairs were calculated in most studies from the temperature dependence of the reaction rate assuming that the reaction is either purely dissociation or purely association. This assumption is generally incorrect and may lead to substantial errors since in fact, the rate of the observed reactions is determined by both, the association rate $r_{ass}=\tau_{ass}^{-1}$, and the dissociation rate $r_{diss}=\tau_{diss}^{-1}$. This point can be illustrated by the analysis of a simple differential equation, describing the reaction kinetics. If we neglect the precipitation of iron, assume that most of the interstitial iron is ionized ($N(Fe_i)=N(Fe_i^+)$), and that the concentration of iron is much less than the concentration of boron, then the iron-boron pairing reaction is given by the following differential equation:

$$\frac{dN(FeB)}{dt} = r_{ass} \times (N(Fe_i) - N(FeB)) - r_{diss} \times N(FeB) \quad (6)$$

where $N(FeB)$ is the concentration of iron-boron pairs. The solution of this equation is given in the general case by

$$N(FeB) = \frac{r_{ass}}{r_{ass}+r_{diss}} \times N(Fe_i) - \left\{ \frac{r_{ass}}{r_{ass}+r_{diss}} \times N(Fe_i) - N_0(FeB) \right\} \times \exp(-(r_{ass}+r_{diss})t) \quad (7)$$

where $N_0(FeB)$ is the initial concentration of FeB pairs at the beginning of the measurement ($t=0$). It is important that the reaction rate is always given by the sum of association and dissociation rates. Hence, the apparent activation energy of the reaction as reported in the literature may actually come out to be between the true dissociation and diffusion barriers.

3.2 Interaction of iron with oxygen

Oxygen and carbon are major impurities in silicon, contained in very high concentrations, between approximately 5×10^{16} cm^{-3} and 10^{18} cm^{-3}. Although understanding of the interaction of iron with carbon and oxygen is of major importance for the characterization of iron in silicon, there are only a few contradictory experimental studies on this subject. The studies of Hackl *et al.* [69] showed that iron prevents the nucleation of oxygen precipitates even if the iron concentration is as low as 10^{11} cm^{-3}, whereas Zhang *et al.* [70], Shen *et al.* [71] and Jablonski *et al.* [72] found that the precipitation of oxygen is significantly enhanced in the presence of iron. Miyazaki *et al.* [73] showed that grown-in iron enhances the formation of OSF and, following the conclusions of [74, 75], suggested that iron precipitates serve as nucleation sites for OSF.

You *et al.* [76] reported an electron trap level at E_C-*0.36 eV* due to the iron-vacancy-oxygen complex (*FeOV*) in irradiated samples contaminated with iron. The identification of this level was based on the fact that the anneals of the samples at 80°C resulted in an increase in the concentration of the level at E_C-*0.36 eV*, accompanied by an equal decrease of the concentration of the *A*-center (*V-O* complex) at E_C-*0.17 eV*. The total concentration of the *A* center and the center at E_C-*0.36 eV* remained constant within 10% during the whole anneal, thus indicating that the first center is converted into the second one [76]. No reduction in the *A*-center concentration was detected during similar anneals in samples containing no interstitial iron, thus confirming that iron is a part of the E_C-*0.36 eV* center. A decrease in the concentration of the *A*-center during iron precipitation was also observed in the EPR studies of Kustov *et al.* [77]. Ammerlaan [78], with a reference to a private communication with J.W.Corbett, reported *g*-values of the EPR signal of *FeOV* center.

Mchedlidze and Matsumoto [79] studied the electrically detected magnetic resonance (EDMR) of iron in Czochralski-grown (CZ) silicon. They found a new signal with an amplitude

correlating with the iron contamination level in the samples. Since the signal was only observed in iron-contaminated oxygen-rich CZ-*Si*, and was not detected in low oxygen content float zone (FZ) *Si*, it was proposed that the signal originates from complexes containing both iron and oxygen, e.g., iron-decorated oxygen precipitates.

3.3 Interaction of iron and its complexes with hydrogen.

The ability of hydrogen to passivate electrically active defects is well known (see, e.g., a review of Pearton *et al.* [80]). Hydrogen passivation of grown-in defects is commonly used in solar cell technology to increase the minority carrier diffusion length (see, e.g., [81, 82]). Passivation is usually implemented by a relatively low-temperature hydrogen plasma treatment. Substantial concentrations of hydrogen are also introduced into the near-surface region of silicon during routine chemical etching (see, e.g. [83-86]). Recent experimental data showed that interaction of hydrogen with impurities is more complicated than just passivation. Complexes of transition metals with hydrogen often introduce new levels in the bandgap (see, e.g., recently published data on *Pt-H* complexes [85], *Ag-H* complexes [87], and *Co-H* complexes [88]).

Despite the importance of the problem of interaction of iron with hydrogen and passivation of iron-related defects, the data in the literature are inconclusive. Tavendale et al. [52, 89] studied the influence of hydrogen plasma treatment on *Fe*-related deep levels and reported that the levels E_V+*0.32 eV* and E_V+*0.39 eV* (note that the latter level is not the level of Fe_i, since interstitial iron had in Refs. [52, 89] a DLTS peak at higher temperatures with the energy E_V+0.40 eV), which appeared in DLTS spectra after diffusion of *Fe* and were thus suggested to be complexes of *Fe* with an unknown structure. These levels were neutralized by hydrogen to the depth of the hydrogen penetration. They also found that the level of interstitial iron was not affected by the plasma treatment. The latter result has recently been confirmed by Weber [90]. Data of Kouketsu *et al.* [91, 92] indicate that the *FeB* peak at E_V+0.1 eV is effectively neutralized by hydrogen. Kaniewska *et al.* [93] reported a change in the shape of the DLTS spectra of *n*-type *Fe*-contaminated silicon samples with dislocations and stacking faults after hydrogenation, although could not identify the passivated centers.

Several authors suggested that the levels at E_V+0.23 eV, E_V+0.38 eV [91, 92], and E_V+0.31 eV [94] appear in the bandgap after hydrogenation of iron-contaminated samples and argued that they are levels of iron-hydrogen complexes. It was shown that these levels are unstable at elevated temperatures and dissociate after anneals at 175^{0}C for 30 min [94]. Unfortunately, the experiments described in Refs. [91, 92, 94] lacked a systematic analysis of the interaction of hydrogen with the impurity levels, such as that recently developed in Refs. [83, 87]. This approach includes the comparison of DLTS spectra of cleaved (no hydrogen) and etched (hydrogen in the near-surface region) samples, and a comparison of the depth profiles of the traps with the predicted distribution of hydrogen. This enables one to even determine the number of hydrogen atoms in a complex.

4 Complexes which include several iron atoms.

A number of EPR studies revealed that iron forms complexes, consisting of several iron atoms and/or vacancies or shallow acceptors. A detailed discussion of these complexes can be found in our recent review [57]. The first report on agglomerates of several iron atoms was published by Muller *et al.* [95], who studied complexes of iron in electron-irradiated silicon and identified $(Fe_iFe_iV)^-$ complex, $(Fe_iFe_iV_2)$ complex, and Fe_iFe_i-complex. The EPR spectrum of Fe_iFe_i pairs was identified by Muller *et al.* [95] and further studied by van Kooten *et al.* [96] and Gehlhoff *et al.* [97]. The disappearance of this center at or just above room temperature indicates that there is a strong preference for the further aggregation of iron at this center. Gehlhoff *et al.* [97, 98] found a resonance of a defect with a monoclinic symmetry, that was identified as another configuration of the Fe_iFe_i center. According to the data of Ref. [97], the disappearance of the EPR resonance of the Fe_iFe_i pairs could be enhanced by the illumination of the sample with above band-gap light.

The next intermediate state of the agglomeration of iron, which was observed by EPR, is the neutral $(Fe_i)_4$ cluster [95]. Studies of the dependence of the concentration of this center on the temperature of isochronal anneals revealed that the concentration of the complex reaches its maximum at temperatures around 140^{0}C. If the sample is annealed at a higher temperature (above 150^{0}C), the intensity of the correspondent EPR signal decreases, which can be explained as a growth of $(Fe_i)_4$ clusters to larger agglomerates of iron.

Ezhevskii *et al.* [78, 99, 100], Gehlhoff *et al.* [97, 98] and Irmscher *et al.* [101] reported complexes with monoclinic and orthorhombic symmetries consisting of two iron atoms and a shallow acceptor such as boron or aluminum. The reaction producing the complexes of *FeFeB* took place during storage at room temperature, and the intensities of the spectra were found to be a function of the storage time [99]. In *Al*-doped silicon, Ezhevskii *et al.* [100] found two EPR spectra with monoclinic-I symmetry, which were identified as $(Fe_i^+Fe_i^0Al^-)$ in two different configurations. The hyperfine splitting due to two ^{57}Fe iron atoms was later reported by Irmscher *et al.* [101], who also showed that the *FeFeAl* defect produces two groups of EPR lines corresponding to the ground and the excited states of the same defect. They reported that storage of the samples at room temperature led to the disappearance of the EPR signal, which could be restored by shining above-band-gap light on the samples.

Thus, EPR studies revealed at least 8 complexes consisting of two or four iron atoms. These complexes may be precursors of the agglomerates of iron present in high defect density areas of solar cells. However, there are no data on electrical and recombination properties of these centers.

5 Techniques for detection of trace levels of iron in silicon

The unintentional iron contamination levels of 10^{13}-10^{14} cm^{-3} were quite possible some ten years ago, particularly in multicrystalline silicon for PV applications at the stages of development of the growth technology. Part of the unintentionally introduced iron was probably present as agglomerates of iron or complexes of iron with other defects, possibly vacancies, oxygen, carbon, or trapped at intragranular defects. Since the density of such trapping sites is limited, most of iron remained as FeB pairs. Development of technology has drastically decreased the iron contamination levels. Consequently, FeB pairs are not considered the major recombination center anymore. On the other hand, iron that is trapped at intragranular defects has attracted increasing attention in the past years, especially in PV research. Detection and analysis of the structure of microdefects and determination of their iron content is an enormous challenge for the silicon metrology. In general, analysis of iron contamination of silicon seeks answers to three questions: (i) how much iron is present in the samples? (ii) where is it located?, and (iii) what is the chemical state of the iron? The first question translates to the integral sensitivity of the method, the second one to its spatial resolution, and the last one to its "chemical resolution". The requirements of high spatial and chemical resolution are incomparably more difficult to meet than that of high integral sensitivity. For instance, the requirement to achieve spatial resolution of 1 micron corresponds, for the total concentration of homogeneously distributed iron of 10^{12} cm^{-3}, to the requirement to detect *one* iron atom in a cubic micron of the sample. No wonder that none of the analytical tools meets all these requirements. In the rest of this section, we will discuss the current state of the analytical tools which are thought to have the highest sensitivity to iron, and will address their individual detection capabilities.

Minority carrier lifetime techniques: The primary technique for determination of concentration of interstitial iron is the analysis of change of lifetime as the result of dissociation of FeB pairs under the influence of heat or light [56, 102]. This procedure is a standard procedure in SPV, and can be used with some limitations (low injection level) by ELYMAT and μ-PCD techniques. Only FeB pairs can be identified. The detection limit of interstitial iron in silicon by SPV, which was only about 10^{11} cm^{-3} [103] in 1992, has been steadily improving during the last

decade and is presently at about 2×10^9 cm^{-3} in the IC processing line environment [104, 105], and down to 8×10^7 cm^{-3} under laboratory conditions [56, 106]. However, lifetime techniques assume that iron is homogeneously distributed in the direction, perpendicular to the wafer surface.

Deep Level transient Spectroscopy: DLTS of p-type silicon can detect all complexes of iron which form electrically active levels in the lower part of the bandgap [57]. Sensitivity of DLTS is determined as a ratio between the concentration of defects, N_T, and the doping level, N_d, and is usually in the range of $N_T/N_D \approx (10^{-4}$ to $10^{-6})$. Hence, the detection limit of DLTS in silicon wafers with resistivity of 10 Ohm×cm ($N_d \approx 10^{15}$ cm^{-3}) is about 10^9 to 10^{10} cm^{-3}. The spatial resolution of a DLTS measurement is determined by the diameter of the Schottky diodes (about 1 mm) and the thickness of the depletion region, formed under the contact after application of external bias (several microns). Thus, one measurement represents local concentration of the deep levels in only 0.00005% of the volume of a 4" wafer. Although mapping of the wafers with DLTS is possible (by evaporation and measurement of a set of diodes onto different spots), it is very time consuming.

Total X-ray Fluorescence: TXRF usually focuses X-rays in an approximately 0.5 cm^2 spot on the surface of a mirror-polished wafer, and detects impurities in the top 5-10 nm layer of the wafer. Flatness of the surface of PV poly-Si wafers is usually not sufficient for TXRF analysis. TXRF does not distinguish between different chemical states of iron and measures the total iron concentration. There is a noticeable trend of improvement of the detection limit of TXRF to iron and most other critical elements from 10^{11} - 3×10^{11} cm^{-2} in the late 1980s (see, e.g., Ref. [107]) to 10^9 - 10^{10} cm^{-2} in the 1990s (see, e.g., Refs. [108-117]). The sensitivity can be further increased by collection the impurities from the whole wafer surface into a single spot by using vapor phase decomposition (VPD) technique, which improves the sensitivity of the analysis to 10^9 cm^{-2} for 100 mm wafers and 5×10^8 cm^{-2} for 150 mm wafers [117-121]; even the sensitivity limits of 1×10^8 cm^{-2} [122] and 8×10^7 cm^{-2} [115] were reported.

Atomic absorption and emission spectroscopy: AAS requires complicated sample preparation, which involves dissolution of either the whole sample, or of a thin near-surface layer, and thus measures the integral iron concentration. The detection limit of bulk concentration of *Fe* is 10^{13} cm^{-3} for analysis of thin layers (1 micron) etched from the surface of a silicon wafer, and 5×10^{11} cm^{-3}, if the whole wafer is dissolved [123]. Sensitivity can be improved by using graphite furnace to atomize the sample, and VPD technique to pre-concentrate the impurities. Gupta et al. [124] reported the surface sensitivity of VPD GF-AAS to iron of about 8×10^9 cm^{-2}, while Shiraiwa et al. [125] reported even better sensitivity of 2×10^9 cm^{-2} (wafer diameter is not reported).

Mass-spectrometry: The simplest and the most common modification of mass-spectrometry is SIMS, which is subdivided into dynamic and static SIMS. In dynamic SIMS, high ion current densities are used to erode successive atomic layers at a relatively fast rate. Dynamic SIMS has the following ***mutually exclusive*** ultimate specifications: detection limits between 10^{13} and 10^{16} cm^{-3} for most impurities in semiconductors, a lateral resolution of 20 nm, and a depth resolution approaching 1-2 nm [126-129]. Static SIMS is confined to analysis of the top monolayer of the sample. This is achieved by a very low-intensity primary ion beam and by a correspondingly low sputtering rate (10^{-3} to 10^{-6} of a monolayer per second). To obtain a sufficient secondary ion yield for such a slow sputtering rate, secondary ions are sputtered from a larger area (about 0.1 cm^2), and the spatial resolution of static SIMS is decreased to about 1 mm [127]. Quantification of the static SIMS is very difficult [127, 130], primarily because no stationary condition of the surface is achieved during sputtering of the first monolayer. While the bulk sensitivity of dynamic SIMS is relatively low, as compared with GF-AAS or DLTS, static SIMS is an extremely sensitive method for the analysis of surface contamination, and enables one to reach the sensitivity to iron of about 5×10^9 cm^{-2}.

The most sensitive modification of mass spectrometry is the inductively coupled plasma mass spectrometry (ICP-MS), where the high-temperature argon plasma torch is used to atomize

and ionize the sample [131]. ICP-MS requires dissolved samples. Reported ICP-MS sensitivity limits for iron are scattered from 2.6×10^{8} cm^{-2} after a VPD-type collection of iron from the surface of 200 mm wafers, as reported by Ruth *et al.* [132], to poorer detection limits of 2×10^{10} cm^{-2} for 6 inch wafers [133], and 2.5×10^{9} cm^{-2}, as reported by Joly [115]. Gupta et al. [124] applied ICP-MS to detection of trace metals in ultrapure deionized water and 2% HF and reported detection limits of 16 ppt for water and 55 ppt for HF.

Neutron Activation Analysis: NAA is based on the quantitative detection of radioactive species produced in samples via nuclear reactions resulting from neutron irradiation of the samples. Unlike DLTS or SPV, NAA measures total iron concentration in the bulk, no matter if it is in the form of electrically active or inactive point defects, complexes, or precipitates. The only radioactive isotope of iron, suitable for NAA analysis from the point of view of its half-lifetime, is ^{59}Fe ($t_{1/2}$=45 days), formed after irradiation of ^{58}Fe with thermal neutrons. Unfortunately for high-sensitivity NAA determination of iron in silicon, the isotopic abundance of ^{58}Fe is only 0.31% [134]. Thus, only 0.31% of the total iron impurity can be activated and detected by NAA. Consequently, the sensitivity of NAA to iron in silicon is one of the poorest among about 43 to 53 elements detectable by NAA, and is about 3 orders of magnitude lower than that for *Co* or *Au* [135, 136]. Development of neutron reactors and particularly implementation of the low-background-noise underground counting facilities which reduce the background radiation by up to a factor of 40 [137] and even up to 1000 [136] result in a continuos increase of detection limits of NAA to iron. The reported sensitivity limit of NAA to iron increased over the years from 2 ppm (5×10^{16} cm^{-3}) in 1951 [138], 20 ppb to 120 ppb (5×10^{14} cm^{-3} to 3×10^{15} cm^{-3}) in the beginning of 1970s [139-141], 430 ppt (1.1×10^{13} cm^{-3}) in 1989 [142], to 8.3 ppt (about 2×10^{11} cm^{-3}) in 1993-1996 [135, 136].

6 Sources of unintentional iron contamination

Veheijke [143] listed the following sources of unintentional contamination: impurities in polysilicon fedstock and contamination during crystal growth; surface contamination during slicing and lapping; contamination from handling by mechanical equipment, which can occur during electrical measurements, numbering or marking, ion implantation, reactive ion etching, or rapid thermal annealing; contamination introduced during epitaxial growth; contaminations introduced during cleaning and etching procedures; contamination from the furnace during high temperature treatments such as oxidation, annealing after implantation, diffusion processes; contaminations during medium temperature treatments such as deposition of layers (Si_3N_4, polycrystalline Si, and SiO_2). Thus, contaminations can be classified as grown-in (those which were not removed from the silicon feedstock by purifying), and as introduced from chemicals (e.g., gases, wet chemistry, photoresist, water), from processing equipment (furnaces, ion implanters, polishing machines, etc.), and from handling between these steps (including cleanroom ambient) [144, 145].

The starting concentrations of iron in polysilicon steadily decrease, as silicon technology develops. The 1957 studies of James et al. [146] revealed iron concentrations in silicon at about 10^{16} cm^{-3}. In 1975, concentration of Fe in poly-Si was about 3×10^{14} cm^{-3} [147, 148]. Relatively recent studies of Huber et al. [135] reported iron concentration in polysilicon below the detection limit of 2.5×10^{11} cm^{-3}.

Crystal growth is the most powerful purifying step in the whole process of production of silicon devices, as long as heavy contamination during growth is avoided. This is because iron, as the other transition metals, has a low distribution coefficient, which means that silicon is purified during crystal growth by segregation of impurities in the melt. Literature data on distribution coefficient of iron between silicon solid crystal and the melt are in reasonably good agreement: 10^{-4}, as reported in [146], 8×10^{-6} according to [149], 3×10^{-5} after [150], 7×10^{-6} as suggested in Refs. [32, 151], and 5×10^{-6} to 1×10^{-5} as reported in [21]. The strong segregation of Fe in the melt enables silicon growers to grow the crystals with iron content below the sensitivity limit of the available

equipment [152]. Solar cell technology can not always benefit from the segregation purification of silicon crystals since it often utilizes fast cooling rates, which decrease the effective distribution coefficient. This explains the recent studies of Smith et al. [136], who revealed iron concentration in the silicon wafers for solar cells of about 1000 ppt (2.5×10^{13} cm^{-3}) .

Slicing and mechanical lapping are, according to the Ref. [153], very dirty operations. Wafers at this stage may be badly contaminated with a variety of impurities. Fortunately, almost all of this contamination is removed at the chemical cleaning step. This is possible because wafers are sliced and lapped at room temperature, where the diffusivity of most transition metals (with the only exception of copper, Ref. [61]) is negligibly low, so that the metals do not penetrate into the bulk of silicon. Contamination of wafers from handling (although on a much lower levels) remains one of major sources of transition metals. Similarly, metal belt used in some PV technological processes, may be an important source of metal contamination. Cleaning processes can paradoxically be one of important sources of impurities for silicon wafers [114]. Chemicals can be contaminated during their distribution in the recirculation/filtering loop of the wet benches by a sudden pump integrity loss, or by dipping cross-contaminated wafers [114]. Fabry et al. [154] reported that ion exchange resins, used in water regeneration systems, may under certain conditions become crucial iron contamination sources.

Contamination of wafers during high-temperature oxidation was a major source of metal contamination in the silicon industry in the beginning of 1980s and probably remains an important contamination source in the modern industry. Analysis of Schmidt *et al.* [153] revealed that metals diffuse from the furnace metal parts and impure SiC liners through the walls of the quartz tube. This diffusion was found to have a very steep temperature dependence, resulting in an enormous increase in contamination level of the wafers if the temperature exceeded approximately 1150^0C. Schmidt *et al.* [153, 155] suggested that transition metals diffuse preferentially along incipient grain boundaries in vitreous quartz at high temperatures. They showed that an effective way to eliminate contamination is to us a double-walled quartz tube with an *HCl*-containing gas (e.g., dry oxygen) being passed between the inner and outer walls of the tubes [153, 155, 156].

7 Summary.

Investigations of iron-related defects provide a perfect example of how different experimental techniques, sensitive to structural, recombination, electrical and optical properties of defects, can be combined to identify the nature of each defect. On the other hand, it revealed how complicated the physics of iron is. Analysis of the literature shows that the interest of research gradually shifts from the properties of interstitial iron and FeB pairs to more obscure reaction paths of iron, which are predominant at low iron concentrations and may result in formation of agglomerates of iron, stable at gettering anneals. These studies will surely be beneficial for the understanding of the effect of iron on the efficiency of solar cells.

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Atomic Structure and Electronic States of Nickel and Copper Silicides in Silicon

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Mechanical Strength Evaluations and Plans

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Summary: The key studies performed on mechanical wafer strength at Siemens Solar Industries are collected herein. The implications of these studies are collectively evaluated for the desired process optimization as well as improvements in the analysis technique.

Motivation: A simple analysis of the contributing cost of Module Fabrication and the savings allowed through reduced wafer thickness gives the following charts:

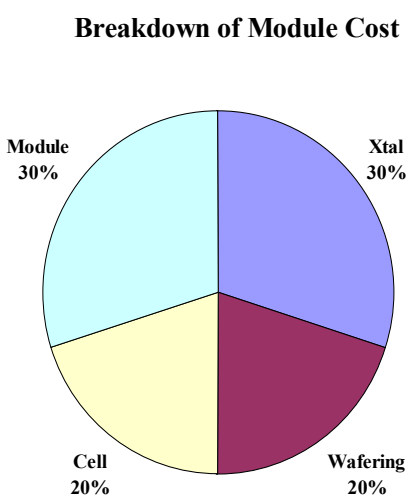


Figure 1.

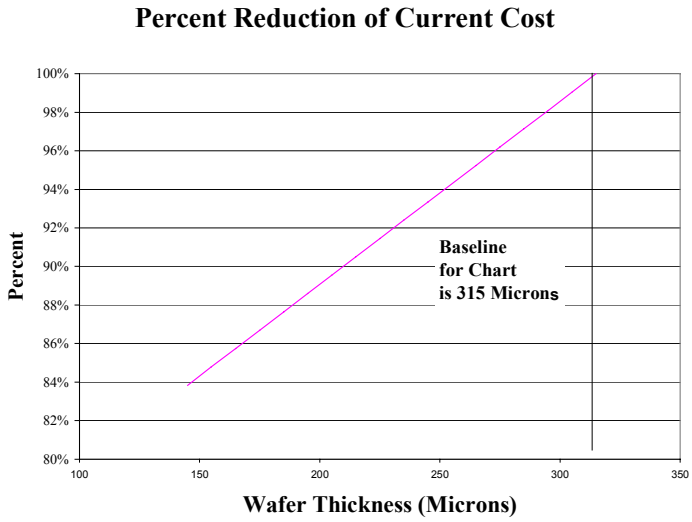


Figure 2.

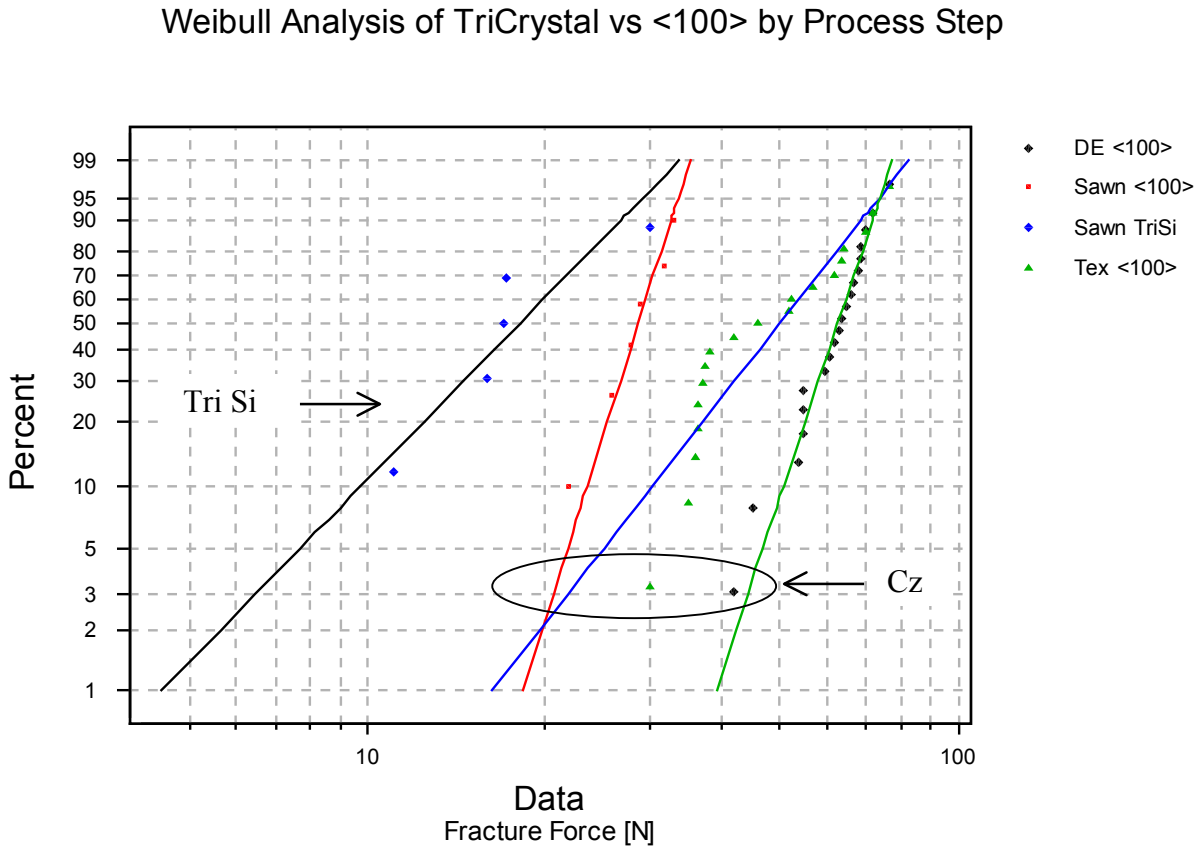
The cost reduction chart, Figure 2, assumes that crystal cost and wafering costs (totaling 50% of all costs) are inversely proportional to the number of wafers per mm of ingot with a constant kerf loss of 180 microns. This should be viewed as an upper limit on savings – wafering cost does somewhat increase with the number of wafers, and the assumption of zero yield impact is unlikely to be true. The degree to which we can reduce the thickness without a yield impact is the degree to which we can obtain the indicated savings. The rest of this paper summarizes our analysis towards this goal. In the effort to achieve these savings, compensating techniques are necessary to prevent a loss in cell efficiency, which occurs as the cells become thinner – these techniques are not addressed in this paper.

Summary of Analyses

The analyses can be summarized into two types – offline and online. The offline analyses are those done by intentionally breaking the cells - mainly with an ASTM –type concentric ring stress. Online analyses are those done by submitting various groups to the production line and collecting data on those that break in processing. Generally, offline testing has not been a good predictor of wafer survivability online. A collection of the benefits and problems with both methods are described below.

Offline Tests

Fracture Force
Siemens Solar Industries has contracted the Fraunhofer Institute to conduct detailed analysis of TriCrystalline Material and Cz <100> material in three conditions – as Sawn, after Damage Etch (DE) and after Texture Etch (Tex). A summary of the results is shown below in Figure 3



Cz

Figure 3.

For this chart, a Weibull analysis was used. In Weibull analysis, it is assumed that fracture at the most critical flaw under a given stress distribution leads to total failure. Thus the Weibull method is also called "Weakest Link Statistics" [1]. A concentric ring, ASTM methodology was used in this test.

The effect, as was seen in 1979 by Chen [1], of <100> material becoming strengthened by damage etch, and then somewhat weakened (and more variable) after texture etch is confirmed here for our process. Another comparison that can be made from this chart is TriCrystalline vs <100> sawn wafers. In this comparison, the TriCrystalline material shows an unfavorable distribution.

Figure 4 shows a direct comparison of fracture strength of Tricrystal vs. <100> as a function of the etch condition, the tricrystal wafers measured much stronger than the Cz (100> wafers.

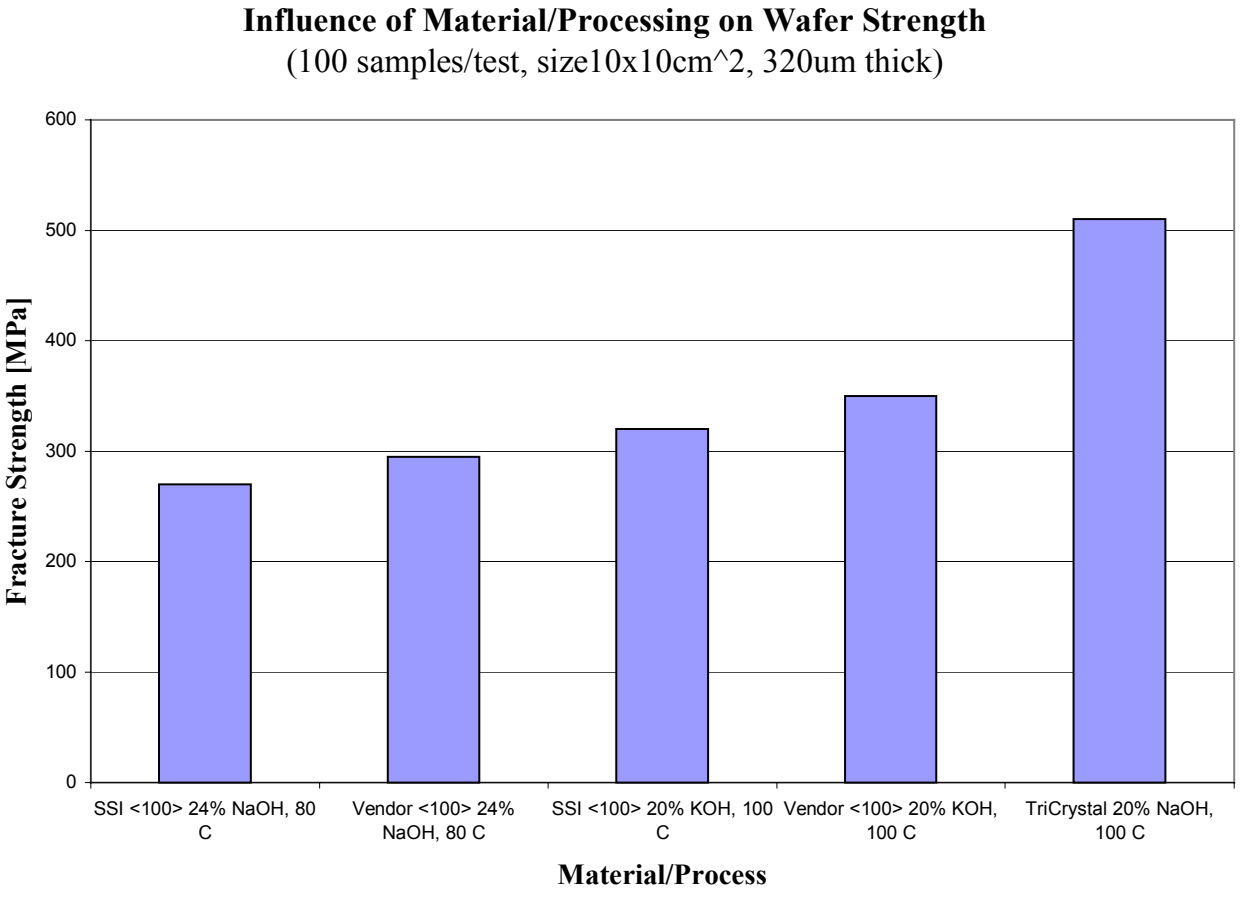


Figure 4.

Fracture force vs size

The following charts demonstrate the challenge of breakage for solar cells relative to the semiconductor industry. The data collected and shown in Figures 5 and 6 shows the continuation of the decrease of the fracture force proportional to the square of the thickness for thicknesses ranging from 800 um to 100 um. The bowing of the wafers prior to breakage becomes much more substantial at thicknesses below 200 um.

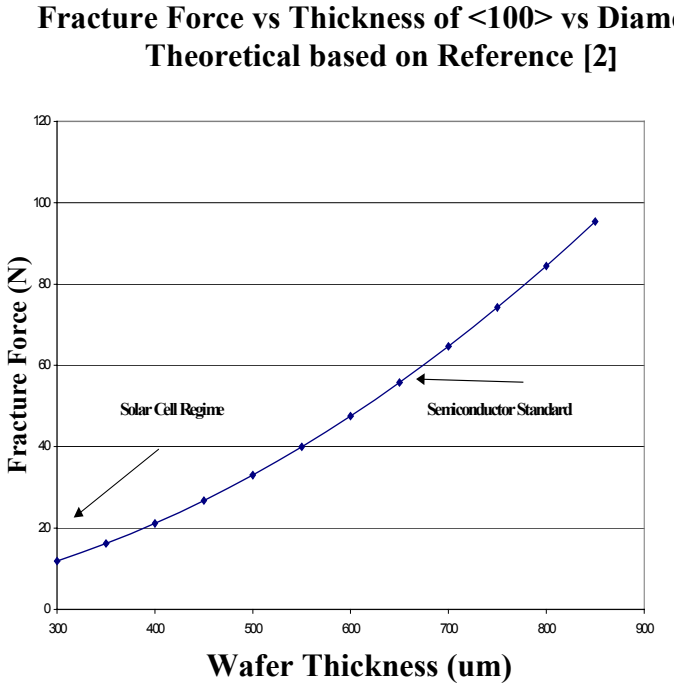


Figure 5.

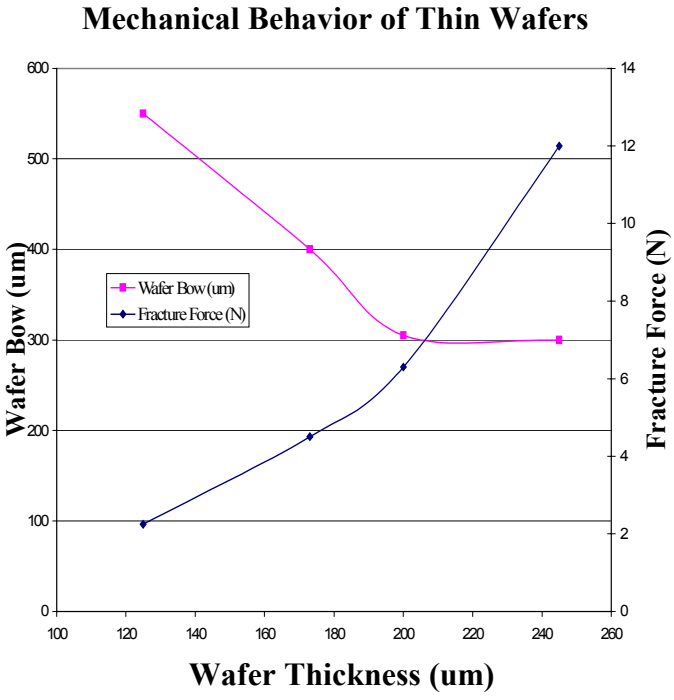


Figure 6.

The following chart illustrates an attempt to test a hypothesis that the breakage in the etch process is ingot related. To perform this test, a comparison of the breakage strength of wafers adjacent to actual broken wafers (in the etch line) vs a control group (from a boat with no broken wafers) was performed. The test concluded that there was no localized affect from the ingot which predisposed a wafer to fail, as measured by the fracture test.

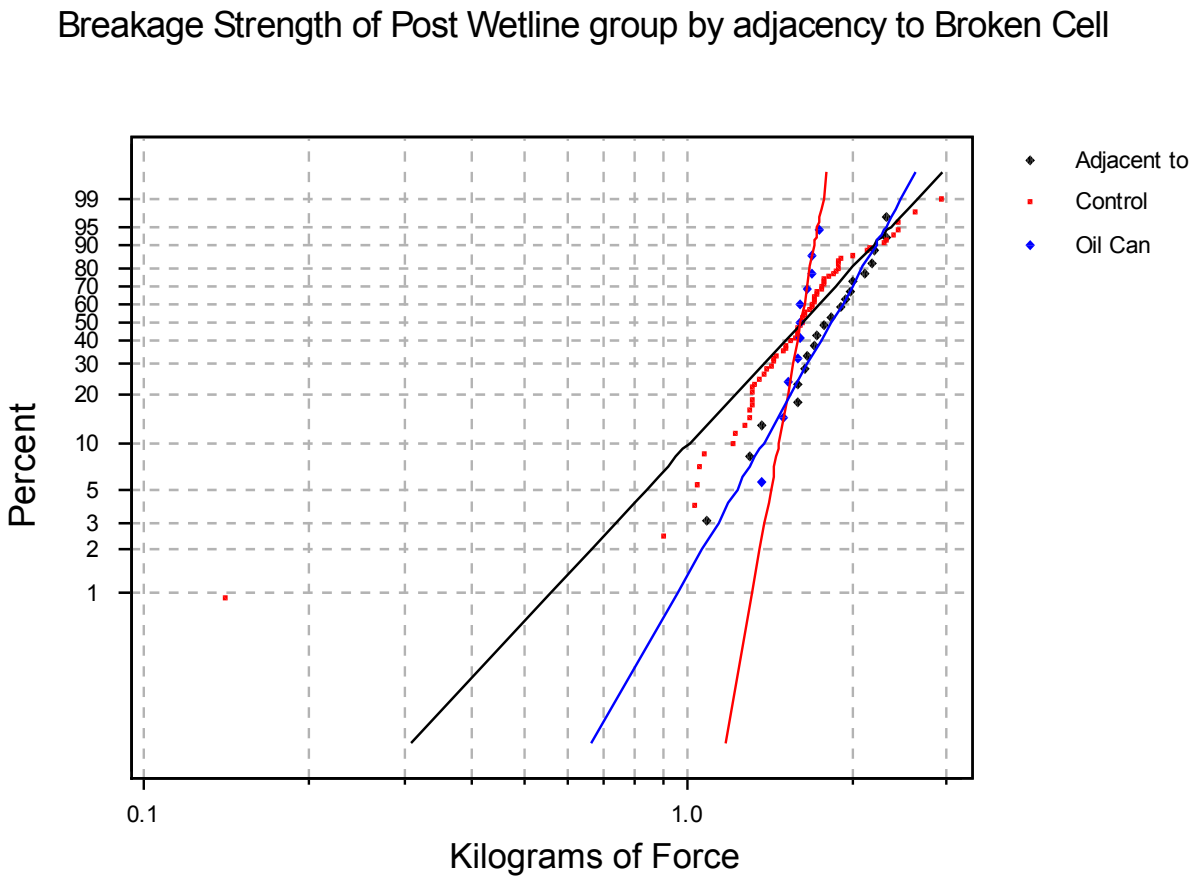


Figure 7.

In summary a list of the benefits and problems of offline testing include:

Benefits
Controllable environment – standardized results
Results traceable to theory, and a body of knowledge
Provides a strength measurement independent of handling roughness

Problems
Correlation with yield has never been established
The methods used thus far do not stress the edges
Wafers can be very vulnerable to breakage in a certain process step yet very strong to these controlled tests

Online Tests

Online testing has been conducted several times at Siemens Solar Industries. In this test, materials are "carefully" processed in an attempt to compare the survivability of different groups. In this case, "careful" means particular attention to assure that nominal conditions are used to process the material. Excessive care towards reducing breakage can lead to deviations from normal conditions which skew the results. It should be noted that the handling gentleness is another effort which pays dividends regardless of the mechanical strength built into the material. This effort is not addressed here.

Figure 8 from an early wafer comparison test shows an encouraging result for thin Tricrystal wafers.

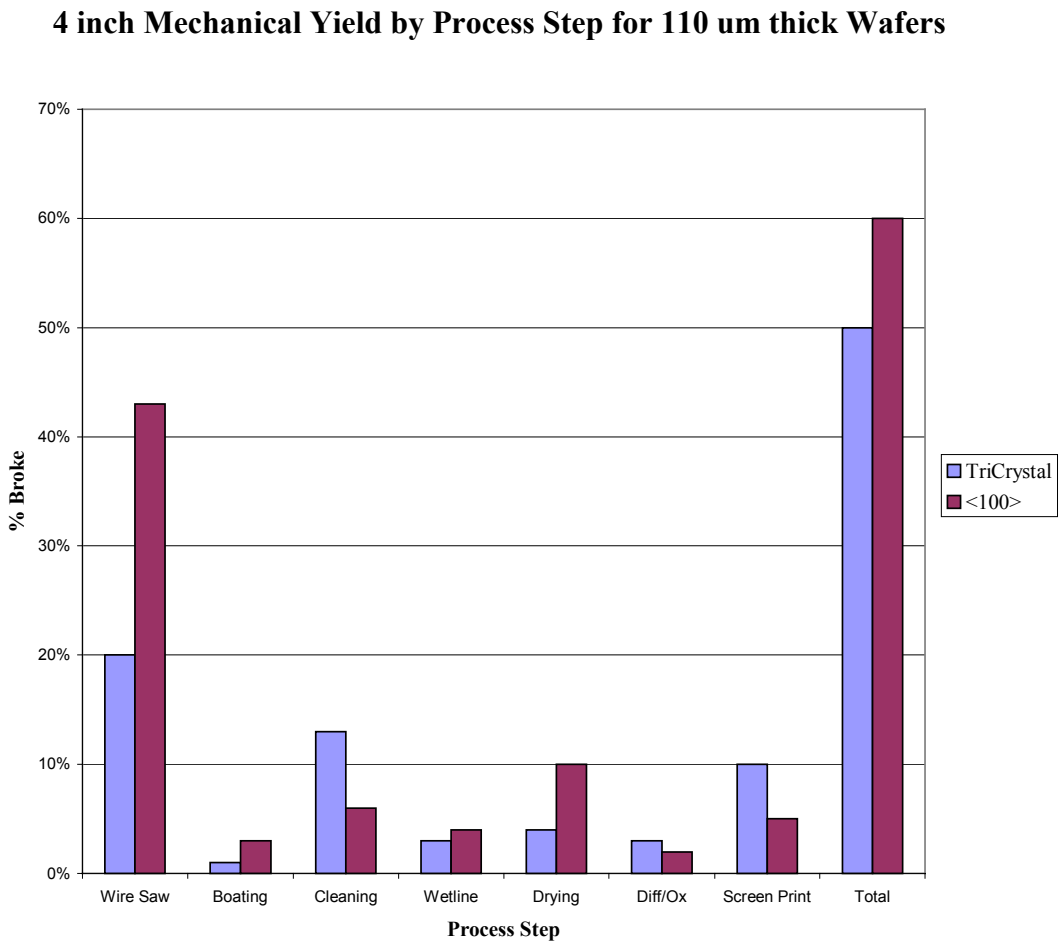


Figure 8.

Figure 9 demonstrates our most recent methodology for testing and reporting mechanical survivability. It also shows the effects of edge treatment. This test compared control or standard wafer lots to edge ground wafers, non edge ground wafers, wafers from vendor 1, and wafers from vendor 2 for breakage.

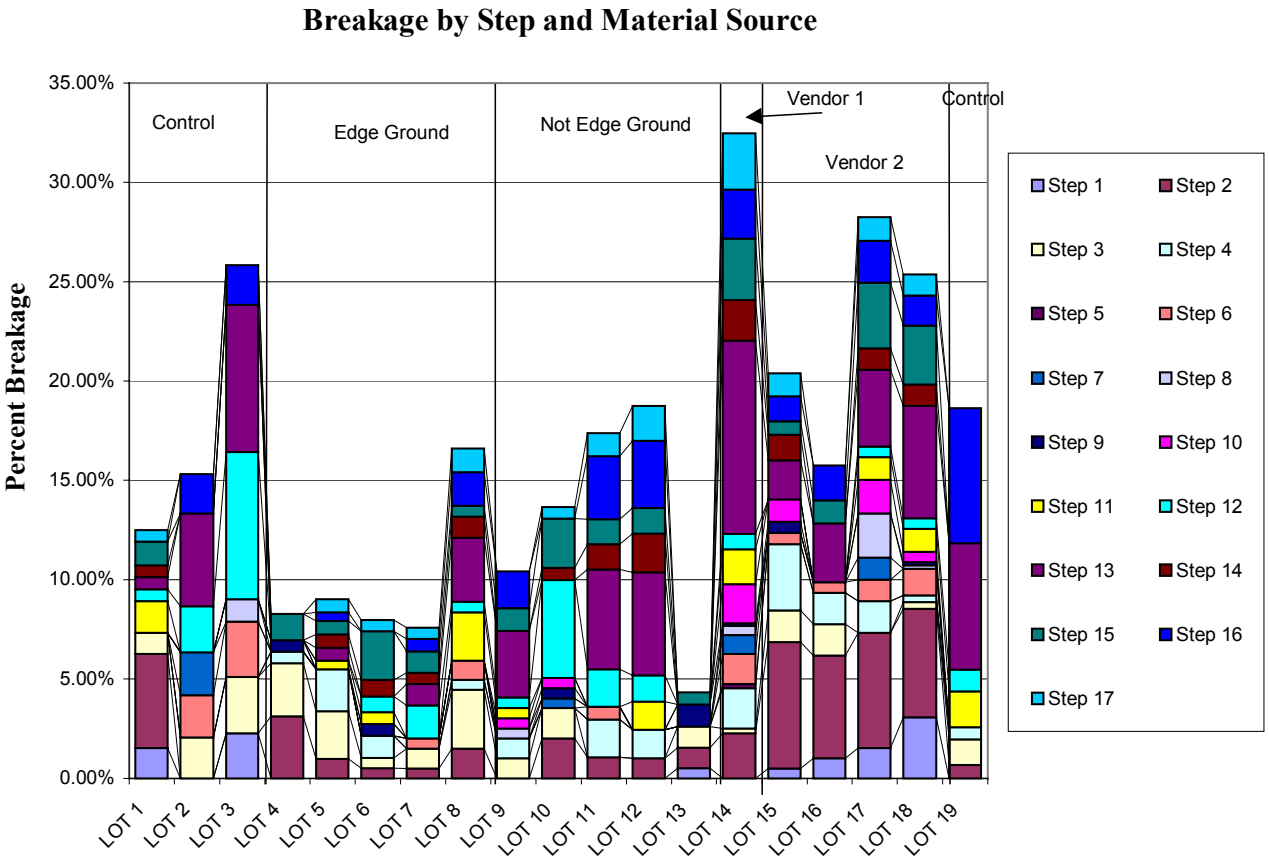


Figure 9.

The same data grouped by edge condition and showing only the totals and confidence intervals yields the following chart:

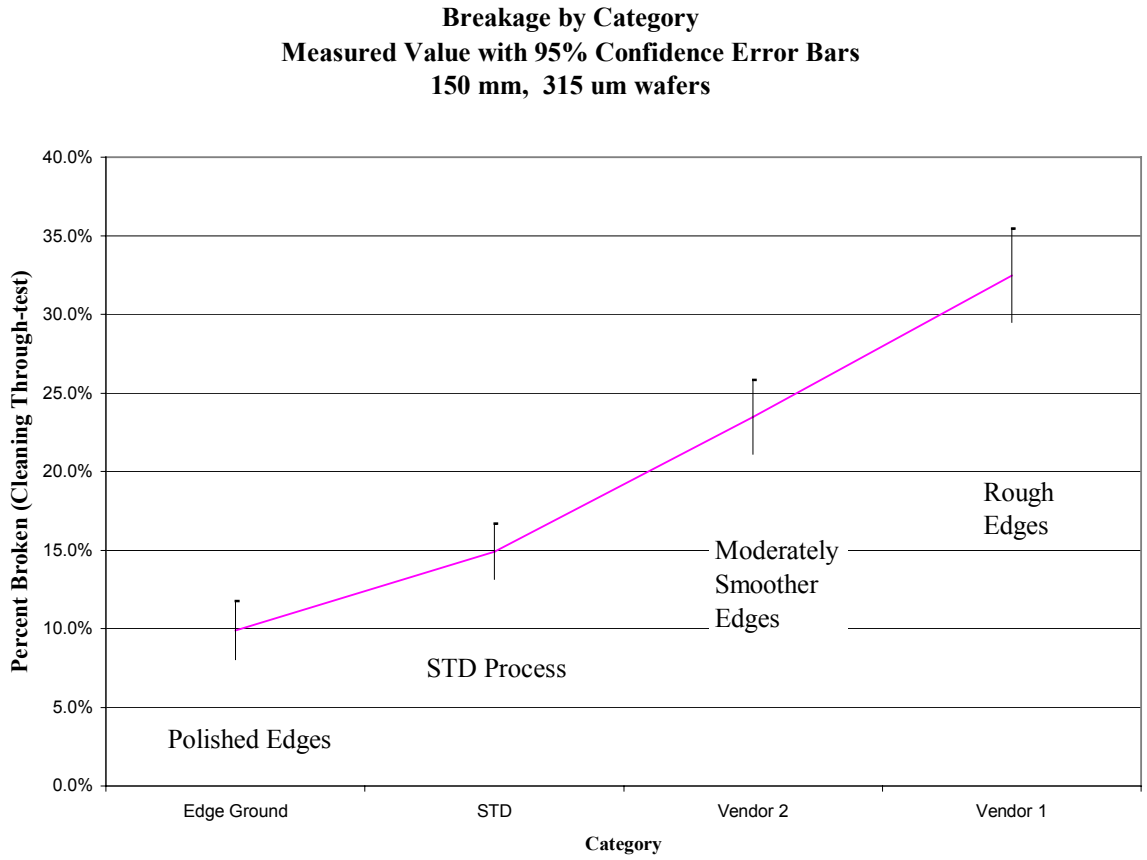


Figure 10.

In summary a list of the benefits and problems of online testing include:

Benefits

A direct test of survivability

Standard statistics for proportions (percent reject) can be used for significance tests

The process of conducting such an experiment stimulates good hypothesis that can be used to further improve the process

Problems

Influences of the test itself can bias results

Not a standard, can not be replicated in a lab

Difficult to emulate nominal care - "Hawthorne Effect"

Sufficient Lot sizes for statistical significance are difficult to manage

Summary

While most of the data collection has been done with offline techniques, the lack of practical correlation with yields has made these techniques poor tools for decision making. Online testing, performed with careful experimental protocol to overcome the above obstacles, is emerging as the most practical methodology to support decisions related to optimization of mechanical strength and reductions of the associated cost per watt.

Plans

The most significant practical question for Siemens Solar Industries at present is the true mechanical benefit of various crystal structures and edge conditions for producing thinner wafers. Preparations are being made to conduct a significant online test inclusive of 315, 250 and 150 micron wafers.

Additionally Siemens Solar Industries has contracted the Fraunhofer Institute to study improved methods of offline testing. The aim of these studies is to gain better correlation with practical results. The approach of the Fraunhofer Institute is to focus the forces only on the wafer edges. The experimental method intends to apply a specific force to a specific area. If the wafer does not break, the test head will move around the wafer to ensure the whole wafer will withstand the set force. If the wafer survives, the force is increased. In this manner, the weakest edge location is identified and Weibull statistics can be used to draw conclusions that have practical significance in line yield and productivity improvement efforts.

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Manufacturing Issues Related to Processing Thin Crystalline Silicon Solar Cells

Dr. Stephen P. Shea, Director of Crystalline Process Development, BP Solarex

Abstract: The cost of silicon feedstock is an important and relatively volatile component of the overall cost of PV products. Processes that reduce either the silicon component in the finished product or the silicon lost during manufacturing are attractive as a means of both reducing the overall cost, and of desensitizing that cost to variation in the price of feedstock. In addition, the ability to process thinner wafers has advantages in the engineering design of high efficiency devices.

The transition from ID to wire saws has produced great progress in silicon use, to the point that wafers as thin as 240 microns are now used routinely in some PV production lines. Thinner wafers can be cut without great difficulty, but are not used in manufacturing because of downstream handling problems and incompatibility with typical cell manufacturing processes.

Further significant progress in reducing wafer thickness will require re-engineering solar cell designs and downstream processing and handling.

Hydrogen-Defect Complexes in Si

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Manuscript not available at the time of printing.

Mass production technologies of SiN passivation process

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Kyocera Corporation

1. introduction

Since kyocera reported the SiN passivation effect by the plasma enhanced CVD at the first international PVSEC in 1984(1), the development of the SiN passivation has been performed by some research organization of USA, Japan, Europe and Australia. Kyocera has produced high efficiency multicrystalline silicon solar cells by introducing the PECVD SiN process. At the present, the PECVD SiN process is very important technology for crystalline silicon solar cells and is investigated to use for mass production. SiN process technologies and mass production technologies will be developed to attain higher performance and lower cost in the future.

2. SiN process

The SiN passivation has two effects. One is the surface passivation. The other is the bulk passivation. These effects are as follows.

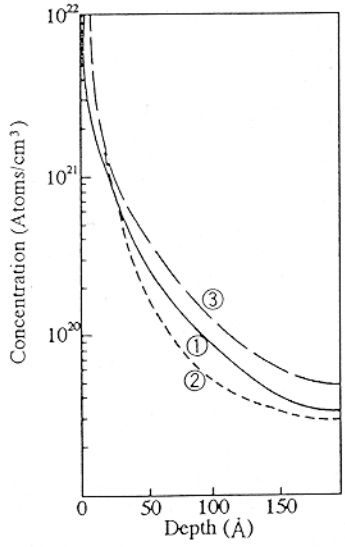
(1) surface passivation

SiN films by PECVD have an effect on the surface passivation(2). Semiconductor-insulator interfaces are very important for the surface passivation. The key parameters are the interface state density, the trapped charge within the interface states, and the insulator charge. SiN films by PECVD have positive charge densities of 10^{11}～ 10^{13} cm-3. The surface recombination velocity of 1～10 cm/s was obtained. Recently the surface state density of about 10^{11}cm-2eV-1 has been obtained. SiN films by high-frequency direct PECVD and remote PECVD are investigated to reduce the surface damages.

(2) bulk passivation

PECVD-SiN is an excellent antireflection coating and an effective passivtion of bulk defects and grain boundaries. High efficiency solar cells have been obtained by SiN film formation process with PECVD using SiH4 and NH3 at over 400℃ as compared with usual antireflection coating process such as TiO2. Higher efficiency was obtained by the thermal treatment after PECVD-SiN deposition(3). Fig.1 shows the relation between hydrogen concentration profiles and thermal treatment after SiN film deposition. As shown in Fig.1, hydrogen is diffused into the bulk by thermal treatment after SiN film deposition.

Fig.2 shows the ESR unpaired electron spin density of oxide passivated multicrystlline silicon substrate with PECVD-SiN. As shown in Fig.3, the spin density is decreased and the bulk quality is improved.



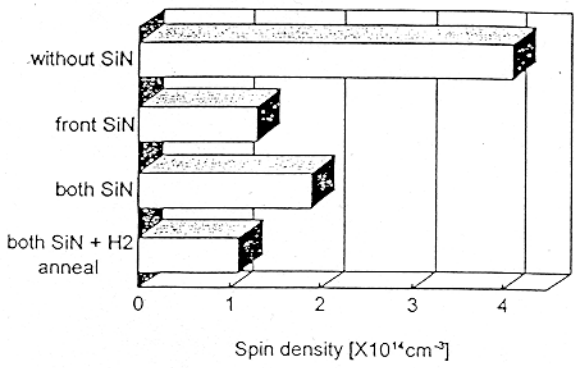


Fig.2 unpaired electron spin density of silicon samples with SiN film

Fig.1 hydrogen concentration profiles in silicon samples

①SiN film formation remove SiN film

②SiN film formation remove SiN film thermal treatment

③SiN film formation thermal treatment remove SiN film

3. SiN deposition method

The direct plasma CVD method is generally used as shown in Fig.3. This technology will progress by the development of performance improvement and mass production process. Recently the remote plasma CVD method in Fig.4 and the Cat-CVD method in Fig.5 have been developed. The remote plasma CVD and the Cat-CVD decrease the damage on surface of substrate in comparison with the direct plasma CVD. In Cat-CVD method, deposition gases are decomposed by the catalytic cracking reactions of a heated tungsten catalyzer placed near substrates, and so that SiN films are formed without any help from plasma or photochemical excitation(4). These films showed good properties for the application as device passivation films. Table1 shows the growth conditions of SiN films. The minimum value of the surface state density is $3.2\times10^{11}cm^{-2}eV^{-1}$. The film is almost stoichiometric composition

Parameter	
Flow rate SiH4(sccm) NH3(sccm)	0.5 60
T substrate(℃)	300
T catalyzer(℃)	1700-1800
Pg(mTorr)	10

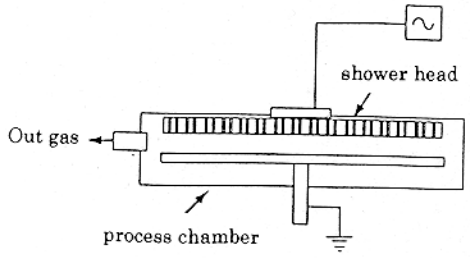


Fig.3 schematic diagram of direct PECVD

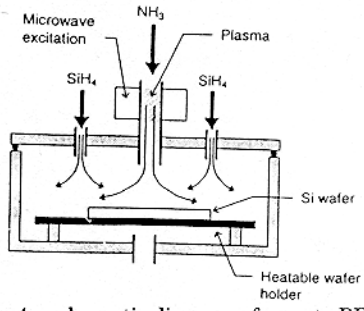


Fig.4 schematic diagram of remote PECVD

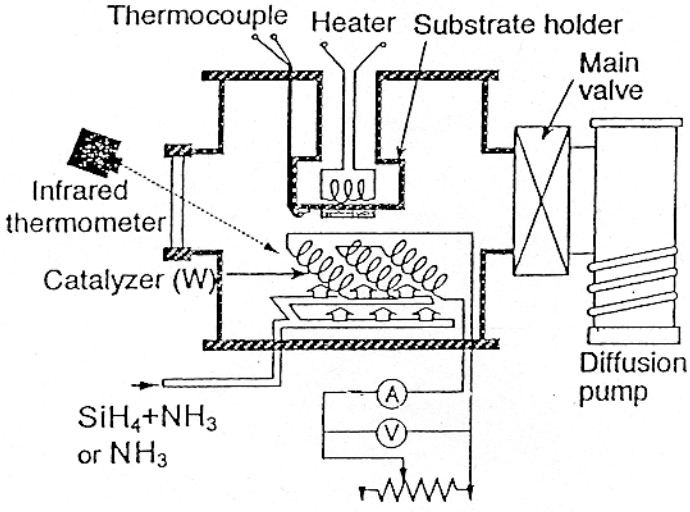


Fig.5 schematic diagram of Cat-CVD

4. mass production

Though there is scarcely any practical PECVD machine for mass production, Kyocera realized the practical use of PECVD-SiN process into mass production 15 years ago. But in the future higher efficiency and lower cost will be required with scale up of production. Fig.6 and Fig.7 show the schematic diagram of mass production machine.

Subjects for development are as follows.

(1) high throughput : 1800wafers/hr (15cm×15cm size)

—high growth rate : over 20A/s

—large area electrode : over 1m×1m

(2) improvement of operation rate

—self-cleaning

—simple maintenance

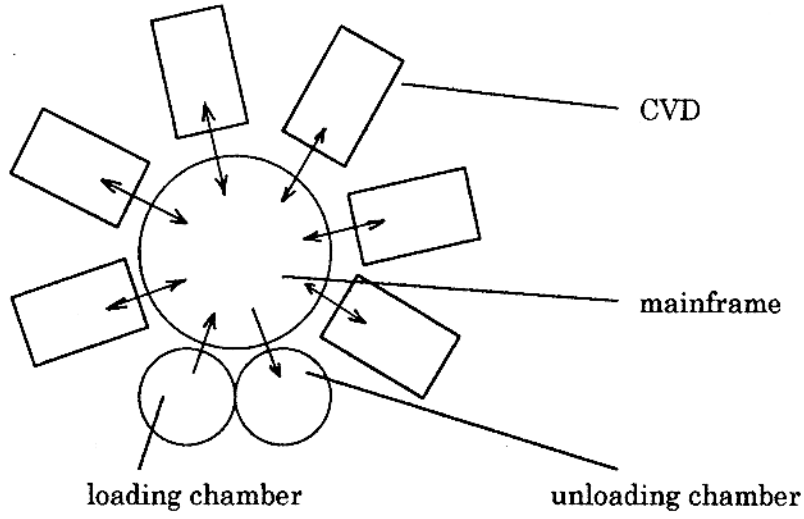
(3) reduction of particles

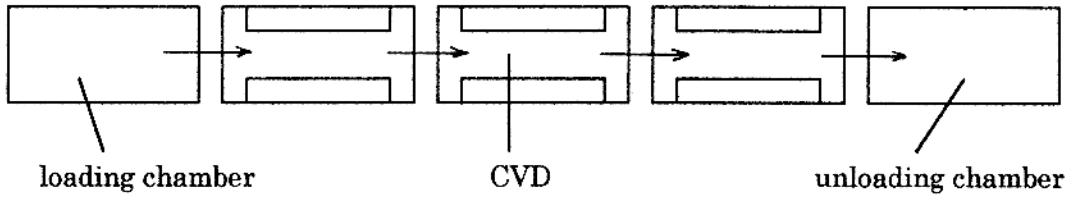
—not use susceptor

—self-cleaning

(4) reduction of machine cost

—standardization of machine specification





5. conclusions

Practical use of crystalline silicon solar cells has been starting. In recent years, improvement of efficiency and reduction of cost have made remarkable progress. But higher efficiency and lower cost will be required for large scale practical use. In the future SiN process technology will be very important for high efficiency and low cost crystalline silicon solar cells.

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Effects of Al-Gettering and Al-Indiffusion Induced Back-Side-Field on the Efficiency of Si Solar Cells

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ABSTRACT

The process of impurity gettering from Si by an Al layer for solar cell applications and the device operation resulting from it are modeled simultaneously. The enhancement of the solar cell efficiency due to the gettering is evaluated. In addition to the gettering, Al indiffusion, which occurs during gettering, is taken into account, and the effect of the created back surface field (BSF) is analyzed. It is shown that, for solar cells fabricated from low quality multicrystalline Si, the efficiency gain is primarily due to gettering, whereas BSF may play a more significant role in solar cells made of Si of high purity. The model allows to work out an optimum temperature regime for both processes.

Introduction

Impurities and imperfections serve as charge carrier recombination centers in Si crystals and can significantly reduce the efficiency of solar cells. Deposition of Al on the wafer surface and annealing at temperatures from 700 to 1200 °C provides gettering effect and can significantly increase minority carrier lifetime. In electronic grade CZ Si, impurities are in dissolved state, and can be gettered comparatively rapidly. In low cost CZ or multicrystalline Si, impurities are present in both dissolved and precipitated state. Gettering of precipitated impurities takes significantly longer time because the precipitates serve as sources that release impurities into the solid solution very slowly during gettering. Using computer modeling of the process, it was shown[1] that by choosing a proper temperature regime, the needed process time can be greatly reduced. It is highly desirable to be able to predict the influence of the impurities remaining in Si on the performance of the SC. Since the recombination centers located at different depth have a different influence on the SC performance, it is necessary to know the depth profiles of impurity concentration for accurate analysis. In practice, simultaneously with gettering, an indiffusion of Al into Si also occurs. Al acts as a p-type dopant, and thus, in cells with p-type bases, a gradient of p-doping concentration is created near the back surface, giving rise to BSF. It provides an additional driving force for the diffusion of electrons towards the front surface, improving their collection and increasing the efficiency of the cell.[2] Earlier attempts to separate effects of gettering and BSF did not include modeling of the gettering process.[3] In order to optimize the process of Al gettering and indiffusion to obtain maximum efficiency enhancement due to both increase of lifetime and BSF and, at the same time, to shorten the process, a model that incorporates gettering and indiffusion has been developed. It allows to predict the achieved efficiency enhancement at any stage of the process by modeling of a SC performance based on the obtained impurity depth profiles.

Modeling

A detailed description of the modeling of gettering process of dissolved and precipitated impurity in Si by an Al layer is given elsewhere.[1] It is described by the following set of equations:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} + 4\pi r C_{ppt} D\left(C^* - C\right), \tag{1}$$

$$C^* = C^{eq}\exp\left(\frac{2\Omega\varepsilon}{rk_B T}\right), \tag{2}$$

$$\frac{dr}{dt} = -\frac{\Omega D}{r}\left(C^* - C\right), \tag{3}$$

$$\frac{dC_{get}}{dt} = -\frac{D}{d_{get}}\frac{\partial C}{\partial x}\bigg|_{x=d_{Si}}, \tag{4}$$

$$C_{get} = mC(d_{Si}), \tag{5}$$

where x is the depth from the front surface of the substrate, Al-Si interface being at $x = d_{Si}$, C is the impurity (metal) atom concentration in the matrix, C^* is the impurity dynamic equilibrium concentration at the interface of Si and a precipitate of radius r, C^{eq} is the thermal equilibrium concentration of the impurity, C_{get} is the impurity concentration in the Al layer, C_{ppt} is the precipitate concentration, Ω is the volume of precipitate per one impurity atom, ε is the precipitate-matrix interfacial energy density, k_B is Boltzmann's constant, d_{get} is the thickness of the getter layer, and m is the segregation coefficient of the impurity between Al and Si. For simplicity, it is assumed that the precipitates are spherical in shape, and the impurity diffuses sufficiently fast in the liquid Al layer, so that its concentration can be considered uniform in that layer. It is noted that Eqs. (1)-(5) apply to the precipitate growth as well as dissolution processes. Solution of this system of equations yields depth profiles of impurity concentration and precipitate sizes at any instant during the process. They can be translated into the recombination rate as function of depth. Generation rate as function of depth can be easily obtained based on the spectral photon flux density of incident light and the absorption coefficient of Si. The reflection of light from the back surface towards the front of the substrate should also be taken into account. Indiffusion of Al into Si is described by diffusion equation, which allows to obtain Al (and hence, p-doping) depth profiles.

Effect of Al gettering and indiffusion on the efficiency of a SC can be evaluated by modeling carrier diffusion, drift, recombination, and generation in the SC. In p-base layer, the flux density of electrons can be expressed as

$$J_n = -D_n\left(\frac{dn}{dx} + n\frac{d\ln N_a^-}{dx}\right), \tag{6}$$

where D_n is electron diffusivity, n is electron concentration, and N_a^- is the p-dopant concentration. In steady state, taking into account generation and recombination

$$\frac{dn}{dx} = \frac{1}{D_n}\left[\int_{d_{Si}}^{x}\left(g - (n-n_0)r\right)dx + \left(n(d_{Si}) - n_0(d_{Si})\right)s\right] - \frac{n}{N_a^-}\frac{dN_a^-}{dx}. \tag{7}$$

where n_0 is the equilibrium electron concentration, r is the recombination constant obtained from impurity concentration profiles, and s is the surface recombination velocity. A similar equation can be written for the hole concentration p in n-emitter. Each of these equations lacks a boundary condition. One boundary condition can be deduced from the fact that at the p-n junction,

$$(p - p_0)N_d^+ = (n - n_0)N_a^- . \quad (8)$$

The other boundary condition depends on the external load of the SC. For instance, the regime of open circuit corresponds to zero flux of carriers into the junction, and the short circuit regime requires that $p = p_0$ and $n = n_0$. From the practical point of view it is desirable to analyze the regime of maximum power output, which corresponds to the maximum of the product of the potential difference across the p-n junction and the sum of carrier fluxes into the junction. The latter condition is used for further analysis.

The implemented model does not take into account Auger recombination, reflection of light from the front surface, front and back contact resistance, resistance of the semiconductor itself, change of concentration of majority carriers, change of the back surface reflection due to Al-Si alloying, and various factors that may influence the efficiency of cells, but are not significantly affected by Al gettering and indiffusion. It allows to predict the results of the process and separate the effects of gettering and BSF.

Results and discussion

For the modeling, Fe was used as a sample impurity. Multicrystalline Si wafer was assumed to be saturated with Fe at 1100 °C, and 10^{10} cm^{-3} of Fe precipitates formed so that thermal equilibrium was reached in the solid solution of Fe in Si at 700 °C. It is assumed that atoms of Fe are the only recombination channel responsible for the lifetime of minority carriers in Si bulk. Other used parameters are: doping of p-base 10^{17} cm^{-3}, doping of n-emitter 10^{19} cm^{-3}, surface recombination velocity on the back side 10^6 cm/s, surface recombination velocity on the front side 10^4 cm/s, wafer thickness 400 μm, depth of p-n junction 0.5 μm, reflectivity of the back surface 0.8, irradiation spectrum – black body at 5762 K with the total energy flux density corresponding to AM0. The temperature of the gettering process modeled was constant, 900 or 1000 °C. Same parameters were assumed for single crystalline Si, except for the impurity saturation temperature of 700 °C and absence of precipitation. For the same process, the cell operation was modeled and its efficiency was calculated in three ways: taking into account just the effect of the BSF due to Al indiffusion, or just the effect of gettering, or both. Results of the modeling are shown in the figure. It can be seen that in multicrystalline Si, initially the efficiency of the SC drops due to the dissolution of precipitates, and transition of Fe atoms into a more electrically active state. This explains the observed drop of solar cell efficiency as a result of gettering.[4] When all the precipitates are dissolved, the concentration of dissolved Fe atoms starts to drop, which results in the gradual efficiency increase until equilibrium is reached. Up to this point, there is almost no change of efficiency due to the BSF. Only longer processing times yield noticeable efficiency increase. It appears that the BSF does not increase the efficiency of a SC made of low purity material if there is no gettering. The BSF is also found to be more beneficial in high purity material. The relative role of the BSF becomes more pronounced if the process of Al gettering and indiffusion is conducted at a higher temperature because the BSF effect tends to increase with the process temperature, whereas the ultimate efficiency of gettering decreases. The role of the BSF is also higher for the SC with lower p-doping level of the base.

For the purpose of this modeling, it was assumed that Fe atoms and precipitates are the only recombination channels in the Si bulk. Other metallic impurities responsible for recombination can be gettered as well, but carbon and oxygen precipitates, possibly including metal atoms, can't be gettered and may put a limit on the ultimate efficiency of gettering. Those defects may be responsible for higher than predicted bulk recombination rate and lower the SC efficiency.[5]

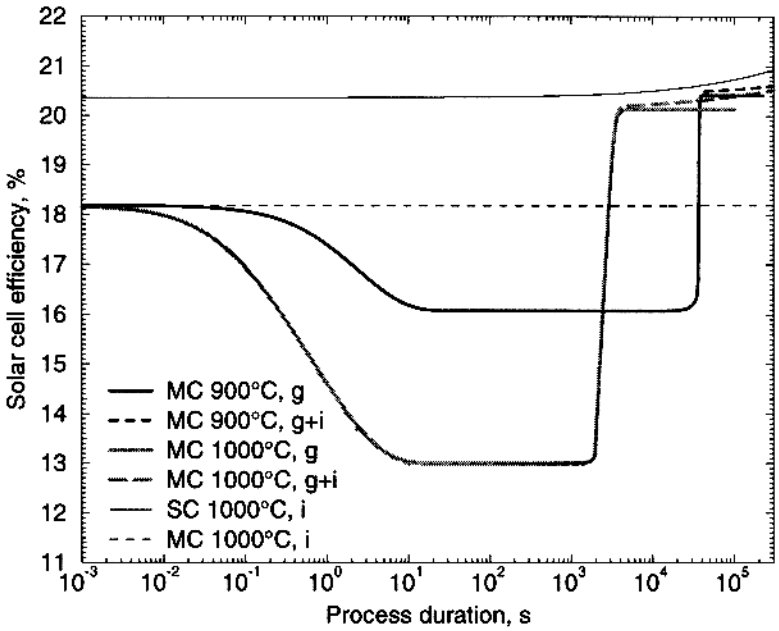

Fig. 1. Calculated solar cell efficiency as a result of Al gettering and indiffusion. Either both factors were taken into account (g+i), or just one – gettering (g) or indiffusion (i). Modeling conducted for multicrystalline low cost Si substrate (MC) or high purity single crystalline Si cells.

Conclusion

Modeling of the process of Al indiffusion and gettering with instant evaluation of obtained efficiency of the solar cell has shown that, for low cost multicrystalline Si, gettering provides a significant improvement of SC performance. BSF due to Al indiffusion plays a significant role for high purity material, and gives some additional improvement for the material that has been gettered. However, BSF is not effective by itself in low cost material. At higher processing temperatures, the role of BSF increases and the role of gettering decreases. Also, at lower p doping level of the base layer, BSF provides greater efficiency improvement.

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Low Temperature Silicon Doping Using Pulsed Laser

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Reduction of degradation losses in Cz-Si solar cells

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Abstract
The reduction of the lifetime degradation losses in Cz-Si solar cells offers a potential for a significant increase of cell efficiency. The major components of the metastable defect underlying the lifetime degradation can be concluded from a couple of recent experimental results: boron and interstitial oxygen. Consequently, one strategy in order to reduce the degradation extent is obvious: the reduction or avoidance of either boron or interstitial oxygen in the starting material. If this is not possible the process should be optimized in order to reduce the defect concentration. Both possibilities have been successfully investigated resulting in excellent efficiencies up to 22.5 %.

1 Introduction

The minority carrier lifetime degradation observed in p-type Cz-Si is induced by carrier injection or illumination[1-6]. After an illumination of about 12 h AM1.5 (depending on the doping level) the lifetime is reduced exponentially to a (fortunately) stable end value. This lifetime degradation can be completely reversed by an anneal step at around 200°C in room ambient.

Since the absolute efficiency loss is about 1 to 1.5 % for cells with high-efficiency structure and about 0.6 % for cells with industrial structure the reduction of the extent of degradation is quite valuable.

2 Origin of the metastable defect

From a couple of recent experimental results it is quite obvious that boron and oxygen are the major components of the metastable defect underlying the Cz-specific lifetime degradation:

- Boron-doped p-type FZ silicon free of interstitial oxygen and other contaminations shows no lifetime degradation.
- Boron-doped p-type FZ silicon intentionally contaminated with oxygen (ρ_{base} = 6.3 Ω cm, $[O_i] = 5.4 \times 10^{17}$ cm^{-3}) shows a degradation behavior very similar to the one observed in boron-doped p-type Cz-silicon, although no other contaminations are present in these FZ wafers [6].
- Phosphorus-doped n-type FZ silicon intentionally contaminated with oxygen ($[O_i]=4.2 \times 10^{17}$ cm^{-3}) as in (2) shows no lifetime degradation [6].
- Phosphorus-doped n-type Cz silicon shows no degradation [4].
- Boron-doped p-type MCz with a very low oxygen conc. (< 1 ppma)silicon shows no degradation[7].
- Gallium-doped oxygen-contaminated Cz silicon (ρ_{base} = 3.4 Ω cm, $[O_i] = 6.8 \times 10^{17}$ cm^{-3}) shows no degradation[4,7].

Schmidt et al.[4] have suggested a model assigning the origin of the metastable defect to the B_iO_i complex. The B_iO_i defect was observed by Kimerling et al.[8] on electron-irradiated Cz-Si. The electron irradiation strongly increases the Si_i concentration and thereby the B_i concentration. Their DLTS

measurements have shown that the DLTS-peak indentified as the B_iO_i defect ($E_v + E_t = 0.29$ eV) vanishes after an anneal in the temperature range from 150°C to 200°C. However, no reactivation of the defect by illumination or carrier injection was reported. Both, the metastable defect behaviour and the correlation with boron and oxygen observed by the lifetime measurements described here are in agreement with their results. However, a non-ambiguous correlation is not possible especially since the results reported in this article are obtained on non-electron-irradiated Cz-Si. A direct determination of the defect in non-irradiated samples with DLTS was not successful yet [1].

In order to determine this correlation more quantitatively we have measured the extent of lifetime degradation, i.e. the lifetime after an FGA, τ_0, and after an illumination of 24 h with AM1.5, τ_d, on different Cz-materials from different manufactures. The lifetime measurements were performed using microwave-detected photoconductance decay (MW-PCD). Although the capture cross section, σ_n, of the metastable defect is not known, it is possible to determine a normalized defect concentration, N_t^*, with these two values from:

$$N_t^* := \sigma_n v_{th} N_t = \frac{1}{\tau_d} - \frac{1}{\tau_0} \qquad (1)$$

assuming that (i) the metastable defect is completely deactivated after the anneal step and completely activated after the illumination step and (ii) all additional defects possibly contained in the material are not affected by the anneal/illumination cycle.

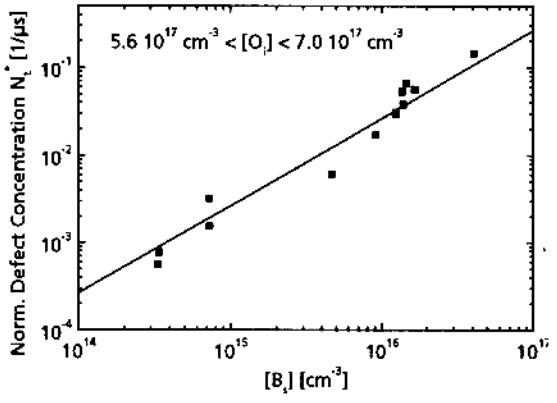

Fig. 1 Normalized defect concentration N_t^* (:= $1/\tau_d - 1/\tau_0$) vs. boron concentration for Cz samples with an interstitial oxygen concentration between 5.6 and $7.0 \cdot 10^{17}$ cm^{-3}.

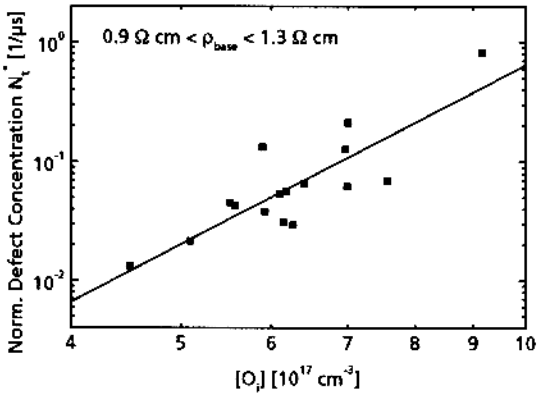

Fig. 2 Normalized defect concentration N_t^* (:= $1/\tau_d - 1/\tau_0$) vs. interstitial oxygen concentration for boron-doped Cz samples with base resistivities between 0.9 Ω cm and 1.3 Ω cm.

In Fig. 1 the correlation between the normalized defect concentration and the boron concentration for Cz-samples with nearly the same interstitial oxygen content is shown. The correlation can be described by a linear fit. In Fig. 2 the correlation between the normalized defect concentration and the interstitial oxygen concentration for boron doped Cz samples with nearly the same boron concentration is shown. Although the scatter of the data is higher compared to Fig. 1 we can draw a clear conclusion: the

[1] Note: The electron capture cross section of B_iO_i defect is extremely high [9]. Thus, even a small defect concentration not detectable with DLTS would result in a lifetime reduction.

measured data can not be fitted by a linear function, the correlation is strongly superlinear. The fit indicated in Fig. 2 is a function with exponent 5.

Additionally, we analyzed the dynamics of the defect reactivation after the anneal. The time constant decreases with increasing boron concentration. A material with a doping concentration of $4.3x10^{16}$ cm^{-3} "needs" 3 h of an illumination with 50mW/cm^2 for the reactivation, while a material with $1.3x10^{16}$ cm^{-3} "needs" 18 h.

3 Reduction of lifetime degradation

There are several strategies to reduce the extent of lifetime degradation in Cz-Si, which can be classified in two groups: (i) changes in the starting material or (ii) reduction of the defect concentration during the solar cell process.

3.1 Usage of material with very low concentrations or even free of interstitial oxygen, as MCz-Si or FZ-Si.

While the usage of expensive FZ-Si is only feasible for high-efficiency cells, MCz-Si could easily increase the performance of Cz-Si cells due to its very low interstitial oxygen content. Very high lifetimes were reported for low-resistivity MCz-Si[10]. In a recent experiment[7] we have used boron-doped 1.2 Ω cm MCz with an interstitial oxygen concentration of 0.5 ppma. The lifetime of this material was above 1 ms and even more important it was not degraded by illumination. Stable efficiencies up to 22.3 % confirmed independently[2] reflect this excellent characteristics.

3.2 Usage of n-type Cz-Si.

Although, in principle the usage of n-type Cz-Si is possible, considerable efforts would be necessary to change the common solar cell technology (e.g. formation of p^+-emitters).

3.3 Substitution of boron by other acceptors as gallium in p-type Cz-Si.

This approach has been pursued in a recent activity[7,11]. Gallium doped wafers with a significant oxygen contamination (13.8 ppma) grown by Shin-Etsu were used. The material exhibits a very high starting lifetime of 782 µs. No degradation was observed. An excellent solar cell performance with confirmed efficiencies up to 22.5 % was achieved in our lab[7]. The only disadvantage of this approach is the low segregation coefficient of gallium in silicon, resulting in a higher resistivity variation over the crystal length compared to boron doping.

3.4 Reduction of boron doping concentration in p-type Cz-Si (e.g. from 1 Ω cm up to 7 Ω cm).

The highest efficiencies on boron-doped oxygen-contaminated in our lab were obtained on relatively lowly doped material (6.8 Ω cm). Stable efficiencies up to 22.0 %[12] were achieved, but since the lower doping concentration does not allow a simple ohmic back contact, a back surface field is obligatory. This complicates the process sequence significantly.

3.5 Reduction of the Cz-specific defect concentration during the process

If standard boron-doped Cz-Si around 1 Ω cm with a significant oxygen concentration is used an improvement of the material has to be achieved during the process. Commonly high-temperature processes are thought to be detrimental for the minority carrier lifetime in Cz-Si. Nevertheless, we have

[2] Note: All efficiences reported in this article are obtained by aperture area measurements, thus, fingers and busbar lie within the illuminated area.

shown that it is not only possible to avoid such detrimental effects, but even to increase the carrier lifetime [2,6].

Recently, the thermal oxidation process necessary for masking oxides and passivation layers was studied comprehensively by experimental design methods. The ramp-up, oxidation and ramp-down parameters were varied and the effect on the carrier lifetime was studied on different Cz materials with different interstitial oxygen and boron concentrations. A FZ-reference wafer was added in order to control the passivation quality of the resulting oxide. The Cz materials under investigation had initial lifetimes ranging from 3 µs up to 12.7 µs, i.e., no "academic" hyperpure material was chosen.

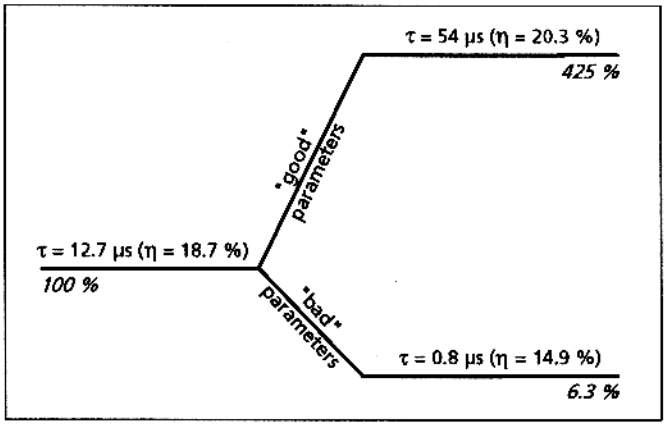

Fig. 3 Influence of process parameters of a thermal oxidation at 1050°C on the stable bulk lifetime. The efficiencies in the brackets are calculated from the measured bulk lifetimes for a simple high-efficiency cell.

It was possible to distinguish between two principal effects. If the ramping conditions were chosen in a wrong way the bulk lifetime was reduced strongly independently of the plateau conditions. If the ramping conditions were chosen properly an increase of the stable bulk lifetime and a reduction of the extent of degradation, respectively, was observed. For properly chosen ramping parameters an improvement was obtained within the whole oxidation parameter range, but best results were obtained for temperatures above 1000°C.

Fig. 3 visualizes the strong influence of the process parameters on the stable lifetime after an illumination of 30 h. Additionally to the measured bulk lifetimes, calculated cell efficiencies which could be achieved with the corresponding lifetimes are given.

The improvement of the material achieved by high-temperature process steps is also observed for the normalized defect concentration, N_t^*. In Fig. 4 N_t^* is shown in the starting material, after an optimized oxidation and after the complete solar cell process. The lifetimes in the first two cases were determined using MW-PCD in the third case we have evaluated spectral response measurements. For all the investigated boron-doped materials with different resistivities and oxygen concentrations a clear reduction of the defect concentration after the oxidation and even more after the whole process was observed.

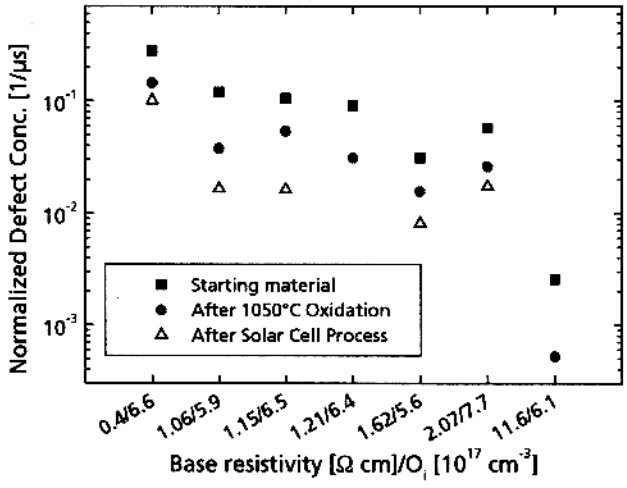

Fig. 4 Reduction of the normalized defect concentration by a thermal oxidation and a complete solar cell process.

4 Conclusion

Although the microscopical background of the metastable defect underlying the lifetime degradation induced either by light illumination or carrier injection is not clarified it seems to be quite obvious that boron and oxygen are the major components of this defect.

In order to reduce the defect concentration or the lifetime degradation several strategies can be followed. The substitution or reduction of boron as the dopant was already quite successful: With lowly doped Cz-Si (7 Ω cm) cell efficiencies of 22.0 % have been obtained, while gallium doped Cz-Si has even yielded in 22.5 %. In both cases no degradation was observed. The reduction of interstitial oxygen in boron doped Cz-Si using the MCz method was very successful too and resulted in cell efficiencies of 22.3 %. If standard boron-doped Cz-Si with a not negligible interstitial oxygen concentration is used, an improvement of the material during the solar cell process has to be applied. It was shown that high-temperature steps with temperatures above 1050°C can either deteriorate the minority carrier lifetime or if proper process parameters are chosen can improve the material quality significantly. With an optimized oxidation step it was possible to increase the stable bulk lifetime by a factor 2-4.

Acknowledgments

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Review of Ohmic Contacts to Silicon Solar Cells

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Introduction

In a properly designed p-n junction solar cell, the electrons move to the metal electrode which contacts the n-type silicon, and the holes move to the metal electrode which contacts the p-type silicon. These contacts are vitally important to the performance of the cell, since forcing current across a high resistance silicon/metal interface or through a high resistance electrode material robs useful power from the cell. The total specific series resistance of a one-sun cell, including interfaces and electrode material, should be less than 1 Ω-cm^2. Such a series resistance corresponds to a power loss of approximately 1 mW/cm^2 from the cell, or 1% (absolute) in efficiency.

It is well known that a number of factors contribute to the total series resistance, including dimensions and resistivity of the metal contacts, sheet resistance of the emitter diffused layer, resistivity and thickness of the silicon substrate, and contact resistance associated with the metal/silicon interface. For commercial terrestrial solar cells with screen-printed contacts, the dominant factor is usually interface resistance. This is at least partly because the contact area is kept as small as possible in order to minimize the power loss from grid shadowing. Such a trade-off results in the grid covering approximately 7% of the illuminated area, which corresponds to a power loss of about 1 mW/cm^2 from the cell. With series resistance losses and shadowing losses balanced in this way (1 mW/cm^2 each), an optimum contact system is realized.

Interface Resistance

Since the resistance associated with the metal/silicon interface tends to dominate the series resistance, it is important to look for ways to reduce it. There are three distinct approaches to reducing this interface resistance [1]. First, it is possible, in principle, to design a low-resistance accumulation contact by a proper choice of metal work function. According to this viewpoint, if the work function of the contact metal is less than the work function of the silicon substrate, an accumulation contact to n-type silicon will be obtained. Conversely, if the work function of the contact metal is greater than the work function of the silicon substrate, an accumulation contact to p-type silicon will be made. For these choices, the Schottky barrier height is negative, and majority carriers can flow freely between metal and silicon. Unfortunately, in practice the barrier height is found to

be nearly independent of the work function of the metal. A high-resistance depletion contact is then formed with a positive barrier height to both n-type and p-type silicon, rather than the desired accumulation contact. This behavior is generally attributed to silicon surface states which pin the Fermi level at $\approx E_v + 1/3 * E_{gap}$. A second approach to achieving a low contact resistance is to damage the silicon surface. Such damage introduces a high density of defect levels in the silicon bandgap which supports the high recombination rate associated with ohmic contacts. However, such damage may also degrade minority carrier lifetime in the vicinity of the contact, and this can reduce V_{oc} as well as J_{sc}. In addition, damage contacts may be difficult to reproduce consistently. Ion beam damage has been used to create an ohmic contact to n-type silicon [2]. The third approach for achieving a low contact resistance, which is nearly universally implemented, is to dope the surface of the silicon heavily. This causes the depletion type barrier to become so narrow that carriers can tunnel through it in a process known as field emission. Since this type of contact is ubiquitous for solar cells, it alone will be considered further.

In order for a contact to pass current by field emission, a fairly demanding requirement is placed on the concentration of dopant atoms at the surface of the semiconductor [3]. For n-type silicon, this dopant concentration must be $\geq 1 \times 10^{19}$ atoms/cm^3 (200 ppma). The requirement is less severe for p-type silicon, where the surface concentration must be $\geq 1 \times 10^{17}$ atoms/cm^3 (2 ppma). In making contact to an n^+ layer, screen-printed silver is usually used. With glass frit included in such a paste to improve metal-to-silicon adherence and metal in the form of small discrete particles, the actual contact area is smaller than the apparent contact area. For such contacts, it is generally necessary to dope the surface of n-type silicon to a sheet resistance of 45 Ω/□ or less in order to achieve an acceptable interface resistance. Such heavy doping results in a fill factor of approximately 0.75. However, this doping reduces the blue response of the cell because of the high recombination rates associated with the heavily-doped layer. In addition, surface passivation is rendered inoperative with such heavy doping, as emitter recombination dominates surface recombination. Such a cell is sometimes said to have an "opaque" emitter, since carriers in the base are not able to "see" the passivated surface through the heavily-doped emitter. Thus, an acceptable interface resistance is achieved, but only at the expense of reduced J_{sc} and V_{oc} if the emitter remains heavily-doped and uniform everywhere.

Selective Emitters

To maximize the energy conversion efficiency it is often desirable to have a relatively low surface doping concentration everywhere on the illuminated surface of a cell except directly beneath the metal electrode, especially for an n-type surface. Such an arrangement is sometimes referred to as a "selective emitter" in that the region beneath the contact metal is selected to have a higher doping density than the region beside the contact metal. Several approaches for achieving such a selective emitter have been reported. In the emitter etch-back process [4], the emitter is initially heavily doped

everywhere and gridlines are screen-printed and fired. These gridlines then act as a mask while the surrounding emitter is partially removed by reactive ion etching. This etching also imparts a texture to the surface. In the selective diffusion process [5, 6], a phosphorus dopant paste is applied by screen-printing in the same pattern as the contact grid. During the ensuing high-temperature step, the silicon beneath the phosphorus source becomes heavily doped while the silicon between the phosphorus screen-printed lines is only lightly doped. This lightly-doped region, created indirectly via gas phase transport of phosphorus, becomes the emitter of the cell. After stripping the diffusion glass, metal lines are screen-printed over the heavily-doped areas, which requires an alignment. Laser overdoping [7] is a variation of the selective diffusion process in which the silicon surface is initially lightly doped everywhere. A laser is then used to melt and dope heavily that part of the silicon surface to be covered with the metal grid. Alignment of the metal grid to the laser-treated area is required. Of these methods for obtaining a selective emitter with screen-printed contacts, the highest efficiency (17.1%, 100 cm^2 cell area) has been reported for the selective diffusion process [6], as applied to a 22 Ω-cm CZ substrate.

Alloyed Contacts

Screen-printed aluminum is widely used in commercial terrestrial cells to create an effective back-surface-field by alloying with p-type silicon. Screen-printed aluminum has also been used as a front grid contact to a p-type emitter in an n-base cell [8]. The aluminum-silicon eutectic metal is sufficiently conductive to serve as a grid material, while the nature of aluminum alloying provides for a deep p^+ region immediately below the eutectic contact. A selective emitter structure, which is self-aligned, naturally follows from this alloyed aluminum front contact. In addition, alloying ensures good adherence between the eutectic metal and the silicon substrate. To achieve a higher p-type doping concentration, a commercial aluminum screen-printing paste was enhanced by adding 1% boron [9]. With aluminum serving as a vehicle by which boron is incorporated into the silicon during the alloying process, a peak concentration of 3×10^{19} cm^3 was achieved. This is a factor of 10 higher than that obtained by aluminum alone. Also using aluminum as a carrier for boron, the performance of an aluminum-alloyed back-surface field was found to be improved with the addition of boron [10]. In this case sputtering was used to deposit the aluminum-boron mixture. Like aluminum, silver also forms a eutectic with silicon albeit at a higher temperature (835°C) than aluminum (577°C). Just as boron can be introduced into silicon via the aluminum alloying process, other dopants can be introduced into silicon by the silver alloying process. For example, antimony was introduced into silicon at a concentration of 2×10^{18} cm^3 by alloying a sputtered layer that was 1.1% (weight) antimony in silver at 900°C [11]. Such an alloyed silver contact is adherent and solderable.

Favorable By-Products of Contact Formation

One way by which the cost of silicon solar cells can be reduced is by realizing more than one desirable cell feature in a single processing step. Creating the contact offers opportunities along these lines. For example, under appropriate processing conditions an aluminum back metal can serve as a contact, a source of dopant to create a p^+ layer, a back surface reflector, and a source of back surface texturing for diffuse scattering of light [12]. Another example concerns the firing of silver paste through a SiN_x AR coating to contact the underlying silicon emitter at approximately 750°C. This temperature is sufficiently high to activate the hydrogen associated with the PECVD SiN_x deposition in order to passivate surface and bulk defects [13, 14].

Summary

An ideal contact material has a high electrical conductivity, makes a mechanically strong bond to the silicon with low interface resistance, does not degrade the electrical quality of the silicon by introducing sites where electrons and holes can be lost by recombination, and is solderable. This contact material should be inexpensive and should lend itself to being applied by an economical process, such as screen printing. A cost-effective process should exist to form a selective emitter structure, preferably in such a way as to realize other cell enhancements as by-products. Commercial one-sun terrestrial solar cells do not include selective emitters at this time. Further developments in emitter etch-back, selective diffusion, and alloyed contact processes are likely to lead to a production-worthy selective emitter structure.

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Review of Issues for Development of Self-Doping Metallizations

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Issues

The concept of a self-doping metallization allows formation of a junction or back surface field at the same time a contact metal is applied. The basic technique is to apply a carrier metal including a dopant species to the silicon. This would be followed by a high temperature growth cycle in which a doped layer is grown by liquid phase epitaxy, LPE. LPE is a crystal growth technique in which a solute is dissolved in a solvent. The solution is cooled, which allows the solute to grow out epitaxially on a substrate. The technique allows growth to proceed at temperatures lower than the crystal melting point. The temperature must be higher than the solute/solvent eutectic temperature. LPE has been used for silicon growth, resulting in high crystal quality[1].

The self-doping metal concept utilizes the same physical phenomenon as LPE. However, the carrier metal remains in place forming an ohmic contact to the grown silicon. The process steps also are analogous to the familiar screen printing process for forming contacts, in that metal is applied in a pattern and is followed by a firing step. However, the end result is very different. It is important for a screen printing fire step to be below the eutectic point of the metal-silicon system. For a self-doping metal, it is required that the firing, or growth step, occur above the eutectic temperature. The screen printed contact requires a doped layer to be in place before contacts are applied, but the self-doping metallization forms its own doped layer.

The idea of using a liquid phase grown layer for forming junctions is not a new one, indeed the earliest semiconductor junctions were formed from the melt. Solid phase diffusion quickly surpassed melt grown junctions and has since been the standard. However, the current research focus for silicon solar cells is to develop processes which can produce high efficiency cells and be compatible with high throughput low cost processing. The concept of a self-doping metal can potentially lower the manufacturing cost of solar cells by combining process steps.

Self doping metals are somewhat restricted in their application due to the fact that the carrier metal remains unremoved. The junction formed is therefore entirely covered by metal, i.e. the junction area equals the contact area. This, however, can be an asset in the right kind of cell structure. For example, a selective emitter on a front contacted cell could be formed from self-doping metals, which would be self-aligned. One device structure to which the self doping metal is ideally suited is the Interdigitated Back Contact (IBC) cell. This cell structure has a junction only on the back surface and interdigitated opposite polarity grid lines. This cell has demonstrated high efficiency both as a concentrator solar cell and a one-sun cell using photolithography, conventional diffused junctions, and evaporated metal contacts[2]. Since the junction need not extend over the entire surface, it can be envisioned that a self doping metal can form this junction.

The self-doping metal is an immature technology, and hence, has a number of issues that require attention. Choice of dopant and carrier metal are primary considerations. Additionally, wetting of the underlying silicon is a well known difficulty

with liquid phase growth of silicon. Composition and quantity of the self-doping metal, temperature and time of the growth cycle will determine the junction depth and doping profile, which will in turn determine the junction's J_0, or effective SRV in the case of a back surface field. Contact resistance of the remaining metal to the underlying grown silicon is an important issue, and is expected to be lower than any other contact formation technology for a given silicon doping level due to the clean interface between metal and grown silicon. Lifetime issues are another critical factor. The carrier metal will be incorporated into the underlying silicon to an extent depending on the segregation coefficient, which can potentially degrade carrier lifetimes. It will be important to choose a carrier metal with both low levels of incorporation as well as benign recombination properties. The lifetime issue can also work in reverse. Most metallic impurities in silicon prefer to remain in the melt[3]. This is the principle used in zone refining. Hence, the self-doping metal may be used as a gettering agent. Its effectiveness will depend on the segregation coefficients of impurities in the melt, but also on the temperature and duration of the epitaxial growth cycle.

This paper will focus on the required growth conditions for self-doping metals and the various lifetime issues. Recent results for a novel self-doping metal system will be discussed briefly.

Growth Conditions

Self-doping metals use the same principles used in the growth of silicon from the liquid phase. In liquid phase growth, thick layers of silicon may be grown assuming that the melt contains enough dissolved silicon, or can be replenished during growth. The self-doping contact will typically only grow a thin layer, perhaps one micron, to be used as a diode emitter or back surface field. The quantity of metal deposited, and the solubility of silicon in the metal will determine the thickness of the grown layer.

Growth temperature is typically an important variable in LPE, since it determines the total amount of material which can be grown, as well as wetting of the substrate. In principle, there would be no need to exceed the eutectic temperature by any significant amount, assuming that an adequate thickness of silicon can be grown at the eutectic temperature. However, increased temperature may be desirable to enhance gettering efficiency of the melt.

Liquid phase grown silicon has shown high material quality[1]. One of the prerequisites for this is to grow the silicon with a slow cooling rate, so as to be near equilibrium. If the growth temperature of the self-doping metal system were to significantly exceed the eutectic temperature, then the literature suggests that the ramp down must proceed slowly, say < 50 C/hour[1]. In conventional liquid phase growth, when growth is terminated, the melt is removed from contact with the substrate. This typically occurs well above the eutectic temperature. Therefore, the self-doping metal system is unique in this respect. It is not clear how the growth conditions at the eutectic temperature will affect material quality of the grown silicon. In principle, a liquid eutectic compound can be cooled and separation of the components will occur, but it is not clear if the silicon component can be grown epitaxially. It is possible that spontaneous nucleation will occur in the melt and component separation will occur non-homogeneously, i.e. particles of solute scattered through the solidified solvent. It seems

likely that cooling will have to be slow when crossing the eutectic temperature. The silicon aluminum eutectic is commonly used as a back surface field, for which purpose it performs well, however, the requirements of a collecting junction are more stringent. The material quality of the silicon grown by the self-doping metal system will be an important research issue.

A more practical matter for self doping metals is the ability to wet the silicon surface. Wetting refers to the ability of the solvent to form a low contact angle with the substrate. If wetting does not occur, then the solvent will ball up on the substrate. Wetting of silicon by molten metals is very challenging due to the very stable native oxide[4]. In silicon epitaxy, liquid phase or vapor phase, the challenge is to reduce the native oxide before the growth cycle by eliminating water vapor from the growth ambient[5]. The self-doping metal system again presents a slightly unique perspective, in that the metal compound will be applied before any high temperature step. Any native oxide remaining on the surface prior to metal application will impede wetting. This is relatively easy to avoid if the metal compound is applied by sputtering. The silicon surface is simply back-sputtered before metal deposition. Our group has found this highly effective for wetting silicon from silver compounds. If the self-doping metal compound is to applied as a screen printed paste, then the situation becomes more difficult, perhaps more difficult than any other issue relating to self-doping metals. This is clearly an unresolved issue for the future of self-doping metals.

Lifetime Issues

The ideal choice for metal depends on a number of factors, such as the incorporation of metal into the grown silicon, lifetime impact of this incorporated metal, wetting of the silicon, resistivity of the metal, and its solderability. The best choices when considering resistivity and solderability are copper and silver. There are quite a few unknowns when considering silicon grown from a silver solution, but it appears that there are enough favorable properties to make silver the default choice for now.

The lifetime effect of impurities is dependent on their concentration, energy levels and capture cross sections. Hence, the concentration of the metal solvent incorporated into the silicon is an important factor. Like most metals, silver has a retrograde solubility in silicon, meaning that solubility of silver in solid silicon peaks at a temperature below the silicon melting point. The solubility of silver in silicon peaks at about 10^{16} cm^{-3} at 1300 C. Rollert, et.al. report silver solubility essentially constant at temperatures below 1000 C at $7*10^{14}$ cm^{-3}[6]. This paper gives an Arrhenius-type drop in the solid solubility at temperatures above 1100 C, and then notes that the drop in solid solubility ceases below 1000 C. This reported behavior is at odds with other transition metals, which show a continuous drop in solubility with decreasing temperature. Neglecting this flat region, the solid solubility drops quite rapidly with decreasing temperature.

There is very little data on the recombination properties of silver in silicon, however, Sze lists silver as having an acceptor level at 0.36 eV and a donor level at 0.33 eV, from the respective band edges[7]. These are similar to the energy levels of other lifetime killing impurities. However, capture cross sections are somewhat obscure. An early study of silver doped silicon was somewhat inconclusive[8]. Photoconductance decay measurements indicated the same minority carrier lifetime in samples diffused with

silver to the 10^{15}-10^{16} cm^{-3} range, as in un-diffused controls. The authors used this data to establish an upper limit on the capture cross sections of the silver impurity. The conclusion was that they were almost two orders of magnitude lower than those of gold in silicon, implying that silver is a much more benign impurity than gold.

Silver has a diffusion coefficient in silicon which is intermediate between fast and slow diffusers[9]. The diffusion coefficient is given in equation 1. At the silver-silicon eutectic temperature, this works out to 11 $\mu m/\sqrt{hr}$. If there are detrimental effects to silver incorporation then they will be confined somewhat near the surface, although deep enough to potentially affect collection efficiency.

$$D(T) = 6 * 10^{-5} e^{-1.15eV/kT} \quad cm^2/sec \qquad 1$$

The other side of the lifetime issue is the potential benefit of forming junctions by a molten metal solution. Metallic impurities prefer to remain in a molten metal, and hence, can be gettered from the silicon during the growth cycle. The gettering efficiency of the metal solution will depend on the distribution coefficient for the impurity-metal-silicon system, as well as the diffusion coefficient of the impurity in silicon. The distribution coefficient is the ratio of impurity concentration in the solid to that of the liquid. The distribution coefficient is difficult to obtain, but diffusion coefficients are well known. For example, the diffusion coefficient of iron in silicon is $1.06*10^{-6}$ cm^2/s at the silver-silicon eutectic[9]. This gives a diffusion length of 617 $\mu m/\sqrt{hr}$. This is adequate for gettering action.

Recent Results

One challenge of the self-doping metal system is to avoid shunting of the metal to the surrounding silicon. Since only the silicon directly underlying the metal is epitaxial silicon, there is very little margin for error when growing a layer of opposite conductivity type. This can be significant problem if the molten metal consumes some of the underlying silicon. In this case, the re-grown silicon will be no higher than the level of the surrounding silicon, hence, it is very easy for the metal to short out the junction. Our approach has been to use a self-doping metal compound incorporating silicon. This raises the metal to silicon interface above the level of the remaining silicon wafer. A compound of Ag/Si/B has been used successfully for creating p on n diodes. Films were applied by sputtering. A brief period of back sputtering was used to assure good wetting. Simple diode structures fabricated to date have shown an adequately low shunt conductance. A plot of the dark current-voltage characteristic of one of these diodes is shown in Figure 1. The substrates used were 0.3 Ohm-cm N-type CZ. The back side was heavily phosphorous diffused and contacted with Ti/Pd/Ag. This diode demonstrates a good I-V characteristic, demonstrating a good quality epitaxial junction. Future work will involve more characterization of the doping profile and silver incorporation. Also, formation of an N-type epitaxial layer will be pursued.

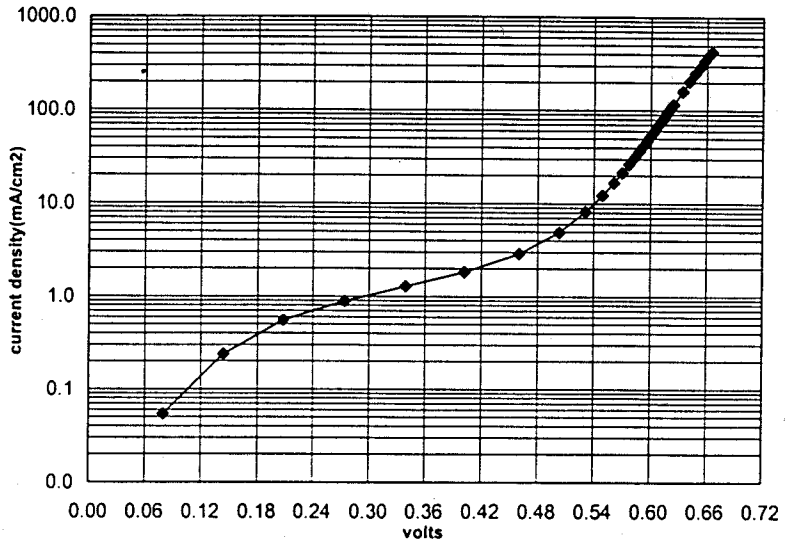

Figure 1. Dark I-V curve of p on n diode created from Ag/Si/B compound.

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Possibilities for Process-Control Monitoring of Electronic Material Properties during Solar-cell Manufacture

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Abstract— **The overall goal for process control in industrial solar cell fabrication would be to obtain the information usually gleaned from I-V curves and spectral response measurements at the earliest possible points in the fabrication process. The use of contactless quasi-steady-state minority-carrier lifetime measurements and probed voltage measurements can approach this ideal in many cases of interest.**

I. Introduction

The typical manufacturing processes for solar cells generally do not include much in-process monitoring of the electronic properties of the silicon wafer. Although high-efficiency solar cell processes on float-zone wafers have long used extensive process control using minority-carrier measurements, this has not been true in typical large-scale production of terrestrial cells. This fact has been primarily due to the difficulties encountered in the interpretation of the data from lower-quality silicon substrates. Recent research has applied new in-process diagnostic techniques to the optimization of the process design and fabrication for single- and multi-crystalline solar cells. By reviewing some of the recent R&D work and supplementing it with new results, several possible process-control applications to industrial processes are proposed and illustrated with examples.

Here, two methods for the electronic characterization of wafers will be demonstrated in detail as representative of the types of measurements that can be done on wafers at intermediate stages of a fabrication process. These are:

1) Minority carrier lifetime measurements using a steady-state photoconductance technique that determines lifetime over a range of light intensities(2-9).

2) Open circuit voltage vs. Illumination intensity(10)

Several points where process monitors can be used are shown in Table 1.

The monitoring of sheet resistance during processing is obvious and needs no discussion. If a photoconductance technique is used for the minority-carrier lifetime determination, often the dark conductance can be simply read off as a free byproduct of the photoconductance measurement. This can be done at any of the points shown in Table 1.

Table 1.

Process step	Electronic Process monitors		
	Sheet resistance	Lifetime	Voltage
Incoming wafers	X	X	
Etching		X	
Phosphorus Diffusion	X	X	X
Passivation &AR		X	X
Back metal/anneal	X	X*	X
Front Metal/anneal		X*	X

The lifetime measurement technique referred to here is the steady-state photoconductance or quasi-steady state technique as described in references 1-10. This method and the voltage measurements will be described in detail.

II. Lifetime Measurement Using the Steady-State or Quasi-Steady State Method.

In this method, a light is incident simultaneously on the wafer and a reference cell. The photoconductance in the wafer is determined by a contactless inductive technique. The incident light intensity is determined by a calibrated reference solar cell.

The lifetime is then calculated as:

1) Effective Lifetime = $\frac{K^* \text{ Photoconductance}}{\text{(Incident Light Intensity)}}$.

where K is a slowly varying function of the mobility of electrons and holes as well as the optics of the wafer under test. The principles of steady-state photoconductance lifetime measurement are detailed in (1-9)

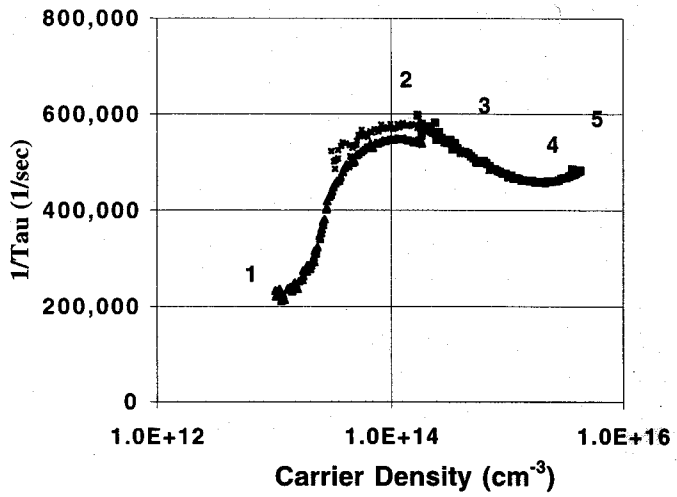

Figure 1. The inverse of the effective lifetime vs. carrier density for a multicrystalline wafer as determined by a steady-state photoconductance measurement.

The lifetime measured in this way is shown in Figure 1 for a multicrystalline wafer. The effective lifetime is a combination of surface and bulk properties of the wafer. Several regimes are shown. At low minority-carrier injection levels, the effective lifetime is dominated by trapping effects. These have been discussed in (11,7), where a classic 1956 model from Hornbeck and Haynes was applied to modern multicrystalline wafer data. This lifetime at low apparent carrier density is actually the lifetime of the trapped minority carriers rather than free minority carriers in the conduction band. As such, it can be considered to be a parasitic nuisance, or, to an opportunist, an additional characterization tool(11,14).

The next region of interest is characteristic of the low-injection minority-carrier lifetime and surface recombination in the material. The third region of interest is generally on the low-doped side of the doping level. This is where the Shockley-Read-Hall theory predicts that the lifetime will increase for mid-gap states as the minority carrier density approaches the dopant density.

The forth region of interest is the high-level injection region. Here, the emitter recombination can be separated from the bulk recombination using the method of Kane and Swanson(13), as generalized and applied to doped material by Cuevas(5). Finally, at very high injection levels greater than 10^{16} cm^{-3}, the fundamental Auger lifetime will be approached for all materials.

The raw data from the low range shown in Fig. 1 is plotted in Fig. 2 to illustrate some points about the trapping artifact. The photoconductance is plotted against the incident light intensity. From Equation (1), the lifetime will be

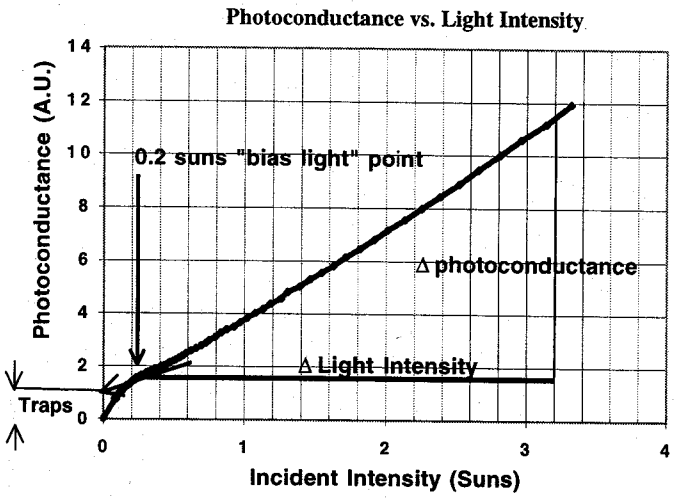

Figure 2. The measured photoconductance for a multicrystalline wafer with trapping behavior at low light intensity.

determined from the absolute photoconductance divided by the incident light intensity.

Note, however that at very low light levels, there is a very large photoconductance that results from little light. This corresponds to the trapping, where minority carriers are trapped with a long lifetime, giving rise to a majority-carrier photoconductance that results from the necessity to maintain quasi-neutrality(1,7,11). This is not a measure of the minority carrier lifetime, and shows up as an artifact in a transient photoconductance or steady-state photoconductance measurement. This can be dealt with by fitting a trapping model to this data as demonstrated by MacDonald et al.(11). Alternatively, with steady-state data as shown in Fig. 2, a graphical method can be used to minimize the effect of the trapping on the calculated lifetime.

By defining a "bias light" intensity, shown in Fig. 2 as 0.2 suns, equation (1) can be applied using the *change* in photoconductance relative to the photoconductance at the bias light intensity and the *change* in light intensity rather than the absolute values. By choosing a bias light intensity corresponding to the point where the traps are just filled, the resulting data corresponds closely to the minority-carrier photoconductance lifetime. The tangent to the curve at the bias point can be extrapolated to find a y-intercept. This can be interpreted as the photoconductance due to traps. It could be considered as the true origin for the minority-carrier photoconductance. In cases where the minority-carrier lifetime has an injection level dependence that overlaps with the trapping region, this procedure is ambiguous. This ambiguity would also apply to the more complete model(11).

The resulting lifetime curve is shown in Fig. 3, and compared to the curve calculated using Eq. (1) without a

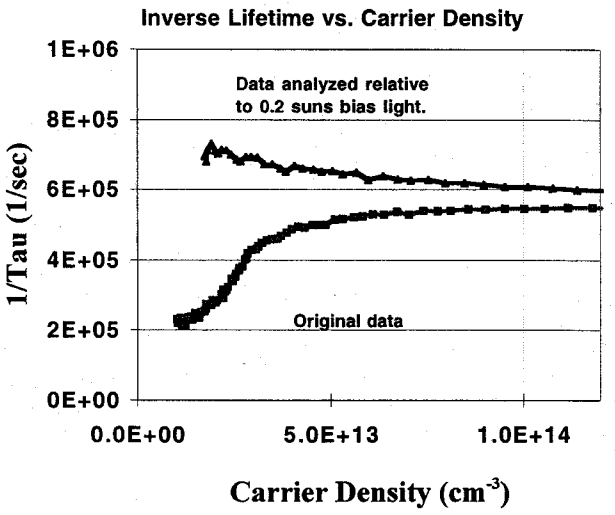

Figure 3. A comparison of the lifetime analysis reference to the origin in Figure 2 (lower curve), or referenced to the bias light point in Figure 2.

"bias light". The "corrected" data extends to low minority-carrier densities, in the range relevant to solar cell operation. Note that a full understanding of the lifetime requires data from a range of injection levels. Historically, steady-state data has not been extensively used due to the artifacts introduced by the trapping behavior(1). By taking data over a range of incident light intensities, this deficiency can be overcome.

Although not proven here, I found that this correction for the trapping is simple and improves the correlation between the measured lifetime and the final solar cell parameters. This method will be referred to in this paper.

II. LIFETIME PRIOR TO PROCESSING.

It would be ideal to have a perfect measure of the wafer quality at the beginning of processing. In practice though, measurements early in the process generally correlate very loosely, if at all, to the final solar cell properties if the material is significantly changed during the high-temperature process steps. However, it is important to control the evolution of the material properties throughout the process. Also, if material is to be outright rejected, it is most valuable to have this information before any expensive processing is performed on the wafers. In some cases, it would be useful to have this information as a form of vendor qualification. The difficulties include:

1) Wafers are unpassivated at the beginning of processing, limiting the lifetime to the "filament lifetime" for unpassivated wafers, typically 2μs for a 300-μm-thick wafer.

2) Prior to processing, wafers typically have strong trapping behavior, either due to the surface condition, or the wafer quality prior to phosphorus diffusion.

For some wafers, a screening that rejects wafers with effective lifetime less than 2 μs may be useful. Although not as sensitive to the bulk lifetime as desired, this has proven to be useful in some cases. To maximize the sensitivity to the bulk minority carrier lifetime, the use of an IR light source minimizes the surface effects. The bias light analysis minimizes the uncertainties introduced by trapping behavior. Finally, the lifetime should be determined at a fixed minority-carrier density, chosen to be as relevant as possible to the solar cell operation. Often this might be the lifetime corresponding to the solar-cell open-circuit voltage if lower carrier densities are much influenced by traps.

An alternative is to push a sampling of incoming wafers through a high temperature step and then test the material quality in order to qualify the batch. This can be the normal emitter diffusion process, or a special surface passivation treatment that is optimized to minimize surface recombination. This was the approach taken by MacDonald et al., in a study of the potential for gettering different regions of a cast ingot. This approach is well-controlled and has been used in a number of studies(6,8,9,11,14,15,17). In the ingot study, a light phosphorus diffusion and oxidation schedule was performed on wafers either as-grown/etched or as-grown/etched/gettered. Some results of this study are shown in Fig. 4. It can be seen that gettering was effective

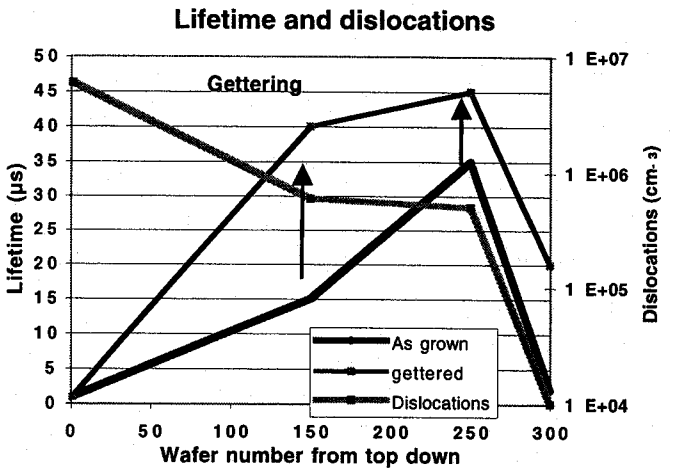

Figure 4. The lifetime before and after gettering for wafers from different regions of a cast ingot.

for wafers from the bottom, center, and near-top regions, but failed for wafers at the top of the ingot. The region that gettering did not improve were shown to have high dislocation densities as well as high volatile metallic contaminant densities(14). The trap density for gettered wafers, extracted from a trapping model, was found to correlate very well with dislocation density for all of the wafers.

Another case where the data may be significant when measuring unpassivated starting material is for wafers with relatively-low as-grown lifetime. Fig. 5 shows lifetime data

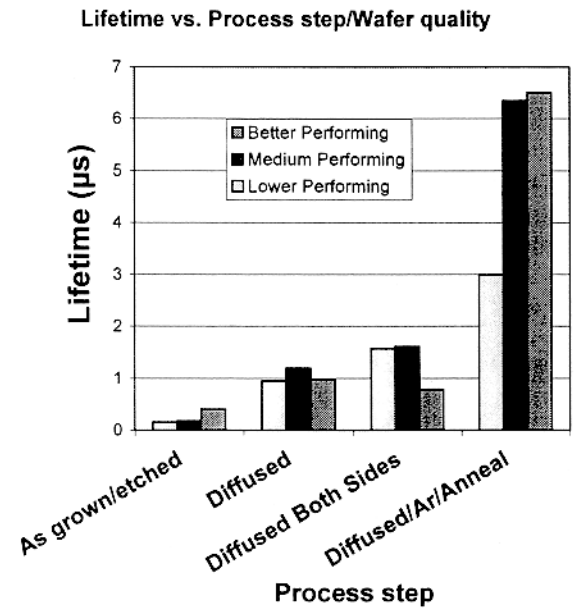

Figure 5. The effective lifetime of different performing wafers at various stages in a process sequence.

for a ribbon material, at various stages in the process including just after a cleaning etch. Several grades of wafers were used, ranked for known potential to achieve efficiency. The lifetime for these as-grown/etched wafers varied from 0.1µs for wafers rated "lower-performing" up to 0.3µs for wafers rated "better-performing". These lifetimes are reasonably true representations of the bulk lifetime for these materials, since the measured lifetimes are much lower than the filament lifetimes that would be due to high surface recombination alone if the bulk lifetime were high. The measurement conditions in this case used a quasi-steady-state measurement instrument(16), with a Xenon flash filtered to pass wavelengths greater than 700 nm. The lifetime here, as well as in subsequent stages as shown in Fig. 5, was evaluated at 5×10^{13} cm^{-3} minority carriers using a 10-sun light bias. Each point represents an average of 18 points, 6 on each of 3 nominally identical wafers.

III. Effective Lifetime After Emitter Diffusion

After the emitter diffusion is an ideal point to measure lifetime. The front phosphorus diffusion and oxidation acts as a surface passivation. This increases the filament lifetime, now limited by the high rear-surface recombination, towards 10µs in typical cases. In many cases, the backside receives some passivation due to the high-temperature step, allowing even higher lifetimes to be discriminated. In the case of the ASE wafers, all grades of wafer were improved into the range of 1 µs effective lifetime by this phosphorus diffusion as shown in Figure 5.

An alternative interpretation of steady-state photoconductance data results in an implied I-V curve rather than lifetime vs. carrier density(2,3). This presentation in shown in Fig. 6 for a multicrystalline wafer after the phosphorus diffusion, then again after the Al BSF formation. The voltage corresponding to open-circuit voltage is shown to drop at the Al diffusion, indicating that this process step determines the cell voltage. Notice that this presentation clearly indicates the ideality factor for the solar cell I-V curve.

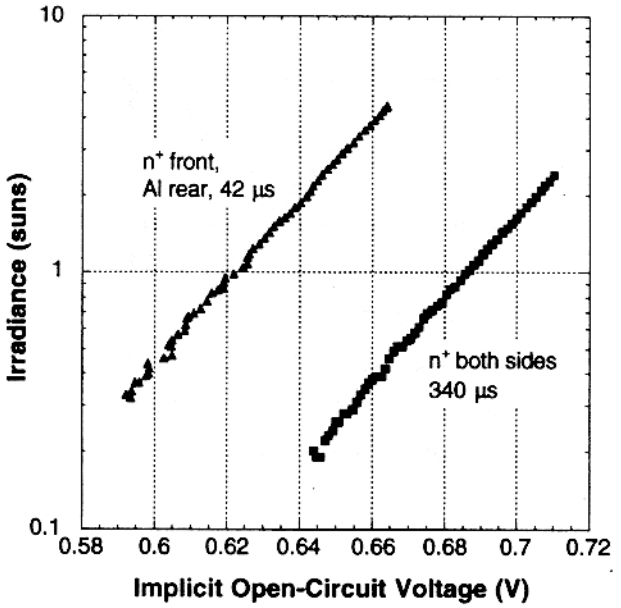

Figure 6. The steady-state photoconductance data interpreted as an I-V curve. The solar cell had a potential for a 680 mV open-circuit voltage after emitter diffusion, but this was reduced to 620 mV by the backside Al.

At any point after the emitter diffusion, the emitter saturation current density can be obtained separately from the bulk recombination using the method by Kane and Swanson(13). If the wafer is in very high-level injection, with free electrons and holes far exceeding the doping density, then there is a clear separation of the bulk and emitter effects on the lifetime as a function of the injection level. In practice, solar grade wafers often have a relatively low lifetime and extreme bulk injection-level dependencies near the doping level. These tendencies in solar cell substrates increase the uncertainties in the separation of

bulk and emitter recombination. In general, I would recommend that lowly-doped, high-lifetime test wafers should be run in parallel with the solar-cell wafers if a precise extraction of the emitter saturation current density and the bulk lifetime is desired at this stage in the process.

IV. Effective Lifetime After Surface and Bulk Passivation

In many cases, the ultimate effective lifetime in the wafer is achieved after the phosphorus diffusion. The bulk lifetime measured at that point will be as great or greater than what

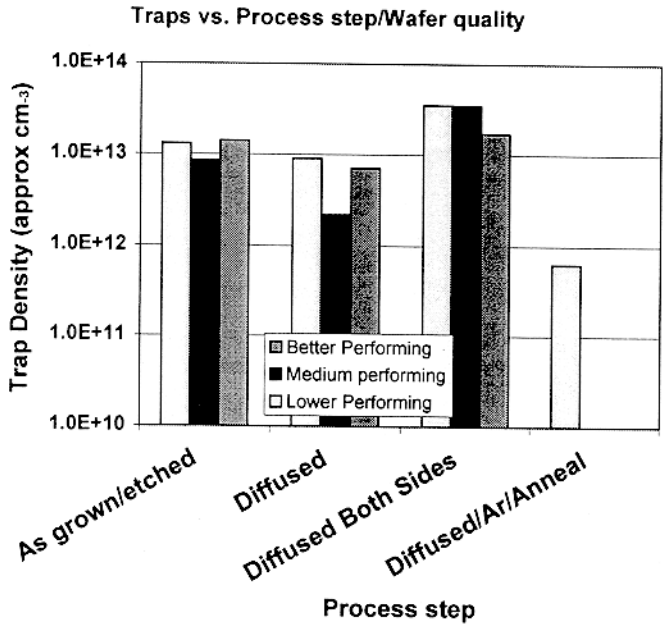

Figure 7. The trap density, extracted as described in Section II. The bulk and surface passivation step eliminates the trapping effects on good wafers.

will be determined at the end of the process using I-V curves or spectral response. However, In cases where surface and bulk passivation are applied after the phosphorus diffusion, further gains in effective lifetime are possible. This passivation effect is seen in the ASE wafers in Fig. 6. After surface and bulk passivation, the lifetime of the better two grades of material is improved to over 6 μs, where the "lower performing" material improved to 3 μs. Interestingly, the trap density, determined as described in Section I, is virtually eliminated in the better quality wafers by the surface and bulk passivation step, as seen in Fig. 7.

V. Contactless "External Quantum Efficiency" Measurement.

The steady-state photoconductance measurements can offer an early evaluation of the surface passivation quality of the emitter at any stage after the phosphorus diffusion. The measured lifetime by the steady-state method is the ratio of the photogenerated carriers in the bulk to the incident light intensity. If the emitter quantum efficiency is low, the photogenerated carriers reaching the bulk will be reduced, giving a lower effective lifetime. Fig. 8 shows a simulated external quantum efficiency curve from PC-1D(18) for a standard solar cell with and without surface passivation.

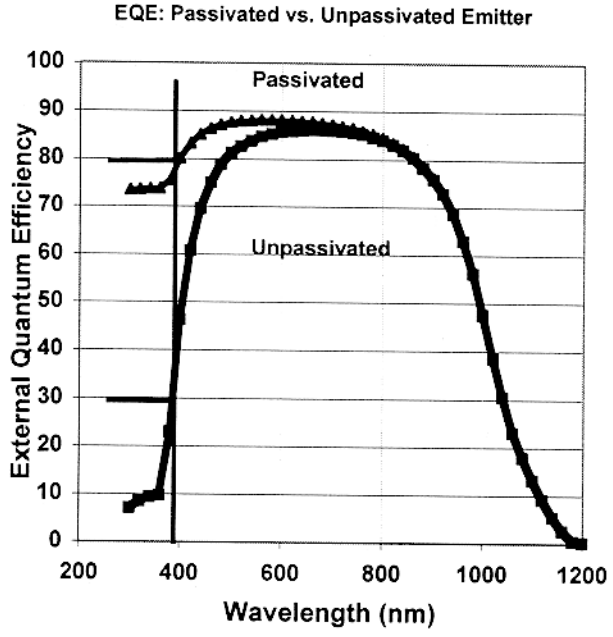

Figure 8. A steady-state photoconductance measurement done with 390 nm light, for example, would give high-sensitivity to measuring emitter surface passivation.

It can be seen that the EQE ratio for the passivated/unpassivated case is 2.5 at a wavelength of light of 390 nm. If this wavelength of light were used for a steady-state photoconductance lifetime measurement, the measured lifetime would be 2.5 times larger for the passivated-emitter case. This is a very simple and sensitive contactless measurement of the spectral response of the emitter. The effect of changes in the bulk lifetime could be evaluated using light with wavelengths longer than 500 nm.

If a passivation process changes the measured lifetime using blue light, but not red light, then surface passivation has occurred and can be evaluated. If the lifetime changed significantly for red or white light as well, then bulk or back surface passivation has also occurred.

VI. Voltage Measurements at Intermediate Process Steps

The most common diagnostic tool for evaluating a solar cell process is the final illuminated I-V curve. An extremely useful variation of the standard I-V curve is the illumination-V_{oc} curve. This second curve can give data

closely indicating what the solar-cell IV curve would look like in the absence of series resistance.

The illumination-V_{oc} curve only requires that the contact to the p^+ and n^+ regions of the cell be much better than the input impedence of the measurement tool. This very simple requirement means that in many cases, the illumination-V_{oc} curve can be taken at any point in the process after the emitter diffusion by simply probing the appropriate areas of the silicon.

Some care must be taken that the probed contacts are ohmic. However, if it is possible to do a probed sheet resistance measurement of the p+ and n+ regions, then it is almost certainly possible to do an illumination-V_{oc} curve as well.

Figure 9 shows a modeled comparison of the illumination-V_{oc} curve with a final V_{oc} curve for a standard solar cell. To construct the illumination-V_{oc} curve in the standard format, the short-circuit current must be assumed, and the superposition principle applied(10). At each voltage, the current is taken to be:

2) $J = J_{sc}(1\text{-suns})$

This illumination-V_{oc} curve has all of the information on ideality factors, as well as a sensitive measure of the shunt resistance. The difference between the two curves can generally be attributed entirely to the series resistance, without ambiguity.

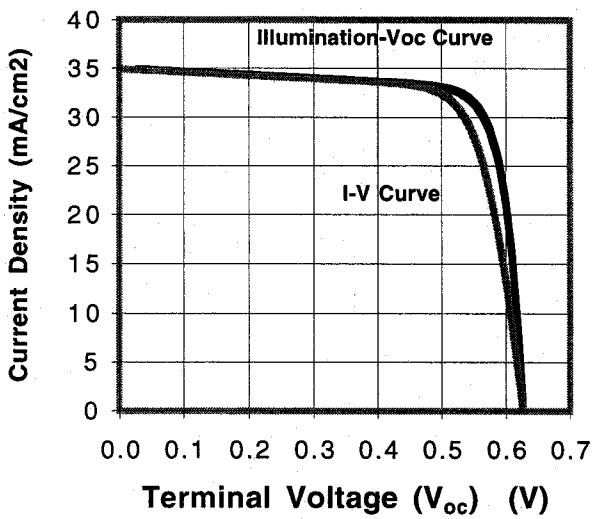

Figure 9. The standard I-V curve compared to an illumination-V_{oc} curve. The difference between these curves is an excellent measure of the lumped series resistance of the solar cell.

Since this measurement can be done at any point after phosphorus diffusion, the detailed effect of each metalization and sintering step can be examined in isolation from the other steps. Changes in shunt, voltage, fill factor and ideality factors at each point on the IV curve (without series resistance) can be tracked through the individual steps. Fig. 10 is an example of data taken in this way on a finished multicrystalline solar cell.

Despite the lack of external current collection, the illumination-V_{oc} curve proves to be a sensitive indicator of contact problems as well. Fig. 11 shows a solar cell with a common contact problem for terrestrial solar cell technologies. One of the contacts is not completely formed. At high illuminations, this poorly formed contact produces a voltage that opposes the p-n junction voltage. In Fig. 11, the illumination-V_{oc} curve looks normal in the region up to one sun, with an ideality factor of nearly 1. However, at the moderate intensity of 15 suns, the voltage peaks and at high intensity the effects of the poor contact are clearly evident by the voltage loss. By 100 suns, the ideality factor is –4 and the voltage is rapidly *dropping* with increasing illumination intensity!! Often, this effect of ideality factors less than unity at high intensities can be seen *before* the problem manifests itself in observed efficiency loss. As such, it is an ideal warning of a drifting process problem affecting the contact uniformity and resistance.

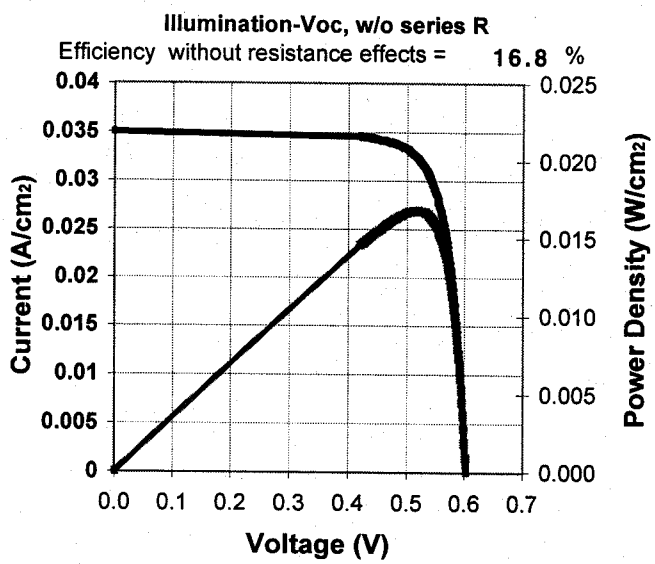

Figure 10. An example of illumination-V_{oc} data taken for a completed multicrystalline solar cell. The curve was plotted in the standard I-V curve format using eq. 2.

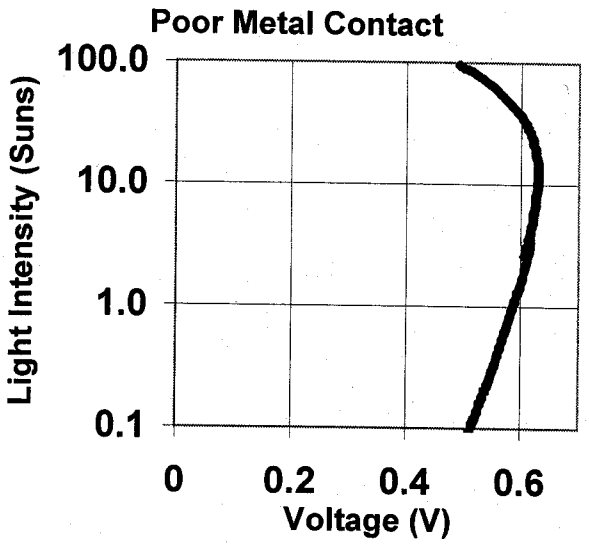

Figure 11. An example of a contact problem as indicated by the high-intensity illumination-V_{oc} data.

VII. CONCLUSIONS

Recent research results using measurements of the electronic properties of the wafers during intermediate process have opened new possibilities for in-line process diagnostics for industrial solar cells.

The effects of many of the individual process steps on the potential wafer voltages, external quantum efficiencies, and contact properties can be observed as they evolve step-by-step through the process with the use of minority-carrier lifetime measurements and probed voltage measurements. Critical information is available if data is taken over a range of minority-carrier densities or voltages.

By isolating steps in the middle of the process, the results are more direct, more fundamental, and less confused by any additional variables introduced in subsequent steps. The electronic properties of the wafer can be optimized using quick-loop experiments in the center of the process independently from contact, series-resistance, and shunting that might be introduced in the back-end processing. These techniques are ideal for qualifying materials and processes or immediately identifying changes in standard materials and processes.

These advances may contribute to future improvements for industrial process optimization and factory process control.

ACKNOWLEDGMENTS

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Process Monitoring in Solar Cell Manufacturing

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Introduction

The photovoltaic (PV) industry has grown very rapidly in the last few years. It is expected that the PV industry can now benefit as a whole from collective research, standardization, and process control. An example of the success of this cooperative methodology is the Si-based microelectronics industry in which standardization and process control have proven to be valuable for improving reliability and throughput in manufacturing. Hence, as the annual production increases further, the introduction of process control and monitoring in PV manufacture is imminent. The PV industry is already using some degree of process monitoring, but a full-fledged process control has to await development of suitable measurement techniques.

In this paper, we describe a new method that is capable of in-line monitoring of several solar cell process steps such as texturing, AR coatings, and metal contact properties. The measurement technique is rapid and specifically designed for solar cells and wafers. The system implementing this new concept is named "PV Reflectometer." The idea was originally conceived several years ago and the principle of the method has been demonstrated for some simple cases in (1,2). Recently, this method has been improved to be more suitable for commercial applications. For completeness, the paper first includes a brief review of the process control requirements and the common monitoring methods in solar cell production.

Requirements of solar cell process monitoring

Solar cell fabrication involves many process steps (see Table 1, columns 1 &2). Specifically, monitoring is needed for:

1. Ingot or incoming wafer quality – the parameters to be measured are the resistivity, minority-carrier lifetime (τ) or diffusion length (L), defect density, impurity concentrations, surface roughness, and cleanliness/contamination
2. Texture quality
3. Junction depth (sheet rho)
4. AR coating thickness(es) and refractive indices
5. Metallization parameters (area, thickness, width, back-contact properties)
6. Cell parameters.

It is clear that the processes to be monitored are similar to those used in the microelectronics industry and that many of the process steps can be monitored using non-contact optical methods. Whereas the microelectronics industry is well equipped with a great deal of instrumentation,

unfortunately these methods are not well suited for solar cell production. Concomitantly, there is now an intense search for proper techniques for monitoring purposes in the PV industry. It is in general desirable to have noncontact optical techniques.

Difficulties in using conventional techniques for PV monitoring

Column 3 of Table 1 shows a number of techniques, originally developed for the semiconductor industry, which are now used for solar-cell process monitoring. These measurement methods are not well suited for solar cell industry because:

1. Solar cells (and substrates) have rough or textured surfaces/interfaces
2. Equipment is expensive
3. Measurements are slow for high throughput facilities, and
4. Measurements are made on small areas. In solar cell monitoring, it is important that the properties of the entire wafer be measured. This is because typical processing introduces strong nonuniformities and, in many cases, local measurements can yield meaningless values as far as process monitoring is considered.

Table 1. A list of the major process steps, parameters that are monitored, and the monitoring techniques used in solar cell fabrication. Also indicated (by X) are the steps that can be monitored using a reflectometer.

Process or monitor step	Parameter(s)	Technique	Possibility of using Reflectometer
Crystal growth (Ingot Quality)	τ	PCD	
Wire Sawing Quality/wafer cleanliness	Surface Roughness/residue		X
Texturing	Texture Height	SEM/Optical microscopy/Reflectance	X
Electronic Quality of wafers	L/τ	SPV/PCD	
Junction Depth	Sheet Resistance	4 Point Probe, groove and stain	
Defect Density	Dislocation Density	Chemical Delineation / TEM	
Impurity Concentration		FTIR, NAA, SPV, DLTS	
AR-Coating	Thickness, Refraction Index	Ellipsometer/Interference	X
Metallization	Line Width	Optical/SEM	X
I-V of Cell	V_{oc}, J_{sc}, FF	Standard I-V measurement	

It is a common experience in commercial solar cell fabrication that measurements on solar cell wafers yield unreliable values. Hence, in most cases, the solar cell industry uses additional "control wafers" in each process step that are polished on one side. However, the use of such "dummy" wafers has many disadvantages, and limits the degree of process control that can be implemented on a production line.

Basic principles and the measurement approach

The 4th column of Table 1 shows various process steps which can be monitored by means of a reflectometer. However, because conventional reflectometers are small-beam instruments, they cannot measure a large-area wafer. One way to overcome this limitation is to scan the wafer. This approach is used in PVSCAN (3,4). Although, such an instrument can yield a great deal of information, the scanning methods are inherently slow.

We have developed a new noncontact technique (PV Reflectometer) for monitoring a number of processes in a solar cell production facility. It can measure the surface roughness, surface cleanliness or contamination, texturing, AR coating properties, and metallization parameters. To overcome the difficulties intrinsic to the conventional methods, the new measurement concept is based on the reciprocity principle in optics. Figure 1 illustrates the reciprocity principle in that the two cases shown are optically equivalent. Figure 1(a) shows the incident light is normal to the sample and the reflected (scattered) light is collected through all the angles, and Figure 1(b) shows the light incident from all the angles and collected normal to the sample. The approach of Figure 1b confers many advantages, including ease of large-area illumination and simplification of the signal collection—features that can greatly enhance the S/N ratio to render a measurement fast. The next section will show how those are made practical.

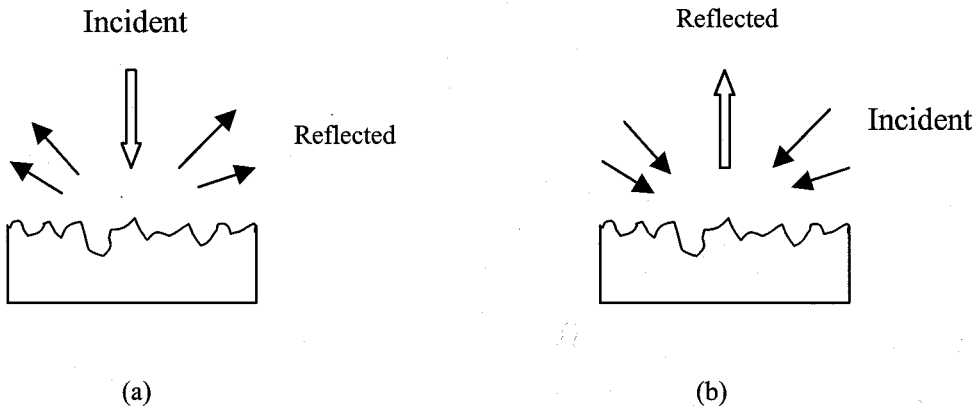

Figure 1. Illustration of the conventional illumination approach (a) and the reciprocal approach (b).

The PV Reflectometer employs the reciprocity principle similar to that in Figure 1b to illuminate the entire wafer. It measures the total reflectance of the sample as a function of wavelength, and uses different segments of the curve to extract information about the front-surface and back-surface properties. This methodology is illustrated in Figure 2. This figure shows a typical reflectance plot of a textured, mc-Si solar cell with an AR coating and front and back metallizations. Here, λ_0, R_0, R_b and $\Delta\lambda$ are used for determining the AR coating thickness, metallization fraction, backside metallization quality, and texture parameters, respectively.

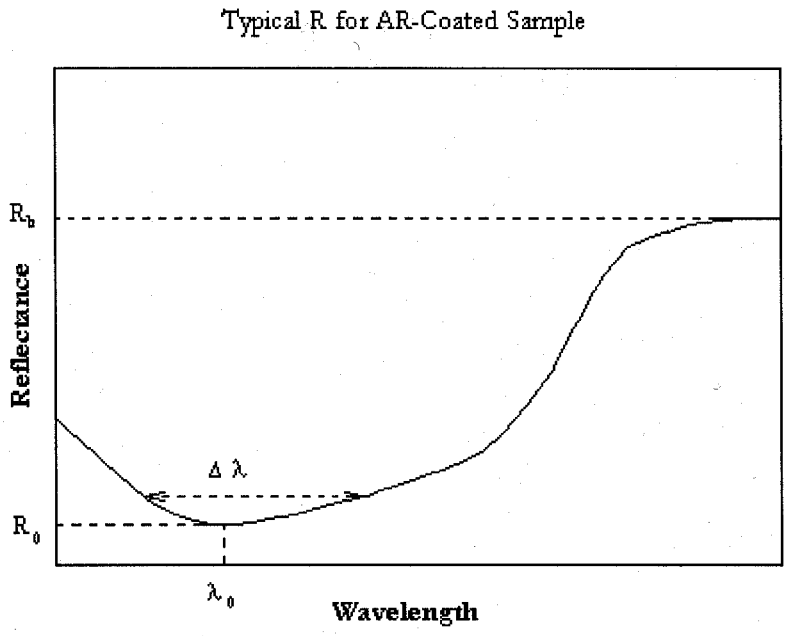

Figure 2. Illustration of the various parameters of a reflectance plot used for process monitoring

Description of the equipment

The reflectometer (see Figure 3) consists of a highly absorbing spherical dome, about 12—18 inches in diameter, with openings at the top and at the bottom. The bottom side has a square flange, within which the test sample is placed. The sample is placed on a platform in a way that the signal, consisting of the reflected light seen by the detector, is due only to the sample. The entire system is designed to eliminate all the possible scattering of the light except by the test wafer. The topside of the dome has a lens and aperture assembly that couples the light reflected from the sample into the optical fiber. The other end of the fiber feeds into a low-resolution monochromator, whose output is detected by a Si photo-diode. If the fiber is taken out of the optical path, one can observe a reflected image of the sample. This image can be further used to map the sample, giving more detailed spatial information.

The monochromator drive, data taking/handling, calibration, and the system control are done by a computer. The system operates in a spectral range that allows reflections from the front and the backside of the cell to be monitored.

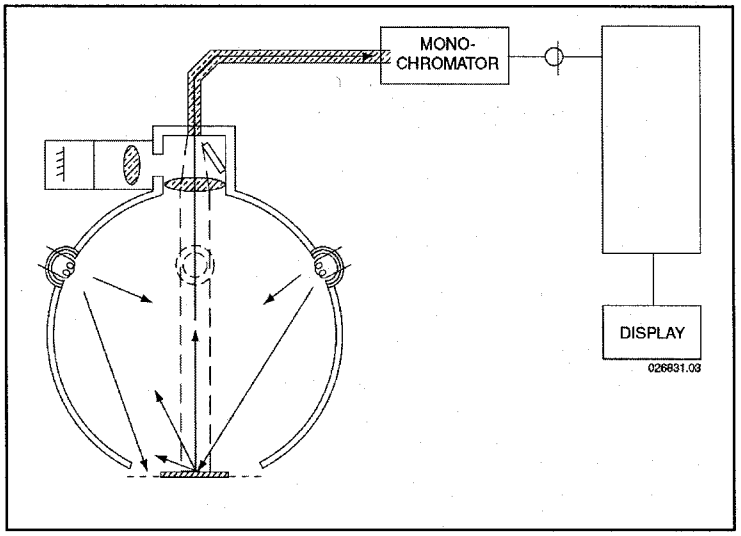

Figure . A schematic of the PV Reflectometer

Using the reflectometer

The reflectometer can be used for all the process monitoring steps shown in table 1. These are briefly described below.

a. Monitoring the sawn wafer and texture quality by surface reflectance
The solar industry usually uses wafers with textured or rough surfaces to reduce overall reflectance of the solar cells, and trap light to enhance its absorbance. Typically, the sawn wafers are cleaned and etched at room temperature in a caustic etchant to remove the surface damage. Any residual damage can be very detrimental to the junction quality of the cell and degrade the bulk material quality by generating dislocations during the cell processing.

The next process step may consist of surface preparation involving texture-etching the wafers in a hot sodium- or potassium-based hydroxide solution. This solution is an anisotropic etch that produces surface structures by exposing (111) crystallographic faces. For example, it produces pyramid-shaped surface texture on (100) wafers. The size and the height of the texture depend on many parameters, including concentration of the hydroxide, temperature of the etch bath, pH of the solution, resistivity of the wafer, presence of surface damage (such as from sawing) on the wafer, and on the number of samples etched (because the composition of such a bath changes with the formation of silicates produced by the dissolution of Si).

Because the texturing properties depend on so many parameters, this process is apt to result in significant variations from batch to batch and within the same batch of wafers, if no monitoring is incorporated. These variations in the surface quality lead to variations in the photocurrent (J_{ph}) of the cells. Furthermore, because it is a common practice in the industry to combine texture

etching with the saw-damage removal step (as a cost-reduction strategy), texture etching is a crucial step in cell production. An incomplete removal of damage can have a tremendous effect of degrading the fill factor (FF) and the open-circuit voltage (V_{oc}) of the cells. Therefore, it is important to measure the surface quality of the wafers before they enter a cell production. Currently, the PV industry does not have a suitable method for monitoring texture quality.

The reflectance of the wafer can be used to monitor the quality of both the sawn and the textured wafers.

b. Measuring AR coating thickness

A minimum or null of the reflectance is used to determine the thickness of the AR coating. However, an AR-coated wafer with rough/textured surface exhibits a broadened minimum. This may require a high S/N ratio to magnify and search for the true minimum. Our reciprocity illumination will result a high detection sensitivity to avoid the problem. PV Optics is used to relate the reflectance and the AR coating parameters.

c. Front surface reflectance/metallization fraction

An AR-coated solar cell, with front metallization, will display a reflectance minimum whose amplitude is related to the fraction of the cell area covered by the metal. It is possible to attain many parameters of the front metallization using illumination with different angular distributions.

d. Back-side reflectance

The reflectance of a solar cell in the long wavelength region can be related to the quality of the back contact. For instance, a good quality Si-Al contact should have very high reflectance. A properly alloyed Al can be controlled to have a reasonably sharp interface and a high reflectance. However, formation of a back-surface field lowers the back reflectance by providing a refractive index gradient at the interface. *PV Optics* allows us to perform calculations to relate the reflectance to the alloy quality of the back contact.

Preliminary Results

Figure 5 shows some results produced on a laboratory system in arbitrary unit using samples from a PV company. The samples are taken at various stages of the cell fabrication—after pre-etch cleaning, after texture etching, and after AR coating. The data include:

1. Reflectance of a commercial 4.5-in. x 4.5-in., mc-Si wafer after sawing and cleaning
2. Reflectance of a commercial 4.5-in. x 4.5-in., mc-Si wafer after texture-etching
3. Reflectance of a commercial 4.5-in. x 4.5-in., mc-Si wafer after the TiO_2 deposition. The measured thickness of TiO_2 ranges from 794–858 Å.

The results show that sawing and wafer cleaning have a tight control, while texturing has a significant variation from wafer to wafer. The AR coating mitigates some of the variation. The average thickness of the coating ranges from 794–858 Å. The current system can accommodate samples as large as 6 in. x 6 in. A typical run of the laboratory system now takes about 15 seconds per sample for the entire measurement.

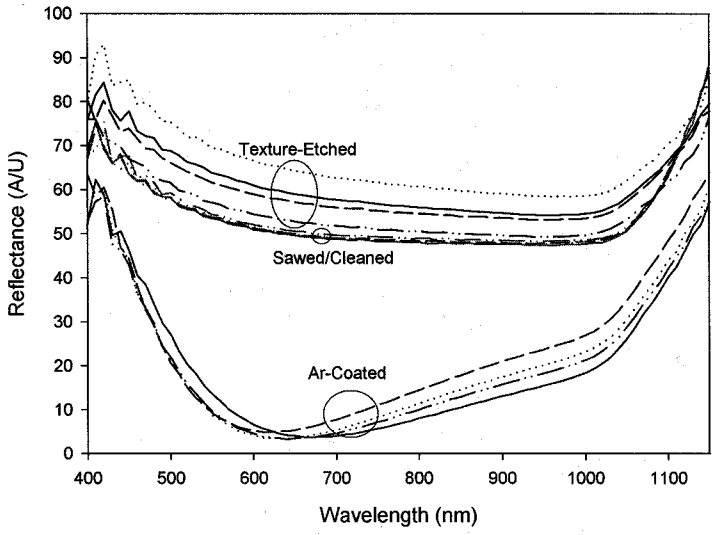

Figure 4. Reflectometer results on three groups of commercial PV-Si wafers (4.5-in x 4.5-in) at different stages of solar cell fabrication.

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A Review of Japanese R&D for Crystalline Silicon Solar Cells

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ABSTRACT:
Last year, Japanese PV market has grown to 49 MWp, 40 % increase as compared with 1998 which is almost close to US market. However, the module price tends to be saturated and is difficult to decrease furthermore. At least, one-third cost reduction will be required to be independent on the government subsidy. Japanese activities for crystalline Si solar materials and devices had been directed to the promotion of Si feedstocks R&D using Kawasaki process. The quality of the Kawasaki cast crystals has greatly improved by a joint work between Japanese companies. 14%-level efficiency cells have been fabricated using good-quality cast wafers and conventional cell fabrication processes. From FY 1999, a new four-year R&D program for multicrystalline Si solar cells could be restarted fortunately to make up the gap between the market and R&D directions. An ambitious 20 % cell efficiency was targetted in the new program. As for single crystal Si solar cells, there is an international joint research for light degradation of CZ crystals and solar cells. This research, non-government based one, is very successful to elucidate the degradation mechanism and to provide the solutions for light degradation.

1. INTRODUCTION

In recent years, PV market growth has been remarkable and attained to be more than 150MWp in 1998 corresponding to 22% increase as compared to 1997[1]. This rapid growth is due mainly to bulk-type crystalline silicon solar cells particulary by using cast Si materials and also amorphous silicon solar cells. And, it should be pointed out that the current PV market is now supported by government subsidy policy for grid-connected power applications. The market growth in the coming century might be suppressed if production technologies on low-cost silicon feedstocks, high-speed slicing and high-efficiency, low-cost solar cells and modules were not developed.

As for the past R&D programs in Japan, steady progress had been achieved especially in the fundamental research and the development of new process technologies for Si feedstocks and solar devices[2]. Especially, the past 4-year government R&D project from 1992 to 1996 for crystalline Si materials and devices was successful. Primary results were the developments of equipment and technologies to produce gigantic cast ingots and also fast cell fabrication processing technologies for multicrystalline Si solar cells. 17%-efficient, large-area multicrystalline Si solar cells were fabricated with 15%-level efficient, modules fabricated using multicrystalline Si solar cells. In addition, very-high efficiency, single-crystal solar cells with a 22%-level were fabricated. However, these goverment program stopped in 1996 as the government programs shiffted to film-type solar cells and advanced approaches except for Si feedstock. The Si feedstock program has been promoted by a new association, SOGA, established in 1996[3].

The Japanese PV industry has began to feel frustration since there exists a misgap between PV market status and government R&D support. Another issues emerged are the saturation of price reduction and the cost gap between current module price and government cost forecast. Last year, the Japanese PV industry discussed with government people about a restart to support R&D for multicrystalline silicon solar cells. As a result, the industry succeeded to restart a new four-year R&D program from FY 1999 to 2002. This program is only one to exist beyond the next century. Other current programs including thin-film solar cells, super high-efficiency solar cells and systems research will be evaluated until FY 2000.

In this paper, current PV market in Japan is reviewed to find out and reconfirm economical and technical issues for bulk-type silicon solar materials and cells. A new four-year R&D program for multicrystalline silicon solar cells is introduced with the program goals including cell efficiency and cost reduction. In addition, a non-government international joint research to solve light degradation of CZ cells is described. This research is very successful to elucidate the degradation mechanism and also to provide the solutions for light degradation.

2. MARKET EXPANSION

In the last ten years, the market growth has been remarkable as shown in Fig.1 and 2. Especially last year, a world-wide PV market expanded to more than 150 MWp, 22% increase as compared to 1997. The market size is about 5 times larger than that in 1988. As indicated in Fig. 1, the increase depends upon a great expansion of cell production using single and multicrystalline Si wafers. As for film-type a-Si and CdTe solar cells, the cell production had been almost constant, but increased substantially in the a-Si solar cells last year. As a whole, crystalline silicon solar cells using bulk Si materials are still dominated in a current photovoltaic market for both remote and grid-connected power applications.

The rapid growth of cell production occurred both in USA., EU and Japan, as shown in Fig. 2. In 1988, about ten years ago, production shares of USA and Japan were almost the same. However, Japanese share declined from 1991 because of economical depression and lower yen price, whereas

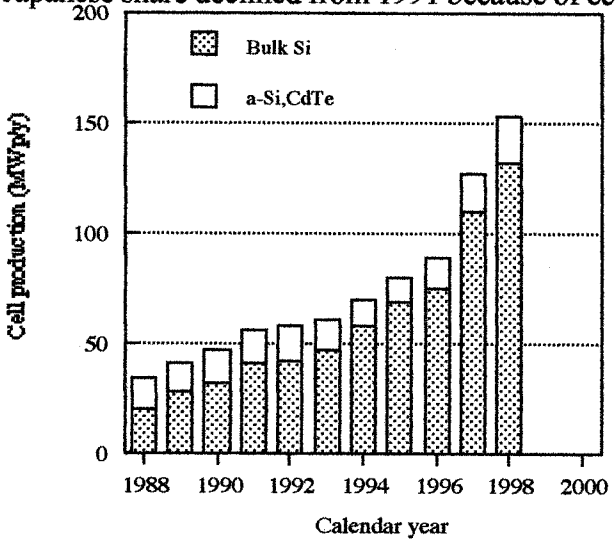

Fig. 1 Yearly cell production of bulk-Si and film-type solar cells.

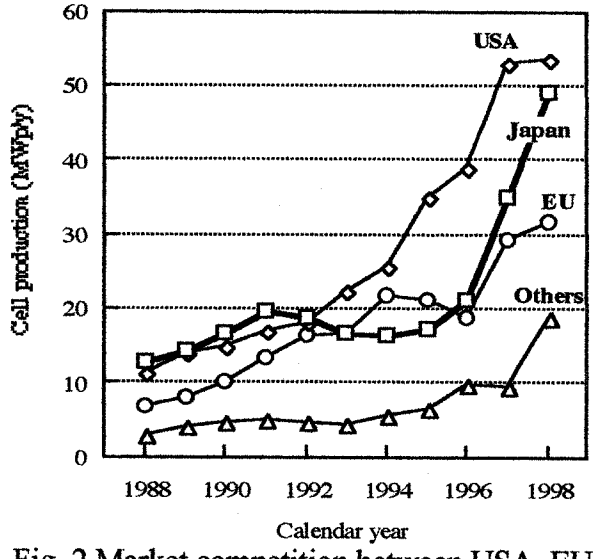

Fig. 2 Market competition between USA, EU, Japan and others in the last ten years.

productions in USA and EU grew steadily. Since 1994, Japanese production tended to recover from the depression and to increase rapidly. Last year, 40% increase was attained as compared with the previous year in Japan. This remarkable increase is mainly due to the initiation of government subsidy program for private PV houses. The number of PV houses in 1997 surpassed 8,000 corresponding to 30 MWp and was expected to be more than 10,000 due to the fixed budget increment in FY 1998.

However, PV system price did not decrease expectedly. The total price of a 3 KWp system in 1994 was 6 million yen (50 k$ using an exchange rate of 120 yen/$) and users had to pay 2 million yen due to the 2 thirds subsidy. In 1998, the total price of the 3 KWp system was about 3 million yens and the users had to pay the same price of 2 million yen due to the one third subsidy. The cost allocation of the modules in the PV systems is about 60%.

As expected, cost reduction of solar modules is a key factor for future cost reduction of the PV systems. Fig. 3 shows yearly reduction of the government module price, so-called NEDO price, and also government cost forecast under an assumed production of 100 MWp/year. As indicated in the figure, the NEDO price is saturated to be about 600 yen (4.3$)/Wp. One of the peculiar point in Fig. 3 is the existence of big cost gap between the current market price and the government cost

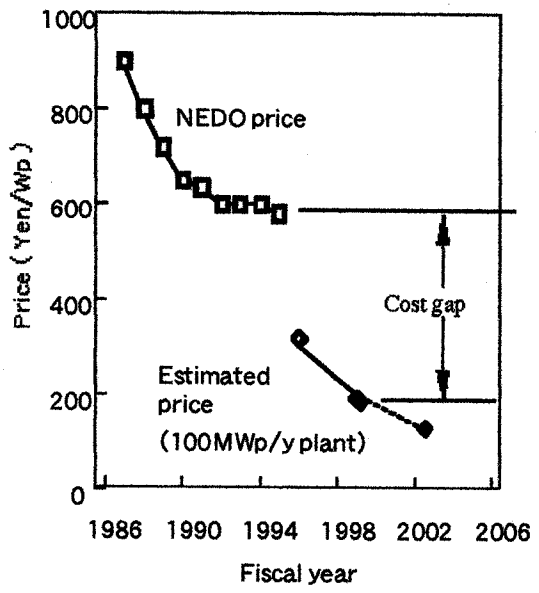

Fig. 3 Yearly reduction of NEDO price and estimated production cost.

forcast of 200 yen/Wp. The cost forcast was calculated by assuming a mass production level of 100 MWp/y for cells and modules and 500 MWp/y for Si materials. The module cost consists of three factors including Si materials, cells and modules. Although a major part is the Si materils, all the factors sould be reduced to at least one third of the current price by constructing an automated, mass production of 100 MWp/y for cells and modules and 500 MWp/y for Si materials. The allocation of cell production was expected to reduce drastically, whereas new ideas are required for the cost reduction of Si materiala and modules

These estimation is considred to be optimistic as the current production of one factory has already attained to be 20 to 30 MWp/y. It will be difficult to reduce the price to one third even if production capacity incresead to about 5 times larger than the current factory level.

3. R&D STATUS AND FUTURE

3.1 Silicon Feedstocks

In the past until 1992, a low-cost process of silicon feedstock by carbothermic reduction of high-purity silica had been investigated. However, the process was not selected for a recent urgent need of Si feedstocks and cast ingots. Instead, refining of metallurgical-grade Si materials has been conducted. In the Kawasaki process in Fig. 4, phosphorus impurity was firstly removed from metallurgical-grade Si feedstocks by evacuation and then boron impurity using plasma oxidation. Boron content could be reduced by mixing water vapor in an argon plasma to a 0.1 ppm level. Metallic impurities were reduced to a ppb level by twice resolidification of the refined MG-Si. Cell efficiencies of around 14% were obtained by a conventional cell fabrication process which is almost the same level in the use of a semiconductor-grade Si feedstock. This year, a pilot-scale setup with a capacity of a few 100 kg will be constructed by the government support. The details will be presented in a different paper at this workshop.

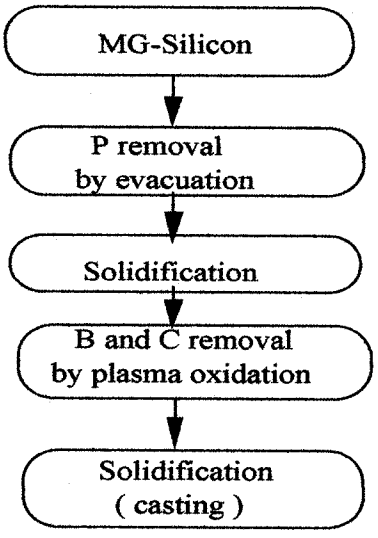

Fig.4 Production flow of Si feedstocks refined from metallurgical-grade silicon source[3].

3.2 A High-Efficiency, Low-Cost Multicrystalline Silicon Solar Cells

As already mentioned, government support for multicrystalline silicon solar cells had finished in FY 1996. However, if we look at the recent market growth, the bulk crystalline silicon solar cells have become prevailed year by year. An another issue emerged is the saturation of price reduction of solar modules and also there is the cost gap between current module price and government cost forecast. The Japanese PV industry has began to feel frustration since there exists a misgap between PV market direction and government R&D support policy. Last year, the Japanese PV industry discussed with government people about a restart to support R&D for multicrystalline silicon solar cells. As a result, the industry succeeded to restart a new four-year R&D program ranging from FY 1999 to 2002. This new R&D program is now organized by New Energy Development Organization (NEDO) and SOG-Si Technology Research Association (SOGA).

In the new R&D program, there are several R&D items and targets to be achieved until FY 2002. Primary targets indicated in Table 1 are a very high cell efficiency of 20% and lower production cost of 147 yen/Wp using a very thin substrate of 150 μm.

Table 1 Outline and targets of a new four year R&D program for multicrystalline silicon solar cells

Item	Target
R& D period	FY1999 to FY 2002
Substrate size	15 cm X 15 cm
Substrate thickness	150 μm
Curf loss	150 μm
Cell efficiency	20%
Production cost	147 yen/Wp (100MWp/y)

Those two targets are very ambitious to meet with the current electricity cost of the conventional utility line and also to compete with film-type approches.To attain the targets indicated in Table 1, the following R&D subjects are expected to be promoted,

(1) Technology development of very-high quality cast ingot production to realize the cell efficiency of 20%. The development will be carried out by investigating the relation between crystal quality and cell efficiency in more detail.

(2) Technology development of an advanced wire-saw slicing for very-thin substrates. This will be performed by developing a thinner durable wire and fast slicing technology.

(3) Development of high-efficiency cell fabrication technology to achieve 20% using the thin substrates. The high efficiency will be realized by fabricating sophisticated structures including light-trapping, passivation of crystal defects in the bulk and surfaces, high-quality pn and BSF junctions, low-resistivity electrodes, etc.

3.3 High-Efficiency, Single Crystalline Si Solar Cells

The bulk-type c-Si solar cells are considered to continue to play a major role in near and mid-term PV markets because of the reliable, abundant and non-pollution materials and processes. Future cost reduction is expected to realize highly efficient (20%) c-Si solar cells with a thinner substrate (<200 μm) structure. As for single crystalline substrates, CZ wafers have been utilized due to the low-cost and high-quality. However, low-resistivity CZ-Si wafers with a possibly highest efficiency have an issue of light degradation of cell performance[4]. To understand the light degradation in more detail and overcome the issue, an international joint research has started on a non-government, private basis.

Several kinds of Si wafers were supplied by Shin-Etsu Handotai Co. (SEH) to major international institutions including Sharp Corp., Hitachi, Ltd., Fraunhofer Institute of Solar Energy Systems, University of New South Wales, Georgia Institute of Technology and Tokyo A&T University. The SEH wafers consisted of conventional CZ, MCZ(magnetic-field applied CZ) and FZ with boron or gallium impurity with various oxygen concentrations. Some typical data are shown in Fig. 5, 6 and 7 for solar cells fabricated using CZ and MCZ with various B and O contents and Ga-doped CZ wafers. The solar cells were irradiated under AM 1.5 simulated sunlight until 2 hours.

(1) The effects of Boron and Oxygen contents on light degradation

As shown in Fig.5, it is clear that conversion efficiency decreased with irradiation time for a lower resistivity cell. However, the light degradation disappeared for a higher resistivity cell. As for the effect of oxygen content, the light degradation was suppressed by reducing the oxygen content to 1.5 ppma level as shown in Fig.6. The low oxygen content was realized in a quasi-static growth condition of magnetic-applied CZ pullling(MCZ).

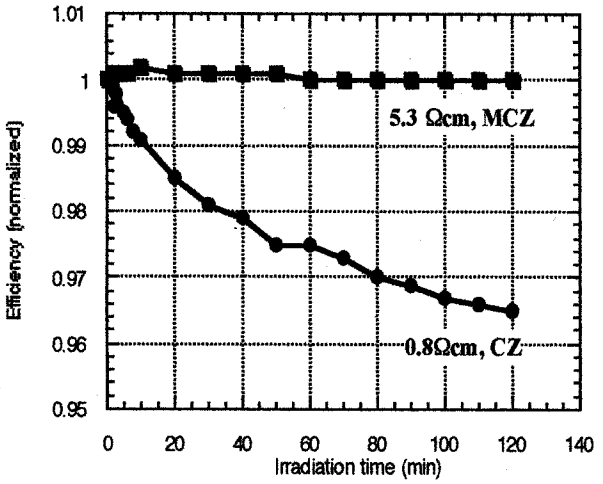

Fig.5 The effect of Boron content on cell efficiency under AM 1.5 irradiation.

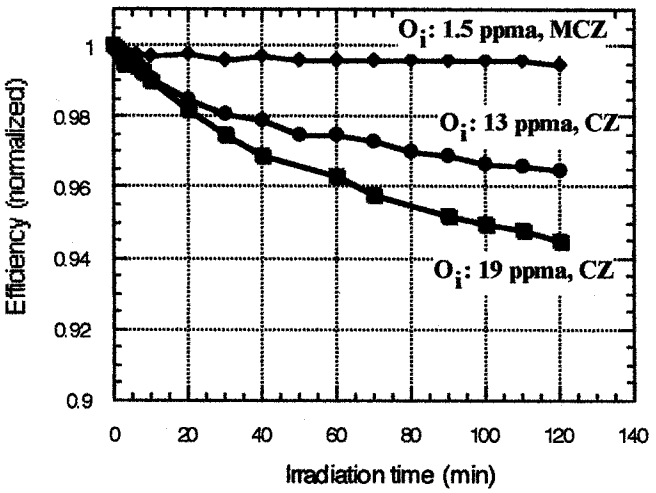

Fig.6 The effect of Oxygen content on cell efficiency under AM 1.5 irradiation.

(2) The effect of impurity species on light degradation

A different dopant, i.e. Gallium, was very effective to suppress the light degradation for CZ cells with a high oxygen content. Fig. 7 is one of the examples in the use of the Ga-doped, 1.6 Ωcm wafers with a high oxygen content of 19 ppma. No light degradation was appeared for the Ga-doped cells.

These results suggest that B-O pairs play an important role in the light degradation of minority-carriers in the CZ cells.

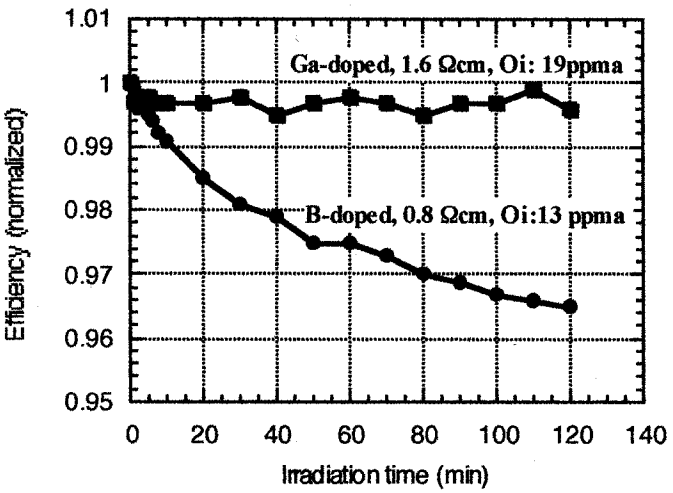

Fig.7 The effect of impurity species on cell efficiency under AM 1.5 irradiation.

Primary achieved results during the joint work are described below.

(1).Light degradation occurs for low-resistivity B-doped CZ wafers with a high oxygen content suggesting the existence of a boron-oxygen complex for the light degradation.

(2).No light degradation is found for Si solar cells using MCZ and FZ single wafers including interstitial oxygen content less than a few ppma.

(3).Ga-doped CZ cells show no light degradation even if the wafers contain high oxygen content.

(4).Highly efficient solar cells with cell efficiencies as high as 20% are fabricated using the low resistivity MCZ and Ga-doped CZ wafers.

From these results, it is concluded that MCZ and Ga-doped CZ wafers are the promising materials for future advancement toward highly efficient and low-cost solar cells.

4. CONCLUSION

A new four-year R&D program for multicrystalline Si solar cells was implemented to make up the gap between the market and R&D directions. An ambitious 20 % cell efficiency using high-quality, 150μm-thick cast substrates was targetted in the new program. The targets of the new program were ascribed to the discussion on *"R&D Issues for Crystalline Silicon to support GW/ year Goal by the Year 2010"* at the 7th NREL Workshop in 1997. As for single crystal Si solar cells, there is an international joint research for light degradation of CZ crystals and solar cells. This research, non-government based one, is very successful to elucidate the degradation mechanism and to provide the solutions for light degradation.

ACKNOWLEDGMENTS

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A Summary of the DIXI Program

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Silicon Wafer Engineering & Defect Science—**SiWEDS**—
An NSF Industry/University Cooperative Research Center

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Abstract

This talk will give an overview of the history, membership, present status, future plans, and sampling of current project activity of SiWEDS, which is a multi-university, multi-company "virtual" research center devoted to **Si**licon **W**afer **E**ngineering & **D**efect **S**cience. The Center mission is to create a unique cooperative culture which will address critical silicon science and technology issues; particularly those which will enable the international silicon materials industry meet the future requirements for advanced integrated circuit manufacturing. The education of graduate and post-graduate students in silicon materials engineering and defect science is a critical component of the Center's activities. The academic community is represented by the following participants: Arizona State University(Dieter Schroder), University of Arizona(Skip Parks), UC- Berkeley(Eicke Weber), MIT(Kim Kimerling), NC State University(George Rozgonyi-Center Director), U of South Florida(Worth Henley), Stanford(Ron Chiarello); whereas the Industry members are Komatsu Silicon, MEMC, Mitsubishi Silicon America, Nippon Steel Corporation, SEH America, Sumitomo Sitix Silicon, and Wacker Siltronic from the wafer vendor community, and recent additions Intel and Texas Instruments(pending) from the IC manufacturors. Representatives of the silicon equipment and metrology support industries have also been invited to join. The organizational structure for the Center is supported by NSF.

Looking back to its origins, SiWEDS has its roots at Sematech where a committee was convened by Dr. Howard Huff in 1993 in order to define that portion of the 1994 Semiconductor Industry Association`s (SIA) National Roadmap for Semiconductors related to Materials and Bulk Processes. Following completion of the 1994 Roadmap, Sematech continued to hold meetings with the major silicon wafer manufactures and materials experts from the IC community, and to provide travel funds for the seven professors on the committee. The SiWEDS center was unofficially formed in February 1996 when support for university based research programs was initiated by the silicon wafer vendors. Professors Robert Helms of Stanford and George

Rozgonyi of NCSU were the founding directors. A formal Industry/University Cooperative Research Center funded, in part, with a five-year administrative support grant from the NSF's I/UCRC program was started in December 1997

Research activities aim to enhance our understanding of both fundamental and technical issues related to the measurement and control of contamination and defects. Projects addressing the underlying mechanisms and processing applications for the gettering of impurities and preparation of atomically ideal surfaces are in place. They include theory, experiment, and modeling/simulation in three highly interactive task areas of Surfaces, Bulk Crystals/ Wafers, and Metrology, which serve to nucleate and couple focused university/industry working groups. The educational component of the Center's mission is enhanced through strong interactions between graduate students, post-docs and engineers/scientists from the Center Industrial Membership. Projects are established by the submission of specific white paper proposals to the Industrial Advisory Board. A key aspect of the process is the identification of research partnerships between the university and industrial members; particularly as the industry is rapidly approaching the 300mm wafer diameter and 100nm critical device dimension era.

A number of SiWEDS activities have a strong overlap with problems faced by the crystalline photovotaic workshop attendees. These include Diffusion, Segregation, Precipitation and Gettering of Fe, Ni, and Cu; Development of a Gettering Simulator, Novel Surface Passivation Treatments; Oxygen Precipitation/Point Defect/Metal Interactions; Frequency Dependent Lifetime and Diffusion Length Characterization; Imaging of Electrical Active Defect Centers; as well as issues related to Packaging Reliability. A General overview of these programs, emphasizing the value of strong industry/university interactions, will be give at the workshop.

Novel Glass-Ceramic Substrates for Thin Film Polycrystalline Silicon Solar Cells

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Introduction

The economical production of thin film polycrystalline silicon solar cells requires transparent substrates that can be processed at high (T>700°C) temperatures. The most heat resistant commercial glass substrates soften at temperatures above 620 °C. Fused silica (often referred to as 'quartz') is transparent and meets the temperature requirements but is expensive and its thermal expansion coefficient is 1/5 of that of silicon, leaving a polysilicon layer deposited at high temperature under a tensile stress.

Glass-ceramics can be formulated to be transparent, resistant to high temperatures and to match the thermal expansion of silicon. The main concern of processing glass-ceramics is that the glass components can out-migrate from the substrate and contaminate the device.

Glass-Ceramic Substrates

After surveying all glass-ceramic systems, the spinel structure SiO_2-Al_2O_3-ZnO-MgO-TiO_2, ZrO_2 was selected [1]. The final microstructure of the glass-ceramic consisted of 10-15 nm-sized spinel crystals, dispersed uniformly in a siliceous glass matrix.

Some glass components, such as alkali atoms, are mobile at the elevated temperatures and can migrate out of the substrate during high temperature processing [2]. To prevent the out-migration of substrate components into the thin film electronics the glass-ceramic substrates need to be coated with a barrier layer.

A triple stack of SiO_2/SiN_x was deposited by Low Pressure Chemical Vapor Deposition (LPCVD) and annealed in N_2 at 900 °C for 8 hours. Secondary ion mass spectroscopy (SIMS) showed that the first SiO_2 layers was saturated with glass-ceramics components (Fig. 1). The concentration of glass components dropped in the first SiN_x layer and reached background levels in the following layers.

Further studies showed that barrier layers deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) had lower surface roughness and higher transparency. A PECVD barrier layer consisting of 1000 Å of SiN_x followed by 1000 Å of SiO_2 was found to meet all requirements. Glass-ceramics coated with this barrier layer were therefore used as substrates to fabricate both majority carrier devices (thin film transistors) and minority carrier devices (p-i-n junction diodes).

Thin Film Polysilicon Transistors

Thin Film Transistors (TFTs) permit to quantitatively measure the carrier mobility and density of mid–gap states in polysilicon. TFTs were fabricated on glass-ceramic, fused silica and oxidized silicon substrates. The 1000 Å thick channel polysilicon was deposited by LPCVD at 550 °C as amorphous and then recrystallized at 900 °C. The gate oxide was also deposited by LPCVD. A detailed process description can be found at [3,4]. The device characteristics were analyzed using a combination of classical MOSFET theory [5] and TFT theory [6].

TFTs fabricated on all substrates had lower leakage currents (below 30 pA) and higher carrier mobility (over 60 $cm^2/V \cdot sec$) (Table 1) than devices fabricated previously on Corning 1737 glass substrates at 620 °C [4]. Figure 2 shows current-voltage curves for TFTs fabricated on various substrates. Note that the performance of TFTs on glass-ceramic and fused silica substrates exceeds those on oxidized silicon wafers. Possible reasons include different grain structure, different gettering ability of substrates, and the electric field distribution in TFT with and without a ground plane, all of which are being investigated.

P-i-n Junction Diodes

To investigate if glass-ceramics would make suitable substrates for thin polysilicon film solar cells, we fabricated and tested p-i-n junction diodes on barrier layer coated glass-ceramics, fused silica substrates and oxidized silicon wafers. The device consisted of 500 Å n+, 6000 Å undoped (i-) and 1500 Å p+ polysilicon deposited at 550 °C and annealed for 4 hours at 900 °C. Grain size of the deposited polysilicon film ranged from 100 Å to 1000 Å. The structures were patterned by photolithography and etched to form isolated devices. Aluminum contacts were deposited on the top and annealed in H_2 at 400 °C for 0.5 hour.

The dark current-voltage characteristics (I-V) were measured and analyzed. P-i-n junctions on both glass-ceramic and oxidized silicon substrates had low reverse leakage currents and high breakdown fields, while on fused silica device performance was much poorer (Fig. 3). Oxidized silicon and glass-ceramic substrates have a coefficient of thermal expansion (CTE) matched to Si, whereas fused silica does not. During cooldown from the high temperature anneal the difference in CTE induces a tensile strain of 0.2% into the polysilicon film. The corresponding tensile stress can reach 60 000 psi exceeding breaking strength of polysilicon which is between 10 000 and 35 000 psi [7]. Visual inspection confirmed the formation of cracks in the polysilicon films that degrade the performance of large area devices fabricated on fused silica substrates.

The forward current-voltage characteristics of solar cells and p-i-n diodes followed an exponential law with ideality factor of ~ 2. This behavior is expected for semiconductor materials such as polycrystalline silicon containing near mid-gap recombination states [8].

Conclusions

Novel transparent glass-ceramics having the high strain point (over 950 °C) and CTE matching to Si, developed by Corning Inc. were shown to be suitable substrates to fabricate low cost thin film polycrystalline solar cells. Out-diffusion of glass components from the substrate could be effectively suppressed with a simple PECVD SiO_2/SiN_x barrier layer.

Thin film transistors fabricated at 900 °C on glass-ceramic substrates had leakage currents and electron mobilities comparable to devices on fused silica and oxidized silicon wafers.

The performance of p-i-n junction diodes, simulating solar cells, fabricated on the glass-ceramic substrates matched that of devices made on oxidized silicon. The difference in thermal expansion coefficient of silicon and fused silica was shown to be the reason for the poor performance of p-i-n diodes fabricated on fused silica substrates.

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Figures and Tables

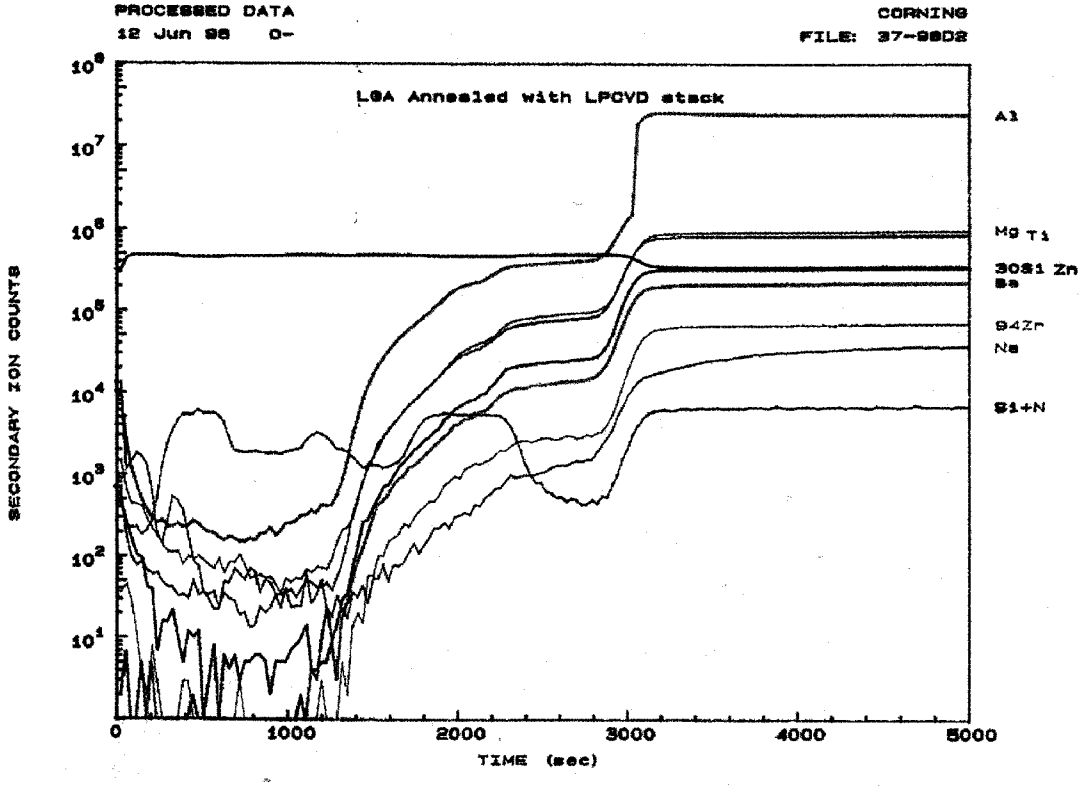

Figure 1. SIMS profile of glass-ceramic components in a triple SiO_2/SiN_x barrier layer. The location of the three SiNx layers is clearly visible in the Si+N profile.

	V_{fb}, V	I_{min}, pA	•, $cm^2/V{\cdot}sec$	Q_t, $10^{12}cm^{-2}$	S, V/decade	V_{th}, V
Oxidized Silicon	2.7± 0.7	83± 14	36.70± 8.97	6.71± 0.37	3.41± 0.26	15.4± 1.3
Fused Silica	-4.3± 0.4	13± 4	80.24± 9.10	4.90± 0.18	1.29± 0.11	3.3± 0.5
Glass-Ceramic	-0.8± 0.7	25± 4	66.19± 14.9	7.10± 0.28	3.08± 0.22	13.0± 0.8

Table 1. Parameters of TFTs fabricated on glass-ceramic, fused silica and oxidized silicon wafers. The columns list, left to right, the flat band voltage, V_{fb}; the leakage current, I_{min}; the intrinsic electron mobility •; the trap density Q_t; the subthreshold swing S; and the threshold voltage V_{th}.

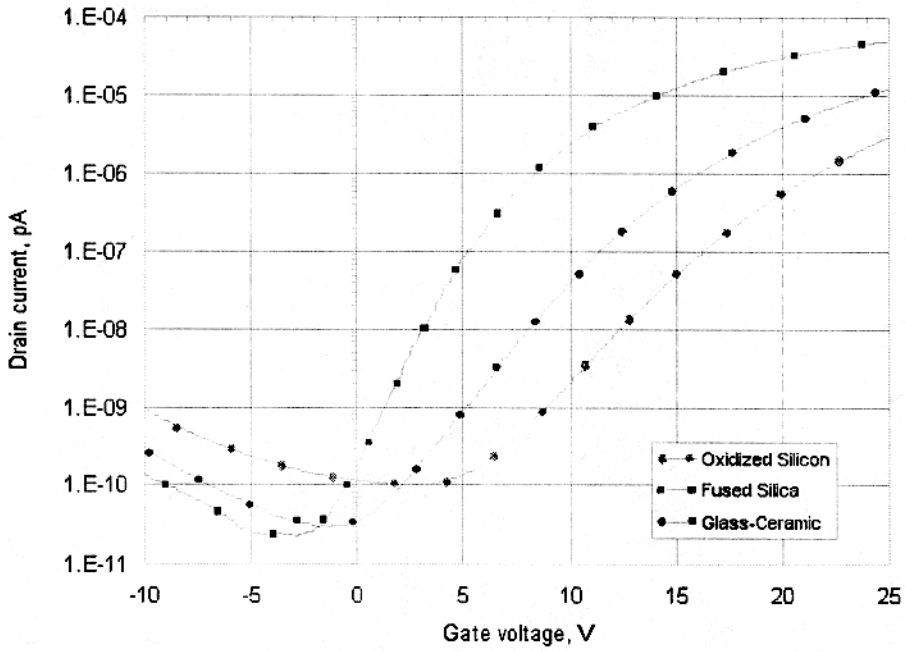

Figure 2. Current-voltage characteristics of thin film transistors fabricated on oxidized silicon, fused silica and glass-ceramic substrates. Channel size is 15 μ x 15 μ. Source-drain voltage V_{sd} =10 V.

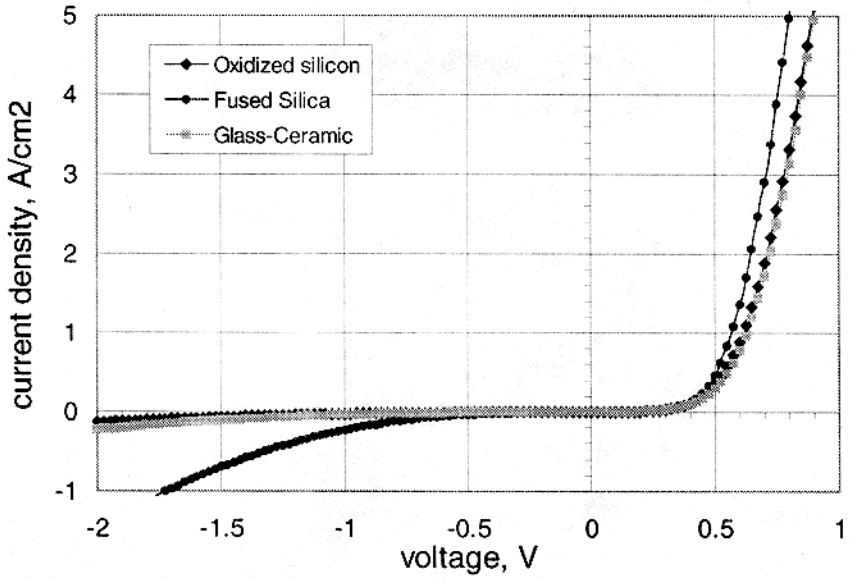

Figure 3. Dark current voltage characteristics (I-V) of p-i-n junction diodes fabricated on oxidized silicon, fused silica substrates and glass-ceramic coated barrier layer.

Material Aspects of Crystalline Silicon Thin Film Solar Cells on Glass

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Abstract: The properties of crystalline Si films on glass are of primary importance for thin film solar cells. The paper outlines general features of Si films relevant to device applications obtained from various crystallization processes. Electronic properties of polycrystalline Si films closely depend on the grain size that determines an upper bound of device performance. Conditions are derived that need to be fulfilled in order to realize efficient thin film solar cells based on poly-Si on glass.

Introduction

The fabrication of solar cells based on thin, crystalline Si films on foreign substrates appears to be an attractive route to realize cheap and efficient photovoltaic devices [1-4]. Combining crystalline Si with glass as a cheap substrate material that in addition allows one to realize very efficient light trapping [5] has stimulated a lot of research activities during the last couple of years. The limited thermal stability of glass and its amorphous nature led to the development of a great variety of techniques to deposit and crystallize device-grade crystalline Si films [6-9] or to transfer monocrystalline Si films onto glass or plastic substrates [10, 11]. From today's perspective, it appears that thin film crystalline Si has not yet fulfilled it's high efficiency promise that resulted from record efficiencies exceeding 24 % using high-quality bulk Si wafers and complex processing [12]. I will therefore discuss the material aspects of crystalline Si thin film solar cells that have to be understood in order to evaluate the limitations involved with the use of poly-Si films deposited at low temperatures.

1. Classification of crystalline Si films

A basic classification of the properties of crystalline Si films may be obtained according to the grain size of the films. In most cases, the grain size is intimately related to the processing temperature used to create the films. In addition, the grain size also determines the choice of the electrical design of the solar cell. Cells based on nanocrystalline Si (nc-Si) films or micro-crystalline Si (μc-Si) films use an intrinsic or moderately doped absorber and therefore employ a pin-junction with a built-in drift field. Large-grained polycrystalline Si (poly-Si) cells use absorbers with a higher doping level and thus employ pn-junctions based on minority carrier diffusion for charge carrier separation. Crystalline Si solar cells based on pn-junctions can, in principle, deliver higher open circuit voltages as compared to pin-devices, as has been shown by modeling of solar cell structures based on thin monocrystalline Si films using PC-1D [13].

However, the doping level required for pn-junctions leads to high recombination of minority carriers at grain boundaries and therefore deteriorates device performance in fine-grained poly-Si films. Open-circuit voltage limitations predicted by device modeling based on the parameters of crystalline Si are, however, not necessarily valid for thin film cells fabricated from nc-Si [14], as this material consists of a mixture of nanocrystalline and amorphous phases [15].

Figure 1 gives a schematic representation of four basic material systems in order to elucidate four different types of crystalline Si films on foreign substrates: a) nc-Si films are deposited on (metal coated) glass substrates at temperatures well below 450°C [16], b) µc- or fine-grained poly-Si is deposited or crystallized on soda-lime, borosilicate [17], or alumina silicate glass [18, 19] or metal films [20] at medium temperatures in the range of 450 to 700°C, c) large-grained poly-Si is formed and processed by (zone) melting processes on high temperature resistant substrates such as graphite, ceramics [21] or high-temperature glass [22] at temperatures well above 800°C. d) Finally, the formation of monocrystalline Si films requires a process that transfers a monocrystalline Si film [10] grown on a monocrystalline Si substrate to a foreign substrate, which can in principle be of arbitrary nature.

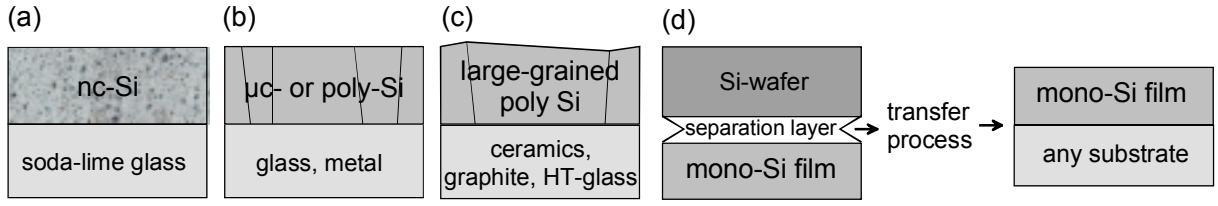

Figure 1: Classification of crystalline Si films on foreign substrates according to grain size. a) nc-Si films with a grain size g ≈ 10 nm deposited at temperatures below 450° on soda lime glass. b) µc- or poly-Si films with a grain size in the range of 0.1 to 100 µm formed by direct deposition and/or solid phase crystallization at temperatures around 450 to 700°C or by laser (re-) crystallization. Substrates such as metal foils or glass may be used, depending on the thermal budget of the process. c) large-grained poly-Si films with mm or larger sized grains are obtained from (zone) melting processes at high temperatures T > 800°C mainly on ceramic substrates and graphite or on high-temperature glass. d) Monocrystalline Si films on foreign substrates are formed on Si wafers and are subsequently transferred to a suitable substrate.

The following discussion in the rest of this paper is centered around the properties of poly-Si as shown in Fig. 1b. Further literature on the properties of nc-Si, large-grained poly-Si and monocrystalline Si films can be found in [1].

2. Properties of poly-Si films obtained from random nucleation and growth processes

The grain size distribution in poly-Si usually obeys a log-normal distribution [23], regardless of growth temperature, crystallization technique or the grain size itself. A comparison of grain size distributions [24] in fine-grained poly-Si having a grain size in the sub-µm range and cast Si with a grain size of several mm shows that, although the grain size is three orders of

magnitude higher in the latter case, the shape of the distribution is the same in both cases. The formation of log-normal grain size distribution is a consequence of the interaction of i) random nucleation, ii) simultaneous grain growth, and iii) a limited volume of crystallization. A detailed treatment of the development of grain size distributions is found in Refs. [25-27] for the case of solid phase crystallization and in Refs. [28, 29] for the case of grain coarsening. As a consequence, Si obtained from almost *any* random nucleation and growth process is expected to have a fairly wide range of grain sizes characterized by a log-normal distribution.

For solar cells, a wide grain size distribution is detrimental: While the photo-generated current obtained from a solar cell is determined by averaging the diffusion length distribution, the open circuit voltage strongly decreases as a consequence of even a small fraction of grains with a small effective diffusion length [30]. Recent investigations have shown, that the minority carrier diffusion length distribution in large-grained cast Si is bimodal and solar cell performance is significantly decreased by the presence of areas with low diffusion length [31]. An additional complication arises from the fact, that further electrical inhomogeneities are present in poly-Si due to an inhomogeneous distribution of intra-grain defects, which are, in the case of cast Si, identified as defect clusters [32]. Such inhomogeneities have been detected in fine-grained poly-Si [33] as well as in large-grained poly-Si [32].

3. Dependence of open circuit voltage on grain size in poly-Si

As follows from the arguments given above and a more detailed treatment in [34], the grain size sets a primary upper bound to the device performance of poly-Si films for a range of grain sizes g around 1 µm < g < 1 mm. I will now assume the diode saturation current of a poly-Si thin film solar cell to be dominated by recombination at grain boundaries, as the pn-junction potential barrier is considerably reduced at grain boundaries. The open circuit voltage V_{oc} in this case depends on g following the relation $q\ V_{oc}(g) = q\ V_{oc}^{*} - n\ kT\ \ln(g^{*}/g)$. Here, q is the elementary charge, k is the Boltzmann-constant, T stands for the absolute temperature and n is the diode ideality factor. The critical parameters V_{oc}^{*} and g^{*} set the scale for the grain size dependence of V_{oc}. Figure 2 shows a compilation of experimental data of V_{oc} of poly-Si thin film cells compared to the relation derived above, for more details see [34].

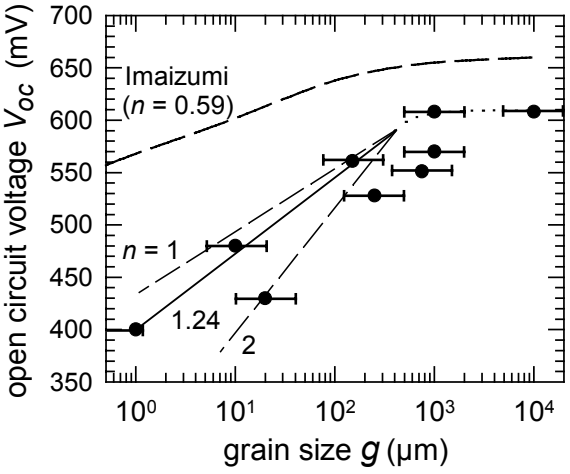

Figure 2: Open circuit voltage V_{oc} as function of grain size g: Experimental results of poly-Si thin film solar cells (dots), sources of data are given in Ref. [1]. Dashed line in the upper part of the graph shows prediction of V_{oc} as function of g for a 100 µm thick Si solar cell [35], not taking into account a reduced barrier height at grain boundaries. Dashes and solid lines in the lower part of the graph show $V_{oc}(g)$ assuming ideality factors n between 1 and 2.

4. Critical parameters for low-temperature epitaxial growth of Si

Three aspects have to be taken into account when depositing poly-Si films at low temperatures: i) The deposition rate of most techniques used to fabricate crystalline Si films strongly depends on substrate temperature. Figure 3 shows a compilation of data on epitaxial deposition rates as function of substrate temperature, data presented here are updated from [36]. Ion-assisted deposition [37] presently achieves the highest epitaxial deposition rate at substrate temperatures below 600°C. ii) At growth temperatures below 450°C, epitaxial growth of Si, e.g. on seeded glass substrates, terminates at a critical epitaxial thickness that is temperature dependent [38]. Epitaxial films with a thickness of several µm can only be obtained at temperatures larger than about 500°C. iii) The diffusion length determined in Si films deposited at low temperatures strongly depends on the deposition temperature [37, 39]. As a consequence of these considerations, deposition of crystalline Si must take place at the maximum temperature tolerable to the glass substrate.

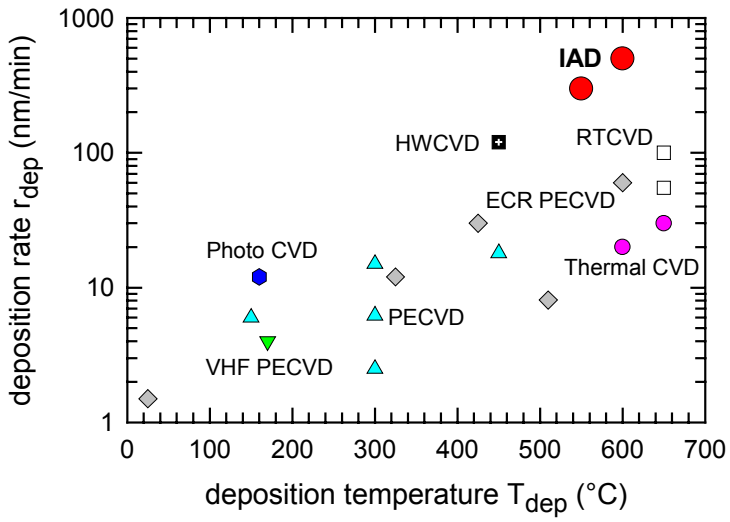

Figure 3: Comparison of epitaxial deposition rates r_{dep} of various deposition techniques suitable for low-temperature Si epitaxy: Ion-assisted deposition (IAD) reaches r_{dep} = 0.5 µm/min at a deposition temperature T_{dep} = 600°C. CVD-techniques: HW: hot wire, ECR: electron cyclotron resonance, PE: plasma enhanced, VHF: very high frequency.

5. Conclusions

Looking at material aspects for the formation of poly-Si films on glass, the following conditions appear to be of significance in order to realize efficient poly-Si thin film solar cells on glass: i) Grain size should be larger than 100 µm. Presently, laser crystallization appears to be the only candidate capable to achieve this goal in combination with the thermal boundary conditions imposed by commercially available glass substrates. ii) Deposition temperature for the formation of crystalline Si films has to be as high as the glass substrate allows for in order to achieve a maximum minority carrier diffusion length. iii) In view of the low deposition rates obtained at low temperatures, it is essential to develop high rate deposition techniques. Ion-assisted deposition appears to be particular suitable in order to realize a high-rate, low-temperature epitaxial deposition process.

Until now, poly-Si on glass has not yet fulfilled it's promise for high efficiencies. However, the boundary conditions for a successful outcome appear to be become increasingly clear and research may be focused in view of the above findings.

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A Review of Stand Alone Thin-Film Silicon Layers

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1 Abstract

The formation of layers of thin film crystalline silicon which may be detached from a reuesable substrate is reviewed. Such layers have a very high efficiency potential, and due to the small amount of silicon which is used, a low cost potential. Efficiencies as high as 16% for a 77μm thick layer and 12.5% for a 12μm thick layer have been reported by Mitsubishi and Sony respectively.

2 Introduction

Thin film silicon layers which can be detached from a reusable silicon substrate have a very high efficiency potential. This is mainly due to the fact that as the substrate is recycled, there is no need to compromise on material quality. In addition, the inherent disadvantages of deposition on non-silicon substrates such as diffusion of impurities, material defects and film stresses are absent [1]. The radiation tolerances of these thin-film cells may be very high because large amounts of damage can be sustained before the diffusion length falls to less than the wafer thickness.

Most of the groups working in this area grow single crystal silicon on a high quality substrate with a sacrificial attachment region. The sacrificial region may be of a different doping level, made from porous silicon or made from SiO_2. A disadvantage of using doping levels and dopant selective etchants is that high temperatures may broaden doping profiles. A porous silicon sacrificial layer allows epitaxy, bonding and oxidation to occur at higher temperatures. Porous silicon also has a very high etch selectivity over non-porous silicon; ratios of up to 10^5 have been demonstrated [2]. When hydrogen is used in the growth of non sc-Si, it is used for both grain boundary passivation and for growth. Thus, when hydrogen is used, the growth of sc-Si is advantageous over layers containing grain boundaries in that less hydrogen is used [3].

Groups who are working on detachable layers include Mitsubishi Electric Corporation, Sony Corporation, a German consortium, the Australian National University, Silicon on Insulator Technology (SOITEC) and Canon Incorporation. With the exception of Canon, the groups detailed here aim to recycle the substrate. At present this has not been a major focus of the literature and if it has been demonstrated, it has not been published.

3 VEST process - Mitsubishi Electric Corporation

A 77μm thick cell with an area of 96cm^2, an efficiency of 16% and a V_{oc} of 589mV has been achieved using the VEST (etching of underlying substrate through via-holes in the silicon film) process at Mitsubishi Electric Corporation [1] [4]. Mitsubishi have also demonstrated the reliability of their technique. From a batch of cells of 10cm^2 area, 22 of 25 had an efficiency greater than 15% [1].

VEST cells are made by first separating the active layer from the substrate and then fabricating a cell.

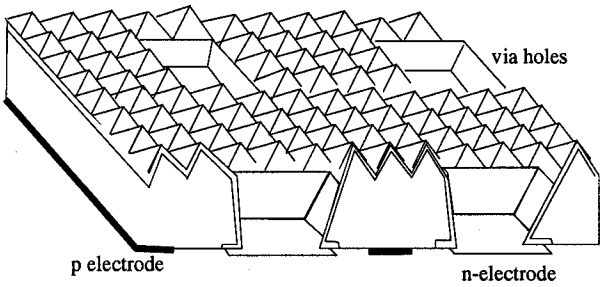

Figure 1: Schematic of the VEST cells, after Morikawa et. al. [4]

Figure 1 shows the detached VEST cell structure. Layer separation is achieved by forming a silicon on insulator (SOI) layer on SiO_2 deposited on a c-Si wafer. A thin seeding layer of silicon ($3-5\mu$m) is deposited by CVD followed by a capping layer of Si_3N_4 and SiO_2. This is followed by zone melt recrystallisation (ZMR) [5]. The resulting silicon is mainly (100) orientated. A thick active layer is then epitaxially grown. An anisotropic etch through a masking layer is used to form an aray of $100\mu m^2$ via holes through the silicon layer to the underlying SiO_2. The hole spacing is 1.5mm. The SiO_2 layer is then removed with HF which enters through the via holes, causing layer separation. Cell fabrication is preceded by another anisotropic etch which forms random pyramids on the front surface.

Cell fabrication involves a phosphorous diffusion to form a heavily n-type region over the entire surface and down the via holes, an etch back of the front surface to form the emitter and application of a SiN antireflection coating using LPCVD. The final steps are formation of an interdigitated pattern of n and p regions on the rear surface, screen printing of both base and emitter electrodes and implantation of hydrogen ions for passivation. The electrodes are made of a paste which is screen printed directly onto the cell. For the emitter it is a Ag paste and for the base, a Al containing Ag paste [4].

A feature of the VEST technique is that the ZMR process results in a mostly (100) surface orientation which allows texturing. Finger shading losses can be avoided since both electrodes are on the rear and current is collected through the via holes. The c-Si substrate may be recycled [1].

The VEST cell fabrication technique has been optimised to overcome a number of difficulties. The diffusion length, L_{diff} after ZMR is quite low (40μm) and this has been increased to 167μm by phosphorous gettering and etch back. There is a decrease in fill factor caused by the high series resistance of the emitter since both contacts are on the rear and the via holes are widely spaced. This has been partially overcome by arranging for a heavy phosphorous diffusion in the via holes and a lighter diffusion on the top surface. The top surface diffusion is $60\Omega/\square$ which results in a significant loss of blue response. A drawback of the VEST technique is that at present the electrodes are formed by a screen printing process, which requires a minimum film thickness of about 80μm [1].

4 Sony Corporation

Sony Corporation have used a sacrificial porous silicon layer and have achieved a 12μm thick, thin film cell of $4.0cm^2$ area, with an efficiency of 12.5% and V_{oc} of 623mV [6]. A material lifetime of 60μs has been demonstrated.

Sony cells are made by first anodising a silicon substrate. Three porous silicon layers are formed, two of low porosity (16% top layer and 26% bottom layer) and one of high porosity (40-70%). The location of the various porosity layers is shown in figure 2. The function of the high porosity layer is to allow easy separation of the cell layer from the substrate. The crystalline structure and pore distribution of the porous silicon are altered by a high temperature hydrogen anneal at 1100°C for 30 minutes. This causes the low porosity layer to form small, circular pores while the high porosity layer tends to form broad based pillars and wide voids. During this anneal, the porous layer also acts to getter metals. Epitaxial growth of the active silicon layer occurs directly onto the top surface of the substrate and as this is of low porosity, the grown layer has a low lattice strain. A 1μm thick p^+ layer is grown epitaxially onto the substrate, using silane and hydrogen diluted B_2H_6 gas at atmospheric pressure. This is followed by the growth of

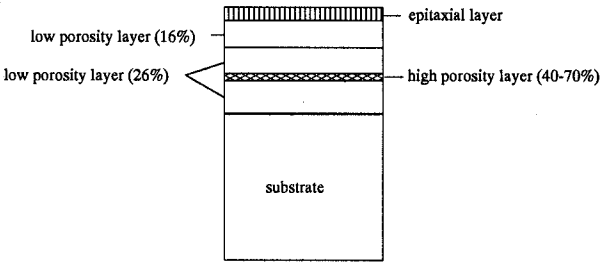

Figure 2: Structure of the substrate, porous silicon and epitaxial layers of the Sony cells, after Tayanaka et. al. [6]

an 11μm thick p-layer which forms the base region of the solar cell. Phosphorous diffusion, application of a TiO_2 antireflection coating and metallization completes the cell. Layer separation is achieved by the application of a weak tensile stress or ultrasound. The porous layer is then removed and the substrate can be recycled [6].

The 12.5% efficient cell had an oxidation step which served to passivate the front surface and a TiO_x antireflection coating. An inexpensive plastic film was adhered to the front surface for mechanical strength.

A minor disadvantage of the process developed at Sony is that the porous layer is 8μm thick at present and this is sacrificed in cell production. A planned improvement is to put an optical reflector on the rear of the cell [6].

5 Ψ process

The Perforated Silicon (Ψ) process developed by a consortium of German groups is very similar to the technique used at Sony. A lifetime of 0.27μs and L_{diff} of 11μm have been achieved on a 5.8μm thick layer [7].

The first step in the Ψ process is the texturing of the surface of a sc-Si substrate using a combination of photolithography and KOH etching. Two distinct porous silicon layers (PSL) are then formed on the substrate using an anodic etch in HF solution. The upper layer is about 30% porous and the bottom about 50%. The PSL are stabilised by an oxidation step. Prior to epitaxy, the sample is heated to 850°C for around 10 minutes to remove the native oxide which forms on the porous silicon. A layer of silicon is deposited using ion assisted deposition (IAD) at a substrate temperature of 700°C and a deposition rate of 4-20μm/hour. The deposited film has the same crystallographic structure as the substrate. A low temperature deposition technique is advantageous since at temperatures greater than 850°C, sintering of the porous silicon occurs due to the surface mobility of silicon atoms on the inner surface. Once cell fabrication is complete, the layer can be separated from the substrate using mechanical stress. This is done by attaching a glass superstrate to the front surface with a transparent encapsulate (poly-ethylenphtalate). Further steps, such as suface passivation and reflector formation on the rear surface, must occur below a temperature which both the encapsulate and superstrate can withstand. Earlier versions of the Ψ cells, which did not have the two porosity levels, were removed by a 2 minute ultrasonic agitation. The rear surface is then passivated and a reflector added. After the PSL is removed, the substrate can be reused several times before retexturing [3] [7].

Future improvements which are planned include a reduction in the porous layer thickness (from about 6μm to less than 1μm) [3] and an increase in the deposition rate [7].

Work on the Ψ process to produce waffle cells has been done by a collaboration of groups from the Bavarian Center for Applied Energy Research, Universität Erlangen-Nürnberg, ANTEC GmbH, Robert Bosch GmbH, and Universität Stuttgart. The films are termed waffle due to the three dimensional texturing of the entire film. The optimum period of texturing for effective light trapping (and reflection control) has been theoretically determined to be about the same as the waffle thickness. Layers of 85mm in diameter have been separated from the substrate using mechanical stress. A feature of this technique is that the

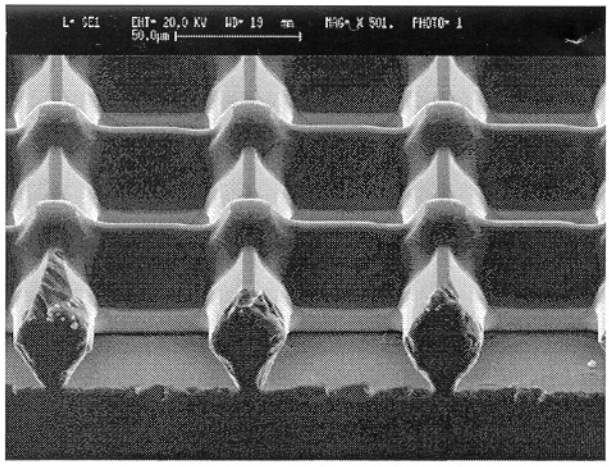

Figure 3: The epilift struture. The epilayer is still attached to the substrate and the diamond cross section of the layer is visible [10].

emitter is grown epitaxially, since this is faster than diffusion. A 7.8μm thick, pyramidal structure with a dislocation density less than $10^4/cm^2$ has been formed [3].

6 Epilift process - ANU Centre for Sustainable Energy Systems

At the ANU Centre for Sustainable Energy Systems, the epilift process has been used to grow layers of 50-100μm thickness on single crystal silicon. A lifetime of 3.8-11.7μs for a sample with a light phosphorous diffusion and thin oxide as surface passivation has been achieved [8].

The epilift process involves deposition and patterning of a masking layer on a sc-Si substrate. The masking layer is exposed in a mesh pattern; lines are of 2-10μm width and spaced 50-100μm apart. The substrate is usually orientated in the (100) direction, the mesh in (110) directions. An epitaxial layer is grown on the substrate using liquid phase epitaxy (LPE). The growth faces have mostly (111) orientation and the layer has a diamond cross section, giving it a natural antireflection texture. Initially deposited layers are more heavily doped (which means they are etched faster) and later layers more lightly doped. A selective etch is used to remove the epilayer. The masking layer and substrate may be reused provided the masking layer is not attacked by the etch. Figure 3 shows an SEM image of the epilayer structure attached to a substrate [8] [9].

The epilift layer grows in a mesh pattern and the holes can be closed over to an arbitrary amount. An advantage of the holes is that they allow both contacts to be on the rear, thereby avoiding shading losses. A possibility for cell fabrication is to leave the epilayer partially attached to the substrate (for example, at the corners) and to process the cell, attach the epilayer to a superstrate and then detach the cell from the substrate [9].

An indium solvent is used in the growth of epilayers, and films with an area of $10cm^2$ and a thickness of up to 100μm have been detached. A film without holes was achieved by leaving an epilayer attached only at the corners, growing again and using shear force to separate the layer. A potential problem with the technique is that the material may have a high dislocation density [9]. The dislocations are due to the oxide mask used and are not evenly distributed across the wafer [8]. Cell efficiencies achieved by this process have not been reported.

7 Smart Cut - SOITEC

'Smart Cut' technology has been introduced at Laboratoire d'Electronique de Technologie et d'Instrumentation (LETI) and co-developed with SOITEC (Silicon on Insulator Technology). The technique provides

a method for separating a thin layer of silicon from a bulk wafer [11]. At present it is mainly in use in the IC industry, although it has applications for solar cells [12]. The technique involves growing a SiO_2 layer, and implanting hydrogen into the silicon underneath this layer. Most of the hydrogen atoms come to rest some distance below the silicon/SiO_2 interface, creating a mechanically weakened layer. By bonding the SiO_2 layer to a silicon wafer or a quartz or glass superstrate, a thin (200nm) layer of silicon can be peeled from the original wafer [11] [12]. When a silicon wafer is used as the superstrate, separation is achieved using a heat treatment at 400-600°C. A second heat treatment at more than 1000°C is used to strengthen the chemical bonds between the superstrate and the thin silicon layer. The substrate wafer can then be polished and is ready for hydrogen implantation and reuse [11].

Advantages of the technique are that the implant temperature is quite low (less than 600°C) [11] and that the silicon layer has low defect levels which are close to those of bulk silicon [13].

Since the separated layer is very thin (200nm [13]) epitaxial growth of a thicker active layer of silicon must take place after separation of this seeding layer from the substrate. A supporting superstrate that has a thermal expansion coefficient similar to silicon will be needed. A number of options exist for such a substrate, such as an oxidised silicon wafer with pre-existing holes at a 1mm spacing. Separation of this wafer from the epitaxially grown layer would simply require immersion in hydrofluric acid (HF). There is also some concern about the cost of hydrogen implantation.

8 Eltran Process - Canon Incorporated

A technique termed ELTRAN (epitaxial layer transfer) has been developed by Canon. This is based on a new BESOI (bond and etch back of silicon on insulator) technology [2]. An epitaxial layer is formed on a 10μm thick porous silicon layer by chemical vapour deposition (CVD) at 1000-1150°C and the rear of the surface is exposed by grinding away the original wafer. The porous silicon can then be removed. An etchant selectivity of 10^5 has been achieved [2]. At present, the fact that the substrate wafer is destroyed makes this process inapplicable for solar cell technology. However, in future the technique may be adapted for photovoltaic applications.

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Directly Deposited Microcrystalline Silicon

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Direct deposition from a glow discharge or by hot wire CVD is the lowest-temperature process for obtaining microcrystalline silicon. Films of material so grown have a complex structure with grain sizes ranging from 3 *nm* to 50 *nm*.

This type of microcrystalline silicon (μc-Si:H) has been grown and studied for 30 years, and has been introduced to device use since the early 1980s. For the first ten years of its device life μc-Si:H was viewed as a more highly conducting alternative to hydrogenated amorphous silicon (a-Si:H). It was used in contact layers to a-Si:H solar cells and thin film transistors. This view began to change with the demonstration of an *n* channel thin-film transistor (TFT), a unipolar device [1]. The breakthrough for μc-Si:H as a universally usable device material came with demonstration and development of a solar cell, a bipolar device, with an active *i* layer of μc-Si:H [2]. A *p* channel TFT of μc-Si:H and a complementary metal oxide silicon (CMOS) inverter of a *p* and an *n* channel TFT integrated on one μc-Si:H film were demonstrated recently [3]. The *p* channel TFT shows that TFT-usable hole mobilities can be achieved in μc-Si:H, in contrast to a-Si:H. μc-Si:H also is being explored as a material for micro-electromechanical systems (MEMS) [4]. By now it is clear that μc-Si:H will continue to be investigated for a wide range of device applications, as it combines the capability of low-temperature, large-area deposition with true bipolar operation.

The common approach to the deposition of μc-Si:H is growth in the presence of a large density of hydrogen radicals. μc-Si:H layers start out amorphous. Within a few *nm* from the substrate crystal growth sets in. An amorphous-to-microcrystalline phase transition in function of film thickness and hydrogen dilution ratio (H_2:SiH_4) has been identified by spectroscopic ellipsometry [5]. The crystals grow columnar, with their diameter increasing toward the top surface of the film. The growth rate is slow at typically $\leq 0.1\ nm\,s^{-1}$. Commonly used structural probes include X-ray diffraction, transmission electron microscopy, UV reflectance, and Raman scattering. Hydrogen, bonded in concentrations of several atomic percent, is analyzed by IR spectroscopy.

The optical absorption spectrum of μc-Si:H lies closer to that of x-Si than of a-Si:H. Films with thickness of several μm, as used for solar cell *i* layers, have optical gaps of ~ 1.1 *eV*. Optical gaps of up to 2 *eV* have been reported for very thin films, such as those used for contact layers to a-Si:H solar cells.

Even though the structure of μc-Si:H films is complex, their electrical properties can be explained with the standard model for polycrystalline silicon [6]. In this model the films are conducting if the number of charge carriers in the grains suffices to fill the grain boundary traps. On the other hand the films behave like intrinsic silicon if the carriers

are fully depleted from the grain into grain boundary traps. One consequence of this interplay between free carriers and grain boundary traps is that the conductivity can vary with film thickness by several orders of magnitude. Nominally undoped μc-Si:H is *n* type, in consequence of a large density of typically 10^{19} cm^{-3} of oxygen donors. The solar cells of μc-Si:H were made possible first by careful compensation of the oxygen donor by boron microdoping, and later by purification of the source gases.

Thus research on directly deposited μc-Si:H has been energized by its introduction as a semiconductor for solar cells and for thin film transistors. We can expect continued exploration of the growth, properties, and device applications of μc-Si:H.

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THE AFFECTS OF HOTZONE MODIFICATIONS ON CZOCHRALSKI GROWN SOLAR CELLS

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Abstract

Energy and Argon are two costly components used in the Czochralski (CZ) growth of Silicon ingot for solar cell manufacturing. Siemens Solar Industries (SSI), in cooperation with the Northwest Energy Efficiency Alliance (NEEA), is developing an energy efficient hotzone (EEH) which significantly reduces consumption of these costly resources. The EEH modifications resulted in substantial reductions in energy and Argon, as well as improvements in productivity, yield, and ingot characteristics. Solar cells manufactured from these systems show marked improvements in short circuit current (Isc), open circuit voltage (Voc), fill factors (FF), and current at rated voltage (Ivr).

Introduction

Past efforts to design hotzone improvements have focused primarily on ingot quality, while providing little information on the actual energy values achieved with the new designs. [iiiiiiivv] The SSI/NEEA project is unique in that the primary objective of the project is to reduce energy, Argon, and associated waste products. The hotzone components consist of various insulation designs, supports components, and heating elements. Recent advances in these components suggest that less power could be used to produce higher quality ingots. SSI capitalized on these improvements and designed an energy efficient hotzone (EEH) using a combination of new components and improved designs.

Ingots grown from standard and EEH assemblies were collected to characterize ingot quality and performance. The ingot characterization consisted of glow discharge mass spectrometry (GDMS) and Fourier transform infrared spectroscopy (FTIR) analysis of carbon and oxygen content. In each analysis independent companies were used. In addition, samples grown from each assembly were processed into solar cells using the SSI manufacturing facility.

Results and Discussion

1. Ingot Characterization

In order to quantify the affects of the EEH design on the ingot, a group of ingots grown from both standard and EEH assemblies were studied. Samples from these ingots were sent to independent laboratories for GDMS and FTIR analysis. Samples from the top or seed end and the bottom or tang end of the ingots were used. A total of 20 samples were analyzed with GDMS and 40 samples were analyzed by FTIR analysis.

1A. GDMS Analysis

The GDMS is capable of detecting trace levels, (> 5 ppb) and in some cases (> 2 ppb), of metallic contaminants. Samples were cut, rinsed, and labeled before shipping. The laboratory etched the wafers and conducted the tests. Molybdenum components are used in the EEH and are in close proximity to the silicon melt, raising concerns regarding contamination. Contamination of transition metals can result in deep-level defects or traps in solar cells. For this reason, potentially harmful metals were selected for the GDMS analysis. Samples grown in both standard and EEH systems showed no detectable level of metals.

1B. FTIR Analysis

The FTIR analysis examined both axial and radial Oxygen and Carbon content in the ingot. Again, samples from the top and bottom of the ingots grown in a standard and EEH were examined. The samples were chemically polished until a mirror smooth surface was obtained. The samples were analyzed using a Bio-Rad QS-300. The machine is set up using a float zone silicon slug. The data gathered for interstitial oxygen, Oi, was correlated to SRM 2551. All data reported for Oi is in ASTM F121-83 units. Currently there is no SRM for substitutional carbon, Cs. All data reported for Cs is in ASTM F123-83 units. The machine was monitored hourly to insure the stability of the readings. Each slug was measured at the center point for Oi and Cs. Figure 1 shows a table of the data.

Slug #	Assembly	Section	Oi (ppma)	Cs (ppma)	Slug #	Assembly	Section	Oi (ppma)	Cs (ppma)
610317	EEH	Top	17.448	0.086	650313	Standard	Top	20.398	0
610317	EEH	Top	17.489	0.06	650313	Standard	Top	20.557	0
610317	EEH	Bottom	13.03	0.157	650313	Standard	Bottom	17.871	0.262
610317	EEH	Bottom	12.89	0.259	650313	Standard	Bottom	17.553	0.167
610318	EEH	Top	16.872	0.039	650317	Standard	Top	20.559	0.056
610318	EEH	Top	17.119	0.038	650317	Standard	Top	20.622	0.063
610318	EEH	Bottom	13.561	0.211	650317	Standard	Bottom	18.081	0.259
610318	EEH	Bottom	13.479	0.199	650317	Standard	Bottom	17.943	0.318
610319	EEH	Top	17.59	0.07	660316	Standard	Top	19.915	0.047
610319	EEH	Top	17.445	0.048	660316	Standard	Top	20.009	0
610319	EEH	Bottom	13.216	0.31	660316	Standard	Bottom	17.724	0.449
610319	EEH	Bottom	13.193	0.338	660316	Standard	Bottom	17.857	0.452
630319	EEH	Top	18.391	0.063	660317	Standard	Top	19.945	0
630319	EEH	Top	18.36	0.07	660317	Standard	Top	19.893	0.006
630319	EEH	Bottom	13.158	0.584	660317	Standard	Bottom	18.215	0.412
630319	EEH	Bottom	13.19	0.609	660317	Standard	Bottom	18.207	0.415
630320	EEH	Top	17.915	0.151	670312	Standard	Top	20.138	0.245
630320	EEH	Top	18.326	0.202	670312	Standard	Top	20.304	0.225
630320	EEH	Bottom	13.472	1.801	660312	Standard	Bottom	17.432	1.942
630320	EEH	Bottom	13.616	1.782	660312	Standard	Bottom	17.244	1.879

Figure 1. FTIR comparison of the EEH and standard hotzone

The mechanisms for the introduction of Oxygen and Carbon into the ingot are well documented.[vi] During the growth of the ingot the silicon melt is in constant contact with a quartz crucible. The resultant reaction enriches the melt with Oxygen, which is incorporated into the growing crystal. Similarly, Carbon is abundant in the hotzone. It is the primary constituent of the graphite components that make up the EEH. At the high temperatures the machines operate CO and CO_2 are readily produced and can be incorporated in the melt. However, the largest source of Carbon originates from the starting polycrystalline materials. In the growth of solar products, Carbon contents vary greatly because a great portion of the starting materials are recycled materials and are not characterized. As a result, the Carbon content in the ingot can vary.

A statistical review of the data shows the Carbon distribution in an EEH and Standard assemblies are similar. The disturbing information is that one sample from the EEH and one from a standard assembly each tested high in Carbon, > 1 ppma. While there is not enough information to determine the cause of the high Carbon content, the initial amounts of Carbon in the top of the both ingots would indicate a high level of Carbon in the starting material. However, the age of hotzones, cleanliness of the grower, and grower setup may significantly affect the Carbon readings. For the purposes of this investigation it suffices to say that the two assemblies performed comparably.

The data shows a significant reduction in the Oxygen content of ingots grown with the EEH despite operating at 70% lower Argon flow rates. The stable thermal conditions in the growth process may result in lower dissolution rates for the crucible. The data also shows a pronounced difference in the effective segregation coefficient as a result of the faster pull speeds and change in interface shape. Additionally, the radial Oxygen variation was higher in the top of EEH ingots but was negligible in the bottom of ingots.

2. Solar Cell Characterization

For the solar cell characterization effort, twenty ingots were selected. Ten were grown on the EEH system while the other ten grown in a standard assembly. Ingots were of comparable lengths, diameters, starting materials, and grown under normal operating conditions. The ingots were sliced into wafers where several wafers from the center region of each ingot were extracted. The wafers were scribed and processed into groups to minimize variations in cell processes.

A one way ANOVA analysis of the data (Figures 2 - 5) indicates statistically significant differences in all of the electrical characteristics studied, including Isc, Voc, FF, and Ivr.[vii] Of possible significance is the non-constant variance of the two samples. Essentially, the EEH grower created more consistent ingots, as evidenced by the individual standard deviations shown in the ANOVA's. Figures 6 and 7 graphically demonstrate the differences between the two populations. While the absolute difference in Isc, Voc, and FF was small, the difference in Ivr is 0.2 Amps. Therefore, the better Voc and Isc values for the energy efficient hotzones indicate the growth method is capable of growing ingots of improved quality for solar cell applications.

One-way Analysis of Variance for Isc

```
              DF        SS        MS        F        P
         1   0.95205   0.95205   226.91    0.000
Error      846   3.54959   0.00420
Total      847   4.50164

                                  Individual 95% CIs For Mean
                                  Based on Pooled StDev
Level       N      Mean     StDev  -+---------+---------+---------+-----
EEH       442    4.5232    0.0410                              (-*--)
Std       406    4.4561    0.0833   (-*--)
                                  -+---------+---------+---------+-----
Pooled StDev =   0.0648           4.450     4.475     4.500     4.525
```

Figure 2. Comparison of Isc performance in an EEH and standard assembly.

One-way Analysis of Variance for Voc

```
           DF        SS        MS        F        P
            1 0.0033633 0.0033633   253.12    0.000
Error      846 0.0112412 0.0000133
Total      847 0.0146046

                                    Individual 95% CIs For Mean
                                    Based on Pooled StDev
Level       N      Mean     StDev  -----+---------+---------+---------+-
EEH       442   0.59610   0.00141                              (-*-)
Std       406   0.59211   0.00506  (-*--)
                                    -----+---------+---------+---------+-
Pooled StDev =  0.00365               0.5925    0.5940    0.5955    0.5970
```

Figure 3. Analysis of Voc for cells from EEH and standard assemblies.

One-way Analysis of Variance for FF

```
           DF        SS        MS        F        P
            1    798.47    798.47   154.92    0.000
Error     846   4360.32      5.15
Total     847   5158.79

                                 Individual 95% CIs For Mean
                                 Based on Pooled StDev
Level       N      Mean     StDev  --------+---------+---------+--------
EEH       442    75.806     1.931                              (--*--)
Std       406    73.864     2.589  (--*--)
                                 --------+---------+---------+--------
Pooled StDev =    2.270              74.20     74.90     75.60
```

Figure 4. FF analysis for cells grown in EEH and standard assemblies.

One-way Analysis of Variance for Ivr

```
           DF        SS        MS        F        P
            1    9.6060    9.6060   399.25    0.000
Error     846   20.3549    0.0241
Total     847   29.9609

                                 Individual 95% CIs For Mean
                                 Based on Pooled StDev
Level       N      Mean     StDev  ----------+---------+---------+------
EEH       442    4.2195    0.1289                               (-*-)
Std       406    4.0064    0.1793  (-*--)
                                 ----------+---------+---------+------
Pooled StDev =   0.1551                4.060     4.130     4.200
```

Figure 5. Ivr analysis of ingots grown in EEH and standard hotzone assemblies.

Conclusion

Energy, Argon, and other waste products have been significantly reduced using an energy efficient hotzone. Benefits in the Czochralski growth process include higher productivity, higher yields, and lower cost silicon ingot. Ingot characteristics showed consistent carbon and lower oxygen content in the ingots grown from the EEH. Solar cells manufactured from these ingots demonstrated better performance on all characteristics measured.

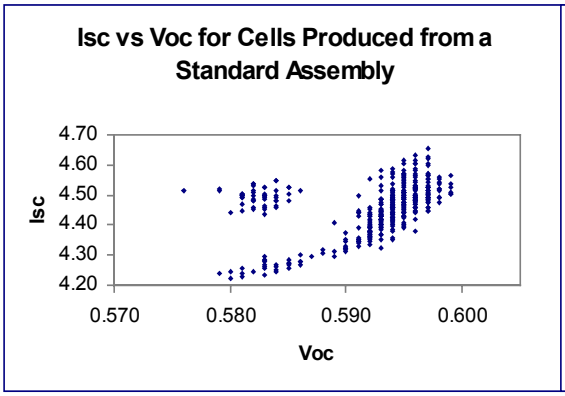

Figure 6. Isc vs Voc for cells grown in standard assemblies.

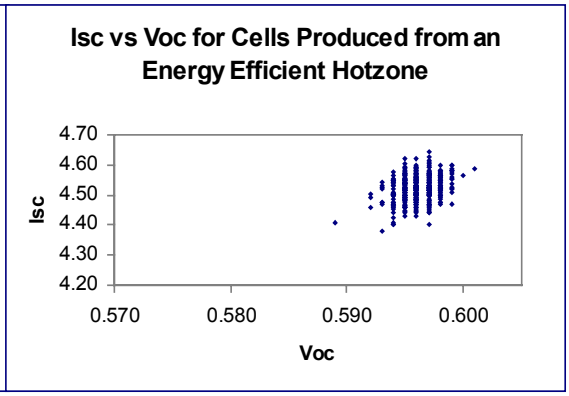

Figure 7. Isc vs Voc for cells grown in energy efficient assemblies.

Acknowledgment

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Scanning Room-Temperature Photoluminescence in Polycrystalline Silicon

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Abstract. Photoluminescence (PL) mapping was performed on EFG wafers at room temperature. Two PL bands are observed: (1) band-to-band transitions with a maximum at 1.09eV, and (2) deep "defect" luminescence at ~0.8eV. PL mapping of 10 cm x 10 cm wafers and solar cells revealed a high degree of inhomogeneity in intensities from both bands. We have also observed that the intensity of the 0.8 eV band is strongest in low quality regions, where the band-to-band PL and minority carrier lifetime are suppressed. Low-temperature PL revealed a dislocation origin of the 0.8eV luminescence. Advantages of the PL mapping technique for quality control in solar-grade materials are discussed.

Introduction. Polycrystalline silicon (poly-Si) is an attractive low-cost Si-based material for photovoltaics. To achieve high (e.g., 18%) efficiency solar cells, poly-Si wafer processing has to be carefully optimized and thoroughly controlled. In this respect, EFG technology presents a particular challenge for electronic quality specification. EFG wafers exhibit a high degree of inhomogeneity in the starting material as well as in the solar cell. Defects that most limit the efficiency in poly-Si solar cells are localized in areas of wafers with high recombination activity, and persist in the processed material.

We report here a new approach to poly-Si diagnostics using scanning room-temperature photoluminescence (RTPL) spectroscopy. RTPL mapping was previously correlated with the distribution of minority carrier diffusion length (L) to show that bulk recombination centers dominate the intensity of band-to-band emission [1]. Our focus here is on the study of regions of the lowest L in EFG wafers, which exhibit the poorest photovoltaic response even after solar cell processing.

Results. The PL spectrum at room temperature is generally composed of two broad bands, as shown in Figure 1a: (i) band-to-band emission with $h\nu_{max}$=1.09eV, and (ii) a "defect" band with a maximum at 0.78eV, that varies weakly across the wafer. Hereafter we give the assignment of "defect" band to the peak near 0.8eV. In areas with high L, we were unable to detect the 0.8eV PL band. A typical PL spectrum in a high and a low quality region of an EFG wafer is presented in Figure 1a.

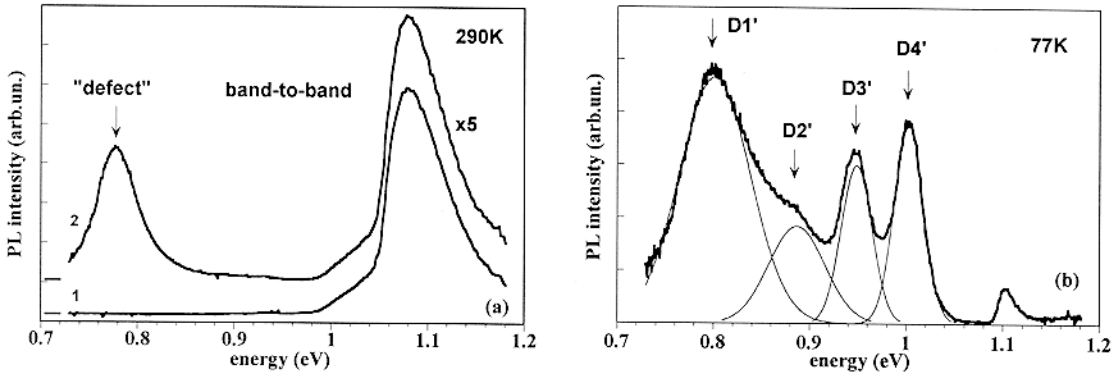

Figure 1. (a) RTPL in high (1) and in low (2) quality regions of an EFG wafer; (b) 77K PL in the low quality area and the deconvoluted spectrum with four Gaussian sub-bands.

RTPL mapping was performed for both bands. First, we measured the band-to-band intensity (I_{bb}) in a scanning mode and compared this to a mapping of the effective minority carrier lifetime. In Figures 2a and 2b, we present a distribution of both values measured independently over the same poly-Si cast wafer. We see that the low lifetime regions of the wafer (dark contrast) correspond to a noticeably reduced I_{bb} intensity (also dark), while the high quality regions in lifetime and PL (white contrast), also are correlated.

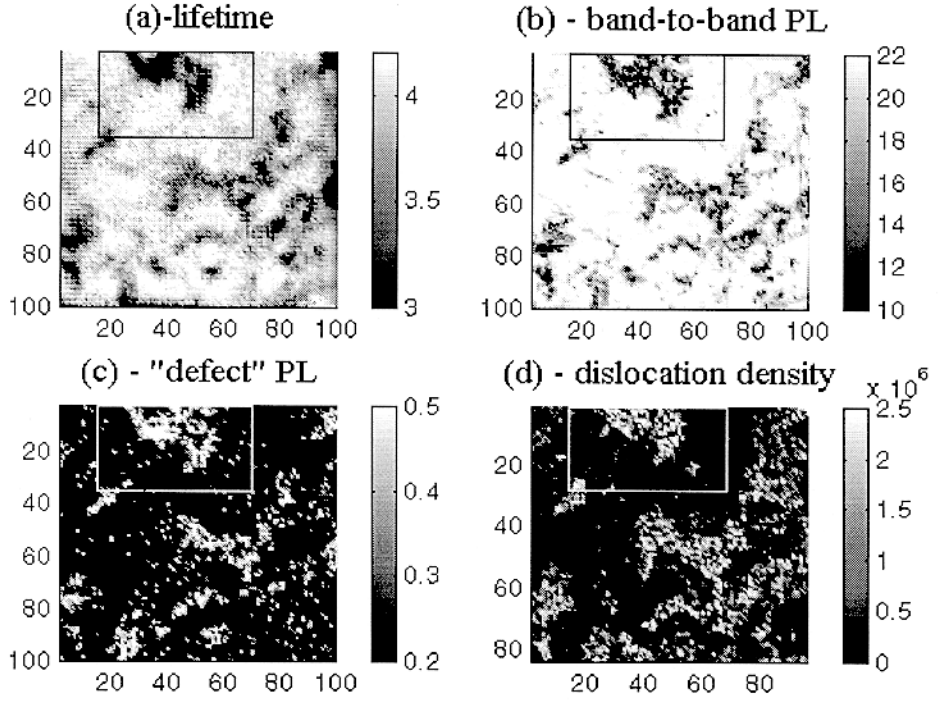

Figure 2. (a) Minority carrier lifetime mapping with laser-microwave reflection, (b) band-to-band PL (290K), (c) defect PL (290K), (d) dislocation density.

This RTPL mapping indicates that the 0.8eV band is strongly localized in low quality regions, and has an inverse relationship to lifetime and band-to-band PL (Fig.2c). This is shown in the framed areas in Fig. 2, which is a low quality region of the wafer. Concurrently with lifetime and PL mapping, we performed measurements of the dislocation density using etch pit density mapping on the same cast wafer. The data presented in Figure 2d document there is a positive correlation in distribution of the dislocation density with the defect PL band. Specifically, the 0.8eV PL band is observed in areas with high dislocation density (1 to 8)E+6 cm^{-2}.

It is significant that the defect PL peaks persist in solar cells. This is illustrated in Figure 3 for a high quality EFG cell with 14.2% efficiency. Thus, these defects are not eliminated completely either with gettering or by hydrogen passivation.

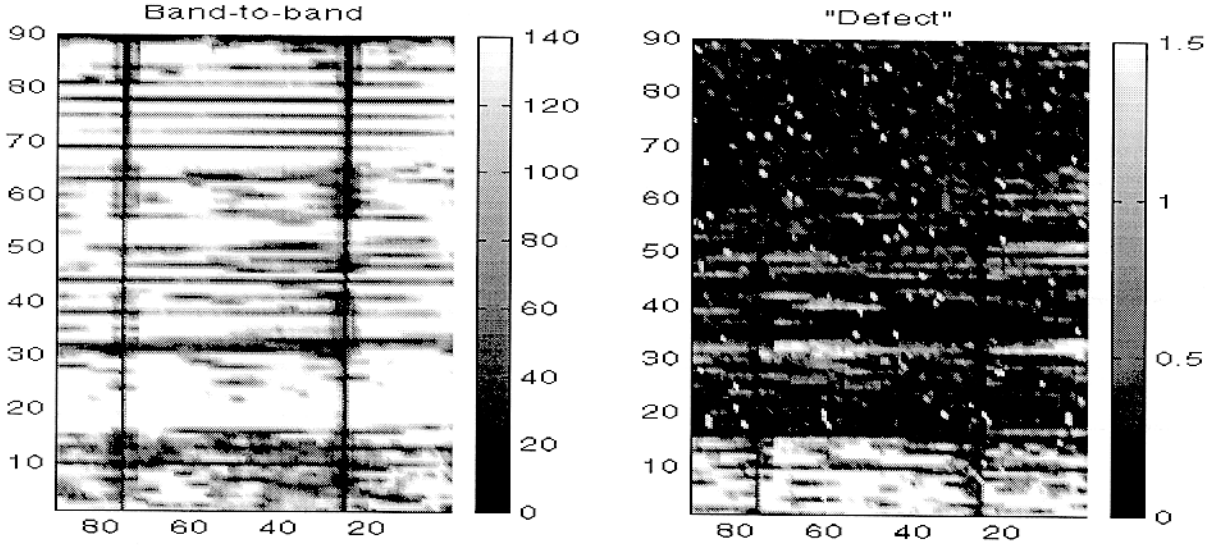

Fig.3 RTPL mapping of band-to-band (left) and defect luminescence (right) on an EFG solar cell with 14.2% efficiency. Mapping area is 90mm x 90 mm, step=1mm. A lower quality region with intensive defect PL occurs in the bottom of the maps.

To investigate the origins of the defect luminescence, we measured PL spectra at temperatures down to 4.2K. The PL spectrum at 77 K of a low quality region in an EFG Si wafer is depicted in Figure 1b (thick line). The band-to-band luminescence is shifted to 1.1eV due to the change in the band gap with temperature. Additionally, rich spectral features are now observed at energies below 1.05eV. Two well-resolved bands have their maxima at 0.95eV and 1.00eV. At lower energies, the PL spectrum shows the maximum at 0.80eV with a barely resolved extra band as a shoulder. When the temperature was increased to 290K, the 0.8eV peak shifted to lower energies, where it can be identified with the previously described 0.8 eV defect band (Fig.1a, curve2). At 4.2K, band-to-band emission is replaced by sharp excitonic lines dominated by the TO-phonon replica of the boron bound exciton at 1.093eV [1]. Aside from an overall increase in PL intensity between 77 and 4.2K, no essential qualitative changes were observed in the PL spectrum

below 1.05eV. For this reason we limited our analyses to 77K luminescence spectroscopy.

We performed a numerical deconvolution of the 77K PL spectrum in the range of 0.72eV to 1.05eV, and found that it can be satisfactory decomposed into four individual Gaussian bands, labeled D1' to D4', (thin lines in Fig.1b), with peak energies as given in Table 1. A set of four PL lines, labeled D1 to D4, with energies very close to those of D1'-D4', was previously observed and studied in detail in plastically deformed Cz-Si, and attributed to dislocation networks [2]. These energies are compared in Table 1. The range

Table 1. Energy positions of dislocation D-lines in Cz-Si and D' bands in poly-Si

	D1	D2	D3	D4
Cz-Si [3]	0.812	0.875	0.934	1.000
	D1'	D2'	D3'	D4'
Poly-Si	0.80	0.89	0.95	1.00

of dislocation densities measured by etch-pit mapping techniques in low quality regions of poly-Si is comparable to that in the plastically deformed Cz-Si. Due to these similarities, we identify the individual bands in poly-Si, D1'- D4' (Fig. 1b and Table 1), with the corresponding dislocation lines D1-D4 of Ref. [2].

Discussion and conclusions. Dislocations with recombination activity are known to limit efficiency in ploy-Si solar cells. We conclude that the defect PL band in these regions originates from these dislocations, and should be identified with the well-known D1/D2 bands in plastically deformed Cz-Si wafers. A unique feature of defect luminescence in poly-Si is that it is observed at room temperature, while the D1/D2 lines in Cz-Si quench rapidly with increasing temperature. This difference may be due to factors such as the presence of additional strain in poly-Si, which could modify recombination parameters of relevant centers, or decoration of dislocations with impurities or precipitates of, e.g., Fe and O.

Scanning RTPL was performed on poly-Si wafers and cells to provide information on low quality regions in the material. Mapping of a new 0.8 eV defect band provides a new diagnostic tool for characterizing wafers and solar cells, and we recommend that it be used to quantitatively assess the recombination activity of dislocations in poly-Si at various steps of cell preparation. The ratio $R=I_{def}/I_{bb}$ is independent of other recombination channels and its mapping represents a convenient parameter for this characterization.

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Chemical State and Stability of Metal Precipitates in Silicon Materials

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ABSTRACT

X-ray absorption spectra are reported for sub-micron iron precipitates in polycrystalline silicon used for solar cells. The x-ray absorption near-edge structure (XANES) from the iron precipitates indicates the chemical state of iron is an oxide or silicate not a silicide or metallic iron. The effect of chemical state is discussed in regards to material improvement.

INTRODUCTION

Polycrystalline and single crystalline silicon are the most economically viable material for terrestrial-based solar cells. Solar cells made from polycrystalline silicon (polysilicon) possess a solar conversion efficiency of 13-15% with low fabrication costs as compared to more expensive, single crystalline silicon solar cells with efficiencies of 17-20%. The lowered efficiencies in polysilicon cells are due to localized regions of high minority carrier recombination. High concentrations of dislocations are generally associated with these regions of poor performance [1-3]. The dislocations have been shown to be decorated with metal precipitates [4]. This result agrees with past work on the recombination activity of dislocations which has shown the dislocation itself does not induce carrier recombination but rather decoration or precipitation of metal impurities at the dislocation prompts the carrier recombination [5-8]. Therefore, metal impurity removal, also known as gettering, from the solar cells would be expected to improve material performance. Phosphorus in-diffusion, which forms the front-side n-p junction of a solar cell, and aluminum sintering, which forms the backside contact, are both known to effectively getter impurities in single crystal silicon used for integrated circuit applications [9-14]. Indeed, the overall material performance of polysilicon improves with phosphorus in-diffusion and aluminum sintering [15, 16]. However, the localized regions with high initial carrier recombination rates do not significantly improve [3, 17, 18], which inhibits polysilicon solar cells from obtaining efficiencies approaching single crystal silicon solar cell efficiencies.

The persistency of poor performance regions indicates the metal impurities are not effectively gettered from these heavily dislocated regions, possibly because of the chemical state of the metal precipitate. A precipitate of one chemical state may be significantly more stable than another due to a difference in the binding energy of a metal atom to the precipitate. The work presented here examines the chemical state of metal impurity precipitates in polysilicon used for solar cells. Specifically, we have compared the x-ray absorption spectra of iron precipitates in polysilicon with spectra from known standards of iron silicides, oxides and silicates using focussed synchrotron-based x-rays. The x-ray absorption near-edge structure (XANES) provides a fingerprint of the chemical state of the iron atoms.

EXPERIMENTAL

In this work we analyzed boron-doped polysilicon grown by a casting technique with an oxygen concentration of 2-3x10^{17} atoms/cm^3 and a carbon concentration of 5-6x10^{17} atoms/cm^3 [19]. We have previously studied this material using LBIC and a synchrotron-based x-ray

fluorescence microprobe (μ-XRF) from which we have correlated low performance regions with metal impurities [4]. Specifically, we detected precipitates of iron, chromium and nickel impurities with radii on the order of 10-100nm and a dispersion of hundreds of microns. Standard lab-based characterization techniques for chemical state identification, such as x-ray photoelectron spectroscopy, x-ray absorption spectroscopy, Auger electron spectroscopy or electron energy loss spectroscopy cannot reliably detect nm-scale precipitates with 100μm-scale dispersion due to either poor sensitivity or a small sampling volume. Prior to analysis, the surface of the material was cleaned with a VLSI grade piranha (H_2SO_4:H_2O_2) etch and HF dips. For sample analysis, we first utilized the synchrotron-based μ-XRF beamline 10.3.1 at the Advanced Light Source, Lawrence Berkeley National Laboratory to ascertain the elemental distributions of metals. Next, we used x-ray absorption spectromicroscopy (μ-XAS) beamline 10.3.2 at the Advanced Light Source, to determine the chemical state. At both beamlines, x-rays from a synchrotron source are focussed down to a spot size of $1\mu m^2$ using elliptically bent mirrors. The x-ray spot can be rastered over the sample, allowing for a large sampling volume. An important aspect of the μ-XAS beamline is the ability to tune the energy of the impinging x-ray beam with a silicon monochrometer while maintaining beam position. Details of the beamline are given in [20]. The absorption studies were performed in fluorescence mode using the Fe Kα signal as a measure of x-ray absorption. Powder standards of FeSi, $FeSi_2$ and Fe_2O_3 as well as a Fe foil standard were analyzed with the μ-XAS beamline for comparison of absorption spectra. In order to avoid self-absorption and signal saturation, the mean powder size was < 10μm and the Fe foil was 5 μm thick. XAS detects changes in the excitation of core-level electrons into empty valence band states. These valence band states are sensitive to chemical state changes of the Fe atoms, therefore, XAS is an excellent tool for determination of chemical state.

RESULTS

An iron, nickel and chromium rich region of the material was located with the μ-XRF beamline. This region was relocated at the μ-XAS beamline by using slightly etched grain boundaries on the polysilicon surface as reference marks. The XAS of the Fe K absorption edge in the polysilicon sample is shown in Figure 1, which is the summation of 19 spectral scans. Multiple XAS scans are also shown in Figure 1 for Fe, FeSi and $FeSi_2$ standards. Fe silicides would be expected to form in this material since silicide formation temperatures are in the same range as crystal growth temperatures and processing temperatures. We observe little similarity between the absorption spectra, indicating the Fe in the polysilicon is not Fe, FeSi nor $FeSi_2$. This is unexpected considering the matrix is silicon.

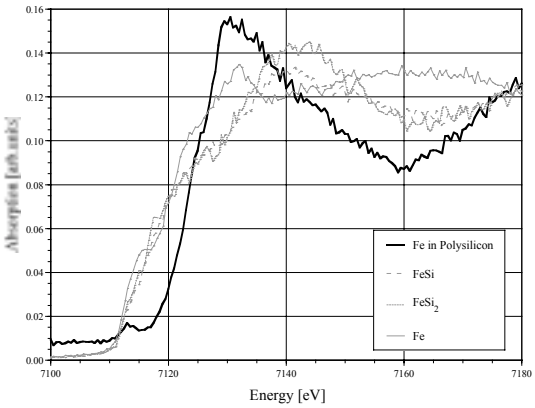

Figure 1: X-ray absorption spectra from Fe in polysilicon, FeSi, $FeSi_2$ and metallic Fe. Note the disparity in edge position and spectra shape.

The shift of the absorption edge and the appearance of the pre-edge structure for the spectra of Fe in the polysilicon suggest the Fe has been elevated to a higher valence state, i.e. the Fe atoms have relinquished electrons to another element in the compound via ionic bonding.

Charge exchange is common for metal oxides and metal silicates. Additionally, past works have indicated that Fe may complex with oxygen in silicon, in turn decreasing the formation energy of oxygen precipitates [21] and oxygen may hinder gettering of metals from silicon [1, 22, 23].

With these possibilities in mind, we analyzed a standard powder of α-Fe_2O_3 with the μ-XAS beamline for comparison to the Fe in the polysilicon. Results are shown in Figure 2 along with spectra of Fe_3O_4 and Fe_2SiO_4 taken previously by Farrel Lytle. We observe some similarity between the absorption spectra of the metal oxides and silicates with the Fe in polysilicon. In particular, the pre-edge structure is remarkably similar between all compounds. Furthermore, the absorption edge of Fe in polysilicon falls between α-Fe_2O_3 and Fe_2SiO_4 and almost on top of the edge of Fe_3O_4. Considering Fe in α-Fe_2O_3 is in a +3 valence state, Fe_2SiO_4 is in a +2 charge state and Fe_3O_4 is a mixed charge state (+2 to +3), the Fe in polysilicon is a mix of +2 and +3 charge states. However, the difference in post-edge absorption spectra between Fe_3O_4 and the Fe in polysilicon indicates the Fe in polysilicon is not completely Fe_3O_4. From these comparisons, one may suggest the Fe in polysilicon is in a mixed state of Fe_3O_4 and α-Fe_2O_3. Further studies of standard powders will be performed along with theoretical calculations to determine the exact chemical state of the Fe in polysilicon.

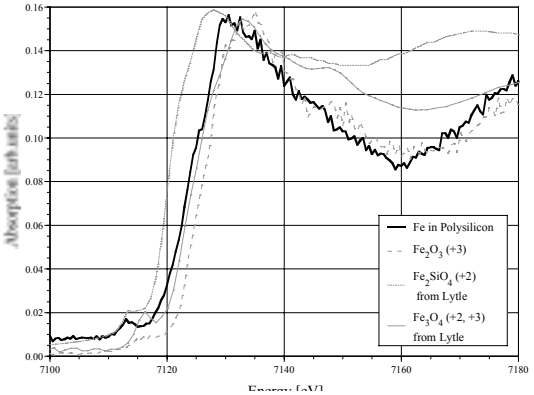

Figure 2: X-ray absorption spectra from Fe in polysilicon, Fe2O3, Fe2SiO4 and Fe3O4. Note the similarity in absorption structure.

DISCUSSION AND CONCLUSIONS

With the iron in an oxide or silicate state, the ability to remove the iron from the material is greatly hindered by to the high binding energy of iron to oxides and silicates relative to iron silicides. Table I lists the standard molar enthalpy and Gibb's free energy of formation for iron silicides, oxides and silicates at 298K. The data has not been corrected for compound formation within a silicon matrix, however, these numbers provide a relative indication. From the data it is seen that thermodynamic formation energies of iron oxides and silicate is significantly higher than iron silicides, thus, the binding energy of the iron atom to an oxide or silicate precipitate is higher than to a silicide precipitate. With a higher binding energy, the solubility of Fe in the presence of an oxide or silicate precipitate will be low, compared to the presence of a silicide precipitate. Since dissolution is a flux-limited process, this lower solubility decreases the dissolution rate.

Table I: Enthalpy and Gibb's free energies of formation for Fe related compounds.

	ΔH_f^o (kJ/mol)	ΔG_f^o (kJ/mol)
FeSi [24]	-39.3	-
$FeSi_2$ [24]	-30.6	-
1/2 Fe_2O_3 [25]	-412.1	-371.1
1/3 Fe_3O_4 [25]	-372.8	-338.5
1/2 Fe_2SiO_4 [25]	-740	-689.5

Another potential impact from these results is that Fe in an oxide or silicate state may be more or less recombination active than Fe in a silicide or elemental state. In this study we did observe high carrier recombination activity with previous LBIC measurements. However, the

presence of Ni and Cr does not allow us to draw conclusions on the affect of chemical state on recombination activity. Further work in this area should be pursued.

Based on our results we can conclude that Fe in polysilicon solar cells can be in the form of an oxide or a silicate. This is contrary to common thought, where a Fe silicide would be expected to form. With the state of iron being an oxide or silicate, the rate of impurity removal is significantly reduced due to a significantly higher binding energy of Fe atoms to oxides or silicates as compared to silicides. These results provide insight into poor performance regions in polycrystalline silicon solar cells.

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Origins of carrier trapping centers in *p*-type multicrystalline silicon

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Carrier trapping effects in multicrystalline silicon wafers are investigated by measuring the dependence of their photoconductance on carrier injection level and by fitting a theoretical model to the data. The main information thus obtained is the density of trapping centres, which can vary significantly for different cast multicrystalline silicon ingots. Typically, the density of trapping centers also changes for wafers from different positions within an ingot, and we have found a correlation between the concentrations of trapping centers and dislocations in the mc-Si wafers. Additional experiments based on cross-contaminating ultra pure single-crystal silicon wafers with multicrystalline silicon specimens revealed that some of the trapping-causing defects are mobile at high temperatures. The density of those trapping centers in *p*-type float zone wafers of varying resistivities was found to be linearly proportional to the background boron concentration, suggesting that the trapping effects are caused by boron-impurity pairs. Two possible physical origins for the trapping centers in multicrystalline silicon have hence been identified: crystallographic defects (dislocations) and mobile impurities.

1. Introduction

The measurement of the minority carrier lifetime of multicrystalline silicon (mc-Si) has been disconcerting for some time: anomalously high photoconductance values (implying very high apparent lifetimes) are frequently observed, particularly at low carrier densities (see Fig.1). Finding a satisfactory conceptual explanation for this anomalous photoconductance was an important step forward in the understanding of mc-Si. A physical model for carrier trapping effects developed in the mid 50's[1,2] proved to be capable of explaining very well the experimental photoconductance of mc-Si at low injection levels[3]; the puzzle was solved, at least conceptually. The next step is to investigate what are the physical origins of the trapping centers and their practical implications on device performance

We present here the results of several experiments aimed at improving the understanding of trapping centers and learning about their physical origin. A group of experiments use phosphorus-gettered multicrystalline wafers, where the consequences of crystallographic defects should be revealed more clearly. The second type of experiments involve the transferring to crystallographically perfect FZ wafers of the mobile contaminants present in un-gettered mc-Si to elucidate whether they also produce trapping or not.

All lifetime measurements presented in this paper were performed using the quasi-steady-state photoconductance (QSSPC) technique[4]. However, any photoconductance based method, such as transient photoconductance decay (PCD), would be subject to the same trapping phenomena explored here[5]. The QSSPC data analysis was performed with both steady-state and transient terms in the determination of lifetimes, allowing a large range of lifetimes to be measured[6].

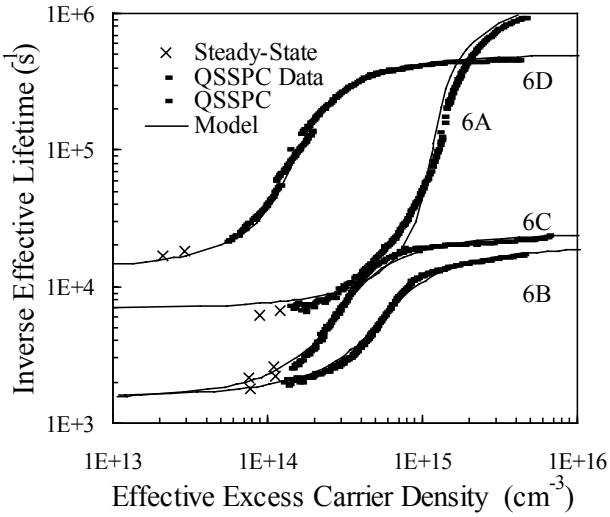


Figure 1. Quasi steady-state photoconductance measurements of wafers from the top (6A), near top (6B), centre (6C) and bottom (6D) of the same mc-Si ingot. The continuous lines represent the theoretical model.

2. Trapping in gettered multicrystalline silicon

Figure 1 shows QSSPC data from four mc-Si wafers from different parts of a p-type multicrystalline solar grade silicon ingot grown by directional solidification at Eurosolare, SpA. Wafers labelled 6A, 6B, 6C and 6D come from the top, near top, centre and bottom of the ingot respectively. The samples were phosphorus gettered, etched, and then given a light phosphorus diffusion and oxidation to passivate the surfaces. The apparent rapid increase in lifetime at lower injection levels is due to minority carrier trapping.

The theoretical model originally developed by Hornbeck and Haynes[1] is, as Figure 1 shows, capable of describing the behaviour of a variety of mc-Si wafers with very different recombination lifetimes and trap densities over a broad range of carrier density levels. By fitting the model to the experimental data, the trap density N_t can be determined. For example, for wafer *6A* the trap density is $N_t = 3\times10^{15}\text{cm}^{-3}$ and the true minority carrier recombination lifetime is 0.7μs. The results in Figure 1 show that the top of the ingot has the largest trap density and the bottom the lowest.

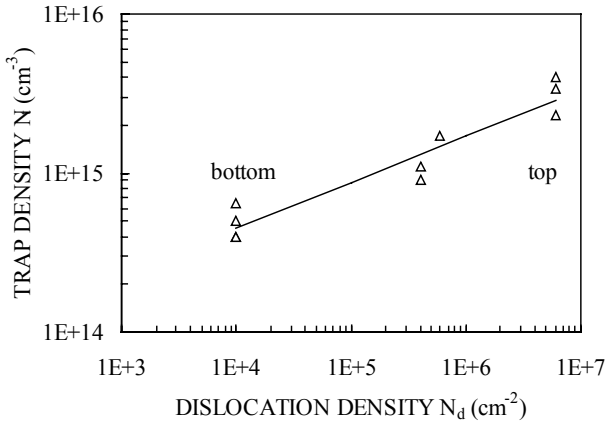


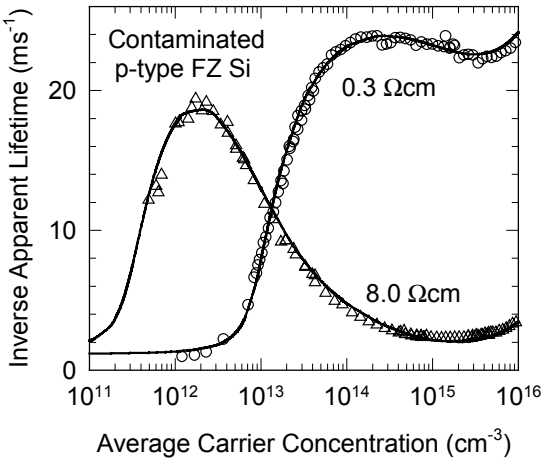
Figure 2. Dislocation density N_d versus trap density N_t for phosphorus gettered wafers from different regions of the same mc-Si ingot. The line of best fit takes the form $N_t = 3.1\times10^{13}(N_d)^{0.29}$.

As an additional characterization of the material, we measured the density of dislocations by counting etch pits under an electron microscope. The dislocation density was found to be highest at the top of the ingot, probably due to high thermal stresses resulting from rapid cooling at the end of the casting process. Figure 2 shows a plot of trap density versus dislocation density for the samples in Figure 1, plus data from five additional samples from the same ingot. Figure 2 reveals that a correlation exists between the densities of trapping centres and dislocations for this particular mc-Si ingot.

3. Transferring some trapping centers to single crystal silicon

Mobile impurities in mc-Si can be transferred to nearby high quality, single crystal, float zone (FZ) wafers by effusion at high temperature[7]. Such cross-contamination produces a reduction in the lifetimes of the FZ wafers that is proportional to the initial contamination level of the mc-Si wafers. We have recently noticed that these contaminated FZ wafers also exhibit considerable trapping effects, which is a clear indication that mobile impurities can also be responsible for the creation of trapping centers.

An important advantage of the cross-contamination experiments is that they allow the study of trapping and recombination centers in a material that is practically free of crystallographic defects. They also provide a way of examining the possible correlation between the background doping and



the trapping effects by contaminating FZ wafers of different resistivities. This may not be possible with the mc-Si wafers, which come only in a narrow dopant density range, and in which a similar crystal quality cannot be guaranteed.

Figure 3: Inverse apparent lifetime versus average carrier concentration for 0.3 and 8.0 Ωcm cross-contaminated FZ Si wafers. The open symbols are experimental data and the solid lines represent the modelling. Both curves show the emitter term dominating at high injection, SRH behaviour at moderate to low injection, and trapping at the lowest injection levels.

Cross-contamination of *p*-type FZ Si wafers was achieved by an 840°C light phosphorus diffusion followed by a thin thermal oxide growth at 900°C, for a

total of 60 minutes. The high temperature allows the effusion of impurities from the mc-Si to the FZ Si (separated by about 5mm), whilst the diffusion and oxidation passivate the surfaces for lifetime measurements. After cross-contamination, the trap density N_t in the FZ wafers was found to be around 100 times less than in the mc-Si wafers. Consequently we used mc-Si samples with a high trap density to ensure measurable trapping effects in the FZ wafers. The mc-Si samples used in this study were adjacent wafers taken from the top of a 1 Ωcm *p-type* cast mc-Si solar grade ingot. These mc-Si wafers were similar to sample 6A of Figure 1, although they had not been gettered and presented a slightly greater trap density of around 7×10^{15}cm^{-3}.

Figure 3 shows lifetime measurements of two such cross-contaminated FZ samples of 0.3 and 8 Ωcm resistivity. At higher injection levels the effective lifetimes reflect the bulk lifetimes, however at around 1×10^{14}cm^{-3} and 2×10^{12}cm^{-3} for the 0.3 and 8 Ωcm samples respectively, trapping effects begin to dominate. The contaminating species are most likely transition metals such as Fe and Cr (known to exist in significant amounts in these mc-Si wafers). Their presence in the FZ material has two effects on lifetime – firstly the introduction of trapping centers and the associated apparent increase in lifetime at low injection level; secondly, the introduction of recombination centres and the resulting Shockley Read Hall (SRH) dependence of lifetime on injection level[8,2]. The presence of the emitter caused by the phosphorus diffusion in these samples also impacts on the lifetime at the highest injection levels [9].

As well as experimental data, Fig 3 also shows fit lines for the trapping model. However, the fitting procedure is more complex than that used in Fig 1, where the recombination lifetime τ_r was assumed constant. The curves in Fig 3 clearly show an injection level dependence at carrier densities higher than the region where traps dominate. This dependence is caused by the SRH behaviour of the impurities, and also by the emitter as mentioned above. As a result, for *p*-type Si, τ_r must be modeled by[2,8]:

$$\frac{1}{\tau_r} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{emit}}.$$

where

$$\frac{1}{\tau_{SRH}} = \frac{N_A + \Delta n}{\tau_{p0}(n_1 + \Delta n) + \tau_{n0}(N_A + p_1 + \Delta n)}$$

$$\frac{1}{\tau_{emit.}} = \frac{2J_0(N_A + \Delta n)}{qn_i^2 W}.$$

Here, Δn is the excess carrier density, N_A the dopant density, n_1 and p_1 the equilibrium densities of electrons and holes respectively when the Fermi energy coincides with the flaw energy, and τ_{n0} and τ_{p0} the capture time constants for electrons and holes[2]. J_0 is the emitter saturation current density, which characterises recombination in the diffused regions ($\approx5\times10^{-14}$Acm^{-2}), and n_i and W the intrinsic carrier concentration and sample thickness respectively.

To obtain an accurate fit to the experimental data in Fig 3, it was necessary to model τ_r with two SRH centers. Having two centers means that there are six fit parameters for the SRH contribution to τ_r, resulting in a large number of possible sets of parameters that provide reasonable agreement with the experimental data. As a consequence, it is not possible to uniquely determine τ_{n0} and τ_{p0} or the energy level of the recombination centers. However, for any set of parameters that provide a good fit, the corresponding trap density N_t is restricted to a narrow range. Hence we are in a position to accurately specify N_t, even if we can infer little about the detailed properties of the SRH centers.

4. Dependence of the density of trapping centers on boron concentration

The trap density was determined for a range of contaminated FZ wafers of resistivity from 0.3 to 1000 Ωcm. For the 1000 Ωcm case the trap density was so small ($<1\times10^{11}$cm^{-3}) as to be unmeasurable. The results for the other wafers are shown in Fig 4 as a function of boron concentration in the FZ substrate. There is a clear linear relationship between these variables, implying that the traps are related to a boron-impurity pair. The impurity, or impurities have clearly come from the mc-Si wafers, and hence must be highly mobile in silicon at high temperatures in order to effuse out of them and diffuse into the bulk of the FZ wafers.

The cross-contamination of FZ wafers with impurities from mc-Si wafers leads to associate some of the trapping centers present in mc-Si with highly mobile contaminants. In the contaminated *p*-type FZ wafers, the density of such trapping centers is linearly related to the boron concentration, implicating the formation of boron-impurity pairs. A similar correlation is to be expected for mc-Si wafers with various boron doping levels.

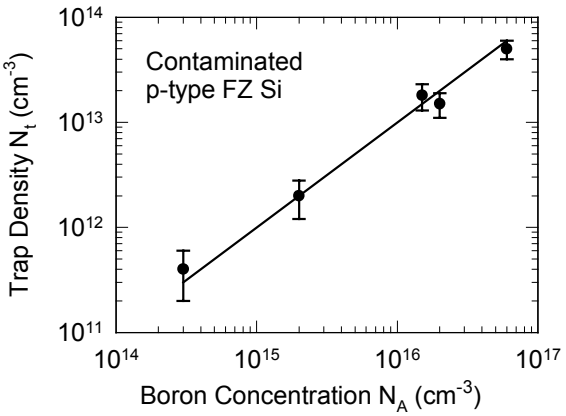


Figure 4: Density of trapping centers N_t vs. boron concentration N_A for cross-contaminated *p*-type FZ wafers of different resistivities. The solid line represents the linear fit $N_t = 0.001 N_A$.

5. Discussion

There are two pieces of evidence, on one hand the trap density in *gettered* mc-Si wafers is related to the dislocation density in the material; on the other hand, it is also correlated to boron-impurity pairs in *un-gettered* mc-Si wafers. The overall effect of trapping in common, un-gettered mc-Si is logically attributable to a combination of both causes, although their specific contributions can vary from sample to sample and can not be discerned yet. It is also reasonable to expect that trapping centers related to dislocations (and possibly other crystallographic defects) dominate the trapping behaviour of gettered mc-Si. Nevertheless, the possible role of residual metal contaminants cannot be completely ruled out, since they may be precipitated at dislocation sites and be impervious to the gettering treatment. In this latter scenario, even if the dislocations may not be the direct cause of trapping they would still be correlated to it as vehicles for the anchorage of the impurities.

In conclusion, two possible physical origins for the trapping centers in multicrystalline silicon have been identified: crystallographic defects (dislocations) and boron-impurity pairs produced by mobile contaminants. Experimental evidence indicates that the trapping effects per se do not affect detrimentally solar cell steady-state operation[10]. It remains to be seen whether they can be useful for material diagnostic and optimization of mc-Si growth and processing techniques.

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Appendix

The application of Hornbeck-Haynes model to quasi-steady-state photoconductance measurements is summarized by the following expressions.

Charge neutrality demands that $\Delta p = \Delta n + n_t$, where n_t is the trapped electron concentration. The excess conductivity $\Delta\sigma$ (due to untrapped carriers) is:

$$\Delta\sigma = q\Delta n(\mu_n + \mu_p) + qn_t\mu_p$$

$$\Delta n = g_e\tau_r$$

$$n_t = \frac{N_t\Delta n}{\Delta n + N_t\tau_t/\tau_g}.$$

where μ_n and μ_p are the electron and hole mobilities, g_e is the photo-generation rate, N_t the density of trapping centers and τ_t and τ_g the trapping and escape times. The effective carrier lifetime τ_{eff} is:

$$\tau_{eff} = \frac{\Delta\sigma}{g_e\ (\mu_n + \mu_p)}.$$

Note that, for a given photogeneration rate, the density of free electrons Δn remains equal to that when no traps are present and that the main consequence of trapping is an increased number of excess holes, resulting in an enhanced photoconductance.

WHY DO COPPER PRECIPITATES REDUCE CARRIER LIFETIMES?

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Abstract

Cu-related defects in Si are studied at the *ab-initio* Hartree-Fock level in clusters containing up to 100 Si atoms. Interstitial Cu, substitutional Cu, and one through five Cu's trapped at an internal void modeled by the ring-hexavacancy are studied. The configurations, electronic structures, and binding energies are calculated. The origin of the electrical activity of copper precipitates is discussed.

Copper is a common impurity in silicon.[1-4] Interstitial copper is believed to exist as the Cu_i^+ ion. It is the fastest-diffusing impurity in Si,[5] with $D = (3.0 \pm 0.3) \times 10^{-4} \cdot \exp -(0.18 \pm 0.01) eV/k_B T\, cm^2/s$. The activation energy is close to the 0.24 eV predicted by *ab-initio* Hartree-Fock (HF) calculations[6] for the diffusion of Cu_i^+ along the interstitial tetrahedral–hexagonal–tetrahedral (T-H-T) path. It has been assumed that the reason for this low value is that Cu^+ has an ionic radius of only 0.75Å and the closed-shell [Ar]$3d^{10}4sp^0$ configuration. It should therefore behave like a small ball which does not interact covalently with the host crystal.

Yet, copper has a tendency to precipitate at dislocations,[1,4,7] grain boundaries,[8] nanocavities,[9-11] radiation-damaged regions,[12,13] stacking faults,[14] etc. It forms star-shaped etch pits, and platelets in {111} planes.[4] Such precipitates reduce carrier lifetimes.[15,16] A range of gap levels observed by DLTS have been assigned to copper precipitates.[3,4] Thus, even though isolated copper is thought to exhibit little electrical or chemical activity, its interactions with defects result in the appearance of deep levels in the gap.

In this work,[17] the trapping of interstitial copper at a model internal void, the ring-hexavacancy (V_6),[18] is studied at the Hartree-Fock level. The geometries are gradient-optimized with no symmetry assumptions using the method of PRDDO,[19] and the geometries are used as inputs for *ab-initio* HF calculations[20] with split-valence polarized basis sets. The host crystal is represented by clusters containing up to 100 Si atoms.

The lowest-energy configuration of Cu_i^+ in Si is almost exactly at the T site, off by less than 0.1Å toward one of its four Si NNs. The energy spectrum shows no state in the gap, but for a very shallow level near the conduction band.

It *costs* 1.67 eV to insert the free Cu^+ ion into the T site in Si. This value matches the measured heat of solution from the silicide, 1.7 eV.[1,10] The electronic configuration of Cu_i^+ is *not* the free ion's $3d^{10}4sp^0$. Instead, Cu_i^+ promotes several electrons from the $3d$ into the $4sp$ shell (Fig. 1). This allows it to interact covalently with impurities and defects, and to hybridize in a variety of ways.

The model internal void considered here for Cu precipitation is V_6, a defect predicted[18] to be stable and electrically inactive. It consists of a hexagonal ring missing from the crystal. V_6 is an ellipsoidal void of diameter 7.8Å, thickness 4.4Å, and trigonal symmetry.

In order to avoid the build-up of positive charge as Cu^+ precipitates in the void, it was assumed that $\{Cu_{n-1}, V_6\}^+$ traps an electron before the next copper binds to the defect. Such a process was proposed[21] as the reason why copper precipitates faster in n- than in p-type Si. However, since copper precipitates are also observed in p-type material, electrons must trap at the defect to maintain a small or zero net charge. Only total energy differences involving closed-shell (spin 0) configurations are included.

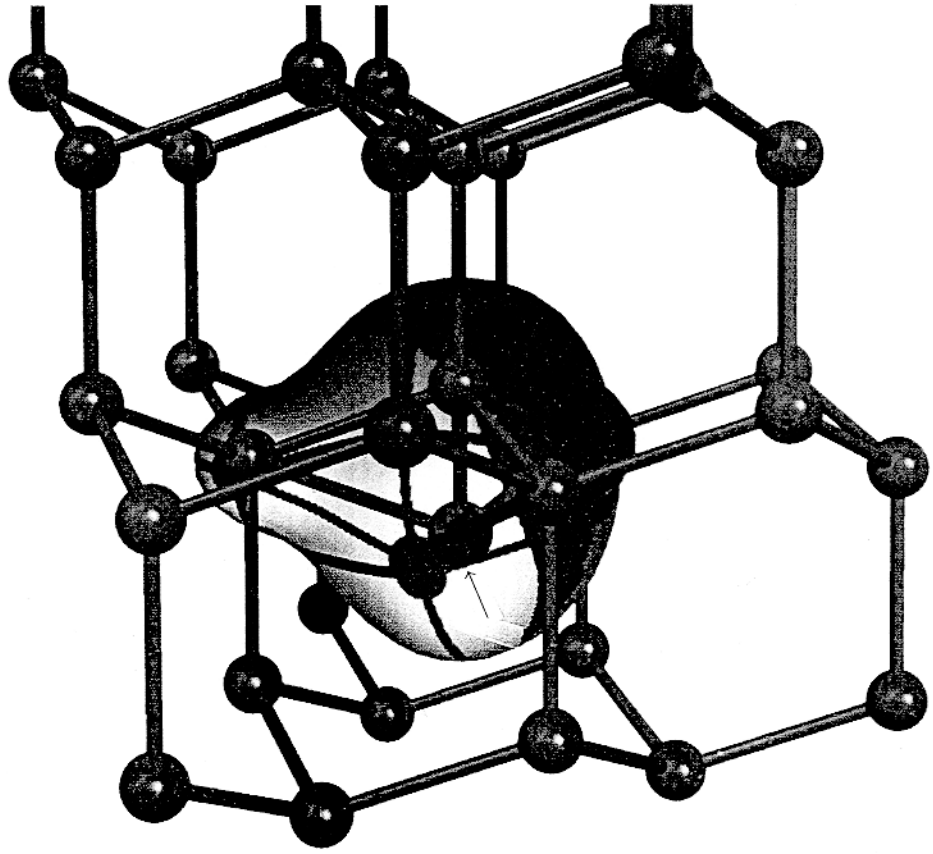

Fig. 1: Electrostatic potential around interstitial Cu (arrow) in Si. The copper ion does not resemble a tiny sphere.

The precipitation of Cu_i^+ at V_6 was handled as follows.

(1) Cu^+ is placed inside V_6, the geometry optimized, and the binding energy ΔE_1 is defined as $Cu_i^+ + V_6 \rightarrow \{Cu_1, V_6\}^+ + \Delta E_1 = 3.36$ eV. It is then assumed that $\{Cu_1, V_6\}^+$ captures an electron, then traps Cu_i^+. This defect traps a second electron and the geometry of $\{Cu_2, V_6\}^0$ is optimized. This defect, a closed shell, is the trap for the next Cu_i^+.

(2) Cu^+ is placed inside $\{Cu_2, V_6\}^0$, the geometry optimized, and the binding energy ΔE_3 is defined as $Cu_i^+ + \{Cu_2, V_6\}^0 \rightarrow \{Cu_3, V_6\}^+ + \Delta E_3 = 4.94$ eV. It is then assumed that $\{Cu_3, V_6\}^+$ captures an electron, then traps Cu_i^+. This defect traps a second electron and the geometry of $\{Cu_4, V_6\}^0$ is optimized. This defect, a closed shell, is the trap for the next Cu_i^+.

(3) Cu^+ is placed inside $\{Cu_4, V_6\}^0$, the geometry optimized, and the binding energy ΔE_5 is defined as $Cu_i^+ + \{Cu_4, V_6\}^0 \rightarrow \{Cu_5, V_6\}^+ + \Delta E_5 = 2.01$ eV. Note that this value coincides with the measured[10] dissociation energy of copper from Cu-saturated internal voids, 2.2 ± 0.2 eV.

In $\{Cu_1, V_6\}$, copper binds to four Si atoms on the inner surface of the void. The Cu–Si distances range from 2.38 to 2.68Å, and the degrees of bonding[22] from 0.6 to 0.4. For a perfect 2-electron covalent bond, this number is 1.0.

In $\{Cu_2, V_6\}$, the Cu's are as far from each other as possible (4.55Å), at opposite inner surfaces of V_6. The Cu–Si bond lengths vary from 2.38 to 2.62Å, and the degrees of bonding from 0.7 to 0.5.

In $\{Cu_3, V_6\}$, the Cu's form an almost perfect isosceles triangle in the plane of V_6. The Cu–Cu distances are 2.75, 2.77, and 4.08Å, respectively. One Cu is bound to the two other Cu's, but the overlap is very small (degree of bonding ≤ 0.2). This Cu is mostly bound to only two Si atoms, at 2.28 and 2.33Å, with degrees of bonding of 0.7 and 0.8. The other two Cu's form four Cu–Si bonds, with bond lengths varying from 2.38 to 2.71Å and degrees of bonding from 0.6 to 0.4.

The copper atoms in $\{Cu_4, V_6\}$ form a perfect rectangle of width 2.36Å and length 3.67Å in the plane of V_6. There are two weak Cu–Cu bonds (degree of bonding 0.4), that is each of the four Cu's is bound to one Cu and four Si atoms. These bonds are similar to those described above.

$\{Cu_5, V_6\}$ is a slightly distorted version of $\{Cu_4, V_6\}$, with the fifth Cu forming the tip of a pyramid with a rectangular base. The tip is on the trigonal axis of V_6. The fifth Cu is eight-fold coordinated (!) but the degrees of bonding are quite small (0.2 to 0.4). The other Cu's are as in $\{Cu_4, V_6\}$.

The following trends for copper precipitation at an internal void are apparent.
(1) The Cu's trap on the inner surface of the void and remain as far apart as possible from each other.
(2) Cu–Si bonding is preferred over Cu–Cu bonding. If there is enough space, each Cu binds to different Si atoms. As the void fills up, some Cu–Cu overlap becomes unavoidable, and a few Si atoms bind to two Cu atoms.
(3) Cu forms four weak Cu–Si covalent bonds. The degrees of bonding vary from 0.4 to 0.8.
(4) The sum of the degrees of bonding associated with each Cu lies in the narrow range 2.3 to 2.6 for all the complexes studied here. Thus, the *total* number of electrons participating in the covalent bonding of each Cu is very near five.
(5) The binding energies of Cu to an internal void vary with the number of copper impurities in the void. For a saturated void, it is $2\,eV$.
(6) The maximum strength of each of the Cu–Si bonds is 0.9 eV. This estimate is obtained by dividing the binding energy of Cu to $\{Cu_n, V_6\}$ (relative to $\{Cu_{n-1}, V_6\} + Cu_i^+$) by the number of Cu–Si bonds involved. Since each copper forms four inequivalent Cu–Si bonds with degrees of bonding ranging from 0.4 to 0.8, some of the bonds are necessarily weaker than 0.9 eV.
(7) Many energy levels associated with the bonding/antibonding orbitals of the weak Cu–Si (and Cu–Cu) bonds are in the gap. Fig. 2 shows that the wavefunction associated with the highest-occupied level is localized on the Cu–Si bonds. This implies that the electrical activity is caused by the energy levels associated with the weak Cu–Si and Cu–Cu bonds.
(8) The binding energy of a single hydrogen to a vacancy[23] is of the order of 3 eV and results from the formation of one strong Si–H bond. Thus, if hydrogen is present, it should easily displace Cu from internal voids, since replacing even the strongest Cu–Si bond by a Si–H bond results in a gain of the order of 2 eV. Such an effect has indeed been reported.[10]

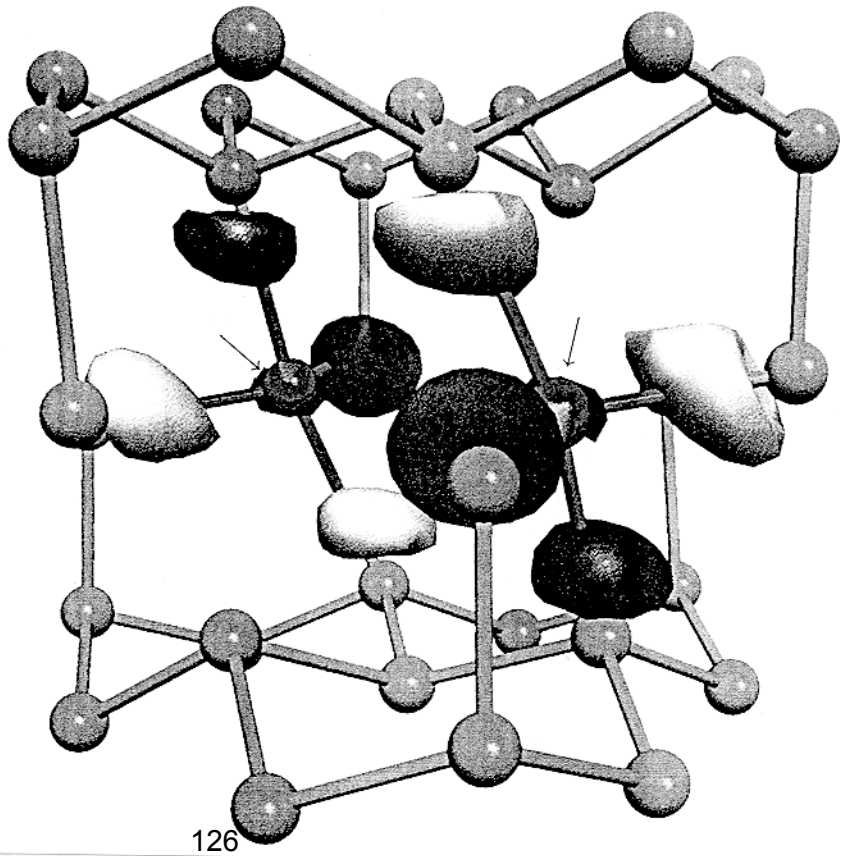

Fig. 2: Wavefunction associated with the highest-occupied deep-level in the gap for $\{Cu_2, V_6\}$. The Cu atoms are shown by arrows.

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THE TRAPPING OF HYDROGEN AT NATIVE DEFECTS

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Abstract

The interactions between hydrogen and intrinsic defects in silicon are studied using ab-initio molecular dynamics simulations in periodic supercells and Hartree-Fock in saturated clusters. The complexes formed by one self-interstitial and one to four H's and the trapping of a single H at various vacancy aggregates are discussed. The binding energies, structures, and properties of these defects are calculated.

Hydrogen is a common impurity in silicon and other semiconductors. It diffuses rapidly and interacts with a wide range of impurities and native defects. These interactions often involve some degree of covalent bonding between H and Si atoms. The most common consequence is a change in the structure of the defect with which H interacts, a change in the energy spectrum associated with it, and a shift of levels within the gap, from the gap into a band (passivation), or from a band into the gap (activation).[1,2] The thermal stability of most complexes containing H is of the order of a few hundred degrees Celsius. The most stable complexes are usually those involving H and intrinsic defects because of the presence of strong Si–H bonds. The simplest intrinsic defects[3] are the vacancy (V) and the self-interstitial (I), but aggregates of V's and I's are traps for H as well.

The isolated I has never been observed in Si, but several $\{I,H\}$ complexes have been detected by FTIR[4] and predicted by theory.[4-6] Possible structures have been calculated for such complexes.[7-9]

It is now well-established[10] that the V has deep levels in the gap and can be fully passivated by four H atoms trapped in it, with all four Si–H bonds pointing toward the center of the vacancy. The $\{V,H_n\}$ complexes have now all been identified by FTIR.[11] The stretch mode at $2222\,cm^{-1}$ with T_d symmetry has been assigned to both the $\{V,H_4\}$ complex[11] and to the interstitial silane (SiH_4) molecule.[12,13] Recent calculations[9] of vibrational modes found the stretch mode of interstitial SiH_4 to be close to $1800\,cm^{-1}$, far too low to be associated with the observed mode.

V-V interactions lead to the formation of vacancy aggregates V_n. One peculiar such aggregate, the ring-hexavacancy V_6, has been predicted[14] to be particularly stable and, in contrast to the other vacancy aggregates, have no localized (deep) levels in the gap. Thus, while four H's are needed to passivate the monovacancy, V_6 needs no H to be free of deep levels.

In the present work, we study two families of complexes: those of the form $\{I,H_n\}$ with n=1,...,4, including the silane and silyl molecules, and those of the form $\{V_n,H\}$ with n=1,...,6. We are interested in binding energies, equilibrium structures, and changes in the energy spectra of V_n caused by the trapping of a single H.

The configurations are obtained from ab-initio tight-binding molecular-dynamics (MD) simulations[15] in periodic supercells containing 64 and/or 216 Si atoms (not counting the defect). Four k-points in the Brillouin zone were included with the smaller cell but only k=0 in the larger one. At first, a wide range of symmetrically inequivalent initial configurations were thermalized and quenched using the faster but less accurate Harris-functional version of the code. Then, the most stable configurations were used as inputs for slower but more accurate self-consistent calculations. Some of these calculations are still under way. All the MD calculations used a spin-averaged scheme.

Once the most stable structures were identified, approximate ab-initio and ab-initio Hartree-Fock (HF) calculations were performed to obtain molecular-orbital (MO) eigenvalues and chemistry of the

various defects. All the configurations considered are closed-shell ones (spin 0). That is, in the HF calculations, the $\{V_n, H\}$ complexes are assumed to be in the +1 charge state, resulting from the trapping of H_{BC}^{+} by V_n^0.

In agreement with other authors, we find that I^0 is stable in the split-$<110>$ configuration. There are numerous strained Si–Si bonds in the vicinity of the defect, and therefore numerous trapping sites for H. The binding energy ΔE_n of H to the $\{I, H_n\}$ complex, defined from $\{I, H_{n-1}\} + H_{BC} \rightarrow \{I, H_n\} + \Delta E_n$ is 1.45 eV for n=1, 2.61 eV for n=2, 0.42 eV for n=3, and 1.35 eV for n=4 (these are Harris functional energies). Thus, the most stable complex in the series is $\{I, H_2\}$, and the least stable one is $\{I, H_3\}$.

The lowest-energy structure of $\{I, H_1\}$ is a distortion of the split-$<110>$ configuration. I is shifted toward an adjacent T site and H is bound to it. Five Si host atoms are displaced from their perfect lattice sites.

The stable structure of $\{I, H_2\}$ (Fig. 1, left) is the same as that found by other authors.[4,7-9] It resembles a (distorted) split-$<100>$ interstitial with one H bound to each of the two Si atoms. The lowest-lying metastable configuration, 0.40 eV higher in energy, is a puckered bond-centered I with both H's bound to it.[5]

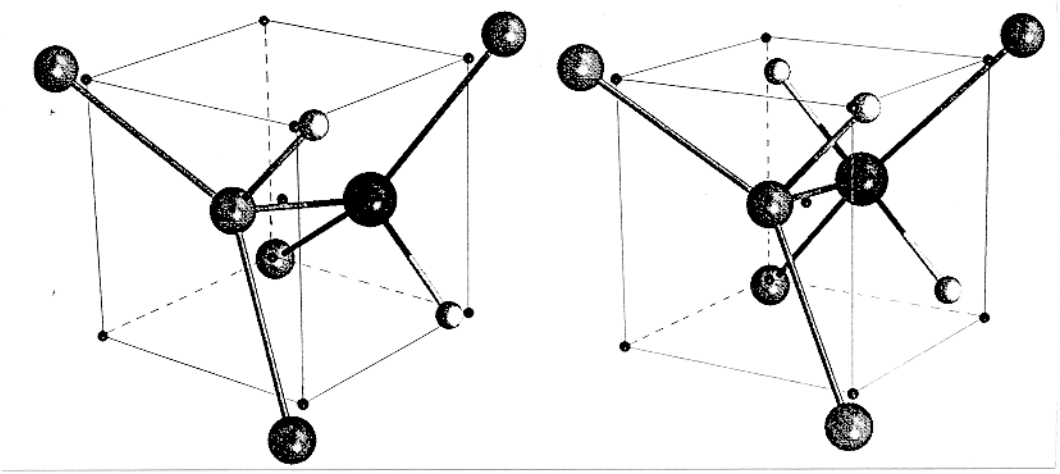

Fig. 1: Structures of the $\{I, H_2\}$ (left) and $\{I, H_3\}$ (right) complexes.

The lowest-energy structure of $\{I, H_3\}$ (Fig. 1, right) is similar to $\{I, H_2\}$ with two H's bound to one Si atom and the third H to the second Si atom. A metastable configuration, only 0.1 eV higher in energy, has the three H atoms bound to three adjacent Si host atoms. The interstitial silyl molecule (SiH_3) with Si very near the T site, is 0.44 eV higher in energy. This is not only higher than two other configurations, but also than $\{I, H_2\}$ plus isolated H_{BC}.

The lowest-energy structure of $\{I, H_4\}$ consists of $\{I, H_2\}$ and two additional H atoms which are bound to a nearest neighbor (NN) and a second NN to I, respectively. The four H's are bound to four different Si atoms. The nearest metastable configuration, 0.2 eV higher in energy, is very similar to $\{I, H_3\}$ (Fig. 1, right) but with two H's bound to each of the two Si atoms. It is likely that the strain associated with this defect can trap additional H atoms, but is it not clear that the simple $\{I, H_n\}$ notation is still appropriate.

Interstitial silane, centered at the T site with the four H's pointing along the four $<111>$ axes, is 2.48 eV higher in energy. Since even $\{I, H_3\} + H_{BC}$ is more stable than interstitial silane, the molecule can be ruled out as a candidate as a model for the 2222 cm^{-1} line.

The binding energies of H to vacancy aggregates V_n, defined from $V_n + H_{BC} \rightarrow \{V_n, H\} + \Delta E_n$ and shown in Fig. 2, exhibit no correlation with the stability of V_n.[14] ΔE_n increases up to n=5 then remains constant at about 3.8 eV. In all the vacancy aggregates, H forms a strong Si–H bond with H pointing toward a perfect (vacant) lattice site. The defect reconstructs around that bond. The larger the defect, the more degrees of freedom, and the easier it is to realize a perfect reconstruction. The general features of the Si–H bond in $\{V_n, H\}$ are largely independent of n, and configurations such as H bridging a reconstructed Si–Si bond never occur.

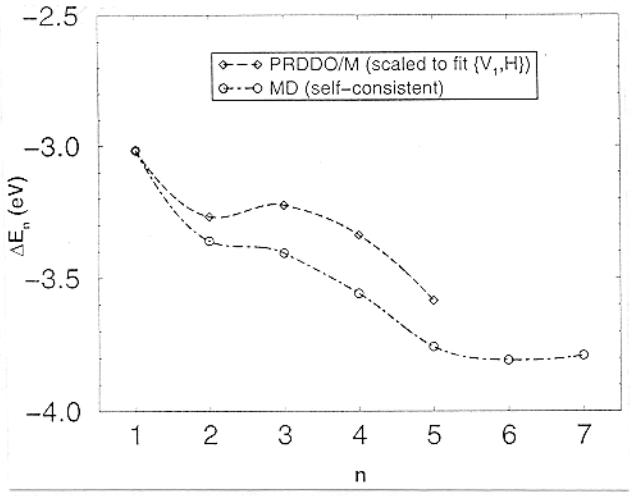

Fig. 2: Binding energy of H to V_n defined as the difference between the total energies of $\{V_n, H\}$ and $\{V_{n-1}, H\} + H_{BC}$.

An comparison of the energy spectra of V_n and $\{V_n, H\}$ shows that none of the V_n's which, by themselves, have deep levels in the gap (n=1, ...,5 and n=7), are passivated by a single H. Some of the energy eigenvalues do shift, but they remain within the gap. On the other hand, V_6 by itself has no localized eigenvalue in the gap. Upon trapping one H, at least one deep level appears in the gap and H activates this defect.

Fig. 3 shows the structure of $\{V_4, H\}$ and several MO's. A 'dangling' p orbital is clearly visible on one of the Si atom. It is associated with one of the deep levels of this defect. Another MO, associated with a shallow level, extends over a reconstructed Si–Si bond with two small antibonding components on either side of it.

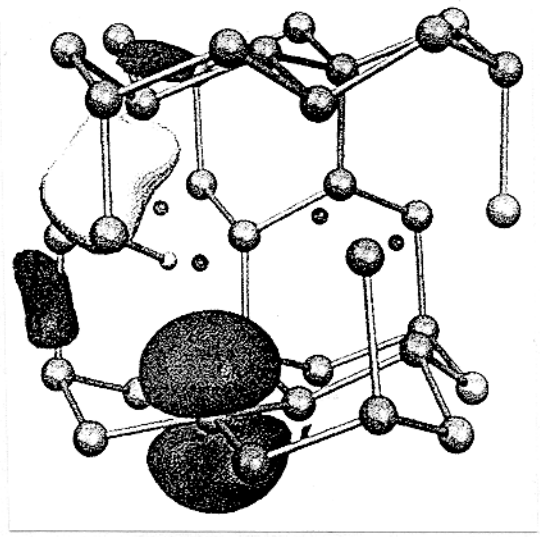

Fig. 3: Two MOs of the $\{V_4, H\}$ complex (see text). The small circles show the perfect lattice sites. Note that the Si–H bond points toward a perfect lattice site.

In conclusion, the stable configurations for four $\{I, H_n\}$ complexes (n=1,...,4) have been obtained. The most stable structures are those with an even number of H's, and of those $\{I, H_2\}$ is the most

stable. More than four H's can bind to the region surrounding I because the strain associated with the defect provides a variety of distorted Si–Si bonds where H can trap. Interstitial silane is more than $2\,eV$ higher in energy than at least two other configurations and that $\{I, H_3\}$ plus isolated H_{BC}. It is therefore not a possible defect.

H traps at V_n aggregates by forming a strong Si–H bond around which the rest of the defect reconstructs. The binding energy of H to V_n (relative to isolated H_{BC}) increases with n up to n=5, then remains mostly constant. There is no correlation between the stability of V_n and the binding energy of H to it. None of the small V_n aggregates is passivated by trapping a single H, and V_6 is activated by it.

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ADVANCES IN STRING RIBBON CRYSTAL GROWTH

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Abstract

Under a PVMaT subcontract, Evergreen has developed methods for improving the String Ribbon crystal growth process. In this report we describe improvements in run length, in controlling grain boundary formation and ribbon edge thickness through edge meniscus control and an automated ribbon thickness control system.

Evergreen's method for the continuous production of crystalline silicon substrates is termed String Ribbon [1,2,3]. Two high-temperature string materials are brought up through a graphite crucible. A seed is lowered into a shallow melt of silicon in the crucible, and a ribbon of (presently) 5.6 cm width is then grown with the strings incorporated into the edges of the ribbon and used to stabilize the edges of the growing ribbon. No serious deleterious effects of leaving the strings in the ribbon have been found. So far, the only effects of incorporating the strings into the growing ribbon is that they can promote the formation of higher angle grain boundaries in a region a few mm wide adjacent to the ribbon edges and that they can result in thinner edges. As will be seen further on, each of these issues have been addressed under this subcontract. The central portion of the grown ribbon consists mainly of coherent twin boundaries and large grains. The material as grown is p-type, with bulk resistivity of about 2 ohm-cm, and is nominally 300 μm thick.

Increasing Run Length—The String Ribbon crystal growth process is designed to be run continuously. Early on, at Evergreen a method to continuously replenish feed material and also a means of continually feeding string material was developed and deployed. As a result, the crystal growth machines can be run 24 hours a day, 7 days a week. With the accomplishment of continuous operation, run length becomes a major driver of operating and consumables cost. Run length is here used to describe either the time (in weeks) or the length of ribbon grown (in hundreds of feet) before the crucible must be replaced.

After a considerable amount of actual running experience, it became clear that the string material was a principal factor in reducing run lengths. We therefore embarked on a major program to develop a new string material. While the principal goal was to achieve higher run lengths, another subsidiary goal was to find a material that would not result in nucleating high-angle boundaries near the ribbon edge.

The main criterion in developing a new material was to find a suitable material with a coefficient of thermal expansion (CTE) match close to that of silicon. Finding a commercially available material with a good CTE match to silicon was a difficult technical problem. For

example, Ciszek [3] has grown ribbon in this process using quartz fibers that are known to have a very different CTE value than silicon. The result is that the quartz fibers literally pop out of the ribbon after growth due to the stresses built up from the CTE mismatch.

In the end, a successful string material was developed and deployed. The result was an increase of run lengths from 2 to 4x their prior values.

Edge Meniscus Control—The general robustness of the String Ribbon growth process allowed us to develop a method to modify the ribbon edge meniscus. The result was that a stronger and thicker edge could be grown and that grain boundary nucleation at the edge could also be reduced significantly, although not eliminated entirely. The stronger edge had a dramatic effect on downstream yields that were improved by 15-20%.

Automated Thickness Control—Thickness uniformity across the 5.6 cm width of the ribbon is another important driver of downstream yield. At present, thickness measurement and control are done manually. The crystal growth operator measures ribbon thickness and then makes corresponding adjustments in the crucible temperature distribution as required. Thus, automating thickness control will both increase yield and boost labor productivity.

Three elements were needed to achieve this goal of automatic thickness control: (i) a method to measure thickness as the ribbon grows, (ii) a means of adjusting crucible temperature distribution, and (iii) an appropriate algorithm to provide for a closed feedback loop between the measured thickness and the temperature adjustment.

We have developed a suitable optical method for (i), an electro-mechanical method for (ii), and are now debugging (iii). The results so far are very promising and represent a major step towards an automated ribbon growth system.

Summary—Significant progress in production sensitive areas such as yield, run length and productivity was accomplished.

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Defect Evolution in Hydrogenated Crystalline Si under Thermal Anneal

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Hydrogen in crystalline silicon evinces considerable interest due to recent developments such as Si wafer bonding, and impurity gettering in buried void layers. Implantation and plasma processing are frequently involved in these techniques, and result in defect formation. The growth and dissolution of these defects on annealing are of considerable interest since they affect the final device properties. In our earlier work we have shown that the defects in Electron Cyclotron Resonance (ECR, a high flux low energy plasma) hydrogenation on crystalline p-Si evolve only on annealing at temperatures greater than ~ 450°C. In this work, we now compare the defect evolution on hydrogenating n-Si, p-Si and Ar ion implanted p-Si using DLTS and TEM.

DLTS studies (for n-Si and p-Si) reveal that the damage due to hydrogenation can be observed only when the samples have been annealed at temperatures higher than 450°C, indicating the presence of latent defects that require thermal activation. The deep levels observed are typically majority carrier type defects.

TEM studies on the other hand reveals a very interesting dopant-type related phenomenon. Extended defects are observed in n-Si after hydrogenation at room temperature, which is not present in p-Si. The extended defects in p-Si (as seen by TEM) evolve only after a high temperature anneal step. High temperature (~ 500°C) anneals in the case of hydrogenated n-Si, in contrast, dissolve these extended defects.

It is known that a damage layer (created for instance, by ion implantation) traps atomic hydrogen. We have hence studied the DLTS spectra of samples that were pre-implanted with Ar before hydrogenation. For a purely hydrogenated sample subjected to a 500°C anneal, four majority carrier peaks of substantial concentration ($> 10^{13}$ cm^{-3}) are observed. However, for a sample subjected to the same hydrogenation and anneal conditions, but implanted with Ar prior to hydrogenation, DLTS reveals just a single majority peak of much lower concentration. For the purely hydrogenated case, hydrogen penetrates deep into the sample. When subjected to a high temperature anneal, this hydrogen outdiffuses resulting in the generation of defects. In the ion implanted case, the presence of the damaged layer, prevents hydrogen from penetrating into the sample, which is the likely reason for not observing any hydrogen-related defects by DLTS. Preliminary results have revealed the presence of minority traps in the sample that was Argon implanted and then hydrogenated. Our presentation will outline the source and evolution of these defects and their implication in Si processing.

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Extending PVSCAN to Meet the Market Needs for High-Speed, Large-Area Scanning

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INTRODUCTION

PVSCAN is a versatile instrument that has many applications in the PV industry, including high-speed mapping of material and cell parameters such as defect density, reflectance, and LBIC response. Recently, the PV community has been interested in acquiring this instrument for material and cell analyses and for process monitoring. NREL has made a commitment to devote internal resources to either build PVSCAN or provide technical assistance for those who wish to license the instrument. Consequently, it has become necessary for us to document the pertinent information about the system and to prepare a suitable operational manual. We have also learnt that each buyer may have somewhat different needs that must be accommodated while making each instrument. In particular, there is increasing interest in upgrading the system to have the capability to scan larger substrates and cells, with higher speeds and finer resolution.

This paper explores various issues that arise in developing a commercial instrument such as PVSCAN. Emphasis is on the technical details of the ability to scan fast and the detrimental effects this fast scan can have on the image quality of various material/cell parameters.

A BRIEF DESCRIPTION OF PVSCAN

PVSCAN uses the optical scattering from a defect-etched sample to statistically count the density of defects. It shines a laser beam on the surface of the defect-etched wafer and measures the (integrated) intensity of the reflected (scattered) light. The total integrated reflected light is proportional to the number of scattering centers [1]. Thus, this system provides a signal that is proportional to the local dislocation density. By scanning over the sample, the instrument can map the defect distribution. Furthermore, grain boundaries and dislocations have different characteristic scattering-patterns, and PVSCAN uses these patterns to distinguish between different kinds of defects, as illustrated in Figure 1. Figure 2 is a schematic of the optical system.

PVSAN also provides a quantitative means of measuring the LBIC response of a solar cell at two different wavelengths (0.633 and 0.905 μm) of light excitation. This enables the instrument to separate the near-surface and the bulk recombination characteristics of the cell. The photo-current response for each excitation can be measured and saved by the computer as the external

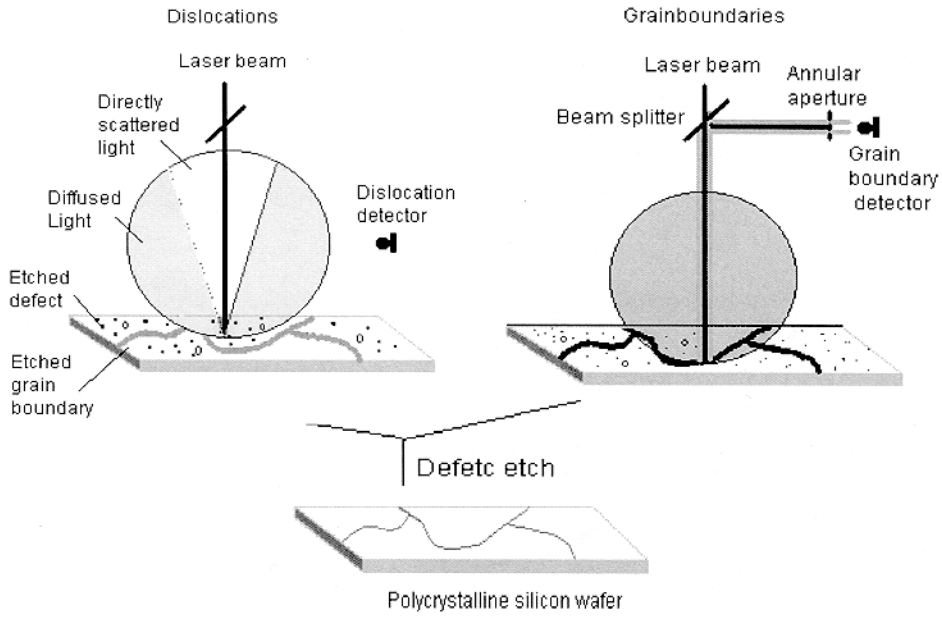


Figure 1. PVSCAN uses differentially reflected light to distinguish between various defect types. After treatment with a special etch, dislocations scatter the incoming laser beam in a cone-shaped pattern which the PVSCAN captures with an integrating sphere (left). Grain boundaries reflect the beam nearly directly, and the PVSCAN redirects a portion of that reflection to a separate detector.

response. PVSCAN's capability of mapping reflectance provides an important step toward identifying losses in the cell because reflectance is a major cause of "efficiency loss" for solar cells. By combining the LBIC reading with reflectance losses, the instrument calculates the cell performance as a function of the light that is actually transmitted into the cell to get an internal photoresponse; this is the core information needed to improve cell performance.

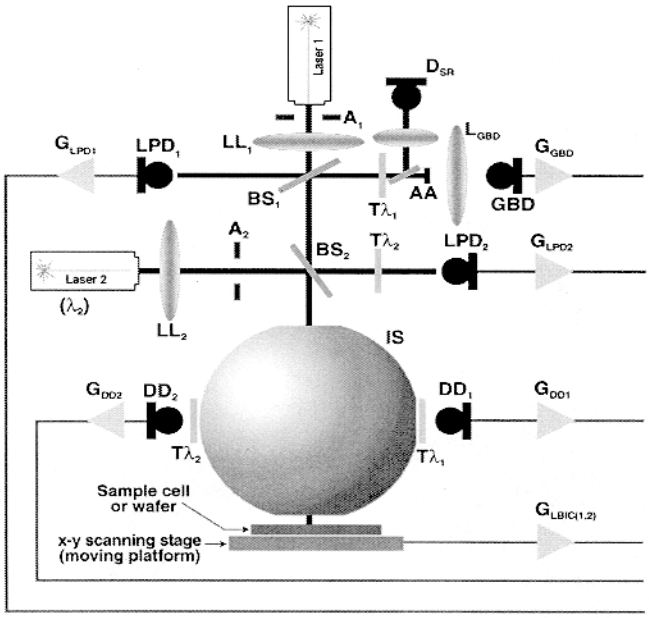


Figure 2. A schematic of the optical system of PVSCAN.

DOCUMENTATION

To build a system, one needs a host of documentation of sufficient detail. The documentation includes:

- a complete set of drawings
- listing all parts/naming the parts
- listing functional modules
- an instruction manual.

NREL is in the process of documenting all details that will allow an outside job-shop to fabricate various parts and the chassis.

MEETING THE TECHNICAL CHALLENGES

1. Larger scan area

There is increasing interest in going to larger wafers and solar cells. The PVSCAN was originally designed to accommodate 4-in. x 4-in. wafers and cells. However, industry is already making commercial cells that exceed this size. We have received requests to increase the ability of PVSCAN to scan 8-in. x 8-in. cells. It is a straightforward matter to achieve this by switching to an X-Y stage with a larger travel, but an increase in the scan area generally leads to an increase in the scanning time (if the resolution is kept the same). In general, an increase in the sample area by a factor of 4 requires an increase in the scan time by a same factor.

(a) A defect map of a 2-in.x2-in. area at the scanning speed of 3 inch/s. The resolution is 0.001 inch. This scan took about 1 hour.

(b) A defect map of the same area at the scanning speed of 1 inch/s. The resolution is 0.001 inch. This scan took about 2.5 hours.

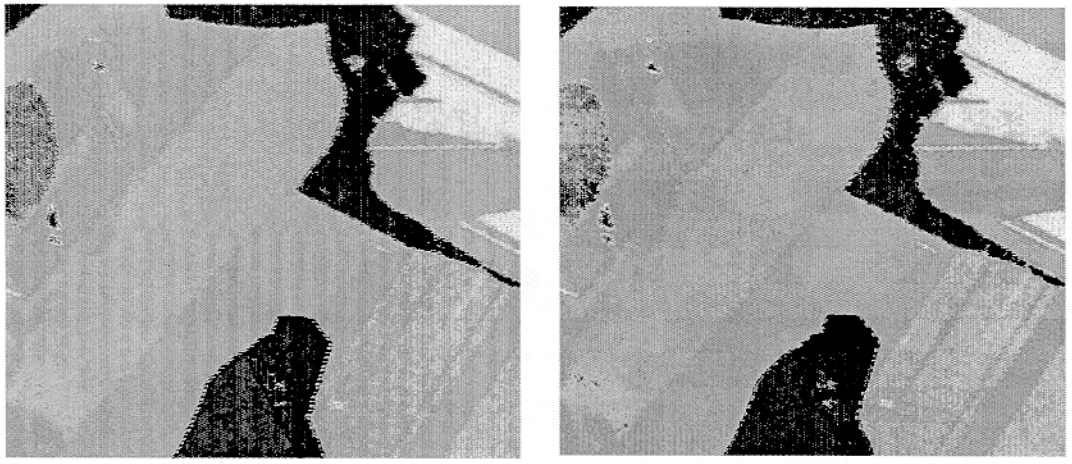
Figure 3. Images of a 2-in. x 2-in. wafer taken at two different scanning speeds, showing nearly identical image quality.

Our approach to increasing the scan area consists of switching to an X-Y stage that has a capability of scanning at a higher speed, typically up to 4 inches per second. Thus, we can scan a 8-in. by 8-in.area, keeping the scanning time and resolution the same as the original PVSCAN. It is crucial that as the speed is increased, the image quality should not deteriorate. Figure 3 compares the quality of the reflectance images of a sample scanned at two different speeds in our system. The resolution is 25 μm, and the difference in the image quality is essentially indistinguishable.

2. Higher resolution

The resolution of a scanning system is a complicated parameter that is determined by:

- Step size of the motors
- Optical beam size
- Time interval between the data-taking events
- Time constant of the electronic signal channel.



(a) **(b**

Figure 4. The defect maps of a 0.5-in.x0.5-in. area. The scanning speed is 0.75 inch/s. The resolutions are (a) 0.001 inch and (b) 0.00025 inch.

In general, the PVSCAN uses a beam size of about 200 μm in the defect mapping mode and smaller size in the LBIC mode. For a motor step of 25 μm, a 50 μm spatial resolution in the image can be achieved. Figure 4 shows that with a typical beam size the scanning resolution has little or no effect on the image quality. Even under higher magnification, Figure 5, the effect is primarily observable as a slight loss in the Y-resolution.

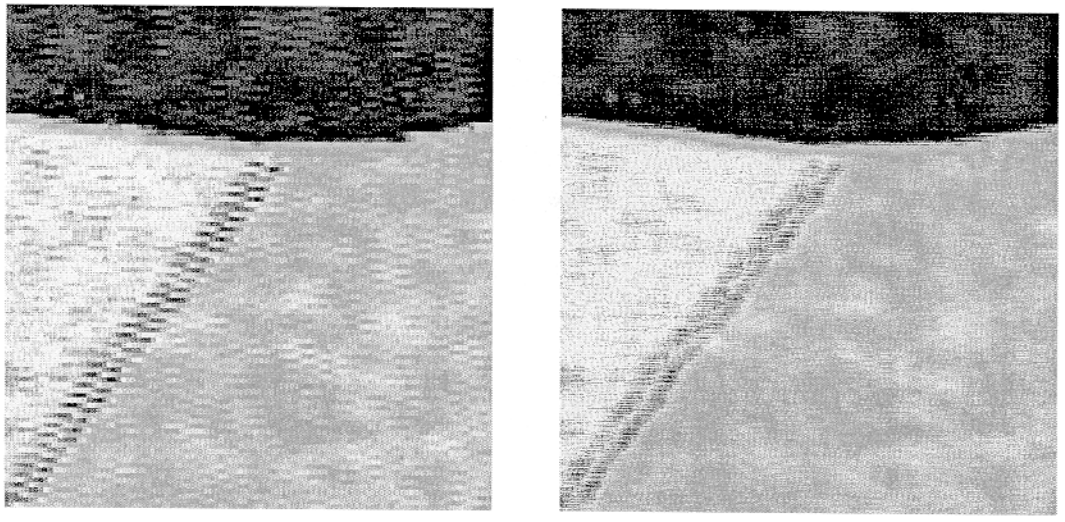


Figure 5. A zoomed-in view of a small region of the sample in Figure 4, showing no effect on the image quality, even when the display is zoomed into a small area.

3. Effect of beam size

It is desirable to have beam size about the same as the lateral step size of the motor. But, in practice, a small beam size makes stringent demands on the optical system. Furthermore, it is important that the beam size exceeds a certain value so that statistical counting of defects is valid. In general, the beam-size requirements for most applications of PVSCAN are only moderate. However, it must be pointed out that mathematically the beam and the motor step have the effect of generating a signal that is an overlap integral of the two. This means that the signal in the "forward" and the "reverse" directions will be shifted laterally. An example of this is illustrated in the scans of Figure 6.

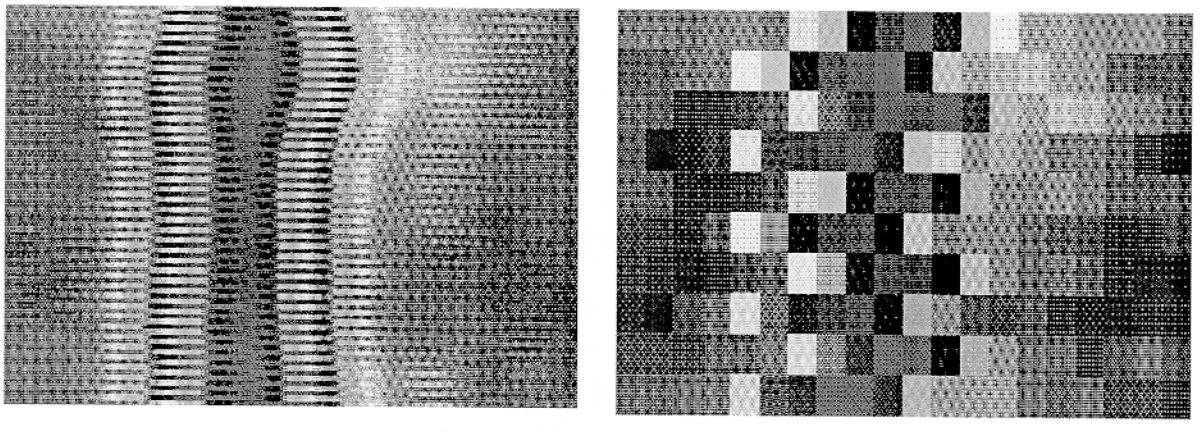


Figure 6. Illustration of the beam-size effect on the scanned image. (a) LBIC image in the vicinity of a metal finger on a solar cell, showing displacement of the signal in the "forward" and the "reverse" directions. (b) A zoomed-in view.

4. Higher-speed scanning

It is generally desirable to have as high a scan speed as possible. However, scanning speed is limited by :

- Maximum speed of the motor(s), resolution of the stepping motor, and the mode of operating the motor (open Vs closed-loop configuration)
- Data-acquisition rate and data-transfer capability
- "Blank" time, in which a Y-step is taken (this time is also used for transferring data from the internal memory to the disk)
- RC time constant of the signal channel(s) and its changes with the gain.

These issues can be optimized to obtain the highest scanning speed. Our system can be operated up to 4 ips without degrading the image quality (as seen in Figure 3).

5. Improvements in the software

The software has been improved to include:

- Statistical module that displays distributions (see Figure 7, showing distribution of defect density in a multicrystalline Si wafer) and other statistical functions
- Additional options on "save" images/scans
- Ease of calibration

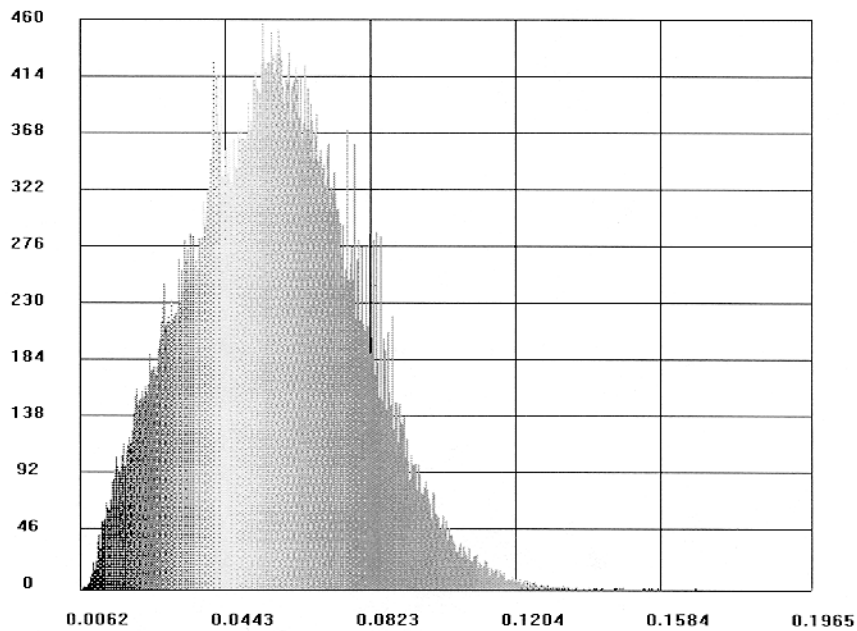


Figure 7. Distribution of dislocations in a mc-Si wafer. The Y-axis shows number of counts and x-axis is the dislocations density, cm^{-2} $x10^4$

CONCLUSION

We have documented the PVSCAN so that it can be built at a job-shop. The operation of the system has been critically analyzed to help the user make an informed decision on setting up the scan parameters and interpret the results. A detailed instruction manual is being written that incorporates examples and results of actual scans. The software has been upgraded to include a number of useful features.

Contactless Characterization of Fe and Ni Contaminated Silicon Wafers Using Frequency Resolved Microwave Photoconductance

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Microwave photoconductive decay (μ-PCD) is generally used as a contactless and non-destructive method to analyze the minority carrier recombination lifetime, the method can also be used to identify more specific materials properties, such as the activation energy, capture cross section, and recombination center concentration [1,2,3,4,5]. Usually the Shockley-Read-Hall model is used for recombination parameter evaluation from the carrier lifetime and then material parameters are evaluated using the least-squares algorithm, which, however, provides a non-unique solution. In order to overcome these limitations the use of additional physical control parameters such as temperature or injection level have been introduced [6,7,8].

In this paper, an approach based on the frequency resolved photoconductance (FR-PC) is described which is particularly suitable for operation at low injection levels [9]. Both the temperature and the injection level dependence have been used for parameter evaluation. The parameters are determined by nonlinear fitting of the experiment frequency dependent spectra with a model using a single level recombination center. It is shown that the procedure gives stable parameters determined from quadrature spectra measured at elevated temperatures 180^0C and 240^0C. Validity of the method has been verified for the p-type silicon wafers containing Fe and Ni impurities and compared with DLTS data. In both Fe and Ni contaminated wafers, only the E_V + 0.48eV level, assigned to iron is detected with concentration 2.25×10^{12} cm^{-3} and electron/hole capture cross sections 9.5×10^{-15} cm^2 and 1.7×10^{-16} cm^2, respectively. The Fe-B pair concentration measured using DLTS was 4×10^{12} cm^{-3} and is about two times lower than value evaluated from frequency resolved spectra.

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Experiments and Computer Simulations of p/p^+ Gettering of Iron in Silicon

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The segregation behavior of iron from typical p doped regions to heavily p or n doped silicon is examined quantitatively. Additionally, the out-diffusion behavior of iron in the presence and absence of a surface oxide is determined. The segregation coefficient of iron into heavily doped regions is determined by where the iron trap level is situated in the bandgap. The high temperature experimental evidence suggest that there is a strong temperature dependence of the $Fe^{0/+}$ trap level, but there have been no studies of the iron trap level at medium temperatures. After intentional iron contamination, iron profiles in p/p^+ and p/n^+ (epitaxial layers/substrate) structures are measured with DLTS for various annealing times and temperatures, i.e. 400°C to 600°C. Experimental iron profiles are fitted with computer simulations in order to determine the segregation coefficient at medium temperatures. Iron-boron dissociation kinetics was studied experimentally in order to calculate the effective diffusivity of iron in the heavily doped substrate. It is observed that there is no segregation to n^+ regions. Additionally, iron out-diffused with a bare silicon surface and did not out diffuse with a 100nm wet oxide. The iron profiles in the p/p^+ structures indicated the iron trap level to be above the expected level. Thus, segregation to highly doped regions is stronger than expected.

About the reaction path of copper in silicon

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Out-diffusion and precipitation of copper in silicon was studied after a high temperature intentional contamination of p-type samples and quench to room temperature. It was found that below a critical copper contamination level the copper predominantly diffuses out to the surface, while for higher initial copper concentrations copper mainly precipitates in the bulk. The critical copper contamination level depends on the doping level of the sample and equals the acceptor concentration plus 10^{16} cm^{-3}. This behavior can be explained by the electrostatic interaction between the positively charged interstitial copper and the growing copper precipitates. The charge state of the electrically amphoteric precipitates changes with the Fermi level position. Both the concentration of shallow acceptors and the interstitial copper, which serves as a donor, determine the Fermi level. If the Fermi level position is below the neutrality level of the precipitates at E_C-0.2 eV, the precipitates are positively charged, and Coulomb repulsion will retard precipitation of copper. Under these conditions out-diffusion of copper predominates. However, the precipitates become neutral or negatively charged if the interstitial copper concentration is large enough to drive the Fermi level above the neutrality level. In this case repulsion between the copper ions and the precipitates disappears and rapid precipitation takes place.

The introduction of copper interconnects in silicon integrated circuit technology has drastically increased the danger of unintentional in-diffusion of copper into silicon substrates. Consequently, the understanding of the physical behavior of copper in silicon and its reaction paths has become an important issue in semiconductor materials science and device technology. Among all transition metals, copper has the highest solubility in the silicon lattice at elevated temperature [1,2]. While at room temperature the equilibrium concentration of interstitial copper drops to a negligible level, it remains highly mobile [3]. Interstitial copper is a single donor with a level close to or even in the conduction band, compensating shallow acceptors [1]. Copper-acceptor pairing can significantly reduce the effective diffusivity of copper in p-type silicon [3,4]. However, this interaction is too weak for effective trapping of copper at room temperature [5]. Only a small fraction of the in-diffused copper forms stable point defects and complexes with mixed covalent-ionic character [6,7,8]. In fact, most of the supersaturated interstitial copper follows one of two distinct reaction paths discussed in literature: out-diffusion to the surface and precipitation in the bulk. Transmission Electron Microscopy (TEM) studies suggested that after introduction of 10^{17}-10^{18} cm^{-3} copper, most of the copper precipitates in the bulk upon cooling [9,10,11]. In n-type silicon it was found that with cooling rates larger than 100 Ks^{-1} the precipitates form plate-like defects throughout the bulk of presumably Cu_3Si mainly on {111} habit planes. These defects introduce band like states in the upper half of the band gap, as has been studied with Deep Level Transient Spectroscopy (DLTS) [8,9,12]. Copper precipitates are electrically amphoteric, i.e. they display a change in their charge state from positive to negative as the Fermi level is raised above the neutrality level at E_C-0.2 eV [10,13]. In contrast to silicon contaminated with very high copper concentrations, Total X-Ray Fluorescence (TXRF) studies on p-type silicon with copper contamination levels around 10^{15} cm^{-3} demonstrated complete out-diffusion of copper to the surface after both slow cool [14] and quench [15]. The objective of this letter is to determine the conditions under which copper diffuses out to the surface or precipitates in the bulk, and to understand why it chooses the one or the other reaction path.

We have investigated p-type dislocation free FZ and Cz-grown silicon with doping concentrations in the range of 10^{14} to 10^{16} boron atoms per cm^3 after intentional copper contamination of 10^{13} to 10^{18} cm^{-3}. Interstitial copper concentrations have been measured with the Transient Ion Drift (TID) technique [16,17]. Although interstitial copper is unstable in the silicon lattice at room temperature, it has been shown that significant amounts of copper remain dissolved for some hours after quench and can be detected by TID. The concentrations of precipitated copper in the bulk were measured by synchrotron-based X-Ray Fluorescence (XRF) at beamline 10.3.1 at the Advanced Light Source [18].

After cleaning the silicon samples at clean-room class 100 conditions with Piranha and HF, copper was dip-coated in a solution containing copper(II) fluoride trihydrate, HF, and H_2O. High temperature diffusion was carried out in a high-purity nitrogen ambient using a vertical furnace. The samples were quenched in silicon oil, ethylene glycol, or 10% NaOH. This results in approximate quenching rates of 500°C per second, 1000°C per second, and 2000°C per second, respectively. Cooling the sample at air, which corresponds to a quenching rate of approximately 100°C, is shown to be not fast enough to keep the copper in the interstitial state. To avoid cross contamination, the time of in-diffusion was chosen to be 30 min, which is sufficient for a

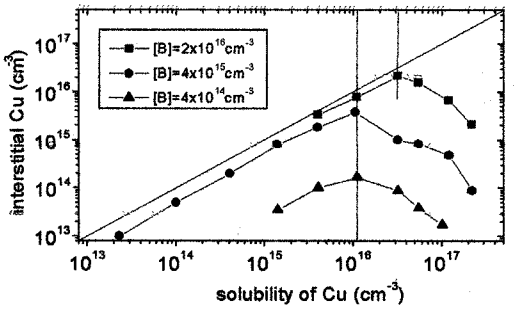

FIG.1. Interstitial copper concentration as measured with TID 30 min after quench at room temperature vs. the solubility concentration of copper at in-diffusion temperature.

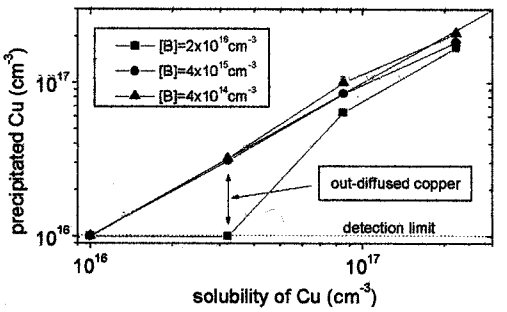

FIG.2. Copper concentration measured with XRF vs. the solubility concentration of copper at the in-diffusion temperature.

homogeneous distribution of interstitial copper throughout the bulk. In contrast to HNO_3 containing dip-coating solutions, HF containing solutions do not form an oxide between the silicon surface and the copper coating, which can serve as an in-diffusion barrier for temperatures below 800°C. However, it was found that the concentrations of copper in-diffused at temperatures below 650°C are far below the solubility concentrations given by E. R. Weber for silicide boundary conditions [2]. Copper silicide nodules are observed by TEM for temperatures above 650°C [19]. To reach solubility concentrations given in ref. [2] for silicide boundary conditions at in-diffusion temperatures below this critical temperature, the samples have been heated above 650°C for 30 min and then cooled down very slowly, with about 1°C per min, to the desired in-diffusion temperature before quench. Following the in-diffusion process the samples surfaces were cleaned in Aqua Riga to remove the remaining metallic copper and a surface layer of about 30 μm was etched off by CP4 to remove copper silicide nodules. To measure the interstitial copper concentrations with TID, small aluminum Schottky diodes were evaporated on the sample surface without removing the surface oxide due to the CP4 process, Ohmic contacts were prepared by gallium eutectic plating on the sample backside. In-between these process steps the copper diffused samples were stored in liquid nitrogen to prevent the copper from diffusing, enabling the first TID measurement after a total time of 30 min at room temperature. To prepare the diffused samples for XRF measurements, the samples were stored for extensive time at room temperature, and a surface layer of several tens of micrometers was etched off. For XRF microprobe profile line scans, samples were prepared by bevel polishing. Copper concentrations were quantified with XRF by comparison to standards of known copper concentration and accounting for matrix effects.

Neither the TID measurements nor the XRF results differed for FZ and Cz-grown silicon or for the three quenching liquids listed above. For this reason we do not specify these parameters throughout this letter.

In Fig. 1 we show the interstitial copper concentration as measured with TID 30 min after quench vs. the solubility of copper at the in-diffusion temperature as given in ref. [2]. For each of the three differently doped samples a lower and a higher copper contamination region can clearly be recognized. At a relatively low copper contamination the concentration of interstitial copper increases monotonically with the solubility concentration until it reaches a maximum at a certain critical contamination level. Beyond this critical contamination level the observed interstitial copper concentration decreases with increasing solubility. The critical copper contamination level has been found to be depending on the doping concentration. While its value approximately matches for the two lower doped samples, the critical concentration for the sample doped with 2×10^{16} cm^{-3} is significantly shifted to a higher value. As a rule of thumb the value of the critical copper contamination level equals the acceptor concentration plus 10^{16} cm^{-3}.

In order to determine the main reaction path of the copper above the critical contamination level we show the bulk concentration of precipitated copper as measured with XRF vs. the solubility of copper at the in-diffusion temperaturein Fig. 2 for the same three doping concentrations as in Fig. 1. These measurements were performed after sufficient storage time at room temperature allowing the interstitial copper to complete its preferred reaction, i.e. to diffuse out to the surface or to precipitate in the bulk. It can be seen that for all samples with an initial copper concentration larger than the critical contamination level, as defined in Fig. 1, the concentration of precipitated copper approximately equals the copper solubility. Thus, if the copper contamination exceeds the critical level, bulk precipitation is the main reaction path of the interstitial copper. Furthermore, in an attempt to investigate bevel-polished samples with the XRF microprobe we were not able to detect a profile of precipitated copper. Hence, in the case of precipitation, most of the copper precipitates immediately after or during quench, i.e., significantly faster than out-diffusion could occur.

In the contrary, if the copper contamination is below the critical concentration, out-diffusion is the predominant mechanism. This can be seen in Fig. 2, where no precipitated copper was detected for the sample doped with 2×10^{16} boron atoms per cm^3 after in-diffusion of copper to an amount that equals the critical copper contamination level of $3\times10^{16}cm^{-3}$

for this particular sample. Since XRF detects all copper regardless of its state, precipitated or dissolved, the missing copper has diffused out of the bulk. Due to the detection limit of 10^{16} copper atoms per cm^3, lower contamination levels could not be accessed by XRF.

To further elucidate the reaction path of the copper at sub-critical contamination, we studied the interstitial copper concentration as measured with TID vs. storage time at room temperature. In Fig. 3 results for three samples with an identical boron doping concentration of 6×10^{15} cm^{-3} and with an identical initial copper contamination of 5×10^{15} cm^{-3} but with varying thickness of 300, 600 and 900 μm are shown. Under these conditions the maximum concentration of copper measured with TID after quench can be close to the solubility concentration of copper at the in-diffusion temperature, while the concentration of interstitial copper decreases with time. The decay is non-exponential and slows down during storage at room temperature. Furthermore, the rate of the decay decreases with increasing sample thickness. Such dependence can be understood by an out-diffusion process. While a bulk precipitation rate would not depend on the thickness of the sample, an out-diffusion rate decreases with the distance the copper ions have to migrate to the surface, i.e., with the sample thickness. The out-diffusion of interstitial copper in p-type silicon can be simulated using a copper-dependent effective diffusivity adapted from Reiss et al. [4]. In the case of $N_{Cu} \leq N_A$ the effective diffusivity D_{eff} is given by

$$D_{eff}\left(N_{Cu}(\vec{z})\right) = D_{\text{int}} \times \left[1 + \frac{\frac{1}{2}\left(N_{Cu}(z) - N_A + \frac{1}{\Omega}\right)}{\sqrt{\left(N_{Cu}(z) - N_A - \frac{1}{\Omega}\right)^2 + \frac{N_{Cu}(z)}{\Omega}}}\right]$$

where $N_{Cu}(z)$ is the mobile interstitial copper concentration at the wafer depth z and N_A is the acceptor concentration. The intrinsic diffusivity of interstitial copper D_{int} is given in ref. [3] and the pairing constant Ω of copper-boron is taken from ref. [5]. Because the TID technique measures the interstitial copper concentration in the space charge region of a reverse biased Schottky diode, we compare the TID measurement results with concentrations taken at the first micrometers of simulated concentration profiles. The computer simulations assume out-diffusion kinetics and no precipitation. Including boundary conditions that depend exponentially on the amount of the out-diffused copper could fit the data well for a given sample thickness. The origin of such dependence could be that the surface band bending defines the out-diffusion conditions of the copper ions, and that the surface charge state changes with the out-diffusion of the interstitial copper. Details of the computer simulations will be reported elsewhere [19]. Thus, the interstitial copper concentrations measured with TID are associated with the out-diffusion of copper.

Next, it can be seen in Fig. 1 that the interstitial copper concentrations measured with TID 30 min after quench depends strongly on, and never exceeds the doping

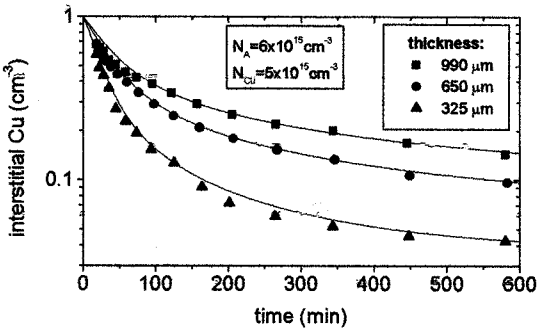

FIG.3. Interstitial copper concentration vs. storage time at room temperature after quench. Symbols represent measurement points as achieved with TID. Lines are simulation results assuming out-diffusion kinetics and no precipitation.

concentration. This observation can be understood by the influence of the copper concentration dependent effective diffusion coefficient and by an additional drift effect, rather than by partial precipitation within the lower copper contamination region. Lower doping concentrations as well as higher interstitial copper concentrations themselves lead to a larger effective diffusivity of the interstitial copper, and consequently to faster out-diffusion and a less steep concentration gradient in the near surface region. Under certain conditions, the interstitial copper concentration can be orders of magnitude higher in the bulk than measured with TID in the near surface region. If the copper concentration exceeds the doping concentration conductivity type inversion may occur and an additional drift effect due to an internal junction forces the interstitial copper concentration in the near surface region do drop very rapid below the doping concentration. We infer that within the lower copper contamination region out-diffusion of the interstitial copper to the sample surface is the predominant reaction path.

Within the higher copper contamination region small amounts of interstitial copper are still observed with TID, see Fig. 1. This indicates that at some point, after large amounts of copper have precipitated, the precipitation process slows down drastically and the remaining interstitial copper diffuses out.

In the following we show that all experimental observations can be explained consistently by a model based on the position of the Fermi level. In Fig. 4 the maximum interstitial copper concentration as measured with TID is plotted vs. the Fermi level position at room temperature. Motivated by the fact that the critical contamination level was found to be independent of the three fast quenching rates the Fermi level position was calculated from the concentration of acceptors and the initial copper donor concentration at the in-diffusion temperature. For an initial copper concentration lower than the acceptor concentration the Fermi level is in the lower half of the band gap and rises slowly with increasing copper contamination. When the copper concentration exceeds the doping level the conductivity type changes from p- to n-type. This is however

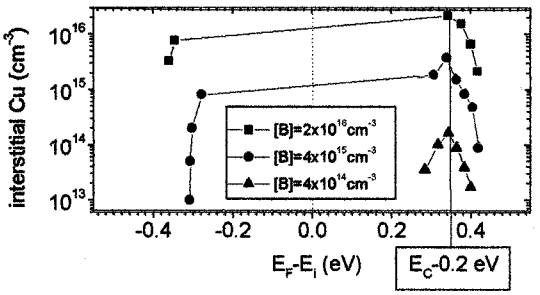

Fig.4. Interstitial copper concentration as measured with TID 30 min after quench at room temperature vs. the Fermi level position immediately after quench. The Fermi level was calculated from the acceptor concentration and the initial copper donor concentration at the in-diffusion temperature.

not sufficient to change the precipitation behavior of copper. Only when the Fermi level exceeds a critical value of E_C-0.2 eV does precipitation take place. Remarkably, this critical Fermi level position at E_C-0.2 eV corresponds to the neutrality level of the copper precipitates observed in n-type silicon [11]. It should be noted that the precipitates found in p-type after quench are identical in morphology and reveal similar band-like states in the upper half of the band gap, as has been shown with High-Resolution Transmission Electron Microscopy (HRTEM) and Minority Carrier Transient Spectroscopy (MCTS), respectively [19]. This enables us to put forward the model that the precipitation of copper is determined by the electrostatic interaction between the positively charged copper ions and the copper precipitates. The precipitates are positively charged if the Fermi level is below their neutrality level and Coulomb repulsion will retard precipitation. If the Fermi level rises above the critical level of E_C-0.2 eV, the precipitates become neutral or negatively charged and precipitation can occur uninhibitedly. As the copper precipitates, the interstitial copper concentration decreases and the Fermi level drops below its critical value, resulting in positively charged precipitates, and the precipitation process slows down drastically.

In conclusion we have shown that a simple electrostatic model can describe satisfactorily the observed difference in the out-diffusion and precipitation behavior of copper in silicon.

We would like to point out the technologically important fact that the above model elucidates the behavior of the recombination activity of copper in p-Si, observed by Naito et al. [20], but not explained up to now. They measured that in p-type silicon copper contamination of up to 10^{16} cm^{-3} did not decrease the recombination lifetime. However, for higher copper contamination the recombination lifetime decreases drastically. This indicates that copper precipitates form strong recombination centers, and that the formation of copper precipitates control the lifetime in PV silicon.

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Characterization of TiO_x single layer antireflective coating on Silicon-Film™ material.

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Abstract

A high throughput single layer antireflective coating (SLARC) system based on spray pyrolysis of TiO_x [1] has been developed and is used in our solar cell manufacturing. The system is capable of ARcoating more than 1000 wafers per hour and yields a uniform coating with easily adjustable thickness and index of refraction. A model predicting the performance of SLARC deposited by spray pyrolysis has been developed and experimentally verified earlier [2]. In this poster we will discuss the behavior of such SLARC on Silicon-Film™ material. We have found that SLARC on Silicon-Film™ wafers has better optical characteristics than on single crystal wafers when both types of wafers were subject to identical surface treatment prior to the application of the SLARC. We will show that SLARC deposited by spray pyrolysis results in a lower solar weighted reflectance (SWR) as well as lower solar and IQE weighted reflectance (SIWR) on Silicon-Film™ compared to single crystal material.

1. Introduction

For the photovoltaic industry to grow into broader markets it is imperative to reduce the cost of PV generated electrical energy to a level that is, given some environmental premium, competitive with conventionally generated electrical energy. AstroPower is pursuing two approaches towards inexpensive solar electric power. One is the development of an inexpensive silicon substrate, Silicon-Film™; the other is implementing a high throughput, low cost, continuous solar cell manufacturing process.

One step in this manufacturing sequence is the application of a reliable SLARC by spray pyrolysis. Based on this method AstroPower has developed a very inexpensive atmospheric-pressure continuous process with high yield and throughput well in excess of 1000 wafers per hour. In addition to its low cost and high throughput our process is extremely flexible, allowing for an index of refraction ranging from 2 to 2.5 and virtually any thickness without impacting throughput and reliability. AstroPower is currently manufacturing two types of silicon solar cells, Silicon-Film™ solar cells and single crystal solar cells made from wafers recycled from the semiconductor industry. The two products have different surface morphologies, which makes it necessary to optimize the SLARC for each product individually.

2. Experiment

Two experiments have been carried out. In the first experiment five precursor solutions were prepared in order to achieve an index of refraction ranging from 2.25 to 2.5. Using these precursor solutions, single crystal and Silicon-Film™ wafers of about 25cm^2, which were subjected to all pre-AR process steps but had no gridlines printed, were coated. The thickness of the layer was chosen such that the minimum of the reflectance curve was centered at 600 nm for Silicon-Film™ material and at 640 nm for single crystal material. The different thickness of the antireflective coating for each product is due to the different red response, which is much greater for the single crystal product. The thickness of the SLARC was controlled by monitoring the color of the sample, and polished single crystal wafers were used to verify the thickness using elipsometry. To account for small variations in SLARC thickness, three samples were coated, measured, and averaged for each data point.

A second experiment was performed to determine the optimal thickness of the SLARC on Silicon-Film™ and to verify that our initial estimate of the thickness was correct. Sample preparation was identical to the initial experiment, except the index of refraction was held at 2.46, as verified by elipsometry measurements.

3. Results and Discussion

Our measurements show that on both types of wafers the best performance can be achieved with a relatively high index of refraction of about 2.45 in conjunction with encapsulation (see Figure 1 and 2). The lowest measured SIWR was about 8% for Silicon-Film™ and about 10% for single crystal wafers. The SWR shows the same trend but is slightly higher for both surfaces. This is due to the low red response, which reduces the significance of strong reflectance at wavelengths greater than 1000 nm. Encapsulation gains are higher for Silicon-Film™ material. On single crystal material there is no encapsulation gain with an index of refraction of 2.35, and there is an encapsulation loss when the refractive index is less than 2.35. However, encapsulation gains on both surfaces are notably higher if measured on samples with gridlines. Figure 3 shows typical reflectance for a high index coating on Silicon-Film™ and a low index coating on a single crystal wafer. It is apparent that long wavelength reflectance is much stronger on single crystal material for both un-encapsulated and encapsulated conditions. The encapsulation gain is higher on Silicon-Film™ material over the entire spectrum. Both effects can be explained by comparing the differences in surface morphology. Single crystal wafers, after being alkali etched, have relatively large flat <100> terraces while Silicon-Film™ wafers are randomly textured corresponding to grain orientation. This texture, although not nearly as effective as a pyramidal texturing, reduces reflectance and increases encapsulation gain. Light that is reflected at the silicon-SLARC-interface is more likely to hit the glass-air interface at an angle that results in reflection back into the solar cell rather than in transmission out of the cell.

With the optimal index of refraction established the optimal thickness for a SLARC on Silicon-Film™ was found to be around 58 nm. This thickness results in a reddish-blue SLARC. The low optimum thickness can be explained by the reduced red response of Silicon-Film wafers (diffusion length is on the order of 50 μm). As material quality improves the optimal thickness is expected to increase, which poses no problem due to flexibility of our AR coating system.

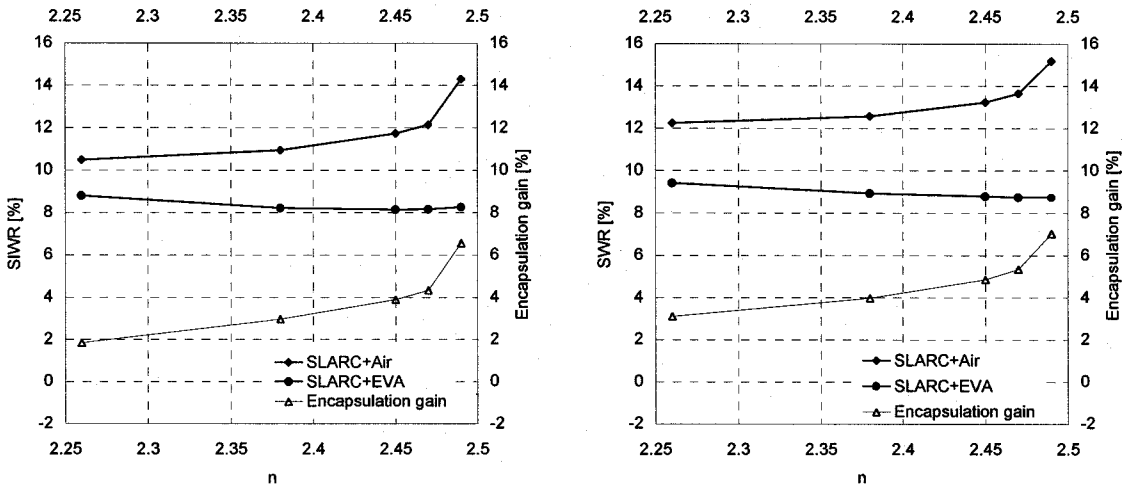

Figure 1: SIWR (left) and SWR (right) vs. index of refraction for Silicon-Film™

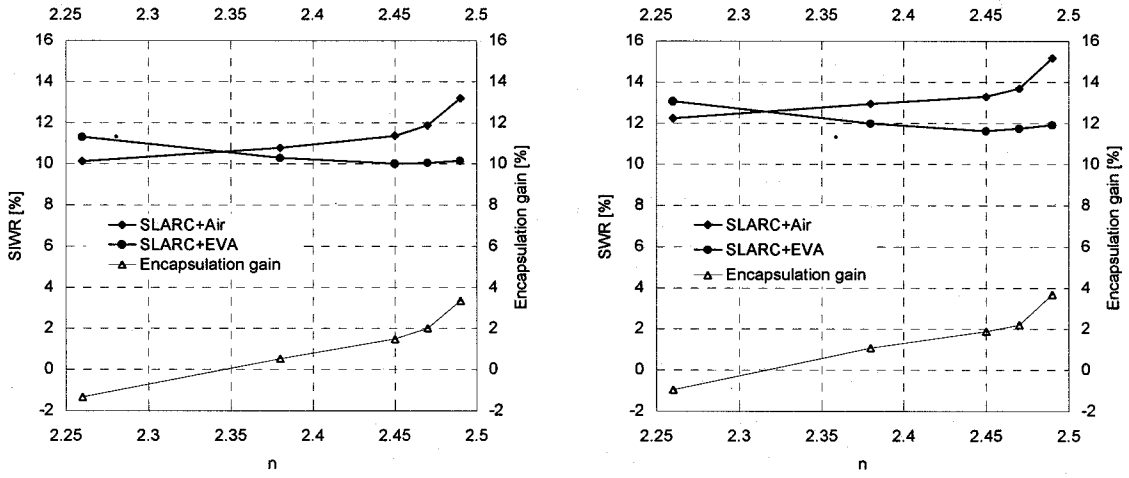

Figure 2: SIWR (left) and SWR (right) vs. index of refraction for single crystal

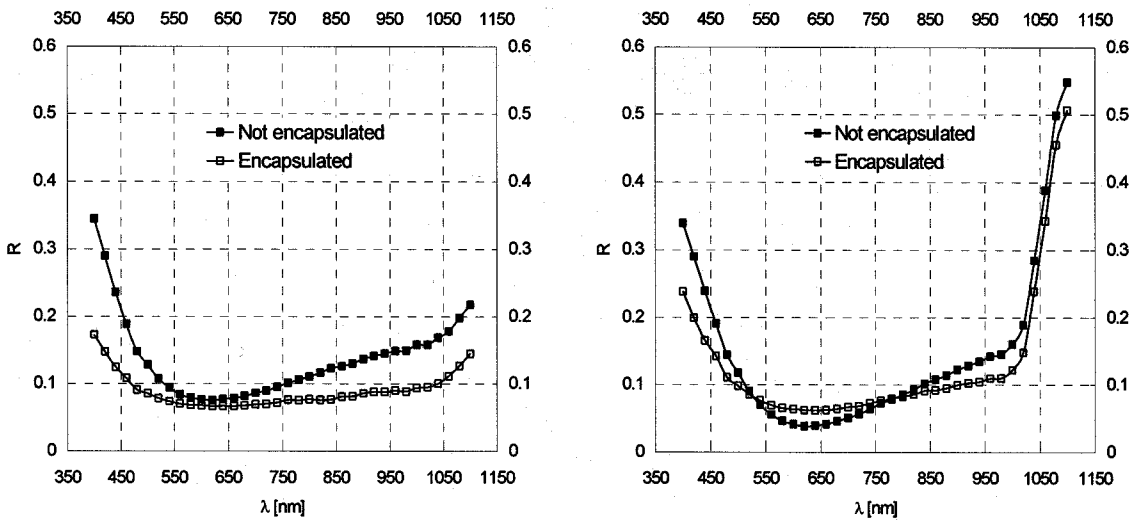

Figure 3: Reflectance of Silicon-Film™ (left, n=2.46) and single crystal (right, n=2.3)

Summary:

We have shown that low reflectance can be achieved with a TiO_x SLARC deposited by spray pyrolysis if an encapsulant with a refractive index of 1.5 is used. This system works especially well on polycrystalline Silicon-Film wafers resulting in SIWR of about 8%. The optimal index of refraction is at 2.45; however, the window in which the SWIR remains very close to the optimum is large resulting in a robust manufacturing process.

Acknowledgements:

I would like to thank Dr. James A. Rand, Jerome S. Culik, and Paul E. Sims for helpful discussions.

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Thin Polycrystalline Silicon Films by HWCVD

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Abstract

Thin polycrystalline silicon films with grain sizes between 10 to 50 nm and having (220) preferred orientation were deposited from pure silane onto 7059 Corning glass and crystalline silicon substrates by Hot-Wire Chemical Vapor Deposition (HWCVD). The effect of processing parameters, such as substrate temperature, silane flowrate and pressure, on the film properties, crystalline fraction and growth rate was investigated. The crystalline fraction was found to depend on the gas phase chemistry and substrate temperature at wire temperatures above 1815 ^{o}C.

Introduction

The goal of photovoltaic research and development is to reduce the cost per watt of solar electricity. Efforts are directed at either reducing the relatively high cost of c-Si wafer-based modules without sacrificing their performance, or increasing the relatively low performance of thin film modules without sacrificing their manufacturability over large areas. These conflicting themes can be resolved by combining the benefits of c-Si performance and stability in a low-cost monolithically integrated thin film module using thin Si devices on low cost substrates. In theory, thin Si solar cells have the potential to exceed the efficiency of thick Si solar cells due to reduced volume recombination, providing that excellent light trapping and surface passivation can be achieved[1,2]. In practice, thin Si films on a foreign substrate are expected to be polycrystalline and, thus, controlling bulk, grain, and surface defects is a critical issue in fabricating thin film Si solar cells. A key requirement for such devices is a process which yields thin Si films, ~10 μm thick, on a low cost substrate, and which have a grain size of ~10 μm, good electronic properties and adequate light trapping. By combining the advantages of c-Si with those of thin film technologies, stable 15% efficient modules could be produced from thin poly-Si in a manufacturable, high rate process on low cost substrates.

However, identifying process conditions leading to high efficiency small area thin poly-Si devices is not a sufficient requirement for developing a large area manufacturing technology. It is necessary to develop the science and engineering base to translate a laboratory process to manufacturing equipment. Effectively accomplishing this requires quantitative knowledge of the relationship between reactor geometry and processing parameters, on one hand, and the gas phase reaction chemistry and film growth on the other. The development of thin silicon film solar cells, thus, presents a significant technical challenge that requires expertise in both thin film deposition and solar cell fabrication. To date, thin Si solar cells with efficiencies over 10% have been made on glass substrates using a CVD process with a Si film thickness of less than 2 microns[3].

In this paper, results are presented on the growth of thin Si films deposited by hot wire chemical vapor deposition, HWCVD, a technique that has the potential to meet manufacturing as well as solar cell performance requirements. The relationship between processing parameters and resulting film properties are discussed with respect to gas phase chemistry.

Experimental

Thin silicon films were deposited from pure silane onto 1 in^2 7059 corning glass and single-crystal (100) silicon substrates. The native oxide was not removed from the silicon substrates. The depositions were carried out in a multi-wire HWCVD reactor which allows uniform deposition over a 6x6 $in.^2$ area. The wire material was high purity Ta and its temperature was monitored with a dual-wavelength pyrometer focused onto the wire through a viewport. A quadrupole mass spectrometer with a resolution of 1 amu and a range of 1-512 amu was used to measure the concentration of the gas phase species during deposition. This unit also featured a variable ionization potential which allowed the detection of individual radical species relative to their parent molecule. The depositions were performed at wire temperatures between 1815 to 1850 ^oC and reactor pressures between 25 and 700 mTorr. Independent heating of the substrates allowed the substrate temperature to be varied from 280 to 480 ^oC. The silane conversion, i.e., the silane utilization efficiency, was calculated from the known inlet silane pressure and the outlet silane pressure measured by the mass spectrometer. The film growth rate was obtained both by measuring the film thickness and the weight gain on the substrates. The silicon film crystalline fraction was determined from Raman spectroscopy. Measured spectra were deconvoluted into the characteristic crystalline (520 cm^{-1}) and amorphous (480 cm^{-1}) peaks and the ratio of their areas used to compute the ratio of crystalline to amorphous silicon[4,5]. The films were also characterized by XRD, to determine the grain size and preferred orientation.

Results and Discussion

For both substrates used, the Si films had grain sizes between 10 to 50 nm and displayed a (220) preferred orientation. The crystalline fraction varied from 0 to 89 percent depending on the process conditions. As reported by Dusane et al.[6], these results demonstrate that crystalline films can be deposited from silane without hydrogen dilution. At the wire temperatures used, the conversion of silane as measured by the mass spectrometer was approximately constant, ranging from 90 to 99 percent.

Film deposition in HWCVD proceeds through a series of reactions which occur simultaneously in the gas phase and at the wire and substrate surface. Understanding how this system of reactions is affected by process parameters is a prerequisite to determining the relationship between process conditions and film properties. Table 1 lists a proposed set of reactions leading to Si film formation[7,8]. Although all silane radicals produced by these reactions are expected to contribute to film deposition, it has been widely accepted that SiH_3, having the lowest sticking probability[9], promotes ordered or crystalline films. Therefore, the observation that atomic hydrogen plays an important role in crystalline film formation is reflected in the second reaction where atomic hydrogen provides the pathway for SiH_3 production.

Figure 1 illustrates the effect of silane flowrate at two silane concentrations (pressures). The increase in growth rate with silane flowrate is the result of larger amounts of silane reacting to form larger amounts of radical precursors. As the pressure increases, the concentration of all radical species increases resulting in a higher growth rate. At the lower concentration, the growth rate becomes constant at the highest flowrates. This trend is attributed to a significant decrease in the residence time which leads to a decrease in the silane conversion. At higher pressures, this effect is balanced by the increase in concentration.

Table 1. Reaction system in the deposition of Si films from silane.

Silane cracking: $SiH_{4(g)} \rightarrow Si_{(g)} + 4H_{(g)}$

Hydrogen abstraction: $SiH_{4(g)} + H_{(g)} \rightarrow SiH_{3(g)} + H_{2(g)}$

Disproportionation: $2SiH_{3(g)} \rightarrow SiH_{2(g)} + SiH_{4(g)}$

Polymerization: $SiH_{2(g)} + SiH_{4(g)} \rightarrow$ higher silanes

Film deposition: $SiH_{x(g)} \rightarrow$ film + $(x/2)H_{2(g)}$

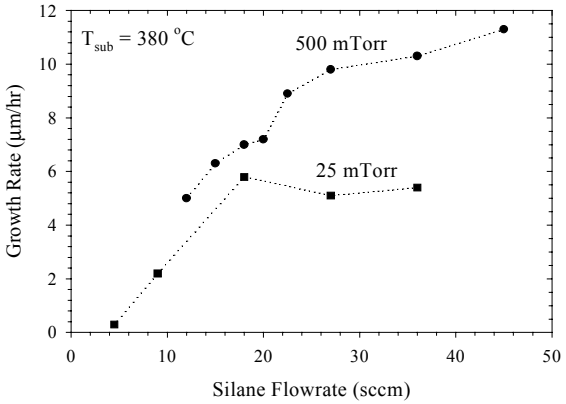

Figure 1. Effect of silane flowrate on the growth rate.

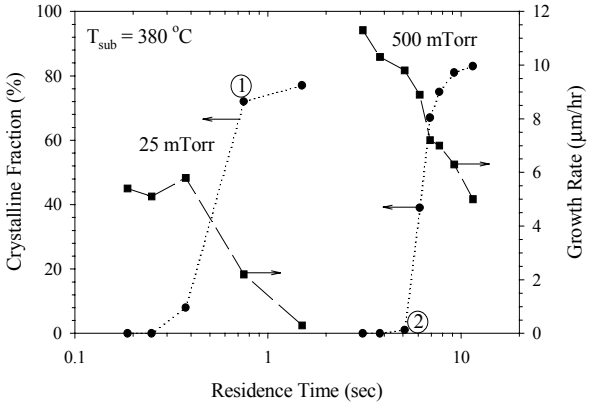

Figure 2. Effect of residence time on the crystalline fraction.

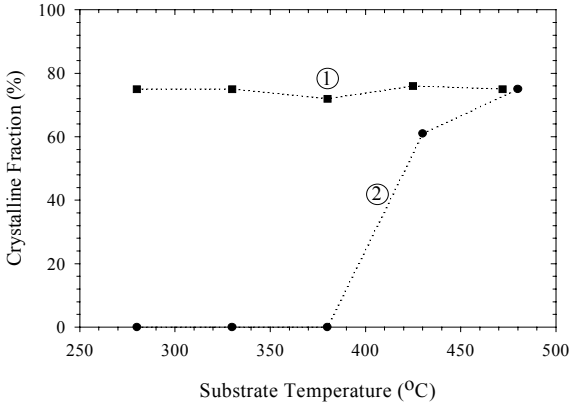

Figure 3. Effect of substrate temperature on the crystalline fraction.

In Figure 2, the effect of residence time on the crystalline fraction is shown. The growth rate was also included for comparison. The residence time is a reactor independent parameter which represents the average time gas phase species spend in the reactor. It is proportional to the ratio of the silane pressure to the silane flowrate. The increase in crystallinity with increasing residence time is related to the sequential nature of the reaction system. Although the above reactions occur simultaneously, their relative importance and that of their products increases serially with increasing residence time. For instance, at low residence times, the cracking reaction is the dominant reaction, and thus, $Si_{(g)}$ is the dominant film precursor. Consequently, films with low crystalline fraction occur. At higher residence times, the hydrogen abstraction reaction becomes an important reaction pathway, shifting the radical distribution in the gas phase to SiH_3 and resulting in films with higher crystalline fractions. For a given residence time, increasing the concentration increases the rates of the disproportionation and polymerization reactions. Since these reactions form SiH_2 and higher silanes, the film crystallinity decreases. As a result, this requires further increases in the residence time to additionally enhance the cracking and hydrogen abstraction reaction and SiH_3 radical production.

Figure 3 shows the dependence of crystalline fraction on the substrate temperature at two different conditions of residence time and concentration labeled 1 and 2 in Figure 2. These

conditions were selected purposely to have starting points of high and low crystallinity, respectively. The effect of substrate temperature on the crystallinity is related to the mobility of the various species adsorbing onto the substrate surface. Not surprisingly, of all the silane radicals, SiH_3 is known to have the highest mobility. However, by sufficiently increasing the substrate temperature, the mobility of other species can be increased to where they also can participate in crystalline film growth. This is the behavior seen in Figure 3. For condition 1, where SiH_3 is the primary film precursor, highly crystalline films are obtained at low substrate temperature, and further gains in crystallinity are not achieved by increasing substrate temperature. However, for condition 2, with low initial crystallinity, there are other species in significant concentrations taking part in the film growth. Since the average mobility of the adsorbates is lower, the crystalline fraction decreases. As the substrate temperature increases, the average mobility of all species increases resulting in improved crystallinity.

Conclusions

Thin polycrystalline silicon films with grain sizes between 10 to 50 nm and (220) preferred orientation were deposited from pure silane onto glass and crystalline silicon substrates. This study demonstrates that highly crystalline silicon films can be deposited without hydrogen dilution. High growth rates can be obtained when high concentrations and flowrates of silane are used. High crystalline fractions result at high substrate temperatures and at concentrations and residence times which lead to relatively high concentrations of SiH_3 radicals.

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THE ROLE OF VACANCIES AND DOPANTS IN SI SOLID-PHASE EPITAXIAL CRYSTALLIZATION

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ABSTRACT

The role and interaction of vacancies and dopants in the crystallization of amorphous Si (a-Si) by solid-phase epitaxy (SPE) was investigated. To this end, we studied: (i) the solid-phase epitaxy rate measured by time-resolved reflectivity (TRR), (ii) the dopant and carrier concentrations measured by secondary ion mass spectrometry (SIMS) and spreading resistance (SR) analysis, and (iii) the vacancy concentration measured by positron annihilation spectroscopy (PAS). Phosphorus was implanted into a-Si on Si (001), which was previously amorphized by $^{29}Si^{+}$ implantation, to create a nonuniform P doping profile. Phosphorus doped samples compensated with similar a boron profile were also studied. Samples were vacuum annealed for various times so that the amorphous-crystal interface was stopped at various depths providing frozen frames of the SPE process. These samples were then studied with PAS to investigate the vacancy population and to identify the impurity-defect complexes. Using this method, we have observed a population of phosphorus-vacancy complexes in the epitaxial layer.

INTRODUCTION

Understanding the mechanisms of dopant-enhanced solid-phase Si crystallization is important in developing an optimum process for low-temperature solid-phase growth of large-grained polycrystalline silicon (poly-Si) thin films on glass substrates for future thin film poly-Si photovoltaic applications. It is well known that dopants like P and B strongly influence the solid-phase crystallization [1], but despite extensive study, the mechanism for dopant-enhanced solid-phase epitaxy (SPE) at high doping concentrations ($\geq 10^{18}/cm^3$) is not well understood.

Kinetic models for the dopant enhancement of solid-phase crystallization have been proposed [2]. In these models, both neutral and charged defects (e.g., dangling bonds, vacancies) could contribute to the amorphous to crystalline silicon conversion. With the addition of dopants, the Fermi level shifts, increasing the population of a certain –but as yet unspecified-- charged defect, and thereby enhancing the growth rate. However, the SPE rate has not been correlated with direct measurements of the concentration of any point defects that could enhance the SPE rate. By using PAS [3] to measure to the vacancy population at various annealing steps, it was possible to probe the relationship between vacancy population and doping effects on SPE.

EXPERIMENT

The samples were designed to have a surface a-Si layer atop a c-Si layer to study SPE, with a doping concentration varying with depth. We studied P-doped Si, P-doped Si compensated with B, and undoped Si for comparison. Float-zone (FZ) Si wafers (<100>, p-doped, 200-300 Ω-cm) were amorphized by ion implantation of ^{29}Si at L-N_2 temperatures. Two implantations, with energies of 70 keV (dose, $2x10^{15}$ at/cm^2) and 200 keV (dose, $6x10^{15}$ at/cm^2), were used to amorphize the surface; ^{29}Si was used to prevent CO and N_2 contamination during implantation. Cross-sectional TEM analysis showed that the amorphized layer thickness was 346 nm. After the amorphization step, the P-doped samples were implanted with P at an energy of 200 keV, and with a dose of $1.3x10^{14}$ at/cm^2; (peak concentration, $7x10^{18}$ at/cm^3). The compensated samples were implanted with both P (above specifications) and B at an energy of 72 keV and with a dose of $1.2x10^{14}$ at/cm^2 (peak concentration, $7x10^{18}$ at/cm^3). TRIM simulations predicted that the peak of the doping profile would occurred approximately at a depth of 300 nm, so the a-Si/c-Si interface would encounter a decreasing doping concentration as crystal growth proceeded.

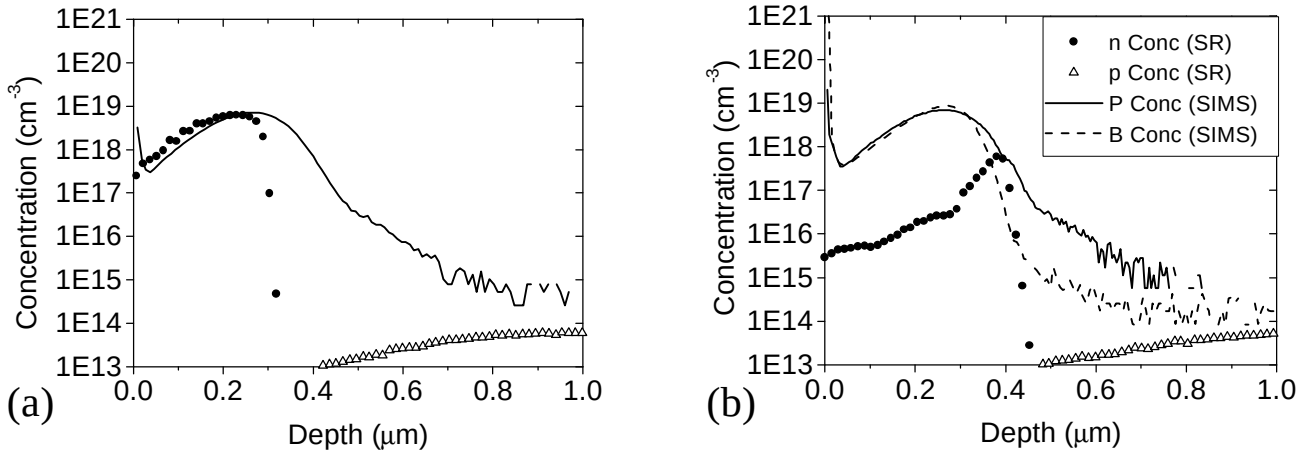

Figure 1. Spreading resistance (SR) and SIMS data for the fully crystallized (a) P-doped sample and (b) P&B-doped sample, annealed at 600°C.

The samples were vacuum annealed (~10^{-6}Torr) on a hot stage at 600°C, and growth was monitored by TRR, using a diode laser (λ=670 nm). The movement of the a-Si/c-Si interface could be monitored via oscillations in reflectivity as the reflections from the surface and the moving interface constructively and destructively interfered. The interface was stopped at different depths, each depth corresponding to a different doping concentration. These samples were analyzed with positron annihilation spectroscopy (PAS) to study vacancy population and to probe the vacancy-impurity complexes. Fully regrown samples were analyzed with SIMS and spreading resistance to determine the total doping and carrier concentration profiles.

In PAS, incident positrons bombard the sample, thermalize and annihilate with electrons in the sample to produce two gamma rays with energies near 511 keV, which corresponds to the rest mass of an electron. Annihilating electrons with nonzero momentum will shift the gamma ray energies away from 511 keV, so annihilations from valence electrons, which have low momentum, produce gamma rays with little shift from the peak at 511 keV. The primary parameter extracted from the energy distribution of the annihilation gamma radiation is the S parameter, which is the ratio of the counts centered at the peak maximum to the whole peak. The S parameter reflects the number of annihilations from valence electrons, which is the most probable annihilation case for positrons in an open volume defect. The S parameter data normalized to FZ Si wafers gives the ratio of open volume defects present in the sample versus clean Si. Using two synchronized detectors, the momentum of the annihilated electron can be resolved. By taking the ratio of the S parameter vs. momentum data for different samples, characteristic peaks are seen, since core electrons of different elements have different momentum. The location of these peaks can be predicted by theory calculations, though amplitude can vary by a factor of two [4, 5].

RESULTS

From the TRR data from fully recrystallized samples, the velocity versus interface depth information was calculated. The P-doped sample had the fastest growth rate, and the compensated sample showed some enhancement. A gradual retardation of the growth rate was observed in all the samples, as well as an additional growth retardation at the surface. The interface velocity slowed from 0.17 nm/s, 0.47 nm/s, and 0.29 nm/s for undoped, P-doped, and P&B-doped Si respectively, to 0.05 nm/s, 0.13 nm/s, and 0.06 nm/s at the surface.

Figure 1 shows the SIMS and SR measurements made on fully recrystallized P-doped and P&B-doped samples. The peak concentration of p and n type carriers coincide in the P-doped Si case, suggesting that the P implant was fully activated. In the P&B-doped sample, the carrier concentration is 2 orders of magnitude less than the dopant profile of P, but not to intrinsic levels, which suggests that the B was not fully activated. This is consistent with the enhancement in the growth rate for the P&B-

doped samples, as compared to the undoped sample. End of range damage from ion implantation can be seen as a drop off of the carrier concentration. We see elevated O concentration at the surface, which correspond well with TRIM simulations of recoil implanted O from a native oxide layer of 20 nm, by implantation of ^{29}Si with the same doses and energies used to amorphize our samples. This elevated concentration of O could be the cause of the retardation of growth at the surface; concentrations of O at 0.5 at % have been observed to retard Si SPE growth by a factor of 0.1 at 550°C [1].

From the positron annihilation spectroscopy data (see Figure 2), several observations can be made. The general reduction of the normalized S (S_N) parameter after the initial anneal implies that some of the defects were annealed out. In the P-doped samples, the shoulder of the curve, seen advancing toward the surface with each anneal, has a shallower slope, possibly due to an increased trapping of positrons, from an increase of negatively charged vacancies from phosphorus-vacancy complexes (P-v), which have been observed in a-Si [6]. The S_N parameter also dipped below one at the surface of all fully crystallized samples, suggesting a contribution from impurities. This is consistent with the recoil implanted O at the surface forming vacancy-oxygen (v-O) complexes [7]. The P-doped sample has a more prominent dip at the surface, which is attributed to an additional phosphorus related effect, though the mechanism is not understood.

The two detector measurements (see Figure 3) show a peak in both the P-doped and P&B-doped samples that corresponds to a P atom in the vacancy neighbor shell, as seen in theoretical calculations. This signal suggests that there are P atoms next to vacancies, and that there are more P-v complexes than would be formed by random distribution of P atoms and vacancies. The P-doped sample has a larger signal than the P&B-doped sample, which is not yet understood [5].

CONCLUSIONS

The interface velocity versus depth was calculated, and a slow retardation was observed for all samples, as well as an additional retardation at the surface, which could be due to recoil-implanted oxygen, which is seen in the SIMS data. The phosphorus was fully activated, but the boron was not, as seen by comparing the spreading resistance and SIMS data. TEM images show that the interface roughness is approximately 10 nm, and there are dislocations extending from the end of range damage. The PAS data suggests that there are O-v complexes in all samples, P-v complexes in the P-doped samples, and vacancy clusters in the end of range region. Further work using positron lifetime measurements and depth profiles will be done to identify the type of open volume defects we have, and to correlate the defect profile with the velocity and dopant concentration data.

ACKNOWLEDGMENTS

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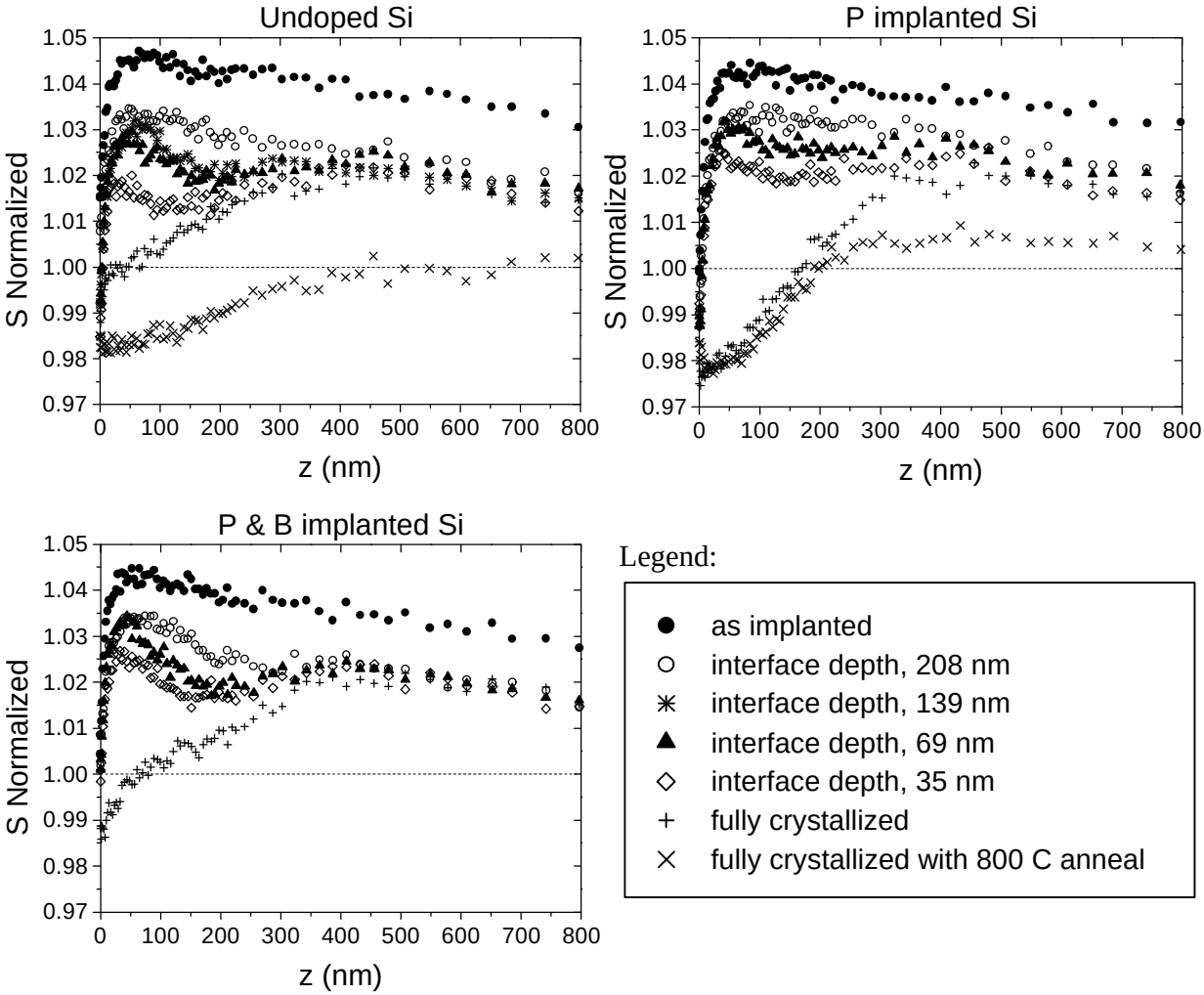

Figure 2. Positron annihilation spectroscopy (PAS) data for undoped, P-doped, and P&B-doped silicon samples. The different curves for each sample include an as-implanted sample (interface at 346 nm), annealing steps with the interface at depths given, a fully crystallized sample, and a fully crystallized sample with an additional 800°C anneal, to anneal out defects in the end-of-range damage region from the ion implantation.

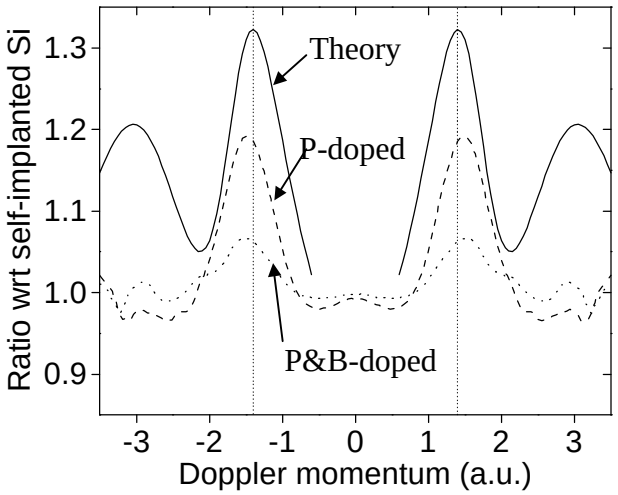

Figure 3. Momentum resolved PAS data for P-doped and P&B-doped Si samples, both divided by the undoped Si data. The resulting data exhibits peaks that correlate with theoretical calculations of P/Si, which suggests there are P-v complexes.

HOT-WIRE CHEMICAL VAPOR DEPOSITION OF POLY-SI IN DILUTED SILANE

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ABSTRACT

A review of efforts underway to explore low temperature polycrystalline silicon thin film growth for solar cell applications is presented. The technique of hot-wire chemical vapor deposition is used, which has produced films with 200-300 Å grain sizes at deposition rates of 2 Å/s. A simplified type of Monte Carlo model is used for making predictions of species concentrations and other pertinent experimental parameters.

INTRODUCTION

The deposition of silicon thin films such as amorphous silicon (a-Si) and polycrystalline silicon (p-Si) at low temperatures has been described as one of the most important technological requirements in the photovoltaics industry [1]. In particular, the technique of hot-wire chemical vapor deposition (HWCVD) has received notice for its ability to create hydrogenated amorphous silicon (a-Si:H) films more stable under light than those created by other techniques. Consequently, such films would be suitable for application in stable a-Si:H solar cells [2]. Given that such films have been shown to be of device quality and low hydrogen content, with growth rates in excess of 5 Å/sec, there exists a possibility for implementing this process industrially [3]. HWCVD is also of interest for growth of polycrystalline Si films at low temperatures for polycrystalline thin film Si photovoltaics.

EXPERIMENT

Figure 1 is a schematic of the HWCVD chamber used in our study. A heated 0.25 mm tungsten wire is used to decompose silane (1% SiH_4 diluted in He), introduced through the gas inlet, into its constituent Si and H atoms; hydrogen is also added when certain deposition conditions are desired. Around this wire region is a shroud made of tantalum that is designed to limit the extent of silicon deposition in other regions of the chamber. Opposite the wire is either a substrate with a resistive substrate heater (for deposition of film samples) or a deposition monitor (for growth/etch rate measurements) at a distance of 0.5 to 4 cm (L). When neither of these two components are installed, a quadrupole mass spectrometer is used for detecting and measuring the gas phase species involved in film deposition. The chamber is also equipped with a reflection high energy electron diffraction (RHEED) gun, used in-situ for determining the crystallographic

structure of the deposited films. Post-growth analysis was performed using transmission electron microscopy (TEM).

SIMULATION

Another component of this work involves the use of a numerical model for the HWCVD process. Specifically, a Direct Simulation Monte Carlo (DSMC) code developed by Bird [4] was modified to include gas-phase chemistry and model gas-phase transport through the ballistic to diffusive regimes. The DSMC technique uses simulation particles, representing groups of molecules, that collide and react with one another to produce collision and reactions rates that are statistically correct. The simulated HWCVD reactor consists of a long wire enclosed by a concentric cylinder substrate; neglecting end effects, mean gas properties are only radially dependent. The reactor is partitioned into annular cells, with the number, identity, momentum, and energy

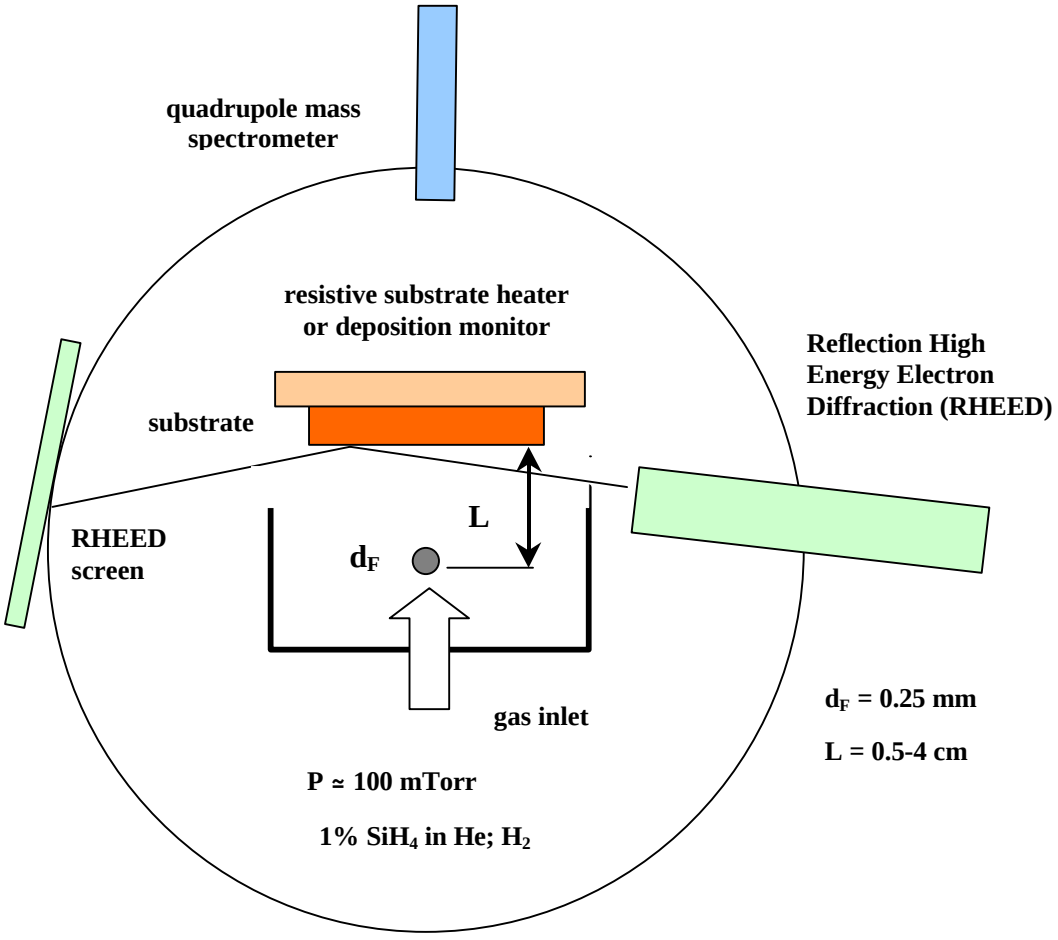

Figure 1: Schematic of HWCVD chamber and associated components

of particles residing in these cells being averaged over many samples to determine these mean gas properties.

RESULTS

Figure 2 shows results obtained with the deposition monitor (a quartz crystal oscillator). The deposition rate was examined under conditions of 100 mTorr SiH_4/He (1% SiH_4), with and without 20 mTorr of H_2, as a function of wire-oscillator distance. The deposition rate appears to have an approximate $L^{-1.4}$ dependence. The flux of growth species should be proportional to the growth rate, suggesting an L^{-1} dependence in the absence of any molecule collisions for this reactor geometry (approximately cylindrical with the shroud in place). The stronger dependence is attributed to collisions of atomic Si incident from the wire with He; the calculated mean free path for a Si-He collision is less than L, while that for a Si-SiH_4 collision is much larger than L, due to the small amount of SiH_4 initially present and the depletion that takes place at the wire.

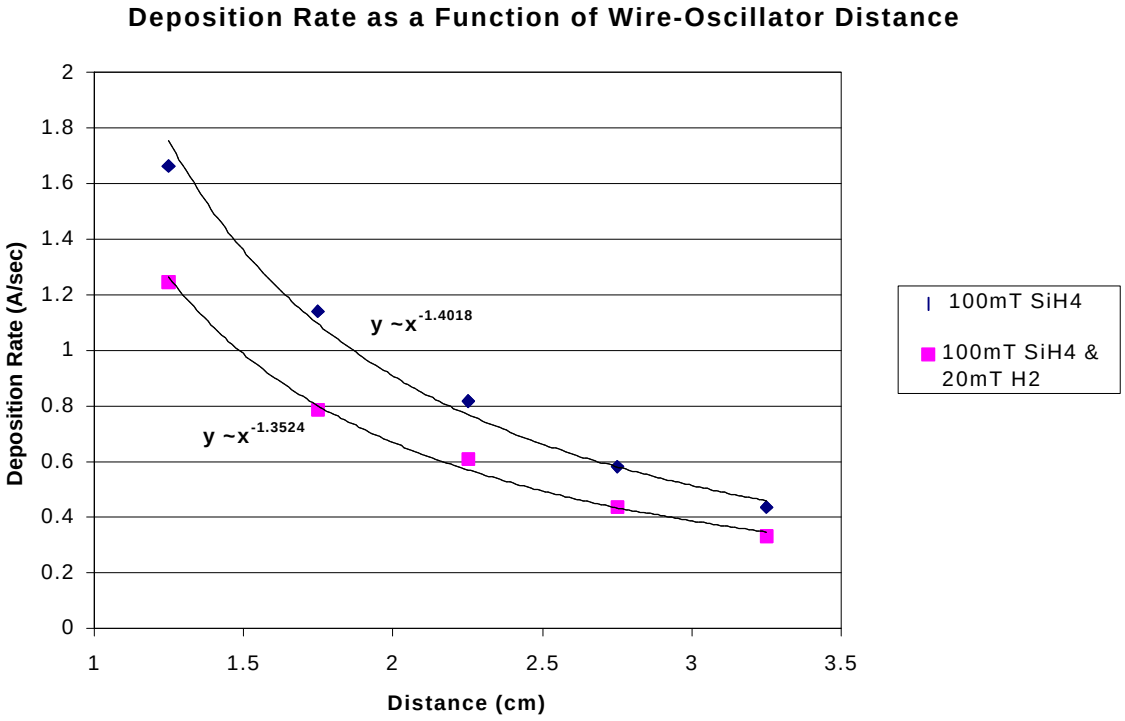

Figure 2: Results obtained with the use of the deposition monitor (quartz crystal oscillator)

Figure 3 shows plan-view and cross-sectional transmission electron microscopy (TEM) images of a film deposited at a substrate temperature of 300°C for 100 mTorr SiH_4/He (1% SiH_4) onto a Si (001) surface. The resulting film was approximately 3500 Å thick, with columnar grains of approximately 200-300 Å and an average deposition rate of 2 Å/sec. Of note in the cross-sectional image is the initial amorphous layer (bottom). This result is likely due to deposition onto a native SiO_2 surface that had not been completely etched away in the hydrofluoric acid solution used in sample preparation.

Questions have long been raised as to the nature of the cracking reaction of SiH_4 on the surface of the tungsten wire. It has been believed that SiH_4 decomposes into SiH_2 or SiH_3. Under both low and high pressure conditions, SiH_3 was thus implicated as an important growth species [5]. To confirm the suspicion, however, that SiH_4 instead decomposes into bare Si and H atoms, measurements were made using the quadrupole mass spectrometer. A peak corresponding to Si was observed (after subtraction of the background nitrogen, also of mass 28 amu), as was a slight H peak (peaks corresponding to H agglomerates H_2^+ or H_3^+ were not seen, and were thought to be unlikely). These results were taken as indicative of the complete dissociation of SiH_4 on the wire. Although mean free path calculations indicated that Si-SiH_4 collisions were unlikely to have occurred and produced Si_2H_x species (x=0-6), the mass range spanning these species was examined. The mass spectra expectedly indicated the absence of any such species.

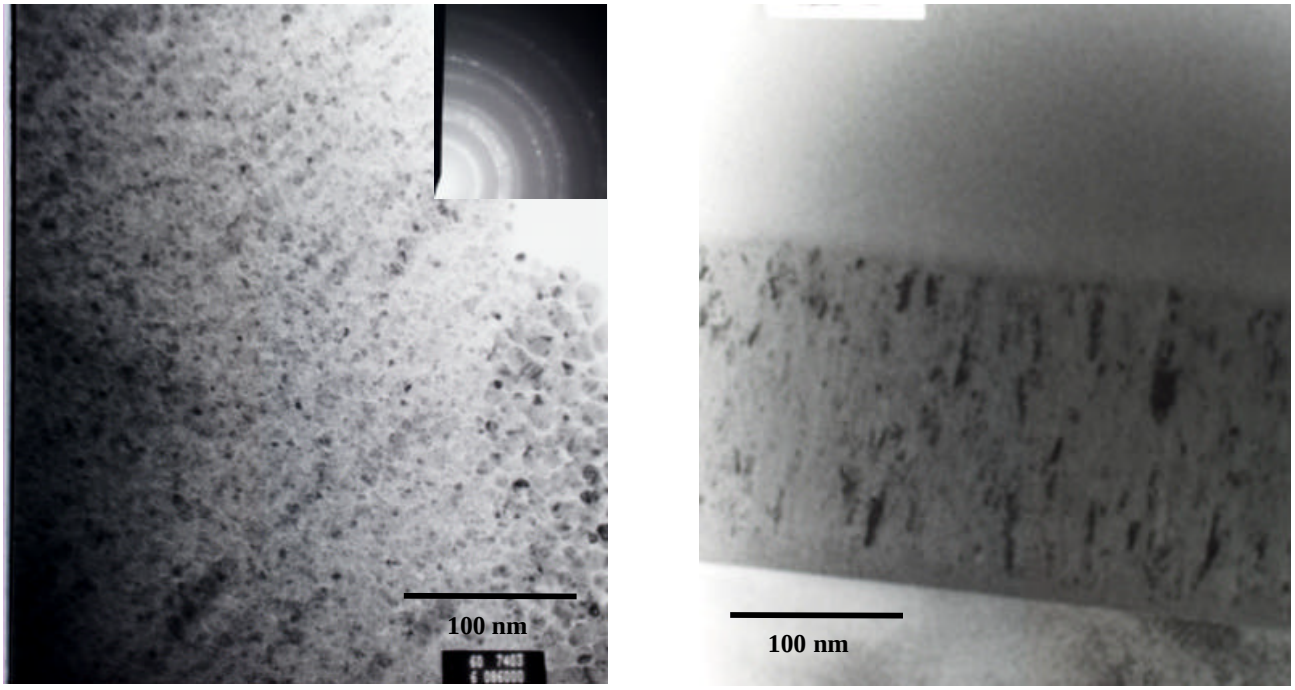

Figure 3: Plan-view (left) and cross-sectional (right) transmission electron micrograph (TEM) images of Si on Si (001).

Although work remains in extending the DSMC model to two-dimensional geometry, the model does reveal some interesting trends. In Figure 4, species profiles are provided under conditions of 300 mTorr total pressure for a 1% SiH_4 in He mixture. Figure 4 indicates that SiH_4 is only slightly depleted under these conditions (approximately 4%), Si atom concentrations decrease precipitously in moving away from the wire, SiH_3 is in low abundance (0.1% of SiH_4) and Si_2H_2 and Si_2H_6 appear to be in significant quantities near the location of the substrate. Under these conditions, it would appear that Si_2H_2 is a possible film precursor. In the lowest energy state of this molecule (hydrogen in bond centered positions), the reactivity should be much less than that of atomic Si [6], a requisite property for high quality films. To model this low reactivity,

Si_2H_2 is assumed to require a dangling on the surface to react, and is assigned a reaction probability of 0.03 (a somewhat arbitrary value which should regarded as uncertain for the present time).

CONCLUSIONS

We have initiated a research program to make quantitative measurements of deposition kinetics in the HWCVD process. The dependence of growth rate on wire to substrate distance is consistent with expectation for linear wire geometry with gas phase collisions. Hydrogen dilution leads to a similar functional dependence with decreased growth rate, consistent with concurrent Si deposition and etching. A continuation of this work will be the measurement of etching rates by atomic hydrogen for different deposition conditions. If hydrogen is initially added to the silane mixture during

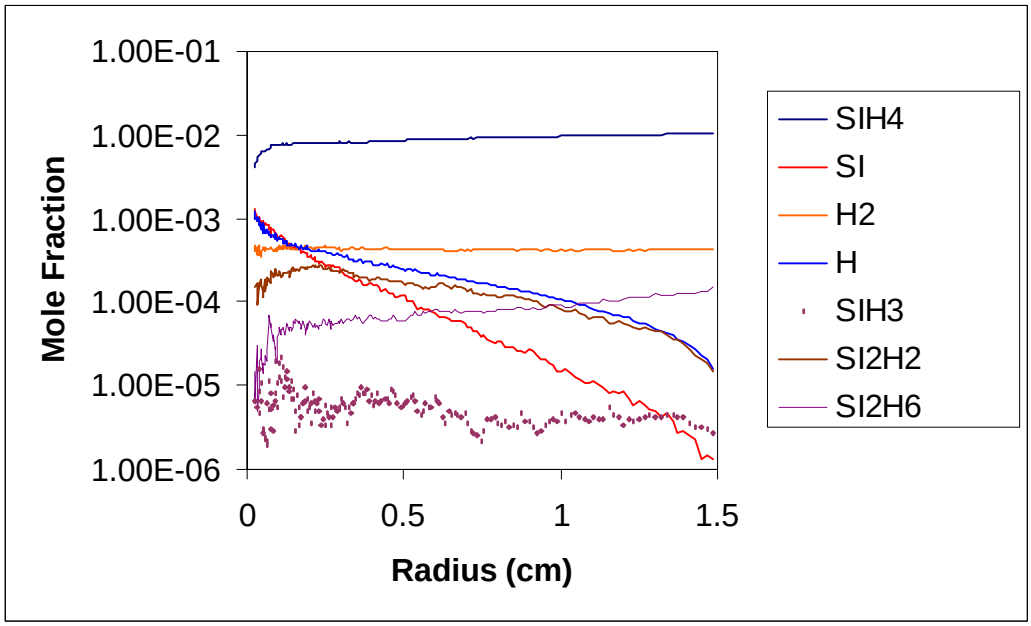

Figure 4: Species profiles obtained from the DSMC simulation under conditions of 300 mTorr total pressure for a 1% SiH_4 in He mixture

deposition, the resulting film is expected to have a higher degree of crystallinity than films deposited with the silane mixture alone (possibility due to etching of amorphous silicon). Consequently, we expect lower etching rates for such deposition conditions, given the lower rate of etching of crystalline compared to amorphous silicon. Deposition rates achieved thus far were approximately 2 Å/s, a limitation primarily due to the use of diluted silane, which is used for safety reasons. It is anticipated that future work will make use of pure silane and consequently allow for higher deposition rates than observed thus far. Mass spectrometry data indicate that silane cracks into its constituent Si and H atoms on the wire, and that in the regime of pressure of the present experiments, little gas phase chemistry occurs, as evidenced by the absence of any Si_2H_x species. Finally, the DSMC model indicates that Si_2H_2 may be an important growth species under particular conditions. As mentioned, work remains in extending the model to two dimensions, obtaining more realistic reaction probabilities and mechanisms, and coupling the model

to a Monte Carlo model of film growth, as opposed to the present use of reactive sticking probabilities.

ACKNOWLEDGEMENTS

The author acknowledges support by the National Renewable Energy Laboratory.

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Defect Density / 10+16
1000
100
10
1
0.370
0.375
0.380
0.385
0.390
Depletion Width (µm)
Sample=1062_13
Temp=347
Freq=10 Hz

Investigation of Undoped and Phosphorus-doped Silver-based Pastes for Self-doping Ohmic Contacts to Silicon for Solar Cell Applications

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Abstract

Undoped and phosphorus-doped Ag-based pastes were applied as spherical contacts to dendritic web n-type silicon. Current-voltage characteristics of as-deposited, 780°C/10 min., 950°C/5 min., and 1000°C/10 min. contacts were evaluated. Annealing above the Ag-Si eutectic temperature yielded silicon precipitation within the silver matrix, resulting in increasing current across the metal/semiconductor system. The contact resistivity was significantly lower for P-doped (< 0.04 Ω-cm^2) than for undoped (1.90 Ω-cm^2) Ag contacts, both of which were annealed at 1000°C. A slower cooling rate from the 1000°C/10 min. annealed condition had the effect of increasing contact resistivity from 1.90 to 5.38 Ω-cm^2.

Introduction

The production of efficient Si solar cells requires the fabrication of ohmic contacts with contact reistivities below 0.01 Ω-cm^2. Metal contacts to silicon substrates for solar cell applications must bond well to the silicon wafer and have good electrical conductivity. Solar cells require a total specific series resistance no greater than 1 Ω-cm^2. The voltage drop across the contact should be minimal as compared to the voltage drop across the bulk material. To achieve sufficiently low contact resistivities, surface dopant concentrations for n-type and p-type Si are typically $\geq 1\times10^{19}$ atoms/cm^3 and $\geq 1\times10^{17}$ atoms/cm^3, respectively.

The use of self-doping contacts allows the elimination of a separate doping step [1]. Self-doped metallization involves the incorporation of a dopant to a substrate through alloying of metal contacts. This process reduces the number of doping steps required of the substrate, thereby lowering processing costs. In a recent study [1], Sb-doped Ag contacts on n-type Si were annealed above the contact/substrate eutectic and quenched to room temperature. The annealing caused the substrate/contact interface to melt, incorporating the dopant into the substrate, creating an ohmic contact at the regrown layer. Boron-doped Al ohmic contacts to p-type Si have also been reported ([2], [3]). In the present study red phosphorus powder was incorporated in an Ag-based paste and investigated as a self-doping contact to n-type Si.

The Ag-Si system exhibits a eutectic at 835°C. Annealing temperatures above (900°C, 1000°C) and below (780°C) the eutectic temperature were employed. Silicon exhibits negligible solubility in silver. All of the Si that reacts with Ag to form a molten

phase at temperatures above 835°C will therefore precipitate out of the Ag phase when cooled. The maximum solubility of P in Ag is estimated to be 0.07 atomic percent [4].

Experimental Procedure

Several n-type single crystal, dendritic web Si samples of <111> orientation were grown at Ebara Solar, Inc. The samples were 100 μm thick and had a resisitivity of 20 Ω-cm. The Si was ultrasonically cleaned in acetone, methanol, and isopropanol, and dipped in an aqueous 10% HF solution. A fritless Ag-based (~70 at. % Ag) paste obtained from DuPont Electronic Materials (#E89372-119A) was used for the circular contacts on the Si substrates. Contact diameters ranged from 0.8 to 1.3 mm. Some of the contacts were doped with pure red P powder, in an estimated amount of 0.07 atomic percent. An as-deposited silver contact cross section is shown in Figure 1.

The samples were pre-annealed in air at 150°C for 20 minutes to remove solvents from the Ag paste. Samples were subsequently annealed in an Ar environment, at 780°C/10 min., 900°C/5 min., and 1000°C/10 min., and cooled at an estimated rate of 8°C/min. Another test sample was heated to 1000°C and cooled at a controlled rate of 2°C/min to 800°C. Current-voltage (I-V) measurements were performed with an HP 4155B Semiconductor Parameter Analyzer to evaluate electrical properties of doped and undoped samples.

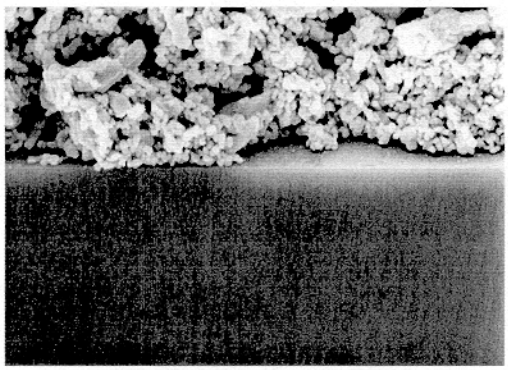

Figure 1. Scanning electron microscope (SEM) image of an as-deposited Ag contact (top) on Si substrate (bottom); 3727X.

Results and Discussion

The Ag paste employed in this study has a fine particulate appearance in the as-deposited state. Annealing the paste causes a coalescence of the particles. A 780°C/10 min anneal (below the 835°C Si-Ag eutectic) resulted in a contact that contains pores (Figure 2). The pores are most likely the consequence of residual resins evaporated during the annealing treatment. Current-voltage measurements showed that the sample annealed at 780°C was less resistive than the as-deposited sample (Table 1, Figure 6). The decrease in contact resistivity is attributed to the coalescence of the Ag particles, and an enhanced interaction with the Si substrate.

A 900°C and 1000°C anneal caused Si precipitation within the Ag contact, as indicated by energy dispersive x-ray (EDX) analysis. A SEM image of a contact annealed at 1000°C for 10 min. is shown in Figure 3. The samples annealed at 1000°C/10 min exhibited ohmic behavior, with the contact resistivity reaching values of

1.90 Ω-cm^2 for undoped Ag and < 0.04 Ω-cm^2 for P-doped Ag contacts (see Table 1). The I-V characteristics for the doped and undoped contacts are compared in Figure 4. These results clearly show the beneficial effect of the P dopant on the ohmic behavior of the Ag contacts.

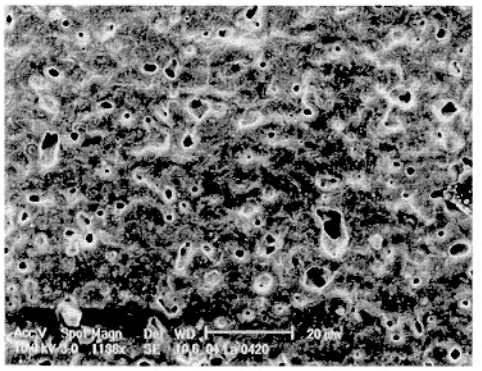

Figure 2. 780°C/10 min annealed Ag contact; 1138X.

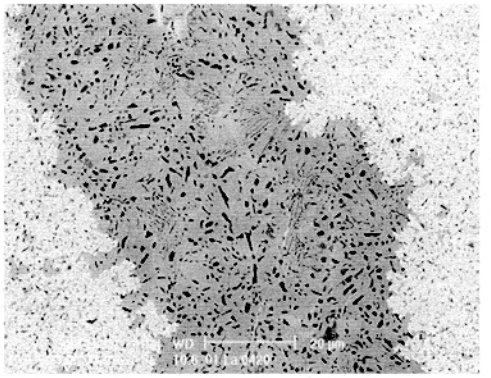

Figure 3. 1000°C/10 min annealed Ag contact; 1136X. Silicon (black), silver (gray), oxide (white).

Table 1. Current-voltage characteristics and estimated contact resistivities for doped and undoped Ag-based contacts with annealing conditions as specified.

Contact	*Annealing Treatment*	*Contact Resistivity (Ω-cm^2)*	*Behavior*
Ag	as deposited	~ 935	leaky diode
Ag	780°C/10min + estimated cooling *	~ 95	semi-ohmic
Ag	900°C/5min + estimated cooling *	~ 10	semi-ohmic
Ag	1000°C/10min + estimated cooling *	1.90	ohmic
Ag:P	1000°C/10min + estimated cooling *	< 0.04	ohmic
Ag	1000°C/10min + controlled cooling**	5.38	ohmic

* *Estimated initial cooling rate of 8°C/min.*
** *Controlled cooling rate of 2°C/min for the first 200°C*

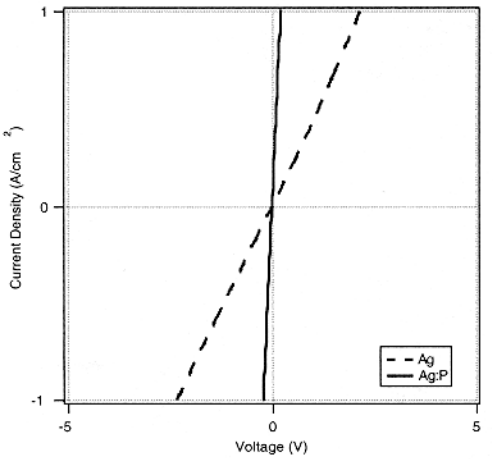

Figure 4. Current density measurements of P-doped and undoped Ag contacts to Si (1000°C/10 min).

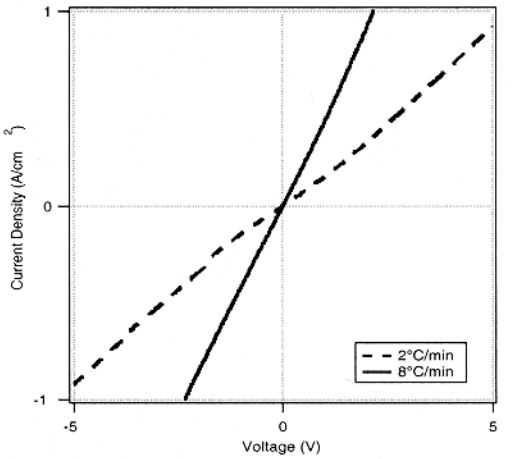

Figure 5. Current density measurements of ~8°C/min. and ~2°C/min. Ag contacts cooled from 1000°C/10 min.

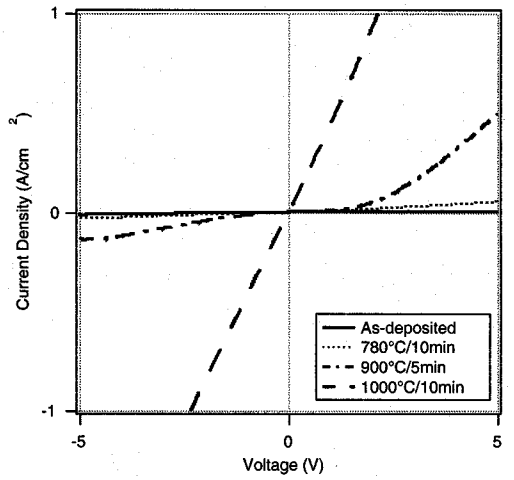

Figure 6. Current density measurements of Ag contacts to Si.

In comparing cooling rates from a 1000°C annealing temperature, slower cooling rates increased electrical resistivity (Table 1 and Figure 5). Samples cooled at 8°C/min. yielded a contact resistivity of 1.90 Ω-cm^2 as compared to 5.38 Ω-cm^2, for the samples cooled at 2°C/min. Good ohmic contacts were formed by cooling from the annealed condition as quickly as possible. A possible reason for this is that the Si/Ag interface may be highly disordered as a result of the rapid cooling rate. Such disorder could lead to defect levels in the Si bandgap which give rise to ohmic behavior.

Conclusions

Annealing at temperatures above the Si-Ag eutectic causes the elements to melt and react. It is believed that liquid phase epitaxy regrowth of the Si occurs with incorporation of P from the P-doped contacts. The incorporation of P in the Si lattice should result in a highly-doped n-type region, which should enhance ohmic behavior, in agreement with present results. Reaction of the Ag and Si, as well as rapid cooling from annealing temperatures above 835°C, and incorporation of dopants, contribute to ohmic behavior. Self-doping Ag contacts eliminate separate doping steps, reducing processing costs. The doped contact resistivity values calculated for the P-doped contacts satisfy the resistance criteria required by the solar cell industry.

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PROCESS OPTIMIZATION AND CONTROL OF A PHOTOVOLTAIC MANUFACTURING PROCESS

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Abstract: The use of least squares regression to develop an empirical model of post diffusion sheet resistance into solar cell efficiency with subsequent development of specifications and a process control scheme is discussed. Complementing the modeling, is the use of an on-line process capability and control system affording the enhanced process visibility necessary for high volume production. The effect of the optimization and control strategy on the quality of the solar cells produced is examined.

Introduction

Process optimization involves moving a manufacturing system to a state of order, at which the system operates at its most efficient, producing some optimal result with a minimum expenditure of resources. Process capability and statistical process control are measures of the compliance of the process to the optimum state[1]. The timely delivery of statistical metrics describing the manufacturing process performance is the prerequisite to maintaining the optimized system. Many quality professionals believe the meaningful nature of the metrics is predicated on the development of empirical models which serve to estimate the relationship between an individual metric of performance and the ultimate response. In a high volume production environment, the ability to develop optimized, capable and controlled processing is the prerequisite for success[2].

Why Capability and Control in Photovoltaic Processing?

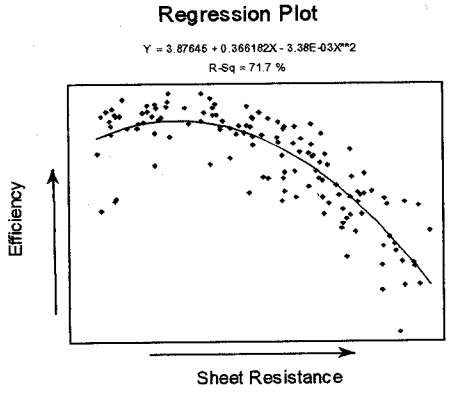
Consider the disparity between laboratory and production cell efficiencies.

Highest lab efficiency CZ single crystal[3]	19%
Typical production efficiency	13-15%

Even within the range of typical CZ production efficiencies, the difference between 13% and 15% solar cells can seriously impact the profitability of a photovoltaic manufacturer. Understanding the departures present in the manufacturing process that result in substantial efficiency losses, then optimizing and controlling the individual processes responsible, is paramount to being a viable manufacturing entity.

Empirical Modeling of a Critical Solar Cell Processing Variable

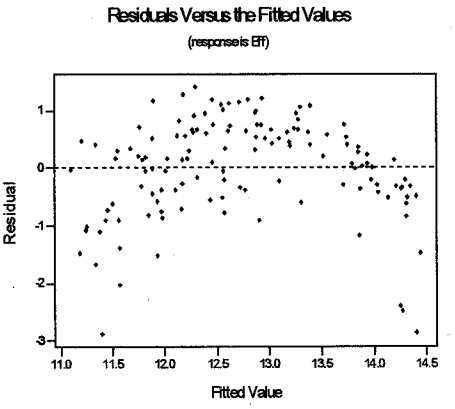
Consider the regression plot of post diffusion sheet resistance vs cell efficiency. The data points represent averages of four adjacent cells generated in multiple diffusion runs.



These data are the product of a designed experiment that varied the diffusion process parameters. Material was randomized prior to diffusion and a strategy of randomizing against, blocking on, or holding constant, potential confounding variables between diffusion and electrical test was sufficient to develop a useful model. A cursory examination of the approach used to develop this relationship is as follows.

The regression plot, shown adjacent, displays a common approach to empirical modeling, the development of the first order model using simple linear regression. The models ability to explain the variation in the data is being given by the R-sq.

Efficiency = 17.6 - 0.0728 ShtRes R-Sq = 54.5%



Many practitioners of regression use residual analysis to determine the models adequacy. The residual vs fitted value plot, shown adjacent, compares the residuals, the actual value minus the fitted or predicted value, to the fitted value. This approach clearly displays the need to fit the second order model as evidenced by the curvature present. A truncated version of the final analysis appears below.

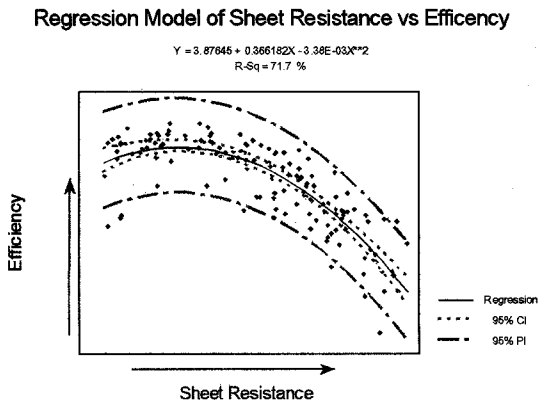
Efficiency = 3.88 + 0.366ShtRes-0.00338 ShtRes^2

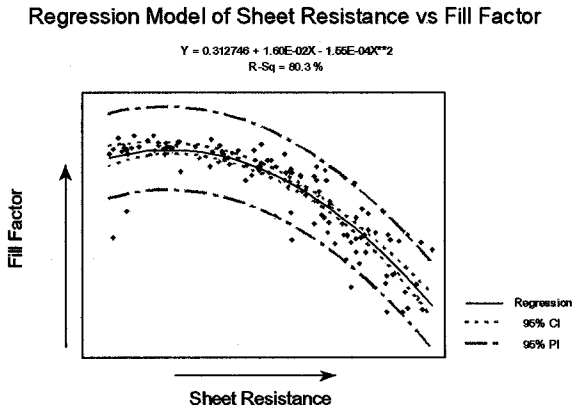
Predictor	Coef	StdError	T	**P-value**
Constant	3.876	1.572	2.47	0.015
ShtRes	0.36618	0.04960	7.38	0.000
ShtRes^2	-0.0033786	0.0003801	-8.89	0.000

R-Sq = 71.7%
R-Sq (adj) = 71.3%
S = 0.6792

The P-value indicates the probability of the test statistic, **T= Coef/StdError** taking on a value at least as extreme as the observed value when the associated coefficient is in fact zero[4]. It is rejected if it is more extreme than a critical value from a t distribution whose shape is defined in part by the model being fit[4]. The coefficient of multiple determination, R-Sq, is supplemented by the **R-sq(adj),** as the common R-sq will continue to increase even with non-significant terms entered in the model[5]. **S**, the square root of the error mean square, a measure of unexplained variation in the data, is also included as a metric of model performance[6]. One among many, applicable to this analysis.

The relationship is well approximated by the second order model with one independent variable. The causal link for the efficiency movement is illuminated with a regression plot relating fill factor to post diffusion sheet resistance. Overlaying a confidence interval, delineating a reasonable range of values the ***mean*** could take on and a prediction interval, similarly indicating a reasonable range ***individual*** values could fall in, completes the bulk of the analysis presented here. Both plots follow.

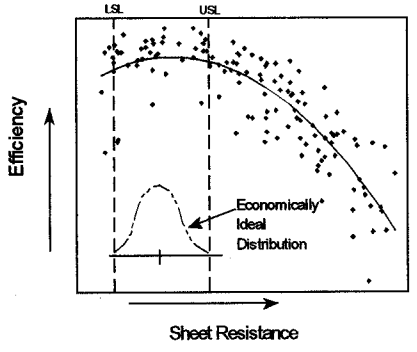




While the development of these models is naïve from the standpoint that the interrelation between processing steps is not represented. The model is a useful predictor for a stable photovoltaic process as it affords a good approximation of the current status.

It should also be noted that the model building approach and analysis discussed here was truncated from the actual in the interest of brevity. For more information one should refer to [4], [5], and [6] at a minimum.

Deriving of Specifications for the Best Economic Process



The regression plot adjacent now displays the specification limits derived from both the regression model and the costs of the raw material, labor and other expenditures associated with the phosphorous diffusion process. As the post diffusion sheet resistance departs from the optimum, electrical performance is degraded. When this reality is considered in light of the costs associated with the phosphorous diffusion process, the departure becomes unacceptably costly only beyond the specification limits. However, even modest departures from the optimum, can cause substantial losses in cell performance. That reality forms the basis for the use of capability metrics and control charting to prevent costly distributional departures.

Process Capability and Control

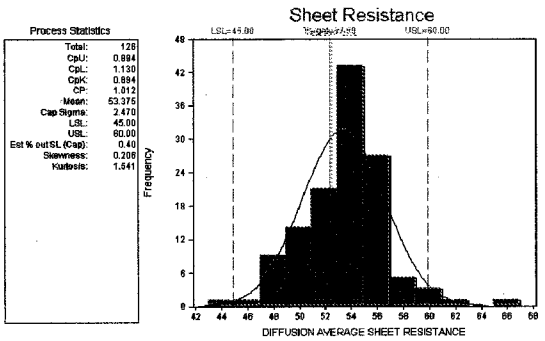
The standard process capability metrics are given by:

CPU = (USL- mu) / 3(sigma) CPL = (mu -LSL) / 3(sigma)

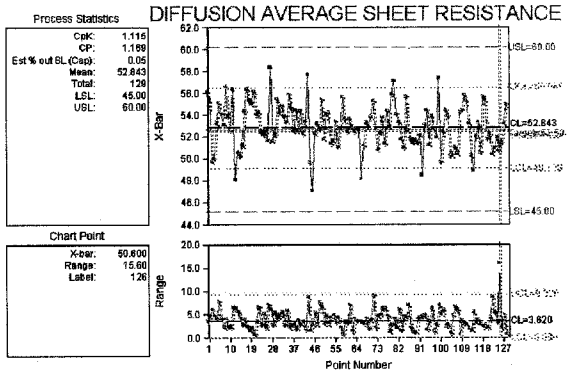
CP = (USL-LSL) / 6(sigma) **Cpk = min{CPU, CPL}**

Where USL and LSL are the upper and lower specification limits respectively. CPU and CPL represent the process capability with respect to the upper and lower specification limits. The CP index is comparing the process distribution to the specification limits without regard to the location of mu. The Cpk considers the dispersion and location of the distribution relative to the specifications.

The histogram of diffusion tube 51, shown adjacent, will illustrate. The **Cpk** metric, .894 in this case, is reduced by the departure from the center of the specifications or target. The Cp metric of 1.012 is an indication of what the Cpk could be if the process mean were on target. The CPU and CPL metrics diagnose the nature of the off target distribution. Average sheet resistance is too high, as evidenced by the low CPU and distribution shifted toward the USL.

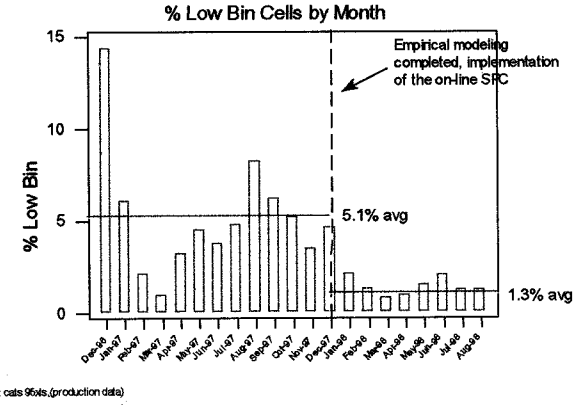


The histogram and statistics provided are part of an ***on-line statistical process control system***[7] being constructed at the Siemens facility. The user may also view control charts as desired from many locations in the facility. The Xbar and Range chart from diffusion tube 53 is shown adjacent. In this case, the process is displaying a reasonable state of statistical control with relatively few data points beyond the control limits, the boundary beyond which examination of the process should take place.



The Effect on Cell Performance

The graph adjacent illustrates the beneficial effect of the empirically derived specifications coupled with the improved visibility on the process the on-line SPC has provided. The graph shows the tail of the electrical distribution, or low bin, has been reduced substantially. A product of the on target with low variation, post diffusion sheet resistance distribution.



The use of state of the art information technology to monitor processes and fundamental industrial statistics has led to the largest improvements in quality in the company's history with the promise of greater benefit in the future. It is part of a multifaceted effort to integrate statistical tools and thinking into the daily activities of the work force.

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Modeling a Dry Etch Process for Large-Area Devices

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INTRODUCTION

There has been considerable interest in developing dry processes which can effectively replace wet processing in the manufacture of large area photovoltaic devices. Environmental and health issues are a major driver for this activity because wet processes generally increase worker exposure to toxic and hazardous chemicals and generate large volumes of liquid hazardous waste. Our work has been directed toward improving the performance of screen-printed solar cells while using plasma processing to reduce hazardous chemical usage [1].

The self-aligned selective-emitter (SASE) plasma-etchback and passivation process incorporates a sequence of three plasma treatments. Cells which have received standard processing through the printing and firing of gridlines undergo reactive ion etch (RIE) with an SF_6 plasma to etch away the most heavily doped part of the emitters. This is followed by a plasma deposition of silicon nitride and an ammonia plasma passivation step.

We have been developing plasma models to simulate each of these processes in sufficient detail that they can be used for process development and control. Reported here is the modeling of the SF_6 RIE plasma. In order to refine the chemical mechanism, a variety of diagnostic measurements were performed on the SF_6 plasma, including silicon etch rates, mass spectrometry probes, Langmuir probe measurements of ion saturation currents, and gas temperature with fluoroptic probe.

DESCRIPTION OF THE CALCULATIONS

The plasma simulations were done using the computer code AURORA [2], which employs CHEMKIN [3] and predicts the steady-state properties of a reactor for plasma chemistry systems. Our approach to plasma modeling is to incorporate all the known chemistry and physics, and make best estimates of the unmeasured, but expected chemistry. For example, much of the plasma behavior is governed by electron collisions with SF_6. We rely heavily on cross section measurements [4,5,6] for the many channels such as ionization to give SF_5^+, SF_4^+ etc., fragmentation to give SF_5, SF_4, etc., attachment to give SF_6^-, and vibrational and electronic excitation of the SF_6. The cross sections (σ) are measured vs. electron energy, and the predicted rate of a given reaction is calculated as the overlap of the electron energy distribution and the σ vs. E curve. We convert the reported σ data into Arrhenius form for computational ease. This introduces a small error which is deemed negligible relative to uncertainty in the actual electron energy distribution in the plasma.

Reaction rates for the neutral reactions are very poorly known. Fortunately, the low densities of radicals in the plasma, and low total pressure result in relatively minor contribution from many of the expected radical-radical reactions. Three-body recombination reactions such as F + F + M = F_2 + M (where F is fluorine and M represents any third body molecule) are expected to play a role even at these reduced pressures. The 3-

body rates which have been reported are typically not obtained using SF_6 as M. Therefore, it is necessary to estimate the contribution from the many potential 3-body reactions.

The importance of fluorine-based plasmas to etch silicon has led to some good fundamental work on the surface reactions of F atom on silicon. Our surface mechanism proposes a predominant reaction of F atoms with surface silicon to give SiF_2 groups and then further reaction to eliminate SiF_4 gas similar to the treatment of Flamm [7]. Ion assisted etch is included explicitly by allowing each positive ion to remove SiF_4. The calculation distinguishes reaction at the chamber walls from silicon and uses a F atom wall recombination rate based on that estimated by Ganguli et al [8] but adjusted for best fit.

Our model incorporates 27 gas phase species including neutrals, electrons, positive and negative ions and a reaction mechanism with 138 gas-phase and 26 surface reactions.

EXPERIMENTAL

Etching of photovoltaic cells, and most diagnostics are done on a PlasmaTherm 790 reactor which is a parallel-plate system operating at 13.56 MHz. The reactor was instrumented with a differentially pumped mass spectrometer which probes the plasma gas directly with minimum wall recombination. Mass spectra are obtained for a range of power and pressure conditions with and without a silicon wafer in place. A Langmuir probe is used to obtain ion saturation current for a range of plasma conditions. In order to determine the silicon etch rate, 100 mm patterned wafers are etched and measured with profilometry at five locations. No significant radial non-uniformity of etch rate is observed.

On a separate research reactor, also capacitively-coupled, parallel plate and 13.56 MHz, the gas temperature of the SF_6 plasma was measured by fluoroptic probe. The reactor geometry is adjusted in the model calculations to allow comparison with this data.

RESULTS

We have developed a plasma chemistry model which gives a reasonably good fit to the data sets. Figure 1 shows a comparison of the etch rate data measured to the calculated rates graphed vs. pressure for five plasma powers. The overall trends are reproduced quite well, with a peak in etch rate observed at high power and intermediate pressure. At low power, the etch rate falls rapidly with increasing pressure. The model explains this falloff as due to electron capture by SF_6,

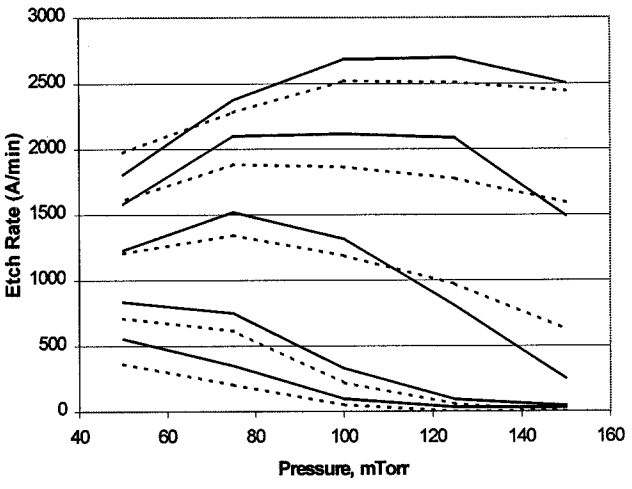

Fig. 1 Etch rate of silicon in SF_6 plasma. Experiment (solid lines) compared to model calculation (dashed lines). Curves are shown for powers (top to bottom) 100, 75, 50, 25, and 15 Watts.

depleting electrons so strongly, that the plasma is almost extinguished. In fact, at the highest pressures and low power, the calculation fails to converge because all

electrons are captured by SF_6 and no plasma solution can be found.

The overall shape of the etch curves is predominantly the result of changes in the electron density, N_e, and temperature T_e. At high power and low pressure, N_e is highest but T_e is low. As pressure increases, N_e falls due to capture of electrons by SF_6, and T_e increases as the rf power is coupled to fewer electrons. The increase in T_e leads to an increased production of F atoms from electron impact on SF_6. Eventually at high pressure, the loss of electrons to form negative ions dominates and F concentration falls. At low power (15 Watts), electron capture and negative ion formation are already significant at the lowest pressure, 50 mTorr, and etch rate decreases monotonically with increasing pressure.

While overall trends in the etch data are determined by electron-SF_6 collisional phenomena, at high pressure and low power the calculation becomes sensitive to almost every reaction in the model. As N_e falls, small changes in any rate constant lead to major changes in N_e and T_e and hence the F atom density and etch rate. This effect probably will correspond to instability and difficulty in achieving reproducible etch rates. Small changes in wall cleanliness or temperature, for example, would be expected to influence etch rate. The model suggests that for manufacturing robustness, the plasma etch process should be operated in a parameter regime away from this instability boundary.

Figure 2 shows three graphs comparing plasma diagnostic measurements to the calculation. The agreement is not perfect, but the trends and magnitudes are reproduced quite well. Although the gas temperature measurements were obtained on a different reactor with much smaller plasma volume, and hence higher power volume-density, the agreement is quite good. The break in the measured temperature above 40 watts is accompanied by a visual change in the plasma emission, and probably represents a reduced power density as the plasma volume increases.

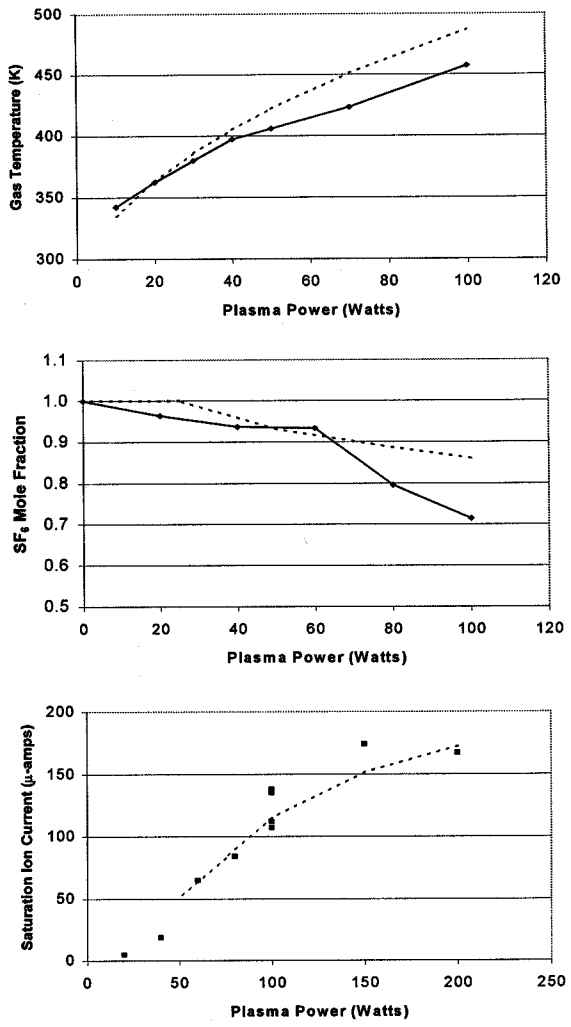

Figure 2. Comparison of calculation (dashed line) with experiment. Top: Fluoroptic probe measurement of gas temperature. Middle: Mass spectrometry measurement of SF_6. Lower: Langmuir probe measurement of ion saturation current.

For a comparison with mass spectrometer measurements any of several masses could be used, but the SF_6 mole fraction is the most

direct, because fragmentation patterns in the ionizer can be calibrated directly. Trends in other mass signals corresponding to the radicals SF_4 and SF_2 are used for fitting, but absolute densities of these species are less certain.

In order to compare the ion saturation current measurements, the calculated density of all 8 positive ions is used with the calculated T_e, and the Bohm velocities, v, for each ion, and the formula $I_{sat}=N_i *e*v$. Agreement with the measurements is quite good.

SUMMARY

We have studied a dry process for plasma-etchback of the emitter in full-size multicrystalline silicon cells. The plasma is pure SF_6 in a capacitively-coupled parallel plate commercial reactor. Plasma diagnostic measurements include etch rates, Langmuir probe measurements of ion saturation currents, mass spectrometric probes of the plasma gas and gas temperatures. A plasma model is developed and tested against these data. We obtain reasonable agreement with the measurements. From an analysis of the model explanation for the fall-off in etch rate at high pressure, we conclude that the plasma is likely to become very sensitive to minor system perturbations at high pressure and low power. Operation in this regime is liable to result in reduced process stability and reproducibility. Further refinement of the model will be possible as more kinetic data and diagnostic measurements become available, however the current model should be reliable enough to guide process scale-up and optimization

ACKNOWLEDGEMENTS

The authors would like to acknowledge many useful discussions with Dr. Pauline Ho on approaches to mechanism development, and Dr Ellen Meeks for initial work on the mechanism. We also appreciate the valuable technical assistance of David Fein in obtaining the plasma gas temperatures.

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Plasma Texturing of Silicon Solar Cells

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INTRODUCTION

Surface texture promotes enhanced light absorption in Si solar cells. The quality of lower cost multicrystalline-silicon (mc-Si) has increased to the point that its cell performance is close to that of single c-Si cells, with the major difference resulting from the inability to texture mc-Si affordably. This has reduced the cost-per-watt advantage of mc-Si.

Surface texturing aimed at enhanced absorption in Si has been historically obtained by creating multimicrometer-sized pyramids using anisotropic wet etchants on single-crystalline silicon that take advantage of its single crystalline orientation. Since the surface feature sizes are several times the length of the incident solar wavelengths involved, the optical analysis of the reflected and absorbed light can be understood using geometrical optics. Geometrical textures reduce reflection and improve absorption by double-bounce and oblique light coupling into the semiconductor. However, geometrical texturing suffers from several disadvantages that limit its effectiveness. Some of these are listed below:

a) Wet-chemical anisotropic etching used to form random pyramids on <100> crystal orientation is not effective in the texturing of low-cost multicrystalline wafers,
b) Anti-reflection films deposited on random features to reduce reflection have a resonant structure limiting their effectiveness to a narrow range of angles and wavelengths.

Various forms of surface texturing have been applied to mc-Si in research, including laser-structuring, mechanical grinding, porous-Si etching, and photolithographically defined etching. However, these may be too costly to ever be used in large-scale production. A Japanese firm has reported the development of an RIE process using Cl_2 gas, which textures multiple wafers per batch, making it attractive for mass-production [1]. Using this process, they have produced a 17.1% efficient 225-cm^2 mc-Si cell, which is the highest efficiency mc-Si cell of its size ever reported. This proves that RIE texturing does not cause performance-limiting damage to Si cells. In this paper, we will discuss an RIE texturing process that avoids the use of toxic and corrosive Cl_2 gas.

EXPERIMENTAL PROCEDURE

A low-cost, large area, random, maskless texturing scheme independent of crystal orientation is expected to significantly impact terrestrial photovoltaic technology. We propose an approach based on randomly etched Si nanostructures formed using reactive ion etching (RIE) that creates subwavelength structures whose properties are explained by physical optics. Enhanced light absorption in these nanostructures may be explained by a waveguide mechanism based on $\lambda/2n$ feature sizes, where λ is the light wavelength and n is the Si refractive index. Figure 1 shows three examples of these highly absorptive Si nanostructures formed by three different RIE process variations.

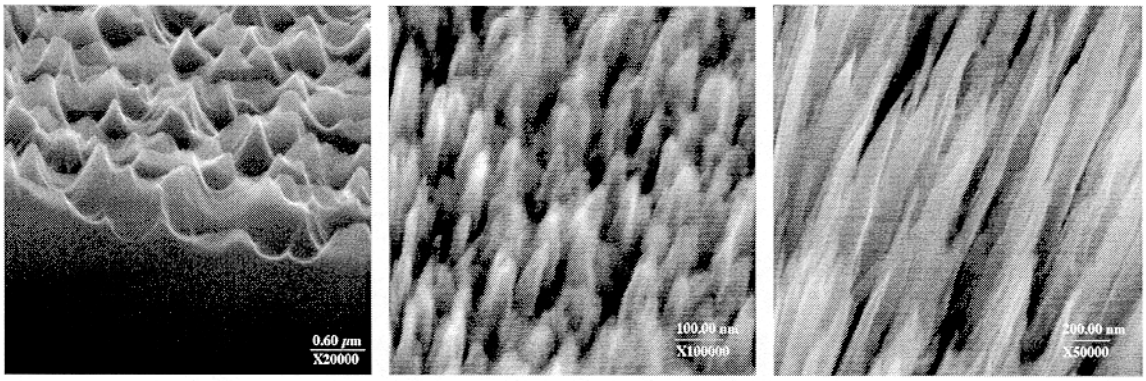

Figure 1. SEM pictures of different types of Si nanostructures formed by RIE process variations on single-crystal Si wafers, large 0.1-0.6 μm pyramids (left), small pyramids 0.02-0.05 μm (middle), and needles 0.03-0.07 μm (right).

These surfaces appear almost black to the eye, and a measurement of absolute hemispherical reflectance shows a broadband minimum below 2% for most of the usable portion of the solar spectrum. Fig. 2 shows hemispherical reflectance measurements for the three surfaces shown in Fig. 1. The lowest spectral reflection is from the small pyramids. The larger pyramids and needles have a more wavelength-dependent reflectance. The reflectance of polished Si is also plotted for comparison. These RIE texturing techniques have also been demonstrated uniformly over 130-cm^2 mc-Si wafers. A reflectance measurement from a mc-Si wafer is shown in Fig. 3.

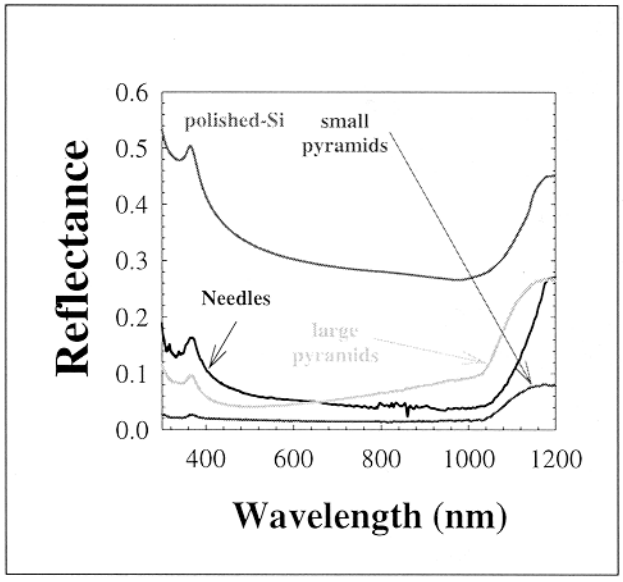

Figure 2. Hemispherical reflectance measurements of the RIE-textured surfaces without AR coatings shown in Fig. 1.

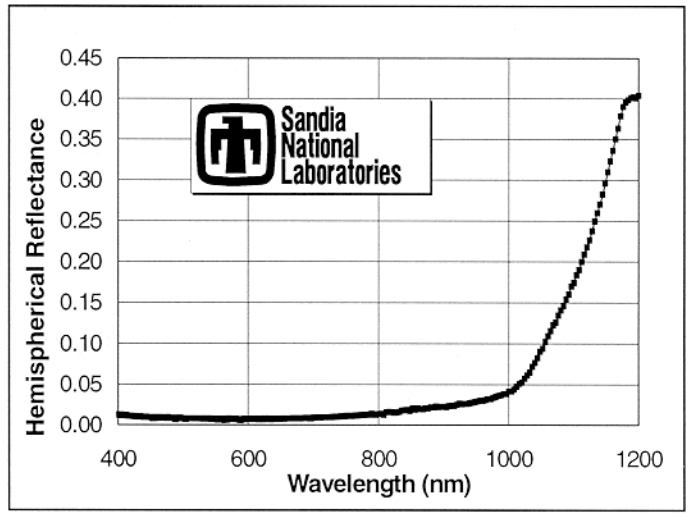

Figure 3. Hemispherical reflectance of a mc-Si wafer textured using a Cr-assisted RIE process. The reflectance reaches a broadband minimum below 1%.

The nanotexturing process used in this research involves the use of metallic catalysts, which alter the etching process in a dramatic fashion compared to what can be obtained without them. This enables a highly uniform texture to be obtained within a wide process window. The proposed

process results in a mc-Si cell with textured feature dimensions much smaller that the wavelength of the incident light. This optically modified layer operates in a regime with characteristics fundamentally different than the traditionally more accessible geometrical regime. With subwavelength fabrication technology, we can intentionally create a layer of a tailored index of refraction, spanning the range defined by the refractive indices of air and silicon. This allows us to fabricate an optimum anti-reflective layer on the cell to maximize light absorption. In addition, we are investigating whether it is possible to create a guiding layer that confines the optical field to a thin layer of the cell to ensure an appropriately long optical path for maximized photon absorption. This allows carriers to be generated close to the collecting junction to maximize internal quantum efficiency, and should increase light absorption for thin Si cells.

EXPERIMENTAL RESULTS

A matched set of Solarex mc-Si wafers were textured using various metallic catalysts and returned to the production line for normal cell fabrication. SEM photographs of some of the textured surfaces are shown in Figs. 4 and 5.

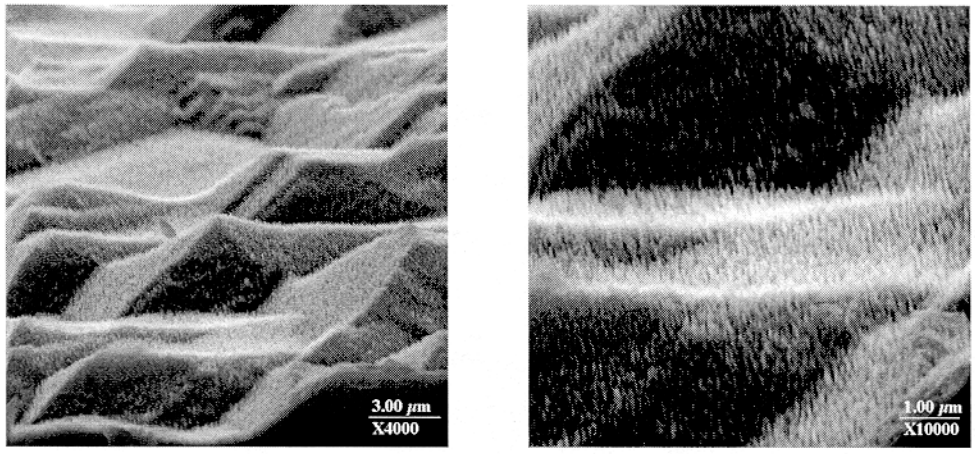

Figure 4. Top View of Cr-assisted RIE on multi-crystalline Solarex Wafers

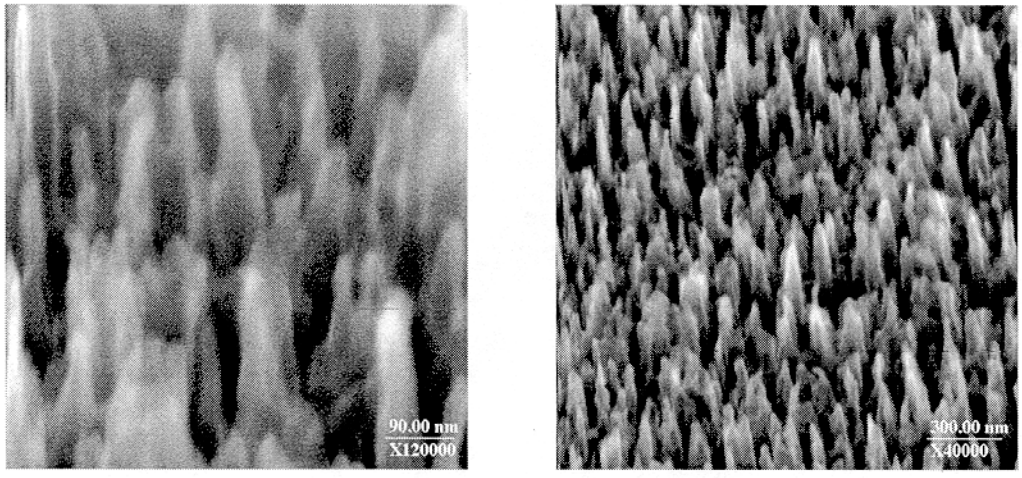

Figure 5. Cross-sectional View of RIE Textures on multi-crystalline Solarex Wafers

The wafers were cleaned at Solarex, textured at Sandia and returned to Solarex for normal production-line processing. Table 1 shows the illuminated IV performance.

Table 1. Performance of RIE-textured cells relative to control cells from the same ingot (percentage difference of Eff. and I_{SC}). The measurements were made at Solarex using standard test conditions. N-Factor is the diode ideality factor.

CELL	Δ EFF (%)	Δ I_{SC} (%)	V_{OC} (mV)	FF	R_{SER} (mΩ)	R_{SH} (Ω)	N-FACTOR
Controls	----	----	593	74.7	8.4	116	1.189
Cr-assisted	-2.06	**+0.54**	591	73.0	8.5	4	1.187
unassisted	-8.60	-7.61	588	74.5	7.3	12	1.270
Al-assisted	-8.79	-6.96	587	73.9	7.8	9	1.280
Au-assisted	-10.40	-5.41	585	71.7	7.2	4	1.367

The texture obtained by the Cr-assisted process consistently produced cells with higher I_{SC} than the controls, in spite of the fact that much of the texture was unintentionally removed from each of the textured cells by the subsequent phosphorus-diffusion and glass-etch steps. In addition, the shunt resistance was reduced considerably on the textured cells, resulting in a decreased fill factor that reduced the efficiency obtained.

DISCUSSION

Efforts are underway to investigate gentler diffusion and glass-etch processes that will retain more of the texture, or the use of slightly larger texture feature sizes that will survive the etching. In addition, we are working to develop a texturization process that removes less Si, so it could be used after the diffusion and etch steps, thereby avoiding the inadvertent texture loss. We are also using diagnostic techniques such as reverse-biased IR emission to ascertain the cause of the cell shunting.

CONCLUSIONS

RIE-texturing has been shown to produce extremely low-reflectance surfaces on multicrystalline Si wafers. The submicron feature sizes produced by this texturing can be controlled by adjusting RIE parameters to create different surface morphologies. The different surface textures obtained have different optical characteristics and compatibility with the rest of the cell fabrication process. If the problems of shunting and texture-loss during etching can be solved, significant improvements in cell performance can be expected.

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Design of a High-Throughput Plasma-Processing System

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ABSTRACT

Sandia National Laboratories has demonstrated significant performance gains in crystalline silicon solar cell technology through the use of plasma-processing for the deposition of silicon nitride by Plasma Enhanced Chemical Vapor Deposition (PECVD), plasma-hydrogenation of the nitride layer, and reactive-ion etching of the silicon surface prior to the deposition to decrease the reflectivity of the surface. One of the major problems of implementing plasma processing into a cell production line is the batch configuration and/or low throughput of the systems currently available. This report describes the concept of a new in-line plasma processing system that could meet the industrial requirements for a high-throughput and cost effective solution for mass production of solar cells.

INTRODUCTION

GT Solar Technologies, Inc. is a manufacturer and supplier of equipment and turnkey fabrication lines for manufacturing photovoltaic multi-crystalline wafers and solar cells. Internationally recognized for its experience and knowledge of the photovoltaic business, including wafer and cell processing, the company maintains a high level of entrepreneurial spirit with a fast response capability to serve the rapidly growing photovoltaic industry.

GT Solar recognizes that reliability and low cost of manufacturing are keys to the continued growth of the PV industry. Therefore, GT Solar has identified certain wafer and cell processing steps that with further development will result in higher efficiency and lower cost. One of these steps is the deposition of silicon nitride by Plasma Enhanced Chemical Vapor Deposition (PECVD). Silicon nitride has an advantage in the cell process in that it provides an antireflective coating and a means to passivate the cell in one operation. As part of its development effort, GT Solar has entered into a contract with Sandia National Laboratories to provide this preliminary conceptual design and cost estimate of a high-throughput PECVD system. GT Solar has placed a special emphasis on cost-savings in the solar cell production process.

PECVD and hydrogenation processes for solar cells have historically been done in batch systems using tube-type or parallel plate reactors. In a tube-type reactor, wafers are typically loaded into a carrier made of parallel graphite plates. After the carrier is inserted into a furnace tube and connected to a RF power supply, the tube is evacuated and the temperature and gas flows are stabilized. The RF power provides the energy to allow deposition of silicon nitride films at low temperature, typically around 350 C. The actual deposition process is only a few

minutes long, but the time required for pressure and temperature stabilization limits the total cycle time to about 30 minutes. A typical PECVD furnace such as the Pacific Western Coyote will have two tubes and a batch size of 140 wafers in each tube (100 mm x 100 mm) to achieve a maximum throughput of approximately 560 wafers per hour. Although they have a relatively high throughput in a small footprint, the carrier design has made it difficult to automate the loading operation. An operator is required to load and unload the carriers.

In a parallel plate reactor, the wafers are loaded onto a flat carrier plate that is inserted into a vacuum chamber. These systems can achieve higher throughput with the use of vacuum load locks that isolate the process chamber(s) from atmosphere. A high throughput system might require a batch size of 100 wafers, requiring a carrier plate approximately 1 square meter in size. The systems can be quite large and expensive as compared to the tube-type reactors, especially if automatic wafer and carrier handling is included.

TASK 1 - In-Line High Throughput PECVD System

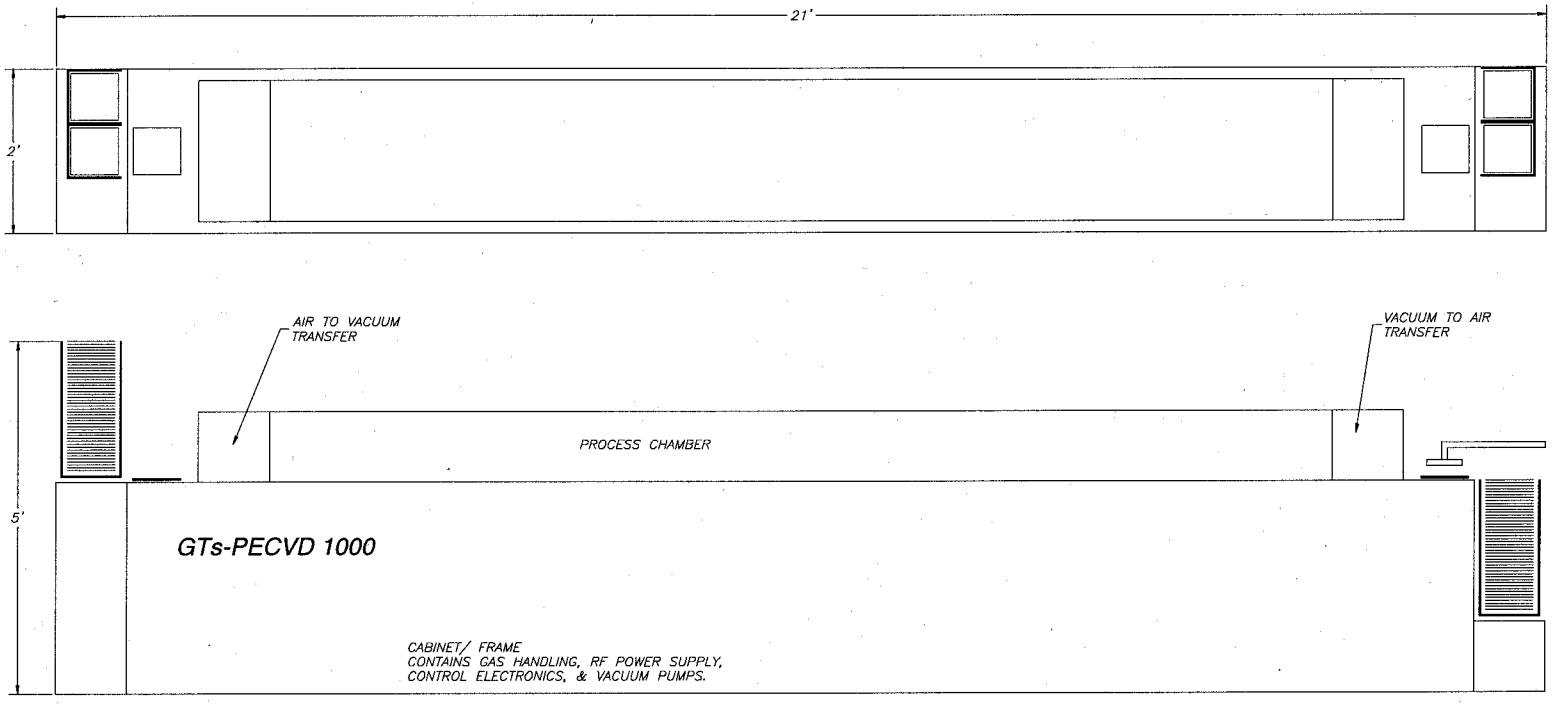
The goal of this task is to conduct an engineering study to develop a conceptual design for equipment that will deposit silicon-nitride on silicon wafers with a refractive index between 2.0 and 2.4. In support of its work, GT Solar has interviewed and consulted with solar cell manufacturers and equipment suppliers concerning the process, equipment throughput, and budgetary cost criteria. A high level of interest was shown by these manufacturers in having a high throughput automated PECVD system that could easily be added to a cell production line.

Conceptual Design

The conceptual design shown in Figure 1 takes into consideration the following requirements: Automatic loading and unloading of the wafers, belt operated system, processing speed to meet the throughput requirements of 1000 wafers/hr, and the process for achieving the deposition parameters. The figure shows that the system will include the following sub-systems:

a. Loading and unloading wafer transfer system
b. Belt transfer mechanism
c. Load locks
d. Vacuum chamber
e. Gas handling components
f. RF power supply and controls
g. Vacuum pumps

FIGURE 1 In-Line PECVD System, the GTs-PECVD 1000



Wafer Throughput Calculations

The consensus of the potential customers and industry participants is that GT Solar should consider the design of a machine with a minimum throughput of 1000wafers/hr.
Such throughput may be achieved according to the following calculations.

Based on 1000, 5" wafers per hour (single row on the belt @ 5.2" center to center), equals 16.7 wafers per minute, which is equivalent to a belt speed of 87"/min.

The current range of deposition rate for silicon nitride in a parallel plate reactor is in the range of 200 to 600 Å/min. Assuming a rate of 400 Å/min, and a required deposition thickness of 800 Å, a 2 min deposition is required. A deposition zone approximately 15 feet long is required.

Capital Cost Estimates

Materials -
- Chamber
  - Belt drives
  - Load Locks
  - Gas Handling
  - Vacuum Equipment
  - Wafer Handling
  - Electronics
  - Controls
  - Computer Hardware

Labor and Overhead -
- Engineering
- Manufacturing
- Software

Other Expenses -
- G&A
- 7% Fee

Total	$ 947,000

Operational Cost Estimate

A deposition area 15 feet long and 8 inches wide is 1440 sq. inches. A typical batch (tube type) PECVD system occupies a deposition area of 2400 sq. inches (for 96, 5" wafers). Therefore, assuming a similar diode geometry is maintained, the RF power requirements for an in-line system will be approximately 60% of that required for a batch system. A 1500-watt RF power supply should be sufficient. The power needed to heat 1000 wafers per hour to 350 degree C is approximately 10 kW. This is a combination of IR and resistance heaters. In

addition to another 5 kW for controls and pumps, we estimate the total power requirement is about 17 kW. At \$0.l0/kwhr, the power cost will be \$1.70/hour.

We assume the usage rates of process gases are similar to the current batch processes, where each wafer requires approximately 17cc of silane and 140 cc of ammonia. At 1000 w/hr, the system uses 17 l/hr of silane and 140 l/hr of ammonia. At \$0.75/l for silane and \$0.006/l for ammonia, the total process gas cost is \$13.60/hr.

The total operational cost is \$1.70 + \$13.60 = \$15.30/hr or approximately 1.5 cents per 5" wafer. We compared this to the TiO_2 APCVD process and found it also costs about 1.5 cents per 5" wafer, but does not provide any cell passivation.At 2.2 watts per cell, the cost per watt for PECVD is 0.7 cents.

TASK 2 - PLASMA HYDROGENATION

The deposition area is divided into multiple gas zones to allow changing the film index of refraction and hydrogen content. The incremental cost of adding each gas zone is approximately \$20K including plumbing and controls for silane, ammonia, and nitrogen. We expect a total of two zones will be required for the optimized silicon nitride process with hydrogenation.

TASK 3 - REACTIVE ION ETCHING

The processing of self-aligned, selective emitter solar cells requires a reactive ion etch of the emitter prior to deposition of silicon nitride [1]. In this process, the printed cells were etched for about 1 minute in 100 mTorr of SF_6 prior to the PECVD deposition of silicon nitride. In this task we have considered the design modifications required to add the RIE process prior to the PECVD process in the proposed in-line plasma processing system.

Assuming the same throughput of 1000 5" wafers per hour, a one-minute RIE process will require about 87" of plasma exposure. The process chamber will be extended by about 8'. The RIE requires a pressure between 100 and 200 mTorr, whereas the PECVD pressure is about 2 Torr. It is likely that a third load-lock will be required between the two chambers.

The cost to add the RIE process to the proposed in-line system is estimated to be \$215,000, and will include the following components:

a) Process chamber with belt mechanism
b) RF power supply
c) Vacuum system
d) Gas handling system
e) Load-lock chamber
f) Engineering & overhead

We believe the addition of RIE to the system is feasible as long as the process time is limited to one to two minutes and the belt speed and/or chamber length is adjusted accordingly.

CONCLUSION

A payback analysis was performed to see if an existing solar cell manufacturer currently using an APCVD TiO_2 AR coating could justify the purchase of an in-line PECVD system. Our calculations show that if the system cost is $950K, and the cell efficiency is improved by 7% (for example from 2.1 watts with TiO_2 to 2.25 watts per 5" cell with nitride), the payback for a 12 MW factory would be less than one year. Of course improvements in cell efficiency will depend on many factors, such as the cell process and the quality of the starting wafers.

ACKNOWLEDGMENTS

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Gettering, Hydrogenation and Resistivity dependence of Minority Carrier Lifetime in Dendritic Web Ribbon Silicon

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Abstract

Five different resistivities (0.34, 0.8, 3.2, 7.0 and 16 Ω-cm) were investigated to understand the dopant-defect interaction in p-type, boron doped dendritic web and study its response to gettering and passivation techniques. As grown and processed lifetime was found to be a strong function of resistivity with higher resistivity displaying higher lifetime. It was found that a 6 min phosphorus gettering in a lamp heated furnace was just as effective as 2 hour phosphorus gettering in a conventional furnace and raised the as grown lifetime of ~ 1μs in 16 Ω-cm web to ~ 6 μs. Al gettering at 850°C/2 min raised the as grown lifetime to 3 μs. PECVD SiN hydrogenation alone at 850°C/2 min did not show any improvement in the as-grown lifetime but SiN hydrogenation from the front in conjunction with Al BSF firing on the back raised the as-grown lifetime from 1 μs to 8 μs, suggesting Al enhanced hydrogenation in web. A combination of phosphorus gettering followed by simultaneous Al gettering and SiN hydrogenation raised the 16 Ω-cm web lifetime to 20 μs, however, lifetime remained less than 5 μs for resistivities below 7 Ω-cm. This suggests strong doping-defect interaction, which could not be fully removed even by the combination of all the gettering and passivation techniques used in this study. Modeling of the processed lifetime versus resistivity data revealed that this doping dependence can be explained by the presence of a shallow trap (~ 0.2 eV) whose density is a function of doping concentration $\{N_T=N_{To}/(1+N_A/N_{ref})\}$ with $N_{ref} \geq 10^{15}$. Because of such a strong doping dependence, the best screen-printed cell efficiency (~ 13.5%) was obtained on 16 Ω-cm web Si, while the efficiencies were below 12.5% on lower resistivity crystals.

Introduction

In order to reduce material cost, many silicon sheet growth techniques have been developed to produce thin substrates for solar cells. These techniques take advantage of the efficient use of silicon feed stock with no kerf loss, and the elimination of mechanical sawing steps including etching to remove saw damage. The trade-offs in the use of these growth techniques include the difficulty of maintaining the desirable properties of silicon such as crystallinity, low defect density, long minority carrier lifetime, low stress, and mechanical integrity including flatness, thickness uniformity and surface roughness [1].

Dendritic web is one of the most promising silicon sheet growth techniques for thin (~100 μm) silicon for solar cells. Dendritic web typically has no grain boundaries but it does have multiple twin boundaries running parallel to the external surfaces [1,2]. These are located in a band about midway through the ribbon thickness. Each (111) surface is made up of a single grain so that losses associated with grain boundaries are eliminated [1]. However, according to Cunningham et al. [3], most of the dislocations in as grown web silicon are electrically active, and accumulate near the twin boundaries forming a thin slab of highly defective material within the web ribbon. This is partly responsible for low as-grown lifetime in dendritic web silicon.

The low as-grown lifetime in the web silicon is attributed to the rapid cooling experienced by web during the growth process. Rapid cooling can quench point defects into the material, which tend to anneal during the processing of solar cells [2]. More so, like other defective materials the minority carrier lifetime in dendritic web silicon is found to decrease with decrease in the base resistivity [4]. The dependence of minority carrier lifetime on the doping concentration is often attributed to change in activity of the recombination centers due to the change in Fermi level position [4]. The lifetime degradation is associated with the existence of defects such as dislocations or precipitates that are introduced during crystal growth or device processing. These defects in turn give rise to energy levels within the bandgap, which can mediate recombination events via the Shockley-Read-Hall mechanism. Because the Fermi level is set by the concentration of the dopant, low resistivity material becomes more sensitive to these defects levels, especially if the defect level is shallow (<0.3 eV), resulting in smaller lifetime [4]. In addition, if the dopants are directly involved in defect formation (such as B-O-V pair) then trap density can increase with doping density, making the lifetime even more sensitive to increased doping.

In this paper we have modeled this effect by using a Kendall like equation: $N_T = N_{To}(1 + \frac{N_A}{N_{ref}})$. In addition to the doping dependence of lifetime web, have investigated a) the effectiveness of phosphorus gettering alone during the lamp heated belt line processing (BLP) b) hydrogenation from SiN before and after phosphorus gettering c) the effect of Aluminum gettering alone during SP back surface field (BSF) formation d) hydrogenation from SiN film during BSF and front metal contact firing cycles and e) the combined effect of phosphorus gettering followed by simultaneous Al gettering and SiN-induced hydrogenation. Rapid belt line gettering process is also compared with the more conventional extended gettering of web during the conventional furnace processing (CFP). Finally, the measured lifetime as a function of doping level was analyzed by modeling to extract the energy level (assuming a single trap level) and the degree of dopant defect interaction expressed in terms of N_{ref}.

Experimental

Five different resistivities (0.34, 0.8, 3.2, 7.0 and 16.0 Ω-cm) of p-type, boron doped dendritic web silicon were obtained from single ribbon pull to eliminate the variability in feed stock and growth run. The samples were cleaned in 1:1:2 H_2SO_4:H_2O_2:H_2O for five minutes followed by a 3 minute rinse in DI water. This was followed by a clean in 1:1:2 HCl:H_2O_2:H_2O for 5 minutes and a 3 minute rinse in DI water. A final dip in 10% HF for 2 minutes was performed followed by 30 seconds DI water rinse. The samples were then used for the as grown lifetime measurements by photo-conductance decay (PCD) technique. During the lifetime measurement, the samples were placed in a 0.001M of iodine in methanol solution to provide effective surface passivation.

Belt line Phosphorus and Aluminum Gettering of web with and without SiN-induced hydrogenation

After the as grown lifetime measurements, the samples were cleaned as above. Each sample was divided into 4 parts to study (a) phosphorus gettering alone (set 1), (b) phosphorus gettering plus SiN hydrogenation (set 1), (c) Al gettering alone (set 2), (d) Al gettering plus SiN hydrogenation (set 3), and (e) combined effects of P and Al gettering and SiN hydrogenation (set 4). Samples in sets 1, 2 and 4 were subjected to phosphorus spin-on and baked for 2 minutes on a hot plate set at 200°C, followed by a 6-minute drive-in at 925°C in a lamp heated belt furnace. After the diffusion, the phosphorus glass was removed in 10% HF followed by a quick rinse in DI water. This resulted in a sheet resistance of ~ 45 Ω/□. An 830Å thick PECVD SiN film with an index of ~ 2.0 was deposited on all the samples (sets 1-4) at 300°C. Al metal was screen-printed on the backside of the samples in sets 3 and 4 and baked for 2 minutes followed by back surface field formation at 850°C for 2 minutes in the belt line furnace. Samples in all the four sets were etched down to bare Si to remeasure the bulk lifetime, shown in Fig. 1.

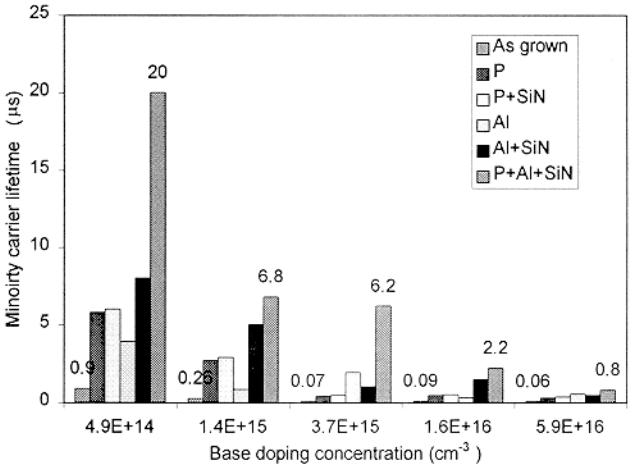

Fig. 1: Resistivity dependence of Phosphorus and Al gettering and SiN hydrogenation of web silicon.

Phosphorus gettering and high temperature anneal in conventional furnace

In order to assess the difference in gettering efficiency of conventional and rapid belt line processing, 10 cm by 2.5 cm samples were cleaned for the as grown lifetime measurement by PCD technique. The samples were then cut into two halves (for each resistivity), and one half was subjected to phosphorus diffusion in a conventional furnace for 2 hours at 900°C. The second half of the samples was annealed in nitrogen ambient for the same temperature and time in order to decouple the effects of phosphorus gettering and heat treatment alone. Both sets of samples were etched to bare Si to measure the bulk lifetime. These lifetimes are summarized in Fig.2. A comparison of lifetime data in Figures 1 and 2 provides the comparison between belt rapid line and prolonged conventional gettering.

Discussion

A. Doping dependence of As-Grown lifetime in dendritic web silicon

As shown in Figures 1 and 2, the as-grown lifetime in this particular web crystal growth run was found to be very low (<1 μs) for all the dendritic web silicon resistivities. However, the as-grown lifetime seems to be somewhat higher for higher substrate resistivity. The low as grown lifetime in dendritic web silicon could be due to the stress-induced recombination-active structural defects (dislocations) which are concentrated in the inner part of the substrate, particularly at and near the twin planes [4]. The structure of these dislocations or precipitates at the twin plane is believed to be more complex than simple dislocations because the simple and clean dislocations, at room temperature, are generally not recombination-active [5]. It could also be due to the quenched-in point defects during the growth. Note that there may be some error in the absolute values of the as grown τ because of PCD tester limit.

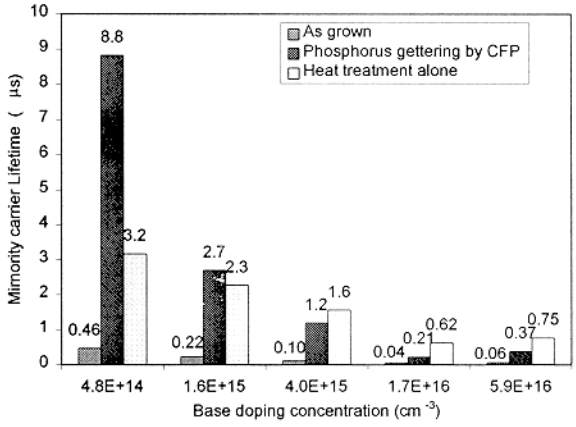

Fig. 2: Resistivity dependence of CFP Phosphorus gettering and heat treatment on web silicon.

B. Effect of Phosphorus gettering and the corresponding high temperature cycle on dendritic web silicon

Phosphorus gettering alone enhanced the minority carrier lifetime for all the resistivities (Figs. 1 and 2). Figs. 1 and 2 also indicate that 6-min phosphorus gettering in the lamp heated belt furnace is just as effective as 2-hour phosphorus gettering in a conventional furnace. For example, both gave a lifetime of ~ 6-8 μs for 16 Ω-cm web silicon.

It should be noted that the heat treatment alone at 900°C for 2 hours (Fig. 2) also improved the lifetime of minority carriers for all the resistivities but with the highest value of 3.2 μs in the 16 Ω-cm web. This improvement could be attributed to the dissolution of the impurities and defects from the bulk to the surface, which can also act as weak sink for the impurities. Also, the straight heat treatment induced improvement in the lifetime is small because the bulk region of the substrate maintains a high super-saturation of oxygen, which may dominate the effective minority carrier lifetime. The formation of oxygen precipitates in the bulk is known to degrade both recombination and generation lifetime in web [6].

C. Synergistic effect of Al gettering and SiN hydrogenation

Combined effects of Al gettering and SiN hydrogenation is found to improve the lifetime for all resistivities by 87– 95%, with greatest improvement (8.8 μs) observed in the highest resistivity substrates (Fig. 1). However, the Al gettering alone is not very effective yielding τ<4 μs. Likewise, SiN heat treatment alone also does not produce much hydrogenation (τ<1 μs). However, the combined effect of Al and SiN is much greater than the additive effects of the two individual processes. We believe the Al BSF process creates vacancies, which facilitates the incorporation of hydrogen into the bulk via the formation of hydrogen-vacancy (H-V) pairs, resulting in enhanced bulk defect passivation with lifetime approaching 9 μs for 16 Ω-cm material. However, τ for ≤ 3 Ω-cm web still remains below 5 μs suggesting alternate gettering techniques need to be investigated.

D. Combined effect of Phosphorus gettering and simultaneous Al and SiN heat treatment

Fig. 1 shows that combined effect of phosphorus gettering followed by simultaneous Al and SiN heat treatment resulted in the largest improvement in lifetime for the 16 Ω-cm resistivity, from 0.9 μs to 20 μs. On the other hand, the lowest resistivity substrate improved to only 1 μs from 0.06 μs. It should be noted that the temperature cycles (925°C/6 min for phosphorus diffusion plus 850°C/2 min for Al BSF + 730°C/ 30 seconds for contact firing) simulate the emitter diffusion and screen-printed contact firing cycles used in actual cell fabrication. Therefore, the measured lifetime after this treatment represents the expected lifetime values in the finished device. The cells fabricated on these materials gave efficiency in the range of 11-13.5%, with 0.34 Ω-cm giving the lowest efficiency and 16 Ω-cm giving the best performance. Additional improvements in fill factor, lifetime, and surface passivation can give further improvement in efficiency. Since the finished lifetime is a function of the starting lifetime and the doping dependence of lifetime remains after processing, it shows that gettering and

passivation techniques used in this investigation so far are not effective enough to eliminate the source of the lifetime problem in low resistivity web.

E. Lifetime Modelling to Assess the Dopant-Defect Interaction

The minority carrier lifetime is generally expressed as $$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + BN_A + C_P N_A^2 \qquad (1)$$

Where C_p is the band-to-band Auger coefficient and B is the radiative band to band coefficient. The τ_{SRH} is given by

$$\tau_{SRH} = \frac{\tau_{no}(p+p_1)+\tau_{po}(n+n_1)}{n+p} = \frac{\tau_o(p+p_1+n+n_1)}{n+p} \qquad (2)$$

For the case where $\tau_{no} = \tau_{po} = \tau_o$ and the trap density is independent of doping density, $\tau_o = \frac{1}{N_T \sigma V_{th}}$. For defective silicon materials, such as dendritic web, where trap density (N_T) can change with doping density, following Kendall-like equation was used to account for this effect in this study

$$\tau_o = \frac{\tau_{o\infty}}{1+\frac{N_A}{N_{ref}}} \quad \text{and} \quad N_T = N_{To}\left(1+\frac{N_A}{N_{ref}}\right) \qquad (3)$$

where $N_{ref} = \infty$ and $\tau_{o\infty} = \tau_o$ or when trap density is independent of doping concentration. Note that N_{ref} is a measure of the doping dependence of τ_o or trap density and the lower the N_{ref}, the stronger the dopant-defect interaction. A combination of N_{ref} and E_t was determined by matching the measured and calculated lifetimes as a function of doping level. Model fit gave a trap level of ~ 0.19 eV with N_{ref} of 3.5 E15, both as grown and processed (P+Al+SiN) respectively, assuming simple trap level. The trap level is shallow which supports the shape of the curve. The doping dependence of trap density is rather weak in this case, because the N_{ref} value is one order of magnitude greater than the doping concentration (4.85E14). More work needs to be done along this line to gain a better understanding of the role of dopants in forming defects.

Conclusion

As grown lifetime in dendritic web was found to be quite low and doping dependent. The low as-grown lifetime can be attributed to the quenched-in point defects during growth and/or dislocations accumulated near the twin boundaries about midway through the ribbon thickness. In order to improve the lifetime for high efficiency silicon solar cells, low cost gettering techniques using lamp heated belt furnace were employed. Lifetime enhancement was found to be resistivity and initial lifetime dependent. The effect of hydrogenation from SiN on phosphorus gettered web was very small. This could be attributed to the lifetime limiting mechanism, which is not affected by hydrogenation or lack of hydrogenation itself. The rapid phosphorus gettering in lamp heated belt furnace was found to be as effective as the 2 hour phosphorus gettering in a conventional furnace processing. The Al gettering alone is not very effective. SiN heat treatment alone without prior gettering does not produce much hydrogenation. However, the combined effect of Al and SiN is much greater than the additive effects of individual process. The Al BSF process can create vacancies, which may facilitate the penetration of hydrogen into the bulk via the formation of H-V pairs, resulting in enhanced bulk passivation of defects. The largest improvement in lifetime was observed for the 16 Ω-cm, from 0.9 to 20 μs. On the other hand, the low resistivity improved to only 1 μs from 0.06 μs.

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Aluminum-enhanced PECVD SiN hydrogenation of defects in Edge-defined Film-fed Grown (EFG) multicrystalline silicon

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Abstract – Gettering of impurities and hydrogen passivation of defects in EFG multicrystalline silicon were studied by low cost manufacturable technologies such as screen-printed Al-BSF and annealing of PECVD SiN antireflection coating in a lamp heated belt-line furnace. Quasi-steady-state photoconductance (QSSPC) technique was used to assess the gettering- and passivation-induced improvement in bulk lifetime. The effect of PECVD SiN hydrogenation on EFG silicon was studied in conjunction with screen printed Al-BSF formation to investigate the synergistic effect of Al gettering and PECVD SiN induced hydrogenation of bulk defects. It is found that PECVD SiN deposition and anneal, without the co-formation of an Al-BSF layer on the back, does not provide appreciable hydrogenation of bulk defects in EFG material. PECVD SiN deposition and anneal after the Al-BSF formation show some hydrogenation of bulk defects, which is a strong function of anneal temperature. The higher the anneal temperature, the smaller the hydrogenation probably because sticking coefficient of hydrogen at defects decreases at higher temperatures. However, simultaneous formation of Al-BSF and PECVD SiN anneal is found to significantly enhance the hydrogenation ability of the PECVD SiN film. Phosphorus gettering (n^+ emitter formation) raised the as-grown bulk lifetime from 1.2 to 3.1 μsec. PECVD SiN anneal and Al-BSF formation individually altered the phosphorus gettered bulk lifetime from 3.1 to 2.8 μsec and to 7.5 μsec, respectively, but the simultaneously formation of Al-BSF and SiN hydrogenation at 850 °C/2min resulted in a bulk lifetime of 12.0 μsec.

Introduction

Electrical properties of PV grade multicrystalline silicon materials can be improved by appropriate gettering and hydrogen passivation techniques[1-9]. Unlike single crystal silicon, PV grade multicrystalline silicon has metallic impurities as well as crystallographic defects such as grain boundaries, twins, and dislocations. These defects can significantly reduce the bulk lifetime. Edge-defined film-fed grown (EFG) silicon used in this study had as-grown bulk lifetime of less than 5 μsec. Therefore, gettering and passivation of impurities and defects are essential for achieving high efficiency (>15%) solar cells on EFG multicrystalline silicon. Many researchers have shown that Al gettering can be very effective in removing the metallic impurities[1-5]. Similarly, hydrogenation has been found to be quite effective in passivating crystallographic defects in multicrystalline silicon[5-9]. Although the synergistic effect of Al gettering and H passivation has previously been examined[10], a study of Al gettering in conjunction with PECVD SiN induced hydrogenation specifically has not been evaluated carefully. This paper presents a systematic study of PECVD SiN induced hydrogenation and screen printed Al gettering of EFG silicon, individually and in combination to understand and study the synergistic effects.

Experimental

Large area (10 x10 cm^2) edge-defined film-fed grown (EFG) multicrystalline silicon wafers from ASE Americas were used in this investigation. A Quasi-steady-state photoconductance (QSSPC) technique, which is more suitable for the lifetime measurement of lower lifetime multicrystalline silicon[11-12], was

utilized to measure the bulk lifetime. The resistivity of p-type EFG wafers used in this study was in the range of 2 ~ 4 Ω-cm. Wafer regions had thicknesses ranging from 10 to 20 mils. Due to the spatial nonuniformity of crystallographic defects in a 10x10 cm^2 wafer, lifetimes were measured at six locations on each wafer and the average of six measurements was used for the reported lifetime. In the QSSPC technique, bulk lifetime was determined at a minority carrier injection level of $1.0x10^{15}$ cm^{-3}. Lifetimes were measured with Iodine-methanol chemical passivation of the silicon surface, as the Iodine-methanol solution is known to be very effective in passivating the silicon surface[13]. After appropriate cleaning steps, P diffusion was performed by spin-on coating followed by a drive in a lamp heated belt furnace to form the n+ emitter (930°C/6min). After the P diffusion, n+ emitter was etched off and the bulk lifetime was measured to assess the impact of P gettering on EFG silicon. For screen printed Al gettering, screen printed Al was applied on the back followed by 850 °C/2min alloying in the belt furnace to form an Al back surface field (BSF) layer. A Plasma-Therm (series 700) reactor which operates at 13.6 MHz frequency was used to deposit 830 Å thick PECVD SiN with an index of 2.0, which is suitable for single layer antireflection coating because after the firing of screen printed contacts this SiN film contracts a little along with a slight increase in the index. After firing, Al layer and/or annealed SiN film were removed in an etching solution. The n+ and p+ layers were etched subsequently in a 15 : 5: 2 HNO_3 : Acetic acid : HF solution for post-processing bulk lifetime measurements to assess the impact of Al gettering and/or PECVD SiN induced hydrogenation.

Results and Discussions

It has been shown that screen-printed Al forms an effective BSF in the belt furnace[14]. During the alloying process, molten Al provides a sink for impurity gettering due to higher solubility of impurity in molten Al compared to silicon[15]. Screen printed Al gettering was performed at 850 °C for 2 min in a lamp heated belt furnace which forms a 5-10 μm deep effective Al-BSF. The P gettering in this study was performed at 930 °C/6min, resulting in sheet resistance of ~ 40 Ω/□. Figure 1 shows change in bulk lifetime of EFG silicon due to individual gettering and SiN hydrogenation, and combinations of gettering and SiN hydrogenation. The P treatment alone improved the as-grown bulk lifetime from 1.2 to 3.1 μsec and the subsequent Al treatment (850 °C/2min) raised the bulk lifetime from 3.1 to 7.5 μsec. In addition to P and Al gettering, we studied the effect of PECVD SiN-induced hydrogenation of EFG silicon. After the P gettering, when a PECVD SiN was deposited on the front followed by an 850 °C/2 min anneal in a conveyor belt furnace without the presence of Al on the back, no improvement in bulk lifetime was observed. This indicates that either PECVD SiN film without the Al does not efficiently passivate the defects in EFG silicon at 850 °C/2min or the lifetime is being dictated by some other mechanism. However, when the PECVD SiN on the front was annealed in conjunction with screen printed Al on the back, this treatment showed a very significant improvement in bulk lifetime. In this scheme, after the P diffusion at 930 °C/6 min, a PECVD SiN film was deposited on the front followed by screen printing of Al on the back. Anneal of the PECVD SiN and gettering of the screen printed Al were performed

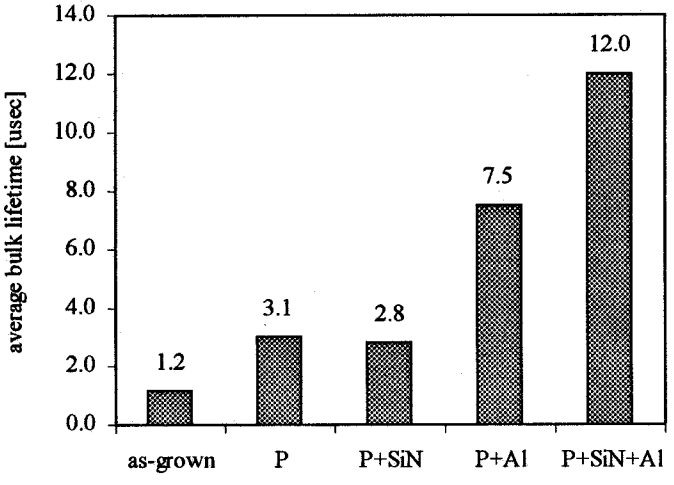

Figure 1. Bulk lifetime improvement due to P, Al gettering and SiN hydrogenation.

simultaneously at 850 °C/2 min in a conveyor belt furnace. This resulted in a very significant improvement in the bulk lifetime of EFG silicon from 3.1 μsec to 12.0 μsec, as shown in Figure 1. Recall that P and Al gettering raised the bulk lifetime from 1.2 μsec to 7.5 μsec and PECVD SiN by itself did not show any hydrogenation. Therefore, 4.5 μsec (12 μsec – 7.5 μsec) increase must come from the synergistic effect of Al and SiN.

To further understand the Al-enhanced SiN hydrogenation in EFG silicon, four different process schemes were designed and studied as shown in Figure 2. In this experiment, wafers with similar as-grown lifetimes (1.6 ~ 1.8 μsec) were selected to minimize the variability in the as-grown lifetime. Bulk lifetime was measured before and after each process scheme. In scheme *A* the PECVD SiN film on the front was annealed simultaneously with the screen printed Al on the back. In the schemes *B, C and D,* the screen printed Al on the back was fired first to form the BSF and then the PECVD SiN was deposited on the front, followed by the 740 °C/1 min, 800 °C/1 min, and 850 °C/1 min anneal, respectively. In these three schemes, Al gettering and PECVD SiN induced hydrogenation was done sequentially rather than simultaneously and the SiN hydrogenation takes place in the second anneal step. The second anneals are performed to simulate a screen printed front contact firing cycle. The results of this experiment are shown in Figure 3. The sequential processing schemes *B*, *C*, and *D* were found to be less effective in improving the bulk lifetime of EFG silicon compared to the simultaneous processing scheme *A*. Even though the thermal treatments in schemes *A* and *B* are exactly same (850 °C/2min + 740 °C/1 min), the SiN anneal temperature is quite different (A: 850 °C, *B*: 740 °C). A lower hydrogenation temperature provides higher "sticking probability" of hydrogen onto defects. Therefore, in the absence of any synergistic effect between Al treatment and SiN hydrogenation, one might expect the sequential scheme *B* to be more effective in improving the bulk lifetime compared to the simultaneous processing scheme *A*. However, the simultaneous scheme *A* gave the best result with the bulk lifetime of 14.2 μsec, suggesting a

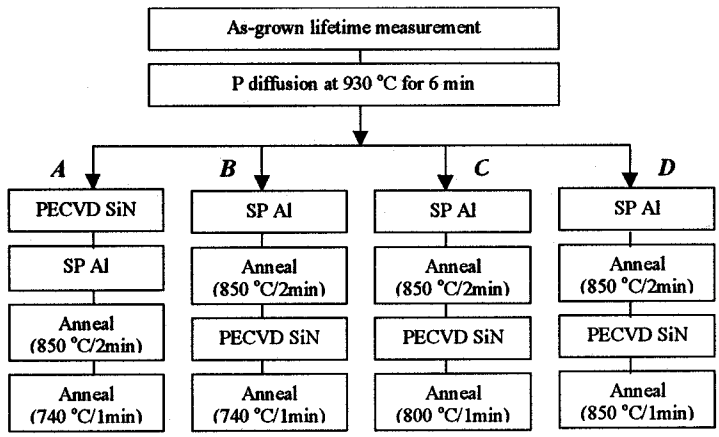

Figure 2. Four different process schemes to understand the synergistic effect of Al-enhanced SiN hydrogenation in EFG silicon.

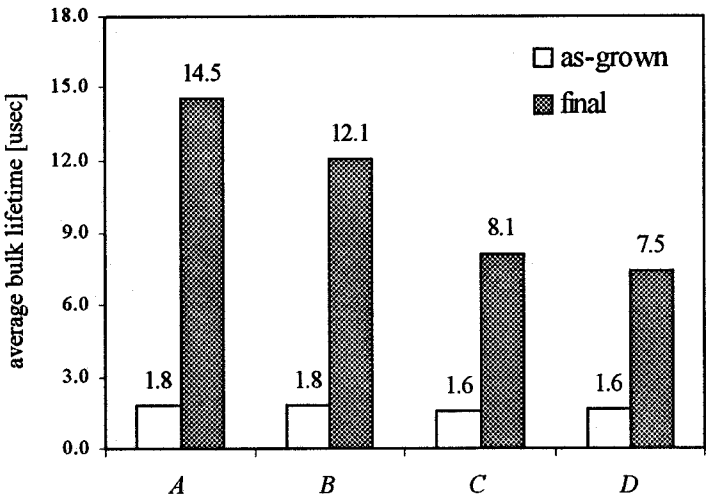

Figure 3. The effect of four different process schemes for SiN hydrogenation on bulk lifetime of EFG silicon.

positive synergistic interaction. One possible mechanism could be that the dissolution of silicon in Al during the simultaneous scheme *A* produces vacancies which interact with atomic hydrogen from the SiN film to form H-V pairs that can diffuse more rapidly into silicon. Such a mechanism has been proposed to explain forming gas-induced hydrogenation of silicon [16]. In the case of sequential process schemes, the Al-BSF layer is already formed and a thin eutectic layer with some amount of silicon exists between silicon and the remaining Al layer. When the second anneal is performed, the eutectic layer also melts along with the Al. Since the eutectic layer had some silicon, there is much less dissolution of silicon into the molten Al, reducing the formation of vacancies or H-V pairs. This reduces the hydrogenation of defects causing sequential scheme to be inferior to the simultaneous scheme. To investigate the competition between vacancy generation and the sticking probability of hydrogen on defects, we did the simultaneous firing at various temperatures ranging from 810 °C to 890 °C for 2 min and indeed found an optimum at 850 °C.

Figure 3 shows that sequential processing involving 850 °C/2 min Al-BSF and 850 °C/1 min SiN anneal (scheme *D*) gives a bulk lifetime of 7.5 μsec which is nearly equal to the bulk lifetime after the P gettering and 850 °C/2min Al treatment (P+Al) as shown in Figure 1. This indicates that scheme *D* does not receive any appreciable hydrogenation from PECVD SiN. However, if the second anneal temperature (or SiN anneal temperature) is reduced to 740 °C (scheme *B*), the bulk lifetime increases to 12.1 μsec. This indicates that effectiveness of SiN hydrogenation improves at lower temperature. This is probably because the sticking probability of hydrogen on defects increases, *i.e.*, hydrogen does not dissociate from the defect so readily at low temperature. Thus, an optimum cell processing should involve the simultaneous formation of an Al-BSF layer and the SiN hydrogenation anneal. The anneal temperature and time should be optimized to balance the vacancy generation which helps hydrogenation, and decrease in sticking probability of hydrogen on defects. Finally the second anneal or contact firing should be either done at low temperature or at high temperature for shorter time to preserve the hydrogenation.

Conclusions

Significant improvement in the bulk lifetime of EFG multicrystalline silicon was achieved by using cost-effective gettering and passivation techniques, such as gettering by spin-on phosphorus and screen printed Al in a lamp heated belt furnace and PECVD SiN-induced hydrogenation. Process conditions used in this study are integral part of cell fabrication resulting in n^+ emitter, p^+ BSF, and SiN AR coating. It was found that a PECVD SiN anneal (850 °C/2min) without the presence of Al on the back does not show bulk lifetime improvement in the EFG silicon. Al gettering at 850 °C/2min, without the PECVD SiN, was found to improve the bulk lifetime from 3.1 to 7.5 μsec. However, bulk lifetime increased significantly when the PECVD SiN on the front was annealed with the screen printed Al on the back. Sequential processing in which an Al-BSF was formed first (850 °C/2min) and then the SiN was deposited, followed by a second anneal, was found to be less effective in improving the bulk lifetime of EFG silicon compared to simultaneous annealing of the SiN and Al layers. These results can be explained by a proposed model in the literature, according to which Al process can enhance the effective diffusion of hydrogen by the formation and increased population of V-H pairs. According to this model vacancies injected from the Si-Al interface during the Al alloying process migrate to the front surface to form the H-V pairs which can diffuse into the bulk more rapidly and effectively. Finally, it was found that the effectiveness of SiN hydrogenation decreases with higher second anneal temperature above 740 °C for a 1 min hydrogenation in the sequential processing.

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Fast shunt hunting in solar cells with highly sensitive lock-in IR-thermography

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Abstract

A novel infrared thermography system is presented, which, using the lock-in principle, extends the sensitivity of a commercial IR-camera into the sub-millikelvin range. Thus the fast, non-destructive, and non-contacting mapping of the leakage currents in solar cells at voltages close to the working point is possible. Typical examples of shunt measurements on a monocrystalline silicon solar cell are presented and discussed.

Introduction

Since solar cells are large-area devices, the lateral inhomogeneities of the cell parameters play an important role in the integral efficiency of the cell. This is especially important for increasing cell sizes and simpler production processes on cheaper substrates, which is decisive in the cost reduction. Whereas for the inhomogeneities in the short circuit current (I_{SC}) LBIC is a very common technique in research and development, only very few data are available on the inhomogeneities of the fill factor (FF) and the open circuit voltage (V_{OC}). This is mainly due to the fact that all parts of the cell are electrically in parallel, thus prohibiting a separation of the bias signal from different sites. In recent years, a few methods have been developed, e.g. by producing an array of small solar cells on the wafer or by separating the cell into arrays of mesa-diodes after the cell process [1,2]. These techniques are very expendable and destructive, and it cannot be guaranteed that they reflect the properties of the original solar cell exactly. Another approach is the indirect measurement of the locally flowing current via the local magnetic field [3]. This approach, however, mainly reflects the lateral current distribution in the cell.

The second indirect method of measuring current inhomogeneities is the mapping of the locally generated heat by thermography. The local heating is proportional to the locally dissipated power representing the local current if a homogeneous voltage is applied. Thermography, which normally is performed in the dark, is based on the correspondence between the dark injection current I_I and the current losses at the same voltage in the illuminated cell (Fig.1).

The classical way of thermography is to use an infrared camera in d.c. mode [4]. But the usual sensitivity, even after averaging, is not sufficient to detect the inhomogeneities in bulk solar cells normally of the order of a few millikelvin. It is possible to measure the cells at a high reverse bias in order to measure shunts due to the higher dissipated power under these conditions, but these shunts often differ from those close to the working point of the cell [5].

To increase the sensitivity of thermography the dynamic precision contact thermography (DPCT) has been developed [6] [7], in which the local cell temperature is measured using a small thermistor in contact with the cell surface. A highly sensitive resistivity bridge together with a lock-in signal treatment allows the measurement of surface temperature modulations down to 100 µK, if the voltage of the cell is pulsed. Scanning the sensor over the solar cell surface generates sequentially a map of the dissipated power. The high sensitivity allows measurements between 0.4 and 0.6 Volt forward bias, covering the range of FF and V_{OC}.

Another general advantage of the lock-in thermography compared to d.c. methods is the better lateral resolution. In d.c. thermography the heat generation is stationary and the lateral contrast is governed by the heat conduction to the thermostatted sample holder. If the bias is pulsed the heat spreading can be treated in terms of thermal waves and the lateral resolution is governed by a

characteristic length determined by the modulation frequency. The lock-in thermography is a quantitative method. The influence of different shunts, for instance, can be separated and the dependence on the illumination level can be calculated [8].

The main disadvantage of DPCT is the relatively long measurement time. Since each pixel takes a few seconds, the serial measurement of , e.g., 100*100 pixels takes approx. 10 hours. To accelerate the shunt measurement with a similar sensitivity, a novel system has been developed, combining joining the advantages of the IR-thermography with the high sensitivity of the lock-in thermography as used in the DPCT. Since it is also a lock-in thermography method, the main features as, e.g., the high sensitivity, influence of the frequency, possible quantitative analysis, non-destructiveness and independence of the solar cell type are still valid.

Experimental

The new system (Fig. 2) is based on a FPA (focal plane array) camera AE4128 from AMBER Inc. This camera with an InSb array is sensitive for wavelenghts between 3 and 5 µm. In the FPA the whole array of 128*128 pixels is exposed simultaneously and read out at a frame rate of 217 Hz. Thus, in contrast to DPCT and scanning IR-cameras, the whole sample is measured in parallel, which allows a much faster measurement. The thermal resolution of a single picture is 6 mK (r.m.s. noise). The sample is thermostatted at 25 °C and a pulsed forward bias of typically 0.5 Volt is applied at the chosen lock-in frequency. The sample is covered with a thin blackened plastic foil and pressed to the thermostat by a vacuum. The black foil causes a high IR emission irrespective of the surface emissivity of the cell. The IR images are amplified and digitized on-line, resulting in a steady data stream of 7 MBaud representing 217 128*128 pixel pictures per second, which is transmitted to a computer. Since this would result in more than 25 GByte after one hour, the data have to be treated on-line. To perform the lock-in correlation, each picture is multiplied by a coefficient, which represents the harmonic correlation function for the time interval the picture was taken in. Summing up these pictures weighted over several (typically thousands of) periods results in one image, in which each pixel is a lock-in correlation of the data accumulated here. This can be understood as 16384 lock-in correlations in parallel, one for each pixel separately, drastically reducing the noise observed in the temperature modulation.

In order to get the complete information, two independent correlations (sine and cosine) have to be made, as usual in lock-in techniques. This is done by two parallel running fast digital DSP frame grabber boards (DIPIX FPG 44) in a PC. This results in two pictures of the temperature modulation of the solar cell in-phase and off-phase to the applied bias pulses, being transmitted to the host computer. Choosing this on-line data treatment the maximum measurement time, limiting the thermal resolution, is limited only by the LN_2 capacity of the camera cryostat. Since at least four pictures per period are necessary for the digital lock-in correlation, modulation frequencies up to 54 Hz are possible. This is significantly higher than the maximum useful frequency in DPCT, thus enabling a higher lateral resolution [9].

Test measurements and comparisons with DPCT showed that after approx. 20 minutes of measurement time a noise level of 10 µK (r.m.s.) can be achieved. Thus, under these conditions the thermal sensitivity has increased by 3 orders of magnitude compared to a single picture, which is sufficient to measure even the heating caused by small leakage currents. Using the standard camera objective enables any image size down to 30*30 mm^2 to be investigated, corresponding to a pixel diameter of 230 µm. If a microscope objective is used, each pixel represents a 12*12 μm^2 sample area, close to the optical limit for the wavelengths used. If a shunt is to be localized for the detailed analysis using EBIC, TEM, EDX or other techniques, the lock-in IR thermography is a powerful tool unrivaled up to now with respect to the other above-mentioned techniques.

Results

Figure 3 shows the IR-thermogram of a solar cell on a monocrystalline silicon Cz-wafer after measurement times of one minute (a) and more than one hour (b), respectively. The short measurement time is sufficient to detect the main shunt of this cell, which is beyond the bus bar, and to detect some additional shunts at the outer edges of the cell. These positions are both typical shunting sites in crystalline solar cells, indicating weak points in the solar cell process. After a longer integration time (b) additional ring structures appear in the image of this sample. These increased leakage currents are caused by a high density of grown-in microdefects in this Cz-silicon, which are not resolved as single shunts. Since the thermal contrast in the rings is only of the order of 20-50 μK, the main shunt is out of scale in this image and appears very wide. This is caused by the halo of the propagating thermal wave. Even the relatively long time for this picture is one tenth of the time necessary in DPCT.

By analogy with DPCT, the thermograms measured here can be analyzed quantitatively [8]. At 0.5 V the microdefects in Fig. 3 are responsible for about 50% of the integrally measured injection current of 230 mA. The main shunt and all edge shunts together carry 8-10 mA each. The homogeneous injection without these shunts would be around 20% of the measured current. This dominance of the microdefects due to their large area would be underestimated in a qualitative interpretation, since the thermal signal at the main shunt is much higher. One should consider that interpreting a thermogram as the locally flowing injection current implies a constant voltage over the whole cell and a negligible series resistance. This usually applies to our measurements.

Since the presented IR technique is similar to the earlier used DPCT, the results on one sample are very much alike. The IR system is advantageus because of a much better lateral resolution due to a higher possible modulation frequency and to the microscopic objective used, and in general because it is a contactless method. But the main advantage is the drastically reduced measurement time necessary for the same thermal sensitivity. The dominant shunts of typical solar cells occur as early as after one minute. Thus, being fast and non-destructive, this system can be used even in the production control, irrespective of a specific cell type and size.

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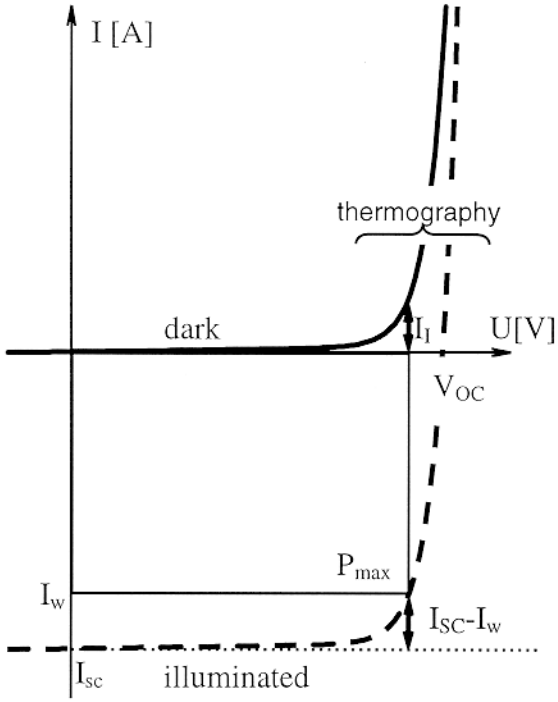

Fig. 1: In thermography the inhomogeneities of the current losses (I_{SC}-I_w) close to the working point and V_{OC} are monitored by the dark injection current I_I at this voltage.

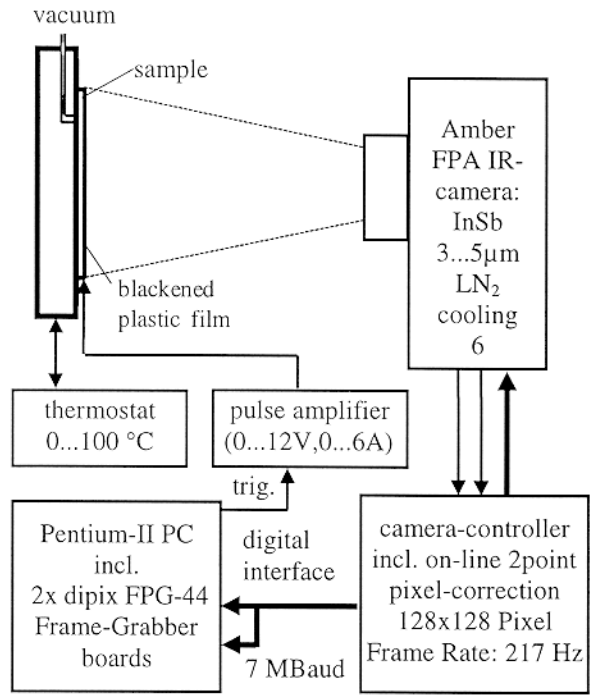

Fig. 2: The schematic layout of the IR lock-in thermography system used.

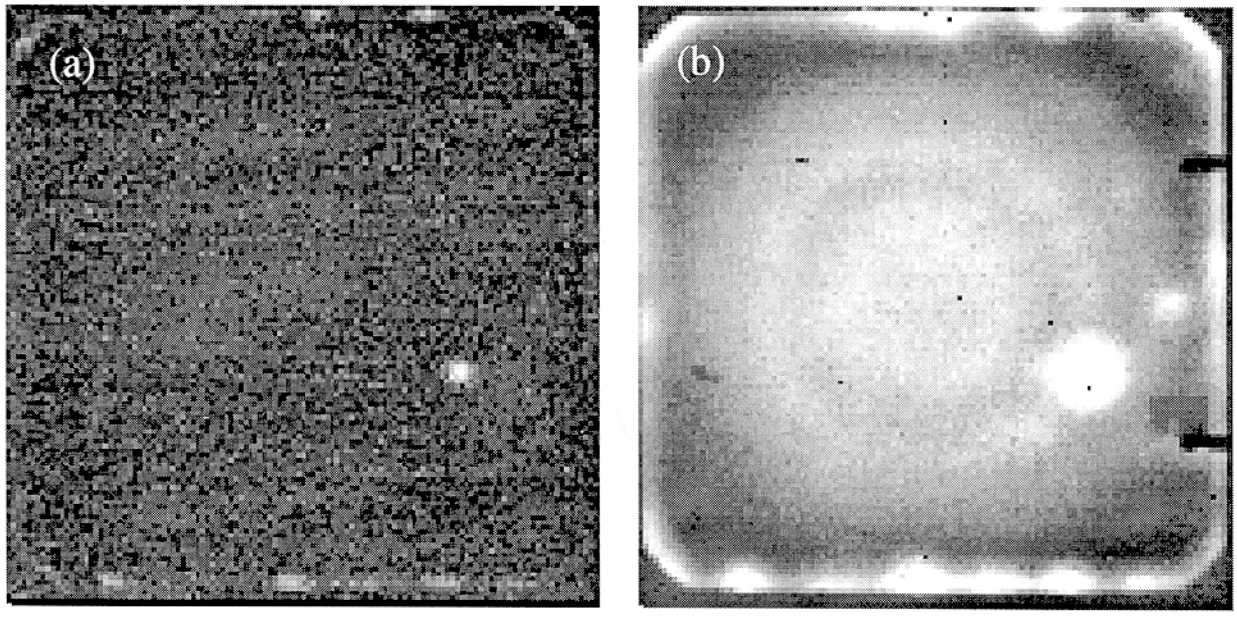

Fig.3: IR thermogram of a 10*10 cm² monocrystalline silicon solar cell at a forward bias of 0.5 V at 13.5 Hz. The main shunt and a few edge shunts already occur after one of minute measurement time (a). The weak ring structure in the right picture caused by grown-in microdefects appears after one hour.

ENHANCEMENT OF DIFFUSION LENGTH IN MULTICRYSTALLINE SILICON BY EXTENDED HIGH TEMPERATURE ALUMINUM GETTERING

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ABSTRACT

While aluminum gettering has been shown to be successful in improving minority carrier diffusion lengths in single-crystal silicon by removal of metal impurities, results have been less promising with multicrystalline silicon wafers for solar cell applications. These wafers have localized regions of high dislocation and precipitate density which do not respond to the usual aluminum gettering anneals below 850°C as applied in solar cell manufacturing or even upto 1000°C for short times as reported in the literature. This is principally because the precipitates dissolve very slowly and continue to supply metal atoms to the surrounding silicon during gettering. It is shown that doing aluminum gettering at higher temperatures for extended times allows more complete dissolution of precipitates and gettering of the dissolved metal atoms. Annealing at 1100°C for 4 h with a 1 μm aluminum layer on both surfaces of 4" square wafers was shown to improve diffusion lengths at all locations in the gettered area, especially at those locations where the original diffusion length was low.

INTRODUCTION

Gettering schemes such as Al gettering and P indiffusion gettering show promise for use in Si solar cell fabrication for improving the cell efficiency[1,2]. The gettering of contaminants which are usually transition metals involves the metal dissolution (if existing in a precipitated form), the diffusion of metal atoms to and their being stabilized at the gettering sites. Al gettering is performed by annealing Si wafers with an Al layer on the wafer surface, which provides a gettering effect because the solubility of typical metal contaminant species is much higher in Al than in Si, thus creating a driving force for the metal species to segregate into the Al layer from the Si bulk. If the annealing temperatures used are above the Al-Si eutectic temperature of 577°C, then a liquid Al-Si alloy layer is formed on the surface of the Si wafer, which may have even higher solubility for metals and thus provide an even stronger gettering effect. Al gettering has been shown to successfully getter specific metal species from Si[3,4] and to result in improved minority carrier diffusion lengths[5-7] in single crystal silicon wafers.

Al gettering has been less successful when applied to multicrystalline silicon(mc-Si) wafers. These often contain localized regions with high dislocation and precipitate density, which have very low diffusion lengths and are practically unresponsive to gettering treatments[8,9]. A major fraction of the metal atoms is in the precipitated, immobile form in these poor quality regions, and thus is inaccessible to gettering. Only the dissolved, mobile metal atoms can be gettered, whereupon the precipitates dissolve further. Long times may be required for complete dissolution of the precipitates and gettering of the dissolved impurities, e.g., upto 60 h at 700°C[10]. Thus, it is not surprising that the gettering treatments applied conventionally at temperatures less than 850°C for a couple of hours or even at higher temperatures upto 1000°C for short times are not successful in improving the diffusion lengths in the poor quality regions.

The present experiments were undertaken to explore the possibility of doing Al gettering at high temperatures for extended times so as to allow complete dissolution of precipitates and gettering of the dissolved impurities.

EXPERIMENTAL

The present experiments used 4" sq matched, mc-Si wafers, with a starting thickness of 400-450 μm. The wafers were RCA cleaned, etched with a 3:5:3 solution of hydrofluoric, nitric and acetic acids to remove about 15 μm from both surfaces, and RCA cleaned again. Diffusion length

maps of the wafers were measured using the ELYMAT technique[11]. In this technique, the silicon wafers are immersed in a dilute HF electrolyte, and it is desirable that the reverse leakage current at the wafer-electrolyte junctions is low. The etching and cleaning procedure was found necessary to remove surface saw damage and expose clean wafer surfaces with leakage currents sufficiently low for measurement. After measurement, the wafers were RCA cleaned again and 1μm Al layers were deposited on half of both surfaces of the wafers by evaporation. After Al deposition and prior to annealing, the wafers were cleaned by boiling in organic solvents and rinsed in deionised water.

For annealing of the Al-deposited mc-Si wafers at high temperature for a long time, it was not possible to use cleanroom furnaces as these would be irreversibly contaminated. Instead, a small quartz container was designed and fabricated that could sit inside a table-top box furnace chamber. This container could be disassembled and cleaned by wet processing. After the wafers were cleaned separately, upto four of them could be stacked inside the clean container and the container could then be reassembled and inserted into the furnace chamber for annealing. A gas injector tube, also made of quartz, could then be used to maintain a suitable inert gas flow through the container. Annealing of the wafers was done in this manner at 1100°C for 4 h in a high-purity nitrogen flow. After insertion of the quartz container with the sample wafers at room temperature, it took about 100 min for the annealing temperature of 1100°C to be attained. At the end of the anneal, the samples were allowed to cool in the furnace to about 550°C in about 40 min with the furnace door closed and then cooled to room temperature with the furnace door open. As the wafers were vertically stacked, the Al-Si alloy layers on the surfaces of the wafers could be seen to have flowed down during the anneal, since the alloy layer had been liquid above the eutectic temperature.

The alloy Al-Si layers were then etched off and in addition, at least 15-20 μm of Si had to be etched off from both surfaces with the etching solution described above before a sufficiently low leakage current for ELYMAT measurement could be obtained. In trial experiments with single crystal silicon wafers, such large thicknesses did not need to be etched off to eliminate the high leakage current caused by the Al-doped p+ surface layer. It is possible that in case of mc-Si wafers, the Al diffused to a greater depth along the grain boundaries.

RESULTS AND DISCUSSION

Figure 1 shows diffusion length maps of a sample wafer before and after the gettering anneal. After annealing, the half which had Al gettering layers on both sides is seen to have higher diffusion lengths than before, while the half that did not have the Al gettering layers is seen to have significantly lower diffusion lengths than before. Figure 2 shows histograms of the diffusion length values before and after the anneal in the half that had the Al gettering layers. It is seen that after gettering, the distribution of diffusion length values is clearly shifted to the higher end of the scale and also has a narrower width. The same scale has been used in the adjacent figures to allow direct comparison. It is significant that unlike earlier experiments, there is a clear improvement in the diffusion lengths in the poor quality regions that are characteristic of mc-Si wafers. The extended time at high temperature has allowed substantial dissolution of precipitates and gettering of the dissolved metal atoms, thus resulting in improved diffusion lengths in these poor quality regions. In addition, the high temperature and long time employed may have contributed to the impovement in diffusion length from mechanisms such as residual stress relief, defect annihilation[12], promotion of precipitate dissolution and impurity atom release due to dislocation climb etc.

The gettering treatments applied in earlier experiments were not adequate to allow sufficient dissolution and gettering in the poor quality regions, even though they did yield improvement in other regions which were of relatively high quality to start with. In some experiments reported in the literature, diffusion lengths were even found degraded after the gettering anneal, as the dissolved impurity concentration was greater than before the heat treatment due to incomplete gettering[8,9]. Poor quality regions in mc-Si wafers can be extremely detrimental to solar cell performance because they can act as sinks that dissipate power internally within the cell[13]. Thus, it is desirable to not only have high diffusion lengths on average but also to have a narrow

distribution of diffusion lengths[14] with the elimination of low diffusion length regions. In the present experiments, such an effect is achieved as illustrated in the histograms in Figure 2. In fact, the effect is underplayed as the ELYMAT technique used by us cannot resolve diffusion lengths lower than about one-fifth the wafer thickness. Hence, the diffusion length values at the lower end of the scale in the initial diffusion length map may in fact be even lower.

The improvement in diffusion lengths is not as pronounced at the higher end of the scale, i.e., in those regions which initially had high diffusion lengths. This may be because the gettering is limited by the segregation coefficient at the high gettering temperature employed[15]. This limitation may possibly be overcome by using a variable temperature gettering anneal, which starts at a high temperature and ramps or steps down gradually to lower temperatures[16]. The half of the wafer without the Al gettering layers is seen to have strongly degraded diffusion lengths. While this may be partially due to the dissolution of precipitates and resultant increase in the dissolved impurity concentration, a much higher contribution is due to contamination from the furnace environment, as the annealing has not been done in standard cleanroom furnaces. One reason why Al layers were deposited on both surfaces of the mc-Si wafers for gettering was to protect the wafers from excessive furnace contamination that might overcome and mask the gettering effect. After a few annealing cycles, the quartz chamber itself became too contaminated due to repeated high temperature exposure to an unclean environment and could not adequately protect the wafers.

SUMMARY

Extended high temperature Al gettering is shown to be successful in improving diffusion lengths in poor quality regions of mc-Si wafers. The resultant narrow distribution of diffusion lengths with elimination of localized low diffusion length regions is desirable from the point of view of solar cell operation. Further improvement of diffusion length may be limited at the high annealing temperature used due to a limited segregation coefficient, and this limitation may be overcome by using a variable temperature gettering that starts at high temperatures and gradually ramps down to lower temperatures.

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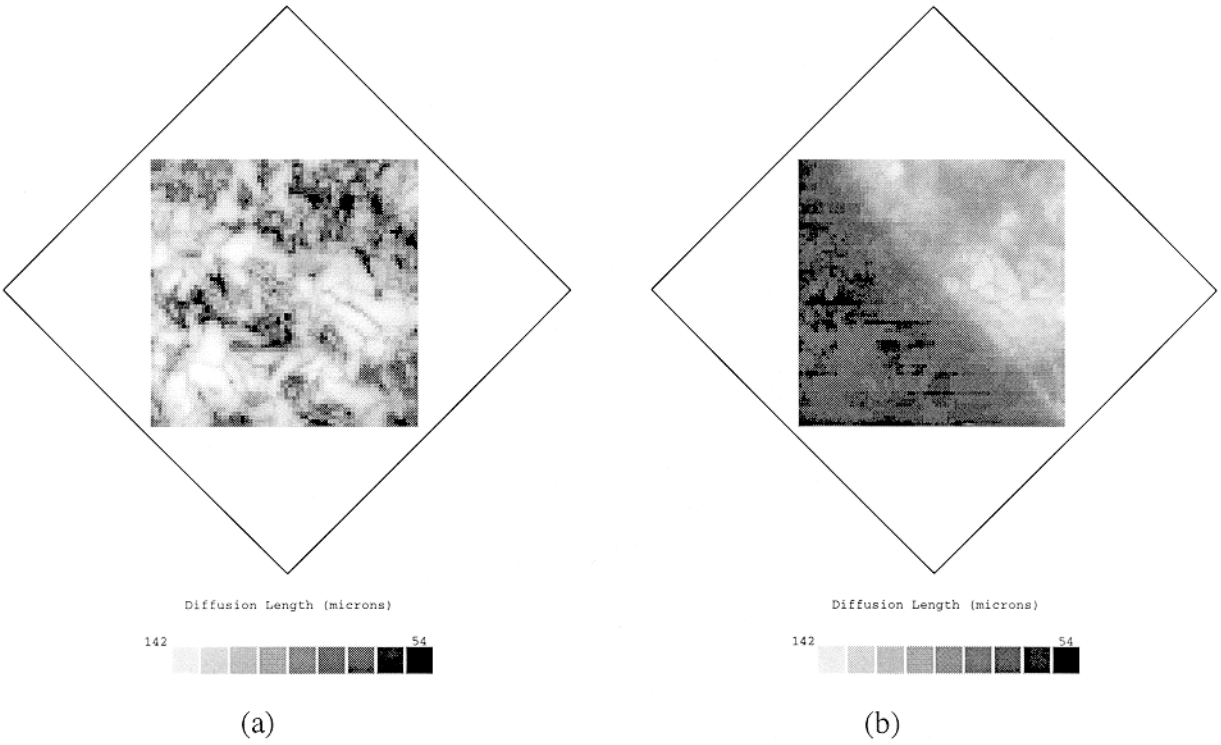
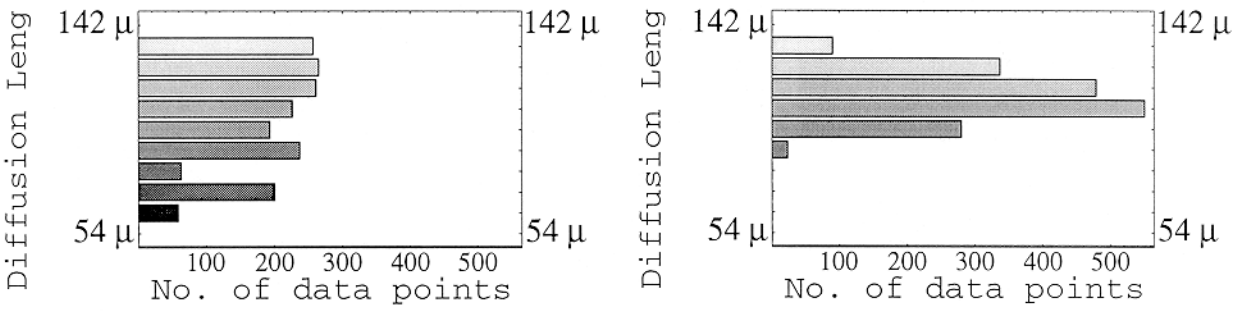


(a) (b)

Fig.1 Diffusion length maps of the same multicrystalline wafer : (a) Initial; (b) After annealing at 1100°C for 4 h with an Al gettering layer on both sides of half of the wafer. The initial diffusion length map has local regions of very low diffusion length. After gettering, the Al gettered half has much higher diffusion lengths than the ungettered half.



(a) (b)

Fig.2 Histograms of diffusion length values in the aluminum gettered half only as obtained from the diffusion length maps of Figure 1 : (a) Before gettering as seen in Fig. 1(a); (b) After gettering, as seen in Fig. 1(b). After gettering, the diffusion length distribution is clearly narrower and pushed to the higher end of the scale.

Submicron Diffractive Gratings for Thin Film Solar Cell Applications

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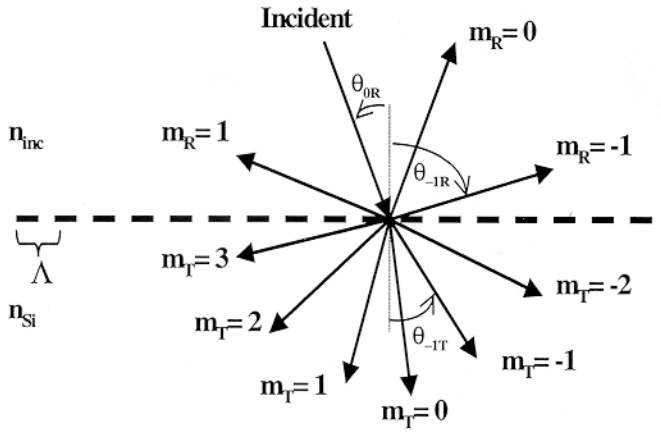
Abstract
Surface texturing with submicron diffractive gratings in Si is employed to enhance solar spectrum absorption. Extensive modeling with rigorous coupled wave analysis codes confirms experimental measurements of reflected light as a function of wavelength. Subsequently, these codes are used to predict optimal diffractive grating configurations for thin Si cells that will simultaneously reduce reflection at the air/Si interface, efficiently couple light into diffracted orders that remain near the interface, and reduce the propagating light that is not diffracted but is transmitted straight through the Si.

Introduction
Diffraction gratings can be utilized to great advantage in solar cell applications. They can reduce light lost to reflection at the air/Si interface. This can be accomplished by reducing the number of reflected orders to just the zero reflected order with a grating whose pitch is less that the incident wavelength of light. In this case, the layer can be considered as a homogeneous layer of artificial index. Thus, with the proper choice of grating duty cycle and grating depth, the bulk Si will be index-matched to air and little or no light is lost in reflection. Moreover, this type of anti-reflection treatment is very broadband, compared to a thin film coating, and is therefore well-suited to the broad solar spectrum.

Decreasing the Si thickness is economically advantageous, attractive for low-weight applications, and desirable from a loss mechanism viewpoint where the optimum thickness should be a fraction of the minority carrier diffusion length [1]. However, the required absorption length is a function of the wavelength of light, increasing with increasing wavelength. One way to accommodate this effect in a thin Si solar cell is to redirect the light propagating within the Si along a path that is nearly parallel to the Si interface. At the same time, the efficiency of the light that propagates straight through the Si solar cell should be reduced for long wavelengths.

The above requirements can be accomplished simultaneously with a single frequency diffractive grating. The grating notation used in this discussion is shown in Figure 1, where Λ is the grating pitch, m_R are the reflected grating orders, Θ_R are the associated reflected angles, m_T are the transmitted grating orders, Θ_T are the associated transmitted angles, and λ_o is the wavelength of light in a vacuum. The grating equation that relates the diffracted angle to the incident angle, wavelength of light, and material parameters is also given in Figure 1.



$$n_{inc} \sin\theta_{inc} - n_{Si} \sin\theta_{diff} = \frac{m\lambda_\circ}{\Lambda}$$

Figure 1. The grating equation and corresponding grating notation.

In this discussion we use a normal incidence configuration so that $\Theta_{inc} = 0$ degrees. Figure 2 shows the diffracted angle of the transmitted light within the Si substrate as a function of wavelength. Also shown are curves of the minimum diffraction angle required for a specific substrate thickness. These curves follow from the absorption coefficient of Si [2].

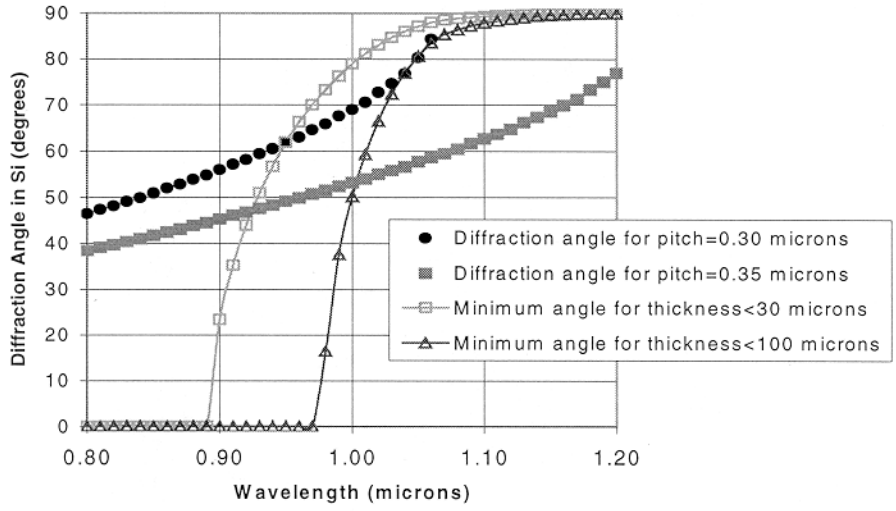
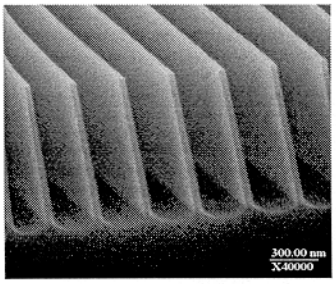


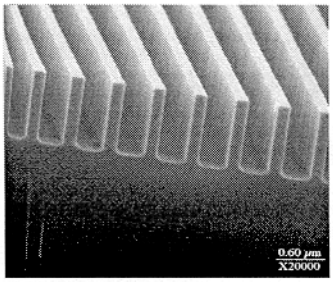
Figure 2. Diffraction angle as a function of wavelength for normal incidence.

Measurements and Predictions

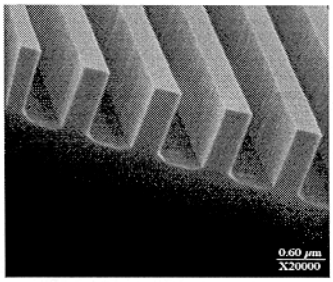
A rigorous coupled wave analysis code [3] was used to predict the reflected efficiencies and confirm the experimental results shown in Figure 3 for the gratings below. Here, hemispherical reflectance refers to the sum of the efficiencies for all of the reflected orders.



Period = 300 nm.



Period = 500 nm



Period = 1000 nm

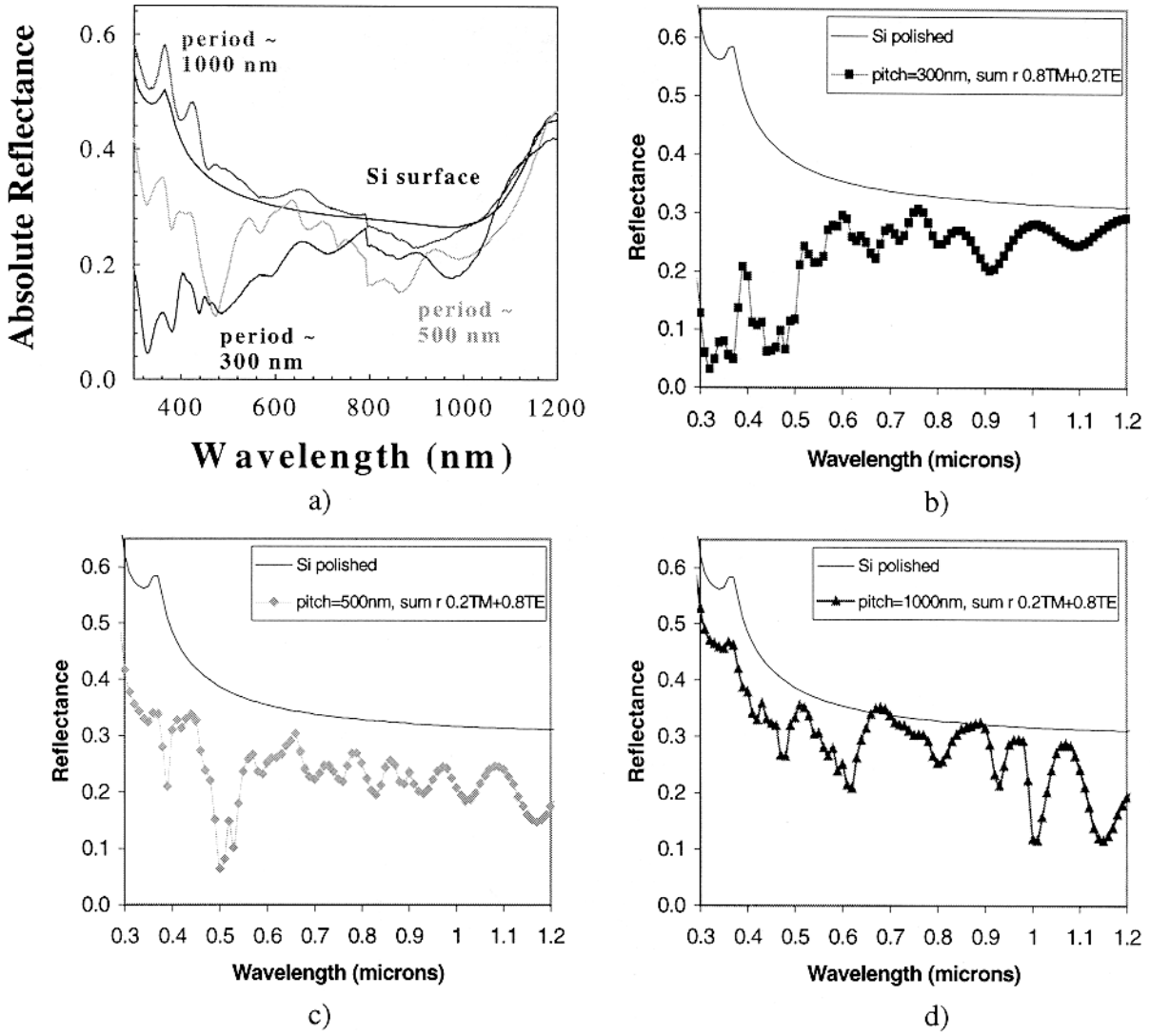


Figure 3. a) Measured hemispherical reflectance for the three gratings shown and a polished Si surface for reference. b)-d) Predicted hemispherical reflectance for the illustrated gratings above. The incident light is mostly linearly polarized and is designated TE if the E-field of the incident beam is parallel to the grating grooves.

In general, the model efforts agree with the above experimental results. One notable exception is the anomalous increase in reflectance present in all experimental configurations, including the polished Si surface. Theoretical modeling indicates that this increase in reflectance is actually light transmitted through the Si substrate, reflected at the back surface and retransmitted through the substrate. The advantage of modeling is that we can not only predict how much light is reflected, but also if light is efficiently coupled to the desired transmitting order. The above configurations are not optimal for this task.

Optimal Grating Designs

Next, we present two designs that approach our goals of minimum reflectance and maximum coupling of light into higher transmitted orders, especially for long wavelength light. Both designs have a pitch of 0.35 μm so that the +/- 1st transmitted orders within the Si are diffracted at angles of approximately 60 degrees, for wavelengths above 1μm. With this

constraint, the grating depth and duty cycle (linewidth divided by pitch) are adjusted to maximize coupling into the higher transmitted orders and to minimize coupling into the reflected and transmitted zero orders. Figure 4 illustrates the results of an optimal rectangular profile grating and an optimal triangular profile.

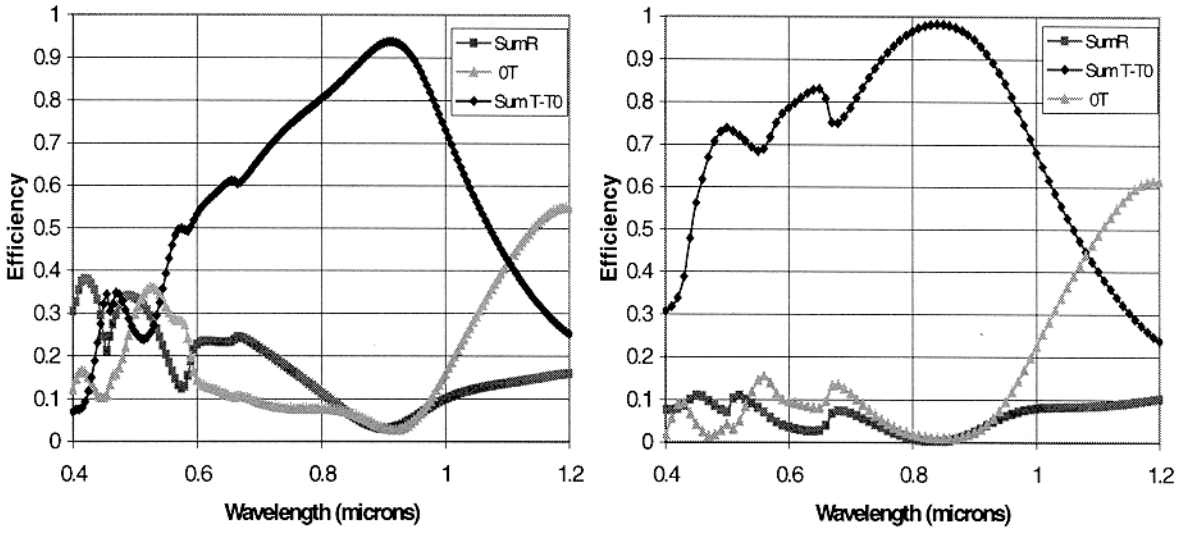


Figure 4. Coupling efficiencies for a) an optimal rectangular profile grating with depth=0.2μm and duty cycle=0.75 and b) an optimal triangular profile with depth=0.24μm and duty cycle=0.50.

The grating solution shown in Figure 4b) illustrates the excellent broadband antireflection response common to triangular profiles. Note that the exchange of energy between the higher order transmitted light and the zero order transmitted light is a function of the grating period. This crossover will move to the red end of the spectrum with increasing pitch, but with an accompanying smaller diffraction angle in the higher orders.

Conclusions

Theoretical modeling for grating design in solar cell applications saves fabrication time and effort when searching the large parameter space spanned by grating pitch, profile, depth, and duty cycle. Moreover, modeling allows us to direct light energy to specific orders within the substrate, a task that is difficult to characterize experimentally. In this project, we have identified two grating configurations that will each enhance solar cell absorption across the solar spectrum, particularly near the band-edge, by simultaneously directing the transmitted light to the appropriate orders while minimizing the light lost to reflection. Both grating profiles are simple solutions and can be fabricated with current technologies.

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High Current, Thin Silicon-on-Ceramic Solar Cell

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Introduction

Thin-film polycrystalline silicon solar cells offer the potential to achieve photovoltaic power conversion efficiencies greater than 19%. By utilizing light trapping and back-surface passivation, high efficiencies can be achieved. The optimal thickness for thin, light-trapped silicon devices is 20 [1] to 35 μm [2]. AstroPower has developed a solar cell device comprised of a 20 micron thick layer of silicon prepared on a ceramic substrate, designed to effect light trapping and back-surface passivation. This device has resulted in a short-circuit current of 25.8 mA/cm^2 (verified by NREL).

Discussion

The solar cell device was developed using a standard silicon process shown in Table 1. A modified RCA clean was used to remove organics, metals, and oxides. Since our ceramic is insulating, an all top contact design was employed. Photolithography was used to define the n and p contacts.

Table 1. Experimental process for thin-film silicon on ceramic

1.	Ceramic is tape cast and sintered to a final thickness of 32 mils.
2.	Silicon is deposited and grown (10 – 30 μm).
3.	NaOH texture etch for front surface texture (5 min. @ 90°C).
4.	RCA clean.
5.	Junction diffusion @ 850°C with $POCl_3$ as dopant source.
6.	HF strip to remove phos-glass layer.
7.	Plasma etch to isolate the active area (0.6 cm^2).
8.	Photolithography to define n and p contacts.
9.	Evaporate all top contacts (n - Ti / Pd / Ag ; p - Al).
10.	The n – contact is plated in silver solution to a thickness of 20 μm.
11.	The anti-reflection coating is a 2 layer PECVD.

Figure 1 shows a cross-section of a 20 μm silicon layer with p-contact and isolation region on a ceramic substrate. The silicon layers are p-type with bulk resistivities ranging from 1-5 Ω·cm.

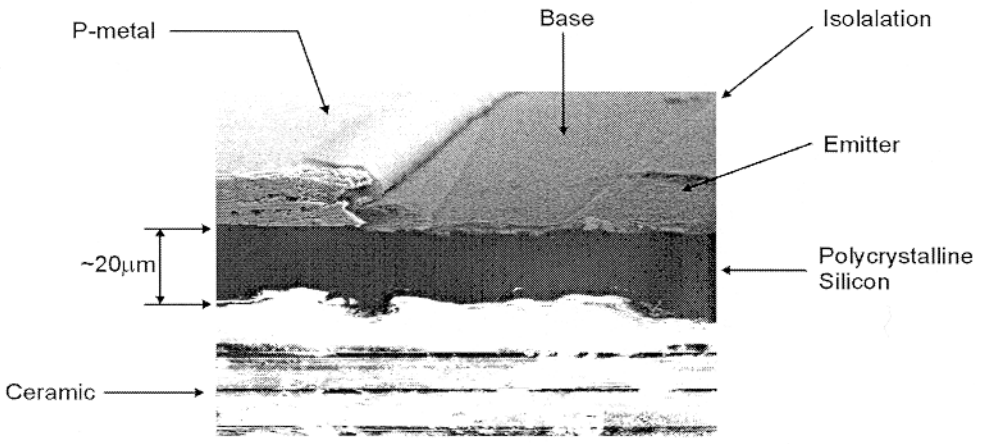

Figure 1. SEM cross-section of 20 micron thick silicon on ceramic

The quantum efficiency measurements for the 25.8 mA/cm^2 device shown in Figure 1 indicate that it has a strong response at the infrared end of the spectrum. This is illustrated in Figure 2. Along with the measured EQE data are curves generated using the PC-1D [3] model. Curve 1 shows the modeled response of a thin silicon layer with excellent minority carrier bulk properties (minority carrier lifetime = 3.5 μs), but high levels of recombination at the surfaces (S_b=10^6 cm/s) and no internal reflection. Curve 2 models the same device with ideal rear surface passivation (S_b=0 cm/s). Curve 3 adds light trapping properties to the device. Both front and rear surfaces are modeled with 90% diffuse reflection. A comparison of Curve 3 and the experimental data indicate the device under study must have high lifetime, high levels of surface passivation, and good light trapping properties to achieve the long wavelength response and high currents tested.

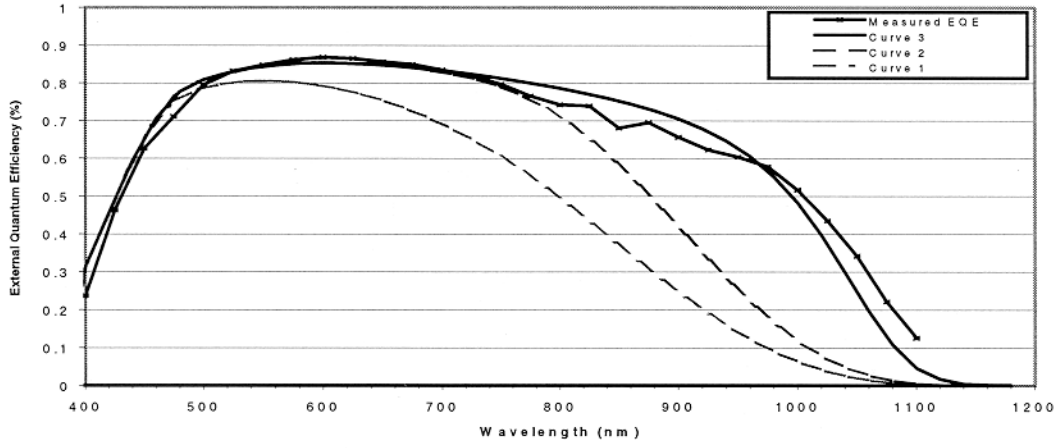

Figure 2. Modeled and experimental quantum efficiencies for a 20 micron thick silicon on ceramic device.

Conclusions

Both light trapping and back-surface passivation have been demonstrated for a thin-silicon solar cell device design employing a ceramic substrate. We believe the achievement of a short-circuit current of 25.8 mA/cm^2 represents the highest short-circuit current observed on a thin (less than 30 micron) layer of silicon grown on a dissimilar substrate. This short-circuit current result for thin silicon and the development of the electrically insulating substrate on which it was grown are major milestones in the development of monolithic, series-connected sub-modules based on polycrystalline silicon.

Acknowledgment

The authors would like to acknowledge the support of the Department of Energy through the Thin Film Photovoltaic Partnership Program administered by the National Renewable Energy Laboratory.

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EMISSIVITY MEASUREMENTS AND MODELING IN SILICON - SOME OBSERVATIONS

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ABSTRACT

Research groups at NJIT and NREL, in collaboration with industry, have been performing joint research on understanding the emissivity of silicon and silicon-related materials. This research study has focussed on understanding the influence of surface roughness, doping, wafer thickness and layers on the emissivity of silicon. Experimental measurements have been performed using a spectral emissometer operating in the wavelength range of 1-20μm and temperature range of 30-900°C. Interesting differences in the optical properties have been reported due to differences in wafer surface morphology. Simulation of the wavelength and temperature dependent emissivity of silicon has been performed using ray optics that considers effects of multiple-reflection and light trapping due to rough surfaces/interfaces as well as changes in carrier concentration.

I. INTRODUCTION

For semiconductor device processing techniques such as Rapid Thermal Processing (RTP), Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD), pyrometers are the instruments of choice for non-contact, in-situ temperature measurements. Pyrometers measure the amount of radiation emitted from a wafer within a narrow wavelength window. The ratio of the wafer emitted radiation to that of a blackbody under the same conditions of temperature, wavelength, angle of incidence and direction of polarization is referred to as emissivity. Emissivity of silicon is a complicated function of both temperature and wavelength [1]. It is also a function of surface roughness [2,3]. The temperature and wavelength dependent emissivity of silicon has been studied extensively in the literature. *However, studies of optical properties of silicon, as a function of doping concentration, surface roughness and the presence of overlayers, that covers a wide and continuous range of wavelengths in the infrared is lacking.*

Absorption mechanisms in the infrared range of wavelengths for silicon have been studied in detail in the literature [4]. The absorption mechanisms are (a) above fundamental edge in the range of 0.4-0.6μm [5], (b) fundamental edge in the range of 0.6-1μm [6], (c) free carriers in the range of 1.5-5μm [7], and (d) phonon absorption for $\lambda > 5\mu m$ [1]. These mechanisms have been modeled mathematically, and the results have been included into various models that aim at predicting the emissivity of silicon for non-

contact temperature measurement techniques in semiconductor processing, for example, rapid thermal processing (RTP) [8,9]. In a detailed study, Spitzer and Fan have reported that an additional absorption mechanism occurs for n-Si in the form of a band that peaks at $\lambda = 2.3\mu m$ [10]. In their study, four dopant materials and doping concentration range of 1.4×10^{16}-$10^{19}cm^{-3}$ have been utilized to investigate the absorption phenomena in the wavelength range of 1-45μm at low and room temperature. Spitzer and Fan [10] have speculated that this feature may have been associated with excitation of carriers from the conduction-band minima or, at low temperatures, from the impurity levels to a higher lying energy band.

II. EXPERIMENTAL DETAILS

The spectral emissometer utilized in this study has been discussed earlier [11,12]. It consists of an hemi-ellipsoidal mirror providing two foci, one for the exciting source in the form of a diffuse radiating near-blackbody source and the other for the sample under investigation. A microprocessor controlled motorized chopper facilitates simultaneous measurement of sample spectral properties such as emittance, reflectance and transmittance. A carefully adjusted set of five mirrors provides the optical path for measurement of the optical properties. An oxy-acetylene/propane torch provides the source of heating of the samples. The spectral emissometer utilizes the Helmholtz reciprocity principle [13] as has been explained in a related study [14]. The sample utilized in the study is a double-side polished p-Si wafer of orientation <100>, thickness t = 250-275 microns and resistivity ρ = 10-100Ω·cm. This resistivity translates into a dopant concentration of $7\times10^{14}cm^{-3}$. At temperatures above 359°C, the thermally generated free carriers are in excess of $8.9\times10^{15}cm^{-3}$ and the sample is in its intrinsic regime.

III. RESULTS AND DISCUSSION

Fig.1 shows the temperature dependent measured and simulated transmittance (based on the MIT multirad model [15]) for the silicon sample considered in this study. Four specific temperatures in the intrinsic regime have been considered here. Based on the measured transmittance data, the absorption coefficient has been extracted as function of temperature. The absorption values show a trend that is related to the free carrier absorption, which is proportional to λ^2 [7]. The temperatures included in this study are within the intrinsic regime of the sample. Hence, the doping type is not of any significance. In the extrinsic regime, p-Si is not expected to exhibit the absorption band at 2.3μm. This observation has been made by Fan et al. [16]. Since the intraband transitions for the valence band are forbidden at k = 0, the transitions off k = 0 will only give rise to a very broad featureless absorption band. Thus, one would expect a broad background contribution to the absorption coefficient, α, but with no discernible peak. In the temperature range of 5-297K, Spitzer and Fan have also shown that the peak location is temperature independent. In order to examine the existence of this band, we have plotted the y-axis as α/λ^2. These results are presented in Fig.2. For temperatures above 470°C, the normalized data in Fig.2 show the 2.3μm absorption band and reveal the same general feature as seen by Spitzer and Fan [10] for n-Si. It has been reported by Fan et al. [16]

that, for p-Si at room temperature, the absorption coefficient rises smoothly as λ^2 characteristic of free carrier absorption. As stated before, the p-Si used in the present study has a low doping concentration of $7\times10^{14}cm^{-3}$. At temperatures corresponding to 479°C, the thermally generated free carriers exceed this number, reaching $7.6\times10^{16}cm^{-3}$, causing the silicon to be in its intrinsic regime. In this case, there exist an equal number of electrons and holes. Thus, the band that arises and peaks around $\lambda \sim 2.3\mu m$ is a result of conduction intraband transitions. To the best of our knowledge, this is the first time that the observations of the 2.3μm absorption band as function of temperature, at temperatures exceeding 300K, is reported in the literature. As expected, the intensity of the peak rises as function of temperature as can be seen in Figs.2(c) and 2(d) because of the increase in concentration of thermally generated electrons. The position of this absorption band is revealed to be essentially temperature independent consistent with its identification with the conduction band gap of ~0.5eV. The splitting of the conduction band as noted by Hensel et al. [17] is not expected to show significant temperature dependence.

IV. CONCLUSIONS

Absorption mechanisms in silicon, modeled in the literature, have not considered the absorption band rising due to transitions of electrons in the conduction band. Spitzer and Fan have first observed this conduction band in n-Si at low and room temperatures. In the above study, the first experimental evidence of the occurrence of this band has been shown in p-Si at elevated temperatures in the intrinsic regime.

ACKNOWLEDGEMENTS

This work was partially supported by grants from NREL, DARPA and SEMATECH.

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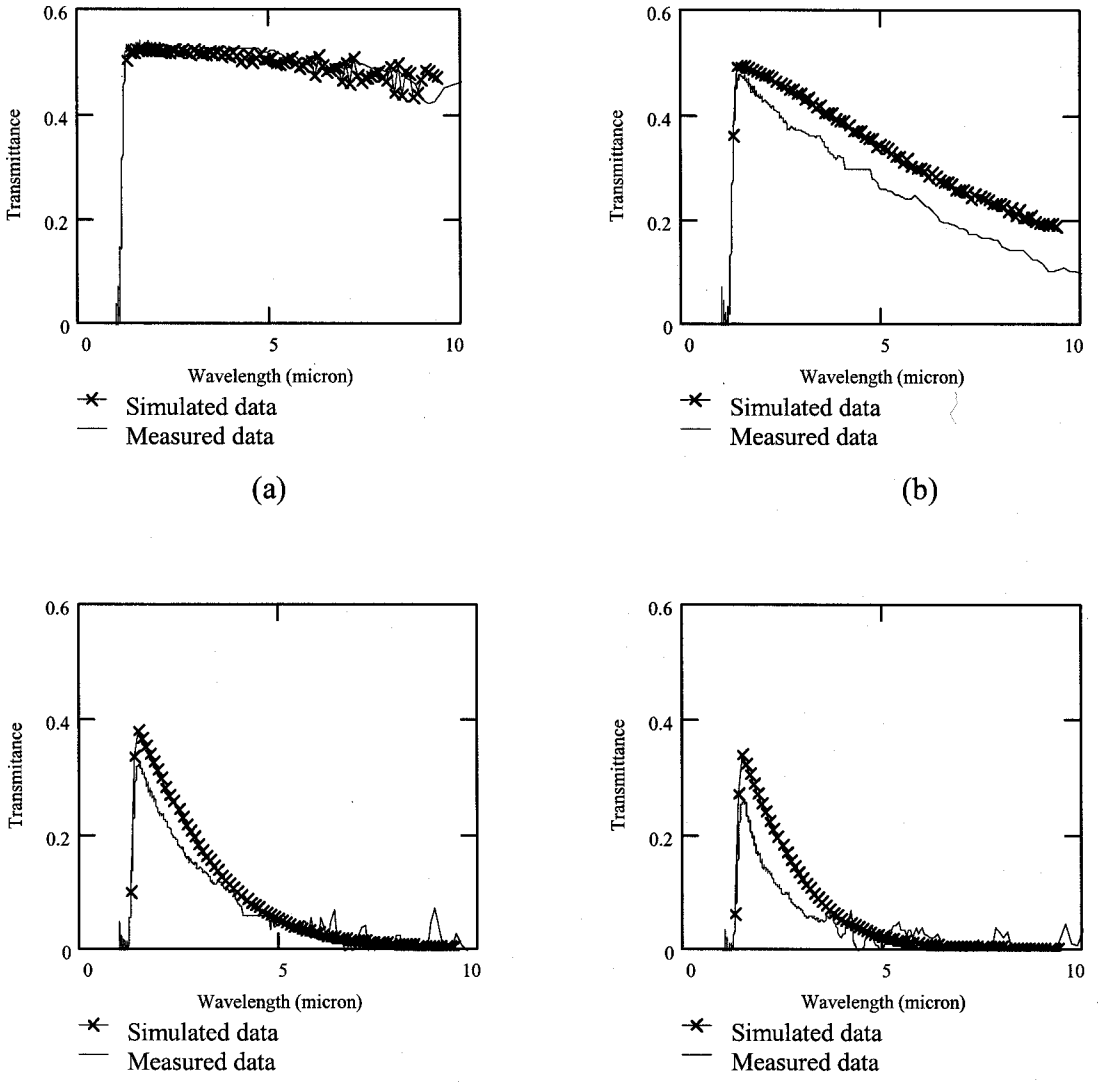

Fig.1 Temperature dependent measured and simulated transmittance for p-Si, $7\times10^{14}cm^{-3}$ for: a) 359, b) 479, c) 605 and d) 632°C

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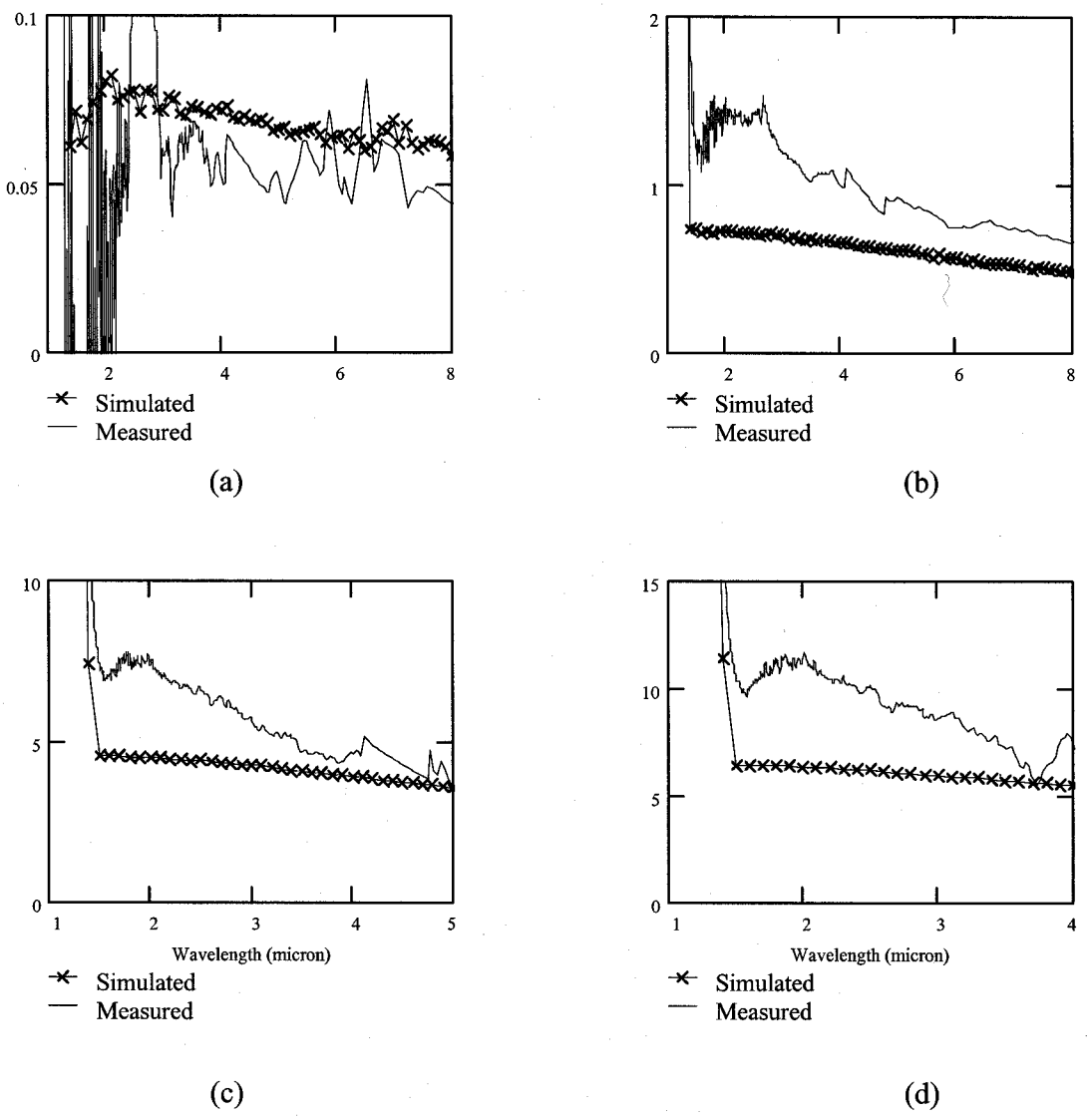

Fig.2 Comparison between the ratios of the measured and simulated absorption coefficient divided by λ^2 for p-Si, $7\times10^{14}cm^{-3}$ for: a) 359, b) 479, c) 605 and d) 632°C

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Gettering of p-type Silicon Using Ti Thin Film

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Metallic impurities in silicon introduce g-r centers within the bandgap. Eliminating and controlling these centers is a fundamental task of semiconductor technology. Cost effective external gettering for PV technology includes Al backside external gettering whose effectiveness depends on impurity diffusion length, time and treatment temperature. The objective of this work is to develop a gettering strategy using a thin metal film deposited on the top side of the wafer. For this purpose titanium has been selected, since oxidized Ti also functions as an antireflective coating. A standard Ar plasma sputtering system was used with N_2 added for near surface nitridation in order to change the surface condition during the deposition. Three getter thin films- Ti, Al/Ti stack, and Ti/Al alloy of thickness 60 nm were deposited. The efficiency of the gettering procedure has been monitored using μ-PCD, DLTS and SEM-EBIC and compared with standard Al external getter. To obtain more specific understanding of the Ti gettering process, p-type CZ silicon wafers with resistivity of 14-25 Ωcm were intentionally contaminated with Ni and Fe impurities. A low (500^0C/300 min) and a moderately high (700^0C/150min) annealing temperature were used in a N_2 atmosphere. The lifetime data were used to optimize the temperature and plasma conditions. The DLTS measurement were carried out for the "best" samples. The lifetime degraded from ~30 μs to below 5 μs for both Fe and Ni contaminated wafers. The Fe-B pair concentration was $3x10^{13}$ cm^{-3} or 10^{12} cm^{-3} on the front surface for Fe and Ni wafers, respectively.

In high temperature gettering (700^0C), lifetime improvement was observed for Ti and Ti+Al stack film getters, for both Ar and Ar/N_2 plasma conditions. The Fe-B pair concentrations measured using DLTS was equal to $4x10^{10}$ cm^{-3} and about 10^{10} cm^{-3} for Fe and Ni contaminated wafers. The lifetime data was comparable to the lifetime data for Al external getter, where an Fe-B concentration of $3x10^{10}$ cm^{-3} has been found for both Fe and Ni contaminated wafers. Low temperature gettering (500 ^{0}C) reveals a similar efficiency for Ti and Ti+Al stack film getters as for standard Al films, with Fe-B concentrations of $2x10^{11}$ cm^{-3} and 10^{11} cm^{-3} measured for Fe and Ni, respectively, while for Al getter the measured concentrations were $8x10^{11}$ cm^{-3} and $3x10^{11}$ cm^{-3}.

Microscopic analysis has revealed large microcrystalline on the film surfaces of the Ti/Al stack. It is worth noting that adding N_2 gas into the plasma results in a color change of the Ti film that can have an impact on the reflection coefficient of the film layer and creates a TiNSi compound. As a result, after etching with a CP-4 solution the wafer surface was smoother than the surface treated with Ar plasma only. The surface roughness and patterns for Ar or Ar/N_2 plasma treatment have been monitored by both the SE and SEM-EBIC images. In conclusion we note that Ti thin film gettering is more efficient than Al for both low and elevated temperatures and Ar/N_2 plasma is recommended for depositing thin Ti film using magnetron sputtering system.

Why is the Open-Circuit Voltage of Crystalline Si Solar Cells so Critically Dependent on Emitter-and Base-Doping?

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ABSTRACT

This paper discusses the critical dependence of the open-circuit voltage (V_{OC}) of crystalline Si solar cells on the emitter and base doping levels. Contrary to conventional models that try to ascribe V_{OC}-limitations to (independent) bulk and surface recombination losses, we suggest, as the dominant mechanism, the formation of a compensated "buffer layer" that is formed as phosphorus is diffused into the p-type (boron-doped) base. The only purpose of the base doping is to optimize the buffer layer. Our calculations show that this model makes the achievement of high V_{OC} and good carrier collection (J_{SC}, FF) interdependent. Sanyo's 'HIT' solar cells are an example of a different method to implement this buffer layer concept for crystalline Si solar cells. The general principle for a V_{OC}-enhancing buffer layer relies on using materials with high lifetimes and low carrier mobilities that are capable of reducing surface or junction recombination by reducing the flow of carriers into this loss-pathway.

INTRODUCTION

The optimization of diffusion-processed crystalline Si solar cells faces the dilemma that the base-doping has to be limited to levels corresponding to resistivities greater a few tenths Ωcm [1]. On the other hand, for cells using a single diffusion phosphorus diffusion step, the doping level of the emitter has to be higher than required for optimum device performance in order to assure ohmic contacts to the screen-printed metal contact grids used on the cells. It is hard, but, within limits, possible, to reconcile this behavior using established solar cell models [2]. Such analyses (have to!) account for the improvements of V_{OC} with increased base doping in terms of reduced dark saturation currents (recombination) in the base. This conclusion is in conflict with the observation that excessive base-doping decreases carrier collection (J_{SC} and/or FF) [1], i.e., appears to enhance recombination in the base. This discrepancy, we suggest, can only be overcome if one is willing to us to question the validity of the prevailing recombination-loss based solar cell models.

In a previous paper [3], we have suggested that it is in principle possible to enhance V_{OC} by inserting a "resistive," low carrier mobility buffer layer near the junction. We also reviewed a number of cell preparation schemes where we believed that this concept had been experimentally realized. The use of resistive layers is often thought to be undesirable because they introduce series resistance losses into the solar cell. However, we argued that a carefully optimized limited additional series resistance can be tolerated and allows maximizing cell performance. This has essentially the effect of shifting the current-voltage [*log*I(V)] dependence "to the right" along the voltage axis, while traditional thinking always looks for improvement by shifting *log*I(V) down to

lower current values. The behavior suggested by us is indeed experimentally observed [1,2, and many other examples in ref. 4]. It is of interest to note that frequently a shift of *log*I(V) to the right, i.e., to higher voltage values, is accompanied by a decrease in the steepness of the *log*I(V) dependence, also reported in Refs. 1 and 2. Traditional considerations would suggest that such flattening of the *log*I(V) dependence would also indicate lower device performance (increase in diode quality factor corresponding to increased recombination losses). However, many examples have been reviewed in Ref. 4 suggesting that a correlation between a diode quality factor and solar cell performance cannot be substantiated experimentally.

PROPOSED MECHANISM

For the investigation of the potential benefit of buffer layers seen as separating the high recombination regions of contacts from the base or absorber layer, we used an analytically solvable method for the determination of "best cases," and thus show the maximum achievable beneficial effects. The approach is based upon:

- Determination/estimation of best case V_{OC} in ideal diffusion diodes as an upper limit of V_{OC} behavior in non-ideal (real) diodes.

- Calculation of local minority carrier concentration m(x) (in $0 \leq x \leq d$) in a homogeneous (Fig. 1a) as well as in an inhomogeneous absorber (Fig. 1b) via 1-dimensional steady-state continuity equation (exclusively diffusion currents) under $\exp(-\alpha x)$ generation with boundary conditions at x=0 and x=d resulting from surface recombination with velocities S_o=S(x=0), and S_d=S(x=d) as a function of layer parameters.

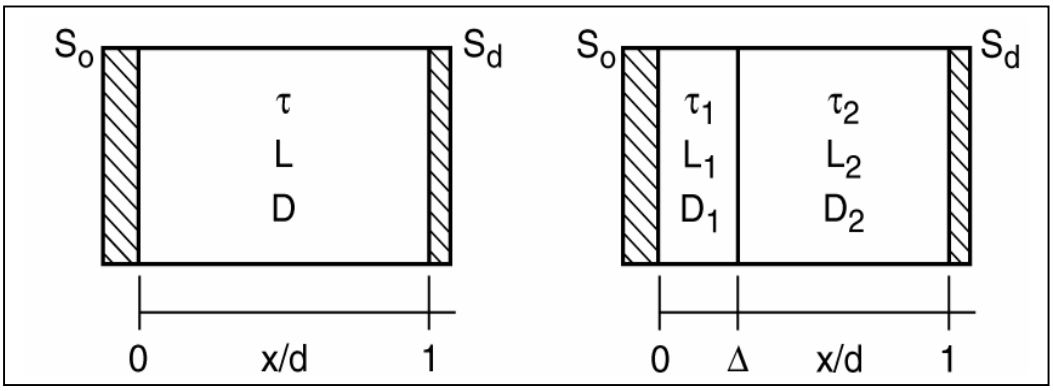

Fig 1a: Schematic of "solar cell" used for calculation.

Fig 1b: Schematic of "solar cell" with a buffer layer of thickness Δ

- The resulting local minority-carrier distribution reads:

$$m_i(x) = A_i \exp[x/L_{m,i}] + B \exp[-x/L_{m,i}] + [(g_o\tau_i)/(1-(\alpha L_{m,i})^2)] \exp(-\alpha x) \quad (1)$$

(with A_i, B_i being dependent in a complex manner on $L_{m,i}$, τ_i, α, S_o, S_d, Δ, and d;

the solution $\alpha L=1$ is excluded for reasons of numerical instability; i=1,2, with i=1 for $0 \le x \le \Delta$ and i=2 for $\Delta < x \le d$).

- The translation of local minority excess carrier densities $m_{phot}(x)$ into the chemical potential and thus the maximum open-circuit voltage V_{OC} is performed via Boltzmann- approximation and the assumption that photogenerated majorities M_{phot} are small compared with their thermal equilibrium concentration M_o:

$$\mu(x) = kT \ln[(m_o+m_{phot})(M_o+M_{phot})/m_oM_o] \approx kT \ln[(m_o+m_{phot})/m_o] \quad (2)$$

where $\mu(x)$ is an ambiguous and monotonous function of m(x).

In Ref. 3 we showed that the introduction of an absorber layers with decreased μ and unaffected τ increases the minority-carrier concentration m(x) continuously with decreasing mobility, or increasing buffer thickness Δ, which means displacing the surface region (at x=0) with its high recombination rate (in terms of diffusion lengths) as far as possible from the junction $x(m_{max})$. Formally, this can be achieved by $L_m \to 0$ (except with $x(m_{max}) \to \infty$). The introduction of buffer layers with unaffected L and decreased τ (i.e., a defect layer) results in an optimum position for maximum excess-carrier density and maximum chemical potential as well. However, such a layer has a tendency to also decrease m(x) near the junction making it a less desirable candidate in comparison with a layer having a reduced carrier mobility.

The operation of solar cells at maximum power point (mpp) conditions requires the extraction of nearly the entire I_{SC} at nearly V_{OC}, which means that the amount of "internally" created (photo- induced) chemical potential $\Delta\mu_{transp.}$ necessary for the transport of minorities to the contacts has to be minimized; because of the introduction of low-mobility buffer layers at current densities according to mpp, some of the internal chemical potential has to be consumed for transport. Our calculations – which due to the large number of parameters have been numerically run only for a limited number of different variables – show that using a buffer layer with reduced mobility the balance of the benefit in V_{OC} equals or is smaller than the losses at mpp.

From an experimental device optimization point, this type of buffer layer leads to a regime in which J_{SC} and fill factor are "traded" for V_{OC}, that is a common observation in many types of cells, and, as an interesting side observation, not necessarily sensitive to the V_{OC}-, J_{SC}-, or efficiency levels of the cell, suggesting that this mechanism is operable whether or not cells are optimized as much as possible. We suggest that the formation of a low-mobility compensated buffer layer that automatically forms in diffusion processed Si would be responsible for this mechanism. If the V_{OC}- enhancing buffer layer can be produced by other means, for example, in "HIT" solar cells manufactured by Sanyo [5], the doping requirements for the cell base become much relaxed. Indeed, Sanyo is using n-type wafers to produce the HIT cells. Sanyo has highlighted the improved temperature coefficients that give HIT cells an additional advantage over diffused Si cells, without being able to explain what would be the cause for this behavior. We suggest that the temperature dependence of buffer layer properties, not bulk Si wafer properties as is conventionally assumed, will account for this difference.

Phenomena observed in other types of Si solar cells can also be explained by our postulation that the presence of a low-mobility buffer layer is required to obtain high V_{OC}-values. A classical example are MIS solar cells. Conventional explanations suggest that the major benefit comes from a passivation effect of the Schottky barrier interface by the oxide layer. The dilemma with this explanation is that it is well known that one or two mono-layers of a suitable thermal oxide provides near perfect passivation of the silicon surface. On the other hand, in order to improve V_{OC} of an MIS cell (in comparison to V_{OC}-values obtainable in a Schottky barrier device) the oxide has to been grown so thick as to almost impede electric transport through it (sometimes referred to approaching the "tunneling limit"). Another example are the "firing through silicon nitride" cells [6]. The dilemma in understanding the benefits of this process is that while one would expect the benefits to come from surface passivation, cell analyses suggest that bulk passivation may be the most responsible mechanism. We suggest to consider the nitride layer as part of the buffer, and suggest that the physical presence of this layer, rather than a bulk passivation resulting from the application of this layer, will be required in order to enhance V_{OC}.

The latter schemes are similar to the technique of using transparent conductor (TCO) bilayers for contacting $CuInSe_2$- and CdTe-based thin-film solar cells. A TCO bilayer with the resistive surface allows thinning and even elimination of the CdS heterojunction emitter layer without a loss of V_{OC} [7,8]. It is of interest to note that for both $CuInSe_2$- and CdTe-based solar cells the best results for cells with very thin or no CdS layers are achieved when the resistivity of the resistive TCO layers is about 10^4 Ωcm [7,8]; typically these layers are a few tens of nanometers thick. It is also of interest to note that the benefit s of the buffer layer could not be broken down systematically into surface and bulk recombination losses [7]. We postulate that traditional loss analyses of Si solar cells (modeling analyses separating surface and bulk losses) would not hold up to systematic investigations (experimental changes causing changes only in either surface or bulk losses), but are merely two-parameter fits without physical relevance to account for the overall losses.

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Understanding and Optimization of Manufacturable Defect Gettering and Passivation Treatments on String Ribbon Silicon

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Abstract

The effectiveness of manufacturable gettering and passivation technologies is investigated for their ability to improve the quality of a promising Si PV material. The results of this study indicate that a lifetime enhancement of 30 μs is found when a backside screen-printed aluminum layer and a thin film of PECVD SiN are simultaneously annealed in a lamp-heated beltline furnace. The application of the investigated gettering and passivation treatments has resulted in solar cell efficiencies as high as 14.9% (confirmed by SNL) when a spike firing contact anneal profile is implemented to preserve the defect passivation. A *PC1D* device simulation indicates that cell efficiencies approaching 16% can be achieved if these gettering and passivation treatments are employed, the substrate thickness is reduced, and a high quality surface passivation scheme is applied.

Introduction

While large area high efficiency silicon solar cells have been developed using high quality silicon substrates and long process sequences, the remaining challenge for silicon photovoltaics is to reduce the cost of module fabrication while maintaining an efficiency level that can reduce module cost by a factor of 2-4. An obvious approach towards reducing the cost of silicon photovoltaic modules is to reduce the cost of the silicon substrate, which accounts for ~ 45% of the current module cost. The *PC1D* simulation of the effect of bulk lifetime and back surface recombination velocity (BSRV) in Fig. 1 shows that high efficiency solar cells can be fabricated by using relatively low-quality, but thin substrates (~100 μm) if high quality surface passivation treatments are applied. The String Ribbon silicon growth process can reduce the cost of substrate growth because substrates are grown directly without wafering [1]. Another advantage of String Ribbon silicon is that it can be grown to a thickness as low as 5 μm, resulting in further material and cost savings [2]. While the growth of String Ribbon silicon makes it an attractive material for low-cost silicon photovoltaics, the as-grown minority carrier lifetime in the material is low, typically 1-10 μs. The results of the simulation in Fig.1 clearly illustrate that a lifetime of 1-5 μs is not suitable for high efficiency (>15%) solar cells, and there is only a small impact of back surface passivation. However, the simulation indicates that the cell efficiency will increase sharply up to 20 μs. For bulk lifetimes greater than 20 μs, improvements in the BSRV are more important than further bulk lifetime

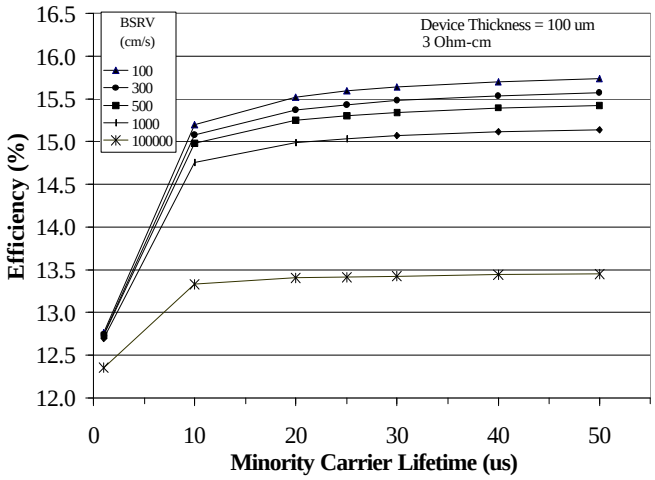

Figure 1 PC1D simulation of the effect of τ and BSRV on efficiency of String Ribbon Si solar cells

improvements in increasing the device efficiency. Therefore, the overall objective of this research is to improve the bulk lifetime in String Ribbon silicon and apply a high quality, manufacturable rear surface passivation treatment to achieve high efficiency solar cells. The immediate goal is to understand and develop gettering and passivation techniques that improve the minority carrier lifetime in the material without significantly raising the cost. In this study, the effectiveness of industrially viable gettering and passivation technologies, namely phosphorus gettering using a liquid phosphorus spin-on dopant, aluminum gettering using screen-printed aluminum paste, and PECVD SiN hydrogenation, will be investigated. The associated heat treatments are all performed in a lamp-heated, continuous beltline furnace. In addition, the effectiveness of sequential and simultaneous combinations of the gettering and passivation treatments were investigated. To monitor the effectiveness of each technology, minority carrier lifetime measurements are made using the recently developed quasi-steady state photoconductance technique (QSSPC) [3].

Experiment

Substrates for this experiment were grown by *Evergreen Solar*, Waltham, MA and doped to 3 Ω-cm, p-type with a thickness of 330 μm. Thick substrates were used in this experiment to avoid breakage of material during the rough cleaning and etching steps for lifetime measurements and cell fabrication. Substrates were cleaned using a modified RCA sequence and acid etched before initial lifetime measurement. Lifetime measurements were made with samples immersed in an I_2/methanol solution that has been shown to effectively passivate silicon surfaces [4]. Lifetime values were recorded at an injection level of 1×10^{15} cm^{-3} to avoid recording erroneously high recombination lifetimes at lower injection level caused by shallow traps [5]. Four lifetime measurements were made on each ~4 in^2 sample and the results averaged to characterize the entire substrate. After the initial lifetime measurement, substrates were again cleaned and subjected to one or a combination of the following gettering or passivation treatments.

Phosphorus Gettering Treatment

A commercially available phosphorus spin-on dopant film was applied to the front surface of selected substrates. Substrates were annealed at a set-point temperature of 925°C for 6 minutes to obtain the target sheet resistance of 45 Ω/sq, which is desirable for screen-printed solar cells. After diffusion, the phos-glass was etched in dilute HF and substrates were again cleaned in the modified RCA clean sequence. Multiple samples were processed and the n^+ layer was removed from one sample before the post-process lifetime measurement.

PECVD SiN Induced Hydrogen Passivation

PECVD SiN was deposited on selected samples using a direct, parallel plate PECVD deposition chamber operating at 13.56 MHz and a temperature of 300°C. Films deposited had a thickness of 860 Å and a refractive index of 1.94. PECVD SiN was deposited on both surfaces of the substrates unless an aluminum layer was to be screen-printed on the back surface of a substrate. In the latter case the substrate was not annealed after deposition, but was subjected to the aluminum gettering treatment. All other substrates were then annealed to drive hydrogen from the film. Anneals were performed for two minutes at set-point temperatures in the range of 650°C – 850°C and the films were removed using a dilute HF solution for subsequent lifetime measurement.

Al Gettering Treatment

A thick film of aluminum was applied to the back surface of selected substrates by screen-printing a commercially available aluminum paste. Substrates were then annealed for two minutes at a set-point temperature of 850°C. The Al layer and underlying Al p^+-doped layer were then removed.

Prior to the post-process lifetime measurement, all substrates were cleaned by the modified RCA clean sequence.

Results and Discussion

Fig. 2 shows that there is some variability in the as-grown lifetime of various samples. Therefore the average of the lifetime measurements on four different regions of each sample, measured before and after the desired treatment, and the relative change are shown in Fig. 2. Phosphorus gettering, PECVD SiN hydrogenation, and aluminum gettering were each moderately effective in improving the bulk lifetime, but were unable to improve the measured lifetime to over 20 μs, previously identified as the targeted lifetime. The combination of phosphorus gettering and PECVD SiN hydrogenation at 850°C improved the lifetime by 7 μs, which is nearly equal to the sum of the enhancement provided by individual phosphorus gettering and hydrogenation treatments. A similar additive effect is observed in the combination of phosphorus and aluminum gettering in which the lifetime improved by over 11 μs. Still the 20 μs threshold was not exceeded by any of the above combinations. In contrast, a noteworthy average lifetime of over 38 μs, an improvement of over 30 μs, was observed when the PECVD SiN hydrogenation treatment and aluminum gettering treatment were combined in one heat treatment at 850°C for 2 minutes. This improvement in lifetime is far greater than the sum of the 850°C hydrogenation and aluminum treatments alone suggesting that there may be a positive synergistic interaction between the hydrogenation from the front surface and the aluminum alloying process simultaneously occurring at the back surface of the substrate at 850°C. Other investigators have noted an interaction between forming gas hydrogenation and backside Al alloying in EFG silicon [6]. A proposed mechanism [7] that describes the interaction of hydrogenation and aluminum gettering involves the enhanced dissociation of molecular hydrogen in the presence of silicon vacancies. A vacancy in a silicon lattice is believed to aid in the dissociation of molecular hydrogen into a fast diffusing hydrogen-vacancy pair and atomic hydrogen. The fast diffusing hydrogen-vacancy pair may be more effective in diffusing to and passivating bulk defects far from the front surface. While the data in Fig. 2 indicate that the PECVD hydrogenation treatment at 850°C without aluminum was only moderately effective, Fig. 3 indicates that some defect passivation in String Ribbon silicon can be obtained *without* aluminum or phosphorus treatments at lower temperatures. However, defect passivation from the anneal of PECVD SiN films without prior aluminum treatments has not been observed in certain materials [8]. A maximum relative improvement of over 100% was found in String Ribbon silicon at 725°C for the 2 minute anneal. At temperatures between 600°C and 725°C, the relative improvement

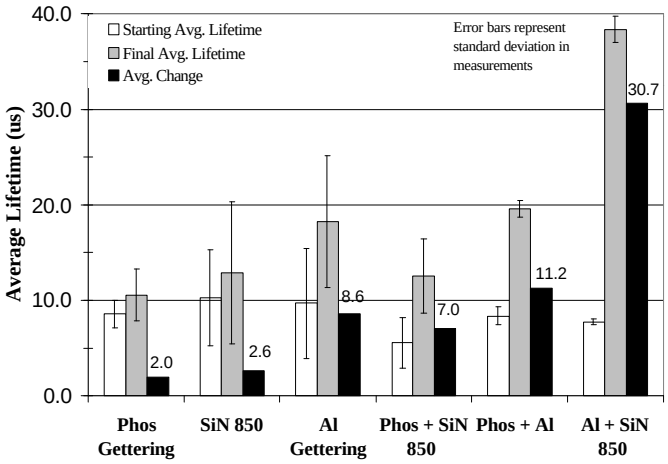

Figure 2 Effectiveness of gettering and passivation treatments

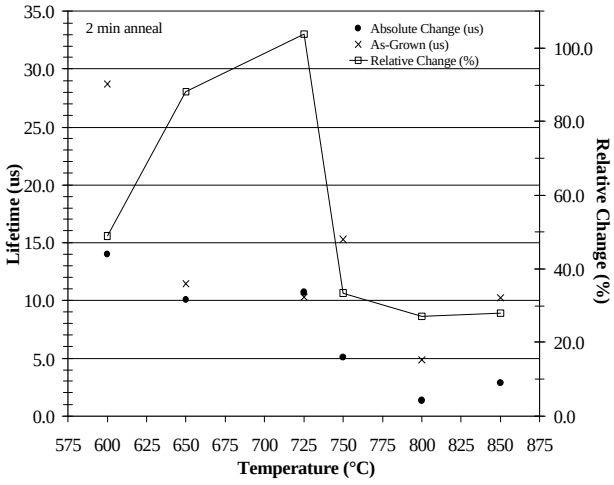

Figure 3 Defect passivation from post-deposition anneal of PECVD SiN

is greater than 50%. For anneal temperatures in the range of 750°C-850°C, the relative improvement drops to near 30%. The dramatic decrease in the effectiveness of hydrogen passivation above 750°C shown in Fig. 3 may be due to the instability of hydrogen at defect sites in the silicon lattice at high temperatures. Hydrogen is known to diffuse out of silicon above 500°C during prolonged anneals [9]. This is in contrast to the situation illustrated in Fig. 2 in which aluminum alloying and hydrogenation are performed simultaneously at 850°C and a significant lifetime enhancement of about 400% is found. One plausible explanation for this result is that the aluminum-silicon alloying process increases the concentration of vacancies and thus the increasing number of H-V pairs. At high temperatures, even if the ability of hydrogen to stick to defect sites decreases, we are able to obtain significant passivation because the passivation may be proportional to the product of a hydrogen-defect site sticking coefficient and the concentration of H-V pairs. To further investigate the thermal stability of the defect gettering and passivation from the phosphorus gettering and simultaneous aluminum and PECVD SiN treatment, we fabricated 4-cm^2, n^+-p-p^+ solar cells on 3 Ω-cm String Ribbon substrates. After the above gettering and hydrogenation treatments, which also form the emitter, BSF, and AR-coating, two screen-printed contact anneal furnace profiles were investigated for defect passivation preservation: i) slow firing - in which the peak temperature in the three-zone beltline furnace was 700°C with a peak zone dwell time of 30 seconds and ii) spike firing performed at *Evergreen Solar* – in which the peak temperature was increased while the dwell time was reduced. Preliminary cell results shown in Table 1 illustrate that that there is a significant improvement in cell V_{oc} and J_{sc} that is attributed to the preservation of defect passivation during spike firing. The long wavelength IQE of devices shown in Fig. 4 also suggest that spike fired cells have a higher effective diffusion length than slow fired cells. This study has resulted in a noteworthy cell efficiency of 14.9% (confirmed by Sandia National Labs) on String Ribbon silicon using industrially viable device fabrication technologies. Our preliminary data indicates that the enhancement in solar cell performance due spike firing is dependent on the effectiveness of the impurity gettering techniques applied or the as-grown quality of the String Ribbon material. For very low quality materials, the improvement in cell performance due to spike firing is not as pronounced.

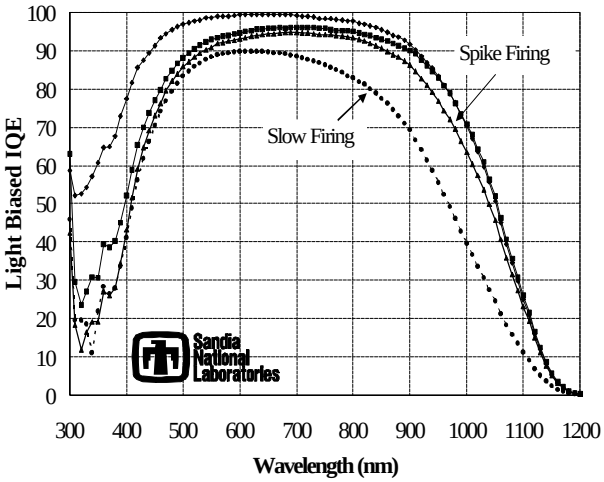

Figure 4 Light-biased IQE of spike and slow fired cells

Process		J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	Eff (%)
Spike Firing	Average	31.2	582	0.736	13.7
	High	32.5	595	0.770	14.9
Slow Firing	Average	30.6	566	0.603	10.5
	High	31.0	565	0.688	12.0

Table 1 Summary of IV characteristics of spike and slow fired solar cells

Conclusions

The results of the QSSPC lifetime measurements indicate that the industrially viable gettering and passivation treatments investigated in this study are effective in improving the bulk quality of String Ribbon silicon substrates. A *PC1D* simulation indicates that the lifetime improvement of 30 μs achieved in this study should be sufficient for the fabrication of low-cost, high efficiency String

Ribbon solar cells. The results of this study indicate that the effect of the sequential combination of phosphorus gettering with aluminum gettering or PECVD SiN hydrogenation is additive, i.e. nearly equal to the sum of the individual phosphorus and aluminum or hydrogenation treatments. However, the effect of simultaneous aluminum alloying and hydrogenation at 850°C appears to be synergistic, i.e. much greater than the sum of the improvements associated with the individual aluminum and hydrogenation treatments at 850°C. Such an interaction between high temperature hydrogenation and aluminum alloying may be due to the formation and high diffusivity of a vacancy-hydrogen pair which can more easily reach defect sites deep in the bulk of the material. In this process, aluminum alloying provides the source of vacancies and PECVD SiN provides the hydrogen. It has also been found that a 2 minute post-deposition anneal of a PECVD SiN film alone can significantly improve the bulk lifetime without prior phosphorus or aluminum treatments if the anneal set-point temperature is below 750°C. This data, along with that reported in the literature [10], suggests that hydrogenation from the post-deposition anneal PECVD SiN films can be preserved at low temperatures, or at high temperatures if the anneal time is reduced. These results were used to optimize the solar cell process sequence in which an 850°C/2 min heat treatment was used for BSF formation, Al gettering, and hydrogenation and was followed by a high temperature, short firing of contacts to preserve that hydrogenation. A spike-firing contact anneal furnace profile was found to be more effective than a slow firing profile in preserving the defect passivation from the simultaneous annealing of Al and PECVD SiN resulting in solar cell efficiencies as high as 14.9 % on String Ribbon silicon. The *PC1D* simulation indicates that the combination of a bulk lifetime of over 30 μs and a *device* rear SRV of less than 300 cm/s can result in cell efficiencies approaching 16% using 100 μm thick String Ribbon silicon.

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Temperature and Doping Level Dependence of Silicon Solar Cell Performance For Exciton Mechanism of Energy Transport

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Since 1997, the PV sales have exceeded 100 MW/yr with > 85% of the production coming from silicon photovoltaics (Si-PV). As the PV demands increase in the new millennium, there will be a host of challenges to Si-PV. The challenges will arise in developing strategies for cost reduction, increased production, higher throughput per manufacturing line, new sources of low-cost Si, and introduction of new manufacturing processes for cell fabrication. At the same time, newer thin-film technologies, based on CdTe and CIS, will come on board posing new competition. With these challenges come new opportunities for the Si-PV-to detach itself from the microelectronics industry, to embark on an aggressive program in thin-film Si solar cells, and to try new approaches to process monitoring.

The 9th Workshop on Crystalline Silicon Solar Cell Materials and Processes will address these issues in a number of sessions. In addition to covering the usual topics of impurity gettering, defects, passivation, and solar cell processing, we have included sessions on poly feedstock, mechanical properties of Si, metallization, and process monitoring.

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