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Silicon-Film™ Photovoltaic Manufacturing Technology

Final Technical Status Report 1 January 1992 - 31 July 1995

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Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project was to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate module. This process starts with the production of continuous sheets of polycrystalline silicon on a supporting substrate using the Silicon-Film™ process.

A number of new solar cell and module products have resulted from this work. The primary product is a 240 cm^2 solar cell referred to as the AP-225. This product has achieved an efficiency of 12.2% (AM1.5G, 1000 W/m^2). A 17.1kW array was constructed for PVUSA using the AP-225 solar cell and was installed in November 1994.

Along with the AP-225, a second, larger, solar cell was developed. The AP-675 solar cell has a device area of 700 cm^2 and has achieved an efficiency of 11.6% (AM1.5G, 1000 W/m^2). Two new module products accompanied the new solar cell products. Table 1 shows the details of the products developed in this program.

Table 1. New Silicon-Film™ Product Developed in This Program

Product	Area *	Power Achieved All Testing Done at NREL
AP-225 Solar Cell	240 cm^2	2.93 W
AP-675 Solar Cell	676.4 cm^2	7.87 W
AP9225 Module (36 AP225 Solar Cells)	0.912 m^2	93.0 W
AP1725 Module (56 AP225 Solar Cells)	1.391 m^2	146.9 W

* Some areas masked to define tested area

The following objectives guided this manufacturing effort:

1. Design, construction, and demonstration of a **Silicon-Film™ wafer machine and process** capable of manufacturing wafers that are 240 cm^2 in size at a rate of 3.0 MW/yr.
2. Development of an advanced **solar cell manufacturing** process that is capable of producing a 3.15 watt, 15.5 cm x 15.5 cm Silicon-Film™ solar cell.
3. Development of an **advanced module design** based on these large area silicon solar cells with an average power of 170 watts for 56 solar cells and 113 watts for 36 solar cells.
4. Investigation of the **larger area solar cell potential** of the developed process represented by 15.5 cm x 45 cm wafers.
5. Design a **large area module (8' by 4')** using the Silicon-Film™ family of products based on feedback from the photovoltaic system and installer industry.

The above objectives lead to the milestones listed in Table 2 (Table 2 represents a subset of the milestones for the entire program).

Table 2. Specific PVMaT Milestones for Phase I through Phase III

	Phase I	Phase II	Phase III
Wafer Machine Production Rate Material Use Efficiency	 400 kW/yr 75%	 1.3 MW/yr 85%	 3.0 MW/yr 90%
Solar Cell Size*	a) 10 cm x 10 cm b) 15 cm x 15 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm d) 1.0 cm^2
Solar Cell Power	a) 1.1 W	b) 2.5 W	b) 3.15 W c) 7.0 W d) 14.0 mW
Module Power	--------	b) 84 W†	b) 98 W† 170 W‡

*Product Designation a) AP-100, b) AP-225, c) AP-675, d)Laboratory Scale Devices
† 36 cell module
‡ 56 cell module

PVMaT Project Guidelines and Tasks

This project incorporates the parallel development of three technologies: (i) a growth technique that produces high quality, polycrystalline silicon sheets on a low cost substrate at high generation rates, (ii) a solar cell fabrication technique that captures the material's potential while qualifying as low cost manufacturing, and (iii) a module fabrication process that efficiently integrates the solar cells into a utility-scale power source. Accordingly, project results are presented in three sections which discuss basic development: (i) The Silicon-Film™ Sheet Fabrication Process, (ii) Solar Cell Fabrication, and (iii) Module Assembly. A fourth section is included that examines very large solar cell fabrication and results: (iv) Larger Area Silicon-Film™ Potential. The 30 individual tasks comprising this project are shown in Table 3 and are identified in the text by number.

Table 3. List of PVMaT-2A Tasks		
Task	**Year**	**Task Title**
1	1	Wafer Performance Benchmarks
2	1	Wafer Process Improvement
3	1	Statistical Process Control
4	1	Solar Cell Efficiency Improvements
5	1	Device Equipment/Process Automation
6	1	Waste Impact/Cost Minimization
7	1	Advanced Module and Panel Design
8	2	Wafer Process Improvement
9	2	Wafer Process Boundary Conditions
10	2	Wafer Machine Building Block Design
11	2	Statistical Process Control
12	2	Solar Cell Efficiency Improvements
13	2	Materials Costs Reduction
14	2	Device Equipment/Process Automation
15	2	Advanced Panel Design
16	2	Module Equipment/Process Automation
17	3	Wafer Process Improvement
18	3	Wafer Machine Building Block Design
19	3	Statistical Process Control
20	3	Solar Cell Fabrication
21	3	Materials Cost Reduction
22	3	Device Equipment/Process Automation
23	3	Module Equipment/Process Automation
24	3	Silicon-Film™ Wafer Production Yield and Capacity
25	3	Optimize Performance of 15 cm x 45 cm Silicon-Film™ Solar Cells
26	3	Cost and Productivity Improvements
27	3	Develop New Panel Products and Processes
28	3	Improve Solar Cell Performance
29	3	Reduce Cost of Critical Baseline Solar Cell Processes
30	3	Reduce Silicon-Film™ Growth Process Manufacturing Costs

Silicon-Film™ Methodology

The Silicon-Film™ Process is a method for fabricating silicon wafers by the production of continuous sheets of thin-film silicon on a low cost substrate which are then cut to size. Because these sheets are produced at the desired thickness, ingot sawing and associated mounting and cleaning steps are eliminated which results in a significant cost reduction. In developing a low cost process, the focus is on limiting the consumption of high quality silicon, reducing sawing steps, and utilizing a high yield continuous manufacturing technology. For the Silicon-Film™ Process, silicon cost is determined by the material quality, silicon thickness, wafer breakage, and

kerf loss during sawing. The continuous wafer generation process produces the volume needed to reduce the per wafer cost of capital equipment and labor.

Key Results

Wafer Machine Performance Benchmarks

The Silicon-Film™ machine and process development was based on the following objectives:

1. Continuous-mode machine for high throughput potential
2. High areal generation rate
3. High quality material at a production capacity of 3.0 MW/yr.
4. Reliable machine components for high yield and continual operation

During this effort, the Silicon-Film™ process progressed from an initial batch-mode version to the final continuous-mode process with a corresponding 1650% increase in areal generation rate. Developments took a stair-like pattern with advances in areal generation rate followed by advances in material quality leading up an increasing production capacity curve. In parallel, cost reduction features and manufacturing attributes were under continual development.

Sheet production capacity for a single machine reached 7.3 MW/yr by the end of the program (see section tilted *Machine Rate*, p.7). Material uniformity and large area potential of this process was demonstrated by the fabrication of a 7.9 watt, 676 cm^2 solar cell.

In the third year, the machine development effort focused on manufacturing capabilities in addition to material quality, specifically, the machine yield, reliability, and material use efficiency were imporved. By performing 14 to 32 hour production runs, we were able to identify and correct component failure modes which only occurred under extended operation. Overall yield reached 73% for 16 hour runs, demonstrating a 62% improvement over a 10 month effort.

Solar Cell Efficiency Achievements

Solar cell fabrication processes were developed along two paths: (i) a baseline production process, and (ii) a laboratory advanced cell process. The objective of the baseline process was to establish a low cost process capable of producing large solar cell lots with an average power of 2.5 watts or better. The objective of the advanced process was to capture the full potential of state-of-the-art material resulting in a 3.15 watt solar cell.

Baseline process efforts focused on reduced cost surface preparation, a gettering diffusion, reduced grid shading, improved contact firing procedures, and increasing performance and throughput of the anti-reflection coating deposition process. The best baseline cell was 2.47 watt (including a 6.5% encapsulation gain) with an area of 240 cm^2. The 2.5 watt average baseline goal will be achieved by fabrication technology improvements in emitter formation (blue response) and AR coating (surface reflection).

Advanced processing efforts focused on improving device performance through enhancement processes such as improved gettering, surface passivation, and hydrogenation (RF plasma and ion-implanted hydrogen). Although significant gains have been achieved using these processes, further gains are attainable through developments in post-growth processing. At the end of the program, the best solar cell fabricated was measured at 2.9 W at NREL. Efforts to improve both as-grown material quality and post-growth processing will continue. We believe progress will be accelerated if post-growth processing technologies are developed on 1 cm^2 substrates and later transferred to a uniform 240 cm^2 substrate.

Module Assembly Achievements

Efforts in module line assembly have focused on measuring the performance of AP-225 solar cells in 36 cell modules, investigating the potential for wider modules (over 100 cm wide), and investigating automation of module assembly steps. Automated tabbing and stringing of front and back contacts was investigated, resulting in identification of the preferred technology and acquisition of an automated stringer/tabber from Spire, Inc. A lay-up table was designed and fabricated in-house at AstroPower for transferring 36 cell matrix strings for lay-up. The new equipment has been used to string Silicon-Film™ solar cells. Once fully implemented it will improve throughput and yield of the tabbing/stringing process.

The best Silicon-Film™ modules verified by NREL were a 93 watt, 36 cell module with a total area of 0.95 m^2, and a 148 watt, 56 cell module with a total area of 1.44 m^2 (details of module performance are contained in the section titled "New Module and Panel Products").

A large panel (approximately 8' x 4') was designed using the Silicon-Film™ family of products (AP-225 and larger solar cells). The panel configuration was based on the results of a survey of industry field installers. The new panel will generate 320 watts and can be handled by two people. A frameless laminate system is used to lower panelization costs.

Larger Area Solar Cell Achievements

In an effort to assess the larger area potential of the Silicon-Film™ process, adjustments were made in the solar cell fabrication process to accept small lots of 15.5 cm x 45 cm wafers. These solar cells have 2.8 times the area of the standard AP-225 solar cell, and they generated 2.7 times more power. NREL measured a 676 cm^2 solar cell at 7.9 W. The small difference in watts per square centimeter (0.4 mW/cm^2) between the two solar cell sizes is believed to be due to the differences in fabrication. Excellent material uniformity was achieved along the length of the Silicon-Film™ sheet, demonstrating the possibility of making larger area Silicon-Film™ products.

The Silicon-Film™ Sheet Process

(Tasks 1, 2, 8-11, 17- 19, 24,30)

Process Description

A setter transports the raw materials through the active layer growth process. The setters are transported in a manner that permits the continuous application of the raw materials and the continuous growth of the active layer; there is only one beginning and one end of the sheet as established by the beginning and the end of the production run. The sheet is cut to the desired length as it exits the machine.

The growth of the active layer is accomplished in a system purged with an inert gas to reduce the effects of oxidation. The linear sheet speed, gaseous ambient, and the axial and transverse thermal profiles of the machine are fundamental parameters that are critical to achieving the desired sheet properties.

Development Goals

Key to the development of the Silicon-Film™ machine and process were clearly defined goals which guided development. These goals were:

1. **High throughput:** material will be grown at a rate capable of at least 3.0 MW/yr production.
2. **High quality:** the active silicon layer will have an as-grown diffusion length of 40 micrometers.
3. **Manufacturability:** low cost features will be built into the process
   - the machine components will be designed for high reliability to attain high product yields under continual operation
   - material use efficiency (MUE) will reach 90%.

There are four key performance factors in Silicon-Film™ machine and process development which are used to quantify developmental progress:

1. material rate (throughput),
2. material quality,
3. material use efficiency, and
4. machine reliability.

The following subsections describe the origin of and the achievements made in each of the above machine performance factors.

Machine Rate
(Tasks 1, 2, 8, 9, 10, 17, 18)

Silicon-Film Machine Rate Calculation

The final machine rate goal for this effort was to demonstrate a sheet generation rate capable of producing 3.0 MW/year. Figure 1 illustrates the geometry for a Silicon-Film™ sheet on the setter. Production rate is the product of the following set of factors: the areal generation rate, M_r, in m^2/hr, the number of operating hours per year, N_o, and the solar cell efficiency, Eff.

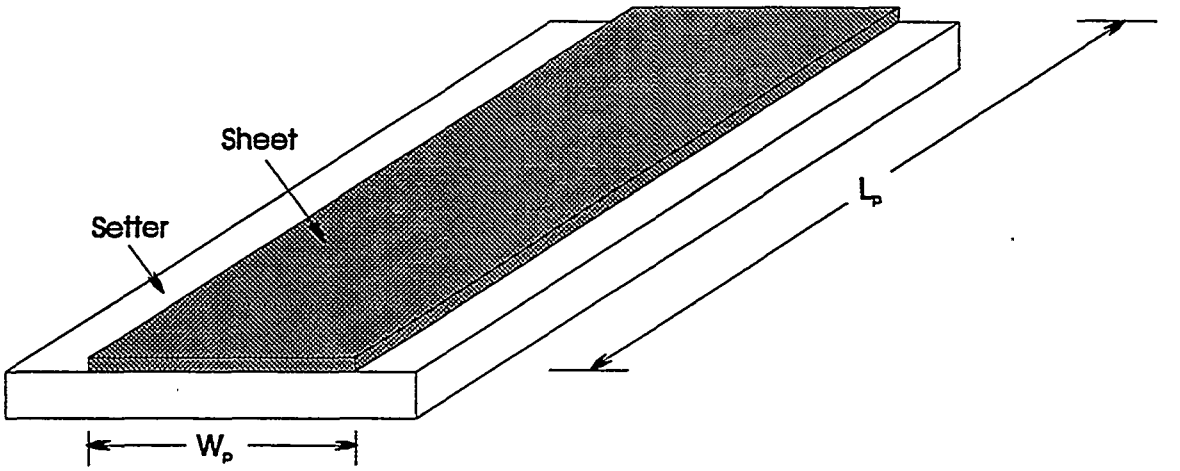


Figure 1. Silicon-Film™ sheet geometry.

The equation for the definition of the production rate is:

$$PR = G_r * N_o * Eff * 10^{-5},$$

where

PR	=	production rate, MW/year
G_r	=	sheet generation rate m^2/hr
N_o	=	number of production hours per year
Eff	=	resultant solar cell efficiency, %.

Silicon-Film Machine Rate Achievements

Our current machine capacity can be calculated using the highest solar cell efficiency measured by NREL (Eff), 8000 production hours per year (N_o ,assuming continuous operation of the machine), and the current baseline sheet generation rate (G_r). Using those inputs, the current machine is capable of a production rate of 4.5 MW/yr. The solar cell efficiency value was based on a NREL verified test using an advanced process on representative wafer material. The sheet generation rate (G_r) is based on finished wafer area generated per hour (as shown in Figure 6).

Figure 2 shows the progress in production capacity during the PVMaT program. During the first year of the program the Silicon-Film™ machine was operated in a batch-mode with a maximum production capacity of 0.48 MW/yr for 100 cm^2 solar cells. The progam goal for the first year was 0.4 MW/yr. During the second year a continuous mode machine was designed, built, and demonstrated with a production capacity of 1.7 MW/yr for 240 cm^2 solar cells (verse a goal of 1.3 MW/yr). After a further year of optimization, a production capacity 4.5 MW/yr for 240 cm^2 solar cells was demonstrated using one prototype machine (verse a goal of 3.0 MW/yr). After fabricating the wafers needed for the PVUSA array, sheet speed was increased. An increase of 60% in sheet speed was implemented with a final capacity of 7.3 MW/yr for one machine. These changes represent a 1500% increase in capacity over the course of the program. Target goals and achieved results are both represented in Figure 2.

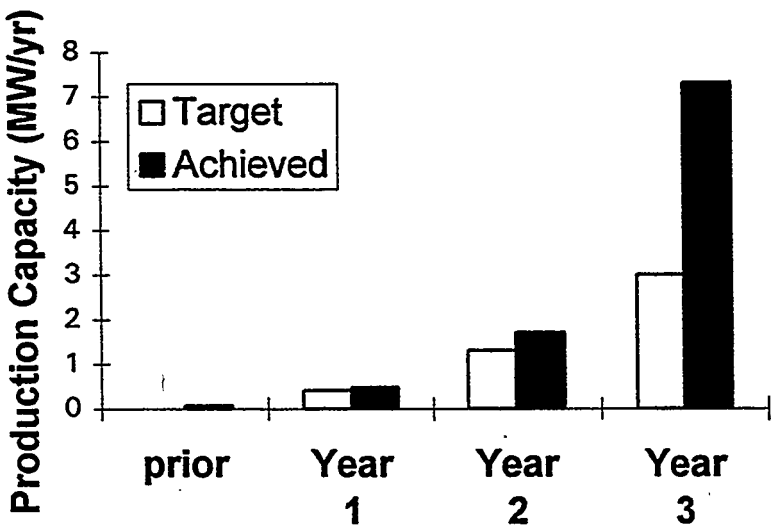


Figure 2. Progress in production capacity throughout the PVMaT program.

Material Quality
(Tasks 1, 2, 7, 8, 9, 10, 17, 18)

Not only is it important that the process produce wafers at high throughput, it is also important that the process generate high quality material. The most important electrical parameter determining the level of quality of the Silicon-Film™ active layer is minority carrier diffusion length. Both the magnitude and spatial uniformity of the minority carrier diffusion length are both important in establishing material quality. This section describes the level of solar cell performance potential of the material (illustrated by modeling), how material was characterized throughout the development effort, the level and uniformity of material quality (measured as diffusion length) achieved to date, and possible causes that limit the performance in the present material.

Expected Performance

Figure 3 summarizes the predicted power from the 15.5 cm x 15.5 cm Silicon-Film™ solar cell as a function of diffusion length and solar cell design. The "baseline process" refers to the production process including screen-printed contacts and automated spray antireflection coatings. The advanced process refers to a process designed to harness the full potential of the material; it incorporates evaporated contacts, some surface passivation, and bulk passivation. Both processes are described in detail in Tables 6 and 7. Modeling of the best advanced process solar cell measured to date revealed potential for improved performance from further surface and bulk passivation, improvement in emitter doping profile, and a reduction in contact resistance. These post-growth process improvements are shown as the "future process" in Figure 3.

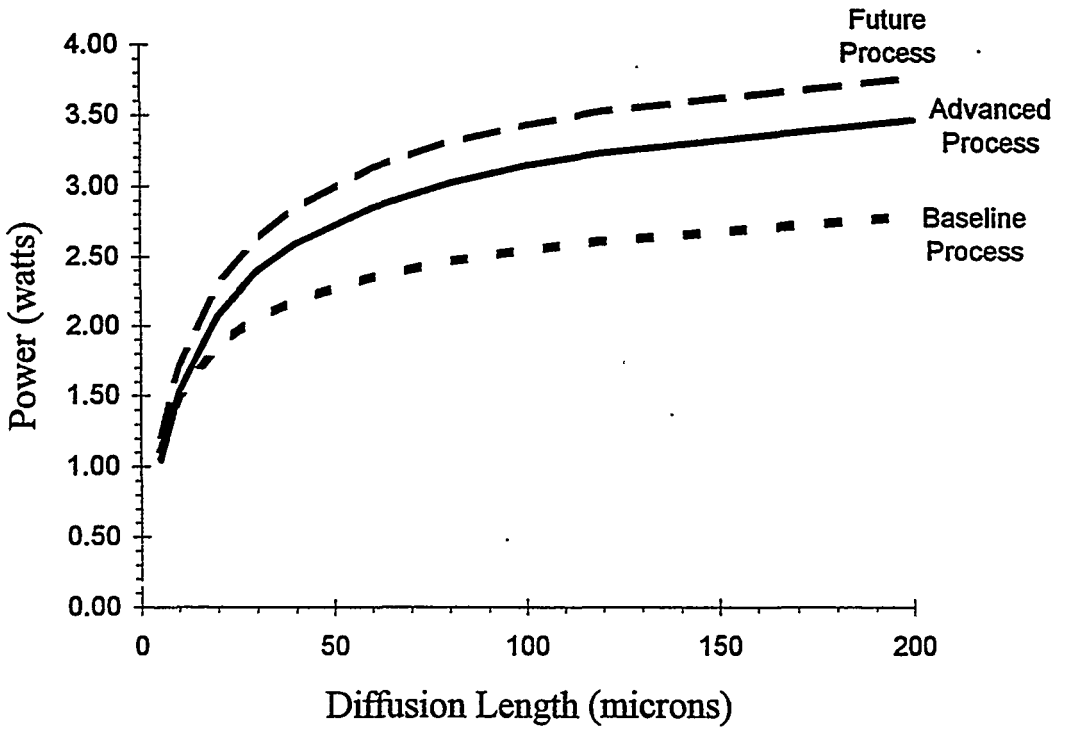


Figure 3. Predicted solar cell power as a function of diffusion length and fabrication process.

Material Quality Characterization

The main characterization tool used during this effort was a small area mesa test device. These devices were fabricated using a process similar to the baseline fabrication sequence used in making large area solar cells. The processing sequence is provided in Table 4. The quick turnaround mesa device (one day processing) was used to: (i) correlate changes in machine parameters with material quality, (ii) evaluate uniformity of material, and (iii) determine which material lots should be processed into large area solar cells.

Table 4. Processing Sequence Used for Fabrication of Mesa Test Devices

Surface preparation - *sandblast* - *NaOH etch* - *$HCl:H_2O$ etch* - *$HF:H_2O$ clean*
Diffusion - *$POCl_3$ source*
HF: H_2O etch
Aluminum paste back contact
Device isolation by dicing
Test

Mesas were fabricated edge to edge across a 15.5 cm width of a Silicon-Film™. No process enhancements such as gettering, front contacts, anti-reflection coating, surface passivation, or hydrogenation were used. Each device had an area of 0.2 cm^2. Testing included J_{sc}, V_{oc}, and L_n measurements (from quantum efficiency measurements). Additional characterization included analysis of quantum efficiency spectra, EBIC (electron beam induced current) imaging, LBIC (laser beam induced current) imaging, dark I-V measurements, and capacitance-voltage measurements for estimations of base carrier concentration. Performance has been correlated between the mesa test device data and the results of AP-225 solar cells fabricated from the same material. The details of that study were reported in the Phase III final report for this program.

Material Uniformity

Comparing mesa performance across the Silicon-Film™ sheet width provides important information on material quality uniformity. Figure 4 illustrates the uniformity of diffusion length across the Silicon-Film™ sheet on samples from Phase II (Run 746) and Phase III (Runs 000 and 001). As shown, the magnitude of diffusion length has improved significantly while further work is required to improve uniformity.

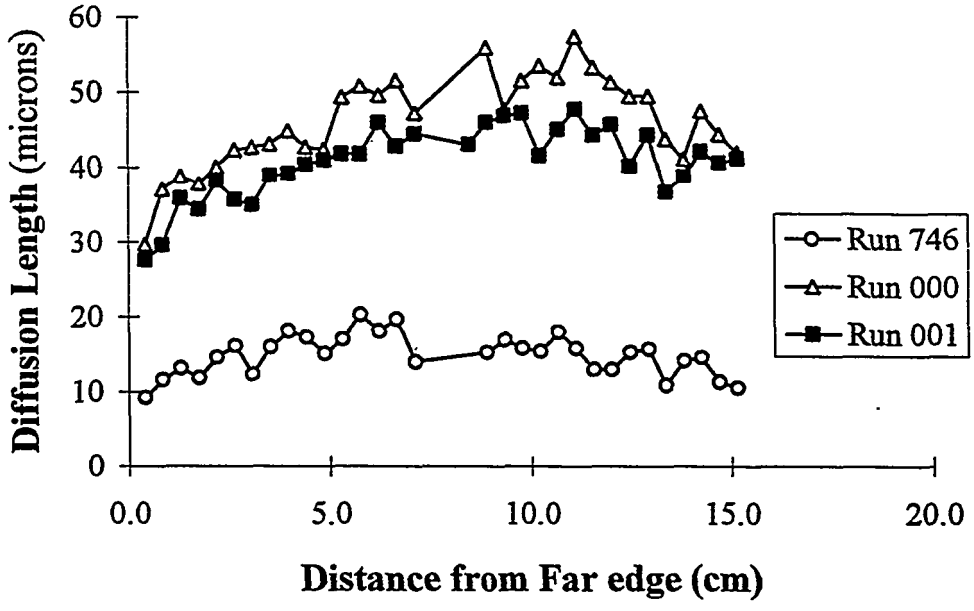


Figure 4. Diffusion length measurements on mesa test devices fabricated across the width of Silicon-Film™ sheets demonstrating level of spatial uniformity.

Possible Causes Limiting Performance

LBIC scans of AP-225 solar cells reveal interesting information about Silicon-Film™ grain boundary effects. Figure 5 shows an LBIC scan provided by Sandia of a 2.84 W AP-225 solar cell [1]. The data were taken at intervals of 20 micrometers with an 820-nm laser focused to a spot diameter of 10 micrometers. The plot was normalized to the position of highest response. The wide dips in the curve represent two gridlines, and each peak represents the response near the center of a particular grain. There are two interesting observations to be made: (i) the decreasing response at the edge of each grain covers a distance much larger than the average effective diffusion length (59 micrometers) of the material, and (ii) the response from grain to grain is moderately uniform. The implication of (i) is that the intergrain diffusion length is higher than the average "effective" measurement of 59 microns (as extracted from QE analysis). An analysis of the data, following Zook [2], leads to the conclusion that the grain boundary recombination velocity is in the range of 400 to 20,000 cm/sec.

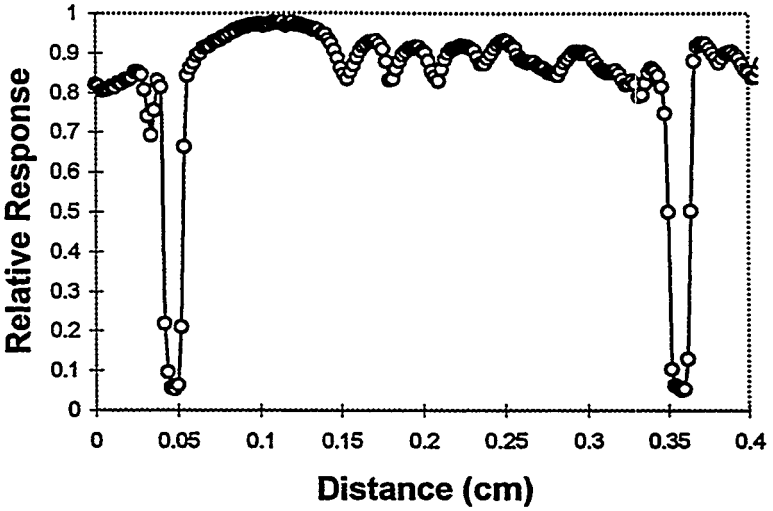


Figure 5. LBIC scan of a 2.84 W AP-225 Silicon-Film™ solar cell.

Correct interpretation of the decreasing response at the edge of each grain may help identify a key area for performance improvement in today's Silicon-Film™ material. It is possible that the decreasing response is due to a particular contaminant that segregates to the grain boundary during growth and diffuses out of the grain boundary during anneal. Future work will be required to determine if this is the correct interpretation followed by identification and elimination of the contaminant.

Material Use Efficiency
(Tasks 1, 2, 7, 8, 9, 10, 17, 18)

Material Use Efficiency Calculation

The material use efficiency indicates the amount of silicon which ends up in the finished wafer compared to the amount of silicon introduced at the beginning of the wafer formation process. The material use efficiency depends on the details of the wafer formation process and can be resolved into the product of three factors: the applicator yield, Y_a, the edge trimming and kerf yield, Y_g, and the wafer visual and mechanical yield, Y_{VM}.

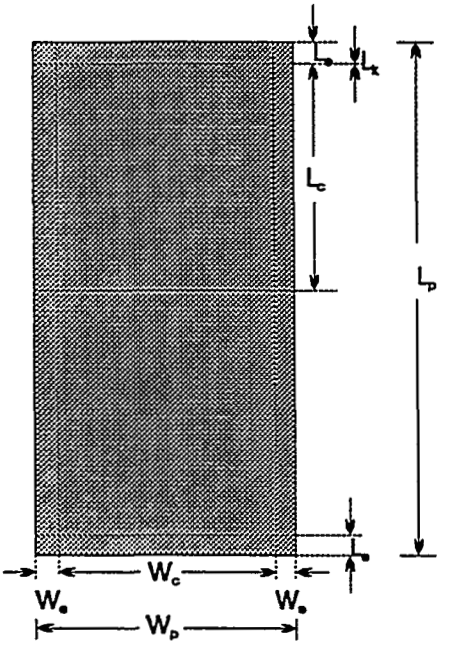
The equation which defines the material use efficiency is

$$MUE = Y_a * Y_g * Y_{VM},$$

where

MUE	=	material use efficiency
Y_a,	=	application yield
Y_g,	=	geometric yield
Y_{VM},	=	visual and mechanical yield.

Figure 6 shows the geometric considerations for determining the finished wafer area and corresponding geometric yield (Y_g).



Lp	=	length of sheet
Wp	=	width of sheet
N	=	number of wafers possible from sheet
Le	=	edge length
We	=	edge width
Lk	=	saw kerf
Lc	=	length of cell
Wc	=	width of cell

$$Yg = \frac{N*Wc*Lc}{Lp*Wp}$$

Figure 6. Definition of dimensions for calculating finished wafer area

Material Use Efficiency Achievements

Conversion from batch-mode to a continuous-mode process led to a significant improvement in material use efficiency. Prior to this development, the areal yield of product was strongly influenced by the growth commencement and termination zones of each sheet. These zones comprised a significant portion of the sheet length. Now that the sheet is continuous, commencement and termination zones occur only once a day and are not a significant percentage of the generated area of sheet.

The applicator yield measures the amount of silicon material applied compared to the amount that is moved into the growth zone. The applicator yield throughout Phase III reached 100%. This improvement from 99% in Phase II is due to smoother setter transport achieved by improving setter joints and guide rail connections.

The geometric yield is based on the number of wafers that could be obtained from the as-grown planks compared to the amount of material applied. Throughout most of Phase III, 16.5 cm wide planks were produced which were cut into 15.5 cm x 15.5 cm solar cells. The geometric yield for a typical 16 hour run is 93%. The visual and mechanical yield accounts for the losses of wafers due to a variety of defects as well as to mechanical breakage. The visual and mechanical yield during our best 16 hour production run was 94% leading to a cumulative material use efficiency of 87%.

To reach the Phase III material use efficiency goal of 90%, we narrowed the grown sheet from 16.5 cm to 16.0 cm. Reducing the edge loss in this manner brought the geometric yield to 96%. In combination with a visual and mechanical yield of 94%, a 96% geometric yield and a 100% applicator yield brought the overall material use efficiency to 90%.

Although a 90% MUE was achieved during Phase III, our 16 and 32 hour production runs were operated at 87% MUE due to a 16.5 cm wide sheet. We found that this sheet width resulted in significantly higher electrical and mechanical yields from solar cell fabrication.

Machine Reliability
(Task 24)

With the Silicon-Film™ machine's basic design established early in Phase III, efforts focused on machine reliability. The goal was to operate the sheet machine for longer periods of time without mechanical failure. Our methodology was to incorporate "next-failure identification" and "incident reports" to our operating procedures. These procedures facilitated identification of component fatigue or failure and eliminated reoccurrence by requiring that affected component designs were modified accordingly.

Production run demonstrations, 16 hours in duration, were completed in February and December of 1994 to assess progress in machine reliability. Progress was evaluated by comparisons of yield, both in wafer and solar cell fabrication. Table 5 provides the yield data for both the baseline 16 hour production run in February and three production demonstrations in December. The following definitions pertain to the abbreviations used in Table 5:

- Y_W is the Silicon-Film™ sheet machine wafer yield and is defined as the number of on-spec wafers divided by the total potential wafers produced from each 16 hour run.
- Y_M is the mechanical yield of the baseline solar cell fabrication process and is defined as finished solar cells divided by wafer starts which were randomly selected.
- Y_E is the electrical yield of the baseline solar cell fabrication process and is defined as the number of on-spec (> 1.70 W) solar cells divided by the total number of finished solar cells.
- Y_O is the overall (total) yield: $Y_W \times Y_M \times Y_E$.
- I_Y is the improvement in overall yield from February to each of the December runs.

Table 5. Improvement-in-Yield Data for Long Production Runs									
Run #	Month (1994)	Potential Capacity (MW/yr)	Run Length (hours)	Y_W %	Wafer Starts	Y_M %	Y_E %	Y_O %	I_Y %
797	Feb.'94	2.1	16	65	400	72	97†	**45**	--
996	Dec.'94	4.4	16	90	500	74	99+	**66**	***47***
000	Dec.'94	4.4	16	93	600	78	100	**73**	***62***
001	Dec.'94	4.4	16	91	500	80	99+	**73**	***62***
087	May '95	4.4	24	84					

†February electrical yield was based on the number of solar cells $\geq$ 1.35 W. December electrical yield was based on the number of solar cells $\geq$ 1.70 W, a 26% improvement in power.

In Table 5, potential capacity (defined in the section entitled "Silicon-Film Machine Rate Calculation" on page 7) infers sheet generation rate at 100% yield utilizing the best performing solar cell cut from representative material and measured by NREL. The increase in potential capacity from February to December is based on a demonstrated 14% increase in solar cell output power and a demonstrated 85% increase in sheet generation rate. The yield data for the 24 hour run (087) was not compiled.

Solar Cell Fabrication Processes

(Tasks 4-6,12-14, 20-22, 28, 29)

Solar cell fabrication processes have been developed along two parallel paths: (i) a baseline process, and (ii) an advanced process. The objective of baseline process development was to establish a low cost process capable of producing solar cells with a lot average of 2.5 watts or better. The objective of the advanced process effort was to capture the full potential of the material with an end-of-effort goal of achieving a 3.15 watt solar cell. Advanced processes that improved solar cell performance and were manufacturable at a reasonable cost became part of the baseline process; a process that provides a 5% increase in power can impact module cost by no more than 5%.

The majority of work in new process development has focused on the optimization of high temperature gettering and diffusion steps. This work has led to the 1.0 cm^2 results detailed below and a path to a 3.35W AP225 solar cell. In addition to the optimization work, two new processes were investigated to improve performance of Silicon-Film™ devices. The first was a new anti-reflection coating based on textured dielectric coatings as identified by James Gee of Sandia. Films were deposited at Harvard University (Department of Chemistry) and evaluated at AstroPower. The second new process investigates the isolation of Silicon-Film™ solar cells with a plasma etching process. This process has been in use on single crystal cells, but just recently extended to Silicon-Film™ devices. Results on both processes are summarized below.

Current Baseline Process

At the end of the program, the baseline solar cell fabrication process consisted of the steps listed in Table 6. At the end of program, this process was capable of handling 3,000 wafers per day. Areas requiring improvements for higher throughput and device performance were identified and are discussed below.

It was found that a double diffusion process led to better overall performance than a standard single step diffusion. The double diffusion process involves a standard diffusion step (40 ohm/square), followed by etchback (in NaOH) of the diffused surfaces, followed by a second standard diffusion step (40 ohm/square). Studies demonstrated an improvement in cell power of 11.9% with the 2 step process. That study was detailed in the Phase III final report.

Table 6. Baseline Solar Cell Fabrication
Process Steps

1) Surface Preparation (Sandblast + NaOH)
2) Gettering Diffusion
3) Etch Gettered Junction
4) Standard Shallow Junction Diffusion
5) Edge Isolation
6) PSG Removal
7) Print/Dry/Fire Back Ag (98%)/ Al (2%) busbars Aluminum paste over back
8) Print/Dry/Fire Front Silver ink grid
9) Spray AR Coating
10) Test

Hydrogenation

Hydrogenation processes were found to result in significant gains in the diffusion length of as-grown Silicon-Film™ material. Early in this effort, Kaufman hydrogenation was employed, but resulted in irreparable surface damage and significant degradation of blue response [3]. An rf-plasma hydrogenation process is presently used in the advanced process sequence on the front surface of the device prior to the emitter etch-back step. Exposure time and rf power have been reduced to maximize diffusion length gains, with only minimum surface damage as measured by the blue response of the device. Some surface passivation is realized by an emitter etch-back step followed by a CVD-deposited SiO_2 passivation layer. A similar process is included in the advanced processing sequence.

Brief RF plasma hydrogenation has been found to reduce the standard deviation of the fill factor on large production lots. Results indicate that poor control of the furnace used to fire the front contacts may be causing variation in contact resistance. As process control and material quality of the Silicon-Film™ sheet has increased, the impact of hydrogenation has diminished. Hydrogenation is still being used as a process control monitor.

Forming Gas Anneal

A forming gas anneal process has demonstrated a significant gain in red response. Diffusion length gains of 72% were demonstrated in Silicon-Film™ material processed at Georgia Institute of Technology when forming gas anneal was isolated from the rest of the process.

Anti-Reflection Coating

A machine to automatically spray a TiO_2 anti-reflection coating was built during Phase III. Process parameters were optimized offering uniform AR coating over the 15.5 cm x 15.5 cm solar cells at a throughput of 490 solar cells per hour. At these parameters, the typical power gain is 37% which is similar to our PECVD anti-reflection coating process. The throughput of the production line PECVD Si_3N_4 anti-reflection coating process is significantly lower offering only 210 cells per hour.

Encapsulation gain was evaluated for the spray AR coating versus the previous standard Si_3N_4 deposited via PECVD. A comparison was performed of reflection spectra for the visible wavelength range of 400 to 700 nm for typical cells with spray TiO_2 AR coating versus cells with Si_3N_4 coating deposited via PECVD. Short circuit current measurements found that an encapsulation gain of 2 to 6% is typical from the spray AR coating, whereas the effect of the Si_3N_4 coating is less reproducible and has a maximum potential encapsulation gain of less than 2%. Figure 7 shows a comparison of post-encapsulation reflection for the two processes. Although the PECVD Si_3N_4 process is less reflective in the blue, the spray AR process has lower reflection over the entire spectrum, resulting in the lower spectrally weighted reflection.

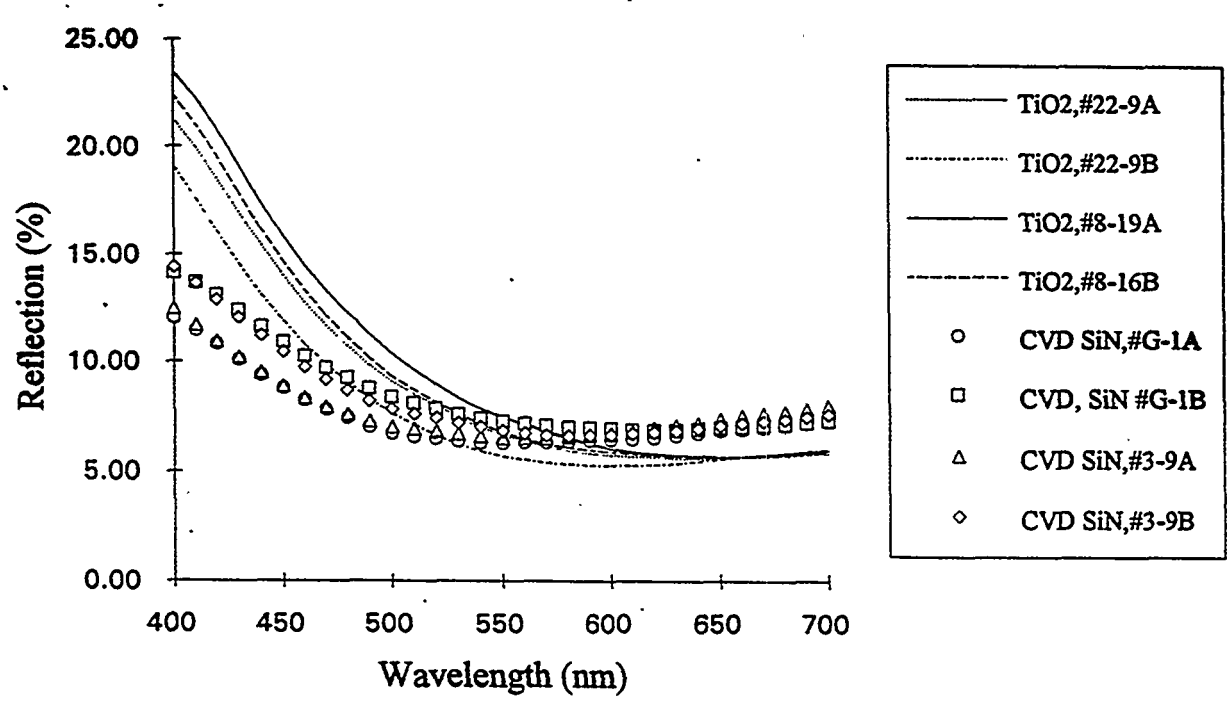


Figure 7. Comparison of post-encapsulation reflection of typical cells with TiO_2 spray AR coating and typical cells with Si_3N_4 PECVD AR coating

In conclusion, we consider the spray AR coating process to have successfully replaced the PECVD Si_3N_4 AR coating process, due to the significantly higher throughput of the process and the consistent power and encapsulation gains of the coating.

Implementation of Plasma Etching for Isolation of Silicon-Film

AstroPower isolates single crystal solar cells in a high throughput plasma etching process. After diffusion, wafers are stacked so that only the edges are exposed. The exposed edges are then plasma etched. The flatness of the wafers is critical, as excessive space between wafers will allow etching to take place on the wafer surface and potentially shunt the device.

Historically, Silicon-Film™ wafers have not been flat enough to utilize this process. Recent advancements in sheet growth have greatly improved flatness. A 10 wafer lot of AP225 cells was plasma etched in a production fashion. The lot was then re-isolated using an edge sanding process. The measured fill factors of the devices after the edge sanding differed by less than 1% from the prior test (plasma etching alone). This potential improvement in processing Silicon-Film™ wafers will significantly reduce the cost of processing AP225 solar cells and indicates the level to which the material has advanced.

Baseline Solar Cell Performance

The best performance of a single cell to date using baseline processing is 2.47 watts. The best median performance of a lot of 466 solar cells was 2.33 watts. These solar cell performance parameters assume a 6.5 % encapsulation gain. We expect that the median baseline solar cell performance will improve to 2.5 watts once we achieve improvements in our emitter doping profile, and surface reflection. Further improvements over 2.5 watt cell medians are expected as as-grown material quality improves and average diffusion lengths go beyond 50 micrometers.

Advanced Processes
(Tasks 4, 12, 20)

The advanced solar cell fabrication process consisted of the steps listed in Table 7. The advanced process incorporated a combination of performance enhancement steps designed to capture the full potential of the material. These enhancement steps included specialized gettering, forming gas anneal, hydrogenation, and evaporated. Future work will focus on tailoring these advanced processes to realize the performance gains on a production scale.

The CP etch surface preparation involves etching the cells in a mixture of HNO_3:HF:CH_3COOH in a ratio of 15:2:5. This provides the smooth surface required for evaporated contact photolithography. The second diffusion step is patterned after the work of Basore [4], and is referred to as the "Sandia-like" diffusion, the effect of which is described below. The purpose of the 0.5 micrometer thick aluminum layer, step 2, is primarily for aluminum gettering during the high temperature diffusion step.

Table 7. Advanced Cell Fabrication Process Steps

1) Surface preparation (CP etch)
2) Aluminum deposition (0.5 μm)
3) Gettering diffusion
4) Strip junction (CP etch)
5) "Sandia-like" diffusion
6) Forming gas anneal
7) RF hydrogenation
8) Emitter etch back
9) CVD SiO_2 passivation layer
10) Evaporated Contacts
11) CVD SiO_2 and Si_3N_4 AR Coating
12) Test

Gettering

Optimized gettering and bulk defect passivation are known to improve the efficiency of polycrystalline silicon solar cells. The two most widely used and effective gettering steps for polycrystalline silicon material are phosphorous and aluminum gettering. Both have been evaluated on Silicon-Film™ material.

The diffusion length of as-grown Silicon-Film™ is typically in the range of 2 5 to 45 micrometers. Phosphorus gettering was investigated for its potential to improve this diffusion length. Experiments were performed to determine the optimum process parameters of time, temperature, and $POCl_3/O_2$ ratio. A 1.0 cm^2 laboratory-scale solar cell process was employed to produce devices for quick feedback. Current-voltage characteristics and spectral response were measured on a total of nine samples for each set of experimental conditions. The minority carrier diffusion length was determined by analyzing the spectral response curve in the range of 750 to 950 nm.

Initially, the temperature was set at 875°C, and the time was set at two hours [5]. Various continuous $POCl_3/O_2$ flow mixtures were then investigated to determine the optimum as determined by maximum improvement in diffusion length. Once the optimal $POCl_3/O_2$ flow mixture was determined at 875°C, it was used to investigate the temperature range from 850 to 900°C. These data indicate that the optimum temperature for $POCl_3/O_2$ gettering is 890°C.

Spectral response data comparing a non-gettering, and a two and an eight hour gettering sequence at the optimized gas flow mixtures and temperature are shown in Figure 8. These data

were used to determine a minority carrier diffusion length of 70 micrometers for the two hour gettering sequence and 160 micrometers for the eight hour gettering sequence.

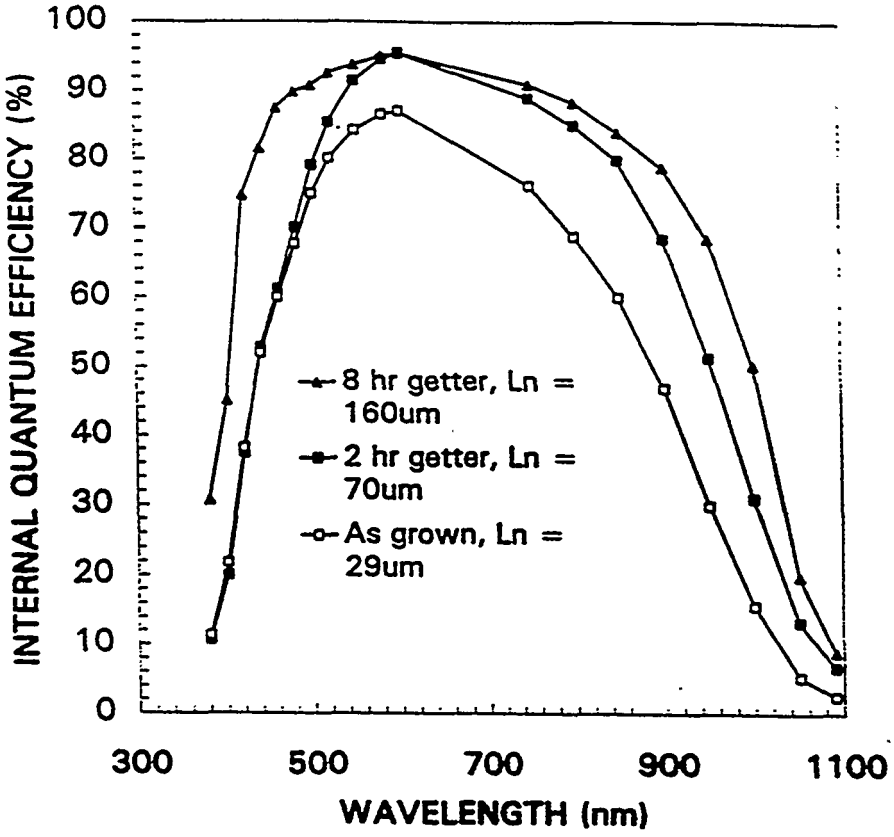


Figure 8. Spectral response curves for as-grown and gettered Silicon-Film™ material.

Enhancements to the Anti-Reflection Process

Textured dielectric coatings have been identified by James Gee of Sandia as a potentially useful method of reducing reflection in a non-textured solar cell. This is of importance to the Silicon-Film™ effort as effective texture etch is difficult to achieve in polycrystalline silicon material. The technology was developed by Roy Gordon of Harvard University, and has been investigated for use in other thin-film solar cell materials, such as amorphous silicon.

High textured coatings of ZnO were investigated on AstroPower's AP-225 solar cells as well as single crystal cells. The coatings were deposited by APCVD on top of TiO_2 layers. The results (Figure 9), indicate reflection is lowered by the presence of the ZnO, especially in the blue and red ends of the spectrum. All data in Figure 9 are for cells with a glass coverslide and a liquid coating emulating the optical properties of EVA.

Coated cells were then laminated into modules to test the effects of the ZnO on I-V characteristics. These data indicated that the ZnO coated cells did not have significantly higher short circuit current than cells with only a standard AR coating. A plausible explanation is that the current gains due to reduced reflection is offset by increased absorption in the ZnO.

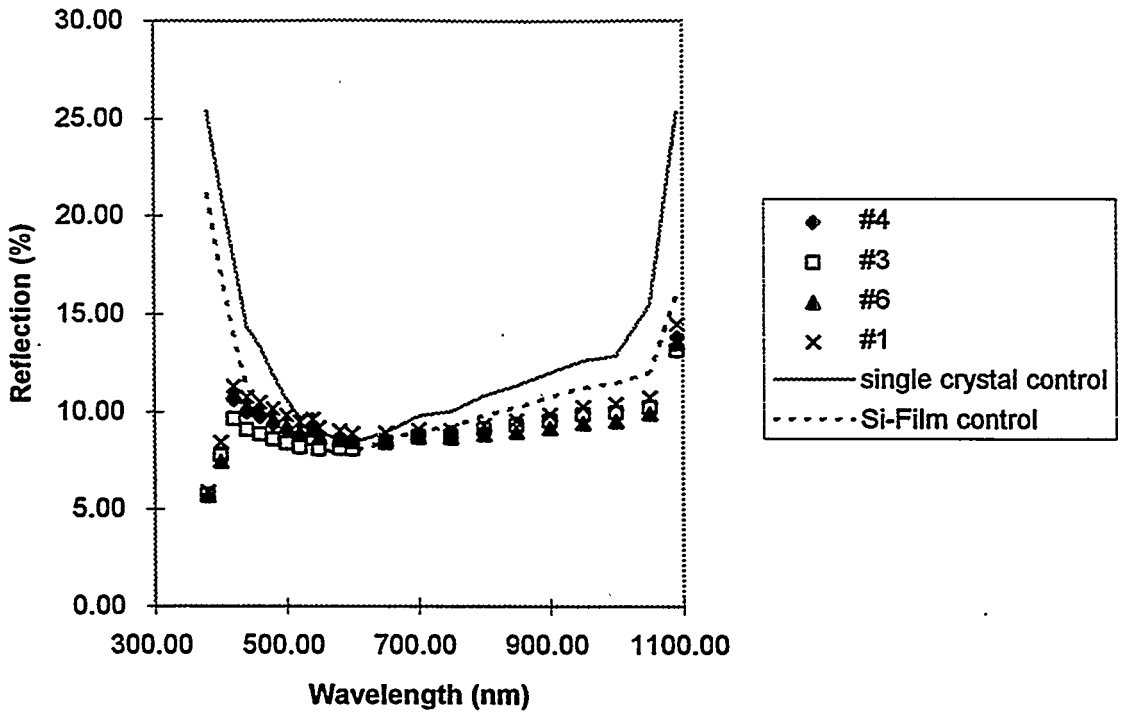


Figure 9. Reflection of Silicon-Film™ solar cells with and without ZnO coatings. The lines indicate solar cells with only TiO_2 coatings, the data points indicate devices with ZnO over TiO_2 coatings.

Emitter Etch-Back

The "simplified diffusion" process developed by Sandia [4] was adapted for the Silicon-Film™ material. The intent of the process was to affect gains from bulk passivation through aluminum gettering, and surface passivation through the generation of a native oxide. However, due to the need for further bulk passivation via hydrogenation, the benefit of the native oxide was lost. In this adaptation, an emitter etch back step which removes some of the front surface damage from rf-plasma hydrogenation was developed. Diffusion profiles, using spreading resistance analysis obtained from Solecon Labs, were used to optimize the junction depth at 0.6 micrometers thus making it plausible to control the emitter etch-back step. This step also assists in reducing the surface concentration and allows for tailoring of the sheet resistance of the emitter.

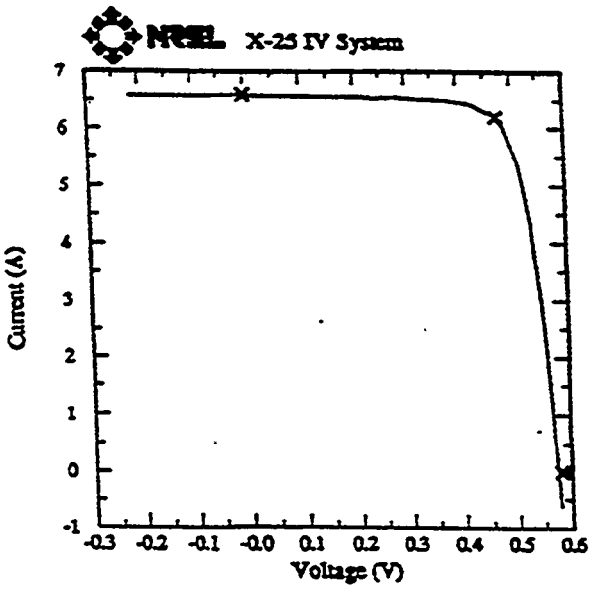
Front Contact Grid Pattern

As post-growth processing and as-grown material quality improved, the high current density of the 240 cm^2 device dictated a re-design of the front contact grid pattern. Fill factor losses indicated a need for reduced series resistance and better collection. The number of gridlines was

increased from 50 to 65, the tabbing thickness was increased from 0.127 mm to 0.203 mm, and the emitter sheet resistance was increased from 50 to 75 ohms per square. As a result, fill factors increased from 0.73 to 0.78, but grid shading increased from 3.4 % to 4.1 %. The overall gain in power from these changes was 6.15%.

Advanced Process Solar Cell Performance

The advanced processes discussed above were combined into a working process sequence using state-of-the-art Silicon-Film™ sheet material. The result was a 2.93 W, 240 cm^2 as measured by NREL. The current-voltage characteristic for this solar cell is provided in Figure 10. Analysis of a similar cell by Sandia indicated that the primary energy losses in the cell were due to front-surface reflectance (3%), non-ideal recombination (3%) and series resistance (5%). These losses add up to 11% loss in power. An 11% improvement in power for the 2.93 W cell would yield a 3.25 W device.



V_{oc} = 0.5819 V	V_{max} = 0.4723 V
I_{sc} = 6.581 A	I_{max} = 6.203 A
J_{sc} = 27.39 mA/cm^2	P_{max} = 2929.3 mW
Fill Factor = 76.49%	Efficiency = 12.2%

Figure 10. Current-voltage curve measured at NREL for a 2.93 W Silicon-Film™ solar cell.

Our plans to improve the advanced process Silicon-Film™ solar cell include improvements in:

- **diffusion length** of the material through higher quality as-grown material and improved gettering,
- **fill factor** through reduced series resistance and increased shunt resistance,
- **blue response** through improved passivation of the front surface.

These performance enhancements were used to generate the "future process" curve showing solar cell power versus diffusion length shown in Figure 3.

Progress in Solar Cell Performance
(Tasks 4, 12, 20)

Figure 11 illustrates the progress made in AP-225 solar cell performance during the course of the PVMaT program. Deliverable goals and achieved results are both represented.

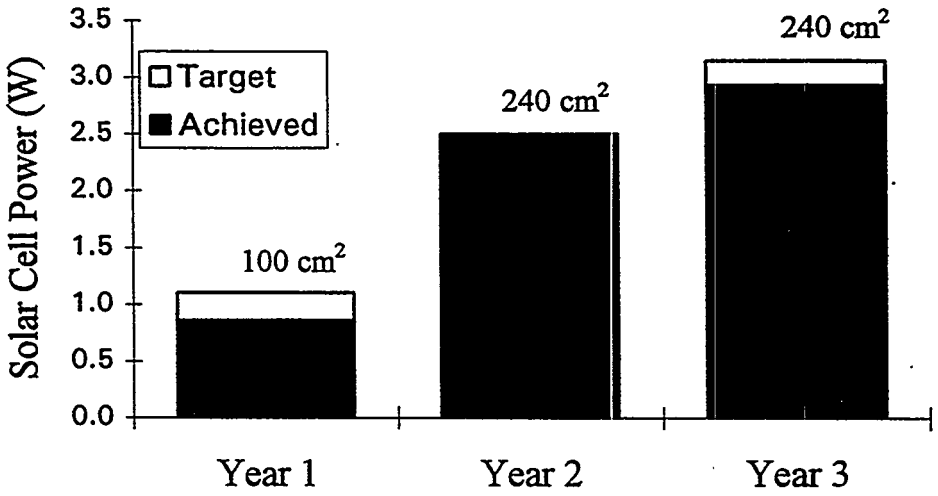


Figure 11. Progress in solar cell performance throughout the PVMaT program.

Cost Reduction
(Tasks 6, 13, 21, and 29)

The purpose of these tasks were to reduce the costs associated with the surface preparation of the Silicon-Film™ wafer for diffusion. Surface preparation includes the removal of the as-grown surface followed by wet chemistry to remove surface damage and provide a smooth surface for contact printing. Three areas of investigation were identified for reductions in cost:

I. *improvements in abrasive removal of the as-grown surface*

II. *improvements in wet chemistry including:*
- A. investigation of alternative chemistries,
- B. utilization of less expensive materials,
- C. reduction in the quantity of materials required,
- D. improvements in material utilization.

III. *reduction in the labor-related costs by automating process steps.*

Improvements in Abrasive Removal of the As-Grown Surface

The present abrasive technique removes the as-grown surface from the Silicon-Film™ sheet by dry sandblasting. However, the resulting damage to the underlying silicon is substantial requiring chemical removal of the damaged silicon. Our approach was to investigate several abrasive surface treatments with the goal of removing the surface while minimizing damage to the underlying silicon. The following abrasive surface treatments were investigated:

I. angle of impact, velocity of particle in sandblasting,
II. abrasive filament brushing,
III. high pressure water jetting,
IV. planar abrading with abrasive coated open weave fabric,
V. abrasives carried in a liquid/gas stream

Of these five areas investigated, abrasives in a liquid/gas stream proved to be the most promising alternative to our present dry sandblasting technique for pre-wet chemistry surface preparation. This method provided the most uniform surface quality with minimal surface damage. Although our investigations are not yet complete, we expect that this technique will have operating costs that are less than or equal to our present sandblasting technique but will reduce the surface etching required in our wet chemistry process. Further work is planned in assessing cost, depth of surface damage, and subsequent wet-chemical etching requirements.

Improvements in Wet Chemistry

Investigation of Alternative Chemistries and Utilization of Less Expensive Materials

During the PVMaT program, a significant reduction was achieved in direct material costs associated with the surface preparation of Silicon-Film™ AP-225 wafers before diffusion. This reduction in direct material costs, illustrated in Figure 12, was achieved in two phases. First, an alternative wet chemistry process was used beginning in Phase II. Second, in Phase III, the cost of the alternative process was reduced by replacing some of the high purity, high cost materials with lower purity, lower cost alternatives. These decisions were supported by experiments (involving several hundred thousand single crystal wafers) designed to test the effect of the chemistry changes on device performance.

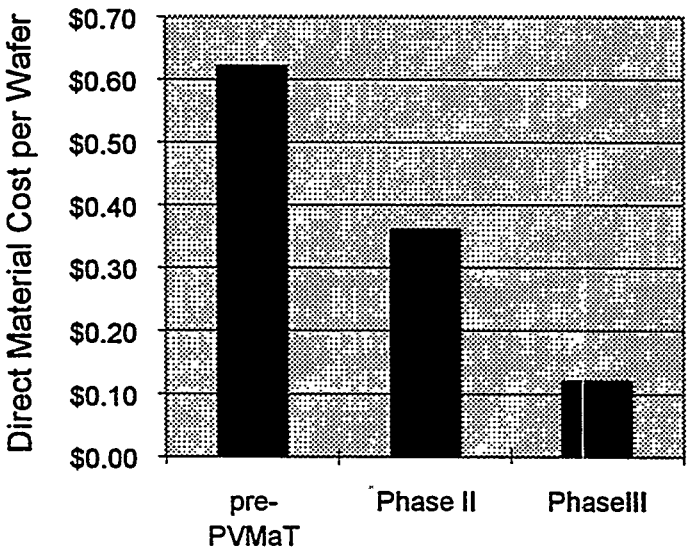


Figure 12. Reduction in direct material costs associated with surface preparation of the AP-225.

Reduction of Materials Required and Improvements in Material Utilization

Several areas have been investigated in improving material utilization. For instance, we have investigated the sale of the spent sodium hydroxide used in our wet chemistry process. A bulk chemical supplier is analyzing our effluent for resale to bulk acid customers for neutralization purposes. We have also initiated investigations in concentration control and by-product removal associated with a critical etchant bath in our wet chemistry process. This would greatly improve material utilization and would reduce associated direct material costs.

Shorter etch times and lower concentrations of chemical etchants were investigated to reduce the quantity of required chemicals. However, the resulting wafer surface texture was not acceptable. As the abrasive surface treatment is optimized and resulting surface damage is minimized, shorter

etch times may again be considered. Hence, we will continue our investigation of shorter etch times in conjunction with the new abrasive surface treatment.

Automation

In an effort to reduce labor costs, reduce potential health and safety hazards, and improve yields and throughput, several areas of surface preparation of the AP-225 have been targeted for automation. These areas include neutralization of chemical etchants, automation of cassette transfer, and application of chemicals by spraying instead of batch etchant baths. Automation in these areas requires large capital investment, considerable design efforts to ensure fail-safe operation, and changes in operating procedure. Initial investigations of each area have been completed and recommendations for further action/development have been made. We expect to continue with automation in these areas.

A fully automated spray anti-reflection coating machine was designed, fabricated, and operated in the processing of PVMaT deliverables. This automated machine demonstrates a throughput of 490 AP-225 solar cells per hour, yielding a higher throughput, a similar solar cell power gain, and an improved encapsulation gain over our PECVD Si_3N_4 process at a significantly lower capital cost.

Cost Reduction in Contact Metallization Processes

Efforts were made to reduce the amount of metal paste used to form the screen-printed back contact. Screen characteristics were investigated to achieve a thinner emulsion. Dominant variables determining paste thickness were found to be ink temperature (viscosity), solar cell thickness, printer parameters, and screen age. Since the optimum thickness for the AP-225 is still under investigation, optimization of metal paste consumption will be postponed until AP-225 product development is complete.

Conclusions

During the three year PVMaT program, the AP-225 surface preparation processes has undergone a dramatic evolution resulting in an 80% reduction in cost per wafer associated with direct materials used in surface preparation for diffusion. Process changes focused on alternative chemistries and processes leading to reduced costs with no reduction in device performance. Numerous areas for further cost reduction were investigated and several were identified for further development. These include baseline changes which will result in an increase in throughput exceeding 200% and a resulting 750% reduction in wet chemistry labor costs (in dollars per wafer). Additional work is planned in automated neutralization of chemical etchants, an alternative abrasive cleaning technique resulting in less surface damage, automated transfer of cassettes in the batch process, and an in-line wet chemistry spray application method to eventually replace the batch process.

New Module and Panel Products

(Tasks 7, 15, 16, 23, 27)

Module Fabrication

During this program, module fabrication efforts focused on: (i) evaluating performance of the AP-225 solar cell within a module, (ii) automating critical areas of the module line process, (iii) investigating the feasibility of wider (than 95 cm) module products, (iv) and the development of new large area panels based on Silicon-Film™ solar cells. Different sizes of AP-225 Silicon-Film™ modules were fabricated: (i) a 36 solar cell (6 cell by 6 cell configuration with a total area of 0.942 m^2) and (ii) a 56 cell (8 cell by 7 cell configuration with a total area of 1.438 m^2). Designs were developed for a large area panel, and a prototype was fabricated.

In 1994, 10% of the total modules fabricated by the AstroPower module fabrication line were Silicon-Film™ modules; 12 of these were delivered to NREL under this PVMaT contract and 312 were delivered to the PVUSA site in Davis, California.

36 Solar Cell Module Fabrication

Eleven modules consisting of 36 AP-225 solar cells each were delivered to NREL during this program. Test data from the best of these are shown in Table 8. The process column refers to the processing sequence used to fabricate the solar cells making up the modules. Progress was also made in the automation of two different steps in the 36 cell module fabrication process: (i) tabbing and stringing, and (ii) transfer to lay-up. These two areas are discussed in detail in the subsections that follow.

Table 8. NREL Outdoor Test Data for 36 Cell Silicon-Film™ Modules

ID #	Process	Temp (°C)	Aperture Area (m^2)	Voc† (V)	Isc† (A)	FF† (%)	Pmax‡ (W)	Aper. η (%)
D-23	advanced	22.2	0.912	20.8	5.9	71.8	93.0	10.2
D-29a	baseline	23.5	0.908	19.4	5.2	68.3	73.6	8.1

†as measured

‡ corrected for irradiance to 1000 W/m^2, not corrected for temperature

The estimated U95 uncertainty of the NREL outdoor measurements is ±5%. Temperature was measured at the back of the module during testing; no correction for temperature was made. Total irradiance during these measurements was less than 1000 W/m^2. For comparison purposes the maximum power entries in Table 8 are corrected to 1000 W/m^2. Corrections for spectral mismatch error and second order irradiance error were not made.

Automation of Tabbing and Stringing

Three technologies were considered in the automation investigation for tabbing and stringing. These alternatives were ultrasonic welding, wire bonding, and high intensity light soldering. After evaluating these techniques and associated equipment, high intensity light soldering was chosen for future use. High intensity light soldering offered the following benefits over the other techniques:

- higher throughput (15 seconds per cell)
- solar cell size flexibility
- fluxless ribbon (environmental benefit: elimination of organic flux cleaners)
- front and back of cell can be tabbed/strung simultaneously

A SPI-ASSEMBLER that implemented this new technology was received from Spire Corporation and installed at AstroPower. The tool is designed to tab and string both AP225 solar cells and single crystal cells. Figure 13 shows the assembler stringing Silicon-Film™ cells. This automated process replaces a very labor intensive step in the manufacture of Silicon-Film™ modules. Spire has continued to be involved as increases in Silicon-Film™ solar cell sizes will require new developments in equipment.

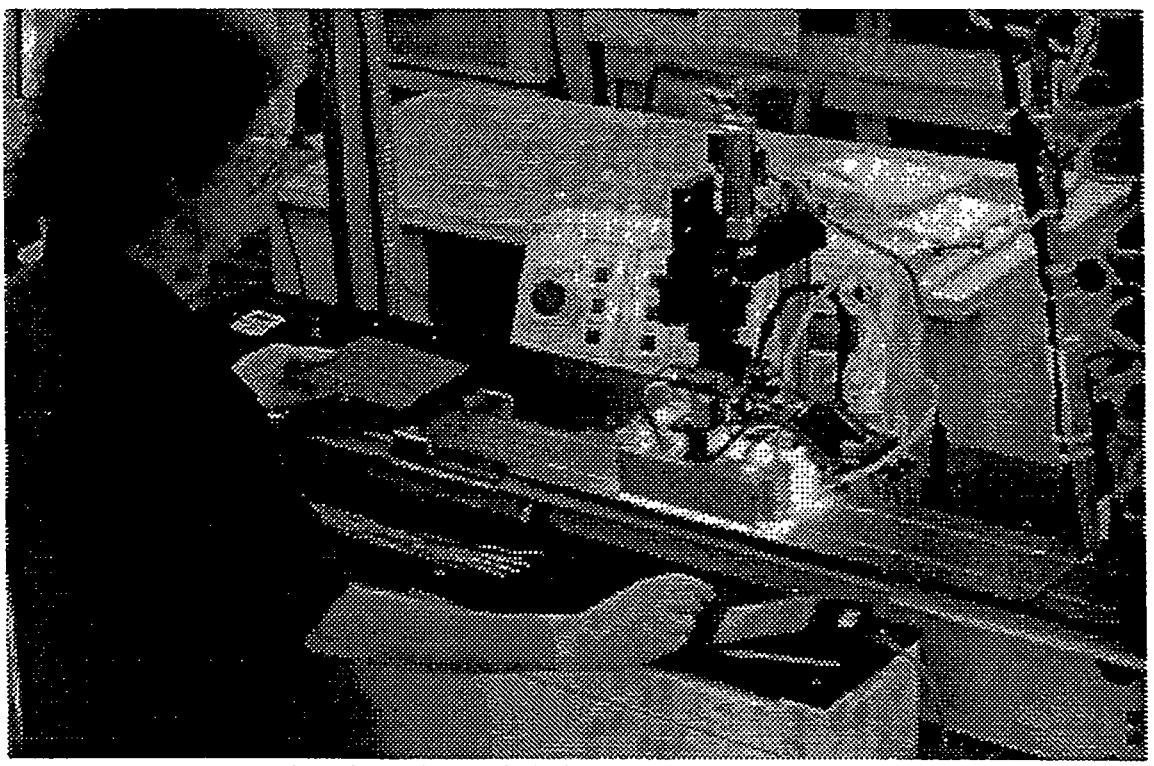


Figure 13. An automated wafer stringing/tabbing station assembling a string of Silicon-Film™ AP-225 modules.

56 Solar Cell Module Fabrication

Three modules consisting of 56 AP-225 solar cells were delivered to NREL during this program. The final module dimensions are 127.4 cm by 111.4 cm. This size and configuration was chosen for a feasibility study for future modules having 127.4 or 111.4 cm widths. No effort was made to automate module assembly processes for the intermediate 56 cell module. All steps (e.g. tabbing, stringing, lay-up) were done by hand. Early on, some shifting of individual cells during the lamination process led to uneven cell spacing. To eliminate this problem, 0.005 inch thick fiberglass sheet (Crane Glass 230) was used as cell backing.

Test data from the best 56 solar cell modules tested at NREL are shown in Table 9. The process column refers to the processing steps used to fabricate the solar cells in each module (similar to Table 13).

Table 9. NREL Outdoor Test Data for 56 Cell Silicon-Film™ Modules

ID #	Process	Temp (°C)	Aperture Area (m^2)	Voc† (V)	Isc† (A)	FF† (%)	Pmax‡ (W)	Aper. η (%)
D-28	advanced	15.7	1.391	31.9	6.1	74.9	147.9	10.6
D-29	baseline	19.7	1.400	30.5	5.6	68.4	115.4	8.2

†as measured

‡ corrected for irradiance to 1000 W/m^2, not corrected for temperature

The estimated U95 uncertainty of the NREL outdoor measurements is ±5%. Temperature was measured at the back of the module during testing; no correction for temperature was made. Total irradiance during these measurements was less or greater than 1000 W/m^2. For comparison purposes the maximum power entries in Table 9 are corrected to 1000 W/m^2. Corrections for spectral mismatch error and second order irradiance error were not made.

Progress in Module Performance

Figure 14 illustrates the progress made in 36 solar cell module performance during the course of the PVMaT program. Deliverable goals and achieved results are both represented.

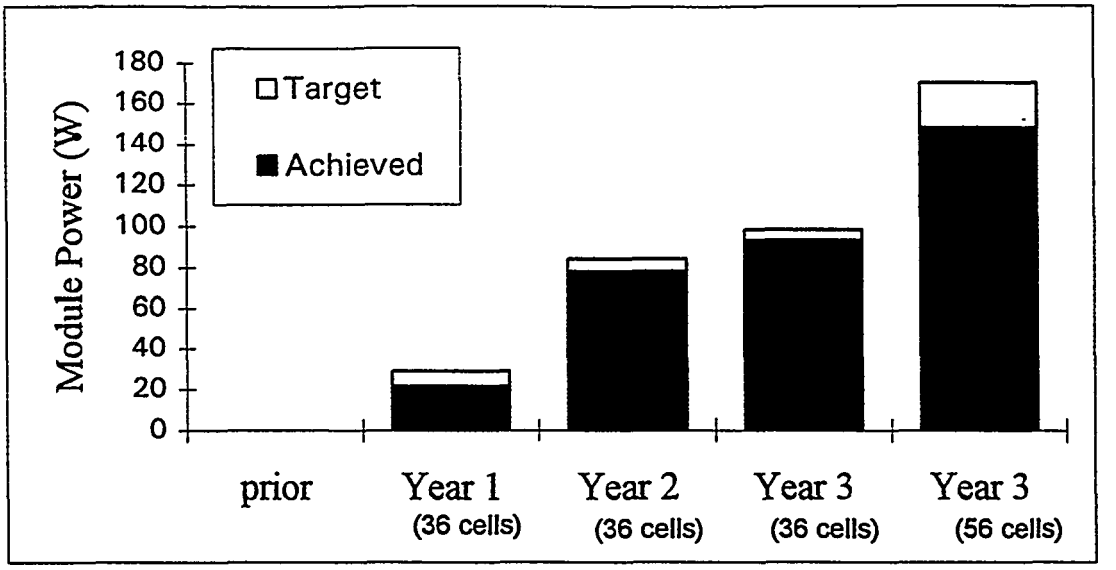


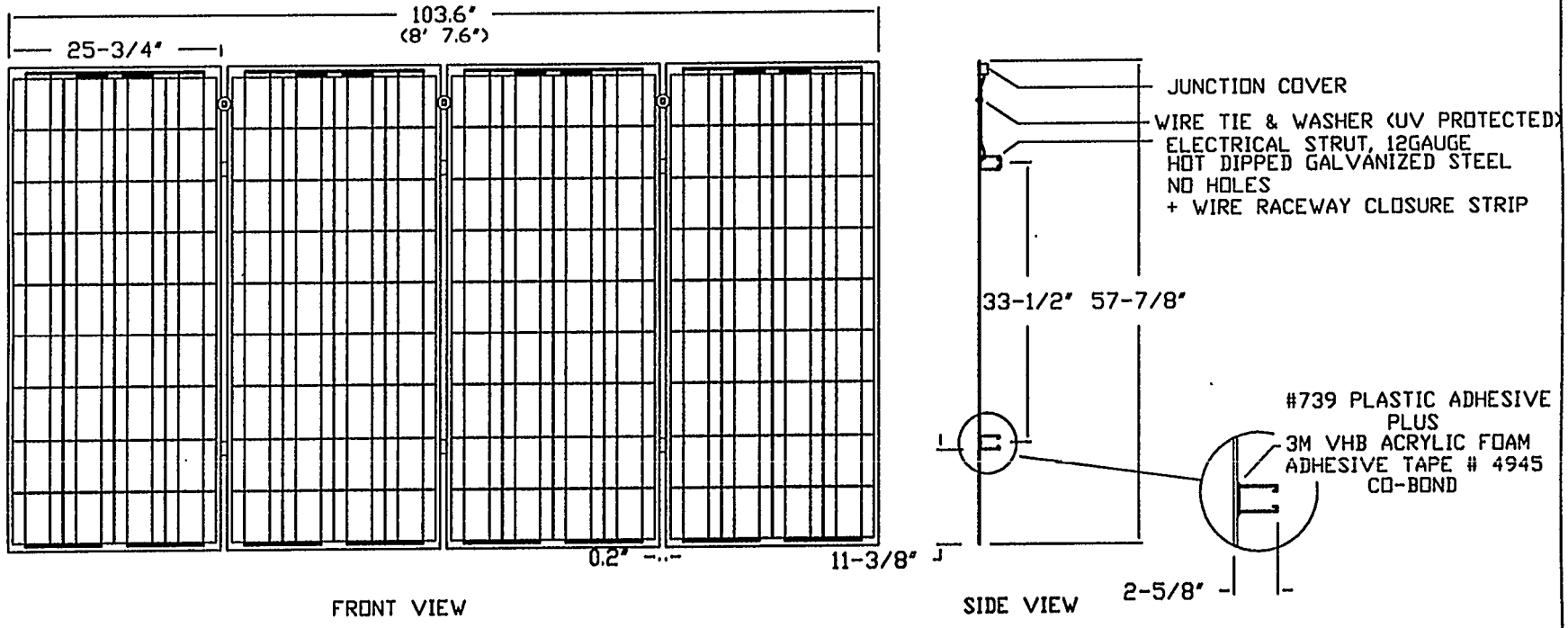
Figure 14. Progress in module performance throughout the PVMaT program.

New Large Area Panel Products

A large area panel has been developed around the AP225 Silicon-Film™ solar cell. The panel is approximately 4 ft by 8 ft. The first generation of this product will produce 320W. A schematic is shown in Figure 15. Costs of these panels will be reduced compared to conventional modules due to the elimination of frames and the incorporation of low cost electrical connects. Installation of the panels will be made by the incorporation of a structural support member and serial interconnection at the factory. Pre-assembly at the factory will allow the panels to be wired and tested prior to field installation. The panel is assembled from 4 frameless Silicon-Film AP-8225 laminates mounted on support rails. The laminates are attached with a combination of adhesive tape and silicone adhesive. Engineering and testing of the large area panel has been completed.

- The laminates will be frameless, attached to conventional steel support members (e.g. uni-strut) with 3M adhesive tape and silicone adhesive. The rail may also act as raceways for the wire.
- The use of conventional support materials allows the use of widely available accessories.
- A new spot welding process will be used to interconnect laminate tabbing to system wiring.
- Each panel consists of 4 laminates, interconnected in series.
- The electrical connection to the laminate is made with small, fully potted, "strain-relief" attachments.
- Edge protection for the panel will be provided to eliminate breakage during shipping and installing.
- 12 Panels will be packaged on a pallet (approximately 4 kW). 120 panels can be shipped per truck (approximately 40 kW).

DATE	SYM	REVISION RECORD	AUTH	DR.	CK.
6/22/95		ADHESION METHOD REVISION			
6/27/95		DIMENSIONS TO ENGLISH			



(4) AP8225 per Panel = 320W
Open Circuit Voltage = 79.2V
Short Circuit Current = 6.05A
Max. Power Voltage = 64V
Max. Power Current = 5A

AstroPower Solar Park Newark, Delaware 19716	DRAWN BY: JAKE BROWN	SCALE: NTS	LARGE AREA PANEL PROJECT
	CHKD:	REV #	
	CHKD BY:	SHEET 1 OF	
	DATE: 5/9/95	DWG #: NIM00001.DWG	

Figure 15. Schematic of the large area panel designed around the Silicon-Film™ family of products.

To assist in the development of this new panel product questionnaires were sent to five major U.S. system integrators, who collectively have significant experience in installing both utility scale PV systems, as well as rooftop PV systems. These two applications are the target market segments for the large area PV panel.

The questionnaire addressed both near term design optimization issues as well as longer term design "guidelines", relevant to future evolution of Silicon-Film™ products. The questionnaire covered the following areas for the near term design:

- Frameless laminates:
- Adhesively bonded back supports:
- Fully encapsulated module termination:
- Sacrificial Packaging:

Issues covered related to the long term evolution of the Silicon-FilmTM product were:

Mechanical configuration:

- Overall Dimensions:
- Weight:
- Shipping Package:
- Mechanical Interface:

Electrical configuration:

- Solar Cell Circuit:
- Connectors
- Inter-Laminate Wiring:

Responses are summarized as follows:

Near Term Design Optimization:

Frameless laminates were considered a good concept, as they run cooler and cleaner, and increase ground path distance. Handling problems need to be solved (i.e. edge protection) during shipping and installation. Adhesively bonded supports were not seen as a risk; sufficient field experience exists. Non-traditional approaches to module termination were met with some skepticism based on previous difficulties (ARCO Solar problems at John Long and Austin were mentioned). There was a mixed response on sacrificial packaging. The large project oriented companies reacted favorably, while the residential rooftop oriented companies worried about the volume of waste to be carried off-site.

Longer Term Design Guidelines

In terms of overall dimensions, the consensus was "bigger is better". Little economic value is associated with specific dimensional increments (e.g. 8' length). A weight of 150 pounds was perceived as being near the practical limits. Some suggestions indicated that the type of hand-holds provided to lift and carry the panel was more important that the exact weight. Materials used for edge protection should be recyclable.

Significant comments were received regarding the role of panel voltage in achieving source circuit voltage within certain capacity increments. In general, the following consensus might be drawn:

Rooftop (particularly residential rooftop) applications require relatively high voltage panels to reach source circuit voltages of up to 600 volts in capacity increments of a few kW. This issue has implications as to the practical maximum individual solar cell size for this application. Larger systems are more tolerant to a wide range of panel voltage. The bottom line seems to be; what saves money at the installed system level?

Larger Area Silicon-Film™ Potential
(Task 25)

During this PVMaT-2A program, the first commercial Silicon-Film™ product was identified and developed. This first commercial product was determined to be the AP-225 which has a specified size of 15.5 cm by 15.5 cm. However, it was also important to investigate the large area potential of the process and material. Due to convenience, an area 15.5 cm by 45 cm was chosen for this evaluation.

Wafer Production

The 15.5 cm by 45 cm wafers were produced under identical sheet production parameters as the standard AP-225. The sheet was simply cut in 45 cm lengths instead of 15.5 cm lengths.

Solar Cell Fabrication

15.5 cm by 45 cm solar cells were fabricated using two different fabrication sequences which were based on the baseline process (Table 6) and the advanced process (Table 7). Table 10 reflects the changes that were made to those processes due to size limitations of the standard AP-225 processing equipment:

Table 10. Process Sequences Used in Fabricating 15.5 cm by 45 cm Solar Cells

Baseline Processing	Advanced Processing
1) Surface Preparation (Sandblast +NaOH)	1) Surface Preparation (CP etch)
2) Gettering Diffusion w/ cells rotated 90° to fit in diffusion boat	2) Aluminum Deposition on backs (0.5 μm)
3) Etch Gettered Junction (NaOH etch)	3) Gettering Diffusion w/ cells rotated 90° to fit in diffusion boat
4) Standard Shallow Junction Diffusion w/ cells rotated 90° to fit in diffusion boat	4) Etch Gettered Junction (CP etch)
5) Isolate Edges	5) "Sandia-like" Diffusion w/ cells rotated 90° to fit in diffusion boat
6) PSG Removal	6) Forming Gas Anneal
7) Print/Dry/Fire Backs Ag (98%) /Al (2%) paste over entire back	7) RF Hydrogenation
8) Print/Dry/Fire Fronts Silver ink grid	8) Emitter Etch Back (CP etch)
9) RF Hydrogenation	9) CVD SiO_2 Passivation Layer
10) CVD SiO_2 and Si_3N_4 AR Coating	10) Evaporated Contacts
11) Test	11) CVD SiO_2 and Si_3N_4 AR Coating
	12) Test

Variations in the standard processing sequences were required to accommodate the larger wafers. In surface preparation a modified cassette was required to hold the wafers, and wafers were dried using a nitrogen blow gun instead of standard spin drying. For diffusion, wafers were loaded 90° from the standard position; gas flow was parallel instead of normal to the wafer. Print screens (baseline process) were not available for printing the back contact; therefore Al/Ag paste was painted on by hand. The automated spray AR machine could not be used for the baseline solar cell process due to insufficient length of the heated zone. Wafers were placed on graphite platens in all CVD depositions and in RF hydrogenation to ensure even heating. In addition, it was determined that the following areas would require significant improvements to handle the larger cells in any significant volume:

- surface preparation (higher throughput, automated drying)
- diffusion (higher throughput)
- isolation (higher throughput)
- contacts (screens for printing backs, furnaces with longer heat zones)
- AR coating (automated spray AR machine for higher throughput)
- testing (automated tester)

Improvements in solar cell processing parameters were needed to bring the 15.5 cm x 45 cm solar cell to a level commensurate with the standard AP-225. Changes in CVD deposition parameters, contact firing temperatures, and gridline and busbar designs were required. Table 11 shows the performance (measured at NREL) of the 15.5 cm by 45 cm deliverables fabricated from identical material using the two different fabrication sequences shown in Table 10. Also included is AP-225 solar cell performance (measured at NREL) from similar quality material illustrating the deviation in performance due to size. As shown, the size of the solar cell had little effect on the power densities measured.

Table 11. Comparison of Solar Cell Performance using Advanced and Baseline Processes on 15.5 cm by 45 cm and 15.5 cm by 15.5 cm Solar Cells.

Processing	Aperture Area (cm^2)	Power (W)	Power Density (mW/cm^2)	% Difference in Power Density
baseline	677.9	6.31	9.3	1.1 %
baseline	240.3	2.40	9.2	
advanced	676.4	7.87	11.6	1.7 %
advanced	238.7	2.82	11.8	

*measured using a SPIRE 240A simulator

Yield Data

Immediately following the three 16 hour production runs of December 1994, the wafer machine was operated to produce five planks; from each plank was cut one 15.5 cm x 45 cm wafer. These wafers were processed into solar cells using the baseline solar cell production process shown in

Table 12. Our goal was to determine potential mechanical yield problem areas in the fabrication process. Yield data for these 15 wafers is listed in Table 12. Y_M is the mechanical yield of the wafers through baseline solar cell fabrication process.

Table 12. Yield Data For Five 15cm x 45cm Solar Cells From Each 16-Hour Production Run

Run #	Wafer Starts	Finished Solar Cells	Y_M (%)
996	5	3	60
000	5	4	80
001	5	4	80

Mechanical yield losses were due entirely to wafer breaks during the diffusion process. All fifteen wafers were diffused together. The diffusion boat had been modified to handle the larger wafers rotated by 90°; however, sufficient space was not provided for the wafers' thermal expansion. Four wafers broke as they reached temperature during gettering diffusion. The boat was then modified for the standard junction diffusion; no wafers broke using the modified boat.

Conclusions from Large Area Solar Cell Effort

The following conclusions were drawn from the 15.5 cm by 45 cm development work:

- excellent material quality uniformity has been achieved along the 16.5 cm wide sheet,
- the cell processing changes required to handle small quantities of the larger area cells did not significantly affect device performance, and
- for a high volume effort involving 15.5 cm by 45 cm wafers, improvements in processes and equipment would be needed in all areas of device processing to achieve acceptable throughput and yields.

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The goal of AstroPower's PVMaT-2A project was to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate module. This process starts with the production of continuous sheets of polycrystalline silicon on a supporting substrate using the Silicon-Film™ process. A number of new solar-cell and module products have resulted from this work. The primary product is a 240 cm^2 solar cell referred to as the AP-225. This product has achieved an efficiency of 12.2% (AM1.5 global 1000 W/m^2). A 17.1 global kW array was constructed for PVUSA using the AP-225 solar cell and was installed in November 1994. Along with the AP-225, a second, larger solar cell was developed. The AP-675 solar cell has a device area of 700 cm^2 and has achieved an efficiency of 11.6% (AM1.5G, 1000 W/m^2). Two new module products accompanied the new solar-cell products.

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