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Sixth Workshop on The Role of Impurities and Defects in Silicon Device Processing

Summary of the Panel Discussions

August 12-14, 1996
Snowmass, Colorado

Workshop Chairman:
B.L. Sopori

Prepared by:
T. Tan, R. Swanson, and B. Sopori

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The Sixth Workshop on the Role of Impurities and Defects in Silicon Device Processing was held in Snowmass Village, August 12-14, 1996. The workshop was attended by 87 participants from academic institutions and photovoltaic industry representatives, from the United States, Australia, Belgium, Canada, France, Germany, Italy, Japan, Belgium, and The Netherlands. The workshop consisted of nine sessions that addressed different aspects of impurities and defects in silicon and applications to solar-cell processing. Each session opened with some review talks summarizing recent advances in this field and introduced important issues for further discussions during a subsequent panel discussion session. In addition, the latest research results were presented in two poster sessions.

The theme of the workshop was "**Technology Transition for Fabricating High-Efficiency, Low-Cost, Commercial Silicon Solar Cells.**" Choice of this theme reflects two important advances in silicon solar cells, one of these advances shows that a great deal of understanding of the basic mechanisms of impurity and defect interactions has occurred in the area of solar-cell processing. This understanding has led to the identification of many mechanisms that limit the cell performance, and has shown that processes such as impurity gettering and passivation can be successfully applied to mitigate such limitations. Incorporating steps such as phosphorus diffusion, aluminum alloying, and hydrogen passivation into the solar-cell fabrication improves the material quality and hence, yields better cell efficiencies. In fact, the application of these concepts has yielded small-area, laboratory solar cells with efficiencies greater than 18.5% on commercial substrates, and large-area, prototype encapsulated cells of greater than 15% efficiency. In the second are of advancement, we see that the silicon solar-cell industry is increasing its capacity in response to higher PV energy demands. This will necessitate acquiring new equipment and trying to upgrade processes to achieve higher efficiencies. Thus, now is the appropriate time for industry to incorporate advanced processes in production. We expect that incorporating these new fabrication approaches into production can lead to 16% commercial solar cells, perhaps without increasing the cell costs. Indeed, the PV industry is evaluating these concepts and, in some cases, has already begun to introduce several other cost-saving approaches. It is believed that these low-cost cell fabrication approaches can realistically promise PV energy costs approaching $2/Wp.

Discussion:
Availability of Poly Feedstock and Purity of Wafers

Panel Members:

Kim Mitchell (Discussion Leader), Dan Heck, Chandra Khattak, Hans Möller, Fritz Wald

The photovoltaics industry growth accelerated during 1990-1995 to reach 71 megawatts in 1995. The market share of crystalline Si increased from 74% in 1990 to 87% in 1995, thereby increasing the Si materials demand from 604 MT in 1990 to 1203 MT in 1995. The Si materials used by the PV industry were or are largely off-spec virgin (40% in 1994) and remelt (55% in 1994) from the semiconductor industry. The Si materials' availability to the PV industry relies on the excess capacity of the polysilicon manufacturers and the availability of off-spec feedstock. Because most off-spec materials are now being used internally by the semiconductor industry, there is considerable concern about a possible shortage of the feedstock. Indeed, the conventional supplies of poly feedstock to the PV industry have become severely constrained in the last year and a half.

In the near-term, most PV companies have responded by re-examining their feedstock specifications and sourcing options, and improving the efficiency of their internal processes. However, the long-term growth of the PV industry will require a consistent, dedicated supply of solar-grade Si in the order of 2000+ MT per year. To this end, an open-member SOG-Si Stakeholders Group has met informally to provide an industry-wide forum for understanding the issues and soliciting interests from potential poly feedstock suppliers.

A solar-grade silicon specification has been drafted to provide the broadest definition of "solar-grade" feedstock in terms of size, resistivity, and impurity levels. Proper packaging is emphasized to prevent contamination and to facilitate use by the buyer. Currently, there appears to be no special requirement on the size or form. On the purity issue, the following are the general requirements: it is preferred that poly have either B or P doping, with no compensation; resistivity at 25 °C should be greater than 1 Ω-cm; oxygen and carbon should not exceed the saturation limits in the melt; and the total non-dopant impurity concentration should be less than 1 ppma.

Discussion: Methods for Thin-Layer Silicon Growth/Deposition/Processing for Solar Cells

Harry Atwater (Discussion Leader), Andrew Blakers, Jim Rand, Zhengrong Shi, Jurgen Werner, Eli Yablonovitch

Thin-layer silicon solar cells have a potential for yielding high efficiencies even with the use of lower quality material. However, this is only possible if the following criteria are met: the thin layer of silicon can be grown on a low-cost substrate, cell design allows efficient trapping of light, the interface recombination is low, and suitable techniques are developed that permit deposition and subsequent processing of silicon at low temperatures. The panel addressed the following issues: the types of substrate needed, the methods of silicon deposition that are compatible with low-cost substrates, and typical deposition rates.

Much of the discussion surrounded the substrate requirements and cost-effectiveness of the substrate and deposition processes. General arguments based on straightforward process steps, in vogue now, would not lower the $/W costs by going to thin-layer silicon solar cells. Rather, limited research performed to date has focused on conventional approaches of liquid-phase epitaxy on single- and multicrystalline silicon substrates, depositions on ceramic and special glasses. These processes clearly are not compatible with low-temperature glasses that have a softening point around 500 °C. If the high-temperature processes for silicon deposition were unavoidable, the cost of the substrate might become an issue. It was generally felt that a thin-layer silicon solar cell would gain acceptance only if a 12%-13%-efficient cell of this structure is demonstrated. The group discussed the costs of various potential substrates as well as deposition processes and it reached the following conclusions.

- It was generally believed that sodalime glass may be the only currently available material that would meet the cost requirements of a substrate. Other substrates such as metallurgical-grade silicon, ribbons, and moderate-quality multicrystalline silicon wafers could not meet the cost requirements, although they would simplify growth processes and thermal-matching demands.

- Several deposition processes such as chemical vapor deposition using chlorosilanes, epitaxy-like processes for deposition from liquid melt produced by metal-silicon eutectics, and magnetron sputtering could meet the throughput requirements.

- The grain size needed to yield reasonable voltages for >12%-efficient cells appears to be about 100 μm. Producing such a grain size in a thin layer would require grain-enhancement techniques or recrystallization.

- The cell structure and process techniques would have to be tailored to the temperature demands of the substrate. Conventional processes of diffusion, requiring >800 °C temperatures, would not be suitable for junction-formation processes.

There was no well-identified device configuration for a thin layer silicon cell. It was felt that making contacts to such a cell may be difficult. The group agreed that interface recombination would play a major role in controlling the cell efficiency. Passivation of interfaces and grain boundaries would be crucial. It is anticipated that new light-trapping designs based on modeling will emerge that can better define the cell configuration.

Discussion:
Impurity and Defect Interactions during Gettering/Defect Passivation

Panel Members:

Lubek Jastrzebski (Discussion Leader), Isabelle Perichaud, Sergio Pizzini, Doug Ruby, Carl Seager, Scott McHugo

The discussion centered on the process of gettering metallic impurities, including the dissolution from a precipitated state, their diffusion to the gettering region, and the subsequent stabilization in the gettering region. The methods of gettering include intrinsic (internal) gettering and external gettering, referred to as the gettering region locations. The mechanisms include relaxation-induced gettering, segregation-induced gettering, and injection-induced gettering. For solar cells, only the external-gettering schemes of Al, P, or (P+Al) can be used. Gettering using (P+Al) works best. Gettering can be very effective in low-dislocation-density ($<10^6$ cm^{-2}) materials also containing a low oxygen concentration. For a dislocation-density higher than ~10^7 cm^{-2}, gettering usually does not work, possibly because of impurity dissolution from precipitates and the formation of oxygen precipitates. It is not practical to getter slow diffusers such as Ti. The gettering processes show a temperature dependence, with the optimal gettering temperature at ~900 °C. Above 900 °C, the process can sometimes lead to a deleterious effect, probably because of oxygen precipitation and because of the metallic impurity atom release from precipitates that is necessary to reach a concentration higher than that initially present in the solution.

Presently, understanding on the intrinsic electrical activity of undecorated defects (e.g., point defects or dislocations) in Si is poor. Knowledge on the interaction of impurities with defects is very limited. Thus, further work needed will include experimental and modeling studies of the impurity release process, material degradation at high gettering temperatures, and the relation to the H passivation process.

In Si, the hydrogen passivation process is driven by a chemical or electrochemical potential, which is independent of the materials type but depends on the nature of the surface state. The process appears to be influenced by morphology and chemistry, vacancy concentration (V-H pairs), and oxygen concentration (O-H bonds). Passivation occurs via bond formation with dangling bonds (e.g., SiH_1) at surfaces. Thus, there is a large number of factors influencing the pas-

sivation process. Presently, it is not known what are the defects that can be passivated, why oxygen can passivate the Si surfaces but not extended defects, what metallic impurities can be passivated by hydrogen or other chemical species by compound formation, if there are any chemical species that can passivate extended defects, and the configurations of the surface species and their energy positions in the gap (except for some metals at clean and specifically oriented surfaces).

Some of the possibilities for making the passivation process more viable include the use of external surfaces as a model for extended defects, and carrying-out ad-hoc experiments using spectroscopic and electrical measurements to understand the physics and chemistry of passivation; on the basis of known values of metallic hydride bond energy, do hydrogenation experiments of metal-doped Si and establish the correlation with the passivation yield; do hydrogenation experiments on oxygen and metal-decorated dislocations, and conduct computational or theoretical studies.

Discussion: Effects of Impurities and Defects

Panel Members:

Teh Tan (Moderator), Kim Kimerling, Lubek Jastrzebski, Eicke Weber

In Si, all impurity species, as well as the native point-defect species vacancies and self-interstitials, reach a thermal equilibrium concentration at a given temperature. On the other hand, the extended defect species, including dislocations, stacking faults, and grain boundaries, are not thermal equilibrium defects; i.e., their thermal equilibrium concentration is identical to zero. Nonetheless, extended defects always exist in real Si crystals, which are introduced during crystal growth or other high-temperature processes. Their introduction is due to the kinetic requirement that the crystal's Gibbs free energy be minimized at a maximum possible rate at the given temperature. Thus, dislocations may be generated by stress relief and/or by point-defect condensation, which do not result in the minimum Gibbs free energy of the system, but the Gibbs free energy lowering rate is the largest. All impurities interact with all kinds of defects. For example, more impurity atoms are dissolved near a dislocation core. At the dislocation core, the impurity-precipitate nucleation barrier is lowered by ~1 eV. Similarly, a dislocation-loop nucleation barrier is lowered by impurity-atom aggregates and precipitates.

Extended defects and metallic impurities degrade the solar-cell efficiencies via degradation of the Si minority-carrier lifetimes or diffusion lengths. Even clean dislocations contain recombination sites. Such sites are few, e.g., probably only at kinks and jogs. Clean dislocations can be passivated. Dislocations decorated by metallic impurities (e.g., Fe) are very active electrically, leading to decreased V_{oc} in solar cells. The ways of reducing the ill effects of defects and impurities include reducing metallic contaminants in the feedstock and processing environments, reducing dislocations by minimizing thermal gradients, passivation by H, and the use of gettering. However, it is known that a high density of dislocations leads to "bad" regions in multicrystalline solar-cell Si, which cannot be improved by a gettering treatment.

There is no established standard on the tolerable impurity concentration level and dislocation density in solar cells. However, the established standard for the integrated-circuit industry is that there should be no dislocations, and the concentration of Cu and Ni should be less than 10^{12} cm^{-3}, that of Fe, Cr, and Mo should be less than $3x10^{11}$ cm^{-3}; that for Ti and V should be less than

$3x10^{10}$ cm^{-3}; and that of the inert impurities O and C should be less than ~$7x10^{17}$ cm^{-3} and $4x10^{16}$ cm^{-3}, respectively.

Discussion:
RTP and Belt Furnaces as Potential Solar-Cell Processing Technologies

Panel Members:

Bala Bathey (Discussion Leader), Don Lindholm, Chungshin Lee, N. M. Ravindra, Mike Kardauskus, Mohan Narayanan

Rapid thermal processing is gaining acceptance in the microelctronics industry as a cost-effective process for fabricating contacts, ion-implant annealing, and reflow processes. It is, however, anticipated that as the wafer size goes beyond 8 in., the RTP processing may out-perform conventional furnace processing in uniformity. Future devices based on <-0.25-μm device rules highly favor RTP. The demands on an RTP processing system for microelectronic fabrication are extremely severe, resulting in quite expensive machines. However, it is believed that solar-cell fabrication does not demand such stringent requirements, which may significantly reduce the cost of such units. Some preliminary comparison of the throughput for diffusion process steps, indicate that RTP could be competitive with furnace diffusion. In addition, certain substrates, such as ribbons, may have higher yield. Several photovoltaics manufacturers have planned acquisition of RTP systems to evaluate the systems' performance.

RTP fabrication may offer other advantages that are not yet recognized in the industry. For example, enhanced diffusion due to optical illumination may increase the through-put of such a system.

The cost of RTP process steps and its throughput is a matter of debate at this time. The major time factors appear to be the loading and unloading of wafers compared to the actual process time.

RTP systems are extensively used in large-area display devices.

Belt furnaces offer a distinct advantage of large throughput. However, processing on a conveyor belt could have severe repercussions if very high temperatures are required—it can produce thermal stress that may result in excessive wafer breakage. Additionally, maintaining a clean ambient is difficult.

Discussion:
How Can the Proposed Processes be Implemented in Production Environment?

Panel Members:

R. M. Swanson (Discussion Leader), James Gee, Bob Hall, Juris Kalejs, Richard King, Hugo de Moor, J. Poortmans

The technical progress since the last workshop has been truly staggering. Gettering is now well-enough understood to be used with the confidence and comfort that the processes are doing what is advertised. Low-temperature passivation using plasma-enhanced (PECVD) nitride is now well established and provides an additional attractive avenue for hydrogenation. Hydrogenation itself is much better understood, with regard to both diffusion and passivation mechanisms. A startling development is the continued confirmation that diffusion of optical enhancement is now confirmed by multiple groups and can have large, beneficial effects. The workshop consensus is that thin wafers are doable and offer significant advantages in performance and cost. Clearly, all manufacturers must be preparing for this trend. Most new processes that are under serious consideration, such as increased use of RTP and belt furnaces, appear to have acceptable economics. Manufacturers would do well to keep a close eye on wafer handling, loading, and unloading costs. These can be the dominant throughput and cost drivers. Two promising approaches to improvement are: selective emitters combined with screen printing and PECVD passivation and hydrogenation, and non-screen-printed processes with improved metal aspect ratio and decreased contact resistance. Surprisingly, most workshop attendees felt that several non-screen-printed processes hold promise and deserve serious consideration. There is some disappointment that the adoption of these new processes into products has been slow. There are many reasons for this, but the most significant is the poor profitability performance of the PV industry. The tools for continuing the historical continuous improvement in module performance and cost are clearly in place and bode well for the industry; however, it appears that continued support from government programs such as photovoltaic manufacuring technology and from the national laboratories (NREL and Sandia) are still crucial to the long-range success of the PV industry. In contrast to the cornucopia of exciting new processes, a large cloud hangs over the industry in the specter of a polysilicon shortage of serious proportions. The industry will likely be preoccupied with this problem for some time to come, and this will further delay the introduction on new processes.

Concluding Remarks

It is clear that under the conditions of curtailed funding, future research should focus on mechanisms limiting cell efficiency. The near-term goal of the NREL/DOE program is to perform coordinated research that can lead to the manufacture of silicon solar cells of 18% AM1.5 efficiencies. At the same time, the potential of thin layer silicon needs to be explored. It is clear that future research should include further understanding the mechanisms that limit large-area cell performance and developing processes that can overcome these limitations to produce greater than 18% large-area cells. Recent work has shown that current gettering and passivation processes that work well in low-defect-density regions of a silicon wafer are not effective in the regions of high dislocation densities (defect clusters). As a result, regions of defect clusters lead to strong non-uniformities in the cell with low-performing regions acting as "sinks." Therefore, emphasis must be placed on characterizing such defect clusters, determining what prevents effective gettering, and arriving at processes that can improve these regions. Some suggestions to help achieve these goals include identifytng:

- Mechanisms that prevent impurity gettering and passivation in the regions of defect clusters
- Impurity-defect interactions during crystal growth that cause decoration of defects
- Impurity dissolution during gettering
- Dissociation of defect networks by post-growth processes
- Passivation of defect clusters
- Optimum process sequences that can produce synergistic effects of gettering and passivation and that are compatible with low-cost processing.

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This report is a summary of the panel discussions included with the Sixth Workshop on the Role of Impurities and Defects in Silicon Device Processing. The theme of the workshop was "Technology Transition for Fabricating High-Efficiency, Low-Cost, Commercial Silicon Solar Cells." This workshop provided a forum for an informal exchange of information between researchers in the photovoltaic and non-photovoltaic fields on various aspects of impurities and defects in silicon, their dynamics during device processing, and their application in defect engineering. This interaction helped establish a knowledge base that can be used for improving device-fabrication processes to enhance solar-cell performance and reduce cell costs. It also provided an excellent opportunity for researchers from industry and universities to recognize mutual needs for future joint research.

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