The Crystalline-Silicon Photovoltaic R&D Project At NREL And SNL

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Abstract. This paper summarizes the U.S. Department of Energy R&D program in crystalline-silicon photovoltaic technology, which is jointly managed by Sandia National Laboratories and National Renewable Energy Laboratory. This program features a balance of basic and applied R&D, and of university, industry, and national laboratory R&D. The goal of the crystalline-silicon R&D program is to accelerate the commercial growth of crystalline-silicon photovoltaic technology, and four strategic objectives were identified to address this program goal. Technical progress towards meeting these objectives is reviewed.

INTRODUCTION

While a wide variety of semiconductor materials have been examined and are still currently under development for photovoltaic (PV) modules, the dominant technology today still uses bulk crystalline-silicon (c-Si) substrates. Crystalline-silicon PV modules represented around 85% of the 81 MW_p of PV modules sold in 1995 [1]. Despite the relative maturity of c-Si PV technology, industry continues to make improvements in their manufacturing processes and module design to reduce manufacturing cost and increase throughput. For example, Wohlgemuth *et al.* recently reported that Solarex is on target to reduce the manufacturing costs of their multicrystalline-silicon (mc-Si) module by a factor of 2 and increase their manufacturing capacity by a factor of 3, while Mitchell *et al*. described the relatively straightforward extensions of present technology necessary to reach a production level of 100 MWp per year using Czochralski (Cz) silicon [2,3]. Basore and Gee noted that c-Si PV is capable of meeting a residential PV system market of around 40 GW_p in the United States (U.S.), while a recent European study found that conventional c-Si PV modules could reach direct manufacturing costs approaching \$1 per W_p at production levels of 500 MW_p per year [4,5]. The net result is that c-Si PV technology has followed an aggressive learning curve, with various reports associating a reduction of 68% and 83% in average selling price

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with each doubling of cumulative sales [6,7]. Extrapolation of these economic and technical trends with PV growth rates of between 20 and 40% achieved in recent years by U.S. PV manufacturers predict that c-Si PV modules will be able to meet U.S. Department of Energy goals for 2000 and 2010 as outlined in the recent five-year plan [8].

The past success and current improvements in c-Si PV technology has benefited greatly from the R&D investment in c-Si technology, and the U.S. Department of Energy supports a R&D project in c-Si PV technology to help continue this progress. This paper reviews the U.S. DOE crystalline-silicon PV R&D program. This program is jointly managed by researchers from the National Renewable Energy Laboratory (NREL) and Sandia National Laboratories (SNL), and features a balance of basic and applied R&D, and of university, industry, and national laboratory R&D. The paper first provides a description of the mission and strategic objectives, and then provides a description of the technical projects that address these strategic objectives. Included in the description of the technical projects are selected recent technical highlights from the national laboratories. For completeness, references are supplied for supporting work by university subcontractors.

MISSION AND STRATEGIC OBJECTIVES

The goal of the Crystalline-Silicon R&D Project is to accelerate the development of c-Si photovoltaics and to enhance the United States' position in c-Si photovoltaics technology. This goal is approached through the following objectives:

- Improve the performance and/or reduce the cost of *present-generation commercial* c-Si solar cells and modules.
- Improve the *fundamental understanding of crystalline-silicon material*, with an emphasis on controlling the deleterious effects of impurities and defects in crystalline silicon.
- Develop *next-generation* c-Si PV technologies that significantly improve throughput, reduce energy consumption, and/or reduce manufacturing cost compared to the present technology.
- Coordinate national laboratory, university, and industry c-Si PV research, and non-PV c-Si R&D programs, through hosting of a workshop on c-Si processing and through operation of a c-Si R&D cooperative (Crystalline-silicon Research Cooperative).

TECHNICAL PROJECTS AND HIGHLIGHTS

The mission goal of the project is approached through three technical tasks: silicon crystal growth, crystalline-silicon material science, and crystalline-silicon devices and processing. The goals and status of each of these tasks are reviewed.

Silicon Crystal Growth

This task emphasizes research on innovative and novel approaches to Si crystal growth methods, which complements work in industry by examining next-generation technologies. These new crystal growth methods potentially have superior throughput, reduced energy and/or materials cost, and/or improved conversion efficiency compared to existing approaches.

There is currently considerable interest worldwide in thin-layer c-Si PV [9]. Thin-layer c-Si refers to crystalline-silicon layers with thicknesses less than 100 μm on a supporting substrate. The potential advantages of thin-layer c-Si PV include reduced material and energy usage compared to bulk c-Si PV, all planar processing for reduced manufacturing costs, and monolithic module integration. Our work (Ciszek *et al.*) in this task is examining growth of thin-layer c-Si films on low-cost metallurgical-grade c-Si substrates (MG-Si) by liquid phase epitaxy (LPE). LPE is an attractive technique because it has adequate growth rates (around 1 μm/min) at moderate temperatures (around 900°C), has high quality (near-equilibrium crystal growth), and uses relatively simple equipment. A conventional method to improve surface wetting in LPE is to melt back the surface in the solution. However, the melt-back step is not desirable with metallurgical-grade silicon substrates since impurities from the substrate would then contaminate the solution. We developed a Cu-Al-Si that is able to wet the surface well without a melt-back step. The high solubility of Si in Cu-Al (20-35%) at a growth temperature of ~900°C also creates an atomically rough solid/liquid interface, facilitating isotropic growth and a macroscopically smooth crystal surface (Figs.1 and 2). Details of this work is provided in another paper at this conference [10].

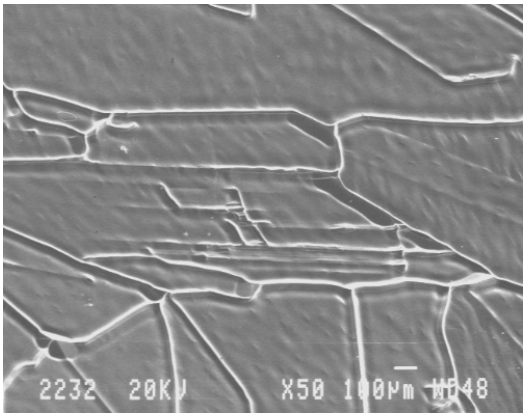

Figure1. Surface morphology of a LPE-Si/MG-Si layer grown from a 23%Si-28%Al-49%Cu solution.

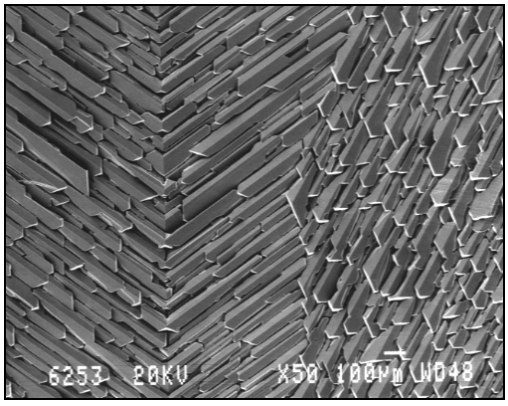

Figure 2. Surface morphology of a LPE-Si/MG-Si layer grown from a 3%Si-97%In solution.

Other work in thin-layer c-Si PV supported by the SNL/NREL c-Si PV Project includes seeded crystal growth (California Institute of Technology) and optical confinement theory and experimentation (University of California/Los Angeles and NREL). Some of this work is summarized in other papers at this conference [11-13].

Crystalline-Silicon Material Science

This task seeks to develop a fundamental understanding of the role of defects and impurities in c-Si materials and device processing. The goal of this research is to ameliorate the deleterious effects of defects and impurities in c-Si solar cells, which is an important objective with high industry relevance because the concentrations of defects and impurities are frequently increased by the use of lower cost Si feedstock and c-Si growth methods. Major activities in this task include generation and characterization of samples with controlled concentrations of dopants, impurities, and defects, research on the physics of and methods to getter impurities and passivate defects, and hosting of a workshop on crystalline-silicon PV technology. A major concern of this task is to improve the performance of large-area multicrystalline-silicon solar cells whose performance is reduced by the influence of bad grains that are difficult to getter using conventional methods. A summary of R&D requirements for improving large-area mc-Si cell performance is presented in another paper at this conference [14].

Iron is a very common metallic impurity in silicon that is also a recombination center. Developing a fundamental understanding of Fe in silicon, including interactions with crystal defects and with other impurities (dopants, oxygen, etc.), is of increasing importance due to the wider usage of less pure Si feedstock and interest in new thin-layer c-Si growth techniques using metallurgical-grade c-Si substrates. The float-zone (FZ) method for silicon crystal growth allows a high degree of control over background impurity and defect levels and is an excellent vehicle for controlled studies of deliberately introduced impurities and/or defects. At NREL, we (Ciszek *et al*) grew Fe-doped multicrystalline ingots by the FZ method to study Fe effects on minority charge carrier lifetime, grain structure, and electron-beam-induced current characteristics of multicrystalline silicon. Details of the growth and characterization is provided in Ciszek *et al.* [15].

Representative data is presented in Fig. 3. The minority-carrier lifetime decreased monotonically with increasing Fe content for similar grain sizes (from ~10 μs to 2 μs for $< 10^{-3}$ cm^2 grains, from ~30 μs to 2 μs for ~5 x 10^{-3} cm^2 grains, and from ~300 μs to 2 μs for $> 10^{-2}$ cm^2 grains) as the Fe content increased to $1 \cdot 10^{16}$ atoms/cm^3. We had previously observed that grain size alone has a strong effect on lifetime. We also saw evidence of constitutional supercooling in the heavily doped samples, with a dramatic accompanying effect on grain structure [15]. Such observations might aid in understanding the precipitation of Fe during ingot crystal growth and design of new thin-layer c-Si growth techniques.

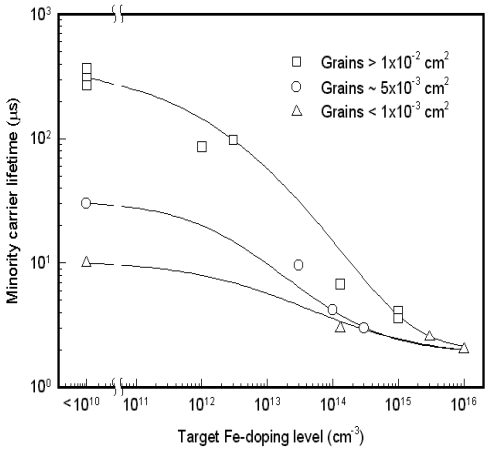

Figure 3. Measured bulk minority-carrier lifetime vs. target Fe-doping level for float-zoned multicrystalline-Si ingots with various grain sizes.

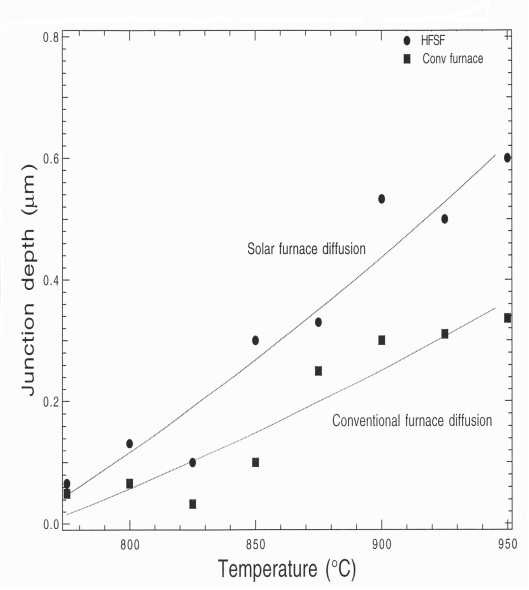

Figure 4. Junction depth of phosphorus diffusion performed with a solar furnace and with a conventional furnace.

Other work in this task includes the following: research on the physics of gettering and hydrogen passivation; development and characterization of gettering techniques on commercial c-Si materials; and development of new gettering techniques [16-23].

Crystalline-Silicon Devices and Processing

This task develops new processes and device structures with a goal of improving commercial PV module performance (cost, efficiency, and reliability). This task emphasizes research activities with near-term impact that are identified collaboratively with major c-Si manufacturers. Recent work at the Georgia Institute of Technology and at SNL has found that the material quality of photovoltaic-grade c-Si substrates is capable of much higher performance than can be obtained with commercial fabrication processes, so that there is ample opportunity to improve the performance of commercial c-Si modules [24,25].

The goal of our process development work is to develop processes with significantly improved throughputs. Optical processing methods -- such as optical anneals, rapid thermal processing, or solar furnace processing – are of interest due to the reduced thermal budget and short process time. In particular, there may be possible kinetic advantages to optical processing. We (Tsuo *et al.*) recently demonstrated that dopant diffusions performed using high-intensity solar flux are deeper than obtained with the same time-temperature profile in an isothermal furnace (Fig. 4). This same work also demonstrated improved out-diffusion of impurities from a metallurgical-grade multicrystalline-silicon substrate [18]. Other

work in this task includes development of plasma processes and novel doping processes for forming back-surface fields [26,24,29].

Major emphasis in cell development this year will be placed on two novel cell concepts (emitter wrap-through cell and self-aligned selective-emitter cell) that have the potential for significantly improved performance and reduced cost. The self-aligned selective-emitter cell uses plasma processing to achieve a low-recombination passivated emitter with commercial metallizations (Fig. 5). The cell is potentially low cost because the cell uses screen-printed grids, the emitter etch is self aligned, and the plasma etch and deposition can be performed in the same chamber. We (Ruby *et al.*) recently demonstrated an improvement in efficiency of 0.5% absolute with the new process compared to the baseline process on 103-cm^2 multicrystalline-silicon cells [26].

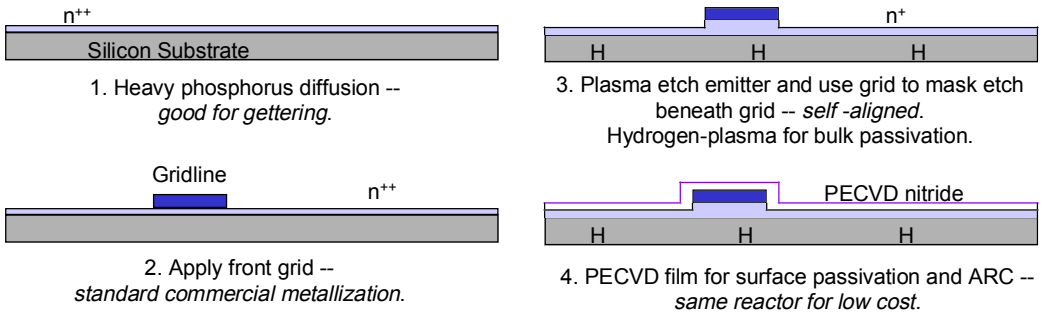

Figure 5. Process sequence for self-aligned selective-emitter cell. PECVD refers to plasm-enhanced chemical vapor deposition. A plasma hydrogenation step can also be included in the process.

The second cell concept under investigation is the emitter wrap-through (EWT) cell. The EWT cell has both contacts on the back surface, which is achieved by wrapping the emitter through laser-drilled holes from the front surface to the back surface (Fig. 6). The back-contact geometry has potentially higher performance due to no grid obscuration, and we (Gee *et al*) have projected efficiencies over 20% for 100-cm^2 EWT cell using photovoltaic-grade silicon [24]. The best result to date is 15.7% for a 42-cm^2 EWT cell with bifacial contacts and a photovoltaic-grade Cz silicon substrate [24].

The most significant advantage of the back-contact configuration is simplification of the module assembly. The present geometry with contacts on front and back surfaces is difficult to automate and module fabrication (including labor and materials) now accounts for nearly 50% of the finished module cost [27]. We (Gee *et al.*) are working on a new module assembly concept that encapsulates and electrically connects *all* the cells in the module *in a single step.* The key features of this new process include the following: (1) back-contact cells; (2) a module backplane that has both the electrical circuit and encapsulation material in a single piece; and (3) a single-step process for assembly of these components into a module (Fig. 7). This process reduces costs by reducing the number of steps, by

eliminating low-throughput (e.g., individual cell tabbing, cell stringing, layout, etc.) steps, and by using completely planar processes that are easy to automate. We refer to this process as "monolithic module assembly" since it translates many of the advantages of monolithic module construction of thin-film PV to wafered c-Si PV. Simplifications in the module fabrication have been estimated to reduce the cost of module fabrication by up to 50%, which corresponds to a reduction of around 25% in the total manufacturing cost for the module [28]. To date, we have demonstrated a two-step assembly process where (1) the back-contact cells are soldered to the backsheet and (2) the cells/backsheet are then encapsulated in the module. The demonstration used Kapton™ for the backsheet, the circuit on the backsheet consisted of copper strips that was applied by a proprietary selective plating technique, and the backsheet did not yet include an encapsulation layer.

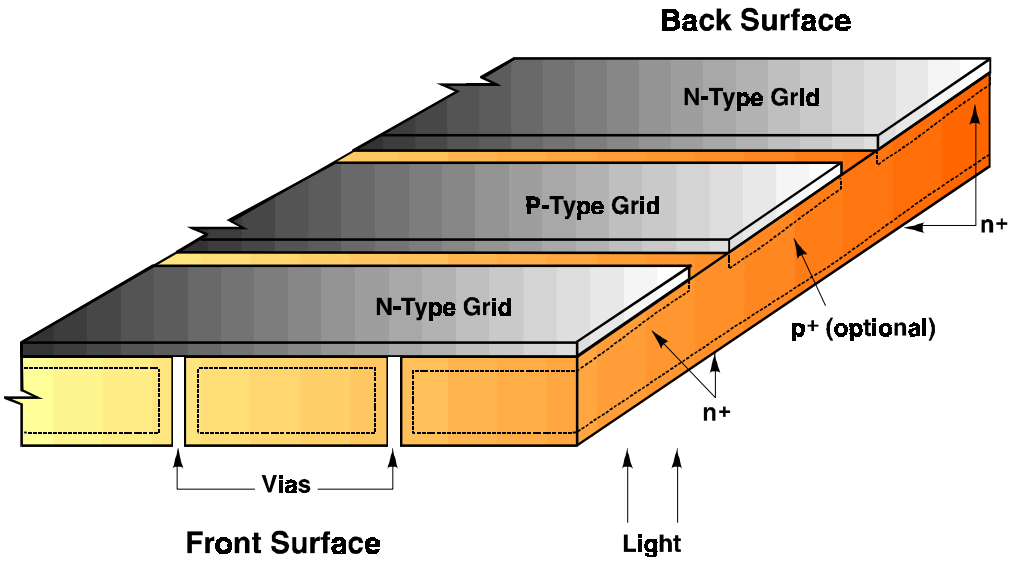

Figure 6. Illustration of an EWT cell.

Fundamental research to improve state-of-the-art device performance and investigate novel process and device concepts is addressed through support of a University Center of Excellence in Photovoltaics (UCEP) at the Georgia Institute of Technology. The work at UCEP is presently developing high-efficiency cells on commercial c-Si substrates, developing cell processes with potentially large throughput (e.g., screen-printed contacts and rapid-thermal processing), and examining advanced back-surface field processes. Some of this work is summarized in recent publications [25,29-31].

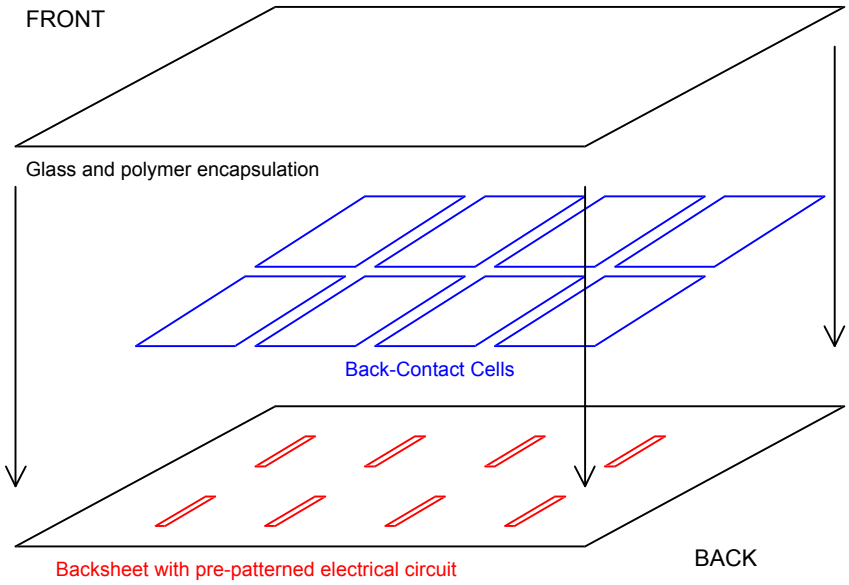

Figure 7. Illustration of monolithic module assembly.

SUMMARY

Crystalline-silicon PV has the capability of meeting major Department of Energy goals for PV technology. This paper has summarized the structure and progress in the SNL/NREL c-Si PV R&D project. The project is divided into three tasks. Significant progress was achieved in all three tasks, including development of LPE growth on metallurgical-grade multicrystalline-silicon substrates, fundamental studies on the effect of Fe impurity in silicon, and development of novel cell and module concepts with the possibility of significant performance and cost improvements.

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