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MIS AND PN JUNCTION SOLAR CELLS ON THIN-FILM POLYCRYSTALLINE SILICON

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ABSTRACT

Theoretically, MIS-type solar cells offer potential advantages over p/n junctions on thin-film polycrystalline silicon substrates. The Photovoltaic Advanced Silicon (PVAS) Branch at the Solar Energy Research Institute (SERI) has initiated a comparative study to assess the potential of these cells for low-cost terrestrial photovoltaic systems in terms of performance, stability, and cost-effectiveness. Several types of MIS and SIS solar cells are included in the matrix study currently underway. This approach compares the results of MIS and p/n junction solar cells on essentially identical thin-film polycrystalline silicon materials. All cell measurements and characterizations are performed using uniform testing procedures developed in the Photovoltaic Measurements and Evaluation (PV M&E) Laboratory at SERI. Some preliminary data on the different cell structures on thin-film epitaxial silicon on metallurgical-grade substrates are presented here.

I. Introduction

Metal-Insulator-Semiconductor (MIS) and Semiconductor-Insulator-Semiconductor (SIS) structured solar cells are considered a viable alternative to p/n junctions for use with thin-film polycrystalline silicon substrates. These cells possess characteristics, such as low-temperature processing and potentially low-cost material and fabrication technology, considered attractived for large-scale production. The MIS and SIS solar cells should have an enhanced short wavelength response because of the absence of a "dead layer" usually present in p/n junctions (1). Thus, the MIS-type cells should perform better than p/n junctions on small grain polycrystalline silicon where the diffusion length is expected to be short. However, the majority of the research on MIS devices to date has been conducted on thick (>250 μm) single crystal or large grain, bulk polycrystalline silicon wafers (e.g., Wacker/Silso) with minimal research on thin-film substrates (2). This paper presents a first-time comparative matrix study of MIS and p/n junction solar cells, fabricated with state-of-the-art technology, on essentially identical thin-film (<100 μm) polycrystalline silicon substrates. Devices are fabricated on adjacent portions of the same substrate whenever possible. The data collected from this continuous study will be used to assess the viability of the MIS/SIS-type solar cells to make a significant contribution to terrestrial photovoltaics. The experimental matrix and typical solar cell characterizations are discussed. Finally, some preliminary experimental data are presented.

II. Experimental Matrix

The assessment of the MIS cell potential for terrestrial photovoltaics requires fabricating substantial solar cells so statistical averages are established. The development of a large data base is required before conclusions can be drawn from this study. Figure 1 indicates the major elements in the comparative study. The polycrystalline silicon materials will be obtained from various PVAS-sponsored programs. The current thin-film materials of interest are epitaxial layers on metallurgical-grade (mg) silicon, silicon-on-ceramic (SOC), and electron or laser beam recrystallized RTR ribbons (3). The substrate materials will be characterized in-house by the PV M&E Laboratory. Substrates will be sorted and characterized in terms of impurities, grain size,. resistivity, and growth technique. Different solar cell devices will be processed on like materials. The PV M&E Laboratory will characterize the devices electrically, optically, and if required, chemically.

Finally, characterization information will be fed back to the device fabrication groups or to the groups preparing silicon substrates. The data generated should guide certain processing sequences and help in the optimization of a given technology. The ultimate goal is to identify the optimal MIS or SIS technology on thin-film or low-cost materials and compare the results with a given low-cost p/n junction processing technology.

III. Substrate Materials

One of the promising approaches to low-cost thin-film polycrystalline silicon is the growth of a

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thin (15-50 μm) epitaxial layer on a large-grain mg-silicon substrate. In this study, mg-silicon substrates were prepared by directional solidification using either the heat exchanger method (HEM) by Crystal Systems or the Czochralski (CZ) technique by Motorola. Detailed discussion of these processes can be found in papers presented by the participating organizations elsewhere in these proceedings and in the literature (4, 5). Typical grain sizes in these substrates vary from several millimeters to greater than one centimeter near the seed end of the ingot. Near the tang end of the ingot, the grain sizes average less than one millimeter. The average resistivity of the mg-silicon wafer varied from 0.07 Ω-cm to 0.04 Ω-cm from the seed to the tang end, respectively. The major impurities, determined by spark source mass spectroscopy analysis (SSMS), in the p-type substrates are Al, Fe, Ni, Ti, Mn, and V. Table I lists the typical impurity concentrations in the mg-silicon substrates. Wafering of the ingots was carried out by conventional ID sawing.

Prior to epitaxial film deposition, about 50 μm of mg-silicon were chemically etched from both sides of the wafers. After etching, the material typically possesses a high density of etch pits and includes particulates assumed to be SiC. The substrates were then polished, cleaned, and dried. High purity silicon films were epitaxially grown on the mg-silicon substrates by chemical vapor deposition (CVD) from the decomposition of dichlorosilane. P-type films of 18-μm, 20-μm, and 36-μm thicknesses have been prepared. The temperature of the substrate during growth is typically 1100°C, and the growth rate is 2-5 μm/min. Table II lists the epitaxial growth procedure performed for SERI by RCA Laboratories. The typical epi-

TABLE I. Typical Major Impurity Concentration (PPMW)* in Metallurgical-Grade Silicon Ingots (Prepared by HEM and CZ Methods)

ELEMENTS	HEM INGOT		CZ INGOT	
	SEED	TANG	SEED	TANG
Cr	0.07	30	0.1	33
P	4	6	0.6	3.7
Mn	-	100	0.1	100
Al	-	200	60	100
Fe	20	700	100	1000
Ni	<1	30	2	33
Ti	10	80	0.15	100
V	<10	50	-	100
B	<10	10	0.4	1-5

* Parts per million; weight percentage

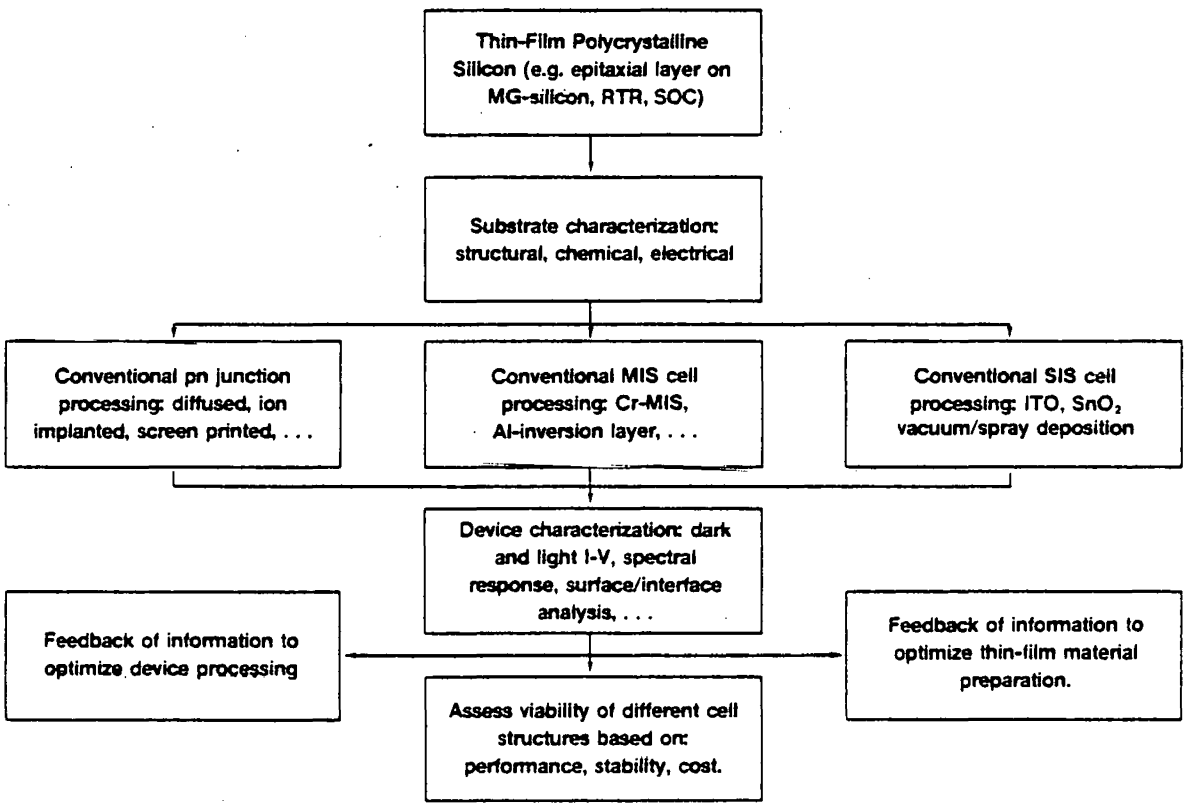

Figure 1. Experimental Matrix for pn Junction Versus MIS/SIS Solar Cell Assessment

TABLE II. CVD Epitaxial Growth Process

1. Substrate chemically etched in HNO_3:HF (6:1), polished, cleaned, and spun dry
2. Reactor flushed with H_2 (30 ℓ/min for 10 min)
3. Substrate heated to 1150°C with H_2 flowing for 5 min
4. ~5 μm etched from substrate in 1% HCL for 5 min at 1150°C
5. Reactor flushed with H_2
6. Substrate temperature adjusted to 1100°C
7. Gases introduced (SiH_2Cl_2, AsH_3 or B_2H_6) for desired growth rate, doping level, and conductivity
8. Reactor flushed with H_2 for 3 min then power turned off.

taxial film structure is shown in Figure 2. The purpose of the graded layer is to provide a Back Surface Field (BSF) effect on the solar cell. When very small grains in the mg-substrate exist, the resulting epitaxial films do not show improvement in substrate crystal quality. The grain boundaries present in the substrate propagate into the epitaxial layer. Also, some impurities in the mg-silicon substrate diffuse into the epitaxial layer as determined from SSMS analysis. For control purposes, several heavily doped single crystal silicon wafers have also been processed with the mg-silicon substrates. After epitaxial growth, the wafers were halved. One half of each wafer was fabricated into a p/n junction solar cell; the other half was used for MIS junction fabrication.

IV. Cell Structures

Three types of solar cell structures are presently being investigated. Solar cell performance using these structures has been optimized on single crystal and bulk polycrystalline silicon substrates. The first device is the majority carrier Cr-MIS cell (6). The general procedures include:

- Wafers are etched in 75% HNO_3, 17% CH_3OOH, and 8% HF;
- Wafers are degreased, rinsed in D.I. H_2O, and then the thin native oxide is removed in HF, rinsed in D.I. H_2O, and blown dry with N_2;
- 0.5 μm aluminum is evaporated for back side contact;
- Aluminum is sintered at 580°C for 30 min in air to form an ohmic contact and a thin ~20-25 Å oxide interface; and
- 30 Å chromium, 50 Å copper, 0.5 μm aluminum grid, and a 700 Å SiO AR coating, are resistively evaporated in a single pumpdown.

Further refinement of the procedure will probably be required on the thin-film epitaxial polycrystalline silicon materials.

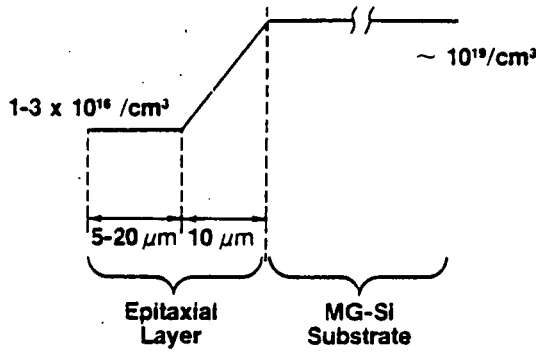

Figure 2. A Typical Epitaxial Layer Structure

The second type of structure being studied is the conventional p/n junction formed by thermal diffusion (7). The procedure typically includes:

- Characterize epitaxial layers;
- Clean wafers in H_2SO_4 : H_2O_2; H_2O_2: NH_3OH; H_2O_2 : HCL boiling solutions;
- Diffuse $POCl_3$ at 875°C for 30 min followed by a slow pull (10 min); Sheet resistance and junction depth are typically 75 Ω/□ and 0.3 μm, respectively;
- Contact with evaporated Ti/Ag on front side (0.2 μm) and on back side (5.0 μm);
- Spin-on TiO_2 AR coating, bake, and sinter; and
- Etch mesas to delineate cell area.

This procedure is not considered very low cost due to the silver metallization and special mesa etching. However, since this processing has resulted in high efficiency cells on single crystal silicon, the structure should give a reasonable indication of the potential performance from the epitaxial material.

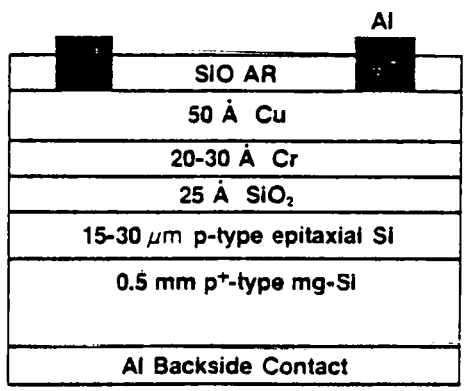

Figure 3A. Cr-MIS Solar Cell

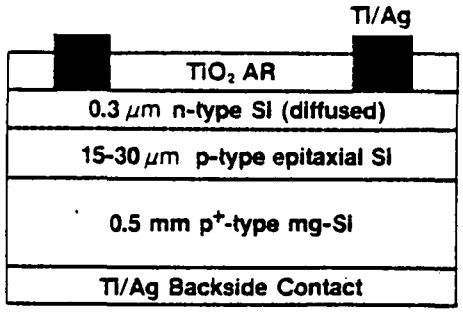

Figure 3B. pn Junction Solar Cell

The third type of solar cell structure is a screen-printed device that includes a screen-printed phosphorous diffusion source and metal contacts (8). Typical procedures in this process include:

- Clean wafers in HNO_3, D.I. H_2O, HF, and acetone vapor;
- Screen print phosphorous doped layer;
- Fire in belt furnace at 910°C for 15 min in N_2 atmosphere;
- Etch back side parasitic junction;
- Spin-on TiO_2 AR coating;
- Screen print front side silver contacts, and fire through AR coating; and
- Screen print aluminum paste on back side and fire at 660°C.

This processing technique is considered potentially low cost and is very amenable to automation since the screen printing and diffusion are continuous processes. Using the above technology, yields exceed 85% for cells of greater than 10.5% efficiency on batches of 250 single crystal wafers (8).

Each of these cell structures is detailed in Figure 3. In future research, the processing for the three cell types will be optimized on the thin-film polycrystalline silicon substrates. Other device structures (e.g., SIS type) will also be considered.

V. Characterization and Preliminary Data

The PV M&E Laboratory at SERI is performing all the measurements and characterizations used in this study. All measurements are performed according to the established laboratory procedures. The goal of the characterization effort is to identify the critical parameters affecting the performance of solar cells on thin-film polycrystalline silicon materials. A solar cell data base is currently being developed that allows analysis of statistical variations in measured data. The data base provides an easy system to track changes in cell performance while feeding back information to the cell and material suppliers.

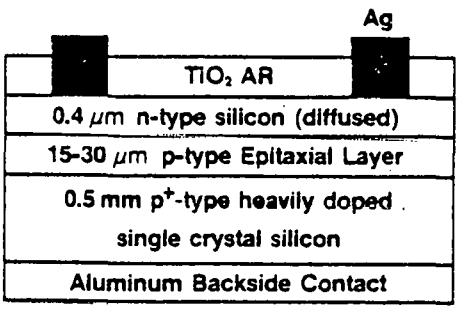

Figure 3C. Screen Printed pn Junction Solar Cell

Standard characterizations in this side-by-side comparison will be used to identify losses due to junction interfaces, shunt and series resistance, epitaxial layer doping, epitaxial layer diffusion length, and the effect of impurities from the base material or processing technology, such as contaminated silver inks used in the screen printing process. Also, the metallization and distributed series resistance losses will be investigated on selected samples. The typical characterizations will include dark and light I-V analysis, C-V and G-V analysis, spectral response, sheet resistance, optical analysis, photoresponse mapping and electron probe microanalysis for chemical and structural information. In certain cases, when anomalies in the device performance are observed, special analysis can be performed to identify the relevant basic mechanisms. Measurements to study the chemical and electronic properties of the thin oxide interfacial regions, fundamental transport mechanisms, and impurity analysis at grain boundaries will be on-line in a few months. These analytical techniques include XRD, XRF, SIMS, ion probe, infrared spectroscopy, DLTS, and x-ray crystallography.

To date, three types of substrates have been used for epitaxial growth. These include HEM and CZ mg-silicon and heavily doped CZ single crystal material. The photovoltaic data on the few cells presently available are listed in Tables III, IV, and V. Adjacent entries in the tables represent either adjacent substrates from the ingot or the same substrate cut in half. Because of the wide variations in cell parameters observed when using low-cost materials and with MIS type devices, it is impossible to draw any conclusions from such a limited data base. For a simple comparison, the photovoltaic data from the best Cr-MIS and p/n junction cells, which incidentally were obtained on

TABLE III. Comparison of Photovoltaic Data for Cells on Motorola's CZ/MG Silicon Substrates

Wafer Number	Material	Epitaxial Layer Thickness	Cell Type	J_{sc}	V_{oc}	ff	η	Area
991	Seed End.	18μm	pn	16.09	557	73.3	6.58*	4.52
260	Large Grain		Cr-MIS	15.49	505	70.5	5.52	2.12
993	Seed End.	36 μm	pn	16.89	550	71.5	6.64	4.52
264	Large Grain		Cr-MIS	15.92	509	69.1	5.61	2.12
996	Tang End.	18 μm	pn	15.30	474	49.4	3.59	4.50
261	Small Grain		Cr-MIS	15.49	483	41.8	3.12	2.12
997	Tang End.	36 μm	pn	14.76	503	68.5	5.10	4.58
—	Small Grain		Cr-MIS	—	—	—	—	—

*The pn junction cells do not have an AR coating.

the same wafer, are included in Figures 4 and 5. The p/n junction device, which has the better cell characteristics, does not have an anti-reflection coating.

TABLE IV. Comparison of Photovoltaic Data for Cells on Crystal Systems' HEM/MG Silicon Substrates*

	Wafer Number	Material	Epitaxial Layer Thickness	Cell Type	J_{sc}	V_{oc}	ff	n	Area
3 Top	750A	Unseeded,	20 µm	pn	21.75	534	42.2	4.90	2.40
	259	Small Grain		Cr-MIS	14.16	379	60.3	3.25	2.12
3 Bottom	750B	Unseeded,	20 µm	pn	20.89	540	66.2	7.47	2.41
	250-E	Small Grain		Cr-MIS	(14.20	500	76.0	5.40	2.12)
5 Top	749A	Seeded,	20 µm	pn	22.20	574	78.6	10.01	2.45
	251	Large Grain		Cr-MIS	13.46	479	67.9	4.39	
5 Bottom	749B	Seeded,	20 µm	pn	21.69	572	77.2	9.59	2.43
	257-E	Large Grain		Cr-MIS	(12.70	480	34.0	2.10	2.12)

*Data in parentheses not measured by PV M&E Laboratory at SERI

TABLE V. Comparison of Photovoltaic Data for Cells on Heavily Doped (10^{19}) Single Crystal Silicon

Wafer Number	Material	Epitaxial Layer Thickness	Cell Type	J_{sc}	V_{oc}	ff	n	Area
#16 E1	Heavy Doped	20 µm	pn*	22.45	544	59.1	7.24	3.24
#27 287	Single Crystal		Cr-MIS	20.14	542	74.1	8.09	2.12
#16 E2	Heavy Doped	20 µm	pn	21.97	549	61.3	7.40	3.24
#22 292	Single Crystal		Cr-MIS	17.96	541	73.3	7.17	2.12

*These pn junctions were fabricated using a total screen printing process.

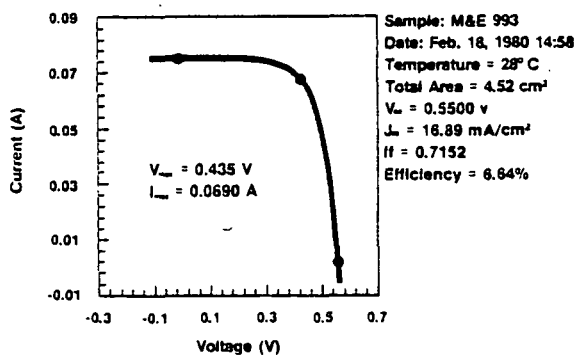

Figure 4. Best Solar Cell Efficiency for pn Junctions Without AR Coating

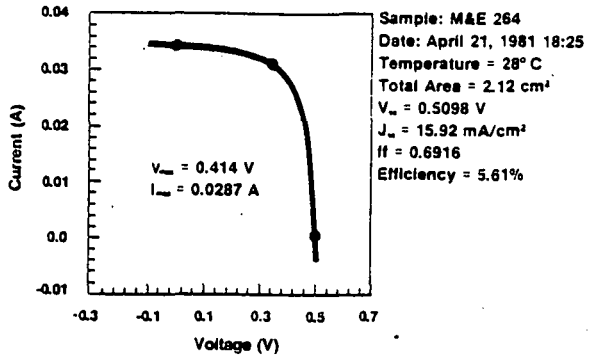

Figure 5. Best Efficiency for Cr-MIS Solar Cell With AR Coating

VI. Conclusion

A program has been established to assess the viability of MIS/SIS-type solar cells in comparison to p/n junction technology on thin-film polycrystalline silicon substrates. The program should be completed in about one year. At that time, the results from numerous side-by-side cell comparisons will be assembled, and the resulting data base will be used to guide future program directions in the area of polycrystalline silicon solar cells. Acknowledgement: Diane Schilly for technical assistance.

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