NREL/TP-411-20143 • UC Category: 1280 • DE96000477

Silicon-Film™ Photovoltaic Manufacturing Technology

Annual Subcontract Report
1 January 1994 – 31 December 1994

S. R. Collins, R. B. Hall, J. A. Rand
AstroPower
Newark, Delaware

NREL technical monitor: R. Mitchell

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

Prepared under Subcontract No. ZM-2-11040-5

November 1995

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (615) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 487-4650

Printed on paper containing at least 50% wastepaper, including 10% postconsumer waste

Table of Contents

List of Figures

List of Tables

Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project is to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate module. This process starts with the production of continuous sheets of thin-film, polycrystalline silicon using the Silicon-Film™ process. Our main product focus in PVMaT-2A has been a 240 cm^2 solar cell. Continuous sheets of silicon are produced and cut into wafers that are 15.5 cm on a side. Both standard modules (36 solar cells) and a new 56 solar cell module were produced. The targeted high power module design is a 170 watt module, used in a twelve module array to generate 2 kW. The solar cells, modules, and array developed here are described in Table 1.

Table 1. Silicon-Film™ Large Area PVMaT Product Goals

Solar Cell Size	240	cm^2
Solar Cell Power	3.15	watts
Module Size	1.4	m^2
Module Power	170	watts
Array Power	2041	watts

Development of a Silicon-Film™ manufacturing technology requires the successful achievement of the following three objectives leading to the milestones listed in Table 2:

1. Design, construction, and demonstration of a **Silicon-Film™ wafer machine and process** capable of manufacturing wafers that are 240 cm^2 in size at a rate of 3.0 MW/yr.
2. Development of an advanced **solar cell manufacturing** process that is capable of turning the Silicon-Film™ wafer into a 3.15 watt, 15.5 cm x 15.5 cm solar cell.
3. Development of an **advanced module design** based on these large area silicon solar cells with an average power of 170 watts for 56 solar cells and 113 watts for 36 solar cells.

Table 2. Specific PVMaT Milestones for Phase I through Phase III

	Phase I	Phase II	Phase III
Wafer Machine			
Production Rate	400 kW/yr	1.3 MW/yr	3.0 MW/yr
Material Use Efficiency	75%	85%	90%
Solar Cell Size*	a) 10 cm x 10 cm b) 15 cm x 15 cm	b) 15 cm x 15 cm	b) 15 cm x 15 cm
Solar Cell Power	a) 1.1 W	b) 2.5 W	b) 3.15 W
Module Power	--------	b) 84 W†	b) 98 W† 170 W‡

* Product designation is a) AP-100, b) AP-225
† 36 cell module
‡ 56 cell module

PVMaT Project Guidelines and Tasks

This project relies on the parallel development of three technologies: (i) a growth technique that produces high quality, polycrystalline silicon sheets at high generation rates, (ii) a solar cell fabrication technique that captures the material's potential while qualifying as low cost manufacturing, and (iii) a module fabrication process that efficiently integrates the solar cells into a utility-scale power source. Accordingly, project results are presented in three sections which discuss basic development: (i) The Silicon-Film™ Sheet Fabrication Process, (ii) Solar Cell Fabrication, and (iii) Module Assembly. The 23 individual tasks comprising this project are provided in Table 3 below and are identified in the text of the results sections by number only.

Table 3. List of PVMaT-2A Tasks		
Task	**Year**	**Task Title**
1	1	Wafer Performance Benchmarks
2	1	Wafer Process Improvement
3	1	Statistical Process Control
4	1	Solar Cell Efficiency Improvements
5	1	Device Equipment/Process Automation
6	1	Waste Impact/Cost Minimization
7	1	Advanced Module and Panel Design
8	2	Wafer Process Improvement
9	2	Wafer Process Boundary Conditions
10	2	Wafer Machine Building Block Design
11	2	Statistical Process Control
12	2	Solar Cell Efficiency Improvements
13	2	Materials Costs Reduction
14	2	Device Equipment/Process Automation
15	2	Advanced Panel Design
16	2	Module Equipment/Process Automation
17	3	Wafer Process Improvement
18	3	Wafer Machine Building Block Design
19	3	Statistical Process Control
20	3	Solar Cell Fabrication
21	3	Materials Cost Reduction
22	3	Device Equipment/Process Automation
23	3	Module Equipment/Process Automation

Silicon-Film™ Methodology

The Silicon-Film™ Process is a method for fabricating silicon wafers by the production of continuous sheets of thin-film silicon on a low cost substrate which are then cut to size. Because these sheets are produced at the desired thickness, ingot sawing and associated mounting and cleaning steps are eliminated resulting in a significant reduction in cost. In developing a low cost process, the focus is on limiting the consumption of high quality silicon, reducing sawing steps, and utilizing a high yield continuous manufacturing technology. For the Silicon-Film™ Process, silicon cost is determined by the material quality, silicon thickness, wafer breakage, and kerf loss during sawing. The continuous manufacturing process produces volume that will reduce the per wafer cost of capital equipment and labor while improving process control.

Key Results

Wafer Machine Performance Benchmarks

The Silicon-Film™ machine and process development was based on the following objectives:

1. continuous-mode machine for high throughput potential.
2. high areal generation rate capable of producing
3. high quality material at a production capacity of 3.0 MW/yr.
4. reliable machine components for high yield and continual operation.

During the three years of this effort, the Silicon-Film™ process progressed from the initial batch-mode version to the final continuous-mode process with a corresponding 1650% increase in areal generation rate. Developments took a stair-like pattern with advances in areal generation rate followed by advances in material quality leading up an increasing production capacity curve. In parallel, cost reduction features and manufacturing attributes were under continual development.

Production capacity of the sheet production process for a single machine reached 4.5 MW/yr (based on an NREL confirmed 2.9 watt, 240 cm^2 solar cell cut from representative material). Material uniformity and larger area potential of this process was demonstrated by a 7.9 watt, 676 cm^2 solar cell which has a comparable power density to its 240 cm^2 counterpart.

In the third year, the machine development effort focused on manufacturing capabilities in addition to material quality, specifically, machine yield, reliability, and material use efficiency. By performing 14 to 32 hour production runs, we were able to identify component failure modes which only occurred under extended operation. Component design was then modified to eliminate the identified failure modes so that they would not re-occur. Overall yield reached 73% for 16 hour runs, demonstrating a 62% improvement over a 10 month effort.

Solar Cell Efficiency Achievements

Solar cell fabrication processes were developed along two parallel paths: (i) a baseline production process, and (ii) a laboratory advanced cell process. The objective of the baseline process was to establish the lowest cost process capable of producing large solar cell lots with an average power of 2.5 watts or better. The objective of the advanced process was to capture the full potential of state-of-the-art material resulting in a 3.15 watt solar cell.

Baseline process efforts focused on a reduced cost surface preparation process, a gettering diffusion, reduced grid shading, improved contact firing procedures, and increasing performance and throughput of the anti-reflection coating deposition process. The best baseline cell was 2.47 watt (including a 6.5% encapsulation gain) with an area of 240 cm^2. The 2.5 watt average baseline goal will be achieved by fabrication technology improvements in emitter formation (blue response) and AR coating (surface reflection).

Advanced processing efforts focused on improving device performance through enhancement processes such as improved gettering, surface passivation, and hydrogenation (RF plasma and

ion-implanted hydrogen). Although significant gains have been achieved using these processes, further gains are attainable through developments in post-growth processing. At the end of the program, the best solar cell fabricated was measured at 2.9 W at NREL. Efforts to improve both as-grown material quality and post-growth processing will continue. We believe progress will be streamlined if post-growth processing technologies are developed on 1 cm^2 substrates and later transferred to a uniform 240 cm^2 substrate.

Module Assembly Achievements

Efforts in module line assembly have focused on measuring the performance of AP-225 solar cells in 36 cell modules, investigating the potential for wider modules (over 100 cm wide), and investigating automation of module assembly steps. Automated tabbing and stringing of front and back contacts was investigated resulting in identification of the preferred technology and preliminary specifications for a specialized machine using high intensity light soldering. A lay-up table was designed, fabricated, and demonstrated for transferring 36 cell matrix strings for lay-up. The best modules measured by NREL were a 93 watt, 36 cell module with a total area of 0.95 m^2, and a 148 watt, 56 cell module with a total area of 1.44 m^2.

The Silicon-Film™ Sheet Process

(Tasks 1, 2, 8-11, 17- 19)

Process Description

A setter transports the raw materials through the active layer growth process. The setters are transported in a manner that permits the continuous application of the raw materials and the continuous growth of the active layer; there is only one beginning and one end of the sheet as established by the beginning and the end of the production run. The sheet is cut to the desired length as it exits the machine.

The growth of the active layer is accomplished in a system purged with an inert gas to reduce the effects of oxidation. The linear sheet speed, gaseous ambient, and the axial and transverse thermal profiles of the machine are fundamental parameters that are critical to achieving the desired sheet properties.

Development Goals

Key in the development of the Silicon-Film™ machine and process were clearly defined goals which guided development. These goals were:

1. **High throughput:** material will be grown at a rate capable of 3.0 MW/yr production.
2. **High quality:** the active silicon layer will have an as-grown diffusion length of 40 micrometers.
3. **Manufacturability:** low cost features will be built into the process
   - the machine components will be designed for high reliability to attain high product yields under continual operation
   - material use efficiency (MUE) will reach 90%.

There are four key performance factors in Silicon-Film™ machine and process development which are used to quantify developmental progress:

1. material rate (throughput),
2. material quality,
3. material use efficiency, and
4. machine reliability.

The following subsections describe the origin of and the achievements made in each of the above machine performance factors.

Machine Rate
(Tasks 1, 2, 8, 9, 10, 17, 18)

Silicon-Film Machine Rate Calculation

The final machine rate goal for this effort was to demonstrate a sheet generation rate capable of producing 3.0 MW/year. Figure 1 illustrates the geometry for a Silicon-Film™ sheet on the setter. Production rate is the product of the following set of factors: the areal generation rate, M_r, in m^2/hr, the number of operating hours per year, N_o, and the solar cell efficiency, Eff.

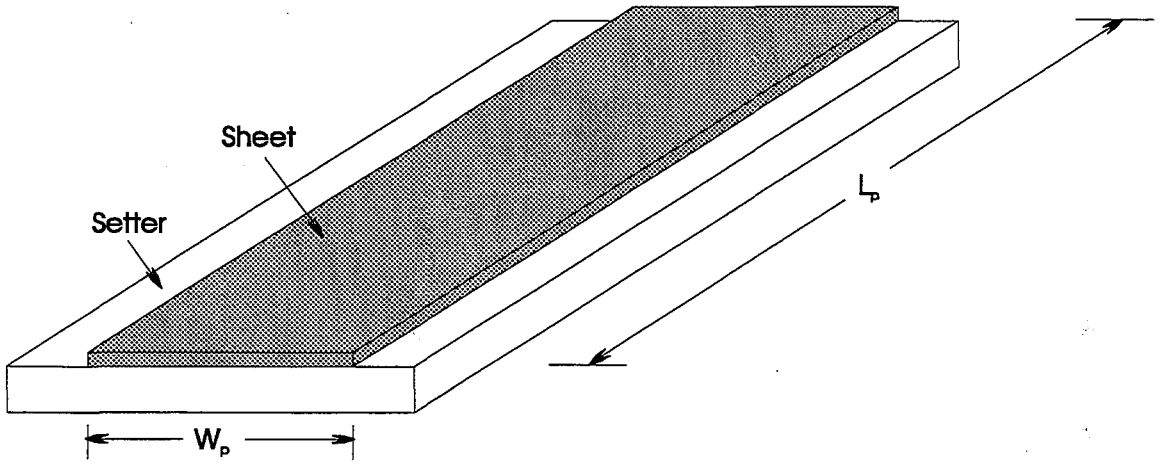


Figure 1. Silicon-Film™ sheet geometry

The equation for the definition of the production rate is:

$$PR = G_r * N_o * Eff * 10^{-5},$$

where

PR	=	production rate, MW/year
G_r	=	sheet generation rate m^2/hr
N_o	=	number of production hours per year
Eff	=	resultant solar cell efficiency, %.

Silicon-Film Machine Rate Achievements

Given the highest efficiency measured by NREL on a solar cell fabricated from representative material, 8000 production hours per year (based on continuous operation of the machine), and the current baseline sheet generation rate (G_r), we calculate that our current machine is capable of a production rate of 4.5 MW/yr. The sheet generation rate is based on finished wafer area generated per hour as shown in Figure 7.

Figure 2 shows the progress in production capacity during the PVMaT program. During the first year of the program, the Silicon-Film™ machine was a batch-mode version with a maximum production capacity of 0.48 MW/yr for 100 cm^2 solar cells. After one year of development a continuous mode machine had been designed, built, and demonstrated a production capacity of 1.7 MW/yr for 240 cm^2 solar cells. After one year of optimization, a production capacity 4.5 MW/yr for 240 cm^2 solar cells was demonstrated using one prototype machine. This represents a 837% increase in capacity over the course of three years. Deliverable goals and achieved results are both represented.

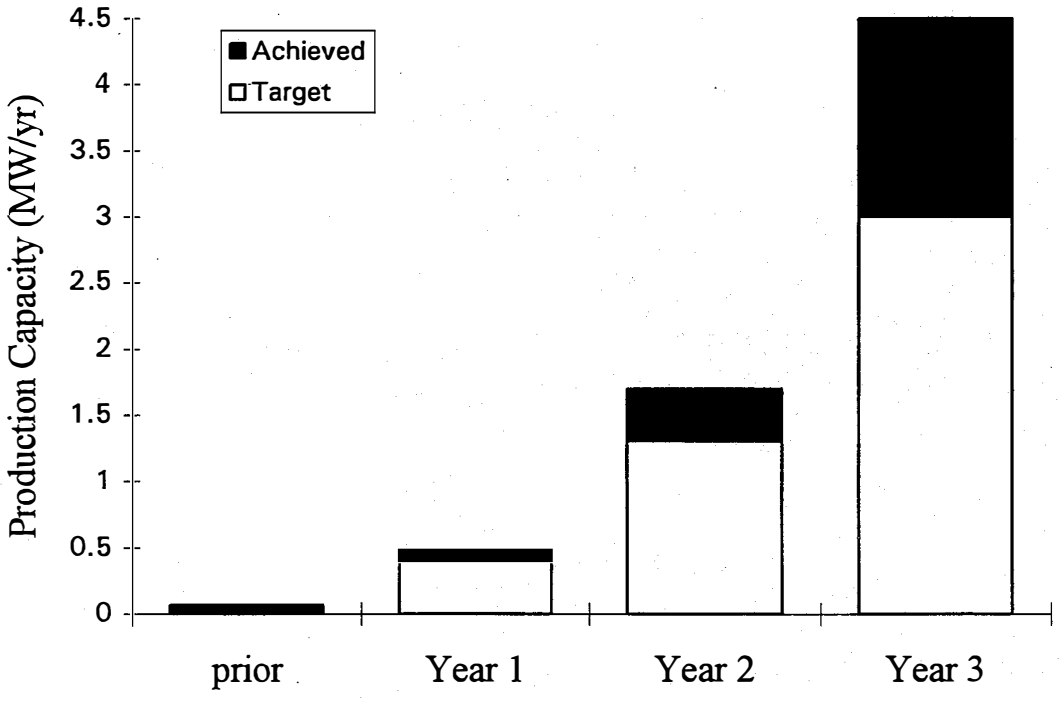


Figure 2. Progress in production capacity throughout the PVMaT program.

Material Quality
(Tasks 1, 2, 7, 8, 9, 10, 17, 18)

Not only is it important that the process produce wafers at high throughput, it is also important that the process generate high quality material. The most important electrical parameter determining the level of quality of the Silicon-Film™ active layer is minority carrier diffusion length. Both the magnitude and spatial uniformity of the minority carrier diffusion length are important in establishing the utility of the material. This section describes the level of solar cell performance potential of the material (illustrated by modeling), how material was characterized throughout the development effort, the level and uniformity of material quality (measured as diffusion length) achieved to date, and possible causes that limit the performance in the present material.

Expected Performance

Figure 3 summarizes the predicted power from the 15.5 cm x 15.5 cm Silicon-Film™ solar cell as a function of diffusion length and solar cell design. The "baseline process" refers to the production process including screen-printed contacts and automated spray antireflection coatings. The advanced process refers to a process designed to harness the full potential of the material; it incorporates evaporated contacts, some surface passivation, and bulk passivation. Both processes are described in detail in Tables 7 and 10. Modeling of the best advanced process solar cell measured to date revealed potential for improved performance from further surface and bulk passivation, improvement in emitter doping profile, and a reduction in contact resistance. These post-growth process improvements are shown as the "future process" in Figure 3.

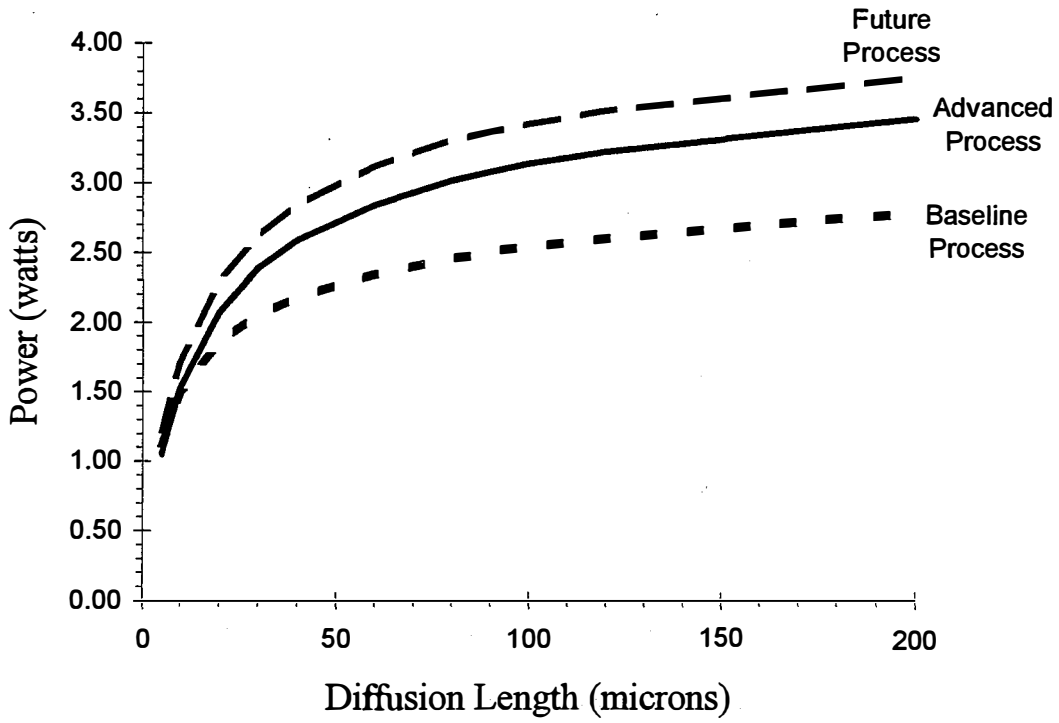


Figure 3. Predicted solar cell power as a function of Ln and fabrication process.

Material Quality Characterization

The main characterization tool used during this effort was the small area mesa test device. These devices were fabricated using a process similar to the baseline fabrication sequence used in making large area cells. The processing sequence is provided in Table 4. The quick turnaround mesa device was used to: (i) correlate changes in machine parameters with material quality, (ii) evaluate uniformity of material, and (iii) determine which material lots should be processed into large area solar cells.

Table 4. Processing Sequence Used for Fabrication of Mesa Test Devices

Surface preparation - *sandblast* - *NaOH etch* - *$HCl:H_2O$ etch* - *$HF:H_2O$ clean*
Diffusion - *$POCl_3$ source*
HF: H_2O etch
Aluminum paste back contact
Device isolation by dicing
Test

Mesas were fabricated edge to edge across a 15.5 cm width of a Silicon-Film™. No process enhancements such as gettering, front contacts, anti-reflection coating, surface passivation, or hydrogenation were used. Each device had an area of 0.2 cm^2. Testing included Jsc, Voc, and Ln measurements (from quantum efficiency measurements). Additional characterization included quantum efficiency spectra, EBIC (electron beam induced current) imaging, LBIC (laser beam induced current) imaging, dark I-V measurements, and capacitance-voltage measurements for estimations of base carrier concentration.

Material Uniformity

Comparing mesa performance across the Silicon-Film™ sheet width provides important information on material quality uniformity. Figure 4 illustrates the uniformity of diffusion length across the Silicon-Film™ sheet on samples from Phase II (Run 746) and Phase III (Runs 000 and 001). As shown, the magnitude of diffusion length has improved significantly while further work is required to improve uniformity.

EBIC images of mesas were used to view grain size uniformity and identify near-surface (to a depth of about 6 micrometers) defect density. Figure 5 is an EBIC image of a mesa device fabricated from Silicon-Film™ material representative of December 1994 (end-of-contract) technology. As shown, there is a wide variety of grain sizes in the state-of-the-art material; the effect of this variation is discussed in "Possible Causes Limiting Performance".

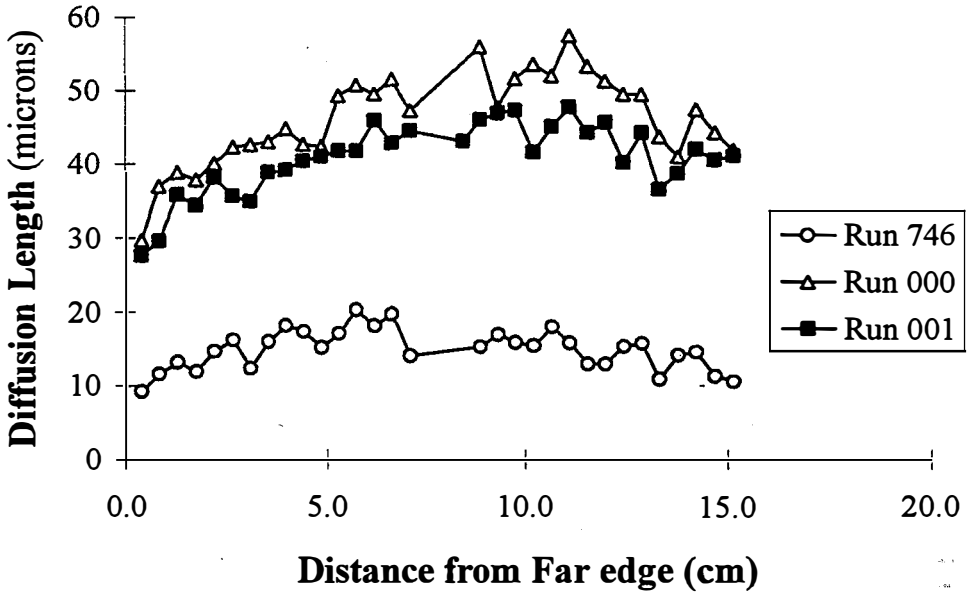


Figure 4. Diffusion length measurements on mesa test devices fabricated across the width of Silicon-Film sheets demonstrating level of spatial uniformity.

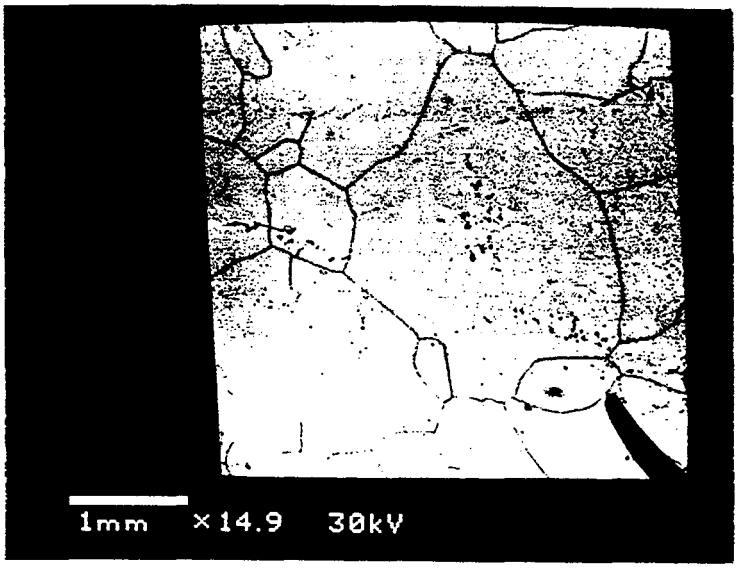


Figure 5. EBIC image of a 0.2 cm^2 mesa device fabricated from Silicon-Film™ material representative of 12/94.

Performance Correlation Between Mesa Test Devices and the AP-225

An example of how mesa performance relates to AP-225 large area (240 cm^2) device performance (before AR coating) is shown in Figure 6. The higher power density of the AP-225 solar cells over the mesa test devices is due to differences in processing including the absence of gettering and antireflection coatings for the test devices.

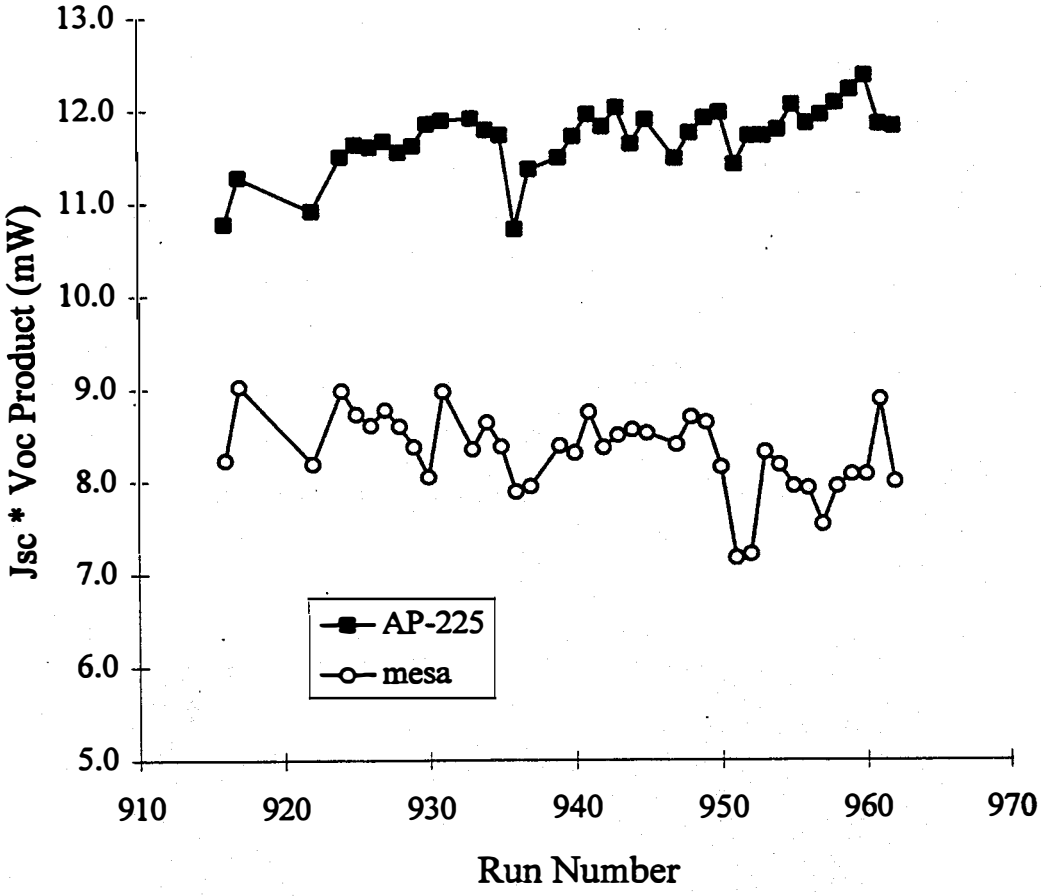


Figure 6. Correlation between AP-225 solar cell Jsc*Voc product and mesa test device Jsc*Voc product

Material Use Efficiency
(Tasks 1, 2, 7, 8, 9, 10, 17, 18)

Material Use Efficiency Calculation

The material use efficiency indicates the amount of silicon which ends up in the finished wafer compared to the amount of silicon introduced at the beginning of the wafer formation process. The material use efficiency depends on the details of the wafer formation process and can be

resolved into the product of three factors: the applicator yield, Y_a, the edge trimming and kerf yield, Y_g, and the wafer visual and mechanical yield, Y_{VM}.

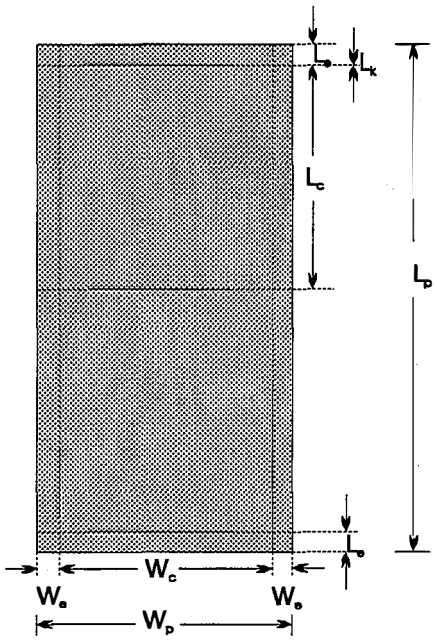
The equation which defines the material use efficiency is

$$MUE = Y_a * Y_g * Y_{VM},$$

where

MUE	=	material use efficiency
Y_a,	=	application yield
Y_g,	=	geometric yield
Y_{VM},	=	visual and mechanical yield.

Figure 7 shows the geometric considerations for determining the finished wafer area and corresponding geometric yield (Y_g).



L_p	=	length of sheet
W_p	=	width of sheet
N	=	number of wafers possible from sheet
L_e	=	edge length
W_e	=	edge width
L_k	=	saw kerf
L_c	=	length of cell
W_c	=	width of cell

$$Yg = \frac{N*W_c*L_c}{L_p*W_p}$$

Figure 7. Definition of dimensions for calculating finished wafer area

Statistical Process Control
(Tasks 3, 11, 19)

An effective SPC system requires: (i) a parameter representing the unit produced that can be easily quantified and which will provide a measure of the quality of that unit, and (ii) a process to which statistical methods can be applied. There are many critical parameters representing the AP-225 wafer and solar cell which could be used to measure the quality of the unit: wafer weight,

performance parameters such as Jsc or Voc, and yield numbers such as geometric yield or visual and mechanical yield. During Phase III, multiple, nearly-identical production runs were performed consecutively which provided a statistical base sufficient for SPC; this was a trial production effort.

MINITAB for Windows® statistical software was used to monitor the quality and consistency of production solar cell performance parameters. As shown in Figure 8, early in the production effort, the fill factor of the AP-225 was very inconsistent and often unacceptably low.

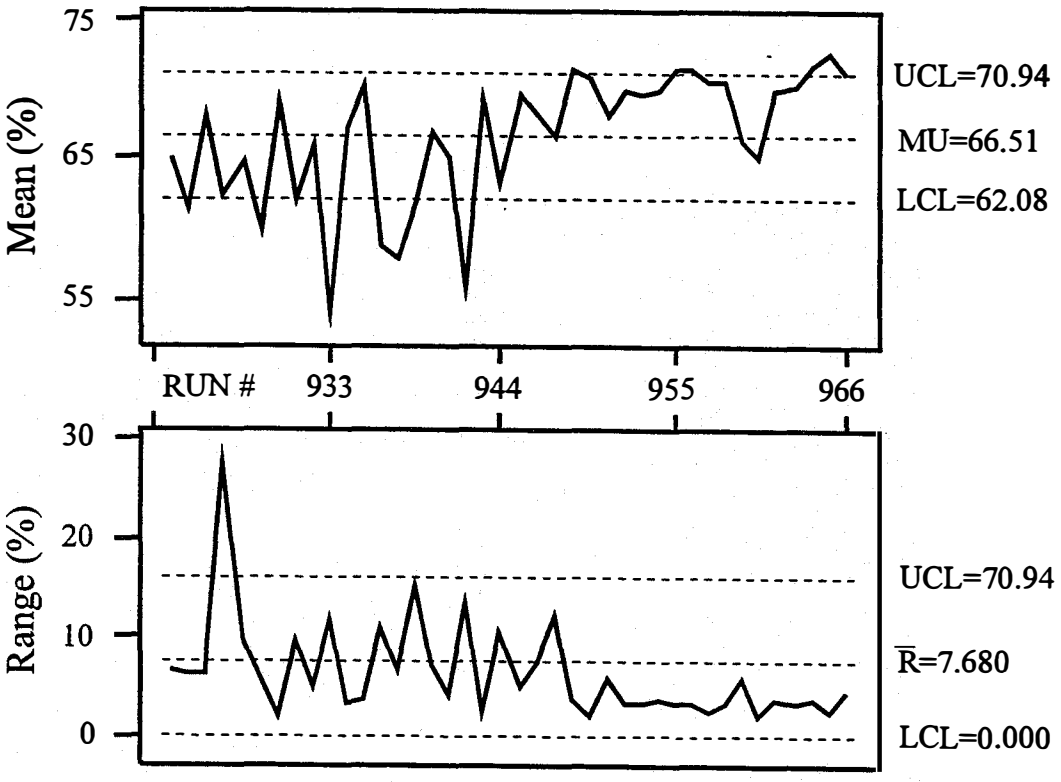


Figure 8. $\overline{X}$-R chart for fill factor of AP-225s during a trial production effort.

It was found that contact firing temperature, which is based on wafer weight, has a dramatic effect on fill-factor; therefore, wafer weight was an important parameter significantly affecting solar cell performance. Every wafer was weighed, sorted, and fired according to weight. As shown in Figure 8, fill factor improved in magnitude and consistency due to these efforts; both tighter control on wafer weight (Figure 9) and optimization of firing temperatures were responsible for the improvement in fill factor. Once the wafer production process is optimized, the spread of weights will become even tighter allowing a single firing temperature.

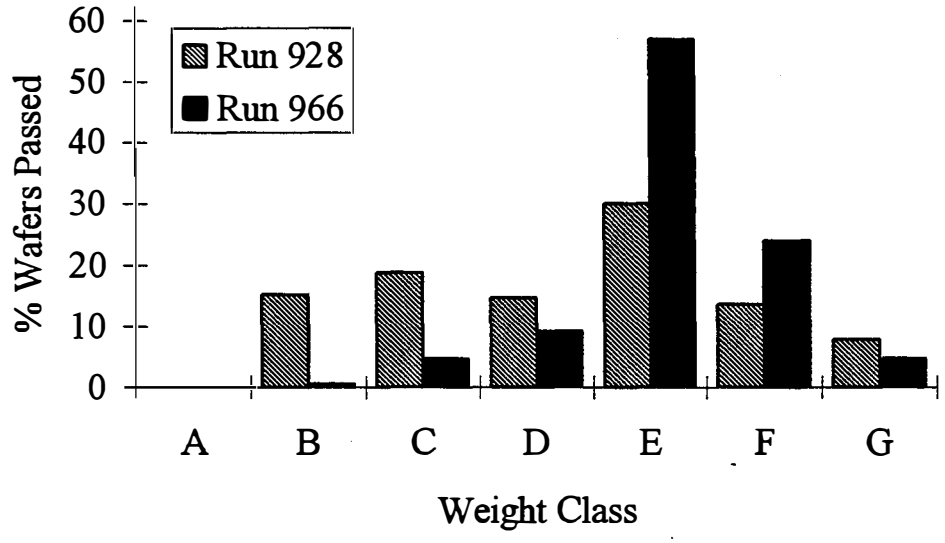


Figure 9. Progress in wafer weight spread from two representative production runs, 928 and 966.

$\overline{X}$-R charts of AP-225 solar cell power (Figure 10) prepared during SPC of Silicon-Film™ were used as an indicator of the manufacturing process rather than an indicator of material quality. Processing parameters such as contact firing temperature have significant impact on fill factor and therefore power measurements for the AP-225 solar cell. This impact therefore reduces the effectiveness of power as an indicator of material quality.

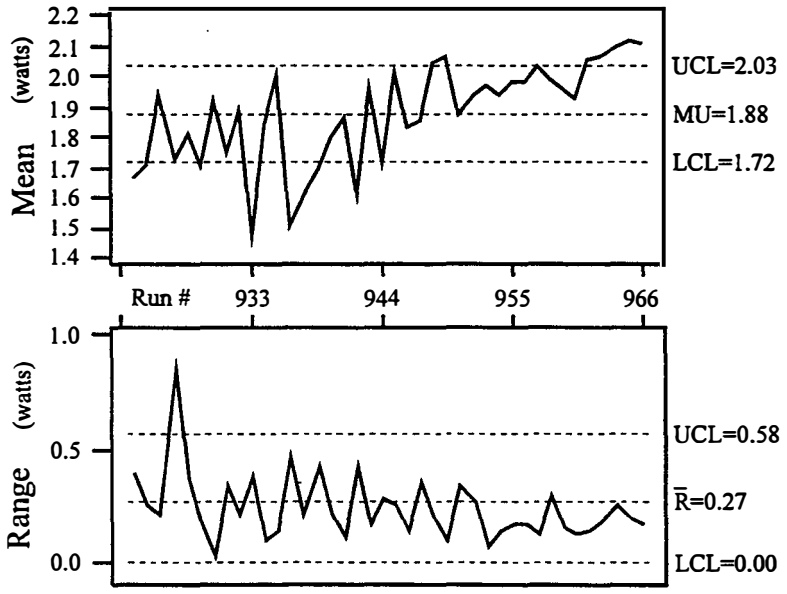


Figure 10. $\overline{X}$-R chart for power of AP-225s during a trial production effort.

Other Attributes Monitored
(Task 3, 11, 19)

SPC was used to monitor gross physical attributes of the solar cells during processing. Product specifications were established and wafers from each production run were visually checked for the following:

1. Cracks, chips, holes
2. Front and back surface texture
3. Wafer thickness
4. Size and squareness

Acceptable ranges for each category were established based on allowances of solar cell fabrication processes. Any wafer not within the acceptable range was rejected. By keeping track of the number and type of rejects, actions could be taken to reduce their occurrence. As shown in Table 5, total wafer rejects was reduced from 47.6% to 5.9% over the course of 48 production runs.

Table 5. Reduction in wafer rejects during a trial production effort

Run Number	**Reject Catagory** (# of wafers rejected)				**Total Rejects** (# of wafers)	**% of Total Wafer Count**
	texture	size	thickness	broken		
924	147	42	10	3	202	47.6 %
972	5	1	16	5	27	5.9 %

Solar Cell Fabrication Processes

(Tasks 4-6,12-14, 20-22)

Solar cell fabrication processes have been developed along two parallel paths: (i) a baseline process, and (ii) an advanced process. The objective of baseline process development was to establish the lowest cost process capable of producing solar cells with a lot average of 2.5 watts or better. The objective of the advanced process effort was to capture the full potential of the material with an end-of-effort goal of achieving a 3.15 watt solar cell. In developing the solar cell fabrication technology for Silicon-Film™ wafers, a baseline process was established while investigating advanced processes in parallel. Advanced processes that improved solar cell performance and were manufacturable at a reasonable cost became part of the baseline process; a process that provides a 5% increase in power can impact module cost by no more than 5%.

Current Baseline Process

At the end of the program, the baseline solar cell fabrication process consisted of the steps listed in Table 6. At the end of program, this process was capable of handling 3,000 wafers per day. Areas requiring improvements for higher throughput and device performance were identified and are discussed below.

Table 6. Baseline Solar Cell Fabrication
Process Steps

1) Surface Preparation (Sandblast + NaOH)
2) Gettering Diffusion
3) Etch Gettered Junction
4) Standard Shallow Junction Diffusion
5) Edge Isolation
6) PSG Removal
7) Print/Dry/Fire Back Ag (98%)/ Al (2%) busbars Aluminum paste over back
8) Print/Dry/Fire Front Silver ink grid
9) RF Hydrogenation
10) Spray AR Coating
11) Test

Gettering Diffusion

It was found that a double diffusion process led to better overall performance than a standard single step diffusion. The double diffusion process involves a standard diffusion step (40 ohm/square), followed by etchback (in NaOH) of the diffused surfaces, followed by a second standard diffusion step (40 ohm/square). Early in Phase III, two sets of AP-225 solar cells, all from the same wafer fabrication lot, were fabricated using (i) a single diffusion process, and (ii) a double diffusion process; the rest of the processing was identical for both sets. As shown in Table 7, the median performance of the double diffused cells was higher in Voc, Jsc, FF, and Power. No antireflection coatings were used.

Table 7. Device Performance of 15.5 cm x 15.5 cm Solar Cells Fabricated with Standard versus Double Diffusion Processes (no AR coating)

Diffusion Process	No. of Cells	Average Voc (mV)	Average Jsc (mA/cm^2)	Average FF (%)	Average Power (W)
Single	17	450	16.1	58.2	1.01
Double	17	462	16.6	61.7	1.13
% Improvement	----	2.7 %	3.1 %	6.0 %	11.9 %

It is believed that the improved performance is due to a gettering mechanism. The initial diffusion getters a significant number of impurities to the emitter, which is removed by etching. The second emitter is then formed in material of higher purity.

Grid Shading

During Phase III, the front contacts of our AP-225 solar cells were evaluated in detail. At the end of the program, two representative cells with different front contact processes were evaluated. Table 8 compares the characteristics of these cells.

As shown in Table 8, the screen-printed cell developed during this work had a total shading loss of 8.6 %. The additional shading of the screen-printed contact over the evaporated contact is due to the grid width. Efforts were made to lower total shading of the screen-printed contact by optimizing the screen-print application and drying process to reduce paste spreading. However, results indicate further improvements cannot be made in the screen-print process until the optimal cell thickness is established.

Table 8. Comparison of Two Representative AP-225 Solar Cells with Different Front Contact Processes

Property	Evaporated Contact Cell	Screen-Printed Cell
Metal Resistivity (ohm-cm)	1.6E-6	3.4E-6
Grid Spacing (cm)	0.238	0.323
Metal Line Width (um)	100	200
Metal Line Height (um)	12	12
Number of Bus Bars (#)	2	2
Side Dimension (cm)	15.5	15.5
Bus Width (cm)	0.2	0.2
Tab Thickness (mil)	8	5
Emitter Sheet Rho (ohms/sq)	75-80	35
Device Power (watts)	2.9	2.3
Total Device Area (cm^2)	240	240
Jsc w/Shading (A/cm^2)	0.028	0.0217
Resistive Losses	4.0 %	3.8 %
Shading Loss (grid)	4.1 %	6.0 %
Shading Loss (bus)	2.6 %	2.6 %
Shading Loss (total)	6.7 %	8.6 %

Hydrogenation

RF hydrogenation has been found to reduce the standard deviation of the fill factor on large production lots. Results indicate that poor control of the furnace used to fire the front contacts may be causing variation in contact resistance. It is expected that as both process control and material quality of the Silicon-Film™ sheet improve, the need for hydrogenation will be eliminated. For the near term, hydrogenation will continue until post-hydrogenation gains are considered insignificant.

Anti-Reflection Coating

A machine to automatically spray a TiO_2 anti-reflection coating was built during Phase III. Process parameters were optimized offering uniform AR coating over the 15.5 cm x 15.5 cm solar cells at a throughput of 490 cells per hour. At these parameters, the typical power gain is 37% which is similar to our PECVD anti-reflection coating process. The throughput of the production line PECVD Si_3N_4 anti-reflection coating process is significantly lower offering only 210 cells per hour.

Encapsulation gain was evaluated for the spray AR coating versus the previous standard Si_3N_4 deposited via PECVD. A comparison was performed of reflection spectra for the visible wavelength range of 400 to 700 nm for typical cells with spray TiO_2 AR coating versus cells with Si_3N_4 coating deposited via PECVD. It was found that an encapsulation gain of 2 to 6% is

typical from the spray AR coating, whereas the effect of the Si_3N_4 coating is less reproducible and has a maximum potential gain of less than 2%. Figure 11 shows a comparison of post-encapsulation reflection and illustrates the benefits of the spray AR process over the PECVD Si_3N_4 process.

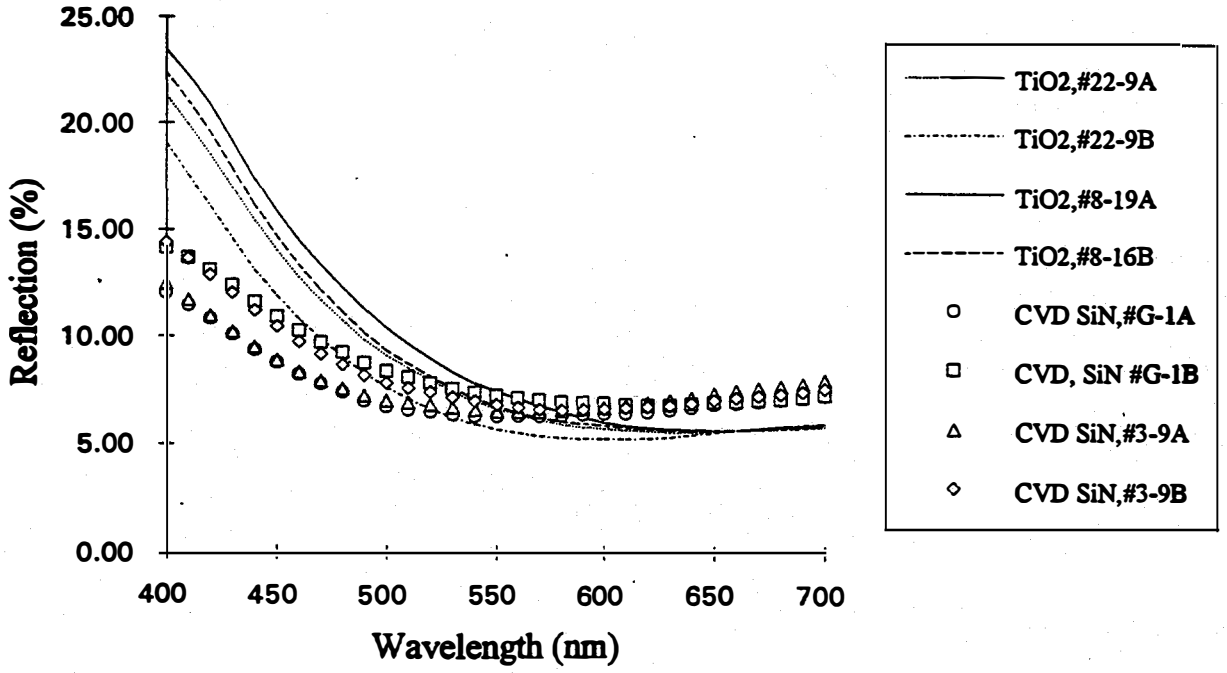


Figure 11. Comparison of post-encapsulation reflection of typical cells with TiO_2 spray AR coating and typical cells with Si_3N_4 PECVD AR coating

In conclusion, we consider the spray AR coating process to have successfully replaced the PECVD Si_3N_4 AR coating process, due to the significantly higher throughput of the process and the consistent power and encapsulation gains of the coating.

Baseline Solar Cell Performance

The best performance of a single cell to date using baseline processing is 2.47 watts. The best median performance of a lot of 466 solar cells was 2.33 watts. These solar cell performance parameters assume a 6.5 % encapsulation gain. We expect that the median baseline solar cell performance will improve to 2.5 watts once we achieve improvements in our emitter doping profile, and surface reflection. Further improvements over 2.5 watt cell medians are expected as a result of improved as-grown material quality reflected by diffusion lengths in excess of 50 micrometers.

Advanced Processes
(Tasks 4, 12, 20)

At the end of Phase III, the advanced solar cell fabrication process consisted of the steps listed in Table 9. The advanced process incorporated a combination of performance enhancement steps designed to capture the full potential of the material. These enhancement steps included specialized gettering, forming gas anneal, hydrogenation, and evaporated contacts which in their initial form were not necessarily practical on a production-scale. Future work will focus on tailoring these advanced processes to realize the performance gains on a production scale.

Table 9. Advanced Cell Fabrication Process Steps

1) Surface preparation (CP etch)
2) Aluminum deposition (0.5 μm)
3) Gettering diffusion
4) Strip junction (CP etch)
5) "Sandia-like" diffusion
6) Forming gas anneal
7) RF hydrogenation
8) Emitter etch back
9) CVD SiO_2 passivation layer
10) Evaporated Contacts
11) CVD SiO_2 and Si_3N_4 AR Coating
12) Test

The **CP etch** surface preparation involves etching the cells in a mixture of HNO_3:HF:CH_3COOH in a ratio of 15:2:5. This provides the smooth surface required by evaporated contact photolithography. The second diffusion step is patterned after the work of Basore [1], and is referred to as the **"Sandia-like" diffusion,** the effect of which is described below. The purpose of the 0.5 micrometer thick **aluminum layer**, step 2, is primarily for aluminum gettering during the high temperature diffusion step.

Gettering

During the Phase III program, the diffusion length of as-grown Silicon-Film™ was measured to be between 25 and 45 micrometers. Phosphorus gettering was investigated to improve this diffusion length. Experiments were performed to determine the optimum process parameters of time, temperature, and $POCl_3/O_2$ ratio. A 1.0 cm^2 laboratory-scale solar cell process was employed to produces devices for quick feedback. Current-voltage characteristics and spectral

response were measured on a total of nine samples for each set of experimental conditions. The minority carrier diffusion length was determined by analyzing the spectral response curve in the range of 750 to 950 nm.

Initially, the temperature was set at 875°C, and the time was set at two hours [2]. Various continuous $POCl_3/O_2$ flow mixtures were then investigated to determine the optimum as determined by maximum improvement in diffusion length. Once the optimal $POCl_3/O_2$ flow mixture was determined at 875°C, it was used to investigate the temperature range from 850 to 900°C. The data indicated that the optimum temperature for $POCl_3/O_2$ gettering was 890°C.

Spectral response data comparing a non-gettering, and a two and an eight hour gettering sequence at the optimized gas flow mixtures and temperature are shown in Figure 12. These data were used to determine a minority carrier diffusion length of 70 micrometers for the two hour gettering sequence and 160 micrometers for the eight hour gettering sequence.

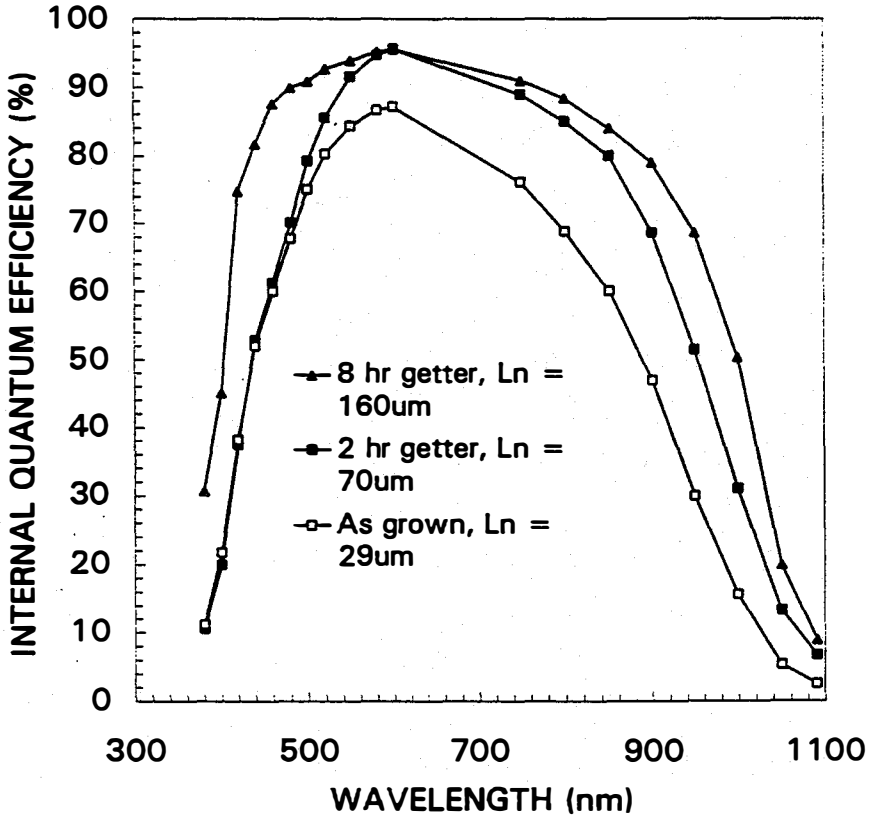


Figure 12. Spectral response curves for as-grown and gettered Silicon-Film™ material.

Forming Gas Anneal

The forming gas anneal process has demonstrated a significant gain in red response. Diffusion length gains of 72% were demonstrated on Silicon-Film™ material processed at Georgia Institute of Technology when forming gas anneal was isolated from the rest of the process.

Surface and Bulk Defect Passivation

Significant gains in the diffusion length of as-grown Silicon-Film™ material were found to result from hydrogenation processes. Early in this effort, Kaufman hydrogenation was employed, but resulted in irreparable surface damage and significant degradation of blue response [3]. An rf-plasma hydrogenation process is presently used on the front surface of the device prior to the emitter etch-back step. Exposure time and rf power have been reduced to maximize diffusion length gains, with only minimum surface damage as measured by the blue response of the device. Some surface passivation is realized by an emitter etch-back step followed by a CVD-deposited SiO_2 passivation layer (see Table 9).

With further development, we expect that as-grown material quality will be improved such that hydrogenation gains by any method will be insignificant, and therefore, blue response degradation from hydrogenation will no longer be an issue.

Emitter Etch-Back

The "simplified diffusion" process developed by Sandia [1] was adapted for the Silicon-Film™ material. The intent of the process was to gain from bulk passivation through aluminum gettering and surface passivation through the generation of a native oxide. However, due to the need for further bulk passivation via hydrogenation, the benefit of the native oxide was lost. In this adaptation, an emitter etch back step which removes some of the front surface damage from rf-plasma hydrogenation was developed. Diffusion profiles, using spreading resistance analysis obtained from Solecon Labs, were used to optimize the junction depth at 0.6 micrometers thus making it plausible to control the emitter etch-back step. This step also assists in reducing the surface concentration and allows for tailoring of the sheet resistance of the emitter.

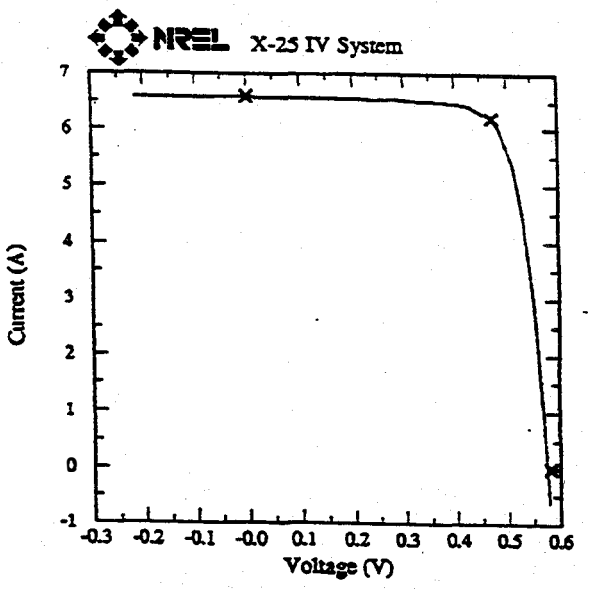
Front Contact Grid Pattern

As post-growth processing and as-grown material quality improved, the high current density of the 240 cm^2 device dictated a re-design of the front contact grid pattern. Fill factor losses indicated a need for reduced series resistance and better collection. The number of gridlines was increased from 50 to 65, the tabbing thickness was increased from 0.127 mm to 0.203 mm, and the emitter sheet resistance was increased from 50 to 75 ohms per square. As a result, fill factors increased from 0.73 to 0.78, but grid shading increased from 3.4 % to 4.1 %.

Advanced Process Solar Cell Performance

One month from the end of this program, the advanced processes discussed above were combined into a working process sequence using state-of-the-art Silicon-Film™ sheet material. The result was a 2.93 W, 240 cm^2 solar cell as measured by NREL. The current-voltage characteristic for this solar cell is provided in Figure 13. Analysis of a similar cell by Sandia indicated that the

primary energy losses in the cell were due to front-surface reflectance (3%), non-ideal recombination (3%) and series resistance (5%). These losses add up to 11% loss in power. An 11% improvement in power for the 2.93 W cell would yield a 3.25 W device.



V_{oc} = 0.5819 V
I_{sc} = 6.581 A
J_{sc} = 27.39 mA/cm^2
Fill Factor = 76.49%

V_{max} = 0.4723 V
I_{max} = 6.203 A
P_{max} = 2929.3 mW
Efficiency = 12.2%

Figure 13. Current-voltage curve measured at NREL for a 2.93 W Silicon-Film™ solar cell.

Our plans to improve the advanced process Silicon-Film™ solar cell include improvements in:

- **diffusion length** of the material through higher quality as-grown material and improved gettering,
- **fill factor** through reduced series resistance and increased shunt resistance,
- **blue response** through improved passivation of the front surface.

These performance enhancements were used to generate the "future process" curve showing solar cell power versus diffusion length shown in Figure 3.

Progress in Solar Cell Performance
(Tasks 4, 12, 20)

Figure 14 illustrates the progress made in AP-225 solar cell performance during the course of the PVMaT program. Deliverable goals and achieved results are both represented.

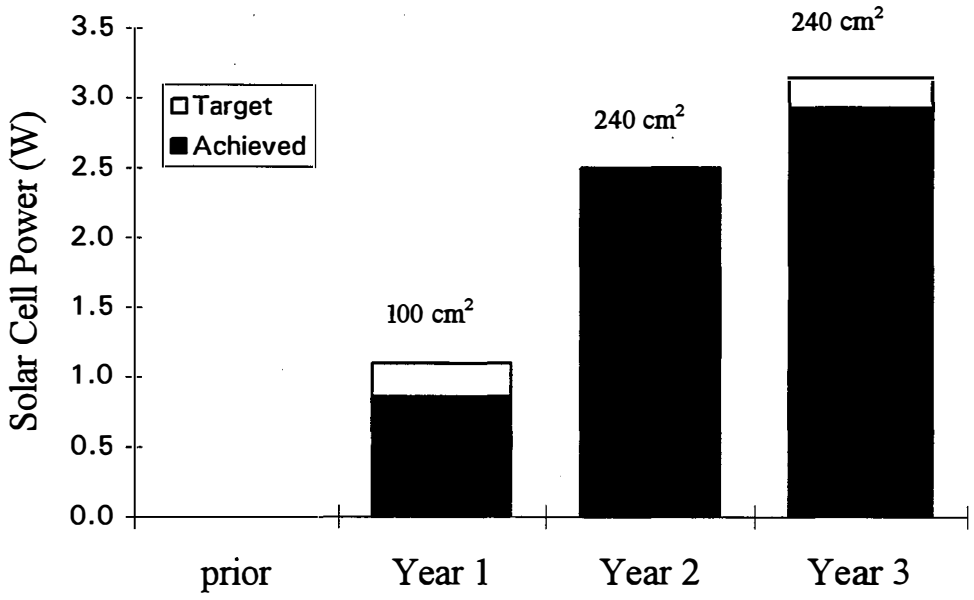


Figure 14. Progress in solar cell performance throughout the PVMaT program.

Material Cost Reduction
(Tasks 6, 13, and 21)

The purpose of these tasks is to reduce the materials' cost of the Silicon-Film™ solar cell process and to reduce the hazardous wastes produced. The main areas of focus were surface preparation and contact metallization processes.

Cost Reduction in Surface Preparation Processes

During Phase II, the surface preparation process was changed to effect a dramatic reduction in both caustic chemical usage and in direct costs. Table 10 shows the direct costs of using the chemical polish (CP) etchant for surface preparation before diffusion. As shown in Table 11, a significant cost savings (67%) was realized in changing to a sandblast and NaOH surface preparation process.

Table 10. Costs of Surface Preparation with CP Etchant Before Diffusion

Material	Cost/unit ($)	Units Consumed	Wafers/unit	Cost/wafer ($)
Hydrofluoric Acid	0.44	9.4	50	0.0830
Nitric Acid	8.12	2	50	0.3248
Acetic Acid	6.72	0.5	50	0.0672
DI Water	0.024	15	50	0.0072
Sodium Bicarb	0.356	20	50	0.1424
Direct Material per wafer				0.6246
Direct Labor per wafer				0.1600
Total Cost of Process per wafer				0.7846

Table 11. Costs of Surface Preparation with CP Etchant Replaced by Sandblasting and NaOH

Material	Cost/unit ($)	Units Consumed	Wafers/unit	Cost/wafer ($)
Sandblast	0.75	21.6	1800	0.0090
NaOH	1.99	66	1800	0.0730
Muriatic Acid	0.10	100	1800	0.0055
HCl	7.8	12	1800	0.0520
HF	0.44	12.5	3000	0.0018
DI Water	0.024	200	1800	0.0027
Sodium Bicarb	0.356	8	3000	0.0009
Direct Material per wafer				0.1449
Direct Labor per wafer				0.0533
Total Cost of Process per wafer				0.1982

Further reductions in the cost, reproducibility, and yield of the NaOH-based surface preparation process are possible. Four inherent problems with this process have been identified:

1. unknown solution concentration,
2. accumulation of reaction side-products in the etching tank,
3. accumulation of etchant residues on wafer carriers,
4. residual NaOH on wafers causing additional localized etching.

These problems are inherent to the batch surface preparation method. Potential solutions were investigated. Off-the-shelf devices for monitoring the NaOH solution concentration were identified as sodium ion probes, however, their accuracy could not be guaranteed due to the corrosiveness of the solution, and the presence of reaction side-products. The reaction side-products composed primarily of sodium silicates contain sodium ions that will affect the probe reading and give false information as to the concentration state of the NaOH solution. Inaccurate monitoring of the NaOH solution leads to both a reduction in product yield and premature

disposal of viable NaOH solution. The more in-depth our study for improvements became, the more convinced we became that an alternative to the batch surface preparation method was needed. Cost/benefit studies on improvements for the batch process never balanced out.

As a result, we are now considering a surface preparation technique that uses a fixed, small quantity of NaOH solution only once. The solution may be sprayed-on and removed with a sprayed rinse. This alternative method would solve the above problems while reducing costs through a reduction in material usage and increased throughput and yield. A complete redesign of the entire surface preparation process and associated equipment is now required. This redesign will consider all future Silicon-Film™ product sizes.

Cost Reduction in Contact Metallization Processes

Efforts were made to reduce the amount of metal paste used to form the screen-printed back contact. Screen characteristics were investigated to achieve a thinner emulsion. Dominant variables determining paste thickness were found to be ink temperature (viscosity), solar cell thickness, printer parameters, and screen age. Since the optimum thickness for the AP-225 is still under investigation, optimization of metal paste consumption will be postponed until AP-225 product development is complete.

Device Equipment/Process Automation
(Tasks 5, 14, 22)

Automation of the present wet chemical surface preparation process is no longer being considered. Preliminary specifications for an alternative method to the present batch process have been completed. In designing the new surface preparation process, all possible wafer sizes to be handled by the system are under consideration.

A fully automated spray anti-reflection coating machine was designed, fabricated, and operated in the processing of PVMaT deliverables. This automated machine demonstrates a throughput of 490 AP-225 solar cells per hour, yielding a higher throughput, a similar solar cell power gain, and an improved encapsulation gain over our PECVD Si_3N_4 process at a significantly lower capital cost.

Module Fabrication Process
(Tasks 7, 15, 16, 23)

Module Fabrication

During this program, module fabrication efforts focused on: (i) evaluating performance of the AP-225 solar cell within a module, (ii) automating critical areas of the module line process, and (iii) investigating the feasibility of wider (than 95 cm) module products. Two different sizes of AP-225 Silicon-Film™ modules were fabricated: (i) a 36 solar cell, 6 cell by 6 cell configuration with a total area of 0.942 m^2 , and (ii) a 56 cell, 8 cell by 7 cell configuration with a total area of 1.438 m^2.

In 1994, 10% of the total modules fabricated by the AstroPower module fabrication line were Silicon-Film™ modules; 12 of these were delivered to NREL under this PVMaT contract and 312 were delivered to the PVUSA site in Davis, California. Fulfilling the PVUSA order generated the volume required to fully test automation projects planned for handling the AP-225 wafers.

36 Solar Cell Module Fabrication

Eleven modules consisting of 36 AP-225 solar cells were delivered to NREL during this program. Test data from the best 36 solar cell modules tested by NREL are shown in Table 12. The process column refers to the processing sequence used to fabricate the solar cells making up the modules. Progress was also made in the automation of two different steps in the 36 cell module fabrication process: (i) tabbing and stringing, and (ii) transfer to lay-up. These two areas are discussed in detail in the subsections that follow.

Table 12. NREL Outdoor Test Data for 36 Cell Silicon-Film™ Modules

ID #	Process	Temp (°C)	Aperture Area (m^2)	Voc† (V)	Isc† (A)	FF† (%)	Pmax‡ (W)	Aper. η (%)
D-23	advanced	22.2	0.912	20.8	5.9	71.8	93.0	10.2
D-29a	baseline	23.5	0.908	19.4	5.2	68.3	73.6	8.1

†as measured
‡ corrected for irradiance to 1000 W/m^2, not corrected for temperature

The estimated U95 uncertainty of the NREL outdoor measurements is ±5%. Temperature was measured at the back of the module during testing; no correction for temperature was made. Total irradiance during these measurements was less than 1000 W/m^2. For comparison purposes the maximum power entries in Table 13 are corrected to 1000 W/m^2. Corrections for spectral mismatch error and second order irradiance error were not made.

Automation of Tabbing and Stringing

Three technologies were considered in the automation investigation for tabbing and stringing. These alternatives were ultrasonic welding, wire bonding, and high intensity light soldering. After evaluating these techniques and associated equipment, high intensity light soldering was chosen for future use. High intensity light soldering offered the following benefits over the other techniques:

- higher throughput (15 seconds per cell)
- solar cell size flexibility
- "no clean" flux (environmental benefit: elimination of organic flux cleaners)
- front and back of cell can be tabbed/strung simultaneously

With the preferred tabbing/stringing technology identified, the new equipment is expected to be designed, purchased, and implemented in 1995.

Automation of Transfer-to-Lay-up

In the third and fourth quarters of 1994, a module transfer unit was designed and built to lift the 6 cell by 6 cell matrix from the stringing jig and to place it onto the lay-up table. This unit was used during the PVUSA effort in which 312 modules containing 36 AP-225 solar cells were fabricated. It will eventually be incorporated into a continuous-mode module assembly line.

56 Solar Cell Module Fabrication

Three modules consisting of 56 AP-225 solar cells were delivered to NREL during this program. The final module dimensions are 127.4 cm by 111.4 cm. This size and configuration was chosen for a feasibility study for future modules having 127.4 or 111.4 cm widths. No effort was made to automate module assembly processes for the intermediate 56 cell module. All steps (e.g. tabbing, stringing, lay-up) were done by hand. Early on, some shifting of individual cells during the lamination process led to uneven cell spacing. To eliminate this problem, 0.005 inch thick fiberglass sheet (Crane Glass 230) was used as cell backing.

Test data from the best 56 solar cell modules tested at NREL are shown in Table 13. The process column refers to the processing steps used to fabricate the solar cells in each module.

Table 13. NREL Outdoor Test Data for 56 Cell Silicon-Film™ Modules								
ID #	**Process**	**Temp (°C)**	**Aperture Area (m^2)**	**Voc† (V)**	**Isc† (A)**	**FF† (%)**	**Pmax‡ (W)**	**Aper. η (%)**
D-28	advanced	15.7	1.391	31.9	6.1	74.9	147.9	10.6
D-29	baseline	19.7	1.400	30.5	5.6	68.4	115.4	8.2

†as measured
‡ corrected for irradiance to 1000 W/m^2, not corrected for temperature

The estimated U95 uncertainty of the NREL outdoor measurements is ±5%. Temperature was measured at the back of the module during testing; no correction for temperature was made. Total irradiance during these measurements was less or greater than 1000 W/m^2. For comparison purposes the maximum power entries in Table 14 are corrected to 1000 W/m^2. Corrections for spectral mismatch error and second order irradiance error were not made.

Progress in Module Performance

Figure 15 illustrates the progress made in 36 solar cell module performance during the course of the PVMaT program. Deliverable goals and achieved results are both represented.

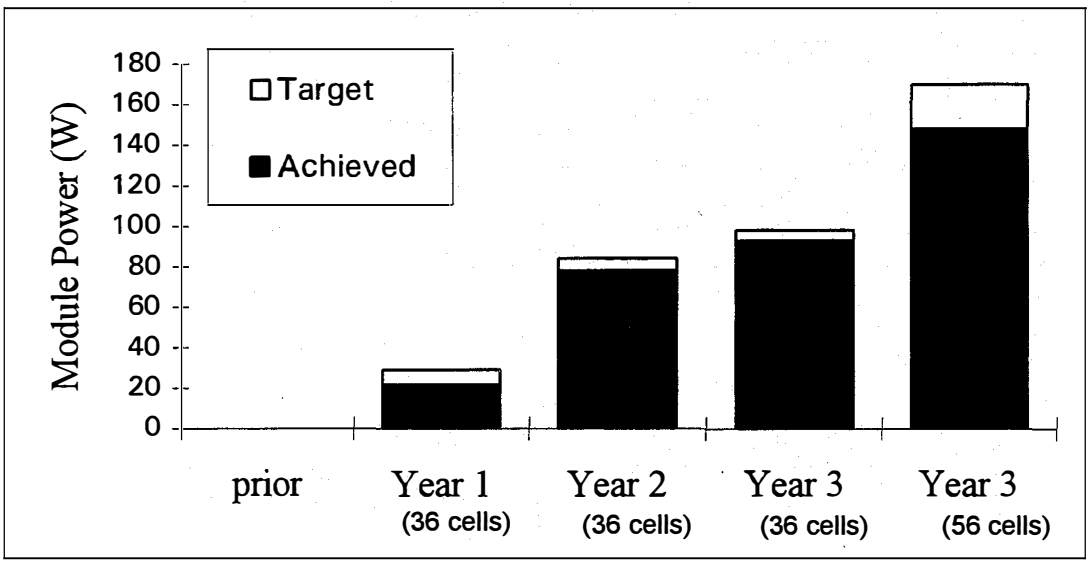


Figure 15. Progress in module performance throughout the PVMaT program.

References

[1] Paul A. Basore, James M. Gee, M. Elaine Buck, W. Kent Schubert and Douglas S. Ruby, "Simplified High-Efficiency Silicon Cell Processing," 7th PSEC, (November, 1993), p. 61.

[2] Isabelle Perichaud, Florence Floret and Santo Martinuzzi, "Limiting Factors of Phosphorus External Gettering Efficiency in Multicrystalline Silicon," 23rd IEEE PVSC, (May 1993), p. 243.

[3] Allen M. Barnett, Sandra R. Collins, William R. Bottenberg, Robert B. Hall, Christopher L. Kendall, Joseph C. Checchi, Steven M. Lampo, William Bloothoofd, David H. Ford, James A. Rand, and Amanda T. Kendall, "Large-Area Silicon-Film™ Solar Cells for Power Applications," 7th PSEC, (November, 1993), p. 245.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 1995	Annual Subcontract Report, 1 January 1994 - 31 December 1994

4. TITLE AND SUBTITLE

Silicon-Film™ Photovoltaic Manufacturing Technology

5. FUNDING NUMBERS

C: ZM-2-11040-5

TA: PV550101

6. AUTHOR(S)

S. R. Collins, R. B. Hall, J. A. Rand

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

AstroPower
Newark, Delaware 19716-2000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

TP-411-20143

DE96000477

11. SUPPLEMENTARY NOTES

NREL Technical Monitor: R. Mitchell

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

UC-1280

13. ABSTRACT *(Maximum 200 words)*

This report describes work performed by AstroPower to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate module. This process starts with the production of continuous sheets of thin-film, polycrystalline silicon using the Silicon-Film™ process. The main product focus is a 240-cm^2 solar cell. Continuous sheets of silicon are produced and cut into wafers that are 15.5 cm on a side. Both standard modules (36 solar cells) and a new 56-cell module were produced. The targeted high-power module design is a 170-W module, used in a 12-module array to generate 2 kW. The project relies on the parallel development of three technologies: (1) a growth technique that produces high quality, polycrystalline sheets at high generation rates, (2) a solar cell fabrication technique that captures the material's potential while qualifying as low cost manufacturing, and (3) a module fabrication process that efficiently integrates the solar cells into a utility-scale power source. Accordingly, project results are presented in three sections that discuss basic development: (1) the Silicon-Film™ sheet fabrication process, (2) solar cell fabrication, and (3) module assembly.

14. SUBJECT TERMS

photovoltaics ; solar cells ; thin films ; polycrystalline silicon ; manufacturing ; PVMaT

15. NUMBER OF PAGES
38

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL