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Advanced Processing Technology for High-Efficiency, Thin-Film $CuInSe_2$ and CdTe Solar Cells

Final Subcontract Report
1 March 1992 - 30 April 1995

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A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
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EXECUTIVE SUMMARY

CIS

The primary objective of this project has been to develop a manufacturing friendly fabrication process for CIS solar cells. The process that we have developed meets this objective. It uses conventional deposition processes and equipment, does not require stringent process control, and uses elemental Se as the selenium source. We believe that it can be readily scaled up using off-the-shelf processing equipment and that it will meet the low manufacturing cost objectives.

Active area efficiencies have approached 10% for non Ga-containing devices. A key issue in the development of this technology is the need to balance bulk and surface/interface properties. The 10% performance level is a compromise between the two. To better understand the fundamental mechanisms driving this interplay, we have used a phenomenological device model to analyze both material and device properties. The model has identified the space charge region adjacent to the CdS as the region that dominates performance through recombination phenomena. Using the guidance of the model we have developed interface modification procedures which significantly reduce recombination and result in V_{oc}'s much greater than those in our 10% devices. There is an accompanying loss in collection efficiency that thus far has limited overall performance. However, we have recently discovered how to control this limitation and expect to boost our V_{oc}'s by 20% which will result in device efficiencies in the 12% range.

We have also developed a considerable basis of understanding of the dependence of material and device properties on deposition parameters. Much of this understanding has come from running three different selenization/anneal processes which has allowed decoupling of complex growth mechanisms. Application of this understanding has allowed the successful transfer of process advancements to our favored, most manufacturing friendly process. This understanding will also guide the next phase of development which will include addition of Ga and S to the process stream. These enhancements will be conducted within our manufacturing friendly guidelines and will advance efficiencies beyond the 12% level.

Another significant achievement of this project has been the development of a reactive sputtering deposition technology for ZnO. ZnO is used in many solar cell devices, and sputtering is a desirable manufacturing technology. However, application of sputtering has been limited because conventional deposition uses ceramic targets which result in low sputtering rates. The use of Zn metal as the target in reactive sputtering overcomes this limitation.

We have demonstrated that ZnO deposited by reactive sputtering has state-of-the-art opto-electronic properties. We have also developed a solid basis of understanding of the fundamental mechanisms which determine those properties and of the relationship of those properties to deposition parameters. Application of that understanding results in large area uniformity and optimized performance. These developments provide a significant opportunity for application and commercialization of the technology.

EXECUTIVE SUMMARY

CdTe

The main objective of this project is to fabricate high efficiency CdTe solar cells using manufacturing friendly processes. Three deposition processes are being used for the deposition of CdS films; chemical bath deposition (CBD), rf sputtering, and close spaced sublimation (CSS). The CdTe films are deposited by CSS. Both borosilicate as well as inexpensive soda lime glass have been used.

The CSS and rf sputtered CdS films were incorporated into the devices which were mainly processed using the same process that have yielded over 15% efficiencies in the past. State-of the-art V_{OC}'s have been achieved using either process for the deposition of the CdS films. Devices fabricated with CSS CdS exhibited FF's in excess of 74%. In general the performance of these cells suggests that efficiencies over 15% are possible; this will be accomplished once the current density of the cells is further increased. Solar cells prepared using CdS by rf sputtering were limited by low J_{SC}'s and FF's. The low J_{SC}'s are partly due to the fact that the thickness of the CdS(rf) must be at least 2000Å in order to obtain high V_{OC}'s and due to excessive interdiffusion that reduces the SR response of the cells. Annealing of the CdS in a H_2 ambient improved the performance of these cells considerably.

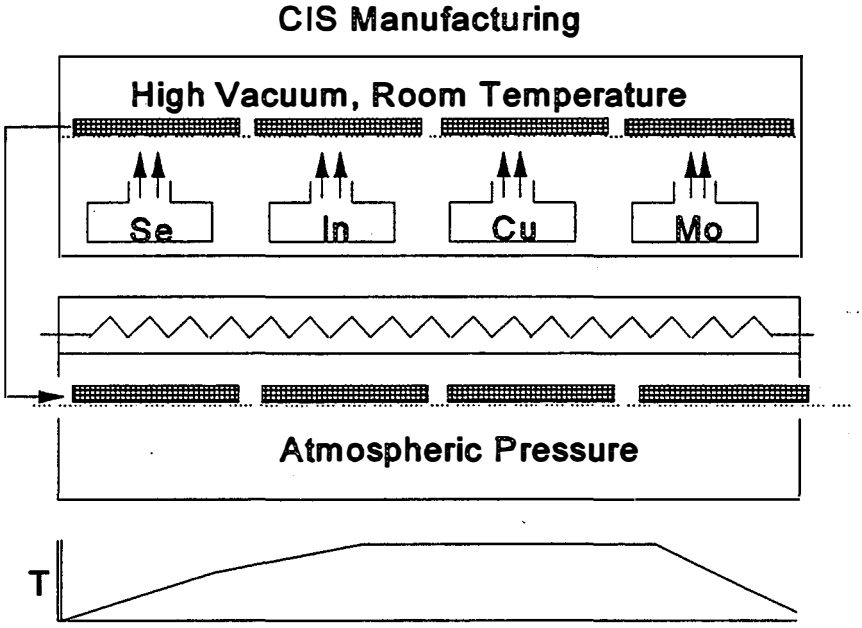
Devices fabricated from CSS and rf sputtered CdS have provided valuable information and insights relating to the formation of the CdTe/CdS junction. The results are suggesting that "some" interdiffusion at the CdS/CdTe interface is necessary for obtaining high open-circuit voltages, however this condition alone does not insure that high V_{OC}'s will be achieved. Controlling the degree of interdiffusion with some precision is still a challenge mainly due to the numerous high temperature processes involved in the fabrication of these devices.

By maintaining all processing temperatures below 550°C CdTe cells have been fabricated using inexpensive soda lime glass substrates. Efficiencies of 13.5% have been verified by the National Renewable Energy Laboratory. Current work suggests that these devices will soon exceed the 14% mark. The efficiencies are mainly limited by low J_{SC}'s due to the poor optical properties of the glass substrates.

PART I: CIS

1.0 DEPOSITION METHODOLOGY

Throughout the course of this project our primary objective has been to develop a process that can be more easily scaled up to a manufacturing level than the "incumbent" technologies. The process which we favor is shown in figure 1 below. This process includes



1. Proposed CIS manufacturing process.

the following features which significantly enhance its manufacturability.

* Deposition of components at room temperature

* Sequential deposition of components, i e, no co-deposition

* Use of elemental selenium rather than H_2Se

* Separate, atmospheric pressure(inert gas) anneal

Because of these significant advantages we have chosen to place primary emphasis on running laboratory processing units which match this process design. And, as will be discussed, we have made our most efficient devices using this process.

With the exception of Se deposition all process steps can be accomplished with conventional off-the-shelf processing equipment. Mo, Cu and In are deposited by magnetron sputtering, a technique that is in common use for producing large area architectural coated glass. The anneal step can easily be accommodated by readily available belt furnaces. The only weak spot in the process is the fact that Se is evaporated. Evaporation over large areas is not known to be a readily available technology, especially for volatile materials like Se. However, the process is less sensitive to Se variations than to variations in the metal thicknesses. That this renders the development of a suitable Se source straightforward remains to be proven, but our development and understanding of the process to date suggest that it should be so.

In the following sections we describe the variations on the above process which we have been running. These fall into two main categories. Process I is identical to the above manufacturing scheme. Process II involves use of a Se flux during the anneal cycle. An outline of the thoughts that have guided these process developments is provided below.

REACTION PATHWAYS

GUIDELINES

* $Cu + In + H_2Se$ works

* $Cu + In + Se(s) \rightarrow CIS$, but, reactivity: $Se(g) > Se_2(g) > Se(s)$ g - gas, s - solid

* $Cu_ySe + In_xSe \rightarrow CIS$, but, less favorable than elementals

PROCESSES

	I	II
Step 1	Sequential Cu/In(.8/1)	Sequential Cu/In(.8/1)
	↓	↓
	$Cu_yIn_x + Cu + In$	$Cu_yIn_x + Cu + In$
Step 2	Deposit Se(≥20% excess)	Heat to 400°
	↓	Add Se flux
	$Cu_yIn_x + Cu + In + In_xSe + Se$	Ramp to 550°
Step 3	Ramp to 550°	
	↓	↓
	$Cu_ySe + In_xSe + Cu_yIn_xSe_z + Se$	$Cu_ySe + In_xSe + Cu_yIn_xSe_z + Se$
	↓	↓
	$CuInSe_2$ (+ $Cu_yIn_xSe_z + Cu_ySe + In_xSe$)	

OBSERVATIONS/ISSUES

* "All" paths lead to CIS

* Secondary phases are also formed and must be controlled

* CIS defect structure must also be controlled

* Reaction pathway may also influence grain size and orientation

* There is insufficient understanding of the above to determine the eventual merits of a given process

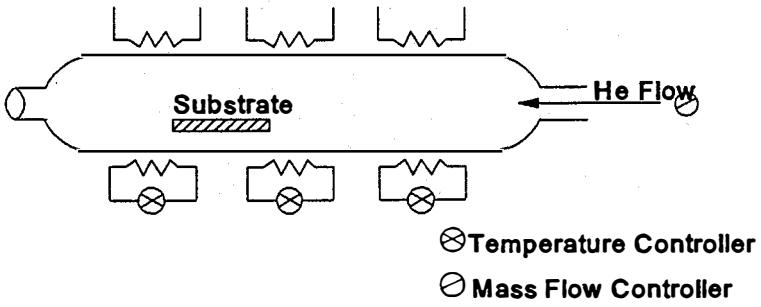
Additional details on the above can be found in the Phase I[1] and Phase II[2] reports for the project. Further discussion of the processes is provided below.

1.1 Process I

The three processes which we are practicing are commonly thought of as "two step" involving deposition of the metal "precursors" followed by a selenization/anneal step. They differ primarily at the selenization/anneal step. Details regarding the glass substrate, Mo deposition, and deposition of the metal precursors can be found in the Phase I[1] and Phase II[2] Technical Reports for this project as well as in various publications which will be referenced later in this report. The basic precursor film common to all processes is sputtered Mo on soda lime glass followed by separately sputtered layers of Cu and In. (We also note that these devices do not contain Ga.) The Cu/In ratio is of course a primary variable.

Each CIS film which we produce is fabricated into a solar cell device in the form: glass/Mo/CIS/CdS/ZnO. Details regarding device fabrication can also be found in the reports mentioned above. Basically we use solution deposited CdS(see Appendix A) followed by a high resistivity/low resistivity film of sputtered ZnO:Al. Measurements in device format is our primary means of determining film properties as well as of evaluating bottom line performance.

A schematic of the Process I reactor is shown in figure 2. It is a multi-zone tube furnace which runs at atmospheric pressure(He). Anneal profiles are achieved by moving the substrate through the various temperature zones which are preset to desired levels. The substrate typically consists of glass/Mo/Cu/In/Se. Additional Se is provided either from the reactor walls or by introducing an additional source into the reactor. In either case there is no attempt to control the Se flux during the anneal. An amount of Se in excess of that required to form stoichiometric CIS is provided, and the film growth mechanisms themselves determine the incorporation of Se. This reactor has no pump, therefore, high He flow is used after inserting the substrate to reduce atmospheric contaminants . (The Process IA reactor described below has a mechanical pump allowing pump/purge cycling to further reduce contaminants.)



2. Process I reactor.

1.2 Process II

Process II involves a selenization reactor in which we can control the Se flux throughout the anneal. Our interest in this type of process is twofold: 1. It can be used to advance understanding of selenization, 2. It may be acceptable as a manufacturing process if Process I does not meet our objectives. With regard to the latter, we note that others feel that this is a commercially viable process, and we agree if it can be demonstrated that the degree of flux control is reasonable. Here we are concerned not just with uniformity over large areas, but as well with uniform rates of flux. As we have stated, we continue to place emphasis on Process I development, and perhaps that is why it presently produces our best devices. Process II however, is close behind. This in part is due to the fundamental differences between the two which result in somewhat different requirements for the metal precursor. Perhaps the key difference between the two is pressure. The low pressure of process II changes the kinetics and availability of Se at the surface. This allows us to study these phenomena in a straightforward way with process II, while for Process I these phenomena are more complex. We thus are using process II to guide our further development of Process I. Comparisons of performance between the two for equivalent precursors is very useful in deconvoluting the complex growth mechanisms.

1.3 Process IA

Process IA is based upon use of a CSS-like reactor similar to that used in the CdTe project. The intent is to be able to match Process I and then extend the process parameters beyond the capabilities

of the tube reactor used for Process I. In particular, Process IA can run under reduced pressures, provides for some measure of control over Se flux, and is less susceptible to atmospheric contamination. Thus Process IA is going to include those components of the above features which are found to be necessary for improved performance.

2.0 FILM PROPERTIES

2.1 Stoichiometry/Structure

Since this deposition approach relies upon intermixing of sequentially deposited layers of precursor materials, it is important to establish the extent to which this occurs. The first level check on CIS film quality is stoichiometry. This is monitored by using EDS on our JEOL 840 SEM. This technique is limited by both the sensitivity and resolution of the instrument and by matrix effects in the sample. To minimize the latter it is necessary to have reference samples that closely match the composition of a given experimental sample. To facilitate this process NREL[3] has kindly provided us with a set of reference samples. Representative atomic composition results from three samples are shown in Table 1 below.

TABLE 1. SAMPLE COMPOSITION DETERMINED BY EDS

SAMPLE	Cu(%)	In(%)	Se(%)
A21	23.43	25.04	51.53
A40	24.48	26.94	48.57
A45	24.13	25.34	50.53

As can be seen the samples are all near perfect stoichiometry, and slightly In rich as desired.

Because the electron beam only probes to a depth of order 5000 Å these values are representative of only that part of the sample, although it is the most important. Nevertheless it is desirable to know the composition of the entire sample both to gauge the extent to which CIS formation occurs throughout the layers and to understand the nature of the remaining bulk material even though it may be outside of the space charge region. To accomplish this a piece of film was peeled from the substrate so that the composition of the bottom of the film near the Mo substrate could also be measured. The results are shown in the Table 2 below. As can be seen, there is little difference between the top and bottom composition for this sample indicating that CIS formation in terms of composition is fairly homogeneous. It is interesting to note that both top and bottom surfaces/interfaces of the sample are In rich as a result of using Cu/In < 1 in the deposited films. The composition of the Mo surface from which the film was peeled is also shown in the table. Although the exact values here are less reliable because they are standardless(i e, not against an appropriate reference), they confirm the presence of In at the back interface and highlight the great propensity for

Cu to diffuse into and form CIS. The high level of Se is also important in that it verifies access by Se to the entire film thickness. It is likely that the Se in this region is in the form of $MoSe_2$.

TABLE 2. COMPOSITION OF TOP AND BOTTOM OF SAMPLE

	PEELED SAMPLE		MO SURFACE
	TOP	BOTTOM	
CU	24.5	23.3	0
IN	27.0	27.6	03.2
SE	48.5	49.1	20.0
MO	0	0	76.8

The gross structural features of the films are also examined by SEM imaging. What we observe is that films with similar stoichiometries can exhibit notable differences in structural properties. Grain size varies from one micron and down, and grain size is not correlated in a straightforward way with performance. One also has to be concerned with the presence of subphases and point defects as well as the interplay between surface and bulk properties and how these are affected by contact formation. As we show below, grain size is part of the performance equation, but accounting for the additional factors is more difficult.

2.2 Defect Density

An issue of importance to this project is to demonstrate low defect I layers, that is, CIS base material with low defect density. We have previously reported defect levels in the $10^{14}/cm^3$ range for films made in conjunction with thin-film transistors[4]. During this project we also achieved a level of $6 \times 10^{14}/cm^3$ as determined by CV in a device(9.5%). As seen in figure 3, the $1/C^2$ vs V plot measured at 500 kHz had a constant slope over a range of about two volts from which N_A is calculated, and an extrapolated built-in voltage of about .8 volts is determined. We note that such classical behavior is not typically observed. We have also assumed a 1-1 correlation between N_A and point defects. In the absence of more definitive techniques at this time we adopt this process for such purposes. Since this process correlates low N_A with our best devices we feel that it is valid on a bottom line basis if not on the details of the fundamental assumptions.

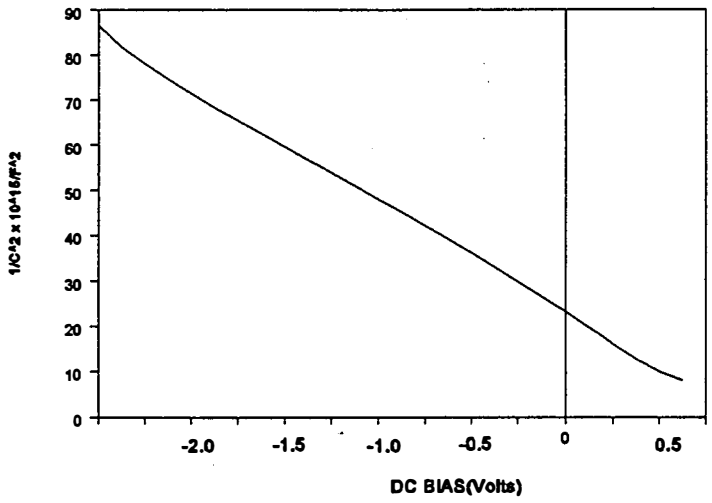


Figure 3. $1/C^2$ vs. V for a high V_{oc} sample.

3.0 DEVICE MODEL

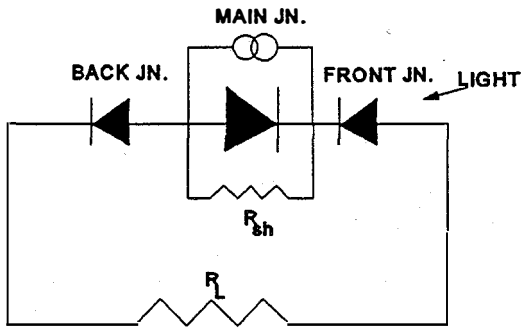
An important activity which we have also been undertaking is the development of a phenomenological model to help guide our fabrication efforts. The primary development of the model itself is being conducted under the auspices of another project[5]. In this project the emphasis is on providing samples and data to support the link to processing. The basics of the model involves use of the following equation which includes both diffusion controlled and recombination controlled current terms.

$$I_F = \{(q/N_A)(D/\tau)^{1/2}n_i^2\}e^{qV/kT} + \{qkTWn_i/2V\tau\}e^{qV/AkT}$$

where A - diode factor
q - charge
N_A - acceptor concentration
D - minority carrier diffusion coefficient
τ - minority carrier lifetime
n_i - intrinsic carrier density
V - applied voltage
k - Boltzmann constant
T - temperature
W - space charge width

Results to date indicate that recombination dominates performance and that the diode factor A in the recombination term varies between 1 and 2.

Before the behavior of the main junction can be observed it is necessary to properly account for the other mechanisms contributing to performance. We have found that the following circuit diagram adequately depicts those mechanisms. The front junction is light sensitive



4. Device schematic diagram.

and accounts for the crossover effect that is commonly observed. The back junction is at the Mo interface. Its presence accommodates the bendover in V_{oc} vs. T plots at low temperatures. Once these mechanisms which are not part of the main junction are accounted for, effects associated with the main junction can be studied. An example of the ability of the model to fit experimental data in a self-consistent manner is shown in figures 5, 6 and 7 below.

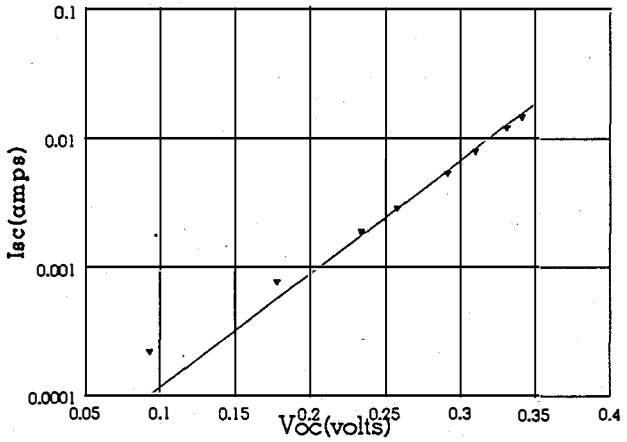


Figure 5. Ln(I_{sc}) vs. V_{oc} - line is A=2 simulation.

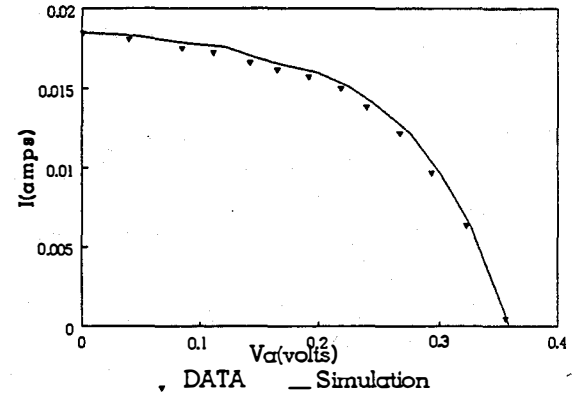


Figure 6. Power curve simulation.

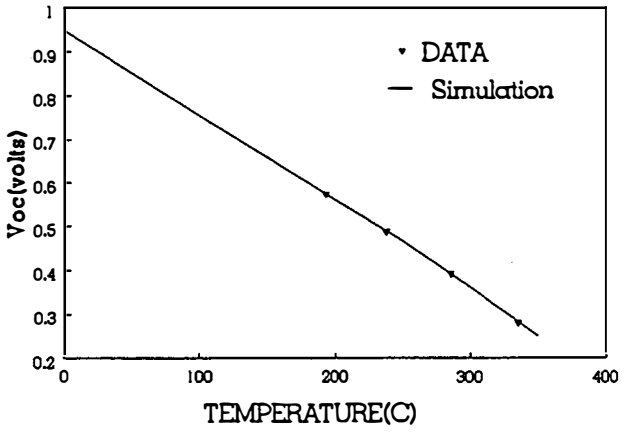


Figure 7. $V_{oc}(T)$ simulation.

The insights provided by the model then allow us to evaluate the performance of each device which is fabricated in terms of fundamentals. We can then relate the influence of processing parameters on these fundamentals. Much of the discussion on device performance which follows revolves around this methodology.

4.0 DEVICE PERFORMANCE

4.1 Effect of Process Parameters on Performance

4.1.1 Metal Ratio

To understand the sensitivity of the favored Process I to processing details we must first describe the baseline. By baseline in this case we mean device performance which is typical and reproducible. For Process I the key attributes of baseline devices are an efficiency of 8% with a V_{oc} of 350 mV. While J_{sc} is typically around 40 mA/cm^2, FF tends to be in the .58 - .6 range because the same mechanism that controls V_{oc} also controls FF. The attributes of the best devices from this process are shown below. J_{sc}'s are on the high side because the band

V_{oc}: 400 - 410 mV
J_{sc}: 35 - 40+ mA/cm^2
FF: .58 - .62
Eff: 9 - 10 %

gap is about .95 eV. This in part also lowers the expected V_{oc}'s, although as we will discuss, they are further limited by other mechanisms. Also, we wish to note that these devices do not contain Ga. Though we expect that the addition of Ga will enhance performance, we have not yet included it in our baseline processing to avoid complications that might hinder progress on understanding the

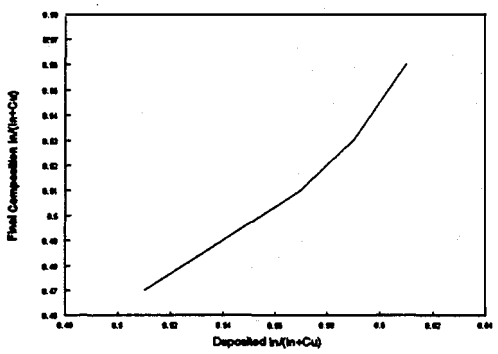


Figure 8. Final metal ratio vs. deposited metal ratio for Process II baseline.

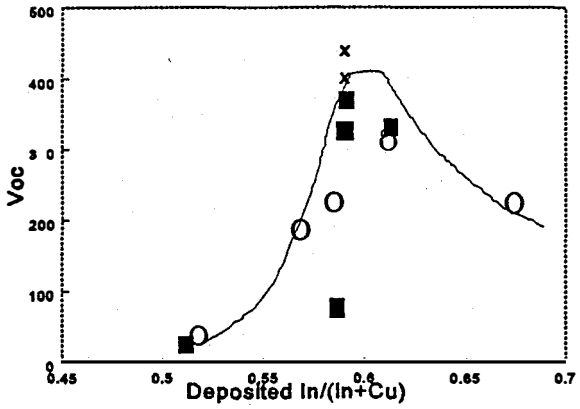


Figure 9. Voc vs. deposited metal ratio for Process I(■) and II(O) baselines and for advanced selenization(x).

fundamental mechanisms for CIS itself. While these efficiency levels can not be compared to those of state-of-the-art devices from the literature, we feel that when placed within the context of the simplicity of the process used to achieve this performance, the results are significant. Furthermore, as we will show below, there are further developments under way which we believe will advance our performance levels toward the 15 - 17% range without compromising process simplicity.

An important issue regarding manufacturability is the sensitivity of performance to atomic composition. In all of our processes we deposit the metal precursor layer first and then add Se under various conditions. We are thus concerned with the sensitivity to the starting metal ratios and to the amount and method of delivery of Se. In figure 8 we show the relationship between the deposited and final(in the finished CIS film) metal ratio, and in figure 9 we show the dependence of V_{oc} on that ratio. To first order J_{sc} and FF track V_{oc}, and thus it is an indicator of overall performance. As seen, the two processes track very closely indicating that Process I, thus far, is able to match the performance of the controlled flux Process II. Sensitivity to metal ratio is high on the low In side with V_{oc} plummeting toward zero as film composition approaches In/(In+Cu)=.5. The In-rich side is less precipitous though still indicating the need for adequate control. The data points above the curve at In/(In+Cu)=.58 in figure 9 are for recent modifications to the baseline processes which have taken us through 400 mV. These advances are discussed in terms of improvements in recombination mechanisms below.

4.1.2 Selenization

We are presently focusing our efforts with these process comparisons on understanding the relationship between selenization details and V_{oc} generation. In Process I we make a specific amount of Se available to the precursor, but have little understanding of the details of its availability and consumption. To address this issue, we have used Process II to mimic one aspect of the Process I reaction, that of the total amount of available Se. We also can deliver the Se during various stages of the anneal. Results from these experiments are shown in figures 10 and 11. In each case we need one micron of Se to be incorporated to achieve

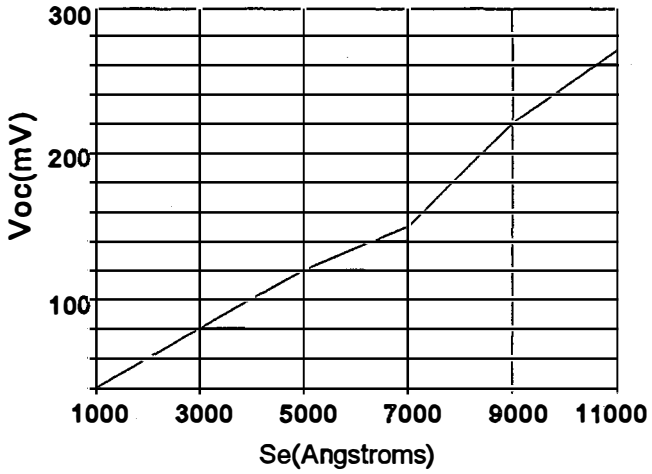


Figure 10. Dependence of V_{oc} on fluxed Se thickness(added to 1 μm base at 300 < T < 400 C).

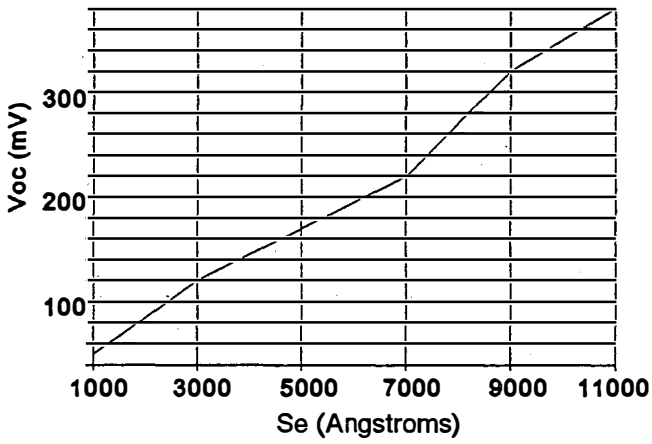


Figure 11. Dependence of V_{oc} on Se flux thickness(added to 1 μm base at T > 430 C).

stoichiometry. Also, for both temperature ranges we have already provided one micron of Se to the surface prior to reaching the subject temperature range. This one micron may be deposited at room temperature or on the way up in temperature. The data shown is a compendium of variations of these conditions. What is plotted is the additional Se flux provided in the indicated temperature range. For the 300 - 400 C range the flux is terminated prior to proceeding to the ultimate anneal temperature above 430 C. As can be seen, there is a steady increase in V_{oc} with Se flux for both ranges. While this suggests that the stoichiometric quantity of Se which has previously been provided has not all been incorporated, we must also consider that this may be an entirely surface driven result having primarily to do with adjustment of the surface composition. We expect that if so, the effect should be a function of the metal ratio.

An important observation from these results in reference to Process I is the necessity of providing Se flux above 430 C to achieve 400 mV. Because of the intentional minimal control design of Process I we know little about the behavior of Se during the anneal. These results tell us that in Process I runs in which we are achieving 400 mV there is Se flux available even at the high temperature end of the anneal. This insight is providing critical guidance to Process I modifications which are expected to lead to further advances in performance.

4.1.3 Anneal Profile

One of the most critical features of processing is the anneal profile. We have throughout the project been experimenting with various profiles to accommodate the different reactor geometries and the large set of possible precursor configurations. Developing an understanding of the interplay among these is the key to processing success. Much of the progress which we have made is attributable to building this basis of understanding. While we have found several "local maxima" in this complex operating space which have led to specific improvements at times, on an ongoing basis we have had to decide when to abandon a route and seek out another that may take us farther and faster. The profile which we have settled on at this point is shown in figure 12. As can be seen it quickly bypasses the low temperature regime and emphasizes temperature over time. This profile produces our best devices with efficiencies in the 9 - 10% range. The best literature efficiencies for devices not containing Ga like these are of order 12%. Thus we are approaching state-of-the-art performance. It is also appropriate to point out an important practical feature of these results. As the profile in figure 12 shows the total anneal time is 30 minutes. However, our standard cool-down time has been an additional 120 minutes. We have shortened it to 60 minutes and have observed no adverse influence on performance. Clearly we want to reduce the cycle time as much as possible. So far we have no evidence of a lower limit that would be unacceptable at a commercial level.

The devices from this process work right out of the reactor and do not require an air anneal as is common for other processes. We have speculated that because of the non-vacuum status of this reactor there is residual oxygen present during film formation which provides for an in situ air anneal.

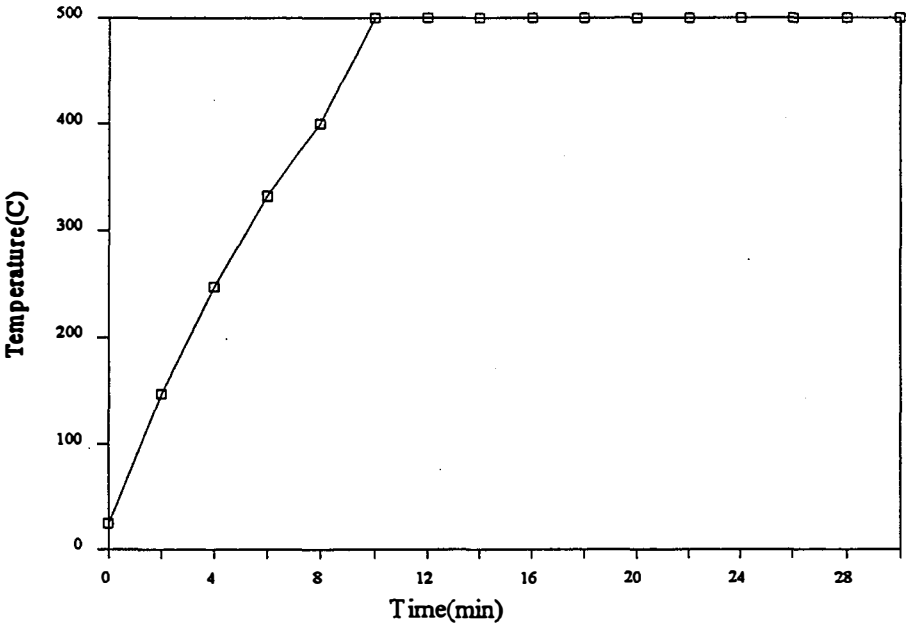


Figure 12. High temperature anneal profile.

However, we are concerned that the in situ anneal sometimes goes beyond the optimum point and diminishes performance from what would otherwise occur for a given run; that is, some devices may perform better for a given set of run parameters if the anneal were a separate, controllable step. We reduced the cool-down time as a means of reducing the time of the in situ anneal. While the resulting unchanged performance is good news for practical reasons, further effort is needed to control and optimize this mechanism.

Another objective of this project is to establish generic understanding of the relationships among processing, film properties and device performance. Table 3 below contains data that addresses this objective in conjunction with variations in the anneal profile. Anneal profile 1 is a multi-step, low temperature profile; anneal profile 2 is a fast ramp, low temperature profile; and anneal profile 3 is that of figure 12. Additional details can be found in the Annual Report for Phase II[2]. The atomic compositions and grain size are determined from SEM/EDS analysis. While EDS is calibrated by a NREL supplied reference, we believe it to be accurate to only +/- 0.5%. As can be seen, the metal composition is essentially the same for all devices. We note however, that the initial Cu/In ratios were in the range .75 - .90. While this is certainly an important variable, the results presented here suggest an at least equally strong role for grain size. As can be seen, grain size varies directly with anneal temperature, and both V_{oc} and J_{sc} vary directly with grain size. Variations in the starting metal ratio certainly contribute to the range of V_{oc} and J_{sc} values observed for a given grain size. This result is

TABLE 3

Sample	Cu(%)	In(%)	Grain size(μ)	V_{oc}(mV)	J_{sc}(mA/cm^2)	Anneal Profile
11	24.3	25.7	.5	190	23	1
21	23.3	25.0	.7	220	33	2
40	24.5	26.9	.7	200	31	2
45	24.1	25.3	.7	175	24	2
148	24.8	24.8	>1	380	39	3
175	24.9	24.8	>1	410	40	3

what one might expect qualitatively. Higher growth temperatures normally result in larger grain size. The presence of additional phases, however, complicates matters and we have not properly accounted for their role here. We may speculate nevertheless that going to a high growth temperature rapidly reduces the number of nucleation sights and thus results in larger grain size.

The dependence of V_{oc} and J_{sc} on grain size is also intuitively comfortable. J_{sc} depends on transport properties, and smaller grain size usually results in poorer transport. V_{oc} behavior suggests that grain boundaries may contribute to J_o. The implications of these and the other effects above on device performance are discussed in the next section.

4.2 Performance Enhancement and Prognosis

4.2.1 Collection Losses

In assessing the performance of our devices it is useful to make comparisons with state-of-the-art literature devices. In figure 13 we show such a comparison with a 12.2% Siemens Solar Inc. device reported in the literature. We have adopted this as our reference because with the exception of the use of H_2Se by SSI we believe their processing approach to be relevant to ours, and, this device did not contain Ga. We have discussed this data and the model which fits the data already in some detail[2]. What we want to focus on here is the observation that our devices generally fall into two categories, those with high temperature V_{oc}-T slopes the same as the SSI sample and those with shallower slopes.

Our recent analysis suggests that devices in the latter category are limited by a current collection mechanism. In particular, device 175 which has a V_{oc} over 400 mV at room temperature falls way

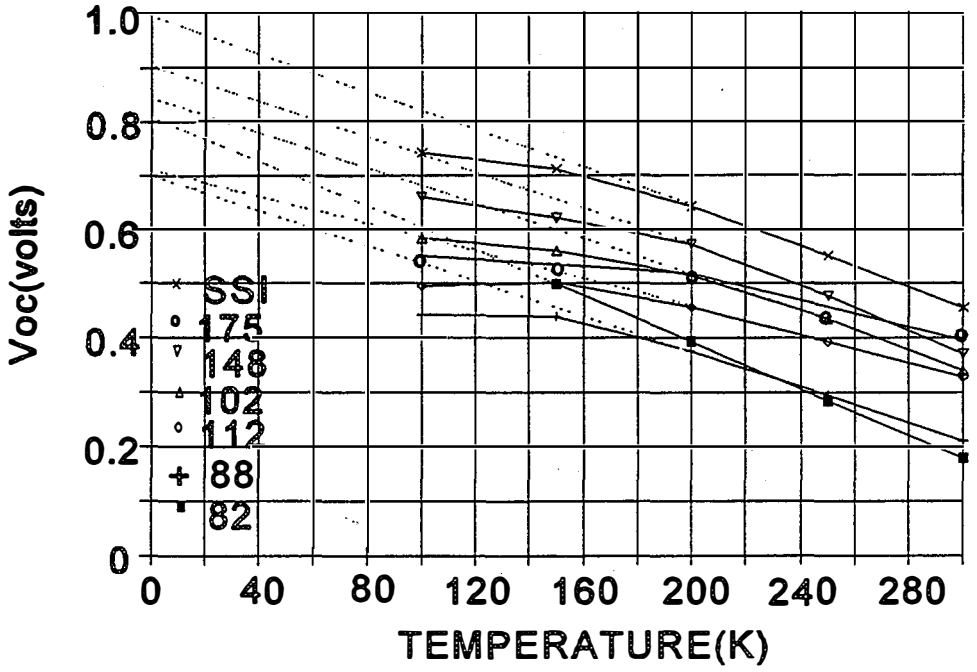


Fig 13. Voc vs. T for a literature device(SSI) and representative USF devices.

below the "idealized" curve as temperature is lowered. The primary cause of this problem is found by examining the power curve at 100 K in figure 14a. As can be seen in 14b, the normal shape at room temperature is distorted into an "S" shape at 100 K. The dark IV curve behaves normally, and the amount of crossover is minimal. Hence we believe the distortion in the power curve to be due to losses in collection efficiency at lower temperature. The effect of temperature on J_{sc} and on the light generated current at a forward bias of .3 volts is shown in figure 15. There is a modest drop with decreasing temperature for J_{sc} and a more dramatic drop at .3 volts. By combining the low temperature data with the room temperature IV curve we have constructed the dependence of light generated current on voltage shown in figure 16. We are currently fitting this behavior to a field-dependent collection model. But the primary point to be made is that this device has lost a significant amount of voltage due to this mechanism. As can be seen , the current is down by about a factor of 2 at V_{oc} compared with its I_{sc} value. The projected effect on the power curve for the device is shown in figure 17. As indicated, if the light generated current were maintained at 40 mA/cm^2, the V_{oc}

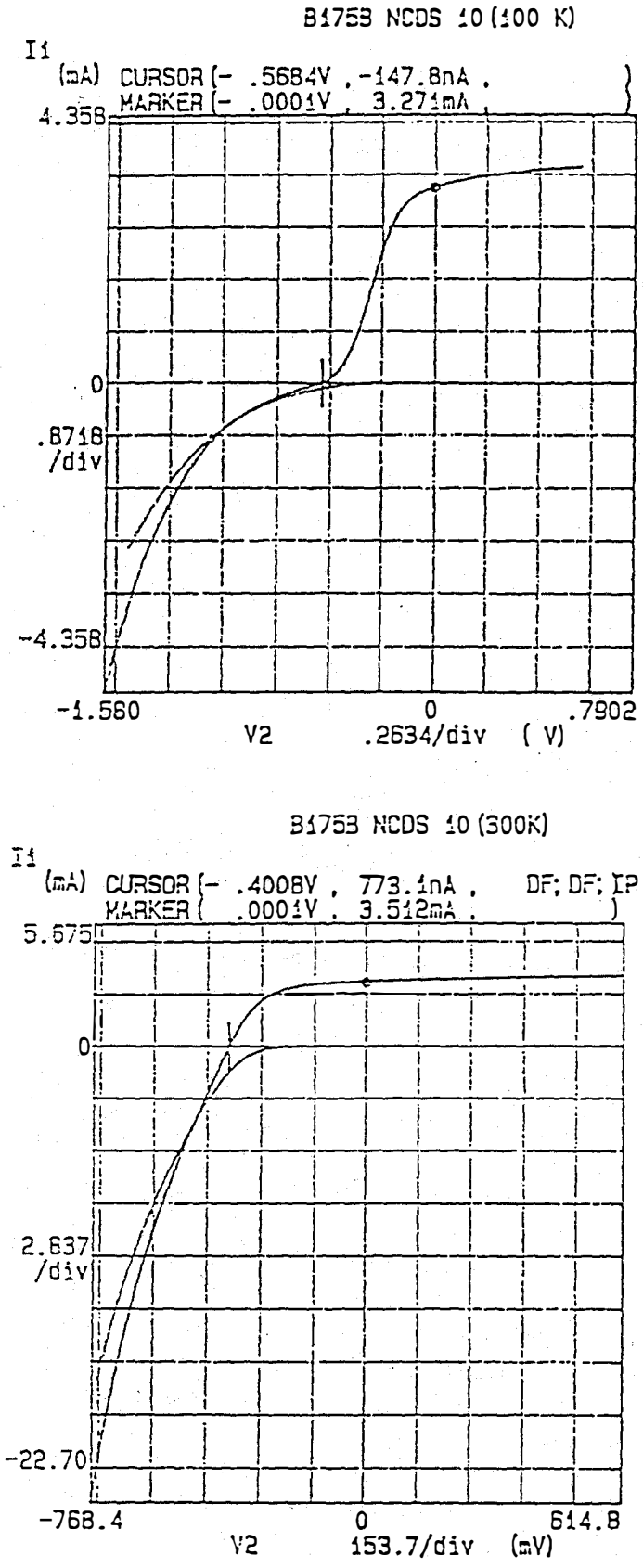
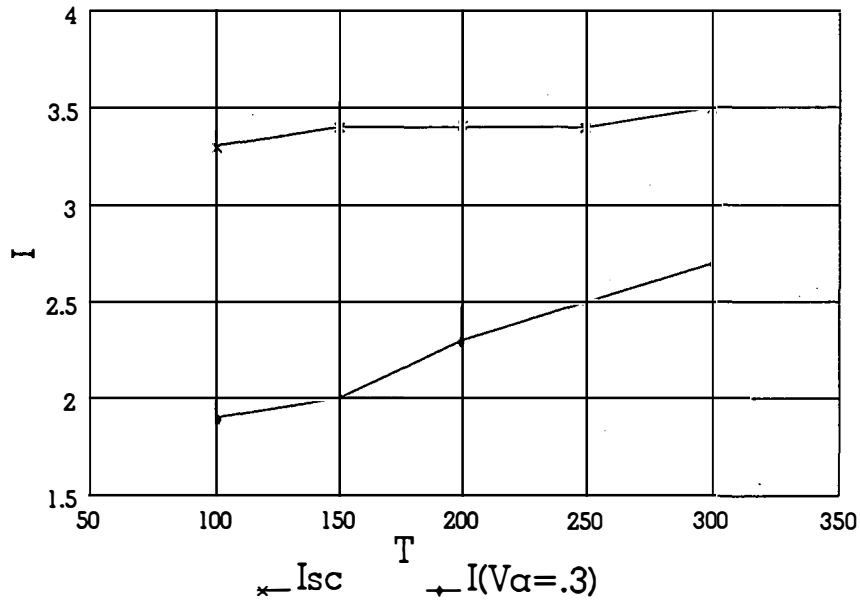
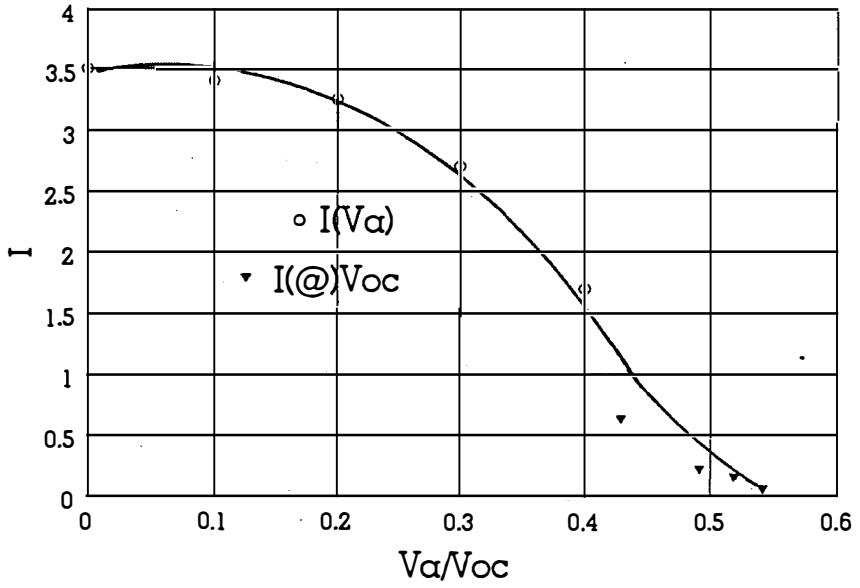


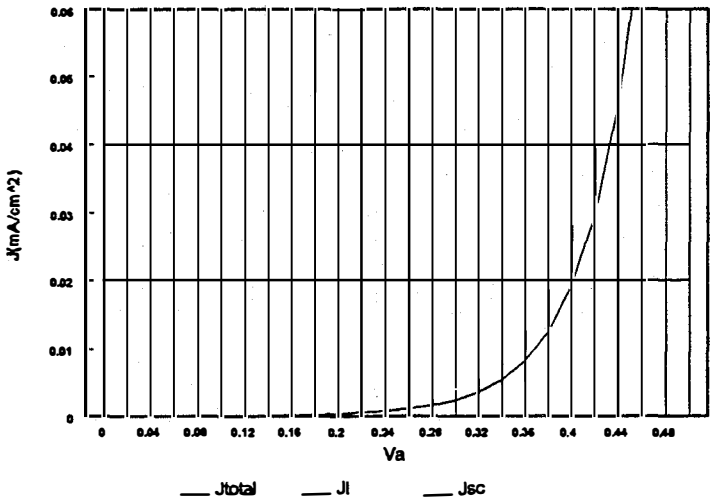
Fig. 14. Power curves at 100 K and 300 K.



15. Light generated current vs. temperature for device 175B.



16. Light generated current vs. voltage for device 175B.



17. Power curve for device 175B. Actual Jl @ V_{oc} = 20 mA/cm^2, projected Jl = 40 mA/cm^2.

would have been 430 mV, placing it within 5% of the state-of-the-art SSI device. In the next section we discuss why we believe this to be a solvable problem and present data showing progress toward eliminating it.

4.2.2 Reduction of Recombination Centers

As discussed above a recombination-based model appropriately describes the performance of our devices. Using the model we have found that the primary determiner of device performance is the density of recombination centers(N_t) in the space charge region. For baseline devices described above the V_{oc} value of 350 mV is due to a recombination center density of about 3 x 10^{17}/cm^3. Since V_{oc} varies logarithmically with N_t as shown in figure 18, improvements in V_{oc} require rather large reductions in N_t. In our better devices with 400+ mV we have been able to lower N_t below the 10^{17}/cm^3 level through improvements in the selenization/anneal profile. Also, we have recently applied an etching procedure to our baseline devices to evaluate their performance as we systematically lowered the recombination center density. In doing so we found that the V_{oc} increased to 430 mV which would correspond to a N_t of 5 x 10^{16}/cm^3. However, as we varied the degree of etching, we also noted a decrease in J_{sc} proportional to the etching time. Through further analysis of device performance we determined that J_{sc} was decreasing due to a reduction in collection efficiency. A tentative explanation is that the etchant, while removing interface recombination centers, was also creating recombination centers deeper into the space charge region. While on balance this helped V_{oc}, it diminished J_{sc}. The effect of the etchant on transport properties produces collection losses similar to those discussed in the section above. Thus this key performance controlling mechanism can be induced in good devices by manipulation of the top surface region. We feel that these insights provide us with a very effective tool to understand and improve performance.

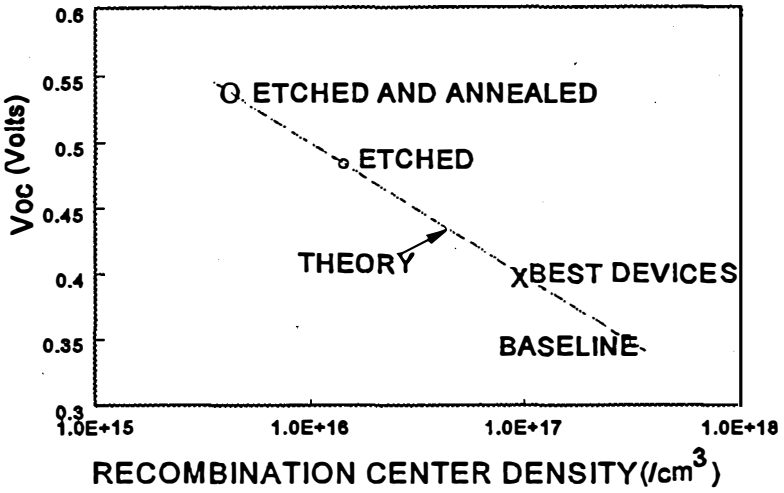


Figure 18. V_{oc} vs. recombination center density.

In recent experiments we have found that it is possible to decouple the effect of the etchant. Initial results with new etchants suggest that we are can reduce the harmful interface recombination centers without affecting the transport properties in the main space charge region. With further effort we expect to realize significant improvements in performance. In fact, in the example just cited if the original J_{sc} had been maintained, the$_{oc}$V would have risen to 530 mV as shown in figure 18(projection). Once this is accomplished with the etching procedure, we expect to apply the understanding which is developed toward modification of our deposition procedure so that these levels of performance can be accomplished without the extra etching step.

4.2.3 Prognosis

We have developed a simple process sequence which produces laboratory cell efficiencies in the 9-10% range. This process can easily be scaled-up with conventional processing equipment and should result in initial module efficiencies in the 7-8% range. The advancements in understanding which we have made provide a solid basis for nudging these efficiencies forward. We have already demonstrated increases in V_{oc} up toward the values of 12% devices from the literature. At the end of the project we developed techniques for maintaining and even improving other properties as we manipulate V_{oc}'s upward. We are confident that we will shortly be reporting efficiencies of 12%, and that the improvements will be accomplished within the constraints of our simplified process. This will then be the basis for a low cost, 10% module technology. Ongoing improvements in performance beyond this threshold can be expected. However, discipline and patience will be required to make those advancements within the low cost framework of the process.

5.0 ZnO

ZnO has become one of the most important transparent conductors for solar cell applications. Its properties are as good or better than other transparent conductors, and it can be deposited by a number of techniques. High quality ZnO films can be deposited by sputtering which is a favored manufacturing technology. However, the deposition rates are slow because ceramic targets are used. We have developed a sputtering technology for ZnO which uses Zn targets and thus can be much faster. The following is an outline of the technical results. Additional information can be found in Annual Reports I[1] and II[2] for this project and in the literature[6].

5.1 PROCESS DESCRIPTION

The fundamentals of our deposition process have been described previously[2]. Basically we reactively sputter zinc in an argon/oxygen environment using a 3" diameter DC magnetron. We dope with aluminum by adding Al pieces to the target and with fluorine through gaseous CF_4. Our substrates are 4" x 4" soda-lime glass.

5.2 PERFORMANCE

Since there is a tradeoff between electrical and optical properties due to free carrier effects and the need to optimize this tradeoff against a particular device, there is no single figure-of-merit to quote for performance.

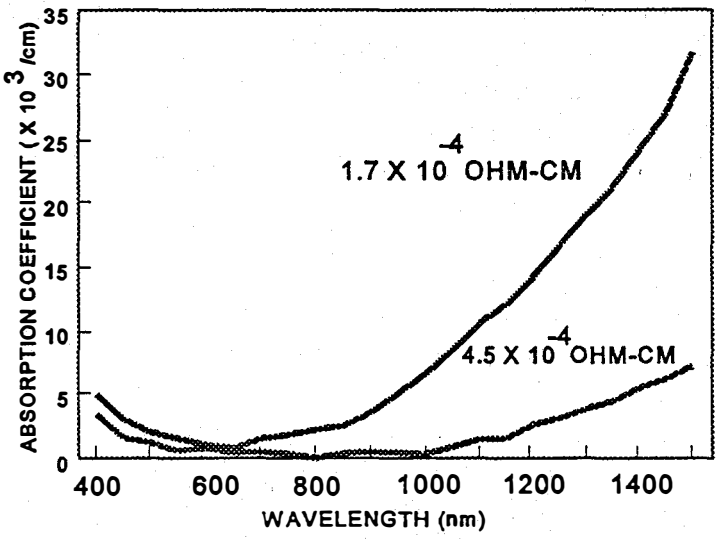


Figure 19. Absorption profile of ZnO.

We thus report that we can routinely achieve resistivities of 4.5 x 10^{-4} Ω-cm with good optical properties as shown in figure 19 and good uniformity as shown in figure 20. As seen in figure 20a, conductivity as well as uniformity is lost at lower substrate temperatures(T_{ss}),

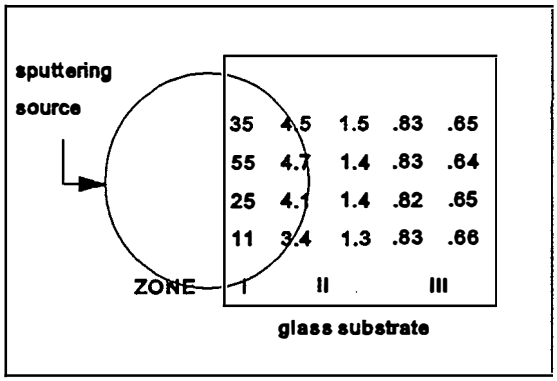


Figure 20a. Resistivity uniformity(value indicated x 10^{-3} Ω-cm) for reactively sputtered ZnO at T_{ss} = 150°C.

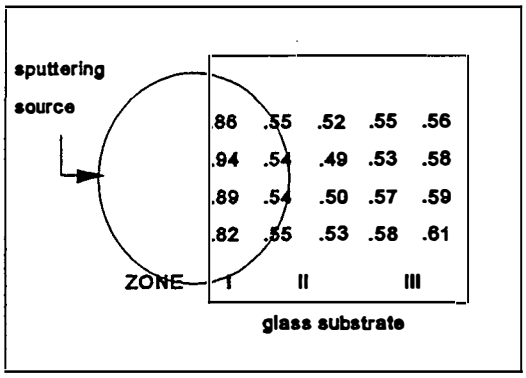


Figure 20b. Same as 20a. with T_{ss} = 350°C.

particularly in the vicinity of the target racetrack. By increasing the doping concentration we can lower the resistivity to 1.7 x 10^{-4} Ω-cm but suffer increased absorption losses(figure 19) due to free carrier effects. These performance parameters are as good as the best reported in the literature for ZnO made by any process. We are now at the point where performance is limited by physical fundamentals rather than by limitations imposed by the deposition process. We thus now focus our efforts on furthering the understanding of these fundamentals to determine how additional improvements in performance can be achieved.

5.3 FUNDAMENTAL MECHANISMS

To consider the effect of deposition conditions on the underlying fundamental mechanisms we have divided our 4" x 4" substrates into three zones as shown in figure 20. The substrate is intentionally offset relative to the target because of the known effects of bombardment, especially over the racetrack region. Thus film properties are generally found to vary according to Zone location and sputtering conditions. Zone I generally exhibits poorer properties because it is closest to the source and most affected by ion bombardment. However, the effects of bombardment are complex and can be manipulated to effect improved performance in Zone I.

Substrate temperature(T_{ss}) is found to have significant impact on performance. Various film properties as a function of T_{ss} and Zone position are shown in figures 21, 22, and 23. A key observation is the generally increasing doping efficiency with increasing T_{ss}. We have in fact achieved doping efficiencies of nearly 100% at doping concentrations of 1-2%.

A more subtle effect is the interplay between carrier concentration and mobility. We have

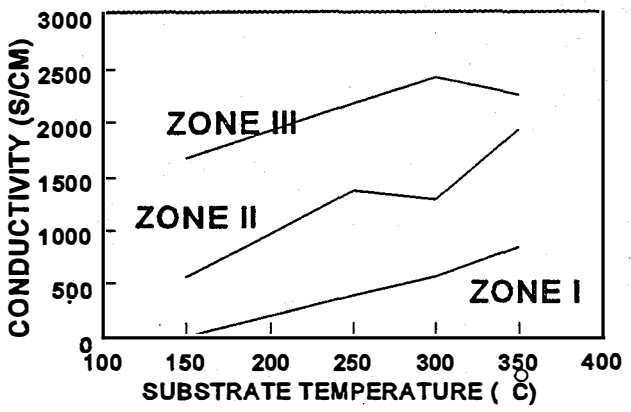


Figure 21. Conductivity versus substrate temperature for ZnO:Al.

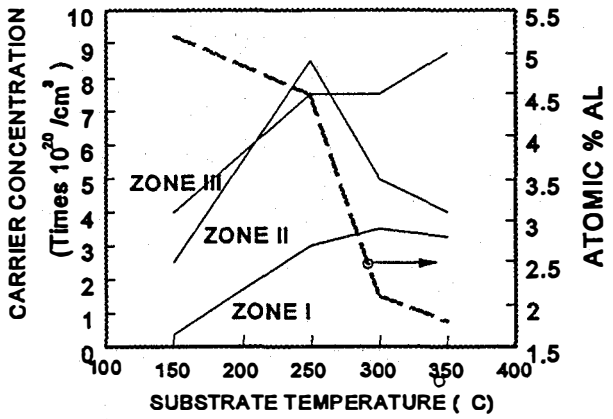


Figure 22. Carrier density and Al content versus substra temperature for ZnO:Al.

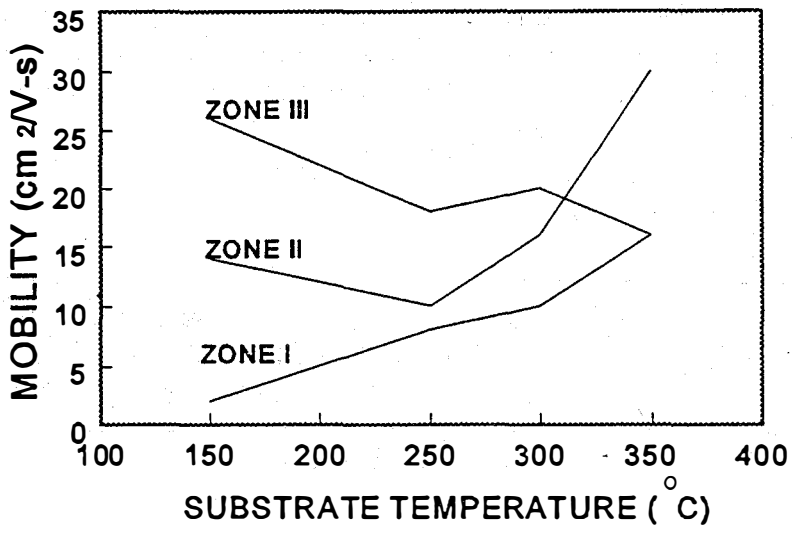


Figure 23. Mobility versus T_{ss} for ZnO:Al.

explained this and the rest of the data in terms of a transition from defect scattering to ionized impurity scattering as the doping concentration is increased[6b]. The implication of these results to solar cell applications of this technology are important. In addition to a tradeoff between deposition rate

and uniformity, the interplay of two fundamental mechanisms must guide our design considerations.

* Optical properties are dominated by free carrier mechanisms in the near IR and perhaps into the visible.

* Carrier concentration and mobility are correlated.

Thus for a target spectral range as determined by the absorber and for a required sheet rho as determined by the grid spacing or cell width there is an optimum choice for the doping level. Since this choice is a tradeoff between optics and conductivity, neither will be optimized. The insights which we have developed about these mechanisms can be used to guide the development of an optimized process. Meanwhile we and others are pursuing advanced doping techniques which may be able to circumvent these fundamental limits to performance.

PART II: CdTe

1.0 CELL FABRICATION PROCEDURE

The process sequence used for the fabrication of CdTe/CdS solar cells is given below. The main variations are in the glass substrate and the CdS deposition process. Several types of soda lime glass substrates (including SnO_2 coated glass courtesy of Libbey Owens Ford) and Corning 7059 borosilicate glass have been used for this work. The CdS films were prepared by chemical bath deposition (CBD), rf sputtering, or close spaced sublimation (CSS).

Fabrication steps:

1. Substrate preparation: varies depending on the type of substrate; more critical for the soda lime glass substrates.
2. SnO_2 deposition: R_{SH} = 7-10Ω/□ (including a thin resistive layer.)
3. CdS deposition: film thicknesses, (a) CBD: 700-1200Å, (b) rf sputtering: >1800-2000Å, (c) CSS: >600Å.
4. Annealing: in the presence of H_2 (occasionally in the presence of $CdCl_2$.)
5. CdTe deposition by CSS: substrate temperatures in the range of 460-630°C.
6. Post deposition heat treatment: in the presence of $CdCl_2$ (applied by dipping or evaporation.)
7. CdTe surface preparation: in a Br_2/CH_3OH or a $HNO_3:H_3PO_4$ solution.
8. Back contact formation: application and annealing of doped graphite paste.
9. Cell isolation.
10. Indium soldering on the SnO_2 around each device.

The baseline process for the fabrication of CdTe solar cells utilizes borosilicate glass substrates, CBD CdS, and CSS CdTe deposited at high temperatures (>550°C). For devices fabricated with soda lime glass substrates, all processes (in particular the CSS of CdTe) are carried out at temperatures below 550°C (in some cases even below 500°C). Results in this area have been very promising, with cell efficiencies exceeding 13%. Devices utilizing rf sputtered or CSS CdS were typically prepared on borosilicate glass. Solar cells fabricated with these two "types" of CdS exhibited state-of-the-art V_{OC}'s (>840 mV). However, devices prepared with CSS CdS demonstrated a better overall performance, and the potential of reaching efficiencies comparable to those achieved with CBD CdS. The following sections discuss in more detail the results obtained for the variations in processing mentioned above.

2.0 CADMIUM SULFIDE

Cadmium sulfide films deposited by CBD are successfully being used for the fabrication of high efficiency thin film solar cells (both CdTe and $CuInSe_2$). Even though this particular process is simple, rf sputtering and CSS were chosen as better candidates for large area manufacturing applications. A key issue is the deposition of thin (<1000Å) and pinhole free CdS films. This would lead to enhanced photocurrents without suffering losses in V_{OC}.

2.1 Chemical Bath Deposition

CBD CdS films are prepared in an aqueous solution that contains NH_4OH, cadmium acetate, ammonium acetate, and thiourea. The deposition is carried out at a temperature of 85-90°C. The PH of the solution as measured at the start of the process is about 9.2. During the deposition the solution is being continuously stirred. The deposition conditions are summarized in table I. More details about the process can be found elsewhere[7]. Slow deposition rates (10-20Å/min) help minimize the formation of CdS precipitates in the solution (homogeneous reaction). After the deposition the substrates are first rinsed with DI water ultrasonically to remove any CdS partriculates from the surface, and then rinsed under running DI water prior to being dried using compressed N_2. The resulting films are specular and free of any particulates (when observed under an optical microscope.) Figure 1 shows SEM micrographs of a CBD CdS film. The film consists of small grains (<0.1 micron). Figure 1a shows the formation of a rather large CdS "particles" on the surface of the film, while figure 1b shows what appears to be a pinhole. Such pinholes are not common for these films, and they are believed to be a result of a CdS particulate (such as the one in fig. 1a) that is removed during the ultrasonic cleaning of the substrates. For a particular set of conditions film thickness is controlled reproducibly within ±50Å depending on the reaction time. The maximum obtainable thickness is about 1000-1200Å. Figure 2 shows the CdS thickness as a function of time. For this particular deposition the substrates (5) were removed from the solution every ten minutes (the first substrate was removed after 15 minutes) and the thickness was measured using a thickness profilometer. Similar results have been obtained using cadmium and ammonium chloride.

Table I. CBD deposition

NH_4OH	0.2 - 0.5 M
CdAc	0.5 - 2.0 x 10^{-3} M
NH_4Ac	0.8 -1.2 x 10^{-2} M
Thiourea	1 - 4 x 10^{-3} M
Temperature	80 - 90°C
PH	9.1 - 9.2

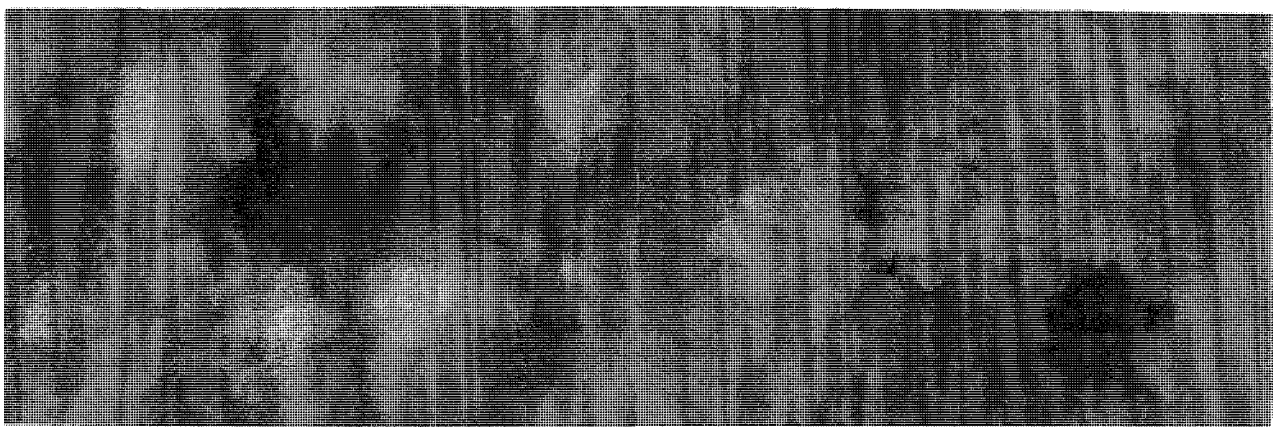


Figure 1a. SEM micrograph of CBD CdS.

Figure 1b. SEM micrograph of CBD CdS.

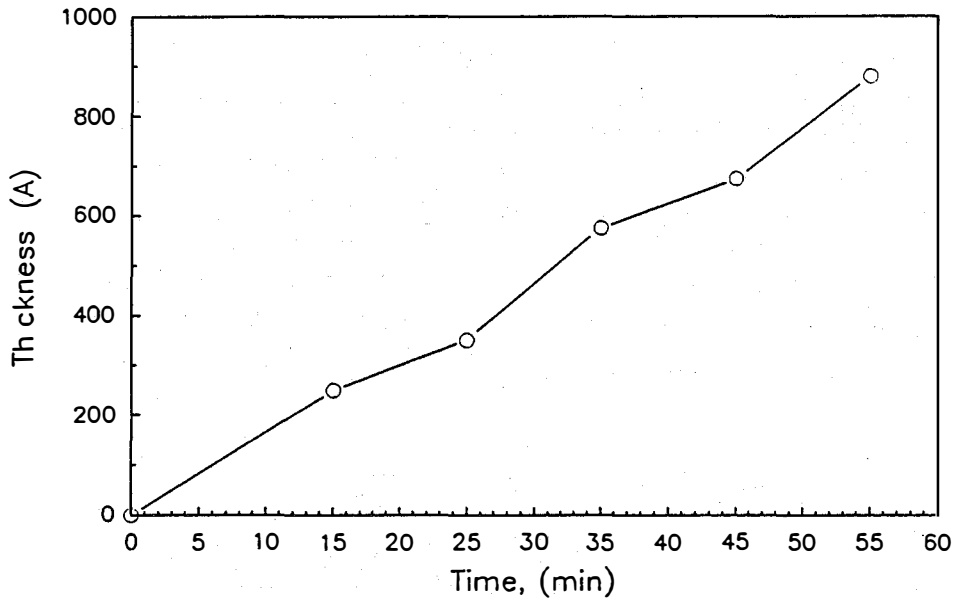


Figure 2. Thickness as a function of time during the CBD process.

2.2 Rf sputtering

The rf sputtered CdS films were deposited using a 3 inch Torus 3M magnetron gun and a 5N CdS target. Additional process details can be found in the Phase II report of this project[2]. Most depositions focused on varying the substrate temperature (150-400°C), which affects the sticking coefficient of the CdS, and the substrate-target distance which is critical in minimizing film damage due to ion bombardment. The deposition rate as a function of the substrate temperature is shown in figure 3. The effect of other process parameters on the deposition rate is shown in table II. The grain size was relatively small, 0.2-0.3 μm (this is larger than the grain size of the CBD CdS) and increased with increasing substrate temperature. From AFM studies the mean half widths of the CdS grains were 0.11 and 0.13 μm for substrate temperatures of 225 and 400°C respectively. The AFM images of the two films (prepared on SnO_2/7059 glass) are shown in figure 4.

From XRD measurements (MoKα radiation) carried out on a small number of films, only a peak located at 12.4° was detected. This could correspond to the (002) orientation of the hexagonal structure, (or the (111) orientation of the cubic structure.) The intensity of the x-ray peak increased by 50% as the substrate temperature was increased from 150 to 300°C. Even though a thorough study of the crystallographic properties of the rf sputtered CdS films was not carried out the above observations are in good agreement with the work of others[8]. Unlike the CBD CdS films that have a light yellow color, the rf sputtered films appeared slightly darker (more orange), possibly due to the higher concentration of S vacancies in the rf sputtered films.

Similar results can be obtained by varying the temperature profiles. Figures 10 and 11 show the substrate and source temperature as a function of time. For the first profile the substrate temperature is originally held at a higher temperature than the source; film growth is initiated by simultaneously increasing the source and decreasing the substrate temperature. This type of temperature profile can be used for enhancing the grain size; however, these films must be prepared at larger thicknesses to eliminate the large number of pinholes present. When a more "conventional" temperature profile is used such as the one shown in figure 11, the grain size decreases, and the grains are densely packed leading to a drastic decrease in pinhole density. The addition of O_2 has a similar effect on the film properties: the deposition and grain size rate decreases, and the film density increases.

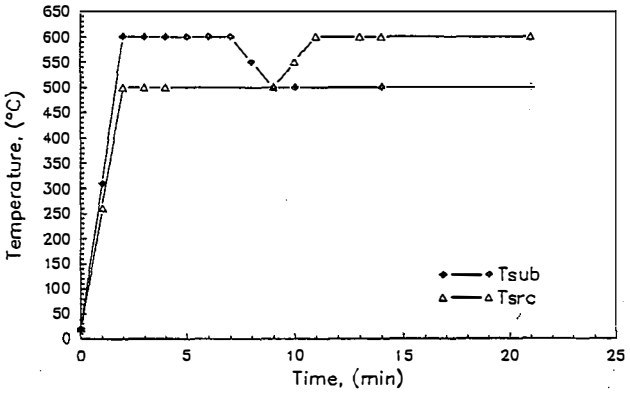


Figure 10. Temperature profile for film shown in 12a.

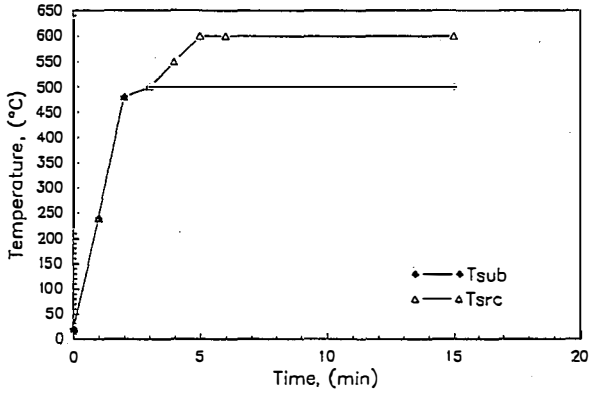


Figure 11. Temperature profile for film shown in 12b.

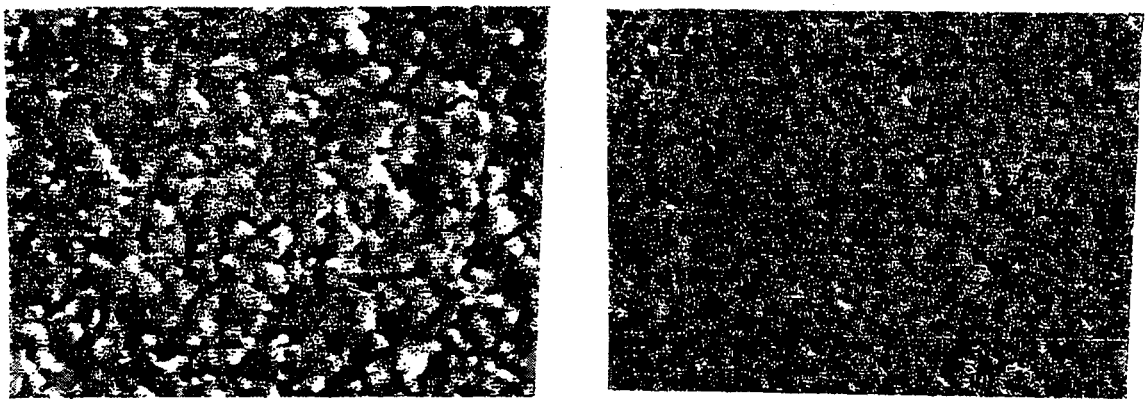


Figure 12. SEM micrographs for CdS films prepared with the temperature profiles shown in figures 10 and 11.

Solar cells prepared with rf sputtered CdS during the early stages of this work exhibited rather poor photovoltaic characteristics (device results will be discussed later). Varying the deposition conditions of the sputtering process had virtually no influence on cell performance, and therefore the focus was shifted to heat treatments. Common CdS heat treatments used for the fabrication of CdTe solar cells include annealing in H_2 or in the presence of $CdCl_2$. The heat treatments affect the optical, electrical, and structural properties of the CdS films[9].

2.2.1 Annealing Effects

A number of annealing experiments were carried out for CdS films deposited on 7059 glass and SnO_2/7059 glass substrates. The annealing temperatures were varied in the range of 350-450°C. The films were annealed in He, O_2, or H_2; the use of He or O_2 did not appear to improve solar cell performance and results were difficult to reproduce. In some cases a 4000-8000 Å $CdCl_2$ layer was evaporated onto the surface of the CdS prior to the heat treatment. The performance of solar cells prepared with such films did not improve, and often the films peeled after the CdTe deposition. This particular heat treatment will be revisited in the future since other researchers have found that it enhances solar cell performance. The focus during this work was placed on heat treatments in H_2, since these have been found to consistently improve solar cell performance. It should be noted that annealing of CBD CdS films in H_2 is a standard processing step for the fabrication of state-of-the-art devices[10].

It has been previously reported that annealing in H_2 reduces the dark resistivity of CBD CdS films.[] Rf sputtered films exhibited a very similar behavior. In order to measure the resistivity of CdS, the films were prepared on glass substrates to thicknesses in excess of 2000 Å. Indium was then soldered on the surface to form four collinear contacts. The resistivity was measured by passing current through the two outer contacts and measuring the voltage across the two inner ones, therefore eliminating any contact resistance effects. All as deposited films exhibited resistivities in the order of 10^6 Ω-cm, independent of the deposition temperature. It should be pointed out that this is the lateral resistivity and it is expected to be dominated by grain boundary effects. The resistivity in the thickness direction may be considerably lower than the lateral resistivity, based on results from shcottky barrier diodes[]. After annealing in H_2 the resistivity of the rf sputtered CdS decreased by about three orders of magnitude (10^2-10^3 Ω-cm). These results seem to suggest that the main effect of the heat treatment is passivation of the grain boundaries.

The mobility of rf sputtered CdS films deposited at different substrate temperatures and subjected to H_2 heat treatments in the range of 350-450°C is shown in figure 5. The films deposited at 150 and 300°C exhibit very similar behavior. At low annealing temperatures the mobility is less than 1 cm^2/V-s, and increases to 10-12 cm^2/V-s as the annealing temperature is increased to 450°C. The mobility of as deposited films was difficult to measure due to their high resistivity. The carrier concentration did no vary appreciably for

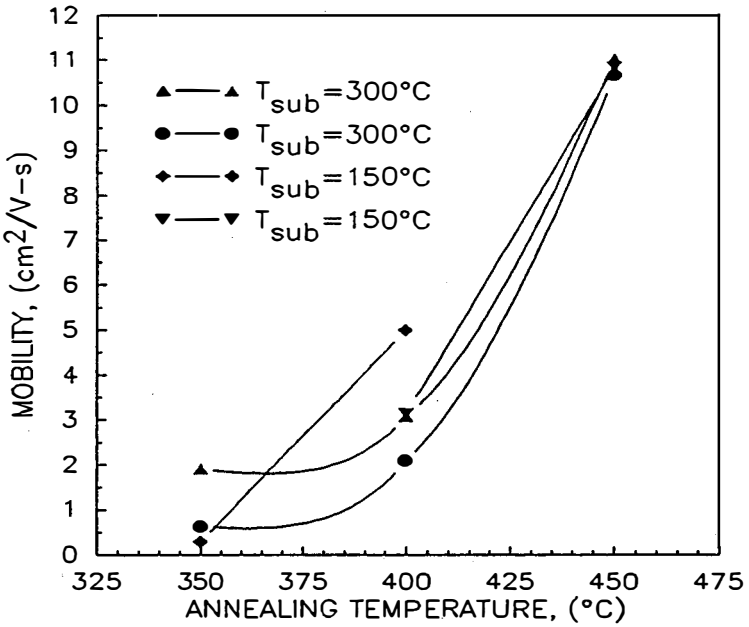


Figure 5. The mobility of rf sputtered CdS films annealed in H_2.

the range of annealing temperatures shown here, indicating that the increase in resistivity is mainly due to the increase in mobility.

2.3 CSS

The CSS process has been previously used for the deposition of several II-VI compounds, including CdTe, CdS, ZnS, ZnSe etc[12,13,14,15]. Source materials, typically in the form of pressed powder, have been used to deposit the above films on substrates ranging from single crystalline materials to glass. Ambients such as H_2, Ar, He, I_2, air, and O_2 have been utilized. A schematic of the reactor used for the deposition of the CSS CdS (and CdTe) films in this work is shown in figure 6. Two graphite plates (1.5 x 1.5 in) are being used to support the source and substrate. The graphite plates are heated using 2 kW tungsten halogen lamps. The source material and substrate are separated using quartz spacers of thickness 2-10 mm. The graphite plates, source, and substrate rest on a pair of quartz rods. Thermocouples are inserted into holes drilled to the side of each graphite plate for temperature monitoring and control. The system is equipped with a mechanical pump, and a gas supply inlet. The process is particularly attractive for thin film solar cell applications due to its simplicity and its high deposition rates. Cadmium sulfide films have been prepared for a wide range of deposition conditions. A summary of the process conditions is provided in table III.

Table III. CSS CdS process summary.

Substrate Temperature	300 - 500 °C
Source Temperature	550 - 650 °C
Pressure	1-100 torr
Ambient	He, H_2, O_2

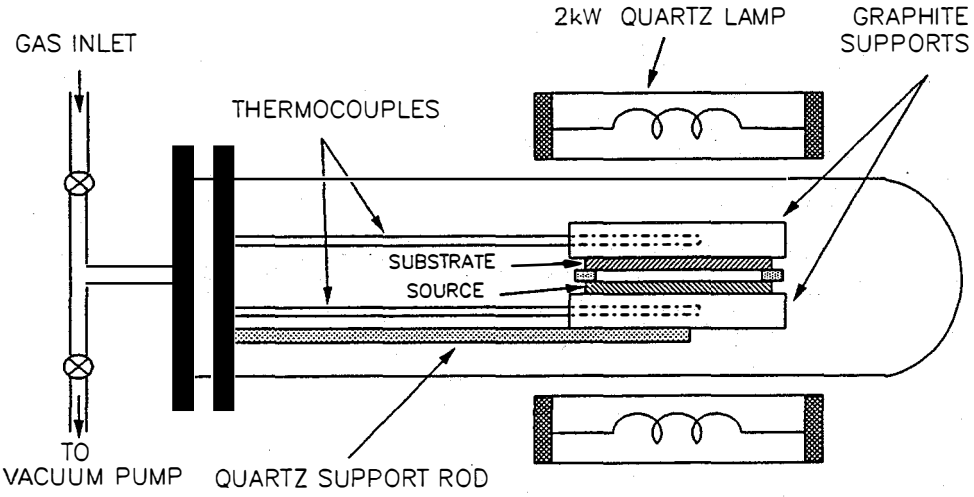


Figure 6. Schematic diagram of the CSS reactor.

In most of the previously reported work the substrate temperatures were in excess of 600°C. Since one of the major objectives for this work is to limit processing temperatures below 550°C in order to utilize soda lime glass substrates the substrate temperature for CSS CdS films was also limited to low temperatures.

Figures 7 & 8 show the deposition rates of CSS CdS films as a function of the source temperature for substrate temperatures of 450 and 500 °C respectively. As mentioned earlier, high deposition rates are easily obtained with this process. For this work the deposition rates were maintained in a range that would allow thickness control within $\pm$50 Å. Total deposition times varied from 2 - 10 min for film thicknesses of 500 - 2000 Å.

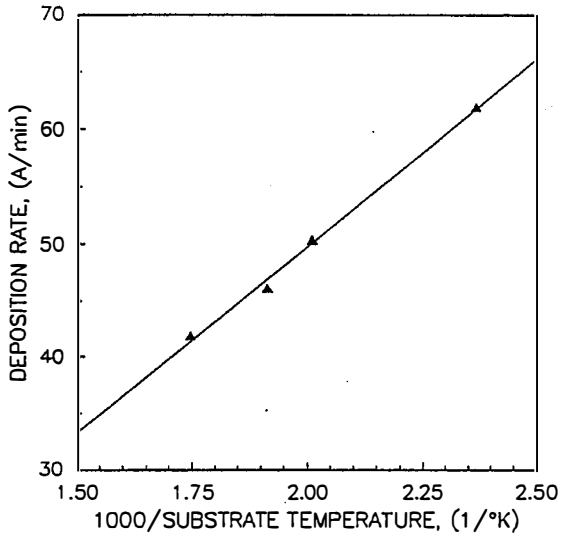


Figure 3. The deposition rate of rf sputtered CdS films as a function of substrate temperature.

Table II. Growth rate of rf sputtered CdS.

Distance (in)	T_{SUB} (°C)	Growth Rate (Å/min)
6.5	300	42
4.5	300	156
6.5	150	62
4.5	150	200

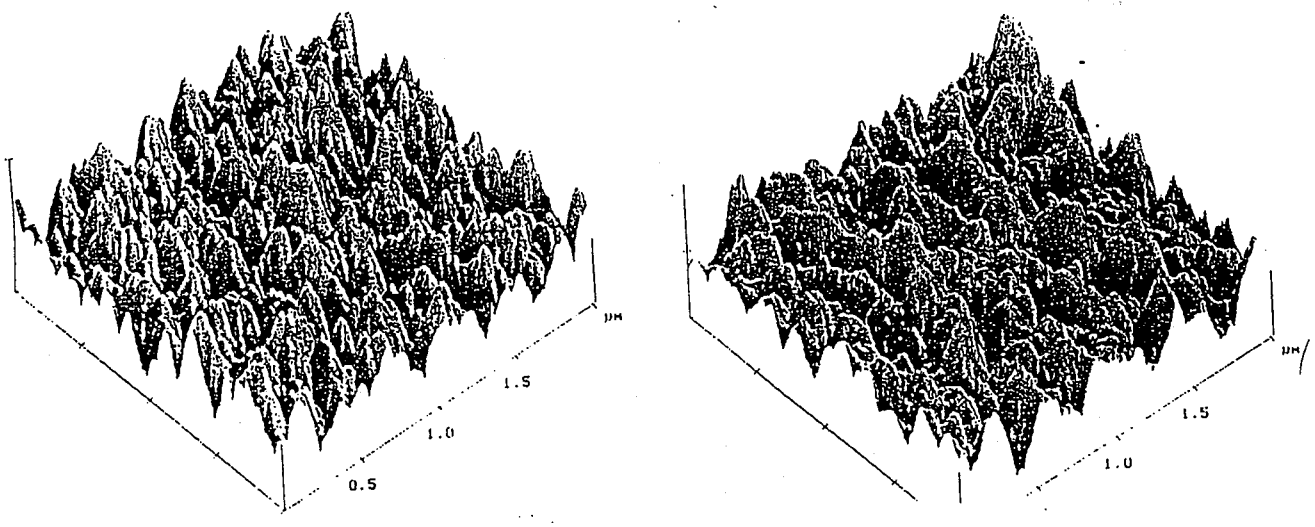


Figure 4. AFM images for rf sputtered CdS deposited at (a) 225 and (b) 400 °C substrate temperatures.

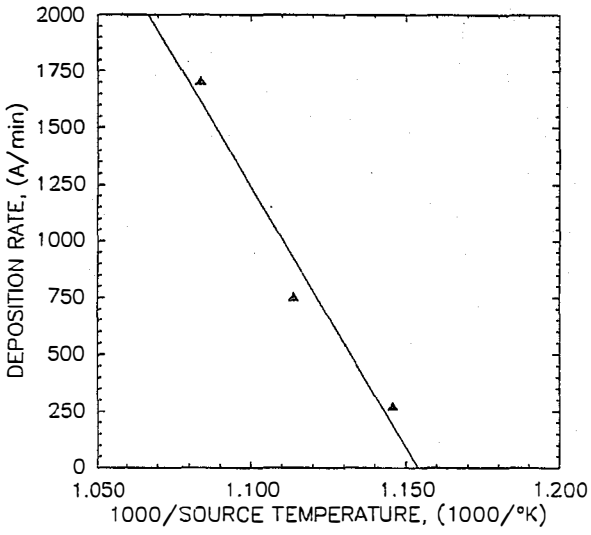


Figure 7. The growth rate of CSS CdS vs the source temperature. T_{SUB}=450°C

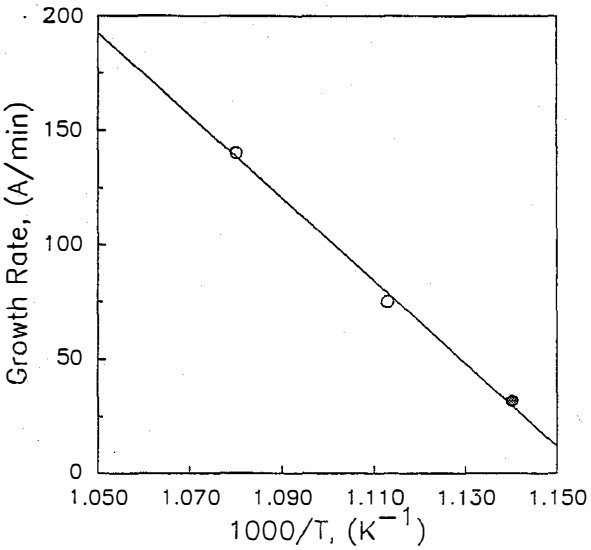


Figure 8. The growth rate of CSS CdS vs the source temperature; T_{SUB} = 450°C.

Unlike the CBD and sputtered CdS films for which the grain size was limited to 0.2-0.3μm, this process yielded a wide range of grain sizes ranging from tenths of microns to over a micron. The substrate temperature, total pressure, ambient, and particular temperature profile used can affect the grain size. Since the main objective is to deposit these films at small thicknesses (1000 Å) emphasis was placed on obtaining relatively small grain sizes and dense films. Figure 9 shows the SEM micrographs of two CSS CdS films prepared at a substrate temperature of 450°C and a pressure of 1 and 5 torr respectively. The grain size decreases and the films become more dense as the pressure increases. Both films were prepared in a He ambient.

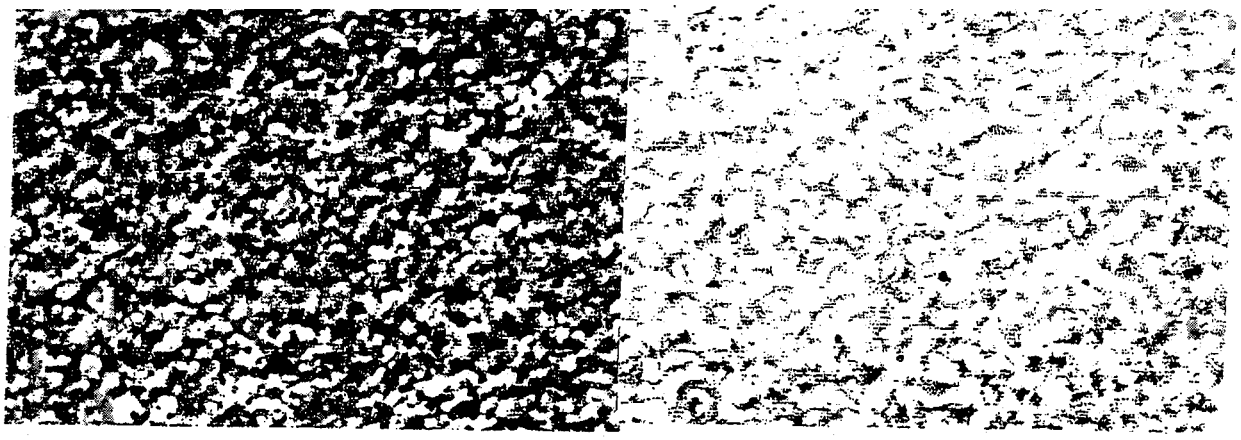


Figure 9. SEM micrographs of CSS CdS prepared in a He ambient at a substrate temperature of 450°C. (a) p=1 torr, and (b) p=5 torr.

3.0 CSS CdTe

The most efficient CdTe solar cells to date were prepared on borosilicate glass substrates due to the high deposition temperatures used during the CSS CdTe process (600°C). However, for low cost module production the substrate of choice is soda lime silicate glass. In order to transfer the high efficiency process to this type of substrate it is necessary to first lower all processing temperatures (at least) below 550°C; the thermal expansion coefficient of soda lime glass is two times higher than that of borosilicate, and its strain, annealing, and softening point temperatures are about 120-150°C, lower. Another problem that could arise from processing soda lime glass at high temperatures is impurity outdiffusion, that could lead to the degradation of the electrical junction.

An attempt was first made to optimize the CSS CdTe process at low substrate temperatures by fabricating cells on 7059 glass substrates. As it has been previously reported the solar cell performance degraded (in particular V_{OC} due to increased shunting) as the CSS deposition temperature decreased below 550°C. More details about SEM and XRD studies have been provided in the Phase II annual report[2]. Briefly, as the substrate temperature was lowered below 550°C the crystallographic orientation of the CdTe changed from preferential along the (111) direction (600°C), to random (550°C), to preferential along the (200) direction (500°C). The grains appeared to be joined at the substrate surface but "grew apart" as the film thickness increased. This dramatically increased the surface roughness of the CdTe films. The increased surface roughness is believed to have had a negative impact on the back contact process, in particular the chemical treatment step. In order to improve the structural properties of the low temperature CdTe all other process conditions (spacing, total pressure, source temperature etc.) had to be modified. SEM micrographs of CSS CdTe prepared at different temperatures are shown in figures 13 through 18; in some cases the corresponding V_{OC} and FF are also shown. All these films/devices were prepared on 7059 glass.

Once a set of conditions that would yield V_{OC}'s in excess of 800 mV were established several types of soda lime glass were incorporated into the process. This transition was not trivial as each type of substrate behaved differently. Visible defects, blistering, and in the worst cases film peeling occurred for certain types of the soda lime glass substrates. Most work focused on commercial 2.5-3.0 mm SnO_2 coated soda lime glass.

Figure 13. CSS CdTe; T_{SUB}=600°C

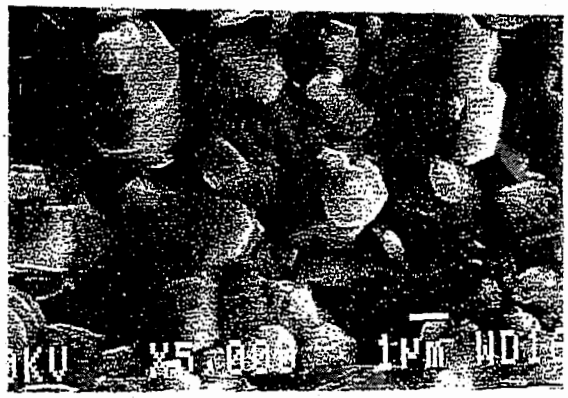


Figure 14. CSS CdTe; T_{SUB}=500°C.

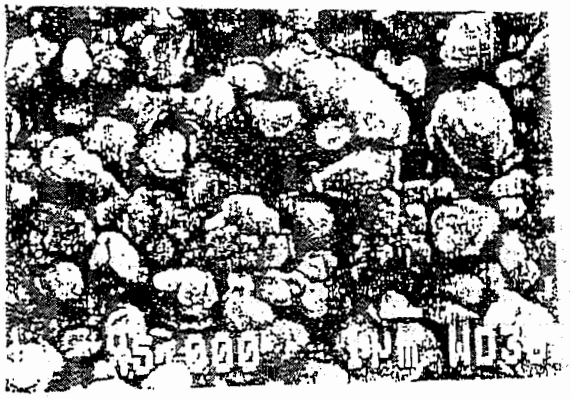


Figure 15. CSS CdTe; T_{SUB}=460°C
V_{OC}=820 mV, FF=68%

Figure 16. CSS CdTe; T_{SUB}=460°C
V_{OC}=820 mV, FF=66%

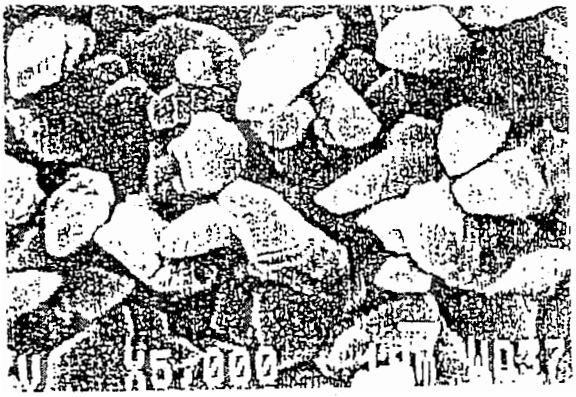


Figure 17. CSS CdTe; T_{SUB}=500°C
V_{OC}=830 mV, FF=68%

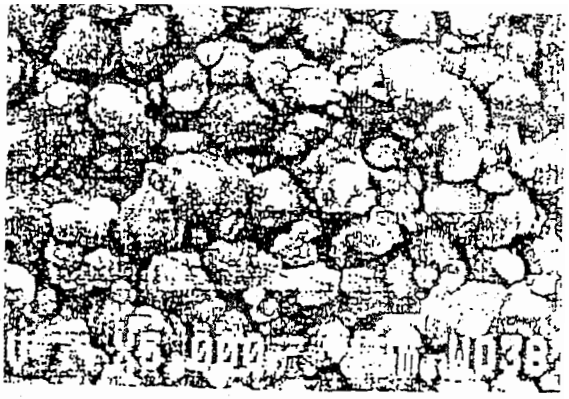


Figure 18. CSS CdTe; T_{SUB}=500°
V_{OC}=830 mV, FF=66%

4.0 SOLAR CELLS

This section discusses the performance of CdTe/CdS solar cells fabricated with the processes described above. Light and dark I-V, J_{SC}-V_{OC}, C-V, and SR measurements are routinely performed in order to characterize the devices and identify the key processing steps that will lead in further enhancement of solar cell efficiencies. Maybe the single most important factor affecting solar cell performance is the CdTe/CdS interface. It appears that efficiencies are enhanced by moving the electrical junction away from the metallurgical junction. This shift of the electrical junction away from the metallurgical interface is a result of S (Te) diffusion into the CdTe (CdS). Since the degree of interdiffusion is a function of a large number of variables, such as the CdS grain size, deposition temperatures, heat treatments etc, achieving this in a controlled manner is not trivial.

4.1 CdTe/CdS(rf sputtering) Solar Cells

The photovoltaic properties of solar cells fabricated using as deposited rf sputtered CdS were rather poor. The open-circuit voltage which is usually used as a guide to evaluate and optimize most of the fabrication procedures was less than 800 mV. This lead to the H_2 heat treatments discussed in a previous section. Table IV summarizes the effect of H_2 on V_{OC}. The best results were obtained for 400°C annealing temperatures. Occasionally, the same V_{OC} performance could be achieved at 450°C but results at this temperatures were not easily reproducible. It should also be noted that the minimum thickness of the CdS films for achieving V_{OC}'s in excess of 800 mV was about 1800-2000 Å.

Table IV. Effect of H_2 annealing on V_{OC}.

Deposition T (°C)	Annealing T (°C)	V_{OC} (mV)
150	400	850
150	450	820
300	450	830
300	None	800

An interesting feature of these devices is shown in figure 19. The turn-on voltage of the dark I-V is shifted to a value of about 1.5-1.6 Volts. Even though this behavior is often present in CdTe devices fabricated with CBD or CSS CdS, the voltage shift in this case appears to be the greatest. Under short wavelength illumination conditions (i.e. < 500 nm) the dark I-V turns on at lower voltages 0.8-0.9 suggesting that the mechanism responsible for this shift is located at the front of the device (i.e. in the vicinity of the CdS layer.)

The spectral response for a number of CdTe/CdS(rf sputtered) devices is shown in figure 20. The CdS films have been annealed in H_2 at different temperatures. For a true heterojunction one would expect the SR to decrease near 510 nm (the wavelength corresponding to the CdS energy gap) and not at 600 nm as indicated in this figure. Even though this roll off at 600 nm is not unique to these devices (also present for CBD and CSS CdS), it is by far the most pronounced resulting in considerable reduction in J_{SC}. Increasing

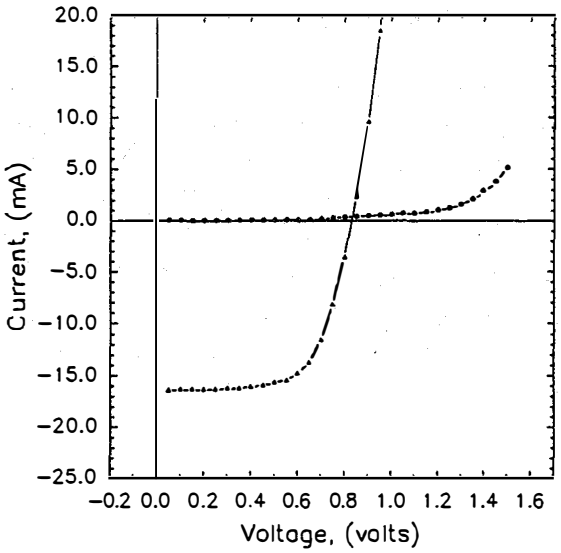


Figure 19. Dark and light I-V of a CdTe/CdS(rf) solar cell.

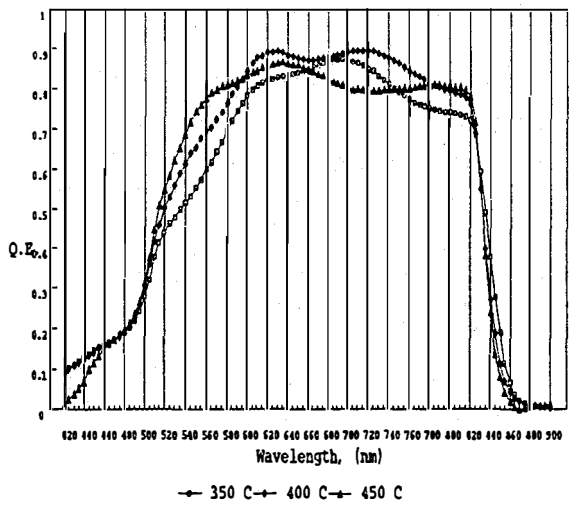


Figure 20. The SR of solar cells prepared with rf sputtered CdS.

the annealing temperature appears to enhance the SR in this region (500-600nm). A possible explanation is that the density of the CdS increases with annealing temperature limiting the degree of interdiffusion at the CdTe/CdS interface. The best solar cell fabricated with rf sputtered CdS exhibited a conversion efficiency of 11.6% (V_{OC}=843 mV, J_{SC}=20.6 mA/cm^2, ff=67%).

4.2 CdTe/CdS(CSS) Solar Cells

Solar cells fabricated with CSS CdS exhibited V_{OC}'s in excess of 840 mV and ff's over 74%. Table V lists some of the better devices fabricated to date. Based on this results it appears that devices fabricated by the CSS (both CdTe and CdS) can reach even higher efficiencies by increasing J_{SC}. Future work in this area will emphasize the optimization of thin (600-700Å) CSS CdS films.

The SR of several CdTe/CdS(CSS) solar cells is shown in figure 21. The responses have been shifted by 10 units along the Q.E. axis for clarity. The V_{OC}'s for these cells from top to bottom are 600, 841, and 833 mV respectively. The low V_{OC} device exhibits a sharp drop off at about 500 nm (CdS energy gap.) The high V_{OC} cells exhibit a sharp drop at the CdS bandedge but they also show a distinct roll off that begins at longer wavelengths of about 550 and 600 nm. This behavior of the SR in the 550-600 nm region is being attributed to the interdiffusion between the CdS and CdTe as mentioned in a previous section, and the results presented here seem to suggest that "some" interdiffusion is necessary in order to achieve high V_{OC}'s.

Table V. Solar cells prepared with CSS CdS.

Sample #	214A	812B	2187A
Eff. (%)	12.93	11.7	12.52
V_{OC}, (mV)	833	852	838
J_{SC}, (mA/cm^2)	21	19.5	21.33
ff	74.08	70.6	70

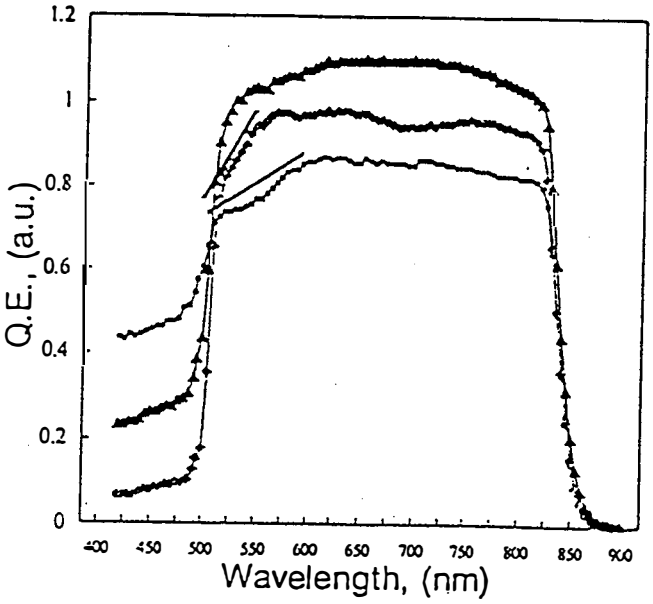


Figure 21. The SR of CdTe/CdS(CSS) solar cells.

4.3 CdTe/CdS Cells on Soda Lime Glass Substrates

Once the properties of the CSS CdTe films prepared at low temperatures was improved as already discussed in the "CSS CdTe" section, solar cells were fabricated on soda lime glass substrates. Solar cells with high V_{OC}'s (>840 mV) and high ff's (>70%) were prepared on soda lime glass for temperatures as low as 460-480°C. Most cells are being fabricated at temperatures in the 540-560°C range. The efficiencies of these devices are limited by low J_{SC}'s mainly due to the poor optical properties of the glass. A summary of some of the better cells measured under AM1.5 conditions at the National Renewable Energy Laboratory is provided in table VI.

Figure 22 shows the carrier concetration obtained from C-V measurements for two devices prepared at different substrate temperatures (both temperatures were below 560°C.) The hole distribution for the device prepared at the low substrate temperature is uniform and approximately 1 x 10^{14} cm^{-3}. The carrier concentration in the high temperature device increases slightly from 5 x 10^{13} to 1.8 x 10^{14} cm^{-3} with increasing reverse bias. Figure 23 shows the

Table VI. Solar cells fabricated on soda lime glass substrates.

Sample #	213A3	41B21	41B11
T_{SUB} (°C)	460	460	460
Eff., (%)	13.2	13.3	13.5
V_{OC}, (mV)	851	851	850
J_{SC}, (mA/cm$_2$)	20.6	21.5	21.45
FF	74.9	72.6	73.8

capacitance vs frequency data for the same two cells. The dispersion is clearly higher for the device prepared at the low substrate temperature. The larger difference between the high and low frequency capacitance of the low T device suggests the concentration of interface states is higher for this device. The high T device slightly outperforms the low temperature one: High T: V_{OC}=847 mV, J_{SC}=21.4 mA/cm$_2$, FF=72.5 %; low T: V_{OC}=830 mV, J_{SC}=20.6 mA/cm$_2$, FF= 70.4%

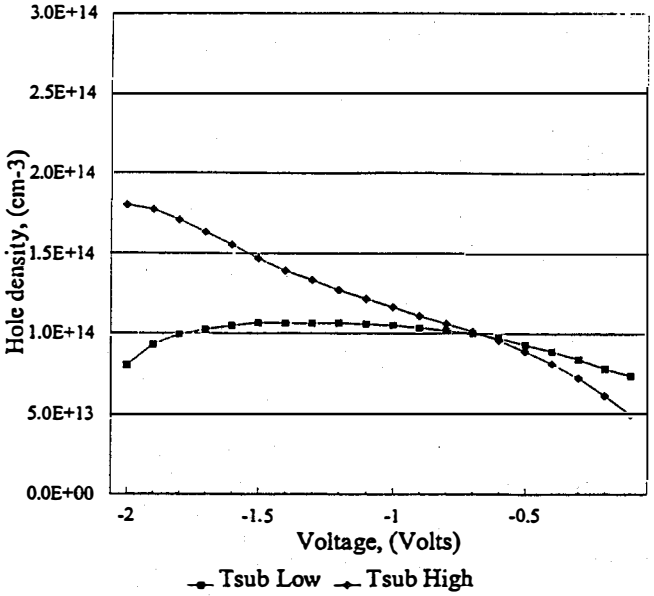


Figure 22. Carrier concentration profiles for low and high T_{SUB} samples.

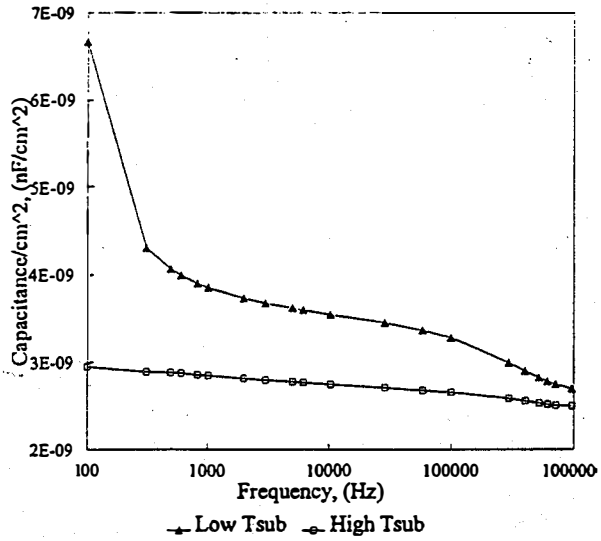


Figure 23. Capacitance vs frequency for the samples of figure 22.

The efficiencies of cells fabricated on soda lime glass (LOF) are currently over 13%. The process appears to be robust and most efforts are directed towards improving J_{SC}. Figure 24 shows the SR of a number of devices prepared using CdS films of several thicknesses. The QE at 450 nm is in some cases greater than 70%. However the V_{OC} and ff for these devices is less than 800 mV and ff in the mid 60's. Figure 25 shows the variation of V_{OC} and FF as a function of the QE at 450 nm. As the QE increases beyond 60% both V_{OC} and FF decrease considerably. Based on the current status of this work efficiencies over 14% on soda lime glass substrates can be achieved in the near future.

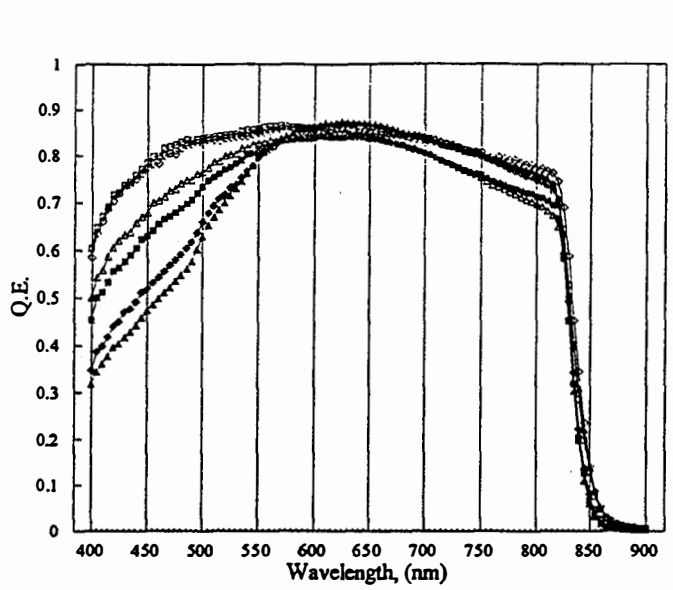


Figure 24. The SR of solar cells prepared on soda lime glass using CdS of various thicknesses.

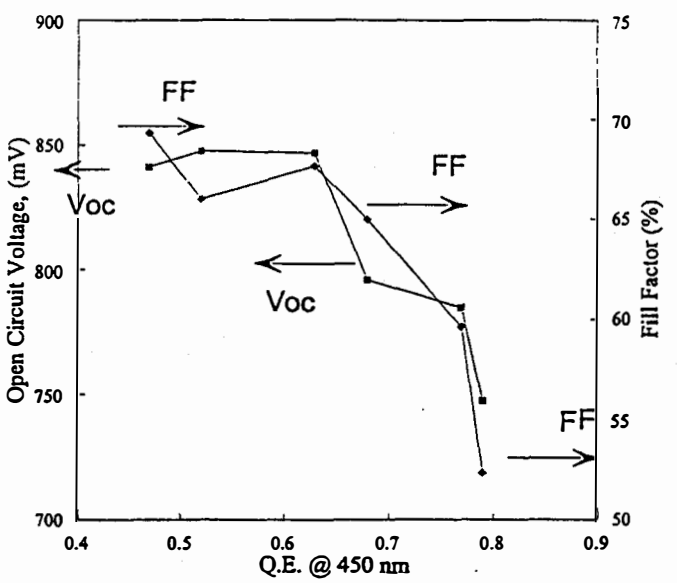


Figure 25. V_{OC} and FF vs the QE at 450 nm for the cells shown in 24.

Appendix A

CdS Deposition

Junction formation consists of chemical bath deposition(CBD) of a thin CdS layer. The solution contains 0.015 molar cadmium acetate, 0.15 molar thiourea, and 0.15 molar ammonium hydroxide in DI water. Once the solution is formed, the substrate is lowered on a glass holder until it is completely immersed. The temperature is slowly raised to 70° C while continually stirring with a magnetic stirrer. As the temperature of the bath approaches 70°, the CdS layer plates out on the CIS surface over a period of 3 - 5 minutes. A new solution is made for each substrate, and by controlling the deposition time the same approximate thickness can be reproduced each time. The resulting CdS thickness is about 200Å . Variations in the surface roughness of the CIS have been found to alter the deposition rate of the CdS and must be accounted for when high precision is sought.

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13. ABSTRACT *(Maximum 200 words)*

This report describes work performed by the University of South Florida to develop a manufacturing-friendly fabrication process for $CuInSe_2$ (CIS) solar cells. The process developed under this project uses conventional deposition processes and equipment, does not require stringent process control, and uses elemental Se as the selenium source. We believe it can be readily scaled up using off-the-shelf processing equipment and that it will meet the low manufacturing-cost objectives. Another significant achievement under this project was the development of a reactive sputtering deposition technology for ZnO. ZnO is used in many solar cell devices, and sputtering is a desirable manufacturing technology. The application of sputtering has been limited because conventional deposition uses ceramic targets that result in low sputtering rates. The use of Zn metal as the target in reactive sputtering overcomes this limitation. We have demonstrated that ZnO deposited by reactive sputtering has state-of-the-art opto-electronic properties. These developments result in large-area uniformity and optimized performance and provide a significant opportunity for applying and commercializing the technology.

The second objective of this project was to fabricated high-efficiency CdTe solar cells using manufacturing-friendly processes. Three deposition processes were used to deposit CdS films: chemical bath deposition, rf sputtering, and close-spaced sublimation (CSS). The CdTe films were deposited by CSS. A cell with a record efficiency of 15.8% was obtained.

14. SUBJECT TERMS

processing ; high efficiency ; thin films ; copper indium diselenide ; cadmium telluride ; photovoltaics ; solar cells ; deposition ; sputtering ; zinc oxide ; cadmium sulfide

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