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Technology Support for Initiation of High-Throughput Processing of Thin-Film CdTe PV Modules

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Abstract

During the first phase of this subcontract, progress has been made in the important areas of stability, advanced deposition techniques, efficiency, the back contact, no-contact film diagnostics (photoluminescence) and cadmium waste control. The progress in stability has been in both the demonstration of devices maintaining at least 90% of the initial efficiency for over 19,000 hours of continuous light soak and the development of methods which can accurately predict long term behavior based on the first 5,000 - 10,000 hours of life. Experiments were conducted to determine if device behavior could be accelerated with thermal or voltage stresses. Notable achievements in advancing the state of the art in deposition technology include depositing CdTe on a 3600 cm^2 substrate at 600 torr and designing and fabricating a new deposition feed system with a remote semiconductor source. Mathematical modeling of the deposition has permitted a more rapid development of a large area coater. The efficiency has been increased on small area devices to 13.3% by decreasing the thickness of the CdS and of the glass substrate. Work also focused on using a high resistivity SnO_2 buffer layer between the TCO and thin CdS to help preserve the open-circuit voltage while increasing the current-density. The back contacting process has been simplified by replacing the wet post-deposition etch with a vapor Te deposition step on small area devices. Results show that the devices perform comparably in efficiency but better in stability under light-soaking and open-circuit conditions. Preliminary studies of the correlation between CdS photoluminescence after the chloride treatment and the final device efficiency have shown a positive correlation which may be applicable for in-line quality control. The final area of progress was through the successful demonstration of preventing at least 99.9% of all incoming Cd from leaving in an uncontrolled manner through the land, air or water.

Introduction

SCI was formed in 1987 to be a vertically integrated manufacturer of multi-megawatt solar electric generating fields. Manufacturing of thin film photovoltaic modules is one part of this mission. In late 1990, SCI began a program to investigate the viability of producing these modules using CdTe based films deposited from elemental vapors onto high temperature superstrates. CdTe was selected as the principal semiconductor layer due to its record of high efficiency, its device stability, and its flexibility with respect to its method of deposition [1]. This flexibility allows SCI the freedom to independently choose a manufacturing method based on attributes of low cost, high throughput, and reliability, and then to adapt that process to the deposition of CdTe based photovoltaic films. Close spaced sublimation (CSS) was chosen due to its high deposition rate and its demonstrated capability to produce state of the art efficiency devices [2-5].

SCI has made several notable accomplishments from both research and manufacturing perspectives. The pilot-production scale deposition system has produced a 7200 cm^2 total area module with an output of 60.5 W and a total area efficiency of 8.34% and routinely produces modules in the 7.5 - 8.0 % total area efficiency range. This has given the capability to install over 50 kW of outdoor arrays for testing in both remote and grid-connected power production configurations. The research efforts have concentrated on refining the manufacturing process for high throughput manufacturing. There has been a concerted effort to reduce the number of wet processing steps by replacement with dry processing or by complete elimination. For example, SCI successfully developed an alternative to the solution applied $CdCl_2$ post-deposition heat-treatment using a vapor HCl treatment with similar time and temperature parameters. There is continuing effort to minimize the chloride treatment time and implement a continuous manufacturing process. The need to evolve from a batch process for material and substrate loading has also prompted research on alternative feed methods as well as work on increasing the ambient deposition pressure to atmospheric to negate the need for vacuum seals or load locks.

Device research has been focused primarily in three areas 1) stability, 2) back contact optimization and 3) efficiency improvement. The stability work has primarily concentrated on documenting the stability of the present preferred manufacturing product as well as testing innovative device designs on the laboratory scale. The stability is evaluated by means of accelerated testing protocols where similarly fabricated devices are evaluated using combinations of illumination, temperature and bias. The test allows for comparison among different device structures as well as the comparison of performance to actual field operation data. Successful implementation and evaluation of these tests permits a high confidence level that the manufactured product will meet warranty requirements.

Tied very closely to stability is the processing required to form a low resistance contact to the CdTe. This has historically been an area of difficulty. The present state of knowledge is that an interfacial layer (IFL) between the CdTe and metal contact is needed. This IFL facilitates the electrical transition from the CdTe, which has a high work function and almost always has a low carrier density. Several standard techniques are used to form this IFL including various etching and/or "doping" procedures which introduce either Cu or HgTe at the interface. Most etching procedures leave a Te-rich surface on the CdTe. Work at SCI has focused on both optimizing the IFL for initial performance and stability while simultaneously eliminating the wet processing steps. Devices made with a rf-sputtered IFL of Te and Cu have performance and stability equal to or better than the standard process.

The SCI standard manufacturing process produces devices with short-circuit current density of approximately 17.6 mA/cm^2 which is about 13 mA/cm^2 lower than the theoretical maximum of 30.5 mA/cm^2. The primary strategy for improving the current collection has been to decrease the CdS thickness

so as to maximize the blue photon absorption in the CdTe. The experiments have focused on developing techniques specific to SCI devices which permit the increased collection efficiency without reducing the voltage output. The techniques have included subtle process variations as well as the addition of an intrinsic SnO_2 prior to CdS deposition.

Stability

Photovoltaic module manufacturers must assure customers about the long-term power-delivery capability of their product. In the absence of extensive field history, methods of accelerated testing are needed. In addition, process development requires techniques to rapidly compare module stability differences resulting from process changes. Correlation of the results of accelerated tests and behavior in the field is complex but necessary.

Many CdTe/CdS fabrication techniques are known. Some of these techniques result in devices with good stability. When observed, instability is usually attributed to the contact to p^--CdTe [6-8]. While recent reports on CdTe module performance [9-12] have been encouraging, the data is limited and a more comprehensive testing methodology is needed.

The first stage of our protocol includes subjecting sub-modules to combinations of continuous illumination, temperature, and bias at indoor test stations. This section presents the results from the first 2.5 years of these tests.

Stability testing procedure

Most of the devices used in our life tests have been interconnected sub-modules (6 cells, aperture area ~ 48 cm^2), but individual cells (1 cm^2), 7200 cm^2 modules, and outdoor arrays have also provided supporting evidence. Sets of sub-modules were made by completely processing 7200 cm^2 substrates followed by cleavage into the sub-module size. Each set contained from 20 to 45 samples depending on cleavage and encapsulation yield and minimum initial performance requirements. Most of the sub-modules were then encapsulated using EVA and glass. Thus the sub-modules from a particular set are as identical as possible.

The members of a particular set were distributed amongst the various stress conditions listed in Table 1. The test most similar to the field environment, continuous light soaking with resistive-load, was more heavily weighted. The duration of each test was 5000 to 20000 continuous hours.

Periodically during each stress test, samples were removed, cooled to room temperature, and their performance measured on a solar simulator system. The simulator illumination source is an Optical Radiation Corp. model 1000 continuous, intensity-regulated, Xenon arc-lamp system (ASTM E927 class B compliant). The measurement system consists of a Kepco model BOP 100-1M four-quadrant power supply, a Keithley model 1601 12 bit A/D and D/A interface card, a 10 Ohm current sensing resistor, and an Intel-486-based computer. We calibrate the illumination source daily using a group of encapsulated CdTe sub-modules that are periodically measured at NREL with the X-25 system. The current-voltage curves were acquired at a voltage sweep rate of +1.5 V/s with a 2 s delay between module illumination and the start of the forward voltage sweep.

Table 1. Summary of Test Conditions.

Illumination	Temperature (°C)	Bias
815 W/m^2	55 *	Open Circuit
700 W/m^2	75	Short Circuit
	90	Resistive Load
Dark	25	+0.5 V/cell
	60	Zero
	100	-0.5 V/cell
	140	

* Nominal temperature

Several stress-test stations were used in this work. The illumination test station consists of a metal-halide lamp array (Phillips MH1000/U 1000 watt bulbs in Lithonia THP-A22 fixtures) mounted 0.85 m above the plane of the samples. The resulting illumination intensity was ~0.8 kW/m^2 with a ± 10% spatial uniformity. At uncontrolled locations, the typical sample temperature is 50 to 60 °C. Glass-covered boxes equipped with convective heaters and forced-air recirculation provided elevated, controlled sample temperatures during light soaking of 75 ± 2 °C and 90 ± 2 °C. Within the elevated temperature boxes, the illumination intensity was approximately 14% lower with similar spatial uniformity. In the light soaking with load tests, fixed resistors (30 ohm) were used to provided an approximate maximum power point bias. The dark-thermal test station consists of a series of N_2-purged ovens equipped with biasing power supplies set to provide ± 0.5 volts per cell.

Results

An empirical and statistical analysis of the efficiency versus time behavior has been the focus of the present approach. Using the various stress conditions, we concentrated on comparing different fabrication recipes. Devices made by many alternative processes show similar types of responses, although the magnitudes of the device changes are process dependent.

Two time windows describe the efficiency versus time-in-test behavior of most devices. During the early stages of device testing (<2000 hrs.), notable changes can occur. For example, small performance decreases following EVA lamination and improvements during early light soaking commonly occur. The early changes due to light soaking, including small shifts in open circuit voltage and reductions in apparent series resistance ($[dV/dJ]_{OC}$), can saturate quickly or may take hundreds of hours to fully develop. Details of the short time effects are under investigation.

After the first 500-2000 hours of testing, the subsequent performance versus time behavior of most devices is well described by a simple linear model (See Figure 1). Therefore we have performed linear regression analysis on the long term performance data for these modules, i.e.,

$$= b + mt \quad \left(2000hrs. < t < t_{\max}\right)$$

where η is the predicted efficiency.

The data was then normalized using the determined intercept, b, to obtain a relative change, i.e.,

$$\frac{\eta}{b} = 1 + \frac{m}{b}t; \quad \frac{m}{b} \equiv \text{Relative Rate of Change}$$

As defined, the relative rate of change is strictly valid only at long times.

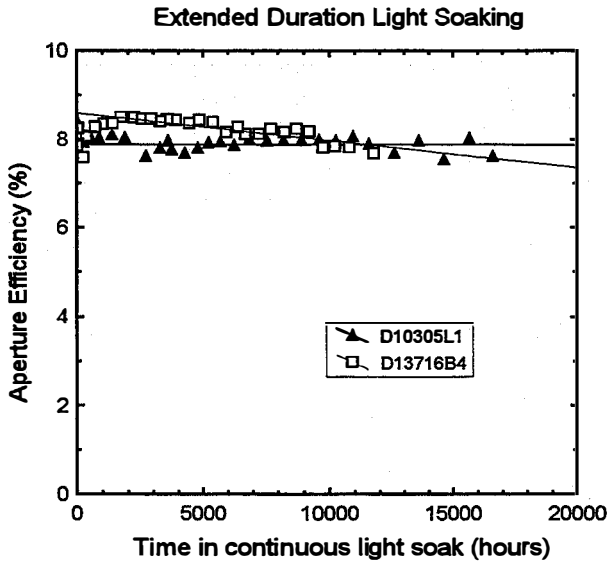


Figure 1. Performance history of two sub-modules fabricated using different recipes. Modules were loaded near maximum power point.

Since many devices are quite stable, the slopes of the efficiency-time curves are very low. Accurate determination of the relative rate of change thus requires testing for more than 5000 hours and careful maintenance and calibration of the solar simulator system.

Increases in apparent series resistance are the dominate feature of the device changes at long times. In severe cases, curvature suggestive of a back diode develops. Some loss of open circuit voltage can also occur. The magnitude of these changes is strongly dependent on the stress condition of the sample.

Capacitance-voltage measurements of degraded devices show a general trend towards lower carrier densities in the CdTe but these changes do not correlate well with efficiency changes.

Light Soaking

The mainstay of the testing protocol, due to the similarity to field conditions, is continuous light soaking with resistive load. Table 2 summarizes the averaged data from a variety of sets made using different fabrication recipes. The data shows several interesting features. First, some device sets have been very stable for up to 18000 hours. Furthermore, enough stability champions (defined as improvement or <0.25% loss per 1000 hours) endure to confidently establish the existence of stable configurations. Recipe 1.1 is currently the standard for large module processing.

Table 2. Average behavior of module sets under continuous light soaking with resistive load at a nominal temperature of 55 °C.

			Relative Rate of Change (% per 1000 hrs.)		Peak efficiency (%)	
SET	Recipe Code	Test duration (hrs.)	Encapsulated	Not Encapsulated	Encapsulated	Not Encapsulated
A	1.0	22000		- 0.61 ± 0.18		9.0 ± 0.5
B	1.1	17000	- 0.33 ± 0.19		8.4 ± 0.2	
C	1.2	14000	- 0.74 ± 0.17		9.0 ± 0.2	
D	1.3	12000	- 0.88 ± 0.43	- 1.9 ± 0.32	8.7 ± 0.3	9.1 ± 0.4
E	1.4	9000	- 0.87 ± 0.01	- 1.5 ± 0.08	8.7 ± 0.4	8.5 ± 0.3
F	2.0	18000	+ 0.89 ± 0.53	- 0.16 ± 0.27	6.7 ± 0.4	6.8 ± 0.7
G	3.0	13000	- 0.82 ± 0.15	- 0.99 ± 0.35	8.5 ± 0.1	8.8 ± 0.1
H	4.0	9000	- 0.19 ± 0.20	- 0.61 ± 0.37	9.2 ± 0.5	9.4 ± 0.5
I	5.0	7000	- 1.7 ± 0.80		8.3 ± 0.4	
J	5.1	5500	- 1.9 ± 0.30		9.0 ± 0.2	

The data in Table 2 also show that EVA-encapsulated modules are more stable than their un-encapsulated counterparts. The difference was not initially apparent and required a number of samples and adequate test duration to determine. The purpose of including un-encapsulated devices was to allow for post-test

destructive analysis.

Differences in the post-deposition chloride treatment primarily account for the recipe variations listed in Table 2. Sets I and J, made using an alternative chloride process, had adequate initial efficiencies, but, on average, poor stability. On the other hand, Set F has shown a slow improvement throughout this test, although at a lower overall efficiency. In aggregate, the samples represented in the above table suggest that chloride process details influence device stability. Reference 13 has previously suggested that the chloride treatment may lead to device instability.

Another factor that may contribute to the difference in stability observed for the various sets is unintentional process variation. The fabrication methods used for the present samples consist of many manually performed, batch-processed steps. Automated production will undoubtedly lead to more consistent processing.

The stability behavior of devices subjected to light soaking depends on the bias state. The data in Figure 2 shows that devices tested under resistive load are quite stable relative to devices tested at open circuit. Figure 2 includes data derived from samples made according to similar recipes (1.1-1.4). Devices held at short circuit conditions are also generally quite stable. We do not fully understand the mechanism responsible for the decreased stability at open circuit, but the effect appears to be rather general and consistently occurs for many, but not all, fabrication recipes. For example, see the section on the Te IFL later in this report.

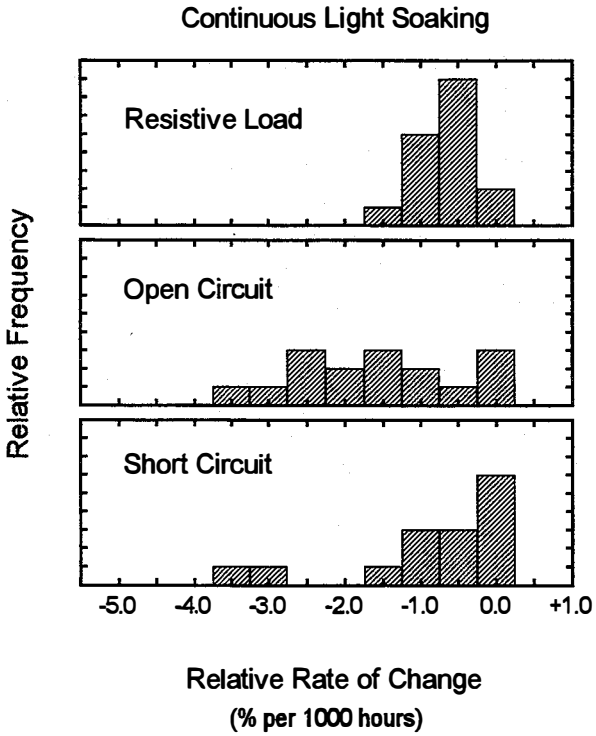


Figure 2. Bias dependence of rate of efficiency change due to continuous light soak exposure at a nominal temperature of 55 C. The data was derived from samples in sets B, C, D, and E.

Increased temperature during light soaking does lead to increased rate of degradation. Depending on fabrication recipe, up to 3.5 times faster degradation at 90 °C has been observed relative to the average rates at the nominal 55 °C tests. Currently the data is insufficient to determine a universal temperature acceleration coefficient for samples in the light soaking test. However, the use of modestly increased temperature during light soaking is effective in speeding comparison between different fabrication recipes.

Thermal and Bias Testing

At elevated temperatures in the dark, most devices held at zero or forward bias are relatively stable and again a linear model is appropriate. For the zero-bias case, aggregate data indicate a monotonic trend of increasing loss rate with increasing stress temperature. The dependence does not appear to be of the Arrhenius type. Furthermore, the temperature variation appears to be recipe dependent. We have observed examples of sub-modules with excellent tolerance of 100 °C at zero bias.

Devices subjected to reverse-bias testing in the dark, particularly at elevated temperatures, typically experience a significant initial loss in device performance in the first several hundred hours followed by a much slower decrease at longer times. The early changes are characterized by a significant increase in apparent series resistance. Some of the initial loss is reversible with the application of forward bias [14]. The time dependence of the early performance loss is complicated but generally follows an approximate t^{-n} functionality with n=0.05 to 0.10. The reverse bias test has been found to be the most strenuous one in the protocol.

Discussion

In the first phase of protocol development we have found that long term device behavior depends on bias and temperature in both light soaking and thermal stress tests. Prediction of outdoor field operation based on indoor continuous light soaking tests at constant temperature is complicated due to several factors. First, sufficient field data has not been accumulated. Second, the inherent variation of illumination and temperature in the field may be important. For example, we have observed partial performance recovery of some degraded devices after several days of interrupted indoor light exposure. Thus a simple illumination dose equivalence between continuous indoor light soaking and intermittent light exposure in the field may not be valid.

The next phase of development will include some extension and revision of the initial approach. First, while we understand some of the operating physical mechanisms, more analysis of device operation and physical changes is needed. Second, more detailed conclusions will require a larger number of samples for improved statistics, and thus concentration to fewer stress conditions is likely. Third, since some evidence of dark relaxation has been observed, an intermittent light soaking test will be added.

Conclusions from Indoor Life Testing

Stable CdTe-based photovoltaic modules have been made with our standard pilot production process. The stability of modules made using a particular process can only be ensured with long-term testing. Simple

indoor continuous light soaking conducted for >5000 hours is the minimal testing recommended. Without such testing, erroneous conclusions about the superiority of a particular fabrication recipe can be made. The recommendation applies to individual cells as well as to modules. Elevating temperatures beyond normal operating conditions by 20 to 35 °C in light soaking and by 40 to 60 °C in the dark is effective in accelerating degradation but can only be used for recipe comparisons at this time.

Outdoor array data

While all of the above described stability data for indoor tests are very important in device design and development, it alone is insufficient to predict module performance in the field. Additional information of actual field performance is required for two reasons. First, one must verify that the same phenomena is occurring in the indoor stress tests and outdoor operating conditions. For example, one must test that normal daily and seasonal temperature, humidity and illumination cycling do not induce additional degradation mechanisms not simulated in indoor tests. Second, one must use outdoor performance as a reference to determine the acceleration factor of indoor stress conditions.

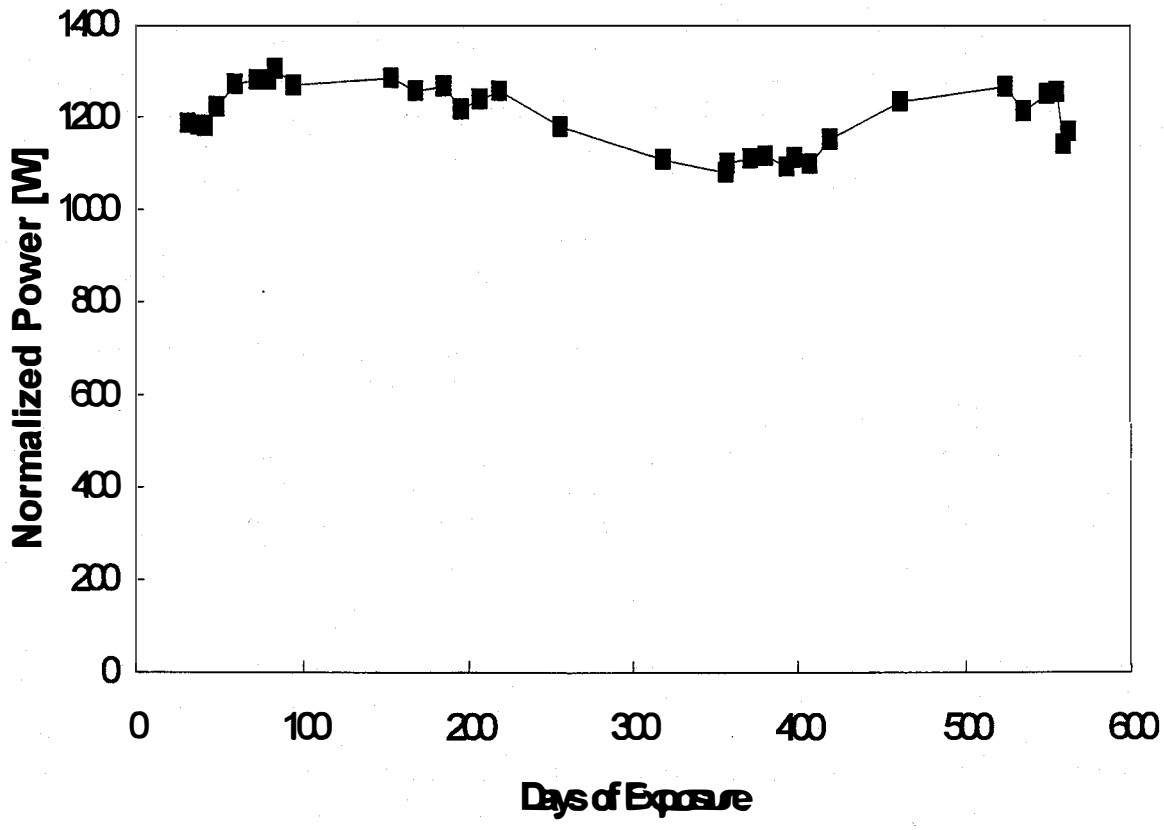


Figure 3. Power output of SCI Westwood 1.2 kW array normalized for intensity variations but not for temperature fluctuations.

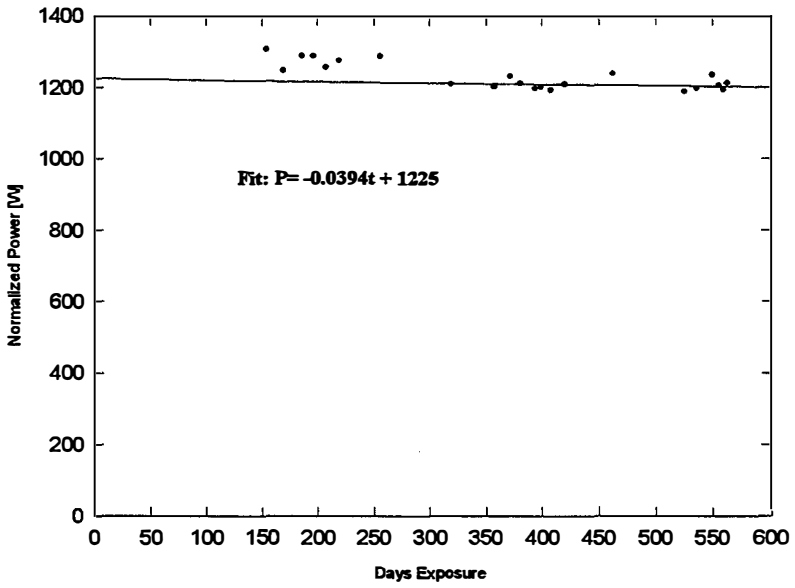


Figure 4. Power output of SCI Westwood 1.2 kW array normalized for intensity variations and corrected for temperature variations from 25 °C.

SCI has detailed performance data on two arrays which can be used for analysis and comparison. Eighteen months of data is available on our Westwood facility 1.2 kW array and twelve months of data is available on our 1 kW array at the Outdoor Test Facility at NREL. Data includes current voltage data as well as illumination intensity and temperature data to permit the normalization of both intensity and temperature variations from standard reporting conditions. The data normalized for intensity from the SCI Westwood array is shown in Figure 3. The periodic nature of the curve is due to the seasonal variation of the ambient temperature. The rated output of the array is 1200 W at 25 °C which agrees well with the average between summer and winter output. The back-of-the-module temperature on days with low wind is typically 20 °C above the ambient which results in operating temperatures during winter months of 0 - 20 °C and summertime temperatures of 50 - 60 °C. A linear regression on temperature vs. maximum power (illumination normalized) yields a temperature coefficient of -0.32%/°C which is large enough to give a noticeable apparent seasonal performance dependence. This is consistent with the range of temperature coefficients measured for small area devices under carefully controled laboratory conditions. Data taken over an eight month period was used to maximize the temperature range. The temperature coefficient calculated from data taken during any one month agree within 5%. Figure 4 shows the array data with the normalized power corrected for temperature away from 25 °C and this normalized output agrees with the initial array rating. With the temperature correction, the data is very close to being linear for time past the first 300 days of installation. The performance for the first 300 days is somewhat better than the second 300 days. This is believed to be similar to the early time (first 2000 hours) behavior of the light-soak loaded samples from the indoor stress sets discussed above. Assuming that this correlation is correct, it is predicted that the array should now stabilize at approximately 1,200 W which was the designed output. There does appear to be a slight decline in time but it is difficult to extrapolate the data accurately to the anticipated warranty term of ten years with the available data.

Data from a module under test for the past two years at NREL is shown in Figure 5. The data has been corrected for both intensity and temperature variations. The trend in the data is similar to the Westwood

array except the initial settling period occurs during the first two months of operation. It is suspected that the customary initial rise in efficiency was present for this module but occurred prior to the start of the outdoor data acquisition. The data again becomes quite linear after the initial settling period with no sign of degradation in the past two years. Note that this data is for an individual module and that from statistics one might expect an individual module to have superior performance to an array where one or two poor performers can bring down the average of the array.

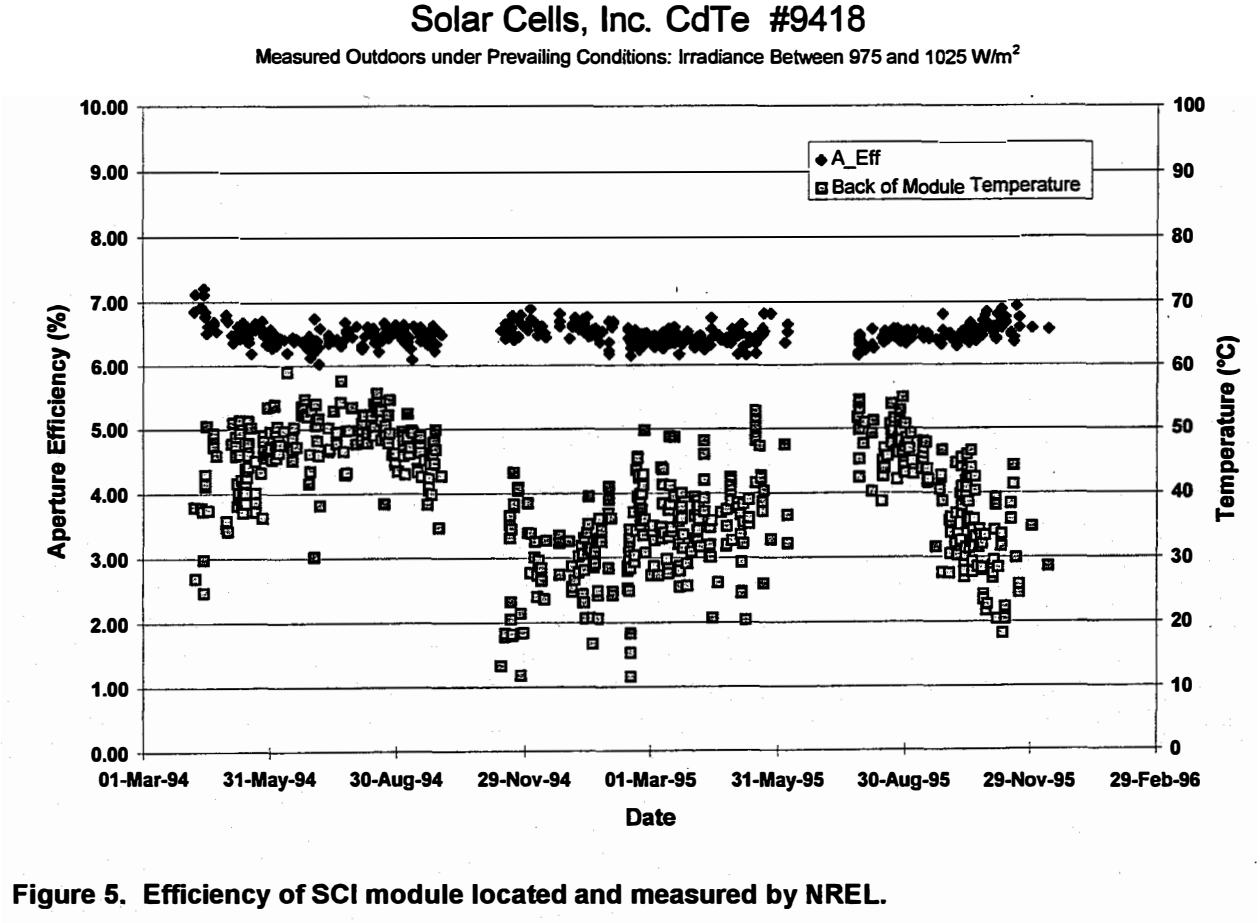


Figure 5. Efficiency of SCI module located and measured by NREL.

Deposition by Vapor Transport

Concept

SCI has been successful in implementing a large-scale close-spaced sublimation vacuum deposition process. Depositions are usually conducted at pressures near 1 Torr. The transport of material from the array of powder-filled source trays to the substrates is diffusion controlled. Likewise in laboratory close-spaced sublimation depositions, the transport of material is diffusion controlled but pressures of 10 to 30 Torr can be used due to closer source to substrate distances.

A commercial CdS/CdTe coater requires methods to supply raw material, to generate vapors, and to uniformly transport the vapors to the glass. Preferably the raw material supply is continuous and the

system can operate for an extended duration. SCI has investigated several techniques for raw material introduction and for vapor generation.

The transport of vapors in most physical vapor deposition vacuum coaters (evaporation or sputtering) is primarily line-of-sight molecular flow. In the case of CdS and CdTe, however, the vapor pressures are sufficiently high at temperatures above 800 °C, that significant quantities of material can be transported in the gas phase. Using inert carrier gas, Tuller et al. [15] and Chu et al. [16] have deposited CdTe at high pressure. Previously we have also deposited CdS and CdTe on a small scale at pressures up to 600 Torr using N_2 carrier gas [17]. Based on these results, we believe that Cd, Te, and S vapors can be generated, transported to the glass in an inert carrier gas, and deposited at the rates required for a commercial coating system. The system so conceived could operate over a wide range of pressures including atmospheric.

Design

In the initial development of the close-spaced sublimation deposition process, we quickly moved to full scale substrates. This strategy proved to be central to the rapid development of SCI's product. We again have followed this approach and have designed an apparatus based on utilizing the existing large scale (60x120 cm^2) prototype deposition system which includes glass pre-heating, glass conveyors, and glass quenching sections. In the standard vacuum deposition system, chamber lids were outfitted with cooling plates, insulation, and heaters but were otherwise passive. For the new test system, we modified a standard chamber lid and incorporated a raw material feed system, and provisions to generate vapors which can be moved with carrier gas. Since carrier gas is introduced into the system, a distributed exhaust plenum has also been incorporated.

Progress

The first system was tested in a separate chamber by depositing films onto a static 60x120 cm^2 substrate. In this system, we demonstrated the operation of the material feed system, heater arrangement, vapor generation, and vapor distribution. Deposition patterns were symmetrical although not uniform. Trials were conducted at pressures from 10 to 600 Torr. Areas of deposition with growth rates up to 1.1 um/min were found at operating pressures of 50 Torr. At higher pressures lower growth rates were observed. A common difficulty encountered was the deposition of dust rather than films. Inadequate carrier gas preheating and too rapid gas cooling at the deposition site were believed to contribute to the dust formation. The deposition of both CdS and CdTe were investigated in the first system.

To aid in the design and implementation of a modified deposition system, a simple one dimensional model of coating onto a moving substrate was formulated. The model consists of a simple injector and dual-exhaust arrangement. Typical model predictions are shown in the following figures. While simple, the model contains no phenomenological or "adjustable" parameters. Comparison with experimental data obtained in our previous vapor transport work [17] indicated reasonable agreement for deposition depletion lengths.

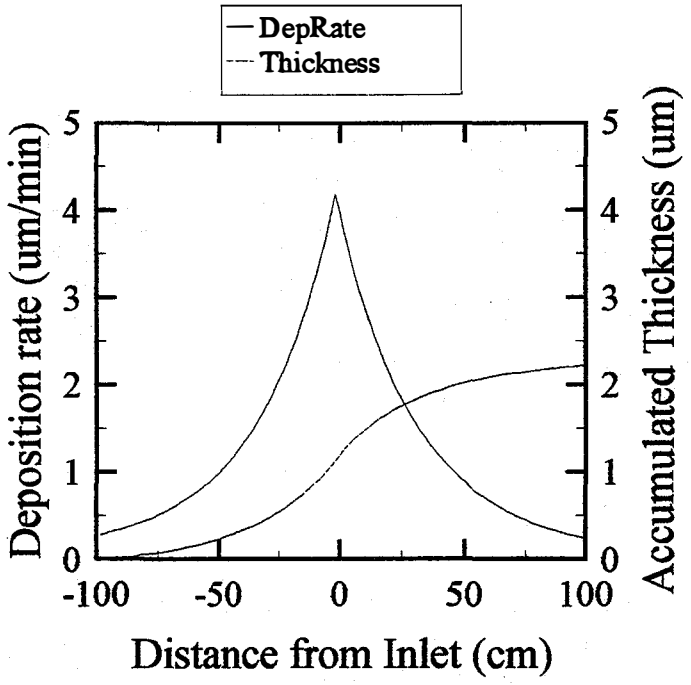


Figure 6. Simulation of atmospheric pressure deposition of CdTe onto a substrate moving at 2 cm/s.

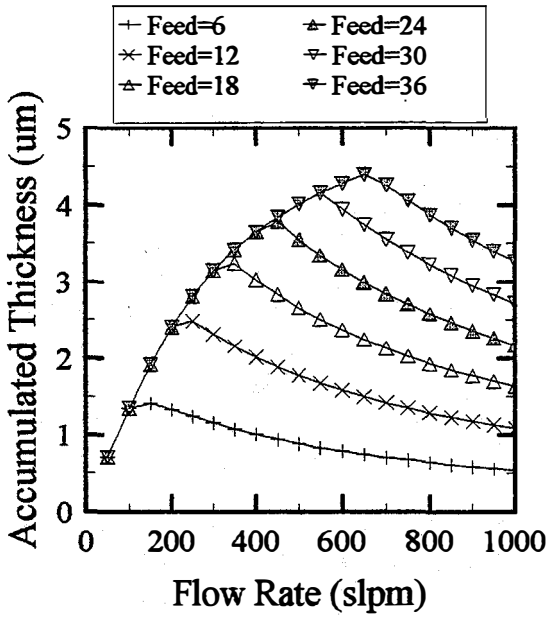


Figure 7. Estimated deposition thickness as a function of carrier gas flow rate and material feed rate in grams/min. Source temperature is 850 °C and glass speed is 2 cm/s.

Based on the results of the first system and on the simple model, a 2-injector system was constructed for use on the prototype chamber where independent glass preheating and glass transport capabilities exist. The initial results from the 2-injector system suggest improved coating uniformity, but lower than expected growth rates and continuing dust formation problems. Glass heating, gas heating, vapor generation, and dust formation issues are currently being addressed.

Efficiency

Analysis of SCI devices has indicated that there are at least two significant loss mechanisms in small area devices - optical absorption in the window layers and series resistance losses. Due to the present manufacturing constraint of using commercially-available TCO coated glass for 7200 cm^2 substrates, only the CdS window layer could be varied. An obvious path for increasing the efficiency is to minimize the CdS thickness and therefore the optical losses.[4] However, in practice, it has been observed that the open-circuit voltage decreases when the CdS thickness is less than 1,500 Å. Furthermore, an increase in short-circuit current has not been realized by the amount predicted from optical measurements of thinner CdS due to a decreased response for wavelengths above 520 nm. The result of these effects for SCI has been a decrease in efficiency when the CdS thickness is decreased. Our approach to increasing the short-circuit current while minimizing negative effects on other device parameters has largely been empirical. The general areas of experimentation on thin CdS have included modified chloride treatment, alternative substrates, and an added undoped SnO_2 buffer layer at the TCO/CdS interface.

Representative data for the standard device deposition and post-deposition processing are listed in Table 3. As expected, the J_{sc} increases as the CdS thickness is decreased. However, as noted above, the highest V_{oc} is for the sample with 1800 Å of CdS, and there is a general trend of decreasing V_{oc} with decreasing CdS thickness. There is not a monotonic trend in the efficiency (like there is for the V_{oc} and J_{sc}) because there is some variation in the series resistance from cell to cell, but there is still an overall net effect of somewhat lower efficiency as the CdS thickness is decreased.

Table 3. Variation of J_{sc}, V_{oc}, and efficiency with CdS thickness.

CdS Thickness [Å]	J_{sc} [mA/cm^2]	V_{oc} [mV]	Efficiency %
1800	17.9	827	10.6
1500	17.7	824	10.4
1400	18.1	819	10.5
1200	18.6	796	10.5
1100	18.6	791	10.1
900	18.8	751	9.2

The Quantum Efficiency curves, taken at NREL, for the devices with CdS thickness of 1,800 and 1,100 Å from Table 3. are shown in Figure 8. The first point to note is that the thinner CdS device has a notably higher response at wavelengths below the 520 nm, which corresponds to the CdS bandgap, as expected from the optics. The response for these two devices is quite similar above 520 nm. However, cases have been observed in which there is a significantly poorer response of the thinner CdS device at wavelengths above 520 nm. The reduction at longer wavelengths seems to be somewhat different from what others have reported because both the red and green response is lower. Others have observed a reduction in green response in the thin CdS samples and have attributed this to lowering of the CdTe bandgap due to S in-diffusion. We have observed a reduction in both green and red response which suggests a more complicated mechanism.

Many trials using our standard process, but reduced CdS thickness, did not produce consistent efficiency improvements. Thus, it was evident that new procedures were needed. One hypothesis was that the thinner CdS was not as robust and could be adversely affected by the $CdCl_2$ treatment. Evidence that the $CdCl_2$ treatment affects the CdS is seen by the change in photoluminescence as discussed in a later section of this report. Past studies have shown that the $CdCl_2$ heat treatment is very sensitive to the treatment temperature and that temperature variations from the optimum as small as 10 - 15 °C have a significant effect on device performance. Trials with thin CdS and treatment temperatures 10 - 30 °C below the standard temperature were performed. Improved efficiency was observed in some trials with a average 15°C lower chloride treatment temperature, but the improvement did not prove to be statistically significant.

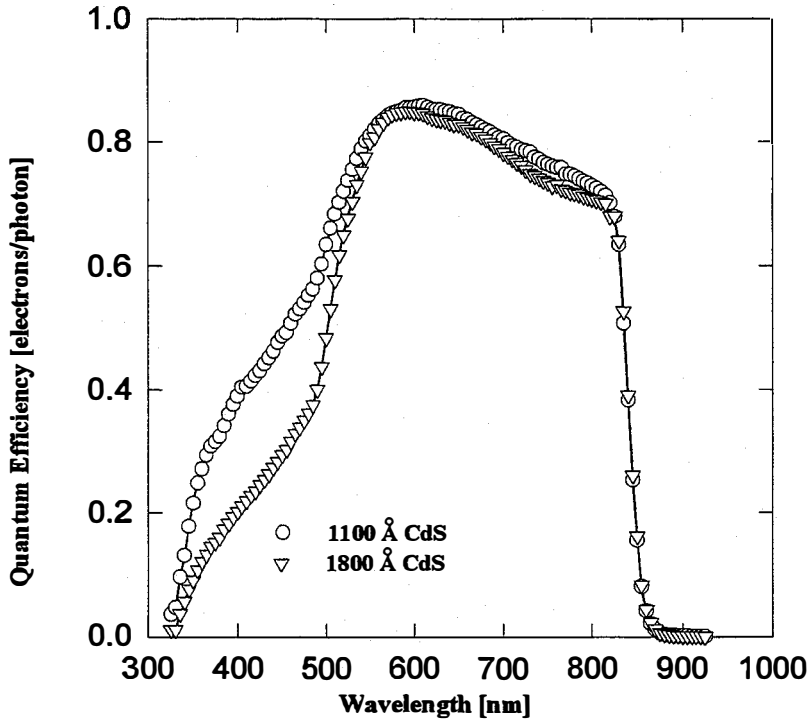


Figure 8. Quantum Efficiency comparison of relatively thin and thick CdS.

A more successful approach to increasing J_{sc}, similar to the USF technique, has been to deposit a high resistivity SnO_2 layer onto standard LOF 8 Ω/□ (TEC 8) glass. SnO_2 200-1000 Å thick has been deposited by rf-sputtering from a SnO_2 target in an Ar and O_2 ambient. The O_2 concentration was varied from 0 - 10%. Sputtered films deposited on plain glass were very insulating with sheet resistances higher than the detection limit of our four-point probe. Transmission measurements have not been made on the composite SnO_2 films but visually they appear almost identical to the LOF TEC8 SnO_2. Results from sequential depositions on substrates with varying SnO_2 thickness are listed in Table 2. All devices were post-deposition processed in an identical manner and all have nominally 1000 Å of CdS. The most striking result from this experiment is that by using the intrinsic SnO_2 there is a pronounced increase in the open-circuit voltage along with an unexpected increase in short circuit current density. The V_{oc} peaks when the SnO_2 is 400 Å whereas the current peaks at 300 Å. The rise in J_{sc} is presumably due to a increased collection efficiency near the interface whereas the decreasing J_{sc} with increasing SnO_2 thickness is due to optical absorption in the SnO_2. The effect on the V_{oc} is still not well understood but some of the working assumptions include 1) it reduces the CdS pinhole related losses, 2) it acts as a n-type semiconductor in conjunction with the CdS or 3) it lessens the effect of surface roughness of the TCO. Table 4 shows the results from only one test but similar results have been seen on a large number of samples which were fabricated in a similar manner and are therefore representative.

Table 4. Device performance for different intrinsic SnO_2 thickness, CdS thickness ~ 1000 Å.

SnO_2 thickness [Å]	J_{sc} [mA/cm^2]	V_{oc} [mV]	Efficiency
0	18.9	761	9.22
300	19.8	805	10.9
400	19.5	814	11.3
600	19.4	788	9.97

The QE curves for the 0, 300, and 400 Å intrinsic SnO_2 thicknesses are plotted in Figure 9. Note that all three curves are very close to the same over the middle wavelengths and slightly deviate only at the long and short wavelengths. The curves are consistent with the arguments given above for the variation of the current density shown in Table 4.

The last area of experimentation on efficiency improvement is work that was done in conjunction the NREL polycrystalline thin-film team activities. Experiments involved deposition of CdS layers of varying thickness onto borosilicate glass which had the two layer SnO_2 TCO deposited by MOCVD by the University of South Florida group. Completed devices were analyzed by the Colorado State University group. There were six substrates fabricated for the test with sets of two having 600, 1000 and 1500 Å of CdS. The results are summarized in Table 5. The J_{sc} is over 20 mA/cm^2 for all samples because of the high transmission through the borosilicate glass. The highest current was 24 mA/cm^2 on one of the 600 Å CdS samples which along with the respectable 775 mV V_{oc} yielded a 11.6 % efficiency. This performance was surpassed by the 1000 Å CdS which produced 800 mV V_{oc} and 22.5 mA/cm^2 J_{sc} to yield an efficiency of 12.3%. These results emphasize the fact that the optical losses are not independent of the junction parameters and that both must be taken into account during the process of device optimization.

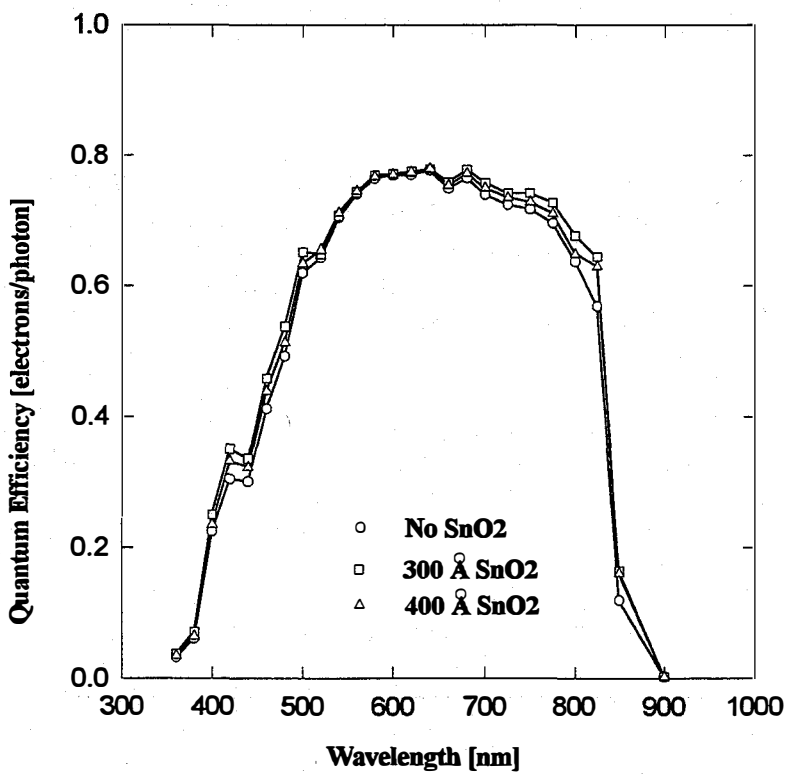


Figure 9. Comparison of quantum efficiency for different intrinsic SnO_2 thickness deposited on the TCO prior to CdS deposition.

Back Contact

Tied very closely to stability is the processing required to form a low resistance contact to the CdTe. This has historically been an area of difficulty as reported in the literature [6-8] and experienced in-house. The present understanding is that there must be an interfacial layer (IFL) or surface conditioning that permits the electrical transition from the CdTe, which has a high work function and almost always has a low carrier density, to the back metal contact. The tell-tale sign that the surface conditioning is not effective is a very pronounced roll-over of the I-V curve in the first quadrant and has also been reported in the literature [17-19]. There are several standard techniques which are used to form this IFL including various etching procedures such as bromine in methanol or phosphoric acid. Most of the etching procedures leave a Te-rich surface on the CdTe [20]. In addition, it has been found that small amounts of either Cu or HgTe must be introduced at the interface. It is beleived that the Te acts as a degenerate semiconductor contact passivating some of the surface defects and lowering the back barrier [20]. The Cu acts as a p-type dopant in the CdTe and changes the band profile such that the contact resistance is reduced. Work at SCI has focused on both optimizing the IFL for initial performance and stability while simultaneously eliminating the wet processing steps. Tests on devices with a rf-sputtered IFL of Te and Cu exhibit performance equal to or better than the standard process.

Table 5. Results from devices made on borosilicate glass with TCO from USF

(measurements performed at CSU)

Cell	1	2	3	4	5	6
CdS [Å]	600	600	1000	1000	1500	1500
Total Area [cm^2]	1.006	1.043	1.035	1.005	1.009	1.005
V_{oc} [mV]	670	775	785	800	800	780
J_{sc} [mA/cm^2]	22.0	24.0	22.0	22.5	22.0	20.5
V_{mp} [mV]	445	555	600	605	635	550
J_{mp} [mA/cm^2]	15.5	20.5	17.5	20.0	18.5	20.0
FF	48	63	61	69	67	63
η %	7.0	11.6	10.6	12.3	11.7	10.1
r [Ω-cm^2] light dark	310 1000	4000 >10000	1200 >10000	5000 >10000	2500 >10000	4000 >10000
R [Ω-cm^2] light dark	3.4 8	3.2 4.7	(2.0) 4.1	2.4 4.2	1.7 2.8	4.8 6.1

Te Interfacial Layer - Efficiency

In examining the possible mechanisms responsible for the behavior of the back contact, SCI researchers reasoned that the primary purpose of the "required" acidic etch step was to produce a Te rich surface which could act as an interfacial layer. The estimated thickness of the Te layer is only a few angstroms based on the quantity of Cd removed with our etch. As a manufacturer of modules, a consistent goal of the research is to find processes that are simple and effective so that the technology can be quickly adapted to the manufacturing line. For example, it is desirable to simplify the wet chemistry etch step used in pilot production. Therefore it seemed logical to try replacing the etch with a simple Te deposition step which would also produce less waste.

The initial trials with a Te IFL were performed using electron-beam evaporated Te films and results from one of the better devices is show in Figure 10. As can be seen from the graph, both the series and shunt resistances are adequate and the device has comparable J_{sc} and V_{oc} to standard processed samples. There is no rollover in the first quadrant which suggests that the barrier height at the back contact is not significant. I-V data taken at lower temperatures do reveal a rollover indicating that a barrier is still present as expected, but lowered. The main difference between the etching procedure and the deposition of Te is the resulting thickness of the Te. In the case of etching, the thickness is estimated to be less than 50 Å whereas 500 - 1000 Å of Te is typically deposited by the vapor process. Despite the thickness difference, the initial efficiency of the devices was very similar. This supports the hypothesis that a Te-rich surface is the reason for the effectiveness of the acidic etch.

Subsequent experiments were performed in which the Te was deposited with RF-sputtering and similar results were recorded as shown in Figure 11. The performance of the sputtered sample exhibited a slightly higher V_{oc} but higher series resistance and resulted in a slightly lower efficiency. Te forms at the interface is not as critical as its presence at the interface. Thus it appears that any method which results in a Te IFL can produce good devices.

The good performance of devices with a Te IFL is not limited to individual cells but has also been demonstrated on minimodules. For example, a near record (for SCI) 64 cm^2 area minimodule with an efficiency of 10.5% had a Te IFL which was sputtered in the small rf-sputtering system. The I-V data taken at NREL is shown in Figure 12. The Te IFL also eliminates a proprietary wet chemistry surface treatment step which SCI has used in the past to boost the device efficiency. Elimination of the wet step without sacrificing performance is important for manufacturing considerations.

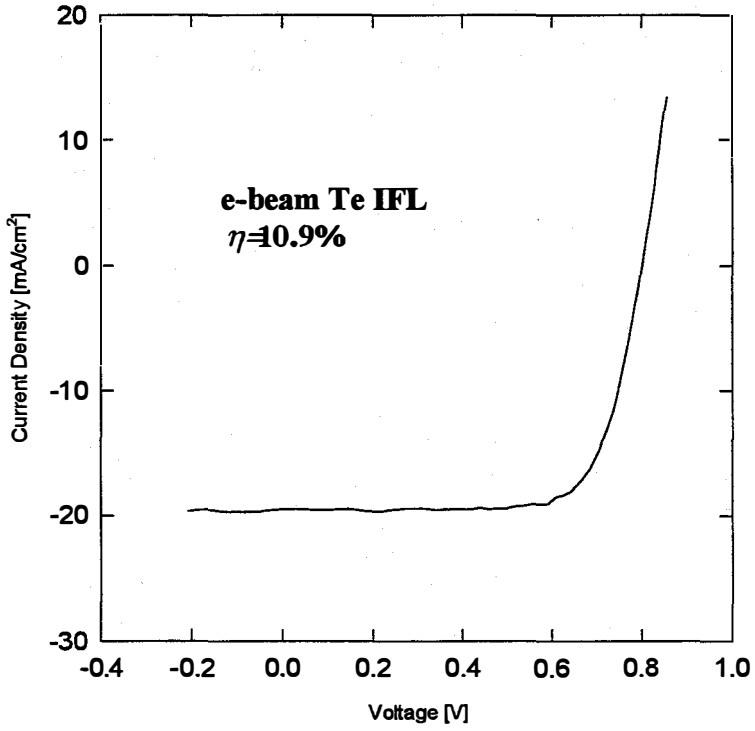


Figure 10. I-V curve of a good efficiency device with a Te interfacial layer between the CdTe and back metal.

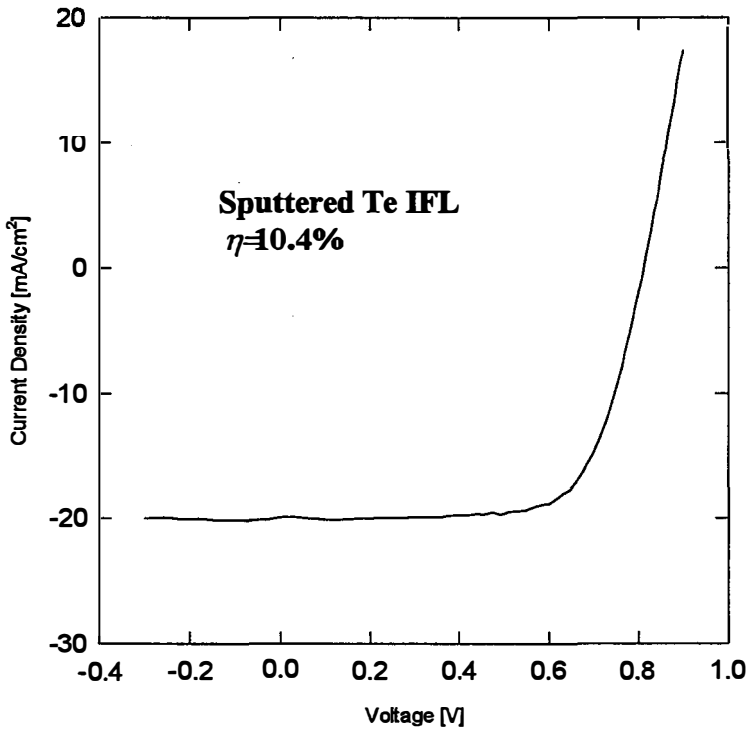


Figure 11. I-V curve for a typical cell with a Te interfacial layer deposited by rf-sputtering.

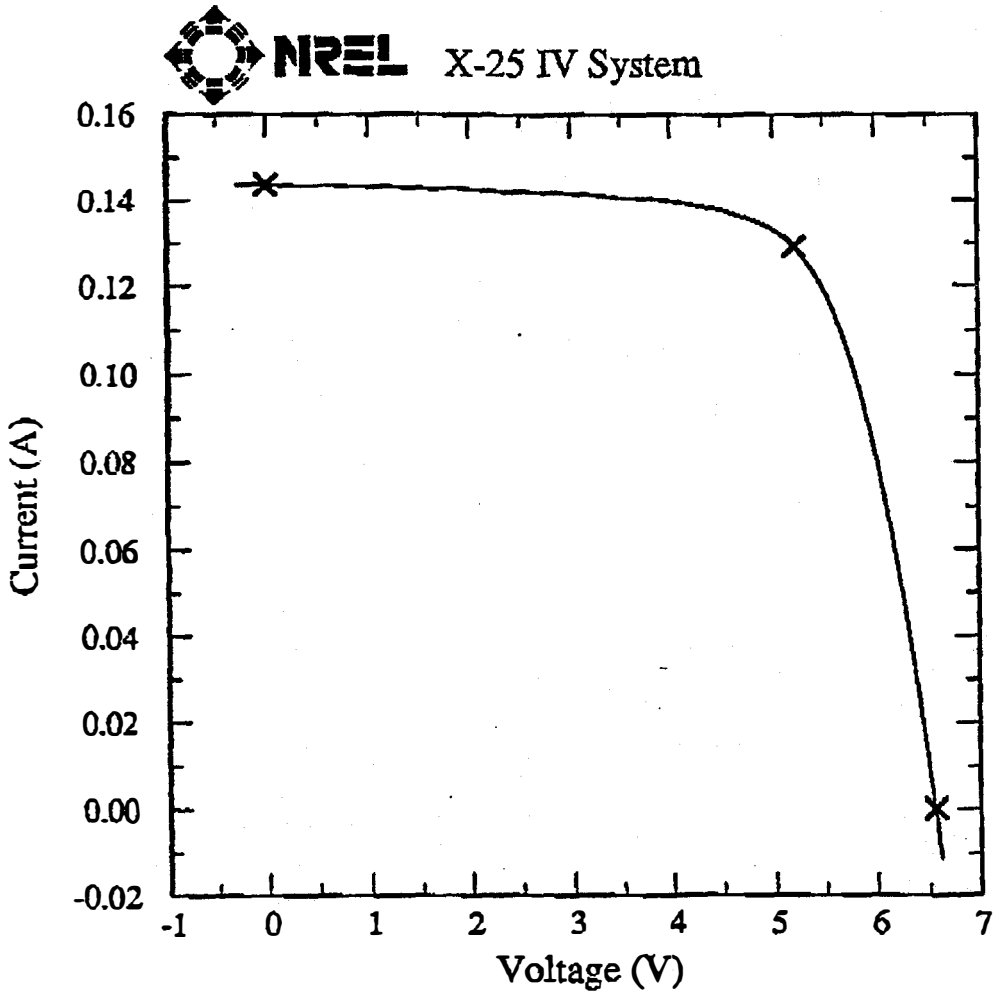
Te Interfacial Layer - Stability

As discussed in the stability section above, before a device structure can be considered suitable as a commercial product it must not only have adequate efficiency but it must also maintain that performance in the field. Data taken on samples with Te IFLs looks promising. Small area devices have shown stability superior to the standard devices, especially when stressed at open-circuit conditions under continuous illumination. A comparison of typical devices with and without a Te IFL and biased at open circuit in the light is shown in Figure 13. Not only is the Te IFL more stable, the device with the Te IFL has a better efficiency. Devices with Te show only a slight difference in response to continuous light soak when biased near maximum power or held at open-circuit. Efficiency vs. Time for a representative Te IFL 48 cm^2 mini-module is shown in Figure 14. Unlike standard devices which often show a rapid initial rise in efficiency with light soak, the performance of devices with Te IFL show a more gradual rise. Standard device efficiency typically peak within the first 1500 hours whereas the Te IFL samples can take 2000 - 4000 of continuous light soak hours to reach the peak efficiency. In both device configurations, the initial relative change is only a few percent in most cases.

Solar Cells Inc. CdS/CdTe

Sample: B14322D5
Feb 1, 1995 8:18 AM
ASTM E 892-87 Global

Temperature = 25.0°C
Area = 63.77 cm^2
Irradiance: 1000.0 Wm^{-2}



V_{oc} = 6.568 V
I_{sc} = 0.1438 A
J_{sc} = 2.255 $mAcm^{-2}$
Fill Factor = 71.17 %

V_{max} = 5.210 V
I_{max} = 0.1291 A
P_{max} = 672.3 mW
Efficiency = 10.5 %

Figure 12. I-V curve of best minimodule with a Te interfacial layer.

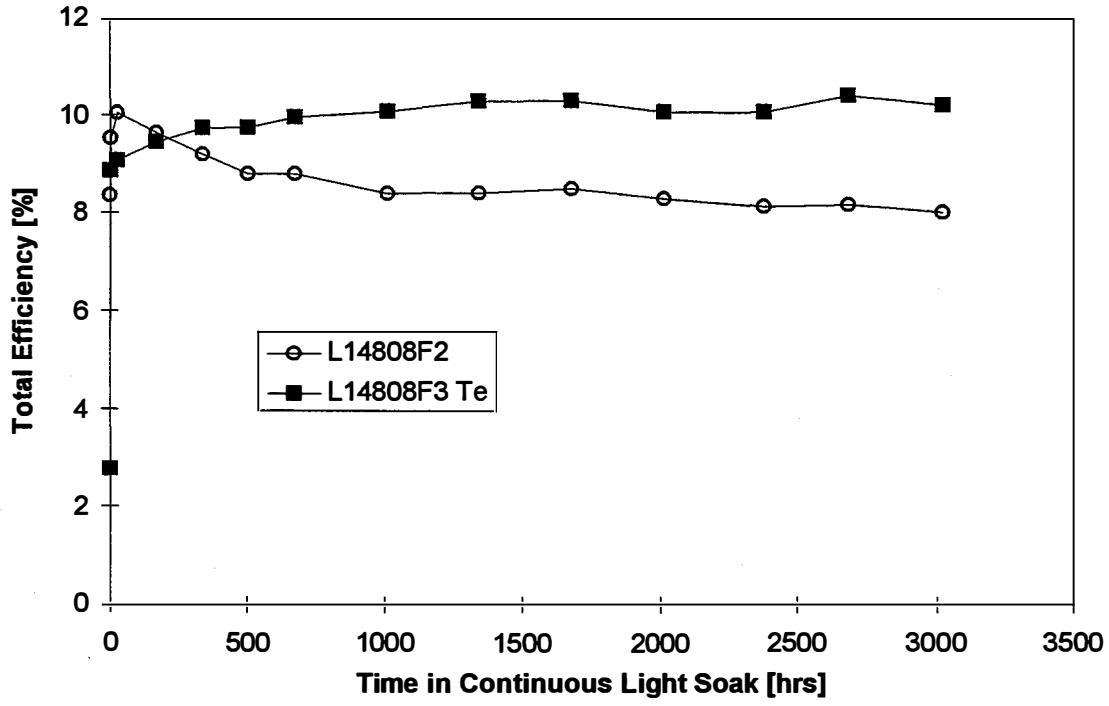


Figure 13 Comparison of initial stability of devices held at open-circuit under 80 mW/cm^2 illumination with and without a Te interfacial layer.

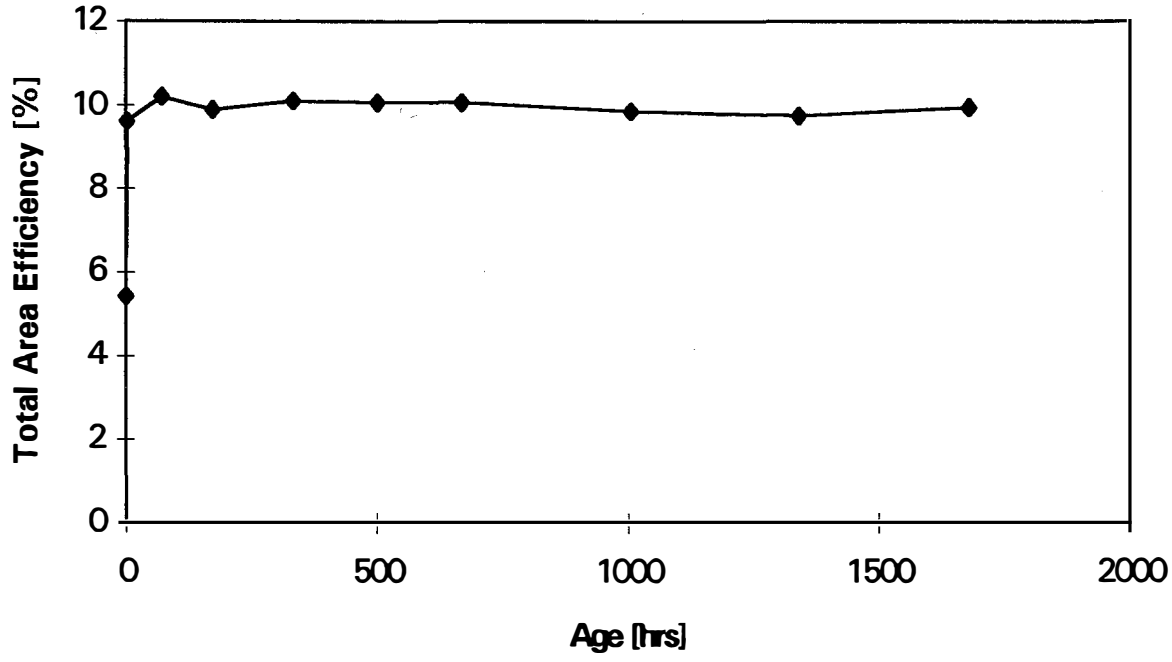


Figure 14. Stability performance for a typical minimodule with a Te interfacial layer.

CdS Photoluminescence

The fabrication of photovoltaic devices is a multi-step process with potential for unintentional variations in the manufacturing procedure. Detection of process variations in the earliest fabrication stages possible is desirable. This permits correction of the variation for subsequent substrates in the process stream and the rejection of unacceptable substrates without costly further processing. Therefore, the development of nondestructive, quantitative, rapid, and reliable diagnostic techniques which can be implemented between process steps is extremely useful for both laboratory and manufacturing scale device fabrication.

It has been observed that chloride treated CdTe/CdS films emit a reddish-orange light when exposed to ultraviolet light. It has furthermore been observed that the intensity of the luminescence is directly correlated to the extent of the chloride treatment which is essential for the fabrication of high efficiency devices. Qualitative information can be obtained through visual observation of luminescence excited using a long-wavelength UV source (i.e. a black-light). Through a CRADA with NREL, a photoluminescence (PL) meter has been assembled by NREL which consists of a UV light source, a photodetector, and band-pass filters arranged so that both the light-source and detector are nearly normal to the substrate surface. This meter quantifies the observed PL from which the extent of chloride treatment can be inferred.

The PL detection system was used to measure the extent of the chloride treatments of varying time, temperature and type. The time of treatment was varied from 5 to 120 minutes, the temperature was varied from 370 to 410 °C and the treatments given were the standard $CdCl_2$ treatment and the newer HCl treatment [21]. The PL signal was measured before and after chloride treatment as well as after other standard post-deposition processing steps. While the exact physical mechanism is not known, the luminescence is thought to be caused by mid-level defect levels in the CdS. The effectiveness of the luminescence centers might be altered through the chloride treatment by the passivation of nonradiative defect levels. The CdS is the layer which is luminesing because the excitation source is in the ultraviolet and nearly all light is absorbed in the CdS. It is also expected that the PL signal will depend on the CdS

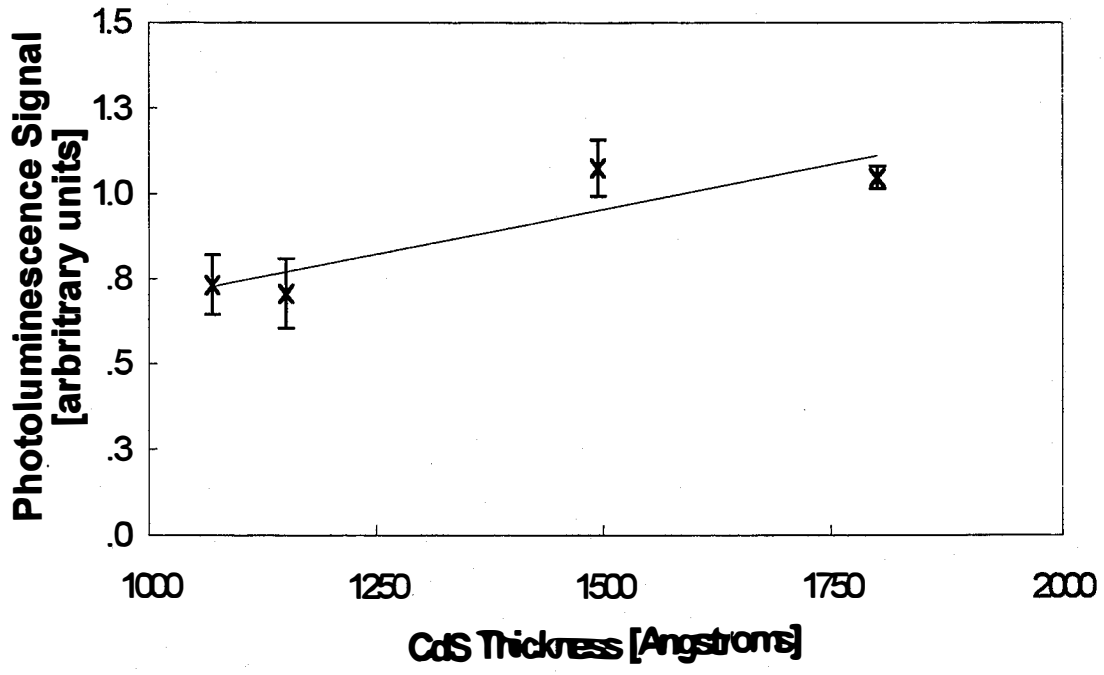


Figure 15. PL signal variation with thickness of CdS layer.

thickness and is verified by data shown in Figure 15 which shows PL signal vs. CdS thickness. Since the PL signal is proportional to CdS thickness, the thickness dependence can be factored out for any given set of CdS growth parameters (or independent thickness measurement) and therefore the effectiveness of the chloride treatment can be monitored. Other than the trials designed to specifically test the PL signal variation with thickness, all samples used in this study had a nominal CdS thickness of 1500Å.

The true test of the procedure is to predict the efficiency range of a device based on its PL signal after the chloride treatment. The results of this test are shown in Figure 16 where it can be seen that there is a definite relationship between PL signal and device efficiency. The range of efficiencies and PL signals was deliberately altered by varying both the treatment temperature and treatment time. Samples that were given a lower than optimum time and temperature treatment have the lower PL signal and efficiency. Samples with a PL signal less than 0.8 have efficiencies less than 8% and would be considered sub-standard, while those with a PL signal above 1.5 have efficiencies mostly above 10 % and would be considered acceptable. There are a few devices with acceptable PL signal but with only marginal efficiency due primarily to factors other than the effectiveness of the chloride treatment such as shunting or high series resistance. From this it can be seen that while a PL signal above 1.0 is a necessary criterion it is not a sufficient condition. Yet, it provides the investigator with required information to diagnose a nonideal chloride treatment in all cases.

The significant interpretation of the data is that the PL signal correlates well with the efficiency for all time and temperature ranges tested which supports the feasibility of using the PL signal as a diagnostic and predictive tool. The data also successfully maps out the time and temperature process latitude of the chloride treatment based upon PL signal and efficiency as well as any spatial variation which may be present in a module.

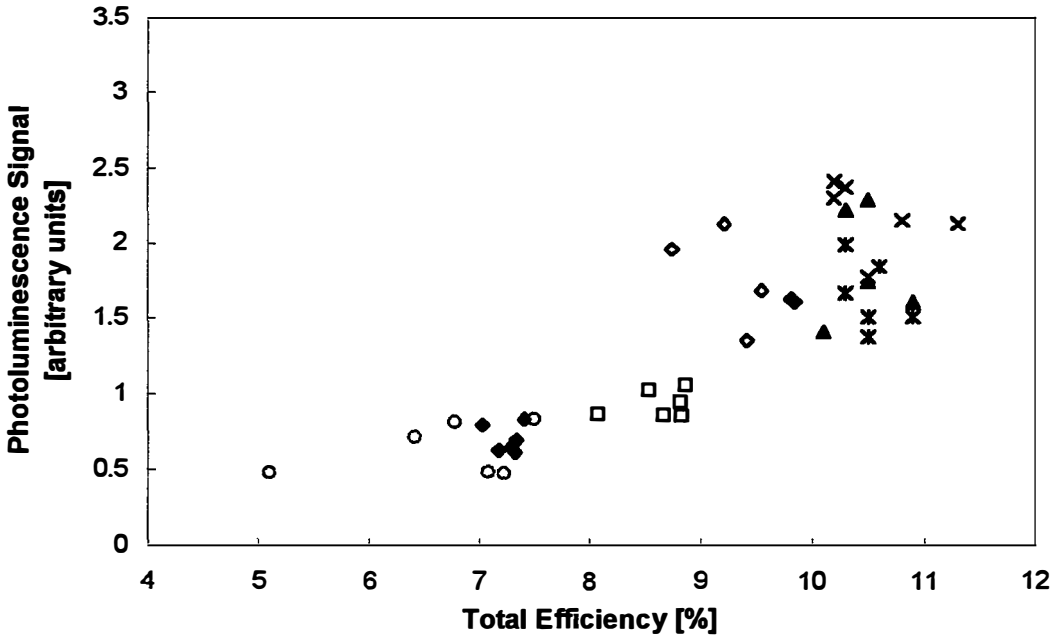


Figure 16. PL signal vs. Efficiency for several devices intentionally processed with different chloride treatment parameters.

ENVIRONMENTAL

Solar Cells Inc. recognizes the importance of properly managing cadmium-bearing production and process wastes. Unfortunately, while cadmium based semiconductors such as cadmium telluride and cadmium sulfide have many beneficial properties for photovoltaics, they must be prevented from creating environmental pollution or becoming a human health threat. Solar Cells has created a multitude of processes and procedures to actively prevent environmental cadmium releases and employee cadmium exposure.

Procedures

Procedures have been developed as listed below and include employee training:

- Resource Conservation and Recovery Act Compliance Plan (40 CFR 261-265)
- Cadmium compound and container management standard operating procedure
- Wastewater pre-treatment standard operating procedure
- Chemical inventory and labeling standard operating procedure
- The OSHA Cadmium Standard (29 CFR 1910.1027) including annual industrial hygiene testing and ongoing medical monitoring

Processes

Processes have also been implemented to prevent cadmium releases or employee exposure as listed below:

- Local ventilation controls for deposition, buffing, sandblasting, lasing and maintenance operations
- Wastewater pre-treatment by lime precipitation
- Recycling of off-specification modules by ASARCO

99.9% Capture and Collection

Cadmium inputs and outputs need to be considered to generate a simple mass-balance material accounting system. If the Solar Cells pilot facility is viewed as a "black box", with certain cadmium compound inputs, the outputs can be broken down into three generation pathways; air emissions, land (soil) emissions, and water emissions.

Air Emissions - Solar Cells has obtained air permit exemptions based on engineering calculations showing minimum cadmium capture efficiencies of 99.9% for all facility processes which are vented to the outside.

Water Emissions - Solar Cells has data showing influent cadmium concentrations for wet processing steps at up to 10 mg/L. Effluent levels (after precipitation) are below 0.1 mg/L. Again, this represents at least 99.9% capture efficiency.

Land (Soil) Emissions - No known local emissions to the grounds surrounding the Solar Cells pilot production have occurred. Cadmium contaminated manufacturing debris, including personal protective equipment and machine parts, are collected and either stabilized for land-filling (if non-combustible) or incinerated (if combustible) at a RCRA permitted facility. Cadmium contaminated wastes are collected separately from non-regulated wastes and waste minimization techniques are being explored.

Additionally, scrap modules are returned to ASARCO for use as "flux" agent in their smelting process at their Helena, Montana location. When, Solar Cells grows beyond pilot production scale, modules will be recycled in-house using a combination of recycling technologies developed especially for recycling Solar Cells thin-film PV modules.

Conclusions - Future Work

During the first phase of this subcontract, progress has been made in the important areas of stability, advanced deposition techniques, efficiency, the back contact, no-contact film diagnostics (photoluminescence) and cadmium waste control. The progress in stability has been in both the demonstration of devices maintaining at least 90% of the initial efficiency for over 19,000 hours of continuous light soak and the development of methods which can accurately predict long term behavior based on the first 5,000 - 10,000 hours of life. Notable achievements in advancing the state of the art in deposition technology include depositing CdTe on a 3600 cm^2 substrate at 600 torr and designing and fabricating a new deposition feed system with a remote semiconductor source. The efficiency has been increased on small area devices to 13.3% by decreasing the thickness of the CdS and of the glass substrate. The back contacting process has been simplified by replacing the wet etch with a vapor Te deposition step on small area devices. Preliminary studies of the correlation between CdS photoluminescence after the chloride treatment and the final device efficiency have shown a positive correlation which may be applicable for in-line quality control. The final area of progress was through the successful demonstration of preventing at least 99.9% of all incoming Cd from leaving in an uncontrolled manner through the land, air or water.

Work in the coming year will center on the same topics but will increase in depth. Particular emphasis will be placed on the continued development and optimization of the new deposition system. A similar system will be installed on the High Throughput Deposition System. The films will be characterized in the typical manner and a new baseline of performance established. Work on efficiency improvement will focus on the further understanding and manipulation of the behavior of thin CdS in devices without sacrificing other diode parameters. Additional emphasis will be placed on developing alternative low-loss interconnecting techniques which are consistent with high throughput production.

References

1) Zweibel, K. And R. Mitchell, $CuInSe_2$ and CdTe: Scale-Up for Manufacturing, SERI/TR-211-3571, UC Category:273 DE89009503, 1989, NREL, Golden, CO.

2) Tyan, Y. And E.A. Peres-Albueme, Proc. IEEE PVSC 16, 1982, pp 794-800.

3) Mitchell, K. W., C. Eberspacher, F. Cohen, J. Avery, G. Duran, and W. Bottenberg, Proc. IEEE PVSC 18, 1985 pp 1359-1364.

4) Chu, T. L. And S. S. Chu, C. Ferekides, C. Q. Wu, J. Britt and C. Wang, Proc. IEEE PVSC 22, 1991, pp 952-956.

5) Anthony, T. L., A. L. Fahrenbruch, and R. H. Bube, J. Vac. Sci. Technol. A **2** (3)

6). Y.-S. Tyan, "Topics on Thin Film CdS/CdTe Solar Cells", *Solar Cells* **23**, 1988, pp. 19-29.

7). A. F. Fahrenbruch, "Ohmic Contacts and Doping of CdTe Solar Cells", *Solar Cells* **21**, 1987, pp. 399-412.

8). L.F. Szabo and W. J. Biter, "Stable Ohmic Contacts to Thin Films of P-type Tellurium-Containing II-VI Semiconductors", U.S. Patent 4,735,662, 1988.

9). T.X. Zhou, R.A. Sasala, and R. C. Powell, "Fabrication of Stable Large-Area Thin-Film CdTe Photovoltaic Modules", in American Institute of Physics Conference Proceedings 353, 13th NREL Photovoltaics Program Review, H.S. Ullal and C. E. Witt Eds., Lakewood, CO, 1995, pp. 31-38.

10). B. Kroposki, T. Strand, R. Hansen, R. Powell, and R. Sasala, "Technical Evaluation of Solar Cells, Inc. CdTe Module and Array at NREL", 25th IEEE PVSC, 1996.

11). S. Ikegami, "CdS/CdTe Solar Cells by the Screen-Printing-Sintering Technique: Fabrication, Photovoltaic Properties and Applications", *Solar Cells* **23**, 1988, pp. 89-105.

12). J. M. Woodcock et al., "Thin Film CdTe Photovoltaic Cells", 12th European Photovoltaic Solar Energy Conf., Amsterdam, April 1994.

13). S. A. Ringel, A. W. Smith, M.H. MacDougal, and A. Rohatgi, "The Effects of CdCl2 on the Electronic Properties of Molecular-Beam Epitaxially grown CdTe/CdS heterojunction solar Cells", *J. Appl. Phys.* **70**, 1991, pp. 881-889.

14). T.X. Zhou, "Fabrication of Stable Large Area Thin Film CdTe photovoltaic Modules", NREL Subcontract ZR-1-11059-1, Final Technical Report (1995).

15) H.L. Tuller, K. Uematsu, and H.K. Bowen, J. Crystal Growth **42**, 150 (1977).

16) T.L. Chu, S.S. Chu, Y. Pauleau, K. Murthy, E.D. Stokes, and P.E. Russell, J. Appl. Phys. **54**, 398 (1983).

17) J. F. Nolan et al., Annual Technical Status Report, Subcontract ZR-1-11059-1, May 1993.

18). Stollerwrk G., and J.R. Sites,"Analysis of CdTe Back-Contact Barriers", Proc. European Photovoltaic Solar Energy Conf. 13, 2020 (1995).

19). Singh, V. P., O. M. Erickson, and J. H. Chao, *J. Appl. Phys.* **78** (7), October 1995, pp 4538-4542.

20). Niles, D. W., X. Li, P. Sheldon, *J. Appll. Phys.* **77** (9), May 1995, pp 4489-4493.

21). Zhou, T. X., N. Reiter, R. C. Powell, R. Sasala, P. V. Meyers, Proc. First WCPEC December 1994, pp 103-106.

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13. ABSTRACT *(Maximum 200 words)*

During the first phase of this subcontract, we made progress in the important areas of stability, advanced deposition techniques, efficiency, the back contact, no-contact film diagnostics (photoluminescence), and cadmium waste control. The progress in stability was in both the demonstration of devices maintaining at least 90% of the initial efficiency for more than 19,000 hours of continuous light soak and the development of methods that can accurately predict long-term behavior based on the first 5,000-10,000 hours of life. We conducted experiments to determine if device behavior could be accelerated with thermal or voltage stresses. Notable achievements in advancing the state of the art in deposition technology include depositing CdTe on a 3600-cm^2 substrate at 600 torr and designing and fabricating a new deposition feed system with a remote semiconductor source. Mathematical modeling of the deposition has permitted a more rapid development of a large-area coater. The efficiency has been increased on small-area devices to 13.3% by decreasing the thickness of the CdS devices and of the glass substrate. Work also focused on using a high resistivity SnO_2 buffer layer between the transparent conductive oxide and thin CdS to help preserve the open-circuit voltage while increasing the current-density. The back contacting process has been simplified by replacing the wet post-deposition etch with a vapor Te deposition step on small area devices. Results show that the devices perform comparably in efficiency but better in stability under light-soaking and open-circuit conditions. Preliminary studies of the correlation between CdS photoluminescence after the chloride treatment and the final device efficiency showed a positive correlation that may be applicable for in-line quality control. We also successfully demonstrated the prevention of at least 99.9% of all incoming Cd from leaving in an uncontrolled manner through the land, air, or water.

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