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Investigation of Polycrystalline Thin- Film $CuInSe_2$ Solar Cells Based on ZnSe and ZnO Buffer Layers

Final Report
16 February 1992 - 15 November 1995

L.C. Olsen
Electronic Materials Laboratory
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NREL technical monitor: B. von Roedern

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ABSTRACT

The major objective of this program was to determine the potential of ZnSe and ZnO buffer layers in solar cells based on $CuInSe_2$ and related alloys. Experimental studies were carried out with CIS and CIGSS substrates provided by Siemens Solar. ZnSe films were deposited by a CVD process which involved the reaction of a zinc adduct and H_2Se. Al/ZnSe/CIS test cells were used for process development. Test cell performance aided in determining the optimum thickness for ZnSe buffer layers to be in the range of 150Å to 200Å for Siemens CIS material, and between 80Å and 120Å for the graded absorber material. If the buffer layers exceeded these values significantly, the short-circuit current would be reduced to zero. This effect is consistent with results reported in the literature indicating that there is a 0.9 eV band offset at the ZnSe-CIS interface. Completed cells were fabricated by utilizing a low resistance ZnO top contact layer deposited by Siemens, and then depositing an Al/Ag collector grid at WSU. The best efficiency achieved for a ZnSe/CIS cell was an active area value of 9.2 %. In general, deposition of a conductive ZnO film on top of a ZnSe/CIS structure resulted in either shunted or inflected I-V characteristics. Two approaches were investigated for depositing ZnO buffer layers, namely, chemical bath deposition and chemical vapor deposition. CVD ZnO buffer layers are grown by reacting a zinc adduct with tetrahydrofuran. Best results were obtained for ZnO buffer layers grown with a substrate temperature (T_{sub}) ≈ 225°C to 250°C. These studies concentrated on Siemens graded absorber material (CIGSS). ZnO/CIS solar cells have been fabricated by first depositing a ZnO buffer layer, followed by deposition of a low resistivity ZnO top contact layer and an Al/Ag collector grid. Several cells were fabricated with an area of 0.44 cm^2 that have total area efficiencies greater than 11 %. To date, the best performing ZnO/CIS cell was measured by NREL to have a total area, AM1.5G efficiency of 11.3 %. The active area efficiency of the device was approximately 12 %, which appears to be the best result for a ZnO buffer layer. In general, we find that ZnO buffer layers should have a resistivity > 1000 ohm-cm and have a thickness from 200 Å to 600 Å. CIS cells studies with ZnO buffer layers grown by CBD also show promise. Finally, simulation studies were carried out using the one-dimensional code, PC-1D.

1. INTRODUCTION AND BACKGROUND MATERIAL

This report concerns work carried out during the period 2/15/92 through 11/16/95 to investigate $CuInSe_2$ (CIS) and CIS alloy solar cells based on ZnSe and ZnO buffer layers. Background information, program objectives and the technical approach are discussed in the remainder of this section, and technical progress made during the program is discussed in subsequent sections.

1.1 Background Material

The key objectives of this effort were to determine if ZnSe and/or ZnO are viable alternatives to CdS for the wide bandgap, n-type buffer layer in CIS cells. Although efficiencies > 17 % have been achieved for laboratory cells with CdS windows, an alternative to CdS may be desirable because of the potential problems presented by the use of Cd in a production process. In particular, even though efficient CIS and CIS alloy cells may incorporate CdS layers with thicknesses of only 200 Å to 400 Å, the problems associated with waste handling in a production facility may present serious problems.

Other studies of ZnSe/CIS and ZnO/CIS cells are rather limited. Nouhi and coworkers reported on ZnSe/CIS solar cells fabricated by depositing ZnSe films onto CIS substrates supplied by industrial laboratories [1]. ZnSe films were deposited by reactive magnetron co-sputtering of Zn and In dopant in Ar/H_2Se. The ZnSe films were relatively low in resistivity, say, 20 ohm-cm. Efficiencies of 7 to 8.5% were obtained with ARCO supplied CIS substrates. Work was also carried out by Yoo, et al. [2]. This study involved fabrication of cells with a thin insulating layer of ZnSe between the base CIS layer and the CdS emitter. Cells were fabricated by depositing ZnSe onto CIS substrates provided by ARCO. The ZnSe films were deposited by physical vapor deposition. Cells exhibited low efficiencies primarily due to the ZnSe layers being highly resistive. More recently, the European group (EUROCIS) reported on studies of Cd-free CIS cells, including results for devices with ZnSe buffer (window) layers [3]. The ZnSe layers were grown by CBD,

whereas our work involves ZnSe films grown by MOCVD. An open circuit voltage of 423 mV and a fill factor of 56 % was reported for a ZnSe/CIS cell in Reference 3.

Prior to this work, the best results published for a direct ZnO/CIS cell consisted of an active area efficiency of 10.5 % and an open circuit voltage of 0.398 Volts achieved by the European CIS group [3]. The EUROCIS work was based on RF sputtered ZnO window layers. The best results were obtained when the ZnO window layer was sputtered from an undoped ZnO target and without the use of oxygen in the plasma, the so-called oxygen-free process. This work has involved ZnO window layers grown by MOCVD.

1.2 Program Objectives

The primary objective of this program is to provide an alternative to CdS for the buffer layer material for efficient CIS and CIS-alloy solar cells. In particular, the use of ZnSe and/or ZnO buffer layers is expected to lead to solar cell structures with efficiencies greater than 14 %. A discussion of the technical approach being used to meet these objectives follows.

1.3 Technical Approach

To achieve the primary objective of this effort, the program was structured into four tasks: (1) Buffer layer growth and optimization; (2) CVD growth of doped ZnO for a top contact layer; (3) Cell fabrication; and (4) Device measurements and modeling. Task 1 was concerned with the growth of ZnSe and ZnO for buffer layers and optimization of the process to maximize cell efficiency. Task 2 involved the growth of low resistivity ZnO for a top contact. Task 3 consisted of complete CIS cell fabrication with ZnSe and ZnO buffer layers. Task 4 involved device diagnostic measurements and simulation studies with PC-1D.

Results of these studies are discussed in the following sections: CVD growth of ZnSe; CVD and CBD Growth of ZnO; CIS substrates; CIS cells based on ZnSe buffer layers; CIS cells based on ZnO buffer layers; and Modeling calculations for resistive buffer layers.

2. GROWTH AND CHARACTERIZATION OF ZnSe

ZnSe buffer layers have been grown by CVD. Details of the growth procedure and some characteristics of ZnSe films are discussed in the following sections.

2.1 CVD Growth Of ZnSe

Growth of ZnSe is accomplished in a SPIRE 500XT reactor housed in the Electronic Materials Laboratory at WSU Tri-Cities by reacting a zinc adduct with H_2Se. The zinc adduct is formed (by a vendor) by reacting triethylamine (TEN) and dimethylzinc (DMZn). The triethylamine is mixed to give a vapor pressure of 16 torr at 20°C. Growth rate of ZnSe is controlled by adjusting the flow of hydrogen through the metalorganic bubbler. The growth rate varies linearly with the flow of hydrogen through the DMZn/TEN bubbler. Typical growth conditions that result in a ZnSe growth rate of 1 Å/s are as follows: a total pressure of 65 torr, 6000 sccm of palladium-diffused hydrogen; 25 sccm hydrogen bubbled through the DMZn/TEN bubbler at 20°C giving 24.3 μmol/min of zinc adduct; 270 sccm hydrogen selenide (1% in H_2) giving 110 μmol/min of H_2Se; and a substrate temperature of 250°C.

Iodine has been used to dope ZnSe n-type. In particular, ethyliodide mixed with helium (1000 ppm) is utilized as a source of iodine. The flow of the ethyliodide/helium mixture is usually set at 100 sccm giving 4.1 μmol/min of ethyiodide. The ethyliodide/helium mixture is also utilized to determine if the CVD system is sealed properly prior to growth of semiconductor films in the WSU reactor.

2.2 Characterization Of ZnSe Films

ZnSe films grown on CIS substrates have a strong (111) orientation. Figure 1 gives X-ray diffraction (XRD) results for a ZnSe film grown by MOCVD on a Siemens substrate at 200°C. Note the strong ZnSe (111) line intensity along with the CIS (112) line intensity. Most of the growth of ZnSe has been carried out at substrate temperatures between 200°C and 250°C. X-ray diffraction studies indicate that the ZnSe films grown on CIS exhibit a

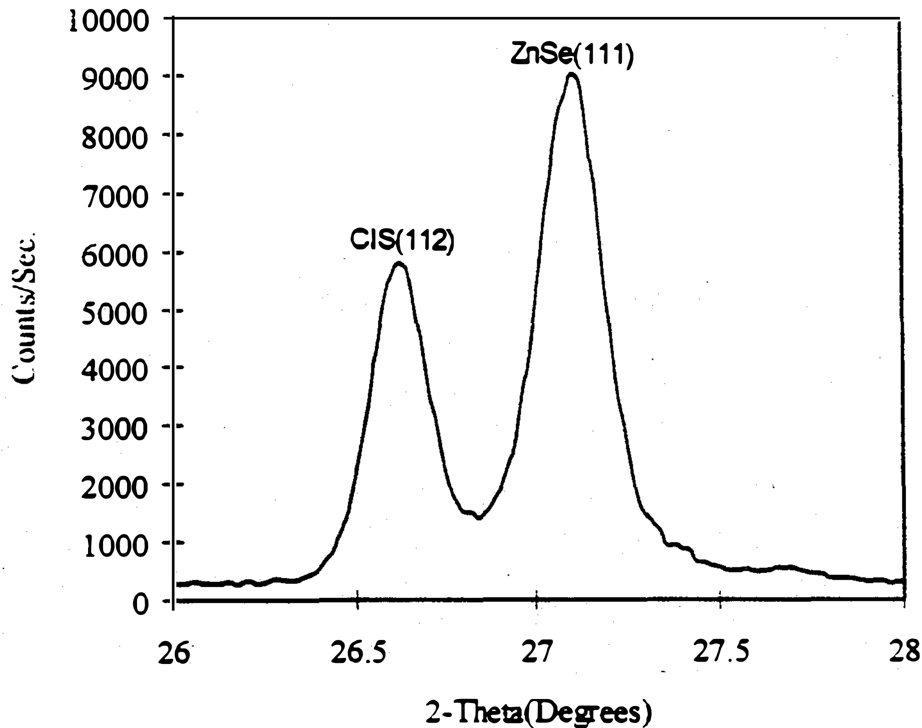


Figure 1. XRD plot showing the (112) reflection of the CIS substrate and the (111) reflection from ZnSe.

strong (111) orientation while the CIS substrates exhibit a strong (112) orientation.

Ethyliodide has been utilized to successively dope ZnSe films. Using a flow of 100 sccm for the ethyliodide/helium mixture, ZnSe films grown on semi-insulting GaAs at 250°C typically exhibit a resistivity of 0.05 ohm-cm. The resistivity was measured with a four point probe. When conducting such measurements on ZnSe it is necessary to utilize indium contacts that have been heat treated above 200°C. Based on studies of CIS cells with ZnSe buffer layers it appears that iodine-doped ZnSe films grown on CIS have a much higher resistivity than films grown on GaAs.

3. CVD AND CBD GROWTH OF ZNO

ZnO films are being investigated as buffer layers in CIS cells and for the top contact film. Two approaches are utilized for buffer layer formation, namely, chemical vapor deposition (CVD) and chemical bath deposition (CBD). Only CVD ZnO films are appropriate for top contact layers. In the following sections the approach used for both of these growth methods and properties of the two types of ZnO films are discussed.

3.1 CVD Growth Of ZnO For Top Contact Layers

The WSU SPIRE 500XT reactor was modified for ZnO growth. Tetrahydrofuran (THF) is utilized as a source of oxygen, while the zinc adduct used for the growth of ZnSe is also utilized for ZnO growth. The THF liquid is stored in a room temperature bubbler and introduction of THF vapor into the reactor is controlled by a PFD Model 1004 gas flow control system. THF has been used with DMZn by other researchers to grow ZnO at substrate temperatures greater than 300°C [4,5]. Studies discussed herein involved ZnO film growth with substrate temperatures in the range of 100°C to 350°C.

Several approaches were investigated to achieve conductive films. One approach simply involves adjusting the VI/II ratio to a relatively low value of 55 (compared to values of 400 for resistive films) to achieve Zn-rich, low resistivity ZnO films. As shown in Figure 2, Zn-rich films were grown with substrate temperatures between 100°C and 150°C. The lowest resistivity attained was 0.01 ohm-cm. These films were quite transparent but gradually oxidize at room temperature. A measure of ZnO film thickness is obtained from optical transmission measurements made on a film grown on a glass witness, and an estimate of the resistivity is obtained with a four point probe measurement on a film grown on semi-insulating GaAs as well as from the film on glass. Film thicknesses were also determined from optical reflection measurements from films grown on silicon witnesses.

Studies of boron- and iodine-doped films were conducted by using diborane and ethyliodide as sources of boron and iodine. Substrate temperatures between 175°C and 275°C, and between 200°C to 300°C were

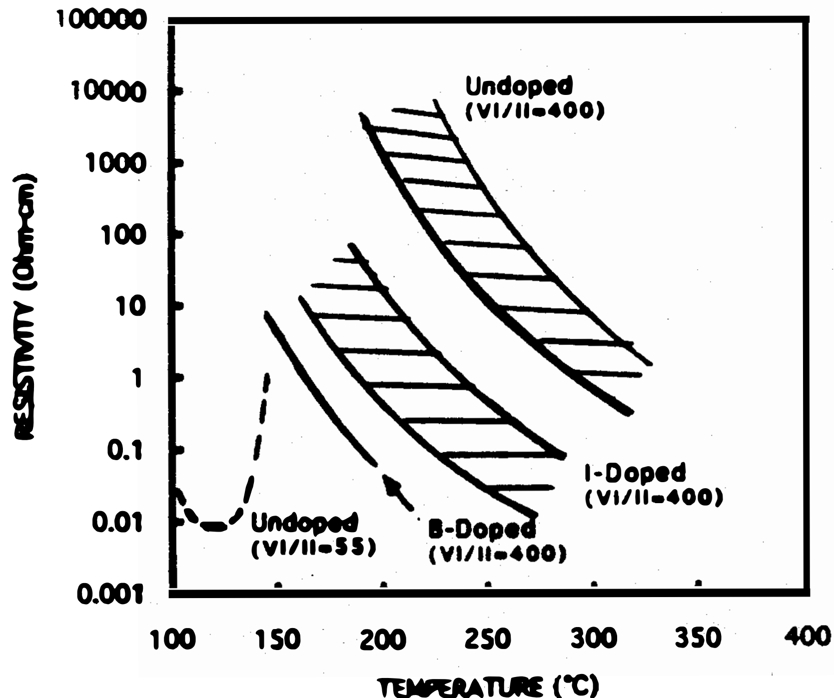


Figure 2. ZnO film resistivity versus temperature.

utilized for boron and iodine doping, respectively. A range of resistivity values was observed for each substrate temperature. At the time the doping studies were being done, we were not aware of the tendency for these ZnO films to oxidize; thus, the range of resistivity values observed at each substrate temperature may be related to oxidation effects.

It is desirable to have a top contact layer that is characterized by a sheet resistance less than 100 ohms/sq., so that a collector grid with less than 10 lines/ cm can be used to complete cell fabrication. These studies have not yet yielded a low temperature growth approach that provides ZnO films with stable, low values of sheet resistance.

3.2 CVD Growth Of ZnO For Buffer Layers

ZnO buffer layers must be very resistive. In particular, we find that the buffer layer resistivity should be greater than 1000 ohm-cm. High resistivity

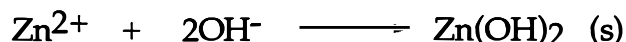
ZnO is obtained consistently if no doping and a VI/II ratio of 400 are utilized. The WSU approach to growing ZnO buffer layers is distinguished from other approaches for growth of ZnO buffer layers in two important ways, namely: (1) The zinc and oxygen precursors are both relatively large molecules; and (2) no extra oxygen, H_2O molecules or ions are involved in the deposition process. Substrate temperatures (T_{sub}) have been varied from 100°C to 350°C, with the best device performance obtained for $T_{sub} \approx$ 200°C to 250°C. It is desirable to know the thickness and resistivity of ZnO films grown on CIS. Results for CIS cells with ZnO buffer layers are discussed in Section 6.

3.3 Chemical Bath Deposition (CBD) Of ZnO For Buffer Layers

Studies were also made of ZnO buffer layers deposited by solution growth, or chemical bath deposition (CBD). A two step procedure is used, namely: (1) a $Zn(OH)_2$ film is grown from the bath and then converted into a zinc hydrous oxide film, $ZnOxH_2O$, by exposing it to air; (2) the final ZnO film is obtained by heat treating in air at 180°C. Further optimization of the growth procedure is needed, but a baseline process was developed and used to grow buffer layers for CIS solar cells. Further discussion of our baseline process follows.

A chemical bath is prepared by mixing zinc sulfate with ammonium hydroxide. After heating the chemical bath to 40°C, CIS substrates are lowered into the bath, and then after a suitable amount of time, the substrates are removed and allowed to dry for approximately one hour. The films are then heat treated in air at 180°C.

There are two key reactions occurring that determine the nature of the hydroxide film that grows on the substrate. First, free Zn^{2+} ions in an aqueous ammonia solution undergo hydrolysis precipitating a solid phase of zinc hydroxide:



$$Zn^{2+} + 2OH^- \longrightarrow Zn(OH)_2 \ (s)$$

the reaction is very fast and uncontrolled resulting in homogeneous

precipitation in the solution. A film deposited as a result of this reaction is a B-quality film, that is, it is not adherent and rather 'powdery'. In order to obtain an A-quality film - one that is adherent and smooth - the above reaction must be controlled with a complexing agent.

The $Zn(OH)_2$ precipitates are readily dissolved in an excess of ammonia, to form the zinc tetra amine complex $[Zn(NH_3)_4]^{2+}$ by the reaction:

$$Zn^{2+} \quad + \quad NH_3 \quad \text{———} \quad [Zn(NH_3)_4]^{2+} \ (aq)$$

Once the zinc hydroxide precipitates are dissolved, the bath temperature can be raised until the second reaction begins to proceed backwards and a film of $Zn(OH)_2$ is deposited by an ion-by-ion deposition process. This process is made possible because the equilibrium constant for the second reaction increases more rapidly with temperature than the constant for the first reaction.

As the substrates are removed from the solution, the zinc hydroxide film oxidizes rapidly in air to form a zinc hydrous oxide [1]:

$$Zn(OH)_2 \quad \underset{\text{AIR}}{\text{———}} \quad ZnO \ x \, H_2O$$

Upon subsequent heating in air, dissociation of the hydrous oxide occurs, resulting in a pure oxide film [2,3]:

$$ZnO \ x \, H_2O \ \xrightarrow[\text{HEAT}]{} \ ZnO$$

CBD ZnO buffer layers grown on CIS substrates have produced encouraging results with test cells. Studies with test cells and completed solar cells are discussed in Section 6.

4. CIS SUBSTRATES

4.1 Physical Characterization

This work has been carried out with Siemens substrates. Siemens Solar has supported the WSU effort by supplying 10 cm x 10 cm plates consisting of a CIS film deposited onto Mo-coated glass. These plates are scribed and broken into 2 cm x 2 cm substrates. Two kinds of material have been utilized, a 'standard' CIS material and the so-called 'graded absorber' material [8]. As discussed in Reference 8, the standard material is essentially $CuInSe_2$ throughout the film except near the CIS-Mo interface where Ga is added. The Graded absorber material has sulfur near the front face such that the concentration of selenium and sulfur are equal at the surface. An Auger depth profile given in Reference 8 for the graded absorber material is shown in Figure 3. It is interesting to note that the photoresponse reported for Siemens cells based on the graded absorber material is very similar to that for the standard CIS material. Thus, although sulfur and Ga are incorporated in the film, this material should not be regarded as simply CIGS with a higher bandgap. This paper concentrates on device studies based on ZnO windows deposited onto the Siemens graded absorber material. In the remainder of this paper, the graded absorber material will be referred to as CIGSS, and the term CIS will be used in a generic sense to refer to $CuInSe_2$ as well as related alloys.

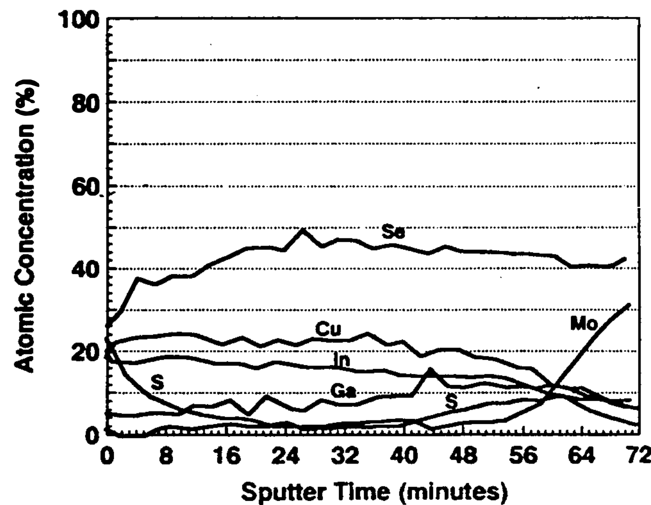


Figure 3. Auger depth profile of the graded absorber structure as published by Tarrant and Ermer in Reference 8 (included by permission).

4.2 Process Development And Properties Of Al/CIS Contacts

Al/CIS Schottky barriers have been utilized to characterize the CIS substrate surface, and for process development. For example, Al/CIS barriers were fabricated to determine the effects of surface treatments prior to deposition of a buffer layer. Attempts to form an Al/CIS Schottky barrier by vacuum depositing aluminum on as-received CIS substrates often resulted in very resistive interfaces. It was determined that a surface preparation involving degreasing with TCA, methanol and acetone followed by etching the CIS substrate with either KBr/Br/H_2O or KCN (10 % by weight) aqueous solutions prior to Al deposition leads to consistent Al/CIS Schottky barrier properties. The use of these etches were discussed by McCandless and Birkmire [9], and Tuttle, et al. [10]. KCN is a selective etch that only removes electrically degenerate precipitates of Cu_2Se from the sample surface, while KBr-Br is a polishing etch that removes approximately 0.34 μm of CIS. The requirement of the degreasing step (for consistent results) could be related to the fact that the Siemens material undergoes considerable handling. In particular, after Siemens mails material in the form of 10 cm x 10 cm plates to WSU, the plates are then broken into 2 cm x 2 cm substrates.

Al/CIS contacts were studied by depositing an array of aluminum circular areas 2.8 mm in diameter onto a CIS substrate as depicted in Figure 4. The individual diodes have areas of .06 cm^2. Al films are deposited with a

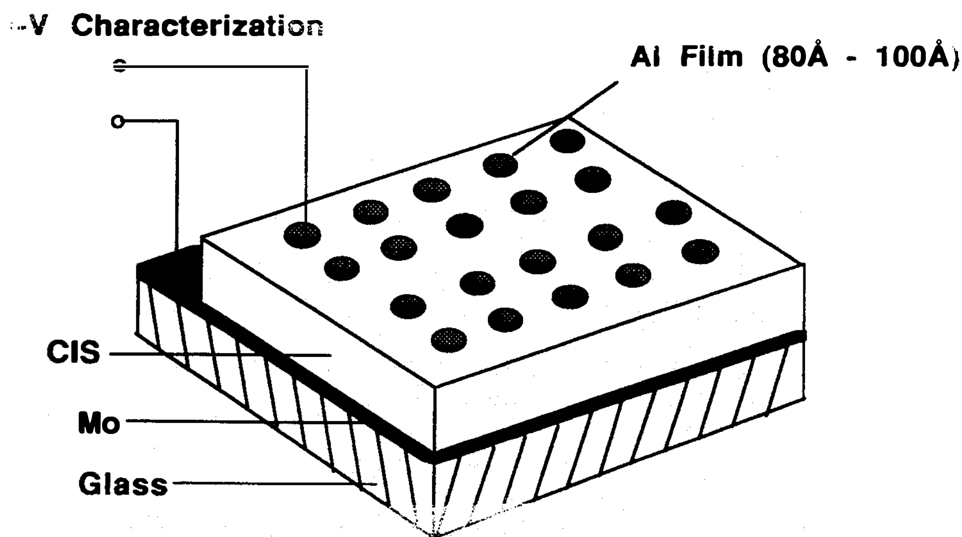
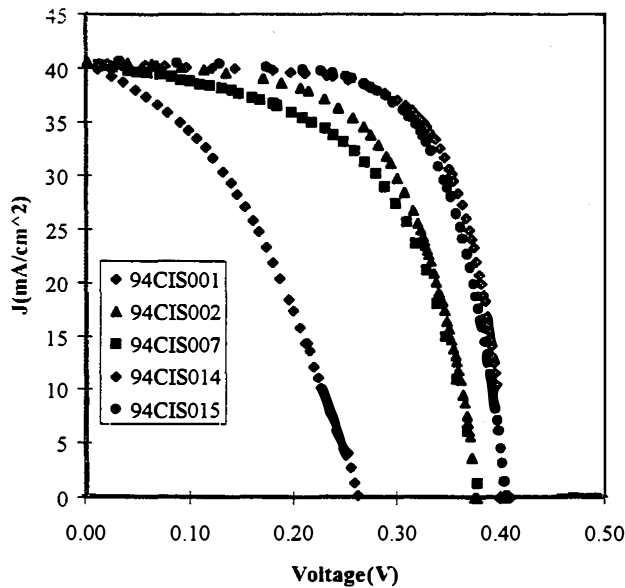


Figure 4. Al/CIS test cell configuration.

thickness of 100 Å to 150 Å and at a rate greater than 10 Å/sec so that light can pass through the film and to minimize the sheet resistance. Illuminated characteristics of test cells are taken by illuminating the device with an intensity such that the short-circuit current is approximately 40 mA/cm^2. Since the Al film typically transmits only 20 % of the incident light, the illumination intensity is five times greater than would normally be used to simulate an AM1.5 spectrum. It is important to note, however, that the actual photon flux entering the test cell is approximately correct for AM1.5 simulation. Since there are no collector grids on test cells to shadow incident light, we consider the test cell values of J_{SC} and efficiency to be active area numbers. The value of 40 A/cm2 for Al contacts formed on Siemens CIGSS and CIS substrates is justified since active area values of 39.2 and 41.0, respectively, were reported for cells based on these materials.

Illuminated I-V characteristics of Al/CIS contacts for CIS substrates prepared in various ways are given in Figure 5. In addition to the use of KCN and KBr-Br etches, results are also given for Al/CIS contacts formed on CIS substrates that were subjected to H_2Se at 250°C after cleaning and etching



Surface Treatment	Sample
Cleaned	94CIS001
KCN	94CIS002
KBr-Br	94CIS007
KCN /H_2Se	94CIS014
KBr-Br / H_2Se	94CIS015

Figure 5. Illuminated Characteristics of Al/CIS contacts for CIS substrates.

steps. The effect of the selenization process was very significant as indicated by the improved test cell properties. However, the improvement due to the selenization treatment gradually disappeared over a period of a few days. The most significant result of these studies, as far as impact on approach to cell fabrication during this program, is that for KCN etched substrates. The properties of a test device such as 94CIS002 are quite stable. The approach to substrate surface preparation used for 94CIS002 was adopted in this program for investigation of CIS cells with ZnSe and ZnO buffer layers.

In addition to process development, analyses of current voltage characteristics of Al/CIS contacts have been valuable for formulating a model for the electronic character of Siemens substrates. Figure 6 gives T-I-V data taken for 94CIS002, and the inserted Table lists results of fitting the data with a single mechanism model. In general, it was found that Al/CIS and Al/CIGSS contacts could be understood with a single mechanism model, whereas test cells and completed solar cells with ZnSe and ZnO buffer layers must utilize a model involving two current mechanisms. The T-I-V data taken under dark conditions are fit very well with the following expression,

$$I = I_o \exp(B\, V_{jct}) + V_{jct}/Rsh \qquad \text{for} \qquad V_{jct} >> kT$$

with kT being expressed in eV and B being independent of temperature. As indicated by the tabulated, experimental values of B, this parameter is clearly temperature independent. A current loss mechanism characterized by a temperature independent value of B can be interpreted as being due to multiple step tunneling. This conclusion is used below to formulate a model for the electron band structure of the Siemens CIS and CIGSS materials. It should be noted that the device current is plotted versus load voltage in Figure 6. As a result, a slight curvature exists in the log I vs V plots particularly at higher voltages. If log I is plotted versus $V_{jct} = (V - R_sJ)$, the plots are quite linear and parallel.

Al/CIS contacts were also used to determine a proper model for the band structure at CIS substrate surfaces. Specifically, it is of interest to know whether or not the surface is inverted, under flat band conditions, characterized by a n-type segregated phase, or a depleted n-type segregated

I-V Parameters For Al/CIS Device 94CIS002

ϕ = 0.155 eV and J_{00} = 9.40E-02.

T(°C)	J_0(A/cm^2)	A	B(1/eV)	R_s(Ω)	R_{sh}(Ω)
-30.0	6.99E-05	3.54	13.46	87.0	1.16E+05
-20.0	8.45E-05	3.36	13.64	72.3	1.14E+05
-10.0	1.12E-04	3.28	13.46	57.3	1.00E+05
0.0	1.00E-04	3.09	13.77	49.9	1.00E÷05
10.0	1.43E-04	3.04	13.49	36.4	5.85E+06
20.0	1.67E-04	2.87	13.80	27.6	5.85E+06
30.0	2.38E-04	2.85	13.44	19.0	5.84E+06
40.0	3.22E-04	2.76	13.44	12.3	5.84E+06
50.0	3.94E-04	2.58	13.91	8.65	5.84E+06
60.0	5.29E-04	2.50	13.93	4.86	5.84E+06

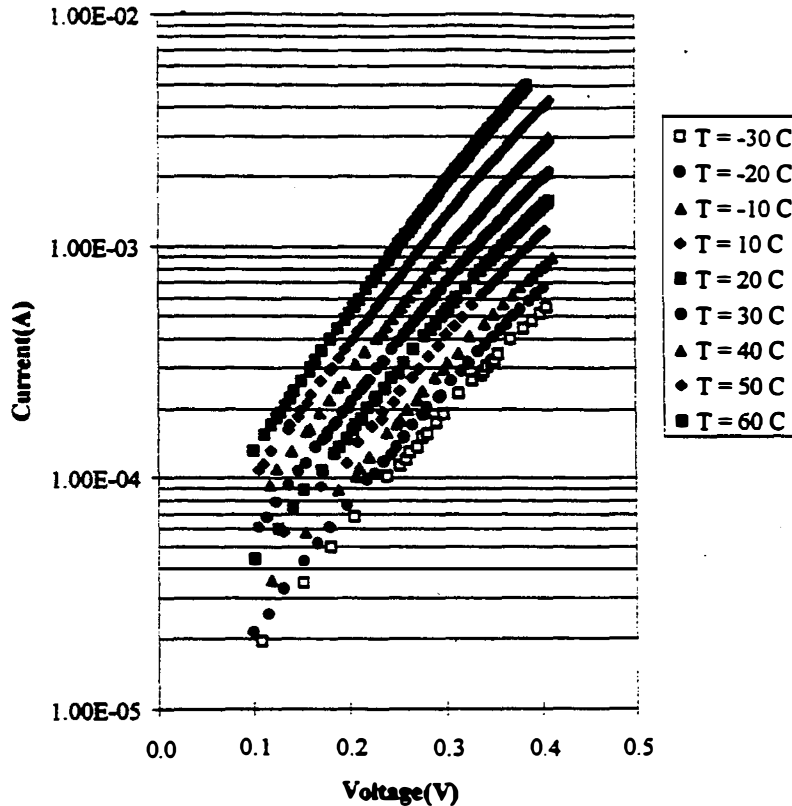


Figure 6. Dark T-I-V data taken for Test Cell 94CIS002.

phase. These studies do not provide all the answers, but we think the results and conclusions are relevant and interesting. Figure 7A describes the approach used for this study. Prior to deposition of Al, the substrates were etched in KCN solution as previously described. Figure 7B gives I-V data taken for a CIGSS substrate. Two key conclusions result from current-voltage measurements acquired with terminals 3-1, 2-1 and 2-3 under dark conditions: (1) I-V characteristics using terminals 3-1 and 2-1 result in diode curves as shown for the 3-1 case in Figure 1B; (2) I-V characteristics measured between 2-3 are as expected for two back-to-back diodes - in fact, the data for negative voltages for the two measurements (between 3-1 and 2-3) are essentially on top of each other.

These conclusions are consistent with the model described by Figure 8, where we have attempted to describe the electron band structure at the surface under the Al contacts and between the Al contacts along the CIS surface. Note that we have not attempted to account for the sulfur at the CIGSS surface by indicating a larger bandgap than in the bulk. The bandgap at the surface is not important to this discussion. If one considers a line between an Al contact and the Mo, a Schottky barrier at the Al/CIS interface gives rise to diode characteristics. If one considers a path from Al contact to Al contact (2 to 3, say), back to back diodes exist and are responsible for the reverse diode characteristics for both positive and negative voltages in Figure 7.

The surface is described as essentially intrinsic in Figure 8. There are two situations for which the CIS surface between Al pads would be inverted, one due to surface states, and the other from a highly doped n-type surface layer. Both of these situations would lead to diode curves when the I-V measurement is made between terminals 3 and 1, or 2 and 1. I-V measured between 2 and 3, however, would result in relatively high conductance compared to the reverse diode characteristics for measurements with terminal 3-1 or 2-1. Therefore, we rule out the possibility that the CIGSS surface is inverted. This conclusion does not rule out the possibility that a segregated phase exists at the material surface. It seems clear, however, that if a n-type layer exists at the surface that would normally be n-type (when isolated), the layer is depleted when in contact with p-type CIS.

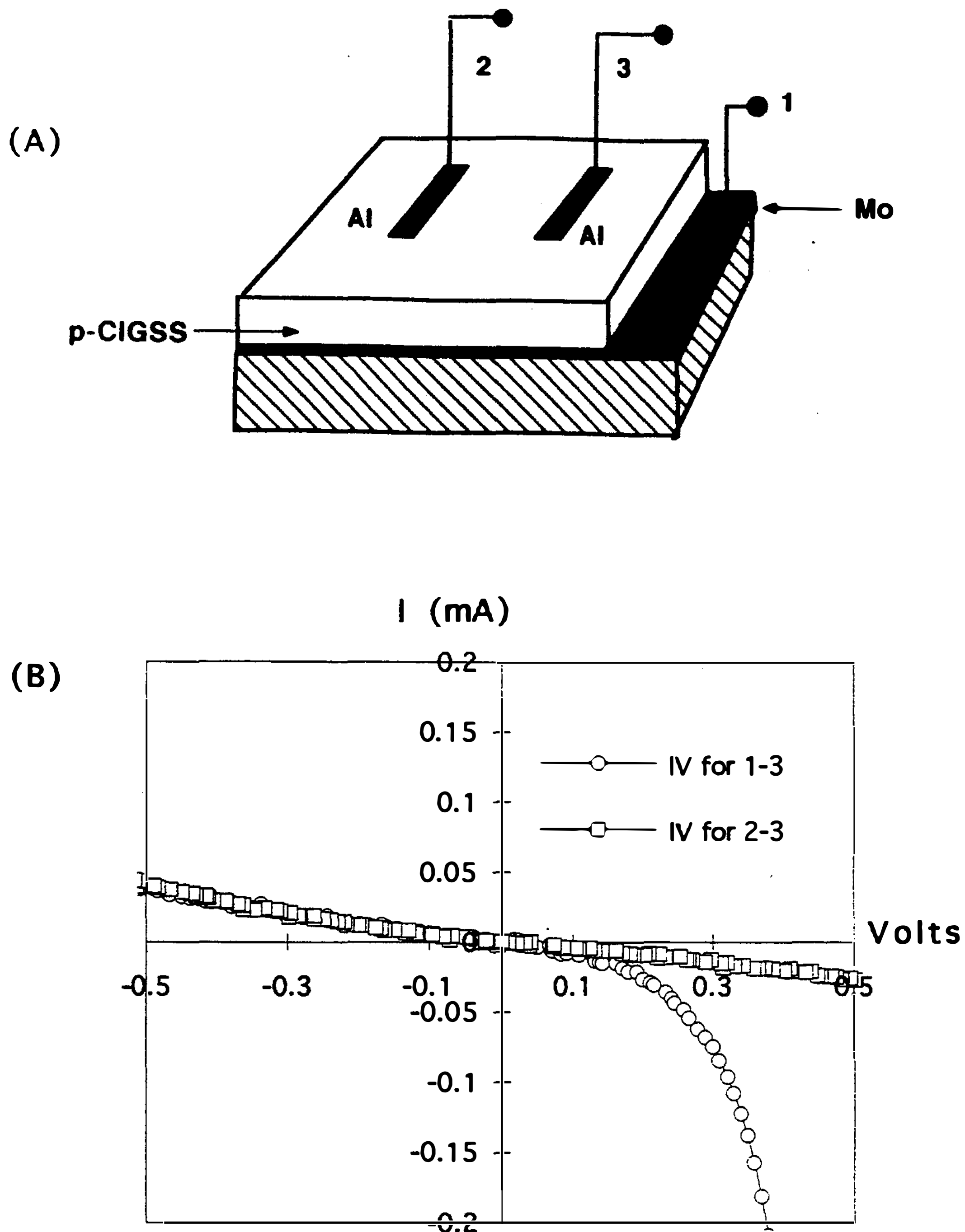


Figure 7. (A) Test configuration for characterizing Al/CIS contacts ; (B) Current-voltage characteristics under dark conditions between terminals as indicated.

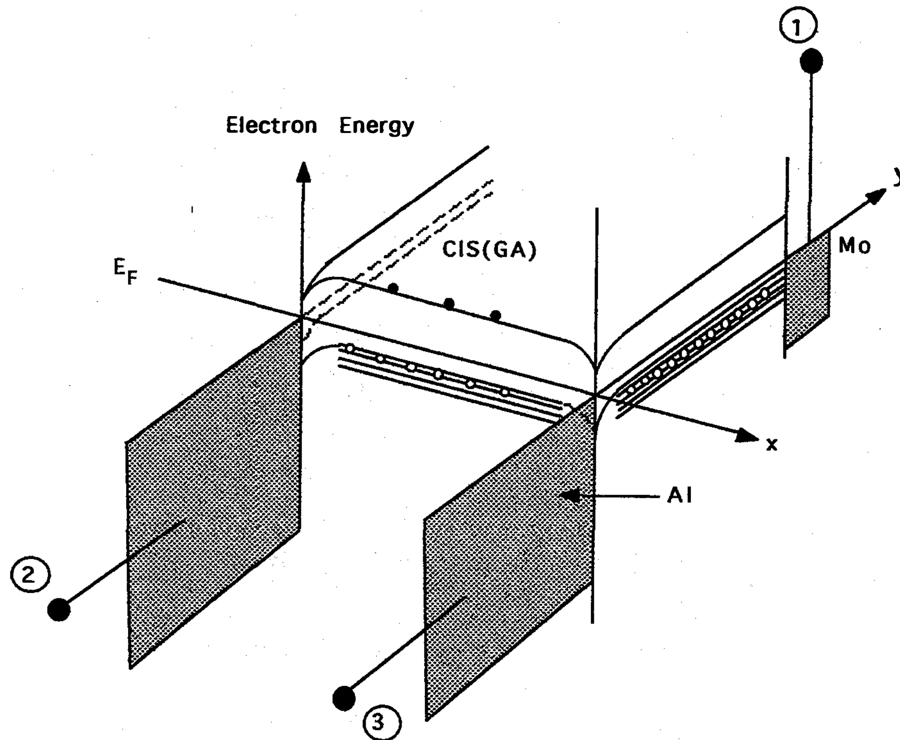


Figure 8. Electron band structure for a CIS sample with Al contacts and the CIS surface between the Al contacts being under approximately flat-band conditions (non-inverted).

Thermoprobe measurements were also carried out to characterize the surface condition. Figure 9 depicts the experimental arrangement. The vacuum deposited, rectangular Al pads are 400 to 500 Å thick. Heat is applied with a small cylindrical heater by letting it touch a glass slide placed between the heater and CIS surface at one end of the sample (tip of arrow). Surface temperatures were measured with an infrared microscope. The experimental arrangement in Figure 9A is such that the sign of ΔV indicates the dominant carrier for surface conduction from Al pad #3 to #2. Results obtained for Siemens CIS, CIGSS and CIS material from EPV are tabulated in Table 1. In all cases, the thermoelectric voltage was essentially zero under dark conditions. Figure 9B describes the electron band structure for a non-inverted surface when heat is being applied. Electrons and holes move across the surface due to the thermal gradient. In general, when there are two types of carriers that can contribute to the voltage, the effective Seebeck coefficient is given by

$$\alpha = \frac{\alpha_1 \sigma_1 + \alpha_2 \sigma_2}{\sigma_1 + \sigma_2}$$

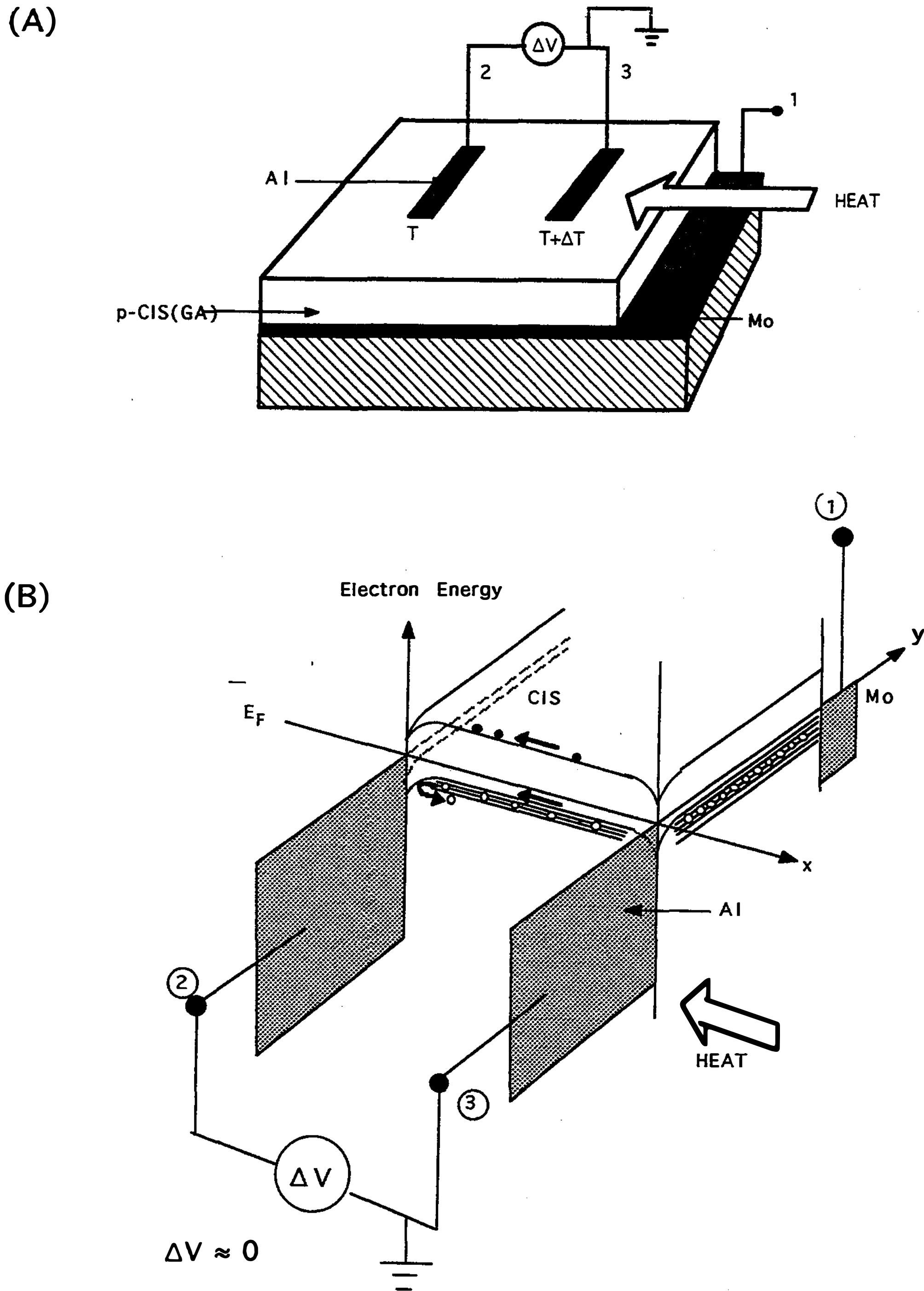


Figure 9. (A) Approach to measuring thermoelectric voltage between Al contacts on the sample surface; (B) Non-inverted surface condition consistent with thermoprobe results.

TABLE 1 -- Thermoelectric Probe Studies Of CIS Samples

Illumination Condition	Temperature Difference (°C)	Voltage Difference (μV)	Effective Seebeck Coefficient (μV/°C)
Siemens CIS			
Dark	8	- 5.0	- 0.6
Room Light	13	- 480	- 37
Siemens CIGSS			
Dark	12	- 95	- 7.9
Room Light	13	- 1770	- 136
EPV CIS			
Dark	10	- 102	- 10
Room Light	9	- 2300	- 256

where α_i and σ_i are the Seebeck coefficient and conductivity of the ith carrier, respectively. The low values of Seebeck coefficient for dark conditions suggest that the surface is nearly intrinsic. If light is allowed to create electron-hole pairs at the surface, the electrons become the dominant carrier leading to a significant negative Seebeck coefficient. Inclusion of the Al/CIS barriers at the terminals presents a more complicated problem than one normally assumes when considering a thermoelectric measurement, but it would appear that the barriers would tend to block hole flow, thus allowing electrons to become the dominant carrier under illuminated conditions. Both the I-V and thermoprobe studies indicate that the electron bands at the surface of Siemens material (both CIS and CIGSS) are not inverted.

These studies may not have an impact on anyone's approach to cell fabrication. However, these studies indicate that the buffer layer and top contact layer must play a part in achieving inversion at the CIS surface (for the materials studied), and therefore, are playing a role in formation of the "working junction."

5. CIS SOLAR CELLS BASED ON ZnSe BUFFER LAYERS

5.1 Optimization Of ZnSe Buffer Layers

ZnSe/CIS structures have been studied by depositing an array of aluminum circular areas 2.8 mm in diameter onto the ZnSe film to form Al/ZnSe/CIS test cells as depicted in Figure 10. The approaches used to deposit aluminum and to characterize the test cells are the same as described in Section 4.2. Figure 11 gives illuminated I-V characteristics for a test cell formed on a CIGSS substrate, 94ZC480. When Jsc is set to 40 mA/cm^2, the estimated active area efficiency is 14.82 %. This is one of the best test cell results obtained for a Al/ZnSe/CIS structure.

Extensive studies have been carried out for Siemens CIS and CIGSS substrates. Figure 12 describes the range of results for ZnSe/CIS structures as the ZnSe thickness is varied. Generally, it is found that for ZnSe thicknesses greater than 250 Å, inflected I-V curves result and values of J_{SC} are reduced. As a result, the test cell efficiency is reduced. The decrease in photocurrent can be interpreted to be a result of the formation of a significant conduction band spike at the ZnSe-CIS interface, as predicted (0.85 to 0.9 eV) in Reference 11 for an interface between relaxed, bulk layers of ZnSe and CIS. The key difference between test cells made on CIS substrates and graded absorber substrates seems to be that the required ZnSe thickness for maximum performance is less in the case of the CIGSS substrates.

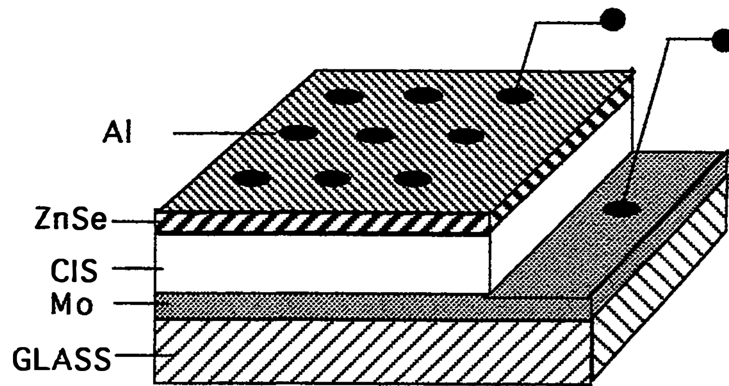


Figure 10. Configuration of test cells on ZnSe/CIS structure.

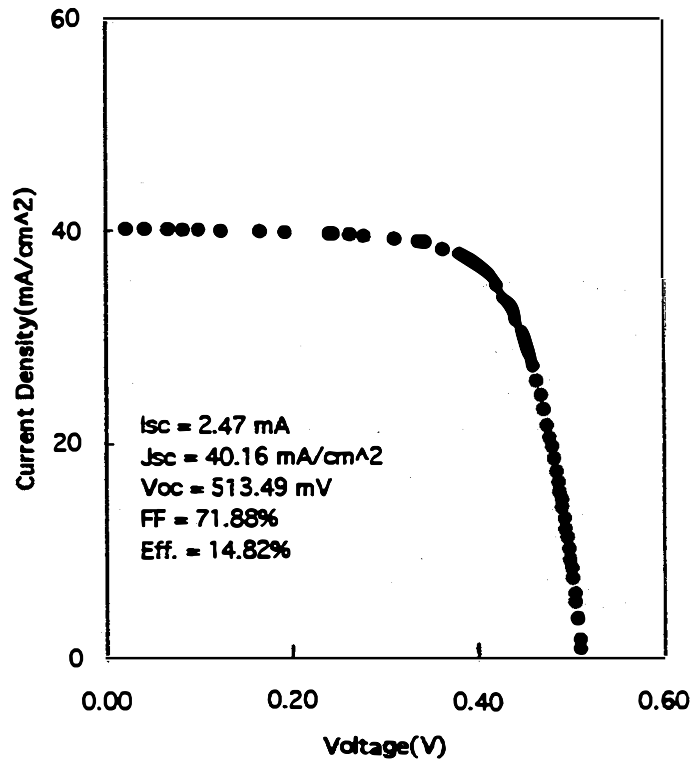


Figure 11. Illuminated characteristics for a test cell formed on graded absorber material (94ZC480).

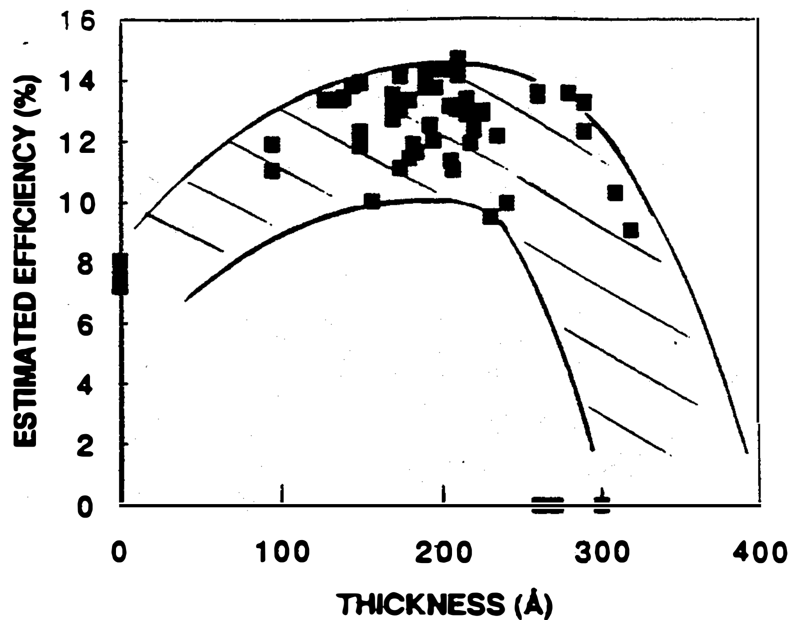


Figure 12. Estimated active area efficiency for test cell structures vs ZnSe thickness.

Temperature dependent current-voltage (T-I-V) analyses have been conducted for numerous devices. The effect of depositing the ZnSe layer is apparent when one compares results of the T-I-V analyses carried out for Al/CIS and Al/ZnSe/CIS structures. Typical dark characteristics for a Al/ZnSe/CIS structure are plotted in Figure 13, and fitting parameters are given in the inserted table. As is always the case for Al/ZnSe/CIS devices, the I-V characteristics appear to involve two current mechanisms, one dominant at low voltages (0 to 0.35 Volts), and one dominant at higher voltages (0.35 to 0.6 Volts).

In general, we assume the dark I-V characteristics can be interpreted in terms of

$$I_j = I_1 + I_2$$

where

$$I_1 = I_{01}[\exp(B_1 V_j) - 1]$$

$$I_2 = I_{02}\exp(B_2 V_j) \quad , \quad V_j >> n_2 kT$$

$$B_1 = (A_1 / kT)$$

$$B_2 = (A_2 / kT)$$

$$V_j = V - R_s I = \text{Voltage Across Junction}$$

$$I_j = I - V_j/R_{sh}$$

$$R_s = \text{Lumped Series Resistance}$$

$$R_{sh} = \text{Lumped Shunt Resistance}$$

It should be noted that the B-parameters may be temperature-independent, and in that case it is not appropriate to relate B_i to A_i, where i = 1 or 2.

The procedure utilized to fit I-V data is discussed in Reference 12. I-V characteristics of ZnSe/CIS structures always exhibit two current mechanisms, one dominant at low voltages (0.1 to 0.35 Volts) and one at higher voltages (0.35 to 0.6 Volts). The low voltage mechanism appears to be due to tunneling since usually the B-factor is fairly independent of temperature. The low voltage mechanism in the ZnSe/CIS devices is always less in

I-V Parameters For Al/ZnSe/CIS Device 94ZC436

ϕ_1 = 0.198 eV and $J_{00,1}$ = 0.688. ϕ_2 = 0.405 eV and $J_{00,2}$ = 0.654.

T(°C)	J_{01}(A/cm²)	B_1(1/eV)	J_{02}(A/cm²)	A_2	B_2(1/eV)	R_s(Ω)	R_{sh}(Ω)
-30	5.05E-05	6.42	2.54E-09	1.94	24.57	12.5	1.92E+05
-20	8.68E-05	5.65	7.90E-09	1.92	23.85	9.71	1.26E+05
-10	1.16E-04	5.59	1.03E-08	1.82	24.33	7.86	2.93E+05
0	1.47E-04	5.54	1.59E-08	1.72	24.76	8.17	1.37E+05
10	1.96E-04	5.51	1.26E-08	1.55	26.48	8.26	1.16E+05
20	2.16E-04	5.93	9.60E-09	1.40	28.37	8.74	6.30E+04
30	2.10E-04	5.82	4.21E-09	1.21	31.69	10.1	2.37E+04
40	4.78E-04	4.93	1.68E-07	1.49	25.03	5.91	2.75E+04
50	5.95E-04	5.03	4.08E-07	1.49	24.09	1.68	1.86E+04

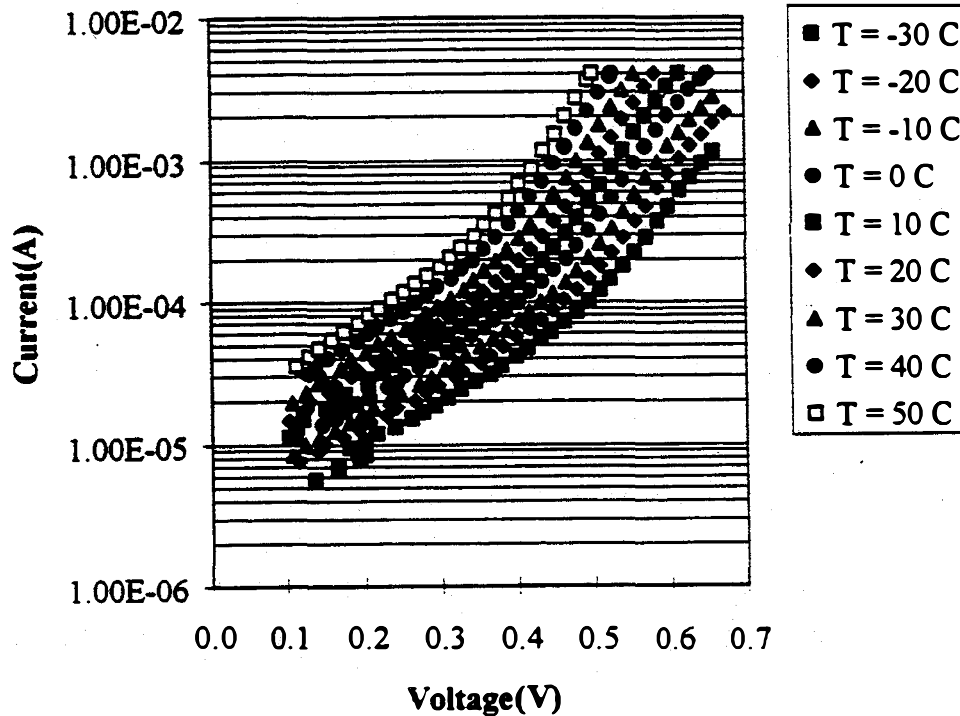


Figure 13. T-I-V data for Al/ZnSe/CIS Test Device 94ZC436.

magnitude than the single current mechanism which dominates the Al/CIS structures. The J_{o1} - value for the tunneling-like components for the Al/CIS and ZnSe/CIS devices are approximately the same, but the B-value for a typical Al/CIS device is much larger than the corresponding parameter for a ZnSe/CIS structure. The J_{o1} - values being similar suggests that the phenomena involved are similar. Simulation studies using PC-1D are currently underway to further examine the difference between the I-V characteristics of Al/CIS devices and structures with buffer layers.

Identification of the large-voltage current mechanism is not straight forward for test cell 94ZC436. Both the A-factor and B-factor exhibit a slight temperature dependence. Since the A-factor is on the order of 1.5, it seems reasonable to assume that the dominant current loss is due to space charge recombination. However, a tunneling/recombination model may be more appropriate in this case [13]. The values for J_{o2} and A_2 for 94ZC436 are similar to those reported for efficient CIS solar cells using CdS windows. In general, we find that T-I-V analyses conducted for Al/ZnSe/CIS test cells indicate that the ZnSe buffer layer suppresses the tunneling currents dominant in the Al/CIS structures.

5.2 Completed ZnSe/CIS Solar Cells

Completed cells were fabricated by sending ZnSe/CIS structures to Siemens for deposition of a low resistivity ZnO top contact layer, and depositing a collector grid onto the ZnO/ZnSe/CIS cell structure. We found that although ZnSe structures exhibited illuminated characteristics similar to Test Cell 94ZC480, the resulting solar cell would always exhibit degraded properties due to an inflected I-V curve or a shunted I-V curve. Apparently, some aspect of the Siemens deposition process for low resistivity ZnO degrades the properties of the ZnSe/CIS structure.

A second approach utilized in the ZnSe/CIS cell development involved the use of a protective layer. First, a layer of CdS was utilized as a protective layer. After growing a ZnSe layer, 300Å to 400Å of CdS was deposited by chemical bath deposition. The CdS/ZnSe/CIS structure was sent to Siemens for deposition of the top contact layer, and then the collector

was deposited to finish the cell. Reasonable results were obtained in this manner. Illuminated properties of such a cell are shown in Figure 14. Cell 94ZC421 was based on Siemens CIS material, not the graded absorber material. The total area efficiency is 11% and the active area efficiency is greater than 12%. I-V characteristics of test cells measured before and after CdS deposition were essentially identical. Although this result is not for an actual non-cadmium structure, it demonstrates the potential of achieving efficient ZnSe/CIS solar cells.

Studies with CdS protective layers were conducted for two reasons. First, it was desirable to determine if the ZnSe/CIS junction properties observed for test cells could be preserved after carrying out the various processing steps to obtain a completed cell. This first objective was accomplished. The second reason for the study was to verify that CdS layers are rather robust, and are able to tolerate the deposition process used by Siemens for the top contact ZnO layer. These studies also suggest one other conclusion, namely, that ZnSe/CIS junctions do not degrade due to the heat treatment used by Siemens, but apparently due to the exposure of the cell structure to precursors used by Siemens in the deposition process.

Since our overall objective in this program was to investigate non-cadmium buffer layers for CIS solar cells, investigation of non-cadmium protective layers had to be examined. As our capability to deposit ZnO by CVD became available, the possibilities of using ZnO protective layers were investigated. Although a limited effort was devoted to this approach, some significant progress was made. Two approaches were considered. One procedure involved growing the ZnSe buffer layer at 250°C followed by the growth of ZnO at 250°C. The second approach consisted of depositing the ZnSe buffer layer at 250°C in one run and the ZnO protective layer at 150°C in a separate deposition step. With the first approach, the ZnO/ZnSe film grown on a glass witness appeared to have a resistivity that was too low, whereas with the second approach one could insure that both ZnSe and ZnO films were quite resistive. Although we expected the second approach to yield the best results, the best result was achieved with the first approach. Illuminated I-V characteristics are shown in Figure 15 for a cell (94XC029) that had a ZnSe buffer layer and ZnO protective layer thicknesses of

approximately 100Å and 300Å, respectively. Although the active area efficiency of 9.2% for a completed cell is encouraging, significant improvements are still required. However, after fabricating completed cells with active area efficiencies approaching 12 % with CVD ZnO buffer layers, we decided to emphasize studies based on ZnO buffer layers. These studies are discussed in the following section.

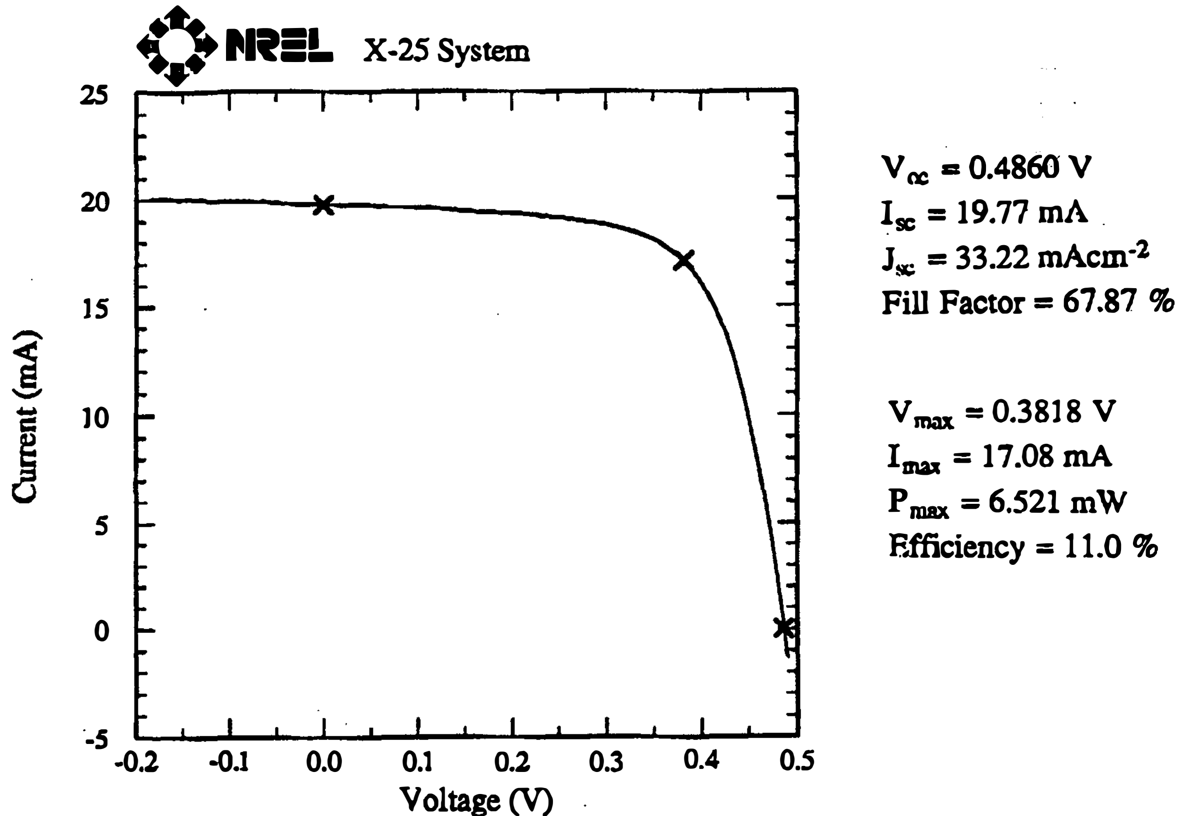
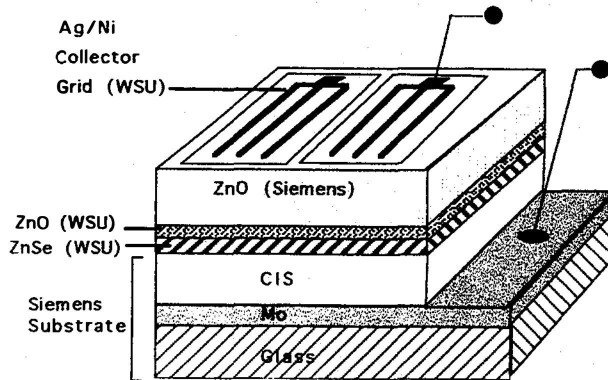


Figure 14. Illuminated I-V characteristics measured by NREL for a 0.6 cm^2 ZnSe/CIS solar cell with a ZnO top contact layer and a CdS protective layer between the ZnSe and ZnO layers.

SAMPLE XC029

AREA = 0.464 sq. cm.

NREL MEASUREMENT



Isc = 15.84 mA

Jsc = 34.12 mA/sq.cm.

Fill Factor = 54.14 %

Voc = 0.473 Volts

Efficiency = 8.74 % (9.2 %)

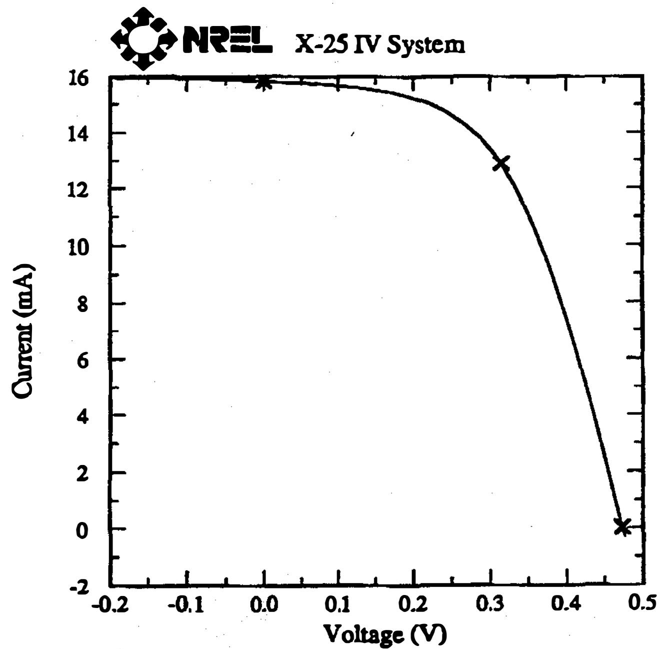


Figure 15. Illuminated I-V characteristics measured by NREL for a 0.464 cm^2 cell with a ZnSe buffer film and a CVD ZnO protective layer. The cell structure is depicted by the insert.

6. CIS SOLAR CELLS BASED ON ZnO BUFFER LAYERS

6.1 Optimization Of ZnO Buffer Layers

The same approach used in determining the optimum process for ZnSe buffer layer formation was utilized for ZnO buffer layers. In particular, investigation of optimum processing parameters for ZnO buffer layers was aided by fabrication and characterization of Al/ZnO/CIS test cells. The approach to deposition of Al circular areas to form Al/ZnO/CIS test cells and to characterize the test cells was the same as discussed in Section 4.2 for Al/CIS devices.

6.1.1 CBD ZnO Buffer layers

A low level effort was devoted to growth of ZnO buffer layers by chemical bath deposition as described in Section 3.3. Further work must be done before the optimum procedure can be determined for growth of ZnO buffer layers by CBD. However, preliminary studies determined that test cells with good performance can be fabricated when the first stage of growth occurs over a period greater than 3 minutes. One of the best test cell results is shown in Figure 16. As discussed in Section 4.2, the illuminated I-V characteristics were measured by forcing the $J_{sc} \approx 40$ mA/cm^2, which provides for an estimated active-area efficiency.

Sample: Test Cell 95-15

Area(cm^2): 0.0616

Illuminated Characteristics
Isc = 2.5 mA
Jsc = 40.67 mA/cm^2
Voc = 466.5 mV
FF = 0.6181
Eff. = 11.73 %

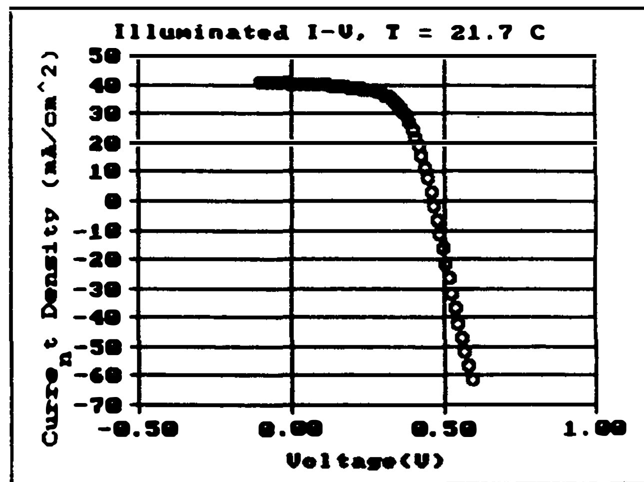


Figure 16. Current voltage characteristics for Al/ZnO(CBD)/CIGSS test cell 95-15.

6.1.2 CVD ZnO Buffer layers

As in the case of ZnSe and ZnO(CBD) buffer layers, test cells were utilized for process development. Some representative results for test cells and completed cells are tabulated in Table 2. Estimates of buffer layer sheet resistance and thickness were determined from measurements on films grown on glass and silicon witnesses, respectively. Illuminated properties of test cells were acquired by forcing Jsc ≈ 40 mA/cm^2. Typical I-V characteristics for a test cell with a ZnO buffer layer are given in Figure 17.

The fill factor for the Al/ZnO/CIGSS test cells is particularly sensitive to the buffer layer resistivity, with low values of fill factor occurring for low resistivities and larger fill factors resulting when the buffer layer resistivity is greater than 1000 ohm-cm. Best test cell and completed cell performances have been achieved when the buffer layer is grown at 225°C without doping, and then heat treated in ethyliodide presumably to introduce iodine from the top surface of the buffer layer. As in the case for CIS cells with buffer layers, there is much to be learned concerning optimum processing procedures and the relationship to the electronic structure of the

TABLE 2-- Effect Of CVD ZnO Buffer Layer Properties On ZnO/CIS(GA) Cell Performance

Device	ZnO Buffer Layer Sheet Rho (ohm/sq.)	Thickness (Å)	Rho (ohm-cm)	Tsub (°C)	Jsc (mA/cm2)	Voc (mV)	FF	Eff (%)
Test Cells								
95-11	6.2E3	987	0.06	250	40	407	0.31	4.5
95-5	6.0E4	548	0.33	225	40	440	0.34	6.0
94-12	3.3E5	380	1.2	260	40	417	0.38	6.8
94-11	1.0E6	757	7.6	270	40	374	0.51	8.1
95-2	4.5E8	408	1840	225	40	420	0.55	9.7
94-83	4.0E8	500	2000	225	40	435	0.58	10.5
After Heat Treatment In Ethyliodide @ 225°C					40	454	0.61	11.3
Completed Solar Cells								
95-100	10	10,000	0.001		33.0	399	0.49	6.45
94-16	4E9	500	2E4	255	34.26	492	0.66	11.1
94-54	2E10	210	4E4	225	35.46	480	0.65	11.0
94-80	1.2E9	810	9700	225	34.66	500	0.65	11.3

(Included Post Heat Treatment Of Buffer Layer In Ethyliodide)

Jsc = 41.1 mA/cm2
FF = 0.61

Voc = 454 mV

Est Active
Area Eff = 11.3 %

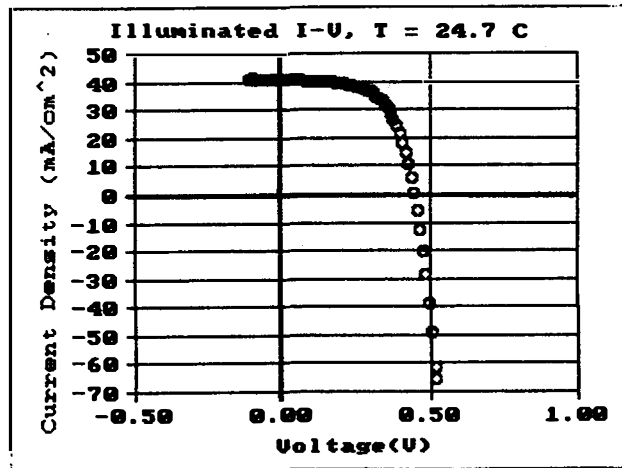


Figure 17. Current voltage characteristics for Al/ZnO(CVD)/CIGSS Test Cell 94-83.

interface. It is clear, however, that the as-deposited buffer layer resistivity plays a key role in determining the cell performance. Due to these experimental results, modeling studies using PC-1D have been conducted to investigate the effect of buffer layer resistivity. These studies are discussed in Section 7.

6.2 ZnO/CIS Solar Cell Performance

6.2.1 Completed Cells With CBD ZnO Buffer layers

Completed solar cells based on CBD ZnO layers have not produced results as good as cells based on CVD ZnO buffer layers. The best efficiencies for completed cells with CBD ZnO buffer layers are in the range of 6 to 7 %. Several substrates were sent to Siemens for deposition of a top contact layer. In many cases, the substrates had Al dots deposited onto them to form test cells. After measuring the I-V characteristics for test cells, the Al dots were

scraped off and the substrates sent to Siemens. Figure 18 gives I-V results for a completed cell formed on the same substrate as the test cell described in Figure 16. The fill factor was reduced due the I-V curve being inflected.

Explanation of these results is not obvious. One possibility is that the exposure to air prior to deposition of conductive ZnO caused problems. It should be noted, however, that test cells formed by depositing Al dots on ZnO(CBD)/CIS structures typically take several days to degrade significantly. Another possible explanation is that the interaction of the conductive ZnO

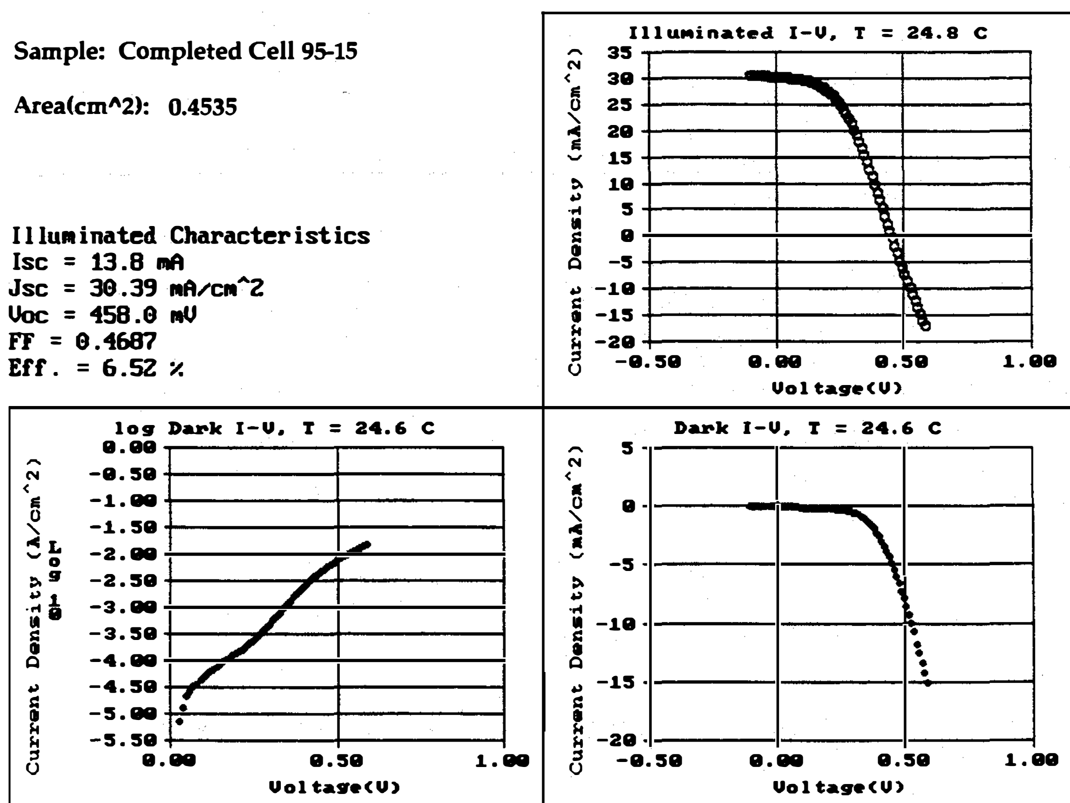


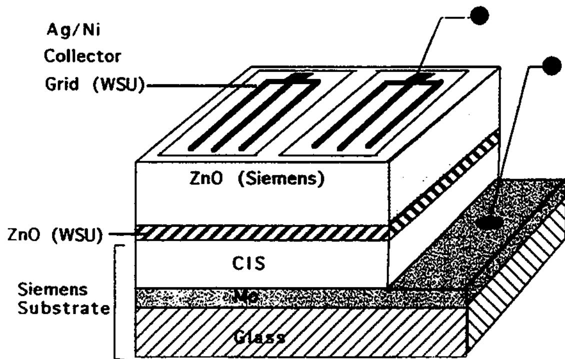
Figure 18. Current voltage characteristics for Al/ZnO(CBD)/CIGSS Test Cell 95-15. Current voltage characteristics for a completed cell based on the ZnO(CBD)/CIS Substrate 95-15 — same substrate for which the test cell properties are given in Figure 16.

(deposited by the Siemens process) with the CBD ZnO buffer layer may have resulted in degraded device properties. Finally, these completed cell properties may result because the CBD ZnO layer is too resistive. It may be that in the case of Al/ZnO(CBD)/CIS test cells a reaction occurs with the thin Al layer which effectively dopes the ZnO layer, whereas in the case of a completed cell no Al layer is ever deposited.

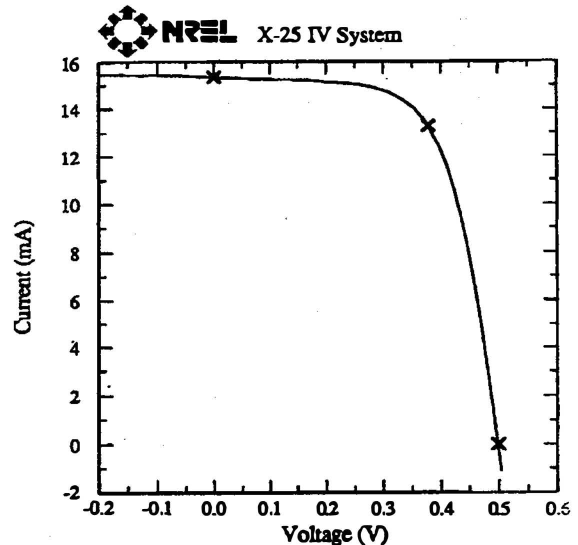
6.2.2 Completed Cells With CVD ZnO Buffer layers

The best results for CIS solar cell performance have been achieved with ZnO buffer layers grown by chemical vapor deposition. Properties of three completed cells as measured by NREL are given in Table 2. Figure 19 gives illuminated I-V characteristics as measured by NREL for Solar Cell 94-80. Details concerning fabrication are given in Table 2. The total area efficiency is 11.3 % and the active area efficiency is approximately 12 %. As far as we

SAMPLE 94XC080
AREA = 0.4427 cm2
NREL MEASUREMENT:
ASTM E 892-87 Global
Irradiance = 1000 W/m2



Solar Cell Configuration



I_{SC} = 15.34 mA
J_{SC} = 34.66 mA/cm2
Fill Factor = 65.5 %
V_{OC} = 500 mV
Total Area Efficiency = 11.3 %
Active Area Efficiency ≈ 12 %

Figure 19. Illuminated characteristics as measured by NREL for a completed ZnO/CIGSS solar cell with a high resistivity CVD ZnO buffer layer.

know this result represents the best performance reported to date for a ZnO/CIS solar cell.. Further optimization of ZnO buffer layers should lead to larger values of fill factor and thus higher efficiencies. Finally, improved efficiencies are also expected when this approach is applied to CIGS material. Results are also given in Table 2 for a completed cell that has the low resistivity ZnO top contact deposited by Siemens Solar directly in contact with the CIS substrate.

6.3 Current-Voltage Analyses

From the results reported for CIS cells with CVD ZnO buffer layers, it is clear that the resistivity of the ZnO buffer layer is an important parameter. Consider the test cell properties tabulated in Table 2. The buffer layer resistivity is the value determined for a film grown on a glass witness immediately after deposition. Devices exhibited low fill factors when the as-deposited buffer layer resistivity was low. Test Cell 94-12 has a low resistivity buffer layer and forward I-V characteristics which are characterized by a single mechanism due apparently to tunneling/recombination. Most importantly, the magnitude of the forward current under illuminated conditions is one to two orders of magnitude larger. Solar Cell 94-80 which was fabricated with a relatively high resistivity ZnO buffer layer is characterized by a forward current that is composed of two mechanisms. The dominant mechanism in the 0.3 to 0.5 volt range can be interpreted as being due to space charge recombination, and the change in characteristics between dark and illuminated conditions is much less than in the case of cells with low resistivity buffer layers. It should be noted that our CVD ZnO films typically oxidize and gradually exhibit a high resistivity. Test cell performance correlates with the as-deposited buffer layer resistivity, however. Thus, since low values of resistivity are achieved for the CVD ZnO films by using a high molar flow of zinc, it appears that excess zinc (during the deposition process) may cause the low fill factors.

7. MODELING CALCULATIONS FOR CIS CELLS WITH RESISTIVE BUFFER LAYERS

It is generally found that there is an optimum range of values for the buffer layer thickness and resistivity in order to obtain a high efficiency CIS cell. If the layer resistivity is low, the resulting devices typically exhibit low values of V_{OC}. On the other hand, inflected I-V curves are often observed for cell structures in which the buffer layer is apparently too thick or too resistive. In an effort to acquire guidance concerning the variation of these parameters, modeling calculations of cell performance for a range of buffer layer properties were conducted.

7.1 Computational Approach

Modeling calculations have been carried out using PC-1D, a one dimensional computer code based on a finite element numerical approach to solve the semiconductor equations. Up to three regions with different material parameters can be used to define a cell structure, each with its own doping profiles and electronic and optical properties. Recombination of the electron hole pairs can be defined in each region by SRH band to band transitions or through user-defined deep level transitions. Surface recombination at interfaces is also taken into account.

Modeling calculations have been carried out for CIS cells with ZnO buffer layers, and with a low resistivity ZnO top contact layer. These studies have concentrated on the effect of buffer layer resistivity and thickness on cell performance. A limited effort has also been devoted to studying the effects of changes in electron affinity for the buffer layer and charged traps in the buffer layer. Although ZnO has been chosen for the buffer layer, the key results are valid for CdS or any other highly resistive buffer layer.

7.2 Results Of Modeling Studies

7.2.1 Efficiency vs Buffer Layer Resistivity And Thickness

Some representative modeling results are tabulated in Table 3. With

the buffer layer resistivity set equal to $1x10^5$ ohm-cm, the surface recombination velocity (SRV) at the ZnO/CIS interface set equal to $1x10^4$ cm/s, current voltage characteristics were calculated as a function of buffer layer thickness. Note that the open-circuit voltage increases from 425 mV to 514 mV as the layer thickness increases. Figure 20 shows the effect of buffer layer resistivity on cell performance. These studies indicate that a buffer region with a resistivity larger than 1.0 ohm-cm leads to increased voltages and efficiencies. The effect of interface recombination is described by Figure 21. In this case, the buffer layer resistivity is set equal to $1x10^5$ ohm-cm, and the buffer layer thickness and SRV are varied. Cell efficiencies are affected significantly once the SRV equals or exceeds $1x10^7$ cm/s. Calculated I-V characteristics for the maximum efficiency case are given in Figure 22.

7.2.2 The Role Of Resistive Buffer Layers

These studies clearly indicate that a buffer layer that is significantly more resistive than the highly conducting top contact layer can improve the

TABLE 3 -- Modeling Parameters For Representative Calculations

ZnO Buffer Layer Thickness (Å)	Rho (ohm-cm)	**ZnO/CIS SRV** (cm/s)	**J_{sc}** (mA/cm^2)	**V_{oc}** (mV)	**P_{max}** (mW/cm^2)
0	--	1E4	38.2	425	10.0
100	1E5	1E4	37.5	501	12.4
200	1E5	1E4	36.7	510	13.3
300	1E5	1E4	36.7	510	13.3
400	1E5	1E4	36.1	513	13.3
500	1E5	1E4	35.5	514	13.2

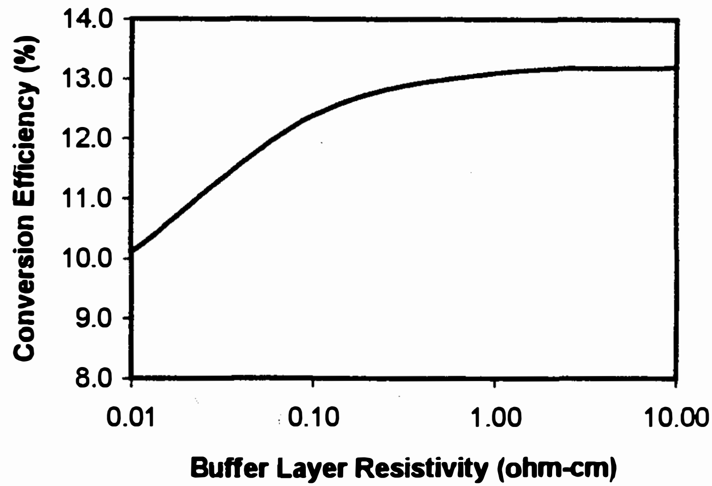


Figure 20 Efficiency vs ZnO buffer layer resistivity for a layer thickness of 300Å and S = 1E4.

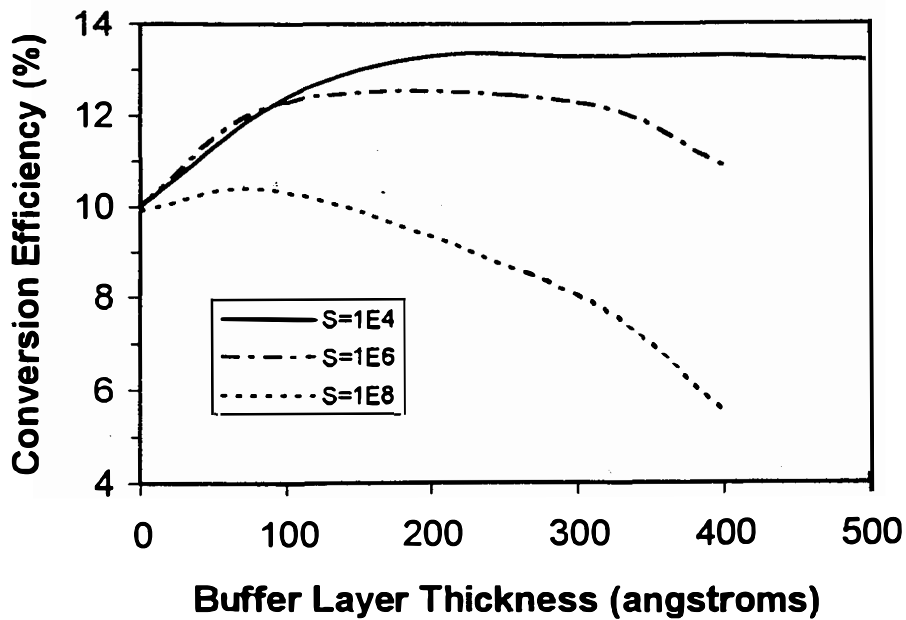


Figure 21. Active area efficiency vs buffer layer thickness for different values of SRV at the CIS-ZnO(Buffer) interface.

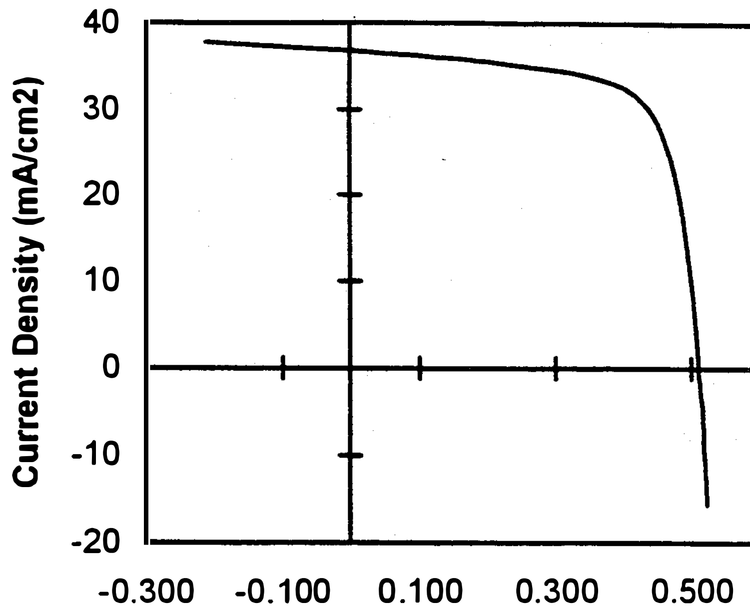


Figure 22. I-V characteristics for a CIS cell with a 300Å buffer layer.

performance of CIS cells. The basic reasons for the beneficial effect of such layers are illustrated in Figures 23. Figure 23A depicts the electron band diagram of a ZnO/CIS structure with a 300 Å ZnO buffer layer that has a resistivity of $1x10^5$ ohm-cm. A plot of recombination rate per unit volume is plotted versus depth in Figure 23B for the condition of maximum power. Two cases are considered, namely, a cell without a buffer layer and a cell structure identical to that for which the band diagram is described in Figure 23A. The effect of the buffer region is to greatly reduce the recombination rate at and near the ZnO/CIS interface. The relatively high resistance of the buffer film prevents the CIS from being strongly inverted at the ZnO/CIS interface, which results in a low electron concentration (n_S) at the interface. The low value of n_S in turn leads to reduced recombination as shown. An equivalent point of view is that the buffer layer provides a field which reflects electrons that approach the space charge region of CIS from the left, which reduces the recombination in the space charge region. As a final point, preliminary studies have been conducted concerning the effect of charged traps in the buffer layer. At this point, it appears that the reflecting electric field constitutes the main effect of a buffer layer.

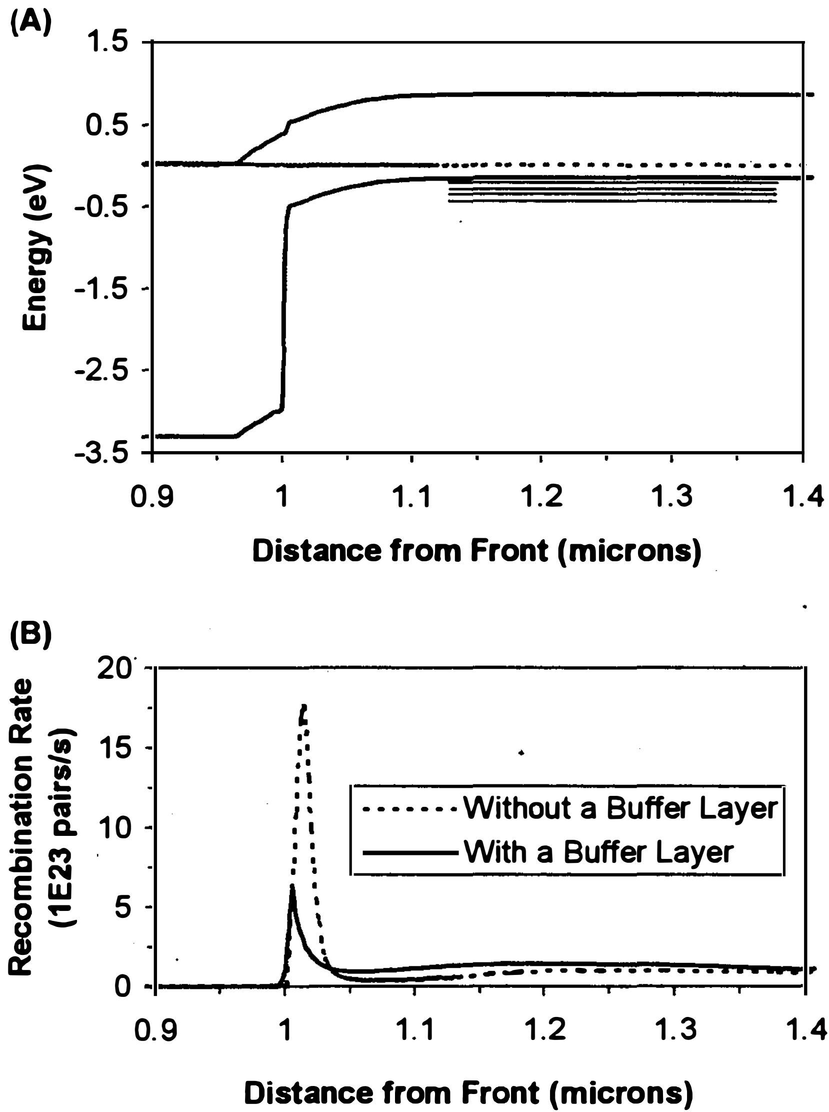


Figure 23. (A) Electron band diagram for a CIS cell with a ZnO buffer layer and a highly conductive ZnO top contact layer;
(B) Recombination rate vs depth.

Additional studies of the impact of buffer layer properties on solar cell performance are clearly needed. Although these studies demonstrate that it is beneficial for the buffer layer to be resistive, predicted efficiencies for buffer resistivities on the order of 0.01 to 1.0 ohm-cm are too high.

7.2.3 A Model For Inflected I-V Curves

CIS cells with buffer layers will occasionally exhibit I-V characteristics that are inflected. We have carried out modeling studies using PC-1D to explore possible causes of inflected I-V curves. One model that leads to such I-V characteristics is based on assuming that the resistive buffer layer is characterized by a smaller electron affinity than either CIS or the conducting top contact layer. The calculated I-V curve in Figure 24 is for the case of the electron affinities being 4.1 eV, 3.8 eV and 4.1 eV for ZnO(top contact), ZnO(buffer) and CIS, respectively. Clearly , it would be unreasonable to assume different electron affinities for the two ZnO layers if they were the same basic material, but with different dopant densities. This may not be the case, however. The two layers are usually grown by different techniques, and, as a result, may have slightly different physical properties. A similar effect has been reported by Kronik, et al. [14]. In particular, those authors refer to seven articles in which the conduction band offset varies over 1.4 eV for the CdS/CIS interface. The spread of values may be due to measurement and/or CdS growth techniques.

The results of these modeling studies are generally in agreement with experimental results. These modeling studies provide insight concerning the effect of the reflecting field provided by a resistive buffer region. Furthermore, a model has been identified that predicts inflected I-V curves. These studies are being extended to cells based on CIGS and Siemens 'graded absorber' material. The effects of a wide bandgap surface layer on the CIS substrate and/or the presence of a high density of deep traps near the CIS surface will also be examined.

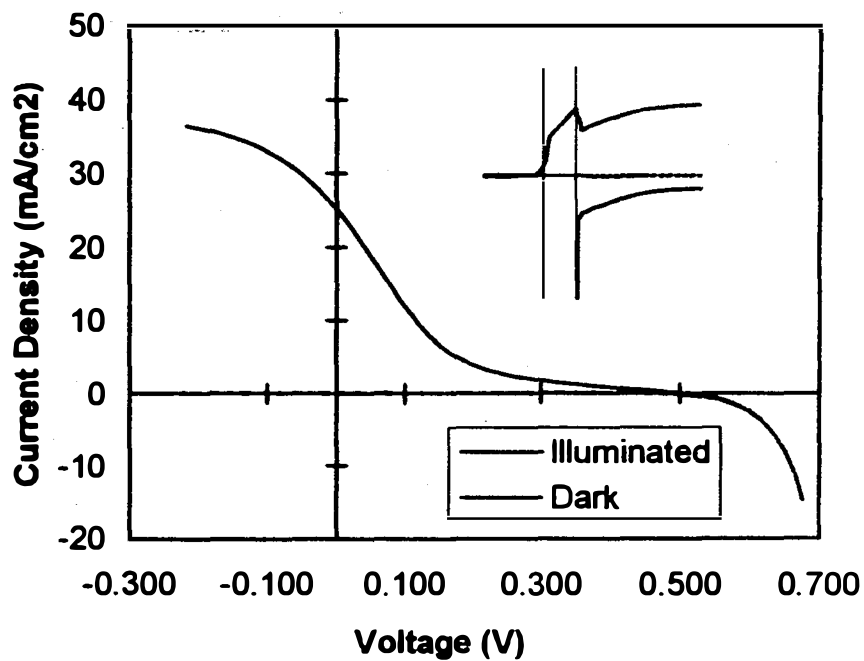


Figure 24 Illuminated and dark characteristics for a cell with a resistive buffer layer and with a band offset as indicated by the insert.

8. CONCLUSIONS

This program focused on investigating the feasibility of using ZnSe and ZnO as buffer layers in CIS solar cells. Experimental studies were carried out with CIS and CIGSS substrates provided by Siemens Solar. ZnSe films were deposited by a CVD process which involved the reaction of a zinc adduct and H_2Se. Al/ZnSe/CIS test cells were used for process development. It was determined from test cell performance that the optimum thickness for ZnSe buffer layers is in the range of 150Å to 200Å for Siemens CIS material, and between 80Å and 120Å for the graded absorber material. It was determined that if the buffer layers exceeded these values significantly, the short-circuit current would be reduced to zero. This effect is consistent with results reported in the literature indicating that there is a 0.9 eV band offset at the ZnSe-CIS interface.

Completed cells were fabricated by sending ZnSe/CIS structures to Siemens Solar for deposition of a low resistance ZnO top contact layer, and then depositing an Al/Ag collector grid after the ZnO coated substrates were returned to WSU. The best efficiency achieved for a ZnSe/CIS cell was an active area value of 9.2 %. In general, deposition of a conductive ZnO film on top of a ZnSe/CIS structure resulted in either shunted or inflected I-V characteristics. The best cell had a thin film of CVD ZnO to protect the ZnSe buffer from the Siemens process. Thus, although Al/ZnSe/CIS test cells exhibited active area efficiencies greater than 14 %, completed cells were significantly lower in efficiency. In order for CIS cells with ZnSe buffer layers to realize their potential, it will be necessary to utilize a protective layer to minimize the reaction between the Siemens ZnO process and the ZnSe buffer layer.

Two approaches were investigated for depositing ZnO buffer layers, namely, solution growth and chemical vapor deposition . CVD ZnO buffer layers are grown by reacting a zinc adduct with tetrahydrofuran. The approach to CVD growth of ZnO is distinguished from other approaches to growth of ZnO buffer layers such as sputtering in two important ways, namely: (1) The zinc and oxygen precursors are both relatively large molecules; and (2) no extra oxygen or ions are involved in the deposition

process. Substrate temperatures (T_{sub}) have been varied from 150°C to 350°C, with the best device performance obtained for $T_{sub} \approx$ 225°C to 250°C. These studies concentrated on Siemens graded absorber material. ZnO/CIS solar cells have been fabricated by first depositing a ZnO buffer layer, followed by deposition of a low resistivity ZnO top contact layer and an Al/Ag collector grid. Several cells were fabricated with an area of 0.44 cm^2 that have total area efficiencies greater than 11 %. To date, the best performing ZnO/CIS cell was measured by NREL to have a total area, AM1.5G efficiency of 11.3 %. The active area efficiency of the device was approximately 12 %. In general, we find that ZnO buffer layers should have a resistivity larger than 1000 ohm-cm and have a thickness from 200 Å to 600 Å. Low resistivity ZnO buffer layers tend to result in cells which exhibit efficiencies less than 10 % and low values of V_{oc}.

CIS cells studies with ZnO buffer layers grown by CBD have also shown promise. Test cells indicate that efficiencies greater than 11 % should also be possible with this approach. The CBD ZnO films tend to be unstable resulting from the adsorption of water. Attempts to fabricate completed solar cells have not yielded reasonable efficiencies.

Modeling calculations of cell performance were carried out for a range of buffer layer properties with the objective of understanding the role played by buffer layers in solar cells based on CIS and related alloys. PC-1D has been used to carry out modeling calculations for CIS cells with ZnO buffer layers, and with a low resistivity ZnO top contact layer. These studies have concentrated on the effect of buffer layer resistivity and thickness on cell performance. A limited effort was also devoted to studying the effects of band offsets between the buffer layer and CIS, and for charged traps in the buffer layer. Results of the modeling studies are in general agreement with experimental studies. They show that it is important for the buffer layer to be very resistive. Plots of recombination rate versus depth clearly indicate how a resistive buffer layer improves the performance of a CIS solar cell. Inclusion of a resistive wide band gap layer between a highly conducting ZnO top contact layer and CIS results in the existence of a field in the buffer region that retards electrons approaching the space charge region of CIS (from the top contact layer), which in turn decreases the magnitude of recombination

taking place in the depletion region. Two interesting features often observed for CIS solar cells were also predicted by the modeling calculations, namely, inflected I-V curves and the 'double mechanism' I-V curve when plotted as log I vs V.

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6. AUTHOR(S)
Larry C. Olsen

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Electronic Materials Laboratory
Washington State University at Tri-Cities
100 Sprout Road
Richland, WA 99352

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13. ABSTRACT *(Maximum 200 words)*
The major objective was to determine the potential of ZnSe and ZnO buffer layers in solar cells based on $CuInSe_2$ (CIS) and related alloys. Experimental studies were carried out with CIS and $CuInGaSSe_2$ (CIGSS) substrates provided by Siemens Solar. ZnSe films were deposited by a chemical-vapor deposition (CVD) process that involved the reaction of a zinc adduct and H_2SE. Al/ZnSe/CIS test cells were used for process development. The optimum thickness for ZnSe buffer layers was found to be in the range of 150Å to 200Å for Siemens CIS material, and between 80Å and 120Å for the graded absorber material. If the buffer layers exceeded these values significantly, the short-circuit current would be reduced to zero. This effect is consistent with results reported in the literature indicating a 0.9-eV band offset at the ZnSe-CIS interface. Completed cells were fabricated by using a low-resistance ZnO top-contact layer deposited by Siemens, and then depositing an Al/Ag collector grid at Washington State University. The best efficiency achieved for a ZnSe/CIS cell was an active-area value of 9.2%. In general, deposition of a conductive ZnO film on top of a ZnSe/CIS structure resulted in either shunted or inflected I-V characteristics. Two approaches were investigated for depositing ZnO buffer layers: chemical-bath deposition and CVD. CVD ZnO buffer layers are grown by reacting a zinc adduct with tetrahydrofuran. Best results were obtained for ZnO buffer layers grown with a substrate temperature $\approx$ 225°-250°C. These studies concentrated on Siemens graded absorber material (CIGSS). ZnO/CIS solar cells have been fabricated by first depositing a ZnO buffer layer, followed by deposition of a low resistivity ZnO top contact layer and an Al/Ag collector grid. Several cells were fabricated with an area of 0.44 cm^2 that have total-area efficiencies > 11%. To date, the best performing ZnO/CiS cell was measured by NREL to have a total-area, AM1.5G efficiency of 11.3%. The active-area efficiency of the device was about 12%. In general, we find that ZnO buffer layers should have a resistivity > 1000 ohm-cm and have a thickness from 200Å to 600Å. CIS cells studies with ZnO buffer layers grown by CBD also show promise. Finally, simulation studies were carried out using the one-dimensional code, PC-1D.

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