Processing and Modeling Issues for Thin-Film Solar Cell Devices

Annual Subcontract Report 16 January 1995 - 15 January 1996

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Summary

During the third phase of the subcontract, IEC researchers have continued to provide the thin film PV community with greater depth of understanding and insight into a wide variety of issues including: the deposition and characterization of $CuIn_{1-x}Ga_xSe_2$, a-Si, CdTe, CdS, and TCO thin films; the relationships between film and device properties; and the processing and analysis of thin film PV devices. This has been achieved through the systematic investigation of all aspects of film and device production and through the analysis and quantification of the reaction chemistries involved in thin film deposition. This methodology has led to controlled fabrications of 15% efficient $CuIn_{1-x}Ga_xSe_2$ solar cells over a wide range of Ga compositions, improved process control of the fabrication of a-Si solar cells, and reliable and generally applicable procedures for both contacting and doping CdTe films. Additional accomplishments are listed below.

<u>CuIn_{1-x}Ga_xSe₂ Solar Cells</u>

Solar cells fabricated from uniform $Cu(InGa)Se_2$ absorber layers deposited by four source elemental evaporation, with bandgap from 1.16 to 1.45 eV, are characterized to determine the effect of increased Ga content on material properties and device performance. The completed devices have ~15% efficiency for x < 0.5 (E_g < 1.3 eV) and high V_{oc} which increases over the entire range of composition to a maximum of 788 mV. At higher Ga contents, the device performance is limited by poor fill factor. The devices are characterized by current-voltage and quantum efficiency measurements.

Cu-Ga-In precursors reacted in a selenium containing atmosphere in the temperature range 400–500°C contain a mixture of CuInSe₂ and CuGaSe₂ phases instead of the desired single phase Cu(Ga_xIn_{1-x})Se₂. From X-ray diffraction and Auger analysis, the mixed phase films form a layered structure with the CuInSe₂ phase near the surface and the CuGaSe₂ phase near the Mo/film interface. Annealing of these films in the temperature range 500–600°C in an inert atmosphere for a duration of 60 to 90 minutes converts the multiphase structure in the film to a single phase Cu(Ga_xIn_{1-x})Se₂. Solar cells made with the multi-phase films are shown to have properties similar to CuInSe₂ devices while cells made with the annealed single phase films behave like Cu(Ga_xIn_{1-x})Se₂ devices with the bandgap expected for the precursor composition.

a-Si Solar Cells

It was found through QE measurements and SMS analysis that there was significant dopant carry over from one run to the next from the film deposited on the "hot" electrode. Deposition of a burying layer of a-SiC:H between device runs was found to be necessary to remedy the dopant carryover. As a result, FFs in excess of 71% were obtained reproducibly. In a second step, H₂ diluted μc n-layers, compatible with ZnO/Ag back contact as well as with tunnel junction in tandem devices, were developed. These μc n-layers with conductivities and activation energies of 1 S/cm and 0.05 eV, respectively, allowed fabrication of devices with p-i-n ZnO/Ag contacts with FFs as high as 72%. In the case of p-i-n Ti/Ag contacts, the deposition rate of Ag was found to be an important parameter in that rates below 100 Å/min resulted in lower FFs.

Analysis of back reflector optical enhancements in a-Si solar cells using substrates with a range of TCO textures concluded that a textured substrate is much more effective at increasing red response than a smooth substrate with external textured Ag back reflector. This suggests that the replication of the substrate texture on the top a-Si surface is crucial to enhance multiple scattering from the underlying substrate.

Within the context of optical enhancement schemes in a-Si devices, the effect of textured tin oxide and zinc oxide substrates on the current generation in amorphous silicon solar cells were also analyzed. The results show that increasing substrate haze above $\approx 7\%$ for SnO₂ and above $\approx 5\%$ for ZnO has negligible impact on the current generation at long wavelengths.

CdTe solar cells

Vapor phase CdCl₂ treatments were developed, permitting the effects of reaction temperature and chloride concentration on materials and devices to be investigated. Vapor CdCl₂ treatment at 420°C was found to result in uniform modification of the film properties. Combined with the contacting process developed in the previous reporting period, the uniform and reproducible treatments have translated into greater consistency in device performance at a baseline efficiency level of 10.5–12%.

Treatment of CdTe/CdS thin film structures in dilute mixtures of HCl vapor at 380–440°C have been shown to promote microstructural changes in the structure of CdTe/CdS films similar to those treated with CdCl₂. While not yet optimized for high conversion efficiency, this shows promise as an alternative to treatments with CdCl₂.

In specially prepared CdTe devices which have been subjected to stresses beyond normal operating conditions, there appears to be changes that are associated with stress temperature and electrical bias. It is not clear whether there is a dependence on the illumination level. One effect is promoted by reverse bias and affects primarily the bulk CdTe properties, as indicated by the severity of the light-dark crossover of the J-V curves. Another effect is promoted by forward bias and results in the strengthening of a reverse diode. Finally, there are changes in both the light-generated current and J_0 whose magnitudes are also bias- and light-dependent. The results reported herein are from work-in-progress. The data were recorded on a limited data set (16 samples), using a single method of device preparation.

In addition to these in-house activities, IEC has maintained an active role in the collaboration with over ten different PV and thin film research and development organizations. More specifically, IEC personnel have major roles in the CuInSe₂, a-Si, and CdTe teamed research activities. It is through these activities that IEC personnel assure that the results of their scientific accomplishments are disseminated throughout the PV community.

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1.0 INTRODUCTION

The overall mission of the Institute of Energy Conversion is the development of thin film photovoltaic cells, modules, and related manufacturing technology and the education of students and professionals in photovoltaic technology. The objectives of this four-year NREL subcontract are to advance the state of the art and the acceptance of thin film PV modules in the areas of improved technology for thin film deposition, device fabrication, and material and device characterization and modeling, relating to solar cells based on CuInSe₂ and its alloys, on a-Si and its alloys, and on CdTe.

In the area of $CuInSe_2$ and its alloys, IEC researchers have produced $CuIn_{1-x}Ga_xSe_2$ films by selenization of elemental and alloyed films with H_2Se and Se vapor and by a wide variety of process variations employing co-evaporation of the elements. Careful design, execution and analysis of these experiments has led to an improved understanding of the reaction chemistry involved, including estimations of the reaction rate constants. Investigation of device fabrication has also included studies of the processing of the Mo, CdS and ZnO deposition parameters and their influence on device properties. An indication of the success of these procedures was the fabrication of a 15% efficiency $CuIn_{1-x}Ga_xSe_2$ solar cell.

In the a-Si area, reproducibility and process control have been achieved through the optimization of processing parameters related to each of the a-Si layers: p, buffer, i, and n, as well as the TCO window and back contact. In addition, analysis and measurements of the improvement in performance of a-Si solar cells due to optical enhancements from a wide range of TCO texture substrates and back reflectors have been completed.

Activities related to CdTe-based solar cells include the development of uniform and reproducible vapor phase CdCl₂ treatments for CdTe/CdS films which have translated into greater consistency in device performance, as well as a HCl vapor treatment that promotes changes in the structure of the films similar to those treated with CdCl₂. In order to determine the long term stability of contacts made to CdTe, stress testing of specially prepared CdTe devices has begun.

The measurement, characterization, and modeling of thin film device operation has been specialized independently for devices produced with each class of materials. Also, data has been accumulated and analyzed to develop baseline device parameters for each type of cell.

IEC personnel are active in teamed research in all three thin film material areas, both through NREL's Thin Film PV Partnership program and on a less formal, one-on-one basis. It is partly through these interactions that IEC serves to disseminate PV expertise throughout the PV community and, thereby, achieve its larger goals.

2.0 CuInSe₂ RESEARCH

2.1 Cu(InGa)Se₂ by Multisource Evaporation

2.1.1 Introduction

The highest efficiency with $Cu(InGa)Se_2$ thin films deposited by multisource elemental evaporation cells have had $x \equiv [Ga]/([In]+[Ga]) \approx 0.25$ corresponding to a bandgap (E_g) of ~ 1.15 eV with $V_{oc} \approx 600$ –650mV [2.1, 2.2]. At greater Ga content, it has been reported that the open circuit voltage did not increase proportionally to the bandgap and the efficiency decreased [2.3, 2.4]. In addition, compositional gradients of the Ga and In in $Cu(InGa)Se_2$ have been reported to improve the device performance [2.5].

In this report, solar cells fabricated from Cu(InGa)Se₂ absorber layers deposited by four source elemental evaporation with bandgap from 1.16 to 1.45 eV are characterized to determine the effect of increased Ga content on material properties and device performance. The Cu(InGa)Se₂ films were deposited with no grading of the Ga and In to avoid gradients in the electrical and optical properties which might effect the device performance differently as the total Ga content changes. The completed devices have ~15% efficiency for x < 0.5 (E_g < 1.3 eV) and high V_{oc} which increases over the entire range of composition to a maximum of 788 mV. At the highest Ga contents, the device performance is limited by poor fill factor. The devices are characterized by current-voltage and quantum efficiency measurements.

The standard substrate for most CIGS cells is Mo-coated soda lime glass. Characterization of the substrate and its effect on the CIGS deposited on it is presented to provide a list of criteria to determine whether a given substrate is suitable for a baseline cell process. One of the concerns regarding the Mo/CIGS contact is that it may be the source of a parasitic second diode sometime seen in cell current-voltage characteristics. A novel device configuration was developed which allows direct measurements of this contact to show that the second diode is not at the back of the cell.

2.1.2 CIGS Deposition

For characterization of Cu(InGa)Se₂ films and devices as a function of Ga content, the films were deposited by elemental evaporation from four Knudsen type sources to independently control the fluxes of Cu, In, Ga, and Se. The substrates were soda lime glass coated by dc sputtering with a 1 µm thick Mo layer. One bare glass substrate was included in each run to allow measurements of the sheet resistance and optical transmission. The Cu(InGa)Se₂ films were deposited using a simplified version of the bilayer process developed for CuInSe₂ [2.4]. This began with a Cu-rich Cu(InGa)Se₂ layer, with [Cu] > [In] + [Ga], deposited at substrate temperature $T_{ss} = 450$ °C, followed continuously by a layer containing only In, Ga, and Se deposited at Tss = 600°C. In this process, the In, Ga, and Se source temperatures and fluxes were kept constant through both layers and the Cu source was simply turned off. A profile of the source and substrate temperatures versus time for a deposition which gave x = 0.38 is shown in Figure 2.1. The first layer had [Cu]/([In]+[Ga]) = 1.3-1.5. The final Cu content could be varied by simply changing the relative times of the two layers and the completed films in this work had $[Cu]/([In]+[Ga]) \approx 0.90 \pm 0.03$. The Cu(InGa)Se₂ films had thicknesses from 2.5– 2.9 µm as determined by the mass gain.

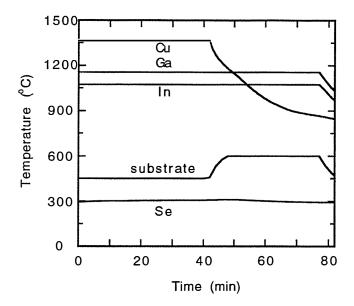


Figure 2.1. Source and substrate temperature versus time profile of a deposition to produce a $Cu(InGa)Se_2$ film with x = 0.38.

With this process, $Cu(InGa)Se_2$ films were deposited with $0.25 \le x \le 0.7$, which corresponds to $1.16 \text{ eV} \le E_g \le 1.45 \text{ eV}$, for characterization and device fabrication. Also, $CuInSe_2$ films were deposited for comparison.

2.1.3 Cu(InGa)Se₂ Characterization

The elemental composition of the Cu(InGa)Se2 films was determined by energy dispersive X-ray spectroscopy (EDS) measurements with a 20 kV acceleration voltage and the composition was used to determine E_g according to published values [2.6]. The grain size and surface morphology were evaluated with a scanning electron microscope (SEM). The compositional uniformity was characterized by X-ray diffraction (XRD) and Auger electron spectroscopy (AES) depth profiles. The XRD scans were performed using Cu K α radiation in a scanning 20 mode with 0.01° step size. Since the Cu(InGa)Se2 films are much thinner than the absorption depth of CuInSe2 (13 μm) and CuGaSe2 (25 μm), the entire thickness of the films was sampled. The AES measurements were done at the National Renewable Energy Laboratory (NREL). Sheet resistance was measured on the sample deposited on bare glass substrate with a four point probe.

SEM characterization of the surface and cross-section of the films showed similar surface morphology and well-defined columnar grains with 1–2 μ m average grain size regardless of the Ga content. An SEM micrograph of a film with x = 0.38 shows this in Figure 2.2.

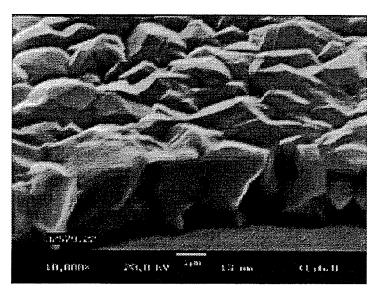


Figure 2.2 SEM micrograph of a typical film with x = 0.38.

XRD measurements were used to determine the Ga content of the films from the lattice parameter and gave good agreement with the EDS. Detailed XRD scans were made of the strongest reflections and the compositional distribution was inferred from the full width at half maximum (FWHM) and peak symmetry. This is shown by the (112) peak and the (220)/(204) peak doublet in Figures 2.3 and 2.4 for four of the films spanning the compositional range. The crystal axis ratio c/a is 2.00 for $x \approx 0.25$ so there is no splitting of the (220) and (224) peaks for the film with x = 0.27. As x increases or decreases, c/a decreases or increases, respectively, and the doublet shows increased splitting. The peaks also show a shift in 2θ consistent with the increase in x. The (112) peaks show an instrumental asymmetry inherent to the apparatus at low 20. The CIGS films have FWHM = 0.15-0.19° compared to the CIS films with FWHM and the instrumental broadening of 0.11°. Other peaks on the CIGS films which could be separated at low and high Ga concentration also had FWHM < 0.2 with no asymmetric broadening. The broadening of the CIS film peaks is likely due to stress in the films because the grain size is sufficiently large to have effect on the peak shape. If the additional broadening of the CIGS peaks is entirely due to compositional non-uniformity, the total variation in x would still be less than $\pm 5\%$ for each film corresponding to a maximum bandgap variation of ± 0.03 eV. Thus the XRD spectra indicate that the films are compositionally uniform.

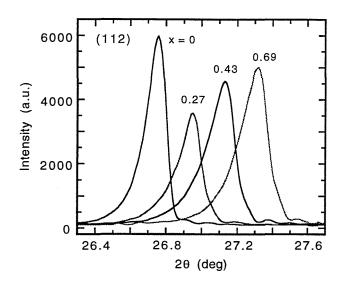


Figure 2.3 XRD scans of the (112) peak for samples with x = 0, 0.27, 0.43, and 0.69.

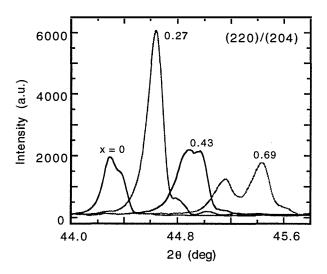


Figure 2.4 XRD scans of the (220)/(224) doublet for samples with x = 0, 0.27, 0.43, and 0.69.

To characterize the relative orientation of the grains within the films the relative orientations of the (112) peak and the (220)/(204) doublet were determined by measuring the areas under the diffraction peaks. The ratios of the integrated intensity I(112) to I(220)+I(204) are compared in Table 2.1 to those of powder diffraction standards for x=0.3 and 0.6 [2.7]. These relative orientations suggest that the $Cu(InGa)Se_2$ films have a nearly random crystal orientation. The $Cu(InGa)Se_2$ orientation may be related to the orientation of the substrate it is deposited on. The random orientation was obtained when the films were deposited onto (110) oriented Mo layers, but $Cu(InGa)Se_2$ deposited directly on glass had a strong (112) orientation with I(112)/[I(220)+I(204)]=420 for the run which gave x=0.38. We have previously shown that there is an inverse correlation between the CIGS orientation and that of the Mo [2.8].

Table 2.1. Relative crystallite orientation of the Cu(InGa)Se₂ measured by the ratio of the areas under the (112) and (220)/(204) peaks and intensities from powder diffraction patterns.

	Eσ	FWHM	(112)
X	$(e\vec{\nabla})$	(deg)	(220)+(204)
	fil	lms	
0	1.0	0.13	2.7
0.27	1.16	0.16	0.7
0.30	1.18	0.21	1.2
0.38	1.23	0.17	0.9
0.43 1.27		0.19	1.6
0.58	1.37	0.17	1.2
0.69 1.45		0.18	1.9
	powder	standards	
0	-	-	0.7
0.3	-	-	2.5
0.6 -		-	1.7

The compositional uniformity was confirmed by AES depth profiles measured on the films with x = 0.38 and 0.58. The atomic concentrations of Mo, Cu, In, Ga, and Se are shown in Figure 2.5 for the first film plotted versus sputter time. The Mo signal rises rapidly after ~130 min sputtering time indicating that the entire film was sampled in this time. The profiles show no gradient in x through the bulk of the film thickness, consistent with the XRD results, and the value of x agrees well with that determined by EDS. Thus, as the total Ga content increases there is no separation or diffusion of the In and Ga as was observed with selenized Cu(InGa)Se₂ films (see section 2.2).

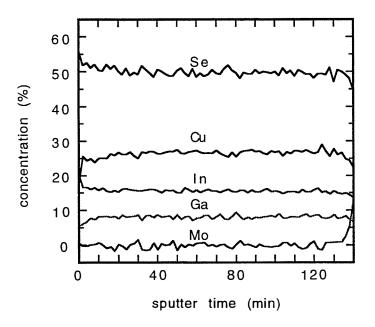


Figure 2.5. Atomic concentrations determined by AES depth profile of Mo, Cu, In, Ga, and Se for the film with x = 0.38.

The AES profiles show that the In concentration at the front surface is greater than in the bulk film while the Cu and Ga concentrations are lower near the front of the film. This is consistent with the presence of a Cu-deficient layer at the front surface of the Cu(InGa)Se₂ film [2.9]. In this case, the AES data suggests that the surface layer also has lower Ga than the bulk so the surface may prefer a Cu-In-Se phase such as CuIn₃Se₅ over an analogous Cu-Ga-Se₂ phase. The effect of such a layer on the device performance is unknown and no attempt is made to account for it in the device analysis below.

Finally, resistivity measurements of the films deposited simultaneously on bare glass also do not indicate any difference in the films as x increases. All films had $\rho = 25\pm15~\Omega$ -cm with no correlation to composition.

2.1.4. Cell Fabrication and Results

Solar cells were fabricated by the sequential deposition of CdS, ZnO:Al, Ni/Al grids, and MgF2 anti-reflection layers on the glass/Mo/Cu(InGa)Se2. The CdS was deposited with a thickness of ~30 nm by chemical bath deposition using a method similar to that described by Kessler et al. [2.10]. The ZnO:Al was deposited in two layers [2.11] by rf sputtering from a compound ZnO:Al2O3 target with 2% Al2O3 by weight. The first layer was deposited with a sputter gas composition of Ar/O2 (2%) to give a 50 nm thick layer with resistivity $\rho \approx 50~\Omega$ -cm. This was followed by a layer deposited with a sputter gas composition of Ar/O2 (0.2%) to give a 500 nm thick layer with a sheet resistance of 15 Ω /sq or $\rho \approx 8x\,10$ -4 Ω -cm. Electron beam evaporation was used to deposit Ni/Al grids with ~5% shading loss and a 125 nm thick MgF2 layer which produces a broad minimum in the reflection spectrum between 500-800 nm. Cell areas were delineated by mechanical scribing to give individual cells with area 0.4 cm². Characterization of the devices included the total area current-voltage (J–V) response measured at 25°C under AM1.5 illumination and quantum efficiency (QE) measured under white light bias as a function of voltage bias. J–V parameters were measured at NREL on four devices, and gave good agreement with the measurements at IEC.

The solar cell parameters V_{oc} , J_{sc} , fill factor (FF) and efficiency (η) determined from J–V measurements at 25°C are listed in Table 2.2 for seven bandgaps from 1.16 to 1.45 eV and the corresponding J–V curves are shown in Figure 2.6. The efficiency is ~ 15% for $E_g < 1.3$ eV with FF = 73–75%, so the increase in V_{oc} offsets the decrease in J_{sc} . For $E_g > 1.3$ eV the FF and η decrease sharply. Figure 2.7 shows the increase in V_{oc} with bandgap up to 788 mV with linear behavior up to $E_g = 1.4$ eV. Quantum efficiency curves for these devices, plotted in Figure 2.8, show a shift in the long wavelength fall-off consistent with the shift in E_g .

Table 2.2. $Cu(InGa)Se_2$ device parameters under AM1.5 illumination at 25 ° C.

E_{g}	V _{oc}	J_{sc}	FF	η	Ga
(eV)	(mV)	(mA/cm ²)	(%)	(%)	(%)
1.16	602	33.2	74.1	14.8	27
1.18	623	32.8	73.1	14.9	30
1.21	653	32.0	73.5	15.4	34
1.23	639	31.9	74.3	15.1	38
1.27	689	28.9	75.0	15.0	43
1.37	746	25.2	69.7	13.1	57
1.45	788	20.3	63.4	10.1	69a

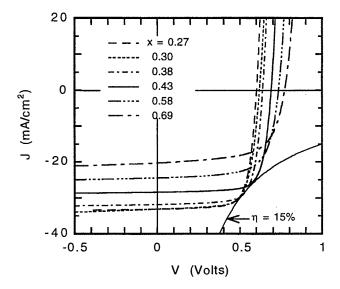


Figure 2.6. J–V curves at 25°C under AM1.5 illumination for E_g from 1.16 to 1.45eV. The equal efficiency line corresponding to 15% is also shown.

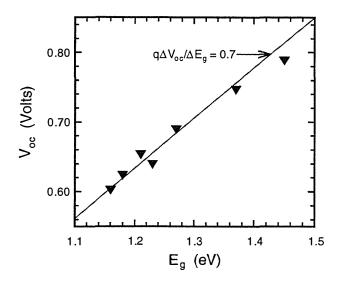


Figure 2.7. The increase in V_{oc} with E_g . The solid line is a fit to the values for $E_g < 1.4$ which gives a slope of 0.7.

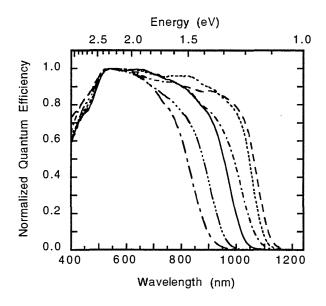


Figure 2.8. The normalized quantum efficiencies of the 7 $Cu(InGa)Se_2$ devices showing a shift in the long wavelength response comparable to the change in E_g . The different lines correspond to the same compositions as Figure 2.6.

2.1.5 Cu(InGa)Se₂ Device Analysis

Detailed analysis of the room temperature J–V behavior was carried out to characterize the diode behavior and identify the cause of the reduced performance with the highest Ga content. The data is described by a standard diode model with the forward diode current

limited by Shockley-Read-Hall recombination through states within the space charge region of the Cu(InGa)Se₂ [2.12, 2.13]. This gives a diode equation

$$J = J_o \exp\left[\frac{q(V - RJ)}{Akt}\right] - J_o - J_L + GV$$
 (2.1)

with

$$J_{o} = J_{oo} exp\left(-\frac{E_{g}}{2kT}\right), \tag{2.2}$$

where J_o is the forward current, A the diode quality factor, R_s the series resistance, G the shunt conductance in the dark, and J_{oo} the forward current prefactor. To analyze the J–V data, G and R_s are first determined and used to determine A and J_o . G was obtained from the minimum value of the slope dJ/dV since the derivative of the first term in Eq. 2.1 is vanishingly small at low or negative V giving

$$\frac{\mathrm{dJ}}{\mathrm{dV}} \approx G - \frac{\mathrm{dJ_L}}{\mathrm{dV}}.\tag{2.3}$$

If JL does not have a strong voltage dependence, then dJ/dV is constant at small voltage, and G is determined for the dark curve in reverse bias. This is used to calculate J' = J - GV. Then R_s and A were obtained from the intercept and slope of a linear fit to dV/dJ' plotted versus (J'+J_{sc})-1 since differentiating Eq. 2.1 with $R_sG << 1$ gives

$$\frac{dV}{dJ'} = R_s + \frac{AkT}{q} (J' + J_{sc})^{-1}$$
(2.4)

Finally, a logarithmic plot of $J'+J_{sc}$ versus $V-R_sJ'$ gives an intercept of J_o and slope q/AkT which was also used to determine A. This gave good agreement with A determined from dV/dJ' as a check on the analysis.

This analysis is shown in Figs. 2.9–2.11 for the devices with $E_g=1.16$ and 1.45 eV. Figure 2.9 shows dJ/dV from -0.4 to 0.4V for both the dark and illuminated data. For $E_g=1.16$ eV, the flat region of the dark curve shows a shunt G=0.4 mS/cm² while the illuminated data is also flat, indicating simple ohmic behavior. For $E_g=1.45$ eV, the dark gives G=0.1 mS/cm². However, in this case the illuminated data does not level off so no simple ohmic shunt behavior can be ascribed. Instead, this suggests a contribution from the second term in Eq. (2.3) indicating a voltage dependent current collection, JL(V). Figure 2.10 shows dV/dJ in forward bias. For $E_g=1.16$ eV, the derivative is linear and the fits shown gives $R_s=0.1$ Ω -cm² and A=1.7 in the dark and $R_s=0.02$ Ω -cm² and A=1.7 under illumination. The device with $E_g=1.45$ eV has similar behavior in the dark, with $R_s=0.1$ Ω -cm² and A=1.9, but under illumination the derivative is not linear and no fit can be done to determine R_s and A.

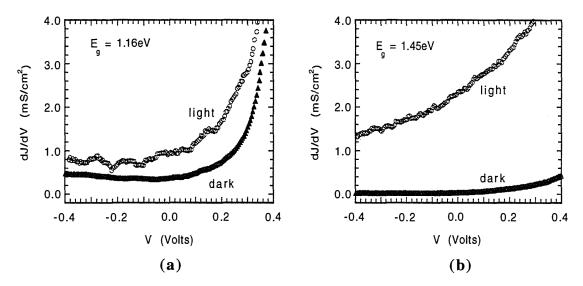


Figure 2.9. The derivative dJ/dV used to determine the shunt, in the dark and under illumination, for (a) $E_g = 1.16$ eV and (b) $E_g = 1.45$ eV.

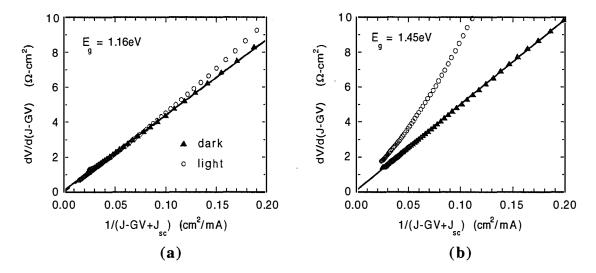


Figure 2.10. The derivative dV/dJ in forward bias, in the dark and under illumination, for (a) $E_g = 1.16~eV$ and (b) $E_g = 1.45~eV$. Lines show the fits to determine R_s and A.

Finally, the logarithmic plot of $J'+J_{sc}$ vs $V-R_sJ'$ is shown in Figure 2.11 for the J-V results both in the dark and under illumination for these samples. For the lower bandgap case, there is little difference in the diode behavior between the dark and illuminated results. The slope in each case gives A=1.7, in agreement with the result from fitting dV/dJ. The linear behavior shown in these plots for $E_g=1.16~eV$ is similarly observed in all the samples with $E_g<1.3eV$. However, the higher bandgap device shows a large excess current under illumination and the J-V data does not follow the simple exponential form of Eq. (2.1). This prevents J_0 and A from being determined under illumination for this sample and for $E_g=1.37eV$.

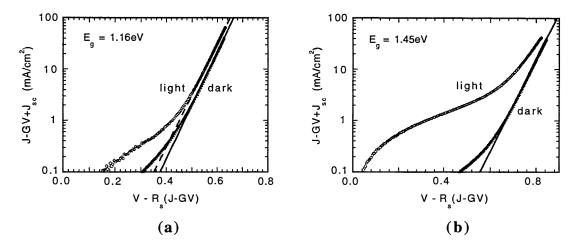


Figure 2.11. Logarithmic plot of J'+Jsc versus V-R_sJ, in the dark and under illumination, for (a) $E_g = 1.16 eV$ and (b) $E_g = 1.45 eV$. Lines show the fits to determine J_0 and A.

The difference between the illuminated and dark J–V characteristics for $E_g > 1.3 \mathrm{eV}$ can be attributed to a voltage dependent current collection. This is seen in the ratio of the QE at reverse voltage bias to the QE measured at J_{sc} which is shown in Figure 2.12 for the same two devices analyzed above. Only the higher bandgap device has this QE ratio increasing significantly as the wavelength increases, suggesting that the current collection is a function of the space charge width in the Cu(InGa)Se₂. The increase in the current from 0 to -1V determined from the integrated QE curves in this case is $1.5 \mathrm{mA/cm^2}$. The voltage dependent current collection can also be seen directly in the J–V curve for $E_g = 1.45 \mathrm{eV}$ in Figure 2.6. The measured current increases by $1.3 \mathrm{mA/cm^2}$ from J_{sc} to -1V.

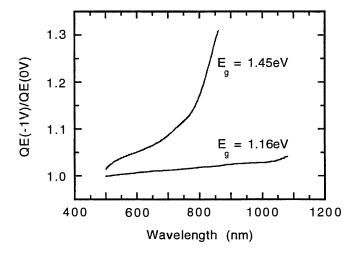


Figure 2.12. The ratio QE(-1V)/QE(0V) for the devices with $E_g=1.16eV$ and 1.45eV showing a voltage dependent current collection for the latter.

The results of the diode analysis for the J–V data under illumination are summarized in Table 2.3, with J_{00} calculated according to Eq. (2.2). The diode factor determined for the dark data, A(dark), is also listed. There is no increase in G or R_s for the high Ga devices

and only a small increase in A, so the voltage dependent collection is apparently responsible for the lower FF. This can also cause a decrease in $V_{\rm oc}$.

Table 2.3. Cu(InGa)Se₂ device parameters under AM1.5 illumination at 25°C and results of diode analysis.

	dark					illumi	nation		
\mathbf{E}_{g}	G	R_s	J_{o}	J_{oo}	Α	R_s	J_{o}	J_{oo}	Α
(eV)	(mS/cm ²)	$(\Omega\text{-cm}^2)$	(mA/cm ²)	(mA/cm ²)		$(\Omega\text{-cm}^2)$	(mA/cm ²)	(mA/cm ²)	
1.16	0.4	0.1	1x10 ⁻⁵	0.7x10°	1.6	0.02	3x10 ⁻⁵	2x10°	1.7
1.18	1.1	0.5	$2x10^{-5}$	$2x10^{5}$	1.7	0.3	$4x10^{-5}$	$3x10^{5}$	1.7
1.21	0.2	0.2	$5x10^{-6}$	$0.7x10^{5}$	1.7	0.2	2x10 ⁻⁵	3x10 ⁵	1.8
1.23	0.1	0.1	$2x10^{-6}$	0.6×10^{5}	1.6	0.07	1x10 ⁻⁵	2x10 ⁵	1.7
1.27	0.8	0.07	$4x10^{-6}$	3x10⁵	1.8	0.05	$5x10^{-6}$	2x10 ⁵	1.7
1.37	0.2	0.0	$3x10^{-6}$	13x10⁵	1.9	*	*	*	*
1.45	0.1	0.1	1x10 ⁻⁶	16x10⁵	1.9	*	*	*	*

^{*} could not be determined (see text).

These device parameters can be used to determine the slope of the increase in V_{oc} with E_g . Solving Eq. (2.1) for J = 0, with $GV_{oc} \ll J_{sc}$, gives:

$$qV_{oc} = \frac{A}{2}E_g + AkTLn\left(\frac{J_{sc}}{J_{oo}}\right). \tag{2.4}$$

The devices with $E_g < 1.3 \text{eV}$ have $A \approx 1.7$ so the first term gives a slope $q(dV_{oc}/dE_g) = A/2 \approx 0.85$. Since $J_{oo} \approx 2.5 \times 105$ mA/cm², the second term reduces this slightly to give a predicted slope $q(dV_{oc}/dE_g) \approx 0.75$ –0.8. As shown in Figure 2.7, a fit to the data up to $E_g = 1.4 \text{eV}$ gives $q\Delta V_{oc}/\Delta E_g \approx 0.7$.

Analysis of the J–V and QE results show that the diode behavior with $E_g < 1.3 \mathrm{eV}$ can be described by a standard diode model with an activation energy of the forward current equal to $E_g/2$ and constant J_{oo} . This supports the determination that the forward current is controlled by recombination in the space charge region of the absorber. V_{oc} increases linearly to 750 mV with a slope determined primarily by the absorber bandgap and the diode quality factor. The dominant additional effect with high Ga content can be attributed to a current collection which depends on the space charge width in the $Cu(InGa)Se_2$ and changes with voltage bias. This may be due to a poor minority carrier diffusion length in these films. It should also be mentioned that the device performance has been suggested elsewhere to fall off with high Ga due to a change in the electronic properties of a Cudeficient surface layer [2.3, 2.9].

In conclusion, the performance of solar cells fabricated from Cu(InGa)Se₂ films with no intentional compositional gradients has been characterized as the Ga content and bandgap are increased. It was shown that the Cu(InGa)Se₂ films could be deposited with a wide range of Ga content and bandgap with no change in structure, morphology, or compositional uniformity. Solar cells fabricated from these films had a constant 15% device efficiency with x < 0.5 or E_g < 1.3eV. V_{oc} as high as 788mV was achieved with E_g = 1.45 eV but with a concurrent fall-off of fill factor and efficiency. Analysis of current-voltage and quantum efficiency results shows that this decrease in device performance for E_g > 1.3eV is primarily caused by a voltage dependent current collection.

2.2 Selenization of Cu-Ga-In Precursors

2.2.1 Introduction

Cu-Ga-In precursors reacted in a selenium containing atmosphere in the temperature range $400^{\circ}\text{C}-500^{\circ}\text{C}$ contain a mixture of CuInSe₂ (CIS) and CuGaSe₂ (CGS) phases instead of the desired single phase CuGa_xIn_{1-x}Se₂(CIGS) [2.14]. From X-ray diffraction and Auger analysis, the mixed phase films form a layered structure with the CIS phase near the surface and the CGS phase near the Mo/film interface. Annealing of these films in the temperature range $500^{\circ}\text{C}-600^{\circ}\text{C}$ in an inert atmosphere for a duration of 60 to 90 minutes converts the multiphase structure in the film to a single phase CIGS. In this section, solar cells made with the multiphase films are shown to have properties similar to CuInSe₂ devices while cells made with the annealed single phase films behave like Cu(InGa)Se₂ devices with the bandgap expected for the precursor composition. Additionally, preliminary results are presented of experiments to determine the diffusion coefficient of In in CGS, Ga in CIS and the interdiffusion coefficients of In and Ga in a CGS/CIS diffusion couple.

2.2.2 Experimental Procedures

Metal precursor films were deposited in the sequence Cu-Ga-In at room temperature onto Mo coated soda lime glass substrates by DC magnetron sputtering 1. The Cu thickness was chosen to be 250 nm and the thicknesses of Ga and In layers were adjusted to yield a Cu/(In+Ga) ratio of approximately 0.9. Precursor films with Ga/(Ga+In) ratios of 0, 0.25, 0.5, 0.75, and 1.0 were prepared.

The films were selenized in a flowing H₂Se/Ar/O₂ mixture for 90 minutes after a 10 min ramp to the chosen substrate temperature [2.15]. A substrate temperature of 410°C was used with the Cu-In precursor while the films containing Ga were reacted at 450°C. Post-reaction heat treatments for 60–90 minutes were carried out in-situ in an Ar atmosphere at 500°C and 600°C for the films with different Ga/(Ga+In) ratios, followed by a second exposure to the gas mixture containing H₂Se to compensate a possible Se loss at the films surface. The structure of the absorber layers was examined by X-ray diffraction (XRD) and their composition was determined by energy dispersive X-ray spectroscopy (EDS) and Auger depth profiles.

CIGS/CdS solar cells were completed on the absorber layers using the processes described in section 2.1.4. No anti-reflection coatings were used. The solar cells were characterized by current-voltage and spectral response measurements. Estimations of the parameters of minority carrier transport and the bandgap of the absorber were derived from the long wavelength cut-off of the spectral response [2.16]. Capacitance was measured with a 100 kHz/50 mV excitation under ambient light.

For the diffusion experiments, CGS films were coated with an In layer with thickness ~1000 Å. These films were annealed at different temperatures ranging from 400°C to 600°C for 30 minutes in an Argon atmosphere. The CGS/CIS diffusion couple was prepared by first reacting Cu-Ga films to form a CGS layer, onto which Cu and In layers, with Cu/In \approx 0.9, were sputter-deposited sequentially, followed by reaction in H₂Se to a form a CIS layer. The desired film thicknesses of CIS and CGS were approximately 2 μ m each. The diffusion couple was annealed at 650°C for 30 minutes in an Ar atmosphere. The concentration profiles in the above samples were determined by AES depth profiling. Depth profiles of a CGS/In sample and a CGS/CIS sample which did not undergo any annealing treatment were also measured.

2.2.3 Selenization Results

The selenization of Cu-In and Cu-Ga precursor films resulted in single phase CuInSe₂ and CuGaSe₂, respectively. However, the selenization of the Cu-Ga-In precursors resulted in a film containing CuInSe₂ and CuGaSe₂ with little intermixing. The XRD spectrum of the (220) and (204) reflections from the film with $Ga/(In+Ga) \approx 0.5$ is shown in Figure 2.13. The as-selenized film showed distinct peaks corresponding to phases close to CuInSe₂ and CuGaSe₂. Even though CuInSe₂ and CuGaSe₂ are miscible at all concentrations, there is little Cu(InGa)Se₂ evident in the spectrum. The Auger depth profile of this film, shown in Figure 2.14, indicates that the film had a layered structure with CuGaSe₂ near the back and CuInSe₂ at the surface.

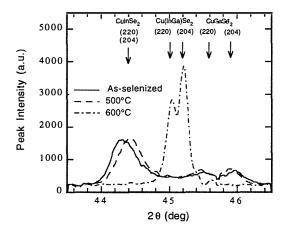


Figure 2.13. X-ray diffraction spectra of (220) and (204) reflections of asselenized and heat treated $Cu(InGa)Se_2$ films with $Ga/(Ga+In) \approx 0.5$.

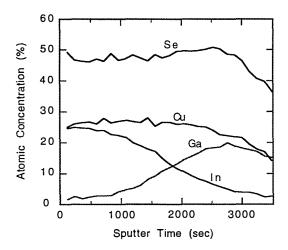


Figure 2.14. Auger depth profile of an as-selenized $Cu(InGa)Se_2$ film with a $Ga/(Ga+In) \approx 0.5$.

XRD spectra after the in-situ Ar atmosphere anneals at 500°C and 600°C are also shown in Figure 2.13. After the 500°C anneal, the film still retained the two-phase structure of the as-selenized film. The 600°C anneal, however, converted the film to single phase Cu(InGa)Se₂. The Auger depth profile in this case is shown in Figure 2.15 and confirms

that the Ga and In are more homogeneously distributed. Similar behavior was observed for the films with $Ga/(In+Ga) \approx 0.25$. However, the film with $Ga/(In+Ga) \approx 0.75$ was converted to single phase after the 500°C anneal. Since the homogenization occurred at a lower temperature, it is assumed that inter-diffusion of In and Ga is faster in films with greater Ga content.

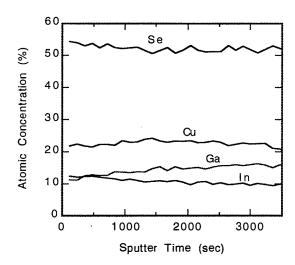


Figure 2.15. Auger depth profile of an annealed (60 minutes, 600° C in Ar) $Cu(InGa)Se_2$ film, with a $Ga/(Ga+In) \approx 0.5$.

Device results for the solar cells made from films with the different Ga contents and anneal conditions are listed in Table 2.4. Spectral response plots for the as-selenized and annealed films with $Ga/(In+Ga) \approx 0.5$ are shown in Figure 2.16. The open circuit voltage and long wavelength cut-off of the spectral response of the as-selenized multi-phase absorbers are similar to CuInSe₂ cells. The photovoltaic response is controlled by the more In-rich, lower bandgap phase close to the heterojunction. The second phase is separated from the active layer of the device and does not deteriorate the cell performance. Devices with the annealed single-phase films have increased V_{oc} and a shift in the spectral response cut-off consistent with the expected Ga/(In+Ga) for these films. Evaluation of the spectral response and capacitance for all cells suggests a narrow field zone and a good diffusion length of 0.6–1 μ m. The long wavelength spectral response can be described with good accuracy by assuming a constant, direct bandgap, i.e., there is no indication for a graded bandgap.

Table 2.4. Cell results from selenized Cu-Ga-In precursors with different Ga content.

Ga Ga+I n	Anneal (°C)	Structure	Cu (at.%)	In (at.%)	Ga (at.%)	Se (at.%)	v _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)
0	-	CuInSe ₂	23.9	25.0	***	51.1	0.44	39	66	11.2
0.25	-	multi-phase	22.3	14.0	2.9	50.8	0.46	39	58	10.4
0.25	500	multi-phase	22.7	22.5	2.6	52.2	0.45	38	68	11.5
0.25	600	single-phase	22.3	18.6	5.9	53.2	0.56	34	67	12.9
0.50	-	multi-phase	22.4	18.9	7.9	50.8	0.53	38	64	13.1
0.50	500	multi-phase	22.4	18.3	8.9	50.4	0.54	35	66	12.5
0.50	600	single-phase	22.3	12.8	13.2	51.7	0.59	30	60	10.5
0.75	600	single-phase	21.6	7.0	19.0	52.4	0.63	22	46	6.4

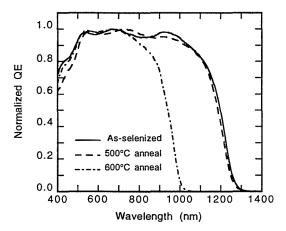


Figure 2.16. Spectral response of devices made from an as-selenized and heat treated $Cu(InGa)Se_2$ film with $Ga/(Ga+In) \approx 0.5$.

To summarize, absorber films prepared by selenization of Cu-Ga-In precursor layers with H₂Se are inhomogeneous with a layered structure containing two phases with compositions close to CuInSe₂ and CuGaSe₂. Cell results and spectral response measurements are consistent with the In-rich phase at the top of the film and exhibit a comparable or better performance than cells based on single phase CuInSe₂. An in-situ anneal in Ar, immediately after the selenization, is shown to create homogeneous, single phase films, even at high Ga-content. Material and device measurements show that these films contain the same Ga/(In+Ga) composition as the starting precursors.

2.2.4 Diffusion Results

Interdiffusion of In and Ga appears to be responsible for this homogenization process of mixed-phase, as reacted CIGS films. Walter and Schock reported that interdiffusion of In and Ga was greatly enhanced in the presence of the copper selenide phase in copper rich CIS/CGS films [2.18]. Thus, all the CGS, CIS films used for the diffusion experiments were prepared copper poor to avoid the formation of a copper selenide phase. SEM, EDS, XRD, and AES measurements have been completed on samples of In on CGS, Ga on CIS, and CGS/CIS diffusion couples. These results will be analyzed to determine the diffusion coefficients. The Auger profiles for In in CGS in the unannealed and annealed samples are shown in Figure 2.17. The concentration profiles of In and Ga for the unannealed sample and the annealed sample are shown in Figure 2.18. This data will be analyzed to determine the diffusion coefficients. The measurements made for Ga on CIS gave unexpected results; after heat treatment, a multi-phase structure was formed consisting of InSe and CIGS. Additional experiments are underway to understand the results.

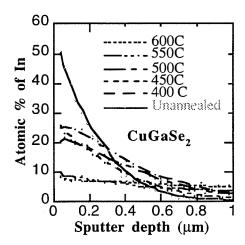


Figure 2.17. Depth profiles of In in CGS.

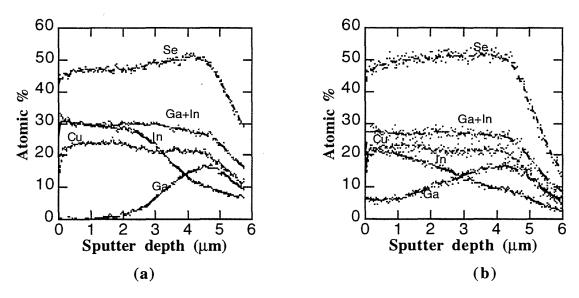


Figure 2.18. Concentration profiles of Cu, In, Ga and Se in CGS/CIS diffusion couples: (a) Initial distribution (b) After annealing at 650°C for 30 minutes.

References - Section 2

- 2.1. J. Hedstrom, H. Ohlsen, M. Bodegard, A. Kylner, L. Stolt, D. Hariskos, M. Ruckh, and H. W. Schock, *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference*, Louisville, KY (Institute of Electrical and Electronics Engineers, New York, 1993), p. 364.
- 2.2. J. R. Tuttle, M. A. Contreras, T. J. Gillespie, K. R. Ramanathan, A. L. Tennant, J. Keane, A. M. Gabor and R. Noufi, *Prog. in PV: Research and Appl.* 3, 235 (1995).
- 2.3. H. W. Schock, *Proceedings of the 12th European Photovoltaic Solar Energy Conference*, Amsterdam, The Netherlands (H.S. Stephens & Assoc. UK, 1994), p. 944.
- 2.4. J. M. Stewart, W. S. Chen, W. E. Devaney, and R. A. Mickelsen, *Proceedings of the 7th International Conference on Ternary and Multinary Compounds*, edited by S. K. Deb and A. Zunger (Materials Research Society, Pittsburgh, 1987), p. 59.
- 2.5. M. A. Contreras, J. Tuttle, A. Gabor, A. Tennant, K. Ramanathan, S. Asher, A. Franz, J. Keane, L. Wang, and R. Noufi, *Proceedings of the 24th IEEE Photovoltaic Specialists Conference*, Waikoloa, HI (Institute of Electrical and Electronics Engineers, New York, 1995), p. 68.
- 2.6. B. Dimmler, H. Dittrich, R. Menner, and H. W. Schock, *Proceedings of the 19th IEEE Photovoltaic Specialists Conference*, New Orleans, LA (Institute of Electrical and Electronics Engineers, New York, 1987), p. 1454.
- 2.7. B. Grzeta-Plenkovic, A. Popovic, B. Celustka, and B. Santic, J. Appl. Cryst. 13, 311 (1980).
- 2.8. R. W. Birkmire, J. E. Phillips, W. A. Buchanan, S. S. Hegedus, B. E. McCandlless and W.N. Shafarman, Annual Subcontract Report No. XAV-3-13170-01, (NREL, Colorado, 1995), pp. 22–3.
- 2.9. D. Schmid, M. Ruckh, F. Grunwald, and H. W. Schock, *J. Appl. Phys.* **73**, 2902 (1993).
- 2.10. J. Kessler, K. Velthaus, M. Ruckh, R. Laichinger, and H. W. Schock, D. Lincot, R. Ortega, and J. Vedel, *Proceedings of the 6th International Photovoltaic Science and Engineering Conference*, New Delhi, India (Oxford and IBH, New Delhi, 1992) p. 1005.
- 2.11. W. E. Devaney, W. S. Chen, J. M. Stewart, and R. A. Mickelsen, *IEEE Trans. on Electron Devices* 37, 428 (1990).
- 2.12. M. Roy, S. Damaskinos, and J. E. Phillips, *Proceedings of the 20th IEEE Photovoltaic Specialists Conference*, Las Vegas, NV (Institute of Electrical and Electronics Engineers, New York, 1988), p. 1618.
- 2.13. W. N. Shafarman and J. E. Phillips, *Proceedings of the 22nd IEEE Photovoltaic Specialists Conference*, Las Vegas, NV (Institute of Electrical and Electronics Engineers, New York, 1991), p. 934.

- 2.14. M. Marudachalam, R.W. Birkmire, J.M. Schultz and T. A. Yokimcus, Proceedings of the 24th IEEE Photovoltaic Specialists Conference, Waikoloa, HI (Institute of Electrical and Electronics Engineers, Hawaii USA, 1994), p. 234.
- 2.15. S. Verma, T. W. F. Russell, and R. W. Birkmire, *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference*, Louisville, KY (Institute of Electrical and Electronics Engineers, New York, 1993), p. 431.
- 2.16. R. Klenk and H. W. Schock, *Proceedings of the 12th European Photovoltaic Solar Energy Conference*, Amsterdam, The Netherlands (H. S. Stephens & Associates, UK, 1994), p. 1588.
- 2.17. T. Walter and H.W. Schock, Thin Solid Films 224, 74 (1993).

3.0 AMORPHOUS SILICON RESEARCH

The present report covers the activities at IEC in the area of a-Si research from 1/16/95 to 1/15/96 within the framework of the Subcontract No. XAV-3-13170-01 from NREL.

The goals set forth for this time period were as follows:

- Obtain a 5% improvement in J_{sc} over the baseline process without any loss in V_{oc} and FF.
- Obtain a 5% improvement in V_{oc} over the baseline process without any loss in J_{sc} and FF.
- Establish through quantitative experimentation how the optical enhancement schemes affect J_{sc} and other solar cell parameters.
- Provide quantitative updates for the device design team storyboards in verifying the effectiveness of countermeasures for the cell performance.

In the following sections the work performed and the results obtained in each of the above topics will be presented separately. However, for practical reasons the topics covering 5% improvement in J_{sc} and 5% improvement in V_{oc} will be combined into one section.

The reference baseline for the J_{sc} and V_{oc} improvements was taken as the average cell parameters obtained in six different runs identified in last year's report [3.1]. These average parameters were (after correcting V_{oc} to 25°C): $J_{sc} = 13.8$ mA/cm², $V_{oc} = 0.814$ V, FF = 71.6%.

It should be pointed out that the above baseline was established in cells of 0.07 cm² area. In contrast, as part of program requirements, the research during the present time period was exclusively conducted with cells of 0.40 cm² area.

3.1 Summary

The first task in improving J_{sc} and V_{oc} was to determine operational characteristics of the a-Si reactor. It was found through QE measurements and SIMS analysis that there was significant dopant carryover from one run to the next from the film deposited on the "hot" electrode. Deposition of a burying layer of a-SiC:H between device runs was found to be necessary to remedy the dopant carryover. As a result, FFs in excess of 71% were obtained reproducibly. In a second step, H_2 diluted μc n-layers, compatible with ZnO/Ag back contact as well as with tunnel junction in tandem devices, were developed. These μc n-layers with conductivities and activation energies of 1 S/cm and 0.05 eV, respectively, allowed fabrication of devices with ZnO/Ag contact with FFs as high as 72%. In the case of 25 Å Ti/5000 Å Ag contacts, the deposition rate of Ag was found to be an important parameter in that rates below 100 Å/min resulted in lower FFs. As a consequence of these developments, the goals of improving J_{sc} by 5% and V_{oc} by 5% over the baseline values, separately and in some cases together within the same device, were achieved as shown in Table 3.1.

Table 3.1. List of devices meeting the J_{sc} and V_{oc} goals of the present contract period.

Sample ID	V _∞ * (V)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)	Contact	$ m V_{\infty}$ Goal	J _{sc} Goal
4492-12-2	0.851	13.7	71.3	8.3	Ti/Ag	\checkmark	
4486-11-2	0.858	13.6	71.7	8.4	Ti/Ag	√	1
4490-21-3	0.821	16.0	70.8	9.2	ZnO/Ag		√
4492-11-2	0.846	14.9	72.0	9.1	ZnO/Ag	$\sqrt{}$	√
4484-11-2	0.837	15.4	71.0	9.2	ZnO/Ag		√ √
4480-11-2	0.827	14.4	71.5	8.5	Ti/Ag		√
4486-21-2	0.846	14.4	71.9	8.8	Ti/Ag	√	√

^{*} Corrected to 25°C

Analysis of back reflector optical enhancements in a-Si solar cells using substrates with a range of TCO textures concluded that a textured substrate is much more effective at increasing red response than a smooth substrate with external textured Ag Back Reflector (BR). Measurements of JV and QE characteristics on ITO/pin/TCO/glass type cells with smooth and textured external Ag BR optically coupled to the glass substrate showed that a *textured* substrate with a *smooth* Ag BR has 15% higher J_{SC} than a *textured* Ag BR on a *smooth* device (15.1 vs 13.3 mA/cm²). The red QE is tripled for the textured substrate (0.11 vs 0.32). Thus, a textured substrate, even though transparent, is much more effective at light trapping than a textured Ag BR on a smooth device. This suggests that the replication of the substrate texture on the top a-Si surface is crucial to enhance multiple scattering from the underlying substrate.

Within the context of optical enhancement schemes in a-Si devices, the effect of textured tin oxide and zinc oxide substrates on the current generation in amorphous silicon solar cells were also analyzed. The results show that increasing substrate haze above $\approx 7\%$ for SnO₂ and above $\approx 5\%$ for ZnO has negligible impact on the current generation at long wavelengths. In presently available textured ZnO, current generation is about 0.6 mA/cm² greater than in textured SnO₂ for i-layer thicknesses in the range of $\approx 0.4~\mu m$.

As part of the work associated with the device design team a simple lumped circuit model previously developed to analyze light and dark JV curves of a-Si devices was applied to a much wider range of single junction devices and conditions. These included p-i-n and n-i-p cells on smooth or textured substrates, a-Si and a-SiGe cells, initial and stabilized, and under AM1.5 and red filtered light. Excellent agreement has been found between the model and the measurements. Devices analyzed covered a wide range of sources. In addition to those from IEC, cells were provided by Solarex, USSC, ECD, and APS. Analysis of triple junction cells using a parameter set based on the stabilized high, middle and low bandgap cells from USSC was also performed.

3.2 Improvements in J_{SC} and V_{OC}

3.2.1 Device Configuration

Devices used in the present program are single junction, superstrate p-i-n a-Si:H solar cells. The device configuration is shown schematically in Figure 3.1, below.

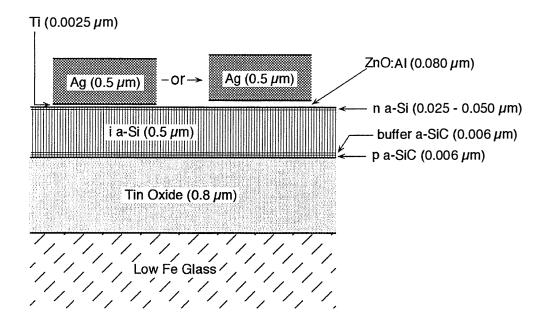


Figure 3.1 Schematic cross section of the devices used in the present program.

Four circular devices of 0.28" diameter (0.4 cm^2 area) were defined on each 1" x 1" substrate by putting down back contact metallization through a 0.004" thick Mo mask. Two types of back contact metallization were used. The first is Ti (25 Å) / Ag (5000 Å) sequentially deposited by ebeam evaporation at deposition rates of 2 Å/s and 100 Å/s, respectively, with a source-to-substrate distance of 14". There was no intentional substrate cooling or heating. System base pressure was in the range of 1 to $3 \times 10^{-6} \text{ T}$. ZnO:Al (800 Å) and Ag(5000 Å) contacts are deposited in different systems. ZnO:Al is sputtered in argon at a pressure of 3 mT and a flow rate of 100 sccm from an 8" circular target of ZnO:Al₂O₃, containing 1% by weight of Al₂O₃. Sputtering rate of 1000 Å/min was achieved at a power level of 900 W, reflected power being 25 W. Target to substrate distance was 2.5". The silver films were deposited, as before, by e-beam evaporation under the same condition.

a-Si films are deposited in a glow discharge reactor which will be described in the next section.

Glass/tin oxide substrates are provided by Solarex Corporation. The glass is of low iron soda lime type of 2 mm thickness. Tin oxide films, doped with F, are made by APCVD at Solarex. Electrical and optical properties of these films are given in Table 3.1, and their surface topography is shown in Figure 3.2.

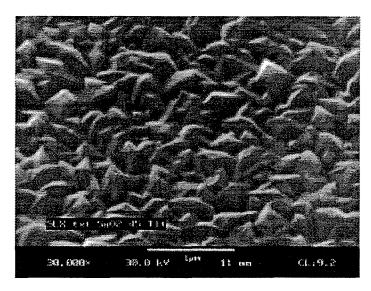


Figure 3.2 SEM micrograph showing surface topography of SnO_2 film. Magnification marker = 1 μm .

3.2.2 Reactor Description

The plasma-assisted CVD (PECVD) reactor used for the deposition of the a-Si:H films has been described previously in the last years report [3.1]. Therefore, only a brief description will be given here.

The reactor is of a three chambered load-locked design with a center chamber housing the deposition "can," and the two outer chambers being used for reactor loading/unloading. The reactor can accommodate substrates up to 4" x 4" in size. In the present program a standard load is four 1" x 1" SnO₂ coated glass substrates labeled -11, -12, -21, -22.

High vacuum ($\approx 10^{-7}$ Torr base pressure) pumping is achieved through the first chamber using a 170 l/s Balzers turbomolecular pumping unit. A 13 l/s Leybold D408CS corrosive series rotary vane pump is used as the process pump. Gases are delivered via mass flow controllers through a manifold into the bottom of the center chamber. Pressure is controlled by an MKS throttle valve controller and capacitance manometer. The substrates and the deposition can are heated separately, the former with quartz resistance heaters, and the latter with a single coiled resistance heating element. Temperature is controlled by Eurotherm temperature controllers. RF power is delivered by an ENI 300W power supply and matching network. The electrode is a 5 in. diameter perforated Mo disc. The electrode-to-substrate spacing is 0.625 in. System diagram of the reactor is shown in Figure 3.3.

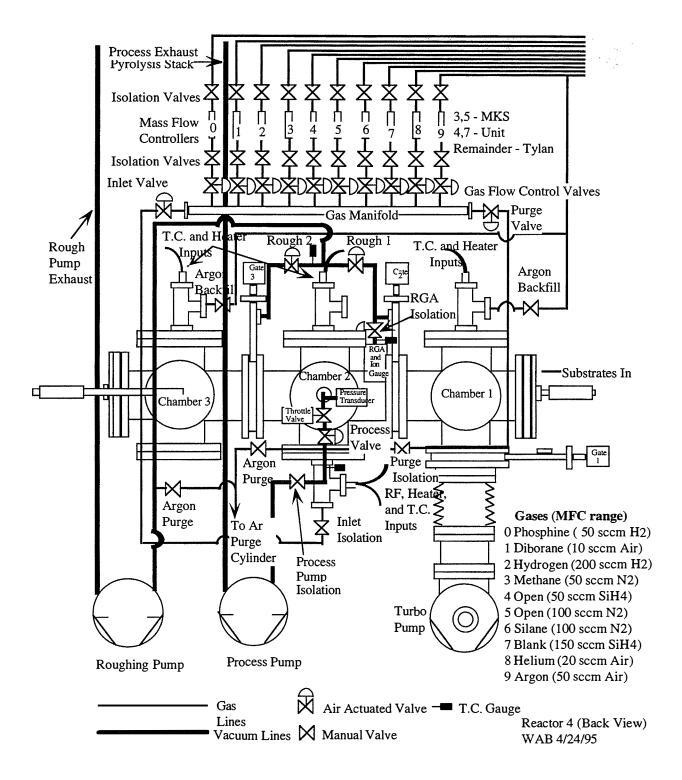


Figure 3.3. System diagram of the a-Si:H plasma-assisted CVD reactor.

3.2.3 Results And Discussion

Process Optimization and Device Results

During the time period covered by this report the goals of the program, which are the subject of this section, were to increase V_{oc} and J_{sc} separately by 5% from the baseline values of the previous reporting period. FF was to be no less than the baseline value. This baseline was (after correcting V_{oc} to 25°C): $J_{sc}=13.8$ mA/cm², $V_{oc}=0.814$ V, FF = 71.6%. In pursuit of this goal 122 runs were made in the PECVD system. Of these 10 were single layer runs made for the purpose of determining properties of the individual layers. The rest were all device runs. Figures 3.4 to 3.7 give V_{oc} , J_{sc} , FF, and Eff, respectively, as a function of run number. Shown are the data from substrate from position -22 contacted with Ti/Ag, and data from substrate contacted with ZnO/Ag when available. As such, they are not necessarily highest efficiency devices from each run.

The starting point of the effort was the device defined earlier as the baseline. The properties of the TCO used are given in Table 3.2 and the deposition parameters of this device are given in Table 3.3.

Table 3.2. Typical properties of Solarex tin oxide films.

Thickness (µm)	R_{sh} (Ω/sq)	ρ (Ω·cm)	μ_H (cm ² /V·s)	n (cm ⁻³)	Haze @ 700 nm (%)	Absorp. @ 550 nm (%)
1.2	16	2.0x10 ⁻³	18	1.7x10 ²⁰	14	5.6

Table 3.3. Deposition parameters of the baseline device.

Layer	р	buffer	i	n
Time (min:sec)	0:20	0:20	30:00	2:00
Pressure (T)	0.2	0.2	0.2	0.5
Temperature (°C)	150	150	175	175
RF Power (W)	20	20	7	10
SiH ₄ (sccm)	20	20	20	10
H ₂ (sccm)				
CH ₄ (sccm)	30	10		
2% B ₂ H ₆ in H ₂ (sccm)	2.5			
2% PH ₃ in H ₂ (sccm)				5

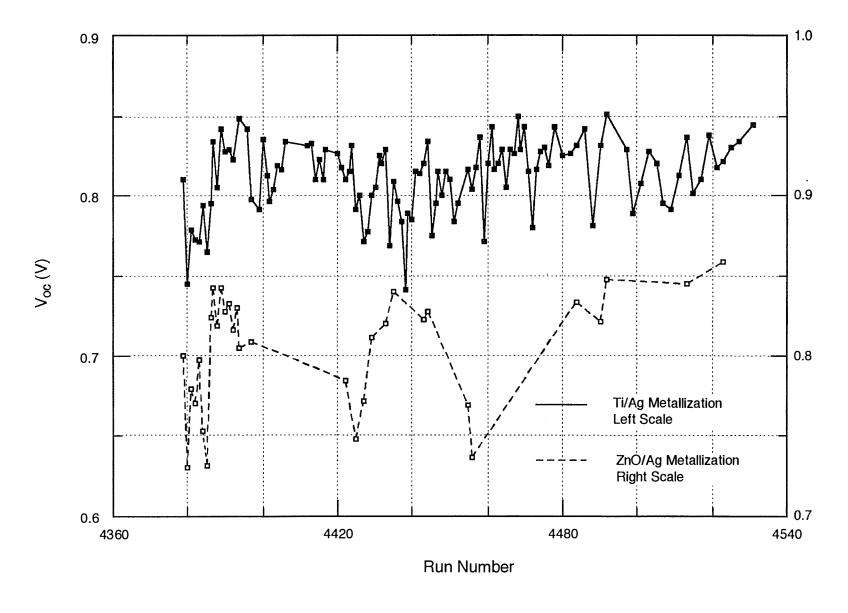


Figure 3.4. Open circuit voltage as a function of run number.



Figure 3.5. Short circuit current as a function of run number.

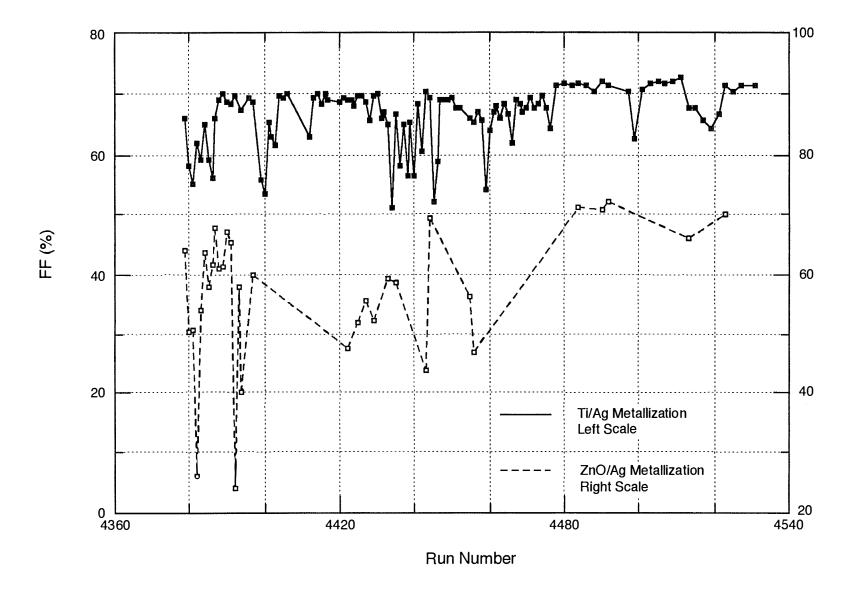


Figure 3.6. Fill factor as a function of run number.

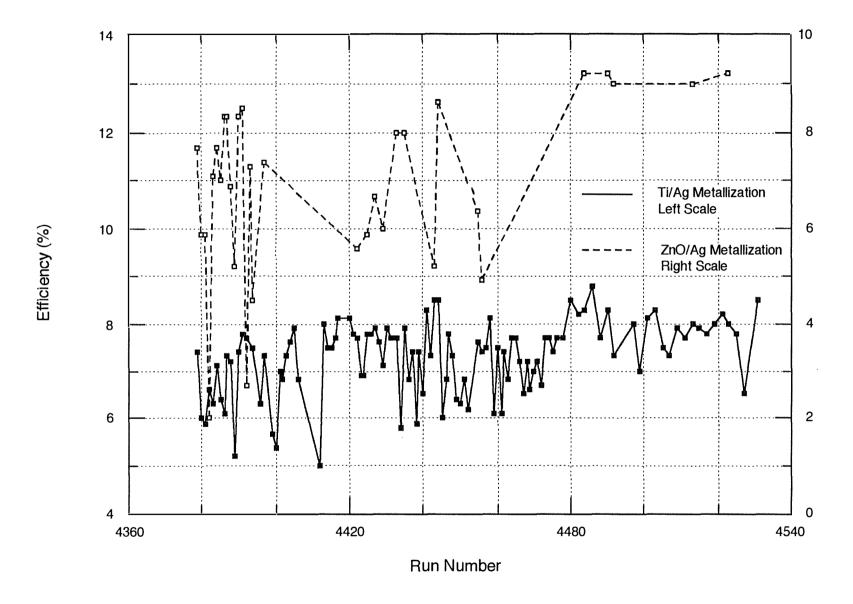


Figure 3.7. Efficiency as a function of run number.

Run 4382, where these parameters were used, resulted in a device (4382-21-2) efficiency of only 6.64%, substantially lower than the baseline. The other device parameters were:

$$V_{oc} = 0.743 \text{ V}$$

$$J_{sc} = 14.3 \text{ mA/cm}^2$$

$$R_{oc} = 6.7 \ \Omega \cdot cm^2$$

QE analysis of this device, shown in Fig 3.8. below, indicated that there was possible phosphorous contamination in the i-layer. This was inferred from the ratio of QE at 0 V to QE at +0.5 V, which is higher in the red than in the blue region of the spectrum. This observation was rather surprising since it meant that there is phosphorous carryover from the previous run's n-layer deposition, and that overnight high vacuum pumping did not completely remove phosphorous from the reactor.

In order to remedy this situation a large number of experiments were performed with different n-layer deposition parameters. These experiments were partially successful in that QE 0 V to +0.5 V ratios were found to be constant through the spectrum range of interest. However, FFs remained consistently at or below 70%, and R_{oc} values, in general, were 6 Ω ·cm² or higher.

At this point, it was decided to have one of the typical samples, 4432-11, analyzed by high sensitivity Secondary Ion Mass Spectrometry. Device #4432-22 from the same run showed a relatively flat QE 0 V to +0.5 V ratio, and had the following parameters:

$$V_{oc} = 0.820 \text{ V}$$

$$J_{sc} = 13.9 \text{ mA/cm}^2$$

$$FF = 67.0\%$$

$$Eff = 7.7\%$$

$$R_{oc} = 8.4 \Omega \cdot cm^2$$

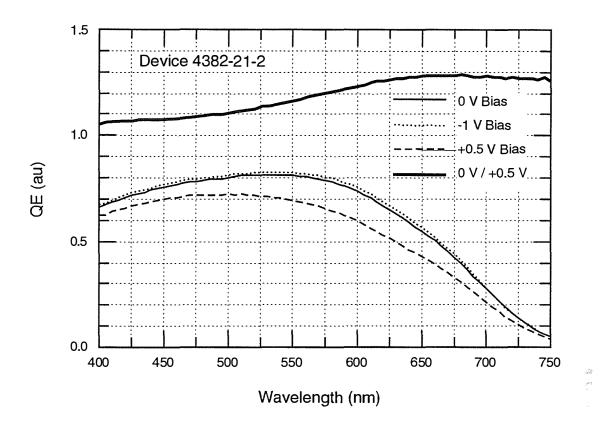


Figure 3.8. QE of device 4382-21-2.

Deposition parameters of run #4432 are given in Table 3.4, and the SIMS depth profiling is shown in Fig 3.9.

Table 3.4. Deposition parameters of run #4432.

Layer	р	buffer	i	n
Time (min:sec)	0:20	0:20	30:00	2:00
Pressure (T)	0.2	0.2	0.2	0.5
Temperature (°C)	150	150	175	175
RF Power (W)	20	20	. 7	10
SiH ₄ (sccm)	30	20	20	30
H ₂ (sccm)				
CH ₄ (sccm)	20	10		
2% B ₂ H ₆ in H ₂ (sccm)	2.5			
2% PH ₃ in H ₂ (sccm)				5

It is quite clear, from the SMS data, that substantial amounts of phosphorous exist in the p-layer. The only possible source of this phosphorous is the phosphorous doped film deposited on the electrode of the reactor. No amount of pumping or gas flow will be able to remove this film. The only possible solution is to deposit a "burying" layer before each run. Starting with run #4478, a 20 minute buffer layer was used as the burying layer between runs. As can be seen from Figure 3.6, FF of the devices show a sudden increase to above 70% starting with run #4478.

It is also observed, from Figure 3.6, that there is a substantial drop in FF in run #4499. This particular run had its i-layer diluted with 10 sccm H_2 , SiH₄ flow remaining at 20 sccm. Such a drop in FF could not be explained with the presence of H_2 gas during the deposition of the i-layer. As a result, both SiH₄ and H_2 lines, mass flow controllers, and valves were tested for leaks and analyzed by RGA. These tests showed that there was heavy water contamination in the H_2 cylinder and a small amount of water contamination in the SiH₄ lines. A new H_2 cylinder was installed and SiH₄ lines were cleaned. Note that the high level of oxygen contamination ($\approx 10^{19}$ cm⁻³) of the i-layer observed in the SIMS data of Figure 3.9 is consistent with the water contamination in the SiH₄ lines.

Removal of any trace of water contamination from the H_2 cylinder resulted in a substantial increase in the conductivity of the μc n-layers that were being used (see following section). The increase in conductivity was such that current collection outside the back contact metallization caused the FF to drop below 70% as can be seen in Figure 3.6 for run numbers around 4500. Reducing the thickness of the μc n-layer was found to be a temporary solution.

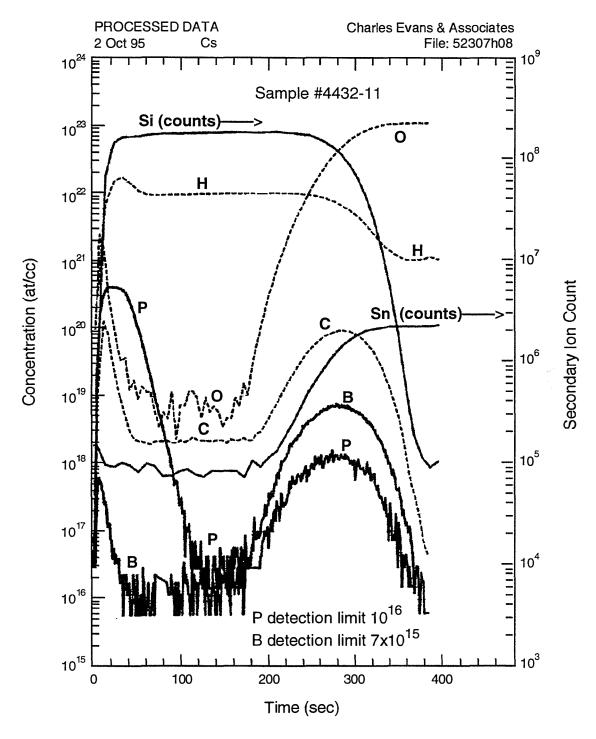


Figure 3.9. SIMS depth profiling of sample 4432-11.

Development of uc n-layers

It is reported that depositing a μc n-layer instead of an a-Si n-layer is critical for the tunnel junction of a multijunction device, and can increase V_{oc} as well due to the higher Fermi level position. Typically, μc material is obtained under conditions of high H_2 dilution and high rf power. A wide range of dilution (up to 100:1 ratio of H_2 : Si H_4 flow) and rf power (10 W to 50 W) were explored.

Highest quality μ c n-layer was obtained with the deposition parameters given in Table 3.4, and had the following properties:

$$E_g$$
 (@ $\alpha = 2000 \text{ cm}^{-1}$) = 1.9 eV
 $E_a = 0.05 \text{ eV}$
 $\sigma = 1 \text{ S/cm}$

Table 3.5. Deposition parameters of the μc n-layer of run #4432.

μс п
8:00
0.5
175
50
2
200
2

Deposition rate of this particular type of μc n-layer was found to be ≈ 0.5 Å/s, determined from the analysis of the SEM cross section micrograph (Fig 3.10) of a similar μc n-layer film deposited on SnO₂ for 40 min.

It should be pointed out that 8 minutes deposition time, giving a thickness of 240 Å, caused current collection outside the back contact metallization, lowering the FF as was pointed out in the previous section. Consequently, 6 minute μc n-layers (180 Å) were used for device optimization. Further studies are underway to remedy this situation.

 μ c n-layers had very little effect on the performance of devices having standard Ti/Ag back contacts. However, as discussed below, μ c n-layers were found to be crucial when using ZnO/Ag contacts.

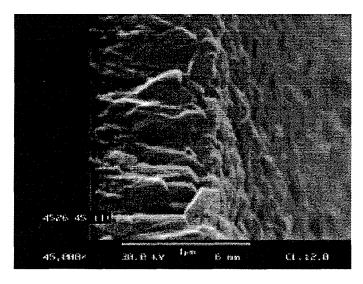


Figure 3.10. μc n-layer deposited on SnO₂; deposition time = 40 min. Magnification marker = 1 μm .

Back Contact Optimization

Three parameters of the Ti/Ag metallization were systematically varied: Ti thickness, system base pressure, and Ag deposition and rate. Post contact deposition heat treatments (HT) were also studied.

Devices were contacted without Ti, and with 25 and 50 Å Ti films (as measured by a quartz crystal monitor), followed by 5000\AA Ag. Devices without Ti had much higher initial J_{sc} due to the higher red QE based on the higher reflectivity of Ag. However, the J_{sc} of devices without Ti decreased significantly after HT, primarily due to a loss in the blue QE, suggesting that Ti acts as a diffusion barrier. Devices with 25 Å Ti had higher red QE but same FF (70-71%), as were devices with 50 Å Ti interlayer. Thus, 25 Å Ti followed by 5000\AA Ag became the standard back contact.

Reducing base pressure in the metallization bell jar from 1 to $3x10^{-6}$ T to $5x10^{-7}$ T before beginning the Ti deposition had no effect on initial or annealed values of FF. Since it required several hours of pumping to reach the lower pressure, metalization at low 10^{-6} base pressure range was continued.

Finally, increasing the Ag rate from 30 to 100 Å/s was found to have a beneficial effect on initial FF but made no difference after heat treatment. It is suspected that the higher electron beam power needed to achieve higher rate was heating the samples. Furthermore, devices with high rate Ag deposition showed very little improvement with HT, implying that the thermal treatment during metalization was to a certain extent equivalent to the post metal heat treatment. In any case, high rate Ag deposition was chosen as the standard process. However, it should be noted that none of the parameters which were varied during optimization (Ti thickness, system base pressure, or Ag deposition rate) had any measurable impact on final FF. The FF remained below the target value of 71%, which was obtained routinely last year with Ti/Ag, until the procedure of depositing a burying layer, as described above, was established.

It is well known that ITO/Ag or ZnO/Ag back contact metallizations give higher J_{sc} due to higher reflectivity compared to Ti/Ag or Al. However, as was reported in last year's report [3.1], although ITO/Ag or ZnO/Ag did improve J_{sc} by 1 to 2 mA/cm², the FF was at best 3 to 4 percentage points lower than with Ti/Ag. During the present reporting period, considerable effort was made to vary the ZnO conditions, the sputtering system vacuum cleanliness, and other process conditions. A new sputtering target was installed. However, only devices with μc n-layers, described above, gave higher FF when contacted with ZnO/Ag. This was further confirmed by sending IEC devices with amorphous and μc n-layers to Solarex for contacting with their ZnO/Ag process. In this case, as well, devices with μc n-layers had 5 to 10 percentage points higher FF than the ones with amorphous n-layers, though the highest FF in these devices was only 68%. The effort at IEC which focused on optimizing ZnO and μc n-layer deposition processes in tandem was successful in simultaneously achieving higher J_{sc} and FF. As a result, devices with ZnO/Ag contacts and μc n-layers had FF = 71 to 72% and increased J_{sc} of 15 to 16 mA/cm² due to higher red response: the QE at 700 nm increased from \approx 0.35 with Ti/Ag to \approx 0.55 with ZnO/Ag (Table 3.1).

3.2.4 Conclusion

Introducing deposition of burying layers between device runs, developing high conductivity, high transparency μc n-layer, and in conjunction with the latter, optimizing ZnO deposition process allowed the increases in J_{sc} and V_{oc} demanded by the program goals for the present reporting period.

3.3 Effects of Optical Enhancement Schemes on J_{SC} and Other Cell Parameters

3.3.1 Analysis Of Back Reflectors And Optical Enhancement For A-Si Solar Cells Using Textured Tco/Glass/Ag Substrates

Analyzing the optical enhancement in a-Si solar cells due to the back reflector (BR) is a challenging problem for both superstrate (glass/pin/BR) and substrate (SS/BR/nip) device structures. The BR increases the red QE and J_{sc} by reflecting and scattering weakly absorbed photons [3.2]. Despite considerable analysis, the BR enhancement and parasitic losses are not well understood [3.3]. We have used a novel device structure to separate the effects of substrate texture, BR texture, and BR reflection.

Experimental technique and device fabrication

Substrates consisted of glass with TCO layers having haze at 700 nm of 0, 1, 5 and 14%. a-Si devices with 0.25 μ m i-layers were deposited by glow discharge at ECD having a device structure: ITO/p-i-n/TCO/glass (Figure 3.11).

For comparison, devices were also deposited in the same run on stainless steel (SS) and ECD's standard textured ZnO/Ag BR [3.4]. After measurement of reflection (R), transmission (T), QE and JV for illumination through the ITO and the glass sides, a layer of Ag was evaporated on the rear of the glass. Alternatively, a smooth Ag BR (Ag coated glass) or textured Ag BR (Ag coated on the 14% haze SnO₂) was optically coupled to the glass substrate, giving a removable external Ag BR (Figure 3.11). This allowed measurements of three different BR (no Ag, smooth Ag, or textured Ag) on the same device sample. Enhanced QE with the optically coupled Ag BR was

equivalent to that found with the evaporated Ag film, indicating no additional losses due to the index matching liquid or external interfaces.

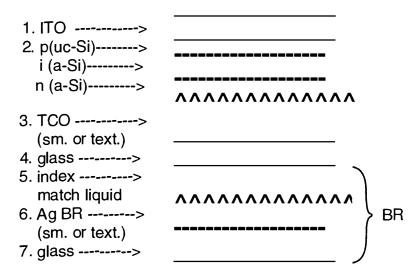


Figure 3.11. Device structure showing external Ag BR (layers 5, 6, 7).

Results

Figure 3.12 shows the QE (at -1V to eliminate collection losses) for light through the ITO/p contact for the four different substrates without any Ag BR. Note the large improvement in red QE as texture increases from 0 to 5%, but the negligible improvement above 5%.

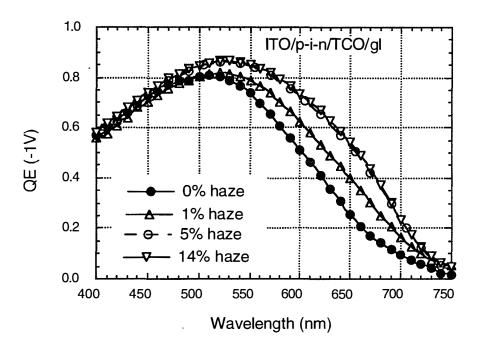


Figure 3.12. Devices on textured TCO / glass without Ag BR.

Table 3.6 lists the J_{sc} for the devices before and after the external smooth Ag BR, confirming the limited increase in J_{sc} for haze greater than ~5%. This same conclusion has been reached by others for <u>superstrate</u> devices [3.5]. QE beyond 650 nm through the glass side of the 5 and 14% haze devices was the same as QE through the ITO, indicating that optical enhancement by scattering weakly absorbed light is independent of the direction of the light. This means superstrate and substrate devices can achieve equivalent optical enhancement from a given textured substrate. ECD's ZnO/Ag BR gives slightly higher J_{sc} than the 14% textured TCO with Ag BR.

Table 3.6. J_{sc} (mA/cm²) for devices of Figure 3.12 without and with smooth external Ag BR. "ECD" refers to devices deposited on SS (no BR) and textured ZnO/Ag/SS (BR).

Haze(%)	J _{sc} without Ag BR	J _{sc} with external Ag BR
0	11.6	13.0
1	12.5	14.1
5	13.7	14.7
14	13.9	15.1
ECD	11.3 (SS)	15.5 (ZnO/Ag/SS)

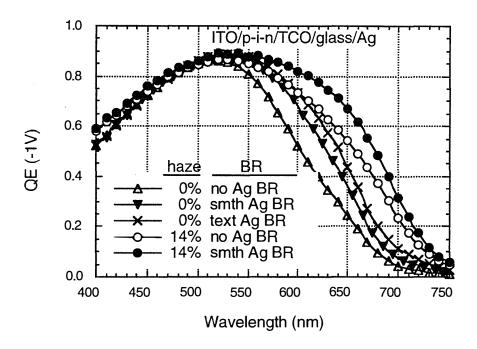


Figure 3.13. External Ag BR (none, smooth, textured) for devices on smooth (0% haze) and textured (14% haze) TCO / glass.

Figure 3.13 shows the QE at -1V with different external back reflectors for devices having the least (0%) and greatest (14%) haze. Since the BR were externally coupled, they only increase reflection but do not affect the a-Si surface texture, n/TCO interface, etc. This is a unique feature of these devices. The J_{sc} values, both absolute and normalized to the smooth TCO without a Ag BR (11.6 mA/cm2), and QE at 700 nm are given in Table 3.7.

Table 3.7. J_{sc} data for devices of Figure 3.13 (rel. J_{sc} is improvement relative to 0%, no Ag).

Haze	external BR	J _{sc} (mA/cm ²)	rel. J _{sc}	QE at 700 nm
0%	no Ag	11.6	1.00	0.05
0%	smooth Ag	13.0	1.12	0.07
0%	text Ag	13.3	1.15	0.11
14%	no Ag	13.9	1.20	0.22
14%	smooth Ag	15.1	1.30	0.32

These results show that a *textured* substrate with a *smooth* Ag BR has 15% higher J_{sc} than a *textured* Ag BR on a *smooth* device (15.1 vs 13.3 mA/cm²). The red QE is tripled for the textured substrate (0.11 vs 0.32). Thus, a textured substrate, even though transparent, is much more effective at light trapping than a textured Ag BR on a smooth device. This suggests that the replication of the substrate texture on the top a-Si surface is crucial to enhance multiple scattering from the underlying substrate, which is supported by the identical red response for textured cells

when illuminated through the ITO or the glass. This has direct consequences for designs which propose the use of smooth substrates with external texture to allow thinner, more stable a-Si devices without shunting problems [3.6]. Such designs will have inefficient light trapping and reduced J_{SC} compared to a device on a textured substrate, independent of whether they are a superstrate or substrate configuration.

Applying the external BR increases the red QE, but it also increases the reflection of red light escaping the front surface due to incomplete internal reflection. With the present devices, we can compare QE+T+R before and after applying the Ag BR. T is zero after applying the opaque Ag BR. Since QE+T+R accounts for all photons leaving the device as either light or electrons, the difference between unity and QE+T+R is parasitic absorption. Below 550 nm, this is due to the player and ITO absorption.

Figure 3.14 shows T, R and QE+T+R for the device with 14% haze. At 700 nm, adding a smooth Ag BR increases QE from 0.22 to 0.32, but also increases parasitic losses from 0.42 to 0.49. This is probably due to small losses accumulating over multiple (3-10) passes. For example, on each pass the Ag BR and glass absorbs 3-5%, n-layer absorbs 1%, and textured TCO absorbs 5%. The R spectrum of the ECD ZnO/Ag BR device was higher in the red and had interference effects while devices on the 8 and 14% haze textured TCO substrates did not. Thus, the textured TCO gives more complete trapping and randomization of the back scattered light, but it still has lower QE and J_{sc}. Reasons for this are under study.

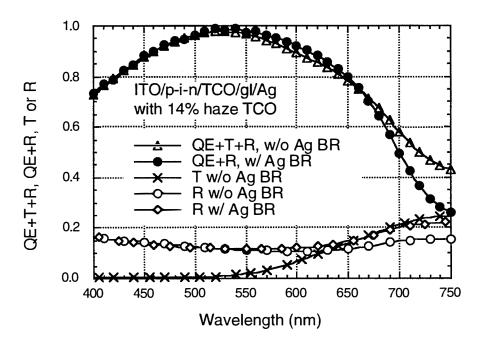


Figure 3.14. QE+T+R, T, and R on textured TCO/glass with and without smooth Ag BR (14% haze).

Conclusion

In conclusion, the effect of substrate texture and reflectivity on optical enhancement has been analyzed and separated in devices with a range of substrate texture. A transparent but well textured substrate is much more effective at increasing red response than a smooth substrate with external textured Ag BR.

3.3.2 Effect Of Textured Tin Oxide And Zinc Oxide Substrates On The Current Generation In Amorphous Silicon Solar Cells

It is commonly assumed that for superstrate amorphous silicon (a-Si) solar cells or modules of glass/transparent conducting oxide, (TCO)/p-i-n/rear contact type, to achieve high efficiencies, the TCO must have a low sheet resistance (< 15 Ω /sq), a low absorption in the visible (< 5%), and a sufficient texture to scatter light (> 5% haze). It is also required that the TCO be stable in the glow discharge environment of the a-Si deposition process. The front TCO electrode commonly used in superstrate a-Si devices is textured SnO₂:F deposited by APCVD. Recently, ZnO:F deposited by APCVD and ZnO:B deposited by LPCVD have been reported to be more transparent and more stable in the glow discharge environment [3.7], but to have less than ideal electrical contact with the p-type a-SiC:H.

The effect of a number of textured SnO_2 and ZnO substrates on the current generation in a-Si solar cells was evaluated. This work is of relevance since most of these TCOs have been used by others for a-Si device research or module fabrication. Secondarily, some qualitative observations will also be made on the relative quality of the electrical contact between the TCOs investigated and the a-Si p-layers.

Experimental Approach

Four SnO₂ films (labeled A, B, C, D) and three ZnO films (labeled E, F, G) were chosen for the present study. Most samples were obtained from commercial TCO vendors or a-Si industrial sources. These films were fully characterized as to their physical, electrical and optical properties. Surface topographies and thicknesses were determined by Scanning Electron Microscopy. Film thicknesses obtained by profilometric methods were in good agreement. Resistivities, carrier densities and mobilities were measured by four point probe and Hall effect methods by Prof. Gordon's group at Harvard. Optical properties were measured by the index matching liquid [3.7] method in a spectrophotometer fitted with an integrating sphere. The TCO absorption was corrected for absorption in the glass and in the index matching fluid. TCO (D) is the only one on soda-lime glass, all other TCOs are on low iron soda-lime glass.

a-Si p-i-n devices were deposited in IEC's PECVD system keeping all deposition parameters constant. Prior to each deposition, TCO substrates were baked under vacuum for 1 hour at 225°C. The device structure chosen for the present study was 200 Å a-SiC:H(B) p-layer / 3500 Å a-Si:H i-layer / 500 Å a-Si:H(P) n-layer. The p-layer bandgap was about 1.96 eV. It should be pointed out that these conditions do not give the highest cell efficiencies but permit more reliable analysis of the device optics. For example, the present p-layer thickness of 200 Å results in lower than optimum J_{sc} but removes uncertainties associated with incomplete coverage of, and high-field effects in, the highly textured TCOs. Devices were deposited on four substrates per run, one of which was always a SnO₂ substrate of type (A) as a control to verify reactor repeatability. Four devices were made on each substrate by the e-beam deposition of four 0.4 cm² Ti (25 Å)/

Ag (5000 Å) contacts. All the devices were characterized by I-V measurements under an AM1.5 Oriel simulator calibrated to 100 mW/cm², and by quantum efficiency measurements at -1 V bias.

Results and Discussion

Table 3.8 below gives the list of the TCOs used in the present study along with their respective deposition methods and physical characteristics. Table 3.9 gives their electrical and optical characteristics.

Table 3.8. List of TCOs and their physical characteristics.

TCO	Material	Deposition	Thickness	Surface Topography			
Label		Process	(µm)	Feature Size (µm)	Feature Shape		
A	SnO ₂ :F	APCVD	1.2	0.6	Angular grains		
В	SnO ₂ :F	APCVD	0.8	0.6	Well formed faceted angular grains		
С	SnO ₂ :F	APCVD	0.7	0.3	Bi-modal size, some well formed grains		
D	SnO ₂ :F	APCVD	0.4	0.2	Small grains, some rounded, some well formed		
Е	ZnO:B	LPCVD	1.5	0.4	Angular grains		
F	ZnO:B	LPCVD	1.6	0.5	Well formed faceted angular grains		
G	ZnO:F	APCVD	1.2	0.3	Small rounded grains		

Table 3.9. Electrical and optical characteristics of the TCOs.

TCO Label	$R_{sh} \ (\Omega/sq)$	$\rho \\ (\Omega.cm)$	μ_{H} (cm ² /V.s)	n (cm ⁻³)	Haze @ 700nm (%)	Absorp. @ 550 nm (%)
A	16	2.0x10 ⁻³	18	1.7x10 ²⁰	14	5.6
В	10	1.0x10 ⁻³	38	1.6x10 ²⁰	7	4.8
С	10	6.0x10 ⁻⁴	32	$3.0x10^{20}$	2	5.4
D	30	1.3x10 ⁻³	20	$2.4x10^{20}$	1	2.2
Е	11	2.0x10 ⁻³	19	$1.7x10^{20}$	5	3.3
F	10	1.6x10 ⁻³	25	1.6x10 ²⁰	5	3.8
G	13	1.6x10 ⁻³	20	1.2x10 ²⁰	6	3.3

SEM micrographs of the TCOs are shown in Figure 3.15 A-G. Two observations could be made which are relevant to device results. First, SnO₂ films (A) and (B) have similar feature sizes, but B appears to have faceted grains with larger peak-to-valley height, despite having lower haze.

Second, ZnO films (G), in contrast to (E) and (F) have small, blunt and rounded grains. Note that the two LPCVD ZnO films (E) and (F) have nearly identical physical, electrical, and optical properties despite being made by different groups.

The haze values shown in Table 3.9 were calculated from the ratio of diffuse to total transmission. The ZnO films have lower absorption losses than the SnO₂ films at comparable sheet resistance.

Table 3.10 gives the cell results and the QE data for devices made with TCOs analyzed above. The cell results shown on this table are for information only and do not correspond, as stated earlier, to results which might be expected by optimizing for a given TCO. Trends in these results are representative of other device runs made on these TCOs.

Table 3.10. Cell results, QE(-1V), and integral of QE (-1V) over AM1.5 global on various TCOs. The first four pieces were deposited in one run, and the second four in another run.

a-Si	TCO	V_{∞}	J_{sc}	FF	Eff.		E (-1V)	@	JQE(-1V)
run #	Label	(V)	(mA/cm ²)	(%)	(%)	450 nm	550 nm	700 nm	(mA/cm ²)
4511	A (SnO ₂ :F)	0.813	13.1	72.5	7.7	0.68	0.82	0.29	13.6
4511	B (SnO ₂ :F)	0.787	13.2	73.4	7.6	0.69	0.81	0.29	13.6
4511	C (SnO _{2:} F)	0.810	12.3	72.6	7.3	0.65	0.79	0.27	12.8
4511	D (SnO ₂ :F)	0.804	12.6	68.4	7.0	0.65	0.80	0.25	13.0
4507	A (SnO ₂ :F)	0.795	12.8	71.5	7.3	0.70	0.82	0.28	13.5
4507	E (ZnO:B)	0.746	13.5	67.0	6.7	0.73	0.86	0.30	14.1
4507	F (ZnO:B)	0.803	13.4	54.8	5.9	0.73	0.86	0.30	14.2
4507	G (ZnO:F)	0.718	11.5	62.7	5.2	0.62	0.80	0.29	13.2

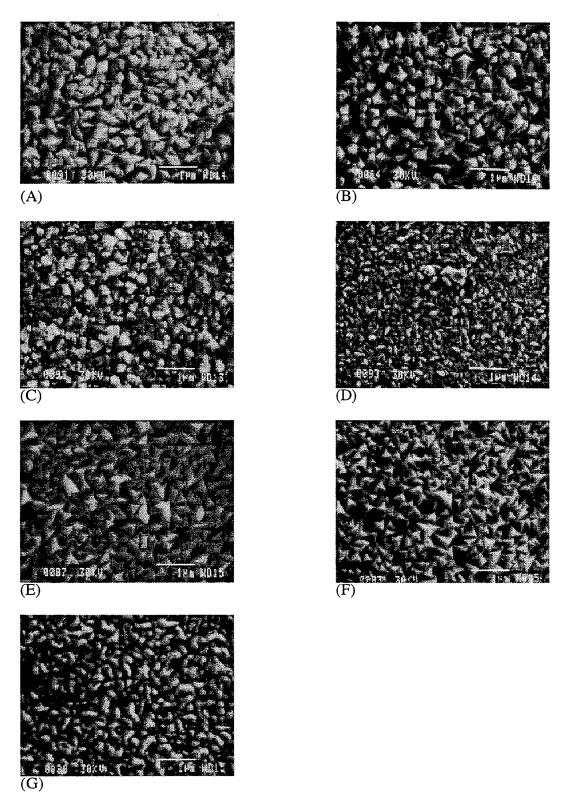


Figure 3.15. SEM micrographs of the TCOs studied in this section. Magnification marker = 1 $\mu\text{m}.$

In general, the high FF (at least on the SnO_2 devices) indicates a high quality a-Si i-layer and interfaces. First, comparing the SnO_2 pieces A, B, C and D, note that increasing haze from 1 to 14% had a relatively minor influence on J_{sc} . The QE at 700 nm, which is most strongly influenced by increased scattering, increases only from 0.25 to 0.29. The effect of haze on the QE is related to the reflection. Devices on low haze TCO (D) have strong interference effects leading to higher reflection losses at 450 and 700 nm. Second, TCO (C) has a lower J_{sc} and QE at all wavelengths because it is the only TCO on standard soda lime glass, and therefore has higher absorption losses. Third, low haze TCO (D) has lower FF which may due to higher R_{sh} (Table 3.9). Finally, TCO (B) always has significantly lower V_{oc} but slightly higher FF than the other SnO_2 pieces. As mentioned above, TCO (B) had surface features with greater peak-to-valley heights than the other TCOs. It also exhibited unstable JV behavior in reverse bias, suggesting a texture-related shunting mechanism which may affect devices on TCO (B).

Regarding the ZnO, the lower FF for TCO F and G is related to series resistance effects and does not adversely affect current generation at -1V. Comparing the best devices on ZnO (TCO E, F) to the best devices on SnO₂ (TCO A, B), the gain in current generation (integrated QE) with ZnO is about 0.6 mA/cm², as expected based on calculations. The lower V_{oc} and FF for ZnO are also consistent with reports from others which is attributed to contact resistance at the ZnO/p interface.

Conclusion

In conclusion, these results show that increasing haze in superstrate textured TCO/pin/metal above $\approx 5\%$ has negligible effectiveness for increasing the generation at long wavelengths. This is the same conclusion reached in the previous section on substrate textured TCO/nip/ITO devices. In presently available textured ZnO, current generation is about 0.6 mA/cm² greater than in textured SnO₂, but this is dependent on i-layer thickness.

3.4 Quantitative Updates for Device Team Storyboards

3.4.1 Analysis Of Multijunction Devices

Much of the modeling and analysis of multijunction devices has been achieved with numerical models requiring a large number of material and physical parameters. Although such modeling provides detailed insight into the microscopic behavior of single and multijunction devices, many of the required material parameters are experimentally inaccessible and the physics of some regions such as interfaces are imperfectly known. Thus, it is difficult to link the model to measurable device performance. We have previously presented [3.8] a method to analyze experimental a-Si JV curves in light and dark to obtain 5 parameters characterizing the illuminated junction. A sixth parameter, the ratio of collection length to thickness at zero volts bias, or $Lc/D=\mu\tau(Vb)/D^2$, is fitted. This parameter represents the field dependent collection. During the present contract year, excellent agreement has been found between this simple lumped circuit model and measured JV curves for a much wider range of single junction devices and conditions than presented in Reference 3.8, including p-i-n and n-i-p cells on smooth or textured substrates, a-Si and a-SiGe cells, initial and stabilized, and under AM1.5 and red filtered light. Devices provided by Solarex, USSC, and ECD were analyzed in addition to those from IEC and APS described in Reference 3.8. Some of this data is presented here, followed by analysis of triple junction cells using a parameter set based on the stabilized high, middle and low bandgap cells from USSC.

The light-generated photocurrent is analyzed by applying the model of Crandall [3.9] which assumes a uniform field F and uniform generation. It is also assumed that the forward bias diode current is independent of light intensity. Then, the net (measured) current through the device is the difference between the dark and light currents,

$$J(V) = J_{D}(V) - J_{I}(V). \tag{3.1}$$

 $J_D(V)$ is the forward bias diode current and $J_L(V)$ is the photocurrent. The diode current is given by the standard expression

$$J_{D}(V) = J_{o} \left[\exp(qV_{j}/AkT) - 1 \right]$$
(3.2)

where the junction voltage V_i is

$$V_{i} = V - (J*R). \tag{3.3}$$

Experimental methods of determining series resistance R, diode factor A, and recombination current J_0 from dark JV data are given in Reference 3.8.

The photocurrent $J_L(V)$ in a-Si solar cells decreases with increasing bias because of the reduction in the internal electric field. The field is assumed to vary as

$$F = \left(V_b - V_i\right) / D. \tag{3.4}$$

The field goes to 0 when the junction voltage V_j equals the flat band voltage V_b . Experimentally, V_b is the voltage at which $J_L(V) = J_D(V) - J(V) = 0$. In comparison, V_{oc} is the voltage at which J(V) = 0.

Crandall [3.9] derived an expression for $J_L(V)$ as

$$J_{L}(V) = J_{L_{0}} *X*[1 - \exp(-1/X)]$$
(3.5)

where J_{L_0} is the maximum (optically limited) photocurrent at far reverse bias, X is

$$X = (L_c/D) * [1 - (V/V_B)]$$
(3.6)

and

$$L_{c}/D = (\mu \tau * V_{b})/D^{2}. \tag{3.7}$$

Since this is a lumped circuit model, there is no calculation of photocurrent based on i-layer absorption, thickness and spectra. Optically limited photocurrent is represented by the value J_{L_0} .

Experimentally, the photocurrent $J_L(V)$ was obtained by subtracting the diode current $J_D(V)$ in the dark from the measured current J(V) under illumination as per Equation 3.1. The remainder was fit using Equation 3.5. The parameters L_c/D and V_b were varied until an optimum fit was obtained. The V_b value which resulted was always within 10 mV of the value determined experimentally. Thus, L_c/D is the primary fitting parameter.

Figure 3.16 shows the measured and calculated JV data under AM1.5 illumination for the a-Si top cell of a triple junction and Figure 3.17 the measured and calculated JV data under red filtered light for a low bandgap a-SiGe bottom cell of a triple junction both made by USSC.

Both Figures 3.16 and 3.17 show the initial and stabilized JV curves. The good agreement of Figures 3.16 and 3.17 from reverse bias to beyond V_{oc} indicate the model accurately represents all portions of the JV characteristic. Agreement is typically within 0.4 mA/cm². Parameters obtained from analyzing the top, middle, and bottom cell JV curves provided by USSC are in Table 3.11.

These devices and their testing and light soaking are described in more detail in Reference 3.10. The parameters in Table 3.11 will form the basis for subsequent analysis of triple junction cells. Table 3.12 shows the illuminated JV performance for each component cell calculated with parameters of Table 3.11 compared to the JV performance measured by USSC under appropriate illumination [3.10]. Very close agreement is found, demonstrating the applicability of this analysis to a-Si and a-SiGe devices under a range of conditions.

A triple junction device can be analyzed by solving Equation 3.1 for each junction with the requirement that the net currents J(V) are equal. Table 3.13 lists the performance of the triple junction devices consisting of the component cells of Table 3.11 in the initial and stabilized states. The efficiency decreases from 11.5 to 9.8% with light soaking (efficiency calculated assuming 100 mW/cm² input). Performance of USSC triple junctions [3.11] from this period are very comparable to the calculated values, with initial efficiencies of 11% and stabilized efficiencies of 9.5%.

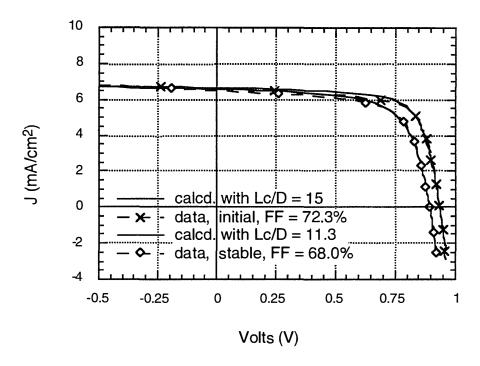


Figure 3.16. Measured (AM1.5) and calculated JV curve for USSC top cell (aSi) in initial and stabilized state. Calculated curves using parameters of Table 3.11, measured and calculated performance in Table 3.12.

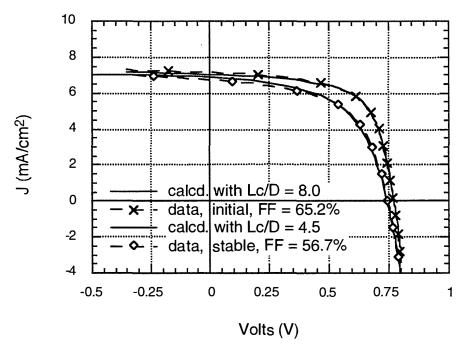


Figure 3.17. Measured (red filtered AM1.5) and calculated JV curve for USSC middle cell (a-SiGe) in initial and stabilized state. Calculated curves using parameters of Table 3.11, measured and calculated performance in Table 3.12.

Table 3.11. Parameters obtained from JV fitting and calculated and measured solar cell performance for initial and stabilized USSC component cells. Top cell degraded and measured under unfiltered light; middle, bottom cells degraded and measured under filtered light (see Ref. 3.10).

cell	state	Α	$J_0 (\text{mA/cm}^2)$	R (Ω·cm ²)	J_{L_0} (mA/cm ²)	L _c /D	$V_{b}(V)$
top	initial	1.67	2x10 ⁻⁹	2.5	6.9	15	1.03
	stable	1.75	1x10 ⁻⁸	3.6	6.9	11.3	0.92
mid	initial	1.54	2x10 ⁻⁸	3.4	7.5	8.2	0.86
	stable	1.93	1x10 ⁻⁶	4.6	7.5	4.5	0.83
bot	initial	1.66	1x10 ⁻⁶	3.3	9.2	5.3	0.89
	stable	1.88	6x10 ⁻⁶	4.1	9.2	4.8	0.73

Table 3.12. Calculated and measured performance of USSC component cells. Calculated values obtained with the 6 parameters from Table 3.11.

			Calcula	ated		Measured			
cell	state	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)	V _∞ (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)
top	initial	0.93	6.67	72.3	4.51	0.94	6.58	72.3	4.44
	stable	0.89	6.59	67.0	3.95	0.89	6.50	68.0	3.95
mid	initial	0.77	7.05	66.1	3.59	0.77	7.15	65.2	3.59
	stable	0.75	6.80	57.0	2.90	0.74	6.86	56.7	2.89
bot	initial	0.68	8.35	64.5	3.65	0.68	8.55	63.2	3.65
	stable	0.66	8.27	57.5	3.13	0.66	8.30	57.2	3.12

Table 3.13. Calculated triple junction performance for different cases of input parameters.

case	conditions	V_{∞}	J_{sc}	FF	Eff.
		(V)	(mA/cm ²)	(%)	(%)
1	initial cell parameters from Table 1.3.1	2.38	6.8	71.1	11.5
2	stabilized cell parameters from Table 1.3.1	2.28	6.7	63.6	9.8
3	same as case 2 except all L _c /D=15	2.34	6.8	71.8	11.4
4	same as case 2 except all V _b increased by 0.1V	2.35	6.7	66.4	10.4
5	same as case 2 except all J_0 decreased by $10X$	2.43	6.7	62.0	10.1
6	combine improvements from cases 3, 4, and 5	2.65	6.8	72.5	13.1
7	same as case 6 except increase all J_{L_0} to 8 mA/cm ²	2.65	7.7	69.3	14.2
8	same as case 6 with J_{L_0} current imbalance	2.66	7.9	71.0	14.9
	$top/mid/bot = 8/8.5/9 \text{ mA/cm}^2$				

The model can be used to indicate the relative payback for improving a given device parameter. Figure 3.18 shows the triple junction efficiency as a function of the L_c/D of the top, middle or bottom cell. All other cell parameters were the same as in the stabilized USSC component cells (see Table 3.11). Figure 3.18 shows that there is a significant improvement from increasing L_c/D up to 15 in the middle or bottom cells, but improvement saturates beyond this point. The most important conclusion of Figure 3.18 is that there is little benefit to significantly improving i-layer collection in one cell in the stack, for example, by greatly reducing the defect density or increasing mobility or lifetime. Instead, as discussed below, all properties of all devices must be improved. It is known empirically that improved a-Si multijunction cell performance results from having a current mismatch between component cells [3.12, 3.13]. The cell with highest FF (the top cell) is designed to have the lowest J_{sc} (i.e., it becomes the current limiting cell) and cells with the lowest FF are designed to have higher J_{sc} . Current mismatch has the biggest impact on the FF of the triple junction device. However, there has been little effort to understand the details or provide a predictive model of this effect.

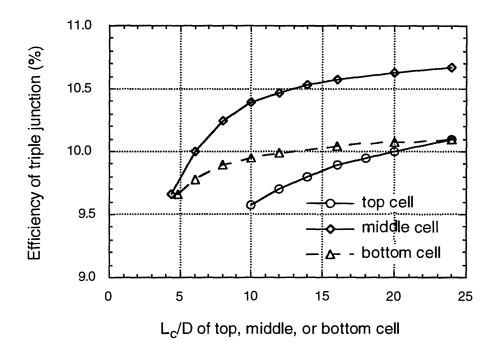


Figure 3.18. Efficiency of triple junction calculated for varying L_c/D of each component cell. Default values of L_c/D were 11.3, 4.5, and 4.8 for top, middle, and bottom cells. All other parameters from stabilized component cells of Table 3.11.

Figure 3.19 shows the effect of current limiting by varying the photocurrent J_{L_0} of the middle and bottom cells, independently. Other parameters are from Table 3.11 for the stabilized component devices. The efficiency continues to increase as either cell is increasingly imbalanced. The magnitude of the effect is similar to that found by USSC in their present triple junctions. The analytical model can thus be used to quantify how much one needs to increase the bottom cell current to obtain an expected increase. The trade-off comes from the inevitable decrease in bottom cell stability if its i-layer is made thicker, and loss in V_{oc} and FF if the i-layer bandgap is decreased.

Table 3.13 also shows the impact of selected improvements needed to achieve 15% using stabilized device parameters from Table 3.11 as a starting point. By improving the i-layer collection L_c/D to 15 (case 3) in all three cells, so that all three cells have i-layer quality comparable to the best initial a-Si device (Table 3.11), the triple junction FF only increases to 71.8% and efficiency increases to 12.6%. Note that V_{oc} increases by 0.06 V as the collection losses decrease because $J_L(V)$ remains larger at large forward bias. Case 4 shows that increasing the V_b of each cell by 0.1 V over the stabilized values increases the triple junction V_{oc} by only 0.07 V. Case 5 shows that reducing J_0 by an order of magnitude in each cell increases V_{oc} by 0.15 V, but efficiency increases by only 0.3 percentage points compared to case 2. Note that the FF actually decreases because V_{mp} is unaffected by J_0 while V_{oc} increases. This is proof that maximum power is almost unaffected by the dark diode, but rather is determined almost entirely by the bias dependent photocurrent collection (Equation 3.6). Case 6 combines all three major improvements of cases 3, 4, and 5, resulting in an improvement in V_{oc} of 0.37 V which is greater than the sum of gains in V_{oc} by changing each parameter individually. The FF increases only slightly (from 71.8% to 72.5%) compared with the value found by increasing only L_c/D to 15 in case 3. This confirms that L_c/D

has the dominant effect on FF. Increasing the flat band voltage or reducing J_0 of each device has a greater impact as L_c/D increases since the device becomes more ideal. It is well known that triple junction J_{sc} of 8 mA/cm² is needed to reach 15% efficiency [3.13]. Case 7 shows the performance when all improvements of case 6 are coupled with higher J_{L_0} of 8 mA/cm² for all three devices. Although J_{sc} increases as expected, FF decreases since the benefits of current mismatching are lost. Case 8 shows the benefit of current limiting with the best cell (top cell). The J_{L_0} values are 8, 8.5, and 9 mA/cm² in the three devices, resulting in no change in V_{oc} , small increase in J_{sc} , but a significant improvement in FF. This shows that current imbalance is an important technique to improve FF even when all three devices have identical and rather high values of L_c/D . Case 8 shows that to achieve 15% efficiency, it is necessary to increase L_c/D significantly in the middle and bottom cells, to increase V_b in all three cells by 0.1 V, to reduce J_0 by an order of magnitude in all three cells, increase J_{sc} to nearly 8 mA/cm², and incorporate current limiting with the top cell.

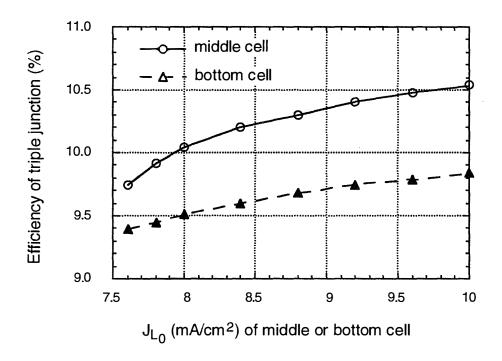


Figure 3.19. Effect of current mismatch on efficiency by varying JL_0 of middle and bottom cells. All other parameters from stabilized component cells of Table 3.11.

3.4.2 Conclusion

Since this analysis was begun, top cells with V_{oc} of 1.0 V have been reported and used in triple junctions. Also, the J_{sc} of the triple junctions has increased. Together, these improvements have lead to triple junction devices with stabilized efficiencies of 11.8% [3.14]. Parameters reflecting these improvements will be incorporated into the model in the current contract year, giving results typical of today's best triple junction devices. These will then be used to evaluate directions and device features needed to extrapolate to DOE's 15% efficiency goal.

References - Section 3

- 3.1 R. W. Birkmire, J. E. Phillips, W. A. Buchanan, S. S. Hegedus, B. E. McCandless, and W. N. Shafarman, *Annual Report to National Renewable Energy Laboratory*, under Subcontract No. XAV-3-13170-01, 1/16/94 to 1/15/95, (1995).
- 3.2 A. Banerjee and S. Guha, J. Appl. Phys. **69**, 1030 (1990).
- 3.3 A. Banerjee, K. Hoffman, X. Xu, J. Yang, and S. Guha, *Proc. 1st WCPVEC*, 539 (1994).
- 3.4 X. Deng, M. Izu, K. Narasimhan, and S. R. Ovshinsky, *Proc. MRS Symp.* **336**, 699 (1994).
- 3.5 R.E.I. Schropp et al, *Proc. 10th European PVSC*, 1087 (1991).
- 3.6 S. Fonash, *Private Communication*.
- 3.7 S.S. Hegedus, H. Liang, and R. Gordon, 1995 NREL PV Program Review, *AIP Conf. Proc.* **353**, 465 (1995).
- 3.8 S. Hegedus and J. E. Phillips, *Proc. 1st WCPVEC*, 654 (1994).
- 3.9 R. Crandall, J. Appl. Phys. **54**, 7176 (1983).
- 3.10 X. Xu, J. Yang and S. Guha, Proc. 23rd IEEE PV Spec. Conf., 971 (1993).
- 3.11 S. Guha et al, 12th NREL PV Program Review, AIP Conf. Proc. 306, 127 (1993).
- 3.12 R. Arya et al, Final Report for Subcontract ZM-0-19033-1 (NREL/TP-411-6841), (1994).
- 3.13 W. Luft et al., 12th NREL PV Program Review, AIP Conf. Proc. **306**, 31 (1993).
- 3.14 J. Yang, X. Xu, A. Banerjee, and S. Guha, *Proc. 25th IEEE PV Spec. Conf.*, to be published.

4.0 CdTe/CdS RESEARCH

4.0.1 Goal/Motivation Approach

Success in developing CdTe/CdS thin film solar cell processes which are compatible with low cost manufacture is contingent upon obtaining high conversion efficiency with an economically scalable process. To accomplish this, knowledge of the relationships between the processing conditions and the device performance are essential. The goal of the work at IEC has been to develop and understand these relationships and improve the device performance, relying on deposition and processing techniques that permit decoupling of the effects of individual processing parameters.

The CdTe/CdS device fabrication process at IEC is based on CdTe and CdS films deposited by physical vapor deposition (PVD). This deposition technique provides a thin film structure consisting of discreet CdS and CdTe films. The as-deposited films do not possess the properties needed to make high conversion efficiency devices. The research challenge lies in the requirement that a post-deposition treatment must render an essentially non-photovoltaic structure to a high efficiency device, simultaneously effecting significant changes to the chemistry, structure, and electronic properties of the CdTe and the CdS. Thus, the research focus has been on identifying and quantifying the effects of the post-deposition processing on the properties of the CdTe/CdS structures and linking these to the performance and limits of performance obtainable.

4.1 CdTe/CdS Device Performance

In this reporting period vapor phase CdCl₂ treatments were developed, permitting the effects of reaction temperature and chloride concentration on materials and devices to be investigated. Vapor CdCl₂ treatment at 420°C was found to result in uniform modification of the film properties. Combined with the contacting process developed in the previous reporting period, the uniform and reproducible treatments have translated into greater consistency in device performance at a baseline efficiency level of 10.5–12%. The devices in Table 4.1 illustrate the level of performance achieved this year with vapor processing of PVD films:

Table 4.1. J-V parameters of devices from 6 different runs processed with CdCl₂ vapor (using a coated plate as the vapor source).

V_{∞}	J_{sc}	FF	Eff	Sample
(mV)	(mA/	(%)	(%)	
	cm^2)			
809	21.4	60.8	10.5	40899.11-5
806	21.6	61.4	10.7	40907.23-3
792	20.8	64.8	10.7	40908.22-1
821	21.5	68.8	12.1	40920.11-4
825	21.8	68.0	12.2	40926.11-3
816	21.0	68.5	11.7	40927.21-3

The J-V curve of the best cell in Table 4.1 is shown in Figure 4.1. The V_{oc} is approaching state-of-the-art values, but J_{sc} and FF are low. The resistance at V_{oc} in these devices is in the range of 6 to 10 mohm-cm². Reducing this to 1–2 mohm-cm² by optimizing the CdTe doping and contact are expected to increase FF to >72% and should enhance the V_{oc} . Control over S interdiffusion with vapor treatment and use of alloyed films is described in the sections below and offers several avenues for improving J_{sc} : 1) use thick CdS (~250 nm) and high S diffusion process to thin down the CdS, boosting J_{sc} contributions from 300–550 nm and 750–900 nm; 2) use ultrathin CdS (<50

nm) and low S diffusion process to minimize loss of CdS film; and 3) deposit $CdTe_{1-x}S_X$ films with x near the solubility limit on ultrathin CdS to minimize driving force for interdiffusion.

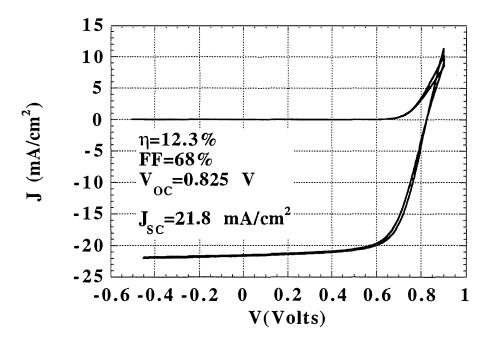


Figure 4.1. J-V curve of PVD CdTe/CdS device 40926.11-3 processed with CdCl₂ vapor (using a coated plate as the vapor source).

4.2 Chemical and Heat Treatment of CdTe and CdS

Three vapor treatment techniques were developed as alternatives to the standard (liquid application) post-deposition CdCl₂:methanol treatment: 1) CdCl₂ vapor treatment using a CdCl₂ coated plate as a vapor source; 2) CdCl₂ vapor treatment using powdered CdCl₂ in a confined reaction zone as a vapor source; and 3) HCl vapor treatment using HCl:Ar mixtures. The feasibility of both the CdCl₂ vapor and HCl approaches was demonstrated by earlier work at IEC [4.1, 4.2]. The CdCl₂ vapor treatment methods result in uniform grain growth, no detectable surface residue, and reproducible and uniform device performance. Method 1 was incorporated into IEC's standard processing and has been in routine use since March 1995, while methods 2 and 3 have been used to investigate a wide parameter space, taking advantage of the additional control over chloride species concentration that they offer.

4.2.1 CdCl₂ Vapor Treatment – Parallel Plate Configuration

Description

CdCl₂ vapor treatments were carried out by exposing the CdTe or CdS surface to CdCl₂ vapor generated from the surface of a Corning 7059 glass slide coated with CdCl₂ by application of 1% CdCl₂:methanol solution and drying. Source plates coated with 10 drops per inch (dpi), 5 dpi, and 0.5 dpi of solution were initially evaluated, producing coatings containing 130 μ g/cm², 65 μ g/cm², and 6.5 μ g/cm², respectively. The different quantities applied to the glass were expected to produce different (but unknown) vapor concentrations at the CdTe surface due to reaction between

CdCl₂ and the glass plate. Separation of CdTe and CdCl₂ was established by use of ~0.5 mm thick shims located at the edge of the samples onto which the CdCl₂-coated source plate was positioned. The sandwich was set in a milled aluminum palette which was inserted into a preheated furnace. Thermal equilibrium was reached after approximately 5 minutes. Heat treatments were carried out in the range known to be effective for the wet application method, from 410°C to 420°C for 10 to 20 minutes in the muffle furnace with room air ambient. In all cases, the CdS received a vapor heat treatment at 420°C with CdCl₂ prior to CdTe deposition. Unless noted, the CdTe and CdS film thicknesses used were 4.5 μ m and 0.2 μ m, respectively.

Materials Results and Analyses

Gravimetric analysis of the source plates used for 5 dpi cases showed a 25% reduction in mass after a 30 minute heat treatment, verifying that some CdCl₂ is lost via vapor transport during the treatment. Some of the mass loss is due to dehydration of the CdCl₂. No chloride uptake was detected on the samples, either by gravimetric analysis to a mass resolution of +/- 2 µg or by EDS analysis at 10, 20 and 30 kV of the CdTe surface after treatment. This observation points to the catalytic nature of the interaction between the CdCl₂ and the CdTe/CdS structure. The source plates became milky and textured after treatment. X-ray diffraction and SEM/EDS of the source plates after treatment and water rinsing revealed significant reaction of the CdCl₂ with the glass, resulting in diffraction patterns consistent with Cd₃Cl₂O₂ and possibly phases of aluminum chlorates.

The surface morphology and grain size distribution on the CdTe film surface were assessed by SEM area surveys for samples treated at 415°C for 15 minutes with different quantities of CdCl₂ on the source plate (Figure 4.2). Similar grain structure to that obtained by the wet application method was observed for the 5 dpi (65 μ g/cm²) and 10 dpi (130 μ g/cm²) cases. The 0.5 dpi (6.5 μ g/cm²) case did not exhibit the large grain structure, possibly due to the overlying morphology or due to little grain coalescence as a result of insufficient CdCl₂.

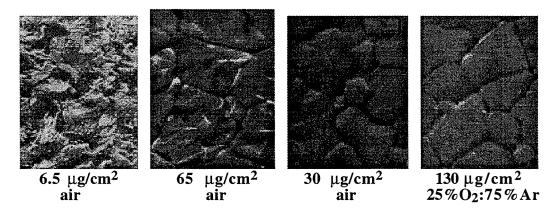


Figure 4.2. SEM photographs (5000X) of CdTe/CdS films from 40875 treated with CdCl₂ vapor at 415°C for 15 minutes in air and in 25% oxygen:75% argon with different amounts of CdCl₂ on the source plate.

X-ray diffraction patterns of the treated CdTe/CdS films were taken using Cu k_a radiation with a scanning diffractometer with Bragg-Bretano focusing geometry. The patterns were used to determine the normalized (111) orientation parameter, p(111), after the method of Harris [4.3] and the precision lattice parameter, a_0 , by extrapolation of a(hkl) versus the Nelson-Riley-Sinclair-Taylor function [4.4] of Bragg angle for each film. Results for vapor treated films are compared to

a film which was treated by the wet application method in Table 4.2. The normalized orientation parameter was determined using 7 reflections and is a quantitative measure of the degree of preferred orientation with respect to a single (hkl) plane. A value of 1 indicates random orientation, a value less than 1 indicates preferential texture of a different (hkl) than (111), and a value greater than 1 indicates preferred (111) orientation of grains with growth axis normal to the plane of the substrate. All treatments reduce preferred (111) texture, but vapor treatments with reduced CdCl₂ source concentration produce the highest degree of (111) orientation and lowest S content in the CdTe layer. The sample treated in a slightly enhanced and drier oxygen atmosphere exhibited enhanced interdiffusion and uniform grain size. The specific role of oxygen in controlling structural modification and in device performance needs to be explored further.

Table 4.2. X-ray diffraction results of CdTe/CdS films from 40875 treated by wet application method and vapor method at 415°C for 15 minutes. Pure CdTe has lattice parameter $a_0 = 6.481$ Å and orientation parameter, p(111) = 1. The sulfur content, [S]/([Te]+[S]), was determined from a_0 using Vegard's law.

Method	CdCl ₂	Atmosphere	Precision	[S]/	I(111)	p(111)	Sample ID
	Amount	-	Lattice	([Te]+[S])	(counts)		•
	on Source		Parameter				
	Plate or		(Å)	(%)			
	Sample		(+/-	(+/-			
	(μg/cm ²)		0.001Å)	0.2%)			
-	-	-	6.480	-	3264	4.0	as dep
wet	100	Air	6.475	0.9	937	0.3	212
vapor	130	Air	6.479	0.3	915	0.3	11
vapor	130	25%O ₂ :Ar	6.477	0.6	847	0.3	22
vapor	65	Air	6.479	0.3	1115	0.7	121
vapor	6.5	Air	6.479	0.3	2375	1.3	122

Device Results

Device results for the best device obtained on each piece of this group using the diffused Cu contacting process and graphite dot contacts with $\sim 0.1~\rm cm^2$ area are shown in Table 4.3. Normalized quantum efficiency (QE) curves in dark at zero volt bias for the sample treated with CdCl₂:methanol (wet) and vapor are shown in Figure 4.3.

Table 4.3. Device results for the samples of Table 1.

Method	CdCl ₂	Atmosphere	V_{∞}	J_{sc}	FF	Sample ID
	Amount		(mV)	(mA/cm ²)	(%)	_
	(μg/cm ²)			,		
wet	100	Air	765	21.5	57.8	212-4
vapor	130	Air	789	21.3	61.9	11-6
vapor	130	25%O ₂ :Ar	812	17.9	62.2	22-4
vapor	65	Air	801	19.8	64.6	121-2
vapor	6.5	Air	782	19.4	62.1	122-1

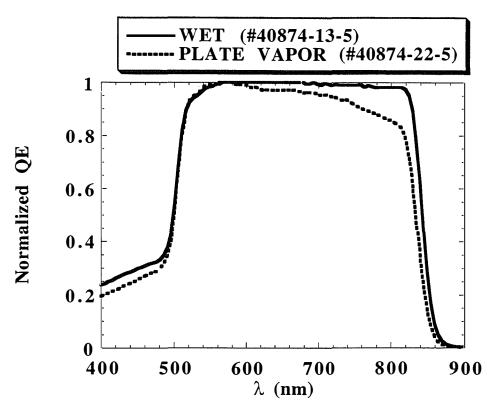


Figure 4.3. Normalized quantum efficiency curves of devices processed with CdCl₂:methanol (wet) and CdCl₂ vapor.

From a device performance perspective, very low source quantities of $CdCl_2$, delivered by vapor phase transport, can be employed to achieve results equal to or surpassing results obtained by the wet application method. The use of a dry ambient such as O_2 :Ar resulted in uniform grain coalescence, enhanced S diffusion, and higher V_{oc} compared to the sample treated in room air in this comparison of pieces deposited in the same CdTe deposition.

The procedure of sample 121, with 65 µg/cm² of CdCl₂ on the source plate, treated at 415°C for 15 minutes, was employed in subsequent device fabrication. Table 4.4 lists the J-V parameters of devices from fourteen different CdTe/CdS depositions runs processed using the vapor treatment in air.

Vapor CdCl₂ treatments with a parallel plate configuration have thus been shown to produce devices having comparable performance to those processed by the wet application method. The vapor treatment appears to reduce the extent of S diffusion into CdTe. However, the plate method still relies on obtaining a uniform coating across the source plate which can be difficult to control with the methanol application method. Further, while experiments with CdCl₂ quantity on the source plate suggest that only a sufficient amount of solid is needed to maintain a vapor-solid steady state, the method permits no decoupling of the reaction temperature from the CdCl₂ vapor concentration, which is determined by the CdCl₂ source plate temperature. Also, gravimetric and chemical analysis of the source plates shows that the CdCl₂ concentration varies spatially and temporally due to CdCl₂ transport out of the sides of the sandwich structure and due to reaction with the glass. This may be expected to adversely affect the uniformity of the CdTe/CdS properties and device operation across a sample. The degree of CdCl₂ loss due to mass transport and reaction may vary from treatment to treatment depending on the morphology and surface area of the CdCl₂ coating. To overcome these difficulties, a reactor with a confined reaction zone was

constructed in which conditions of CdCl₂ vapor phase equilibrium could be established independently of the reaction temperature.

Table 4.4. Device results for samples from different CdTe depositions processed using the vapor method described above.

V_{∞}	Jsc	FF	Sample ID
(mV)	(mA/cm ²)	(%)	-
816	21.0	68.5	40927.21-3
826	21.6	68.8	40926.11-3
821	21.5	68.8	40920.11-4
776	20.9	62.4	40919.23-2
779	20.5	62.6	40914.21-1
792	20.9	64.8	40908.22-1
806	21.6	61.4	40907.23-3
810	21.2	61.7	40906.23-3
781	21.8	63.4	40904.31-1
809	21.5	60.8	40899.11-5
798	18.7	67.9	40894.12-6
828	19.7	65.0	40892.31-1
801	19.8	64.6	40875.121-2
818	18.7	67.6	40738.322-2

4.2.2 CdCl₂ Vapor Treatment - Independent Thermal Control Configuration

Description

CdCl₂ vapor treatments were carried out in a reactor designed and constructed to permit independent control over the reaction temperature and the CdCl₂ source temperature, hence CdCl₂ vapor phase concentration at the CdTe surface. The effects CdCl₂ concentration, reaction temperature at fixed species concentrations, and thermal history on the degree of interdiffusion, grain coalescence, and device operation are presented. The reactor consists of a quartz tube fitted with vacuum-tight endcaps for pumping and purging capabilities with temperature controlled graphite susceptors heated externally by linear lamps made by Research, Incorporated. A graphite susceptor supported on a quartz frame with a milled central cavity holds the CdCl₂ source powder, which is pressed in tightly after dehydration to form a uniform and nominally flat surface. A mica mask acts as a separator and thermal insulator between the source susceptor and the thin film sample. A second graphite susceptor rests on top of the thin film sample to provide independent heating control.

In order to understand the behavior of the gases in the reaction zone, the mass and thermal diffusion characteristics were determined for the reactor geometry. The results of this modelling show that the characteristic times to reach thermal equilibrium in air at 1 atm and mass transfer equilibrium are less than 2 seconds for isothermal reactions (TCdTe=TCdCl2) with a 2 mm separation between sample and CdCl2 surface at 400°C, assuming no mass transport out of the reaction zone. Table 4.5 lists the CdCl2 equilibrium vapor phase concentration, number of collisions with CdTe surface per unit area per second, and the saturation pressure (5) for the temperatures listed in the reaction zone.

Table 4.5. CdCl₂ vapor phase heat treatment reactor equilibrium conditions for isothermal reactions.

CdCl ₂ T (°C)	[CdCl ₂] at CdTe (mol/cm ³)	Wall Collisions N (coll/cm ² /s)	P _{sat} (mtorr)
380	3.25E-11	1.35E+17	1.34
410	1.33E-10	5.62E+17	5.73
420	2.06E-10	8.79E+17	9.03
430	3.16E-10	1.36E+17	14.04
450	7.15E-10	3.11E+18	32.66

Using a CdTe/CdS/ITO/glass sample with an embedded microthermocouple, the time needed to heat the sample to 400° C was measured to be 40 seconds. The time to heat the CdCl₂ susceptor to 400° C was measured to be 20 seconds. Thus, the heat-up rate of the susceptors, not the characteristic diffusion times (~2 sec), controls the time to reach equilibrium conditions in the reaction zone. Gravimetric analysis of the source susceptor with CdCl₂ after heating in air at 400° C for up to 300 minutes in the reaction configuration yielded a negligible mass loss. No discoloration was observed on the quartz tube indicating no evolution and condensation of CdCl₂ to the reactor chamber. These measurements indicate that the susceptor geometry allows sufficient confinement of the CdCl₂ to the reaction zone for the assumptions of the modelling to be valid.

The temperature difference between the source and a bare 7059 sample with no cover susceptor was determined to be approximately 100°C at a CdCl_2 source temperature of 400°C . This temperature difference is sufficient to permit CdCl_2 deposition onto glass substrates for evaluation of the effects of conditions, such as atmosphere composition, on mass transfer. With the top susceptor in place, the temperature difference is approximately 85°C , which establishes the maximum difference that can be maintained for separating reaction temperature from CdCl_2 concentration. Three CdCl_2 deposition trials were performed for a CdCl_2 set point of 420°C and yielded an average transport rate of $4.6~\mu\text{g/min} + 1~\mu\text{g/min}$. The model for the 420°C source temperature, 2 mm separation, and 100°C temperature difference yielded a rate of $5.6~\mu\text{g/min}$, which agrees with the data within the experimental error. This result provides a check on the assumption that the CdCl_2 powder reaches the susceptor set point temperature.

Preliminary evaluation of the effects of $CdCl_2$ vapor phase concentration and reaction temperature were made by independently controlling the temperatures of the thin film (T_1) and the $CdCl_2$ (T_2) : 1) $T_1 > T_2$; 2) $T_1 = T_2$; 3) $T_1 < T_2$. Two types of heating profiles were employed: unison heating to simulate the conditions of $CdCl_2$ -coated samples and delayed heating to allow the CdTe/CdS sample to reach thermal equilibrium before the $CdCl_2$. To prevent $CdCl_2$ condensation on the CdTe/CdS in cases 1 and 2 due to mismatched heating rates, the CdTe/CdS was heated prior to and cooled after the $CdCl_2$.

Materials Results and Analyses

Grain coalescence and S diffusion were assessed by microscopy and x-ray diffraction, respectively, as described in the previous section. Devices were also completed in the same way as described above. Isothermal treatments with delayed heating at 380°C, 410°C, 420°C and 430°C show increasing grain size with temperature (Figure 4.4) as has been observed for the wet process, the ampoule vapor treatment, and the plate vapor treatment.

Fixing the CdCl₂ concentration and increasing the reaction temperature from 380°C to 450°C resulted in progressive grain growth at 380°C–420°C but produced a two layer structure with

underlying grains that are of comparable dimension to those found with the isothermal case at 420°C (Figure 4.5a-c). Fixing the reaction temperature at 420°C but increasing the CdCl₂ concentration (Figure 4.5d) produced similar grain size to that obtained under isothermal conditions at 420°C but, as expected, the surface was coated with dendritic clusters of CdCl₂ which rinsed away in methanol. The reaction parameters, average grain size and x-ray diffraction results for these cases are summarized in Table 4.6 below, which is presented in groups according to type of treatment.

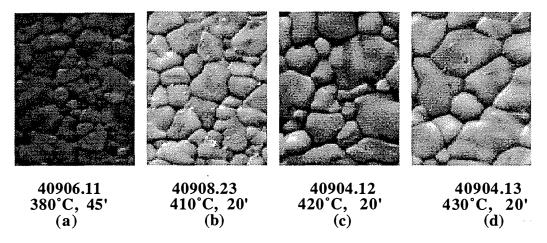


Figure 4.4. CdTe surface SEM photographs (5000X) after isothermal CdCl₂ vapor heat treatments with delayed heating of CdCl₂.

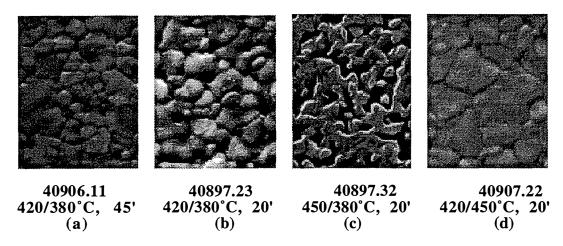


Figure 4.5. CdTe surface SEM photographs (5000X) after isothermal $CdCl_2$ vapor heat treatments at different $CdTe/CdCl_2$ temperatures, with delayed heating of $CdCl_2$.

Table 4.6. Treatment conditions, average grain size (AGS), and x-ray diffraction results for 4.5 μ m CdTe/CdS films before and after processing by CdCl₂ vapor treatment under the conditions shown. All samples were processed with delayed heating except 40601.32 in which CdTe and CdCl₂ were heated in unison.

T	T	Time	P _{sat}	AGS	Precision	[S]/	I(111)	p(111)	Sample
(CdTe)	(CdCl ₂)	(min)	$(CdCl_2)$	(µm)	Lattice	([Te]+[S])	(counts)	_	_
(°C)	(°C)		(mtorr)		Parameter				
					(Å)	(%)			
					(+/-。	(+/- 0.2%)			
					0.001Å)				
-	-	-	-	0.6	6.485	0	2300	3.4	as dep
	200		4.0	0.0		0.4	45.45		4000644
380	380	45	1.3	0.9	6.480	0.1	4747	1.2	40906.11
410	410	20	5.7	1.5	6.479	0.3	3736	0.6	40908.23
420	420	20	9.0	2.1	6.477	0.6	3427	1.0	40904.12
420	420	20	9.0	1.7	6.477	0.6	2816	0.8	40897.21
430	430	20	14.0	2.3	6.477	0.6	3666	1.2	40904.13
200	200	ا ہما	1.0	0.0	6 400	0.1	45.45	1.0	4000611
380	380	45	1.3	0.9	6.480	0.1	4747	1.2	40906.11
420	380	20	1.3	1.2	6.477	0.6	2415	1.1	40897.23
420	380	45	1.3	1.2	6.477	0.6	2365	1.1	40907.32
450	380	20	1.3	2.0	6.478	0.5	2709	0.9	40897.32
400	200		1.0	1.0	C 477	0.6	0.415	1. 1	40007.00
420	380	20	1.3	1.2	6.477	0.6	2415	1.1	40897.23
420	420	20	9.0	2.1	6.477	0.6	3427	1.0	40904.12
420	450	20	32.7	1.7	6.476	0.8	7782	2.6	40907.22
420	420	20	9.0	1 1	6.481	0.0	4196	2.9	40601.31
420	420	20		1.1					40601.31
420	420	20	9.0	2.0	6.446	5.3	3598	2.9	40001.32

In Table 4.6, the grain size increases with isothermal treatment conditions, as observed using the methanol application method. Decoupling the CdCl₂ temperature from the reaction temperature shows that reaction temperature has a strong effect in controlling the grain growth, and the two treatment times used for 420/380°C demonstrates that the grain growth is not kinetically limited in the time spans examined. S diffusion into CdTe, evidenced by the bulk lattice parameter, is constant for fixed CdCl₂ concentration at reaction temperature above 380°C and increases slightly by increasing the CdCl₂ concentration. In general, recrystallization reduced the (111) preferred orientation from the as-deposited condition. Comparing to Table 4.1, it is shown that reactor treated films have greater (111) texture than CdCl₂:methanol treated films. No other consistent trend is observed.

Repeating the isothermal case at 420°C but varying the thermal heat-up history of the CdTe/CdS film and the CdCl₂ source produced distinct differences in the final structure. Unison heating of the CdTe/CdS and CdCl₂ promoted a flat morphology with uniform grain size (Figure 4.6). The x-ray diffraction results of these films (Table 4.6) shows extensive diffusion of S into the CdTe compared to all of the delayed heating reactions.



40601.31 Delayed CdCl₂ Heating



40601.32 Unison Heating

Figure 4.6. CdTe surface SEM photographs (5000X) after isothermal CdCl₂ vapor heat treatment in air with delayed heating and unison heating of CdCl₂.

A measure of the degree of S diffusion was obtained by performing high resolution x-ray diffraction measurements of high order (hkl) reflections. Measurements were acquired under constant count per angle to improve the signal to noise ratio. To maximize the sensitivity for the thin layers at the CdS-CdTe interface, the absorptive loss of signal in the overlying CdTe must be overcome by using films thinner than the penetration depth for that x-ray energy and Bragg angle. Either thinner CdTe films can be employed for the experiments, or device-thickness films (~4–5 µm) can be thinned after processing by a polishing etch with a buffered solution of K₂Cr₂O₇:H₂SO₄, such as Dichrol. The Rachinger correction [4.7] and binomial smoothing were applied to the raw data. Figure 4.7 shows comparative (511) peak profiles for 2.5 µm CdTe/CdS structures treated for 10 and 30 minutes by the CdCl₂:methanol application method, the parallel plate vapor method, and the confined vapor method. All profiles are similar after 10 minutes of treatment. After 30 minutes, the parallel plate and the delayed heating (reactor) methods result in similar and low S diffusion profiles while the wet application and unison heating (reactor) methods result in extended diffusion profiles extending to the solubility limits for S in CdTe_{1-x}S_x [4.8].

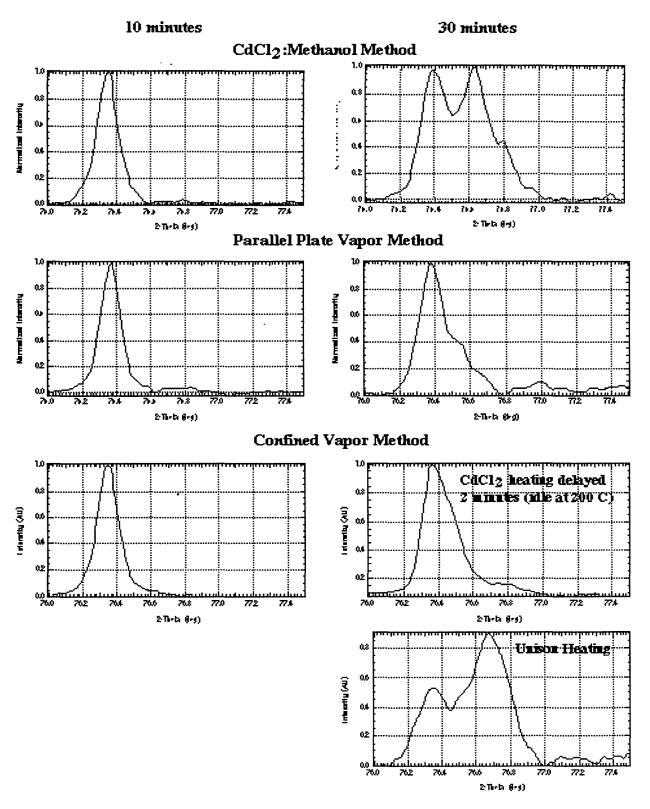


Figure 4.7. $CdTe_{1-x}S_x$ (511) x-ray diffraction peak profiles after treatments by three methods with $CdCl_2$ in air at ~420°C. The CdTe and CdS thicknesses for this comparison were 2.5 μm and 0.3 μm , respectively. The intensities have been normalized to unity.

Device Results

J-V data for samples treated with CdCl₂ vapor under the conditions of Table 4.6 are shown in Table 4.7. For the isothermal reactions, the device performance is comparable to that obtained by treatment with the parallel plate configuration, and the device performance, particularly the fill factor, across each piece is more uniform for samples treated in the reactor, presumably due to the uniform delivery of CdCl₂ species to the CdTe. Data supporting this observation is shown in Table 4.8 for devices from a single CdTe deposition processed with vapor treatments in parallel plate and reactor configurations.

Table 4.7. Device results for samples treated with CdCl₂ vapor in the reactor.

Method	T	T	Time	P _{sat}	v_{∞}	Jsc	FF	Sample
	(CdTe)	$(CdCl_2)$	(min)	CdCl ₂	(mV)	(mA/	(%)	
	(°C)	(°C)		(mtorr)		cm ²)		
Vapor	380	380	45	1.3	740	19.1	57.1	40906.11-1
Vapor	410	410	20	5.7	763	21.8	58.1	40908.23-1
Vapor	420	420	30	9.0	768	22.9	67.3	40927.13-3
Vapor	420	420	20	9.0	779	22.1	65.7	40904.12-3
Vapor	420	420	20	9.0	769	21.1	69.4	40897.21-3
Vapor	430	430	20	14.0	799	20.2	67.5	40904.13-4
Vapor	380	380	45	1.3	740	19.1	57.1	40906.11-1
Vapor	420	380	20	1.3	722	20.4	62.9	40897.23-3
Vapor	450	380	20	1.3	734	20.6	62.6	40897.32-1
Vapor	420	450	20	32.7	793	20.9	51.7	40907.22-1

The bottom of Table 4.7 shows that the treatment at reduced $CdCl_2$ concentration (T=380°C), when spanning a reaction temperature from 380°C to 450°C, gives no difference in V_{oc} , J_{sc} , and FF. However, at a reaction temperature of 420°C, increasing the $CdCl_2$ concentration from 1 mtorr to 33 mtorr improved the V_{oc} to the range obtained in isothermal cases. Thus, for reactions at one atmosphere total pressure of air, isothermal reactions in the range of 420°C to 430°C yield comparable performance to other methods, but with improved uniformity and reproducibility. This suggests that the beneficial modifications of the CdC_2 :air ambient mixture are optimal when the CdTe films are at the temperature required to maintain the $CdCl_2$ at equilibrium in the range from 5 to 10 mtorr. The link between uniform $CdCl_2$ delivery and uniform device behavior shown in Table 4.8 is a significant result and, when combined with the absence of rinse and dry steps in all-vapor processing, offers a favorable approach for large area reactions.

Table 4.8. Comparison of device uniformity for samples from run 40904 treated with CdCl₂ vapor by the parallel plate method and in the reactor. Devices with pinhole related shunts were omitted from the survey.

Method	Temp	Time	V _{oc}	Jsc	FF	Sample
	(°C)	(min)	(mV)	(mA/	(%)	_
				cm^2)		
Reactor	430	20	737	19.9	64.6	13-1
Reactor	430	20	790	20.5	66.0	13-3
Reactor	430	20	797	20.8	67.5	13-4
Reactor	420	20	786	21.4	67.1	12-1
Reactor	420	20	795	21.8	64.2	12-2
Reactor	420	20	779	22.1	65.7	12-3
Reactor	420	20	790	21.0	66.2	12-4
Plate	420	15	785	19.6	58.5	11-1
Plate	420	15	793	20.7	64.2	11-2
Plate	420	15	777	21.8	60.9	11-3
Plate	420	15	776	22.0	65.7	11-4
Plate	420	15	756	22.7	58.7	11-5
Plate	420	15	756	20.9	58.4	11-6
Plate	420	15	781	21.6	63.4	31-1
Plate	420	15	775	21.2	62.8	31-2
Plate	420	15	757	18.9	54.2	31-3
Plate	420	40	724	17.4	46.9	23-3
Plate	420	40	771	22.3	61.5	23-4
Plate	420	40	745	21.8	58.5	23-5
Plate	420	40	744	21.0	51.9	23-6

4.2.3 HCl Vapor Treatment

Introduction

Fabrication of high efficiency CdTe/CdS thin film solar cells using CdTe deposited by non-screenprint or spray methods relies on a post-deposition treatment of the CdTe/CdS structure with CdCl₂ to improve the junction properties [4.9–4.11]. The most widely used treatment technique involves coating the CdTe surface with a CdCl₂:methanol solution, evaporating the methanol, heating at temperatures near 400°C, and rinsing the surface. However, this treatment is not amenable to high-throughput large scale processing due to problems associated with uniform application of the CdCl₂ coating, removal of post-treatment residues, and safe management of large quantities of the Cd salt. Alternative techniques such as evaporating CdCl₂ onto the CdTe [4.12], or reacting the CdTe/CdS in either CdCl₂ vapor [4.13–4.15] or Cl₂ vapor [4.15] have been shown to be suitable substitutes and are more amenable to large scale processing. Of these, the Cl₂ offers advantages with respect to vapor generation and Cd toxicity. Dilute mixtures of HCl offer another possibility. In this paper we report on the effects of treatment of physical vapor deposited CdTe/CdS structures in HCl vapor as a function of HCl concentration and treatment temperature. The effects on both materials properties and device performance are considered.

Experimental Considerations

There are several practical concerns that must be considered when performing the heat treatment (HT) in HCl. These issues not only played a role in developing the procedures reported herein, but may also be important in evaluating the commercial potential of this process step.

Source Gas

Initially the experiments were conducted using HCl gas generated by bubbling Ar through concentrated (25 Mol%) hydrochloric acid and the HCl concentration in the anneal ambient was determined from the integrated gas flow and the amount of HCl measured by titration in an exhaust bubbler. Bubbling Ar through hydrochloric acid led to experimental difficulties related to excessive H₂O vapor and poor control of HCl concentration. The origin of these difficulties is attributed to the fact that the HCl-H₂O system has an azeotrope such that liquid condenses (as on tubing or reactor walls or even the inside of the acid beaker) at a concentration of about 11 Mol%. The vapor in equilibrium with this condensed liquid is approximately 97 Mol% H₂O [4.16, 4.17]. In practice, the system displayed considerable hysteresis with respect to the measured HCl concentration. Once HCl had been introduced into the system it was difficult to remove it, and conversely, in freshly cleaned apparatus the HCl concentration was less than expected.

Another concern is the effect of humidity on the HT. From the literature we know that dry HCl is not very reactive and that reactions with dry HCl often take place only in the presence of catalysts whereas hydrogen chloride in water (hydrochloric acid) is an aggressive reagent [4.16, 4.17]. For both of these reasons it was decided to change the source gas from Ar bubbled through concentrated hydrochloric acid to dry HCl mixed with Ar. As condensation is to be avoided, at no time should the humidity of the source gas reach a level at which condensation occurs.

Oxygen

The effect of O_2 in the ambient HT gas could not be investigated because at T ~400°C, heating in mixed HCl and O_2 produces coatings of solid CdCl₂ and Te layers on top of the CdTe surface. Earlier work has shown that Cl₂ reacts with CdTe to form CdCl₂ and Te [4.18]. In practice, this reaction appears to dominate any other effect, such as oxygen doping, that might occur during the HT.

4.2.4 Experimental Techniques

Sample preparation

The samples have the superstrate structure of 7059 glass/ITO/CdS/CdTe. ITO was deposited by sputtering to a thickness of ~2000 Å and sheet resistance of ~20 Ω /sq. Both CdS and CdTe were deposited by thermal evaporation with substrate temperatures of 200°C and 275°C and film thicknesses of 2200 Å and 5 μ m, respectively.

Experimental apparatus

The HCl post-deposition treatment was conducted in an evacuatable tube furnace system. Before each run the furnace was evacuated with a mechanical pump to ~0.1 torr and backfilled with high purity Ar. Two thermocouples were installed in the system; one was used for furnace temperature control and the other for measuring sample temperature. Commercial 5% HCl in Ar from Matheson was used as the HCl source. The concentration of HCl in the reaction chamber was reduced by adding additional Ar.

Experimental parameters

Samples were divided into two groups. One group was used to study the effect of HCl concentrations of 0, 0.5%, 1.6%, 3.0% and 5% during a HT at a temperature of 400°C for 30 minutes. The second group was used to study the effect of temperatures of 380°C, 400°C, 420°C and 440°C with a fixed 5% HCl concentration for 30 minutes.

After the film properties had been measured, back contacts were applied using the "diffused Cu" method [4.19] and applying carbon paste electrodes. The irregular shape of these electrodes led to ~10% uncertainty in the determination of device area and therefore of the current density.

4.2.5 Characterization

Film morphology and grain size

The effects of treatment on the surface morphology and chemical composition were measured by scanning electron microscopy (SEM) and energy dispersive spectroscopy (EDS). The average grain size (AGS) was calculated by dividing the length of a line drawn across the SEM micrograph by the number of intersections with grain boundaries and then dividing by the magnification.

Preferred crystal orientation

The degree of preferred (111) orientation, p(111), was quantified from x-ray diffraction scans using the method of Harris for polycrystalline fiber texture analysis [4.20]. For the (111) peak this quantity is:

$$p(111) = \frac{I(111)/I_0(111)}{\frac{1}{N} \sum_{hkl} I(hkl)/I_0(hkl)}$$
(4.1)

where N is the number of peaks in the region considered, I(hkl) is the measured intensity of peak hkl, and $I_0(hkl)$ is the relative intensity of the corresponding peak from a powder sample. In this case p(111) = 9 means that the film is completely (111) oriented while p(111) = 1 implies perfectly random distribution.

Optical measurements

Transmission and reflection were measured to determine the absorption edge location, which allows shifts in the bandgap, ΔE_g , to be observed. The bandedge is expected to shift due to the formation of the $CdTe_{1-x}S_x$ as a result of interdiffusion near the CdTe/CdS interface. The shift was measured with respect to the absorption of as-deposited CdTe which has been confirmed by XRD measurements of lattice constant to have $x \approx 0$. The value of x was estimated assuming linear variation of E_g over the range 0 to 6% [4.21]. The shift in bandgap was determined from a plot of the absorption coefficient squared versus energy.

4.2.6 Results and Discussion

Results of the above measurements for films heated at 400°C in various HCl:Ar concentrations are listed in Table 4.9; results for films heated at various temperatures at 5 vol% HCl:Ar are listed in Table 4.10.

Table 4.9. Film parameters vs HCl:Ar concentration (vol%) during a 30 min. HT at 400°C.

[HCl]	AGS	p(111)	d(111)	ΔE_g	[S],
(vol%)	± 0.1		±0,01	(meV)	X
	(µm)		(A)		(%)
as-dep	0.7	4 - 7	3.76	0	0
0	0.7	2.8	3.76	~5	~0.5
0.5	0.9	1.3	3.75	~10	~1.0
1.6	1.0	1.7	3.74	~15	~1.5
3.0	1.2	2.7	3.73	~15	~1.5
5.0	1.1	1.2	3.74	~15	~1.5

Table 4.10. Film parameters vs temperature during a 30 min. HT in 5 vol% HCl:Ar.

Temp (°C)	AGS ± 0.1 (μm)	p(111)	d(111) ±0.01 (Å)	ΔE _g (meV)	[S], x (%)	
380	1.0	1.9	3.76	~10	~1.	0
400	1.0	3.2	3.77	~15	~1.	5
420	1.2	1.8	3.75	~15	~1.	5
440	1.4	0.8	3.75	~20	~2.	0

Film properties

SEM and EDS analysis pictures show that the surfaces of samples treated in HCl+Ar are clean and without residue.

Thermally evaporated as-deposited CdTe films have an average grain size of ~0.7 μm for 5 μm thick films. Figures 4.8 and 4.9 show the surface structure for films heated in various HCl:Ar concentrations and temperatures. The measured average grain sizes are listed in Table 4.9. HCl in the anneal ambient clearly promotes grain growth; heating without HCl produced no change in average grain size. This confirms that HCl (as CdCl₂ does) may work as a flux which breaks down atomic diffusion barriers at grain boundaries and thereby promotes grain growth. The average grain size increases with increasing temperature over the range of 380°C to 440°C, but only in the presence of HCl.

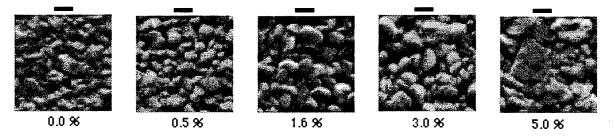


Figure 4.8. SEM photos of the surface of CdTe films heated at 400°C for 30 minutes at the HCl:Ar concentrations indicated. The scale bar is one micron.



Figure 4.9. SEM photos of the surface of CdTe films heated in 5% HCl for 30 min. at the indicated temperatures. The scale bar is one micron.

It was found that for thermally evaporated as-deposited CdTe films, p(111) is usually in the range of 4–7. After post-deposition heat treatment in HCl+Ar for 30 minutes p(111) usually decreases to the range of 1–3. In addition, the data listed in Table 4.9 suggest that for these samples there is also a decrease in the lattice constant.

Plots of the square of the absorption coefficient versus energy are shown in Figures 4.10 and 4.11 for the CdTe/CdS structures treated at 400°C for 30 minutes at varying HCl:Ar concentration and at various temperatures in 5% HCl:Ar. With increasing HCl concentration the optical absorption curves indicate a decrease in bandgap. The bandgap shift with HCl concentration suggests that the effect of the HCl reaches the CdTe/CdS interface, perhaps through grain boundaries, and enhances interdiffusion.

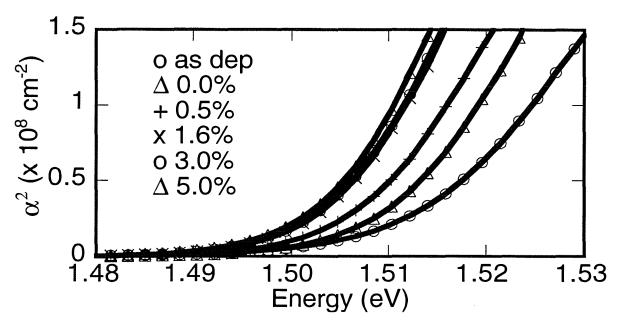


Figure 4.10. Plot of absorption coefficient squared versus energy for CdTe/CdS films treated at 400°C for 30 minutes at the HCl:Ar concentrations shown.

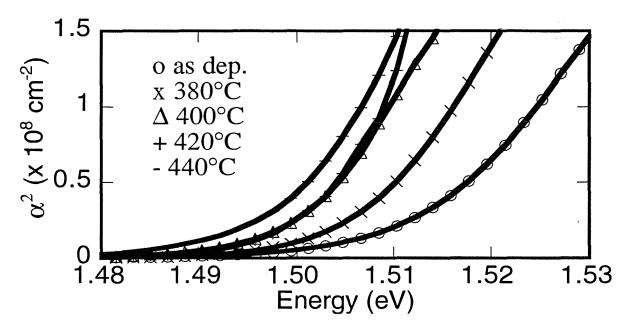


Figure 4.11. Plot of absorption coefficient squared versus energy for CdTe/CdS films treated in 5% HCl:Ar for 30 minutes at the temperatures indicated.

Cell results

The effect of HCl concentration on the dark and light J-V behavior of devices is shown in Figure 4.12 for increasing HCl concentration from 0 to 5%. From the light data we note that carrier collection, as determined from the magnitude and slope of the curve near J_{sc} , improves with HCl concentration. It is not clear whether increasing concentration above the range included in this study would produce results similar to those obtained using CdCl₂ treatments. Figure 4.12 also

shows that the light-dark crossover is less severe at the higher HCl concentrations suggesting that conductivity increases with HCl concentration. The mechanism for this is not apparent. In addition, it was noted that hysteresis between forward and reverse voltage sweeps was reduced at higher concentrations as well.

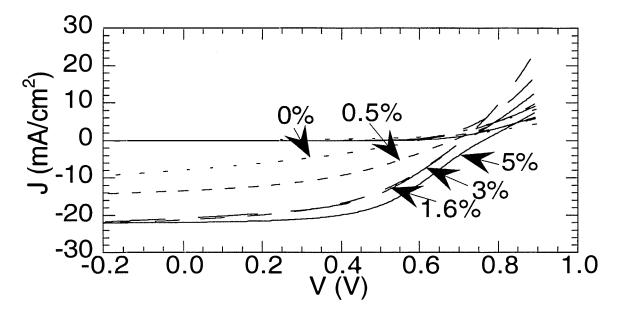


Figure 4.12. Dark and light J-V data for devices made from films heat treated for 30 min. at 400°C in various HCl:Ar concentrations.

The effects of process temperature variations are summarized qualitatively in Figure 4.13. Changing the temperature of the heat treatment in 5% HCl over the range 380°C to 440°C had minimal effect on light or dark J-V behavior. The scatter in data is such that no trends are evident in either the light or dark J-V data. In addition, all of the HCl heat treated devices are characterized by strong light-dark crossover in the first quadrant and poor collection efficiency.

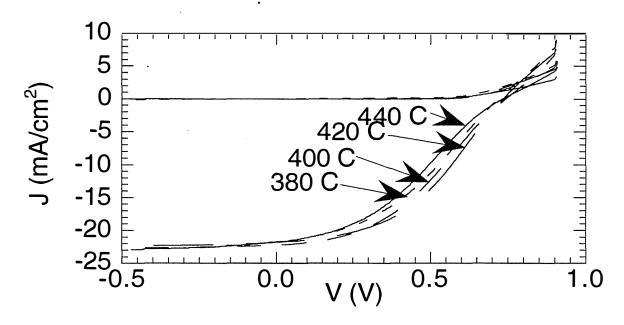


Figure 4.13. Dark and light J-V data for devices made from films heat treated for 30 min. in 5% HCl at various temperatures.

4.2.7 Conclusions

Treatment of CdTe/CdS thin film structures in dilute mixtures of HCl vapor at 380°C to 440°C promotes similar microstructural changes in the structure to treatment with CdCl₂. While not yet optimized for high conversion efficiency, this shows promise as an alternative to treatments with CdCl₂. The structural properties are sensitive to both HCl concentration and treatment temperature. However, the device performance, particularly the short circuit current and fill factor, are highly sensitive to HCl concentration but only slightly sensitive to treatment temperature. Achieving higher efficiency than demonstrated here will require exploration of a wider parameter space, including higher HCl concentration and multiple step treatments, such as HCl treatment followed by air treatment. Some of the difficulties associated with the use of hydrochloric acid as the vapor source and with using HCl:O₂ mixtures have been identified.

4.3 Stress Testing

4.3.1 Introduction

A convincing demonstration of module stability is essential to the long term commercial success of CdTe photovoltaics. This work seeks to contribute to that goal by probing CdTe devices for weaknesses or possible degradation mechanisms that may influence their long term stability under field conditions. One premise of these studies is that the application of electrical, optical or thermal stress at levels beyond those expected under field conditions will activate chemical or electrochemical processes which otherwise might not noticeably affect device performance until several years of use. This premise is unproved, i.e., there is no proof that stressed devices exhibit chemical or electrical characteristics similar to those observed in devices after years of field testing. Conversely, there may be degradation mechanisms which occur in field use which are not accelerated by electrical, optical or thermal stress. Nonetheless, these stresses would be expected to increase the rate of such potential degradation mechanisms as oxidation, electromigration or ionic diffusion, and it is these phenomena which are the target of the present study.

The most delicate feature of the CdTe/CdS device is believed to be the low loss back contact. Low resistance contacting methods typically involve use of Te-rich interfaces or p-type semiconductors such as HgTe or ZnTe, or thin layers including small amounts of Cu [4.22–4.24]. Some devices subjected to stress testing or life testing display high series resistance and/or evidence of a reverse diode—both characteristics which could be attributed to the back contact. It has been reported [4.25] that reverse voltage bias at elevated temperature causes rapid degradation of device parameters and that this effect can be at least partially reversed by the application of a forward bias. Similar effects have been observed with devices produced in our lab. Analysis of the IEC light J-V curves indicated that there were at least two mechanisms responsible. Reversible effects included increases in series resistance and decreases in J₀ of the reverse diode upon application of reverse bias (with opposite changes upon forward bias); permanent effects included an additional increase in series resistance and a reduction in collected photocurrent [4.26, 4.27]. At this point it is not clear whether all CdTe devices display these effects or have the same sensitivity to these stresses.

4.3.2 Experimental Procedure

Devices evaluated in this study had the superstrate structure displayed in Figure 4.14. The CdTe/CdS/SnO₂:F/sodalime glass supplied by Solar Cells, Inc. was cut into 2.5 cm x 2.5 cm pieces from a 7200 cm² superstrate which had been coated and processed using SCI's normal procedures up to the point of completion of the post-deposition heat treatment [4.28]. The devices were completed using the "diffused Cu" back contact processing [4.29], sputter deposition of Mo contacts through a mask, mechanical scribing, and application of a room temperature curing urethane insulator. Electrical contact was made using Ag epoxy (Acheson Electrodag MB80021) which was cured in Ar at 140°C for ~10 minutes. In order to facilitate the subsequent depth profiling, in selected devices the Ag epoxy was applied only to the perimeter of the cell. Wire leads were soldered to the exposed SnO₂ pads using Indalloy solder #204. The leads were necessary to apply and maintain voltage bias on the devices during stressing and were used for making all J-V measurements.

CdTe Solar Cell Test Structure (post-scribe TCO)

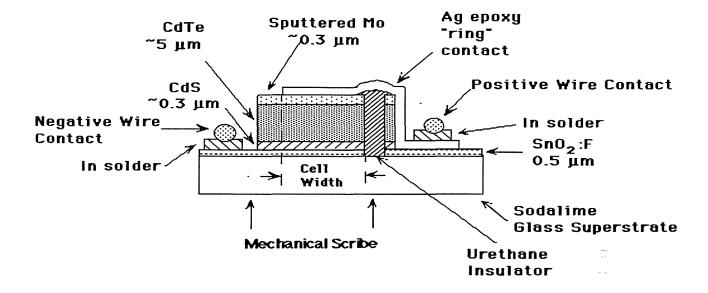


Figure 4.14. Schematic of CdTe/CdS device structure employed in these studies.

Devices were not encapsulated, but all stressing was done inside a glove box with flowing N_2 (Figure 4.15). Inside the glove box humidity was measured at <2% relative humidity at 50°C; oxygen content was not determined.

STRESS TEST APPARATUS

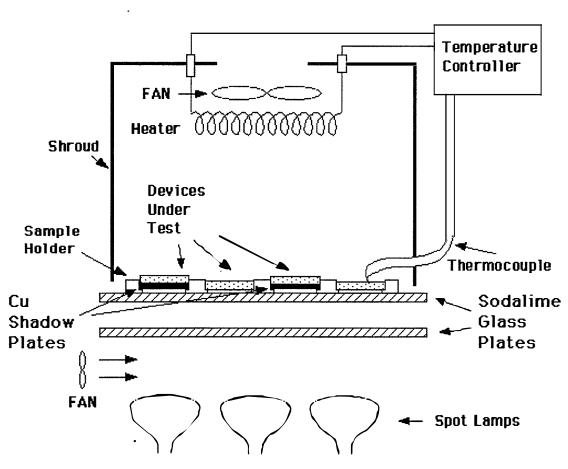


Figure 4.15 Schematic representation of the stress test apparatus.

Prior to beginning the stress testing, devices have been screened to select those whose J-V data is analyzable within the context of a simple equivalent circuit containing a main junction diode with series resistance and shunt conductance. The active area of these devices was estimated and set to $0.6 \, \mathrm{cm}^2$. Briefly, the J-V characteristics recorded at room temperature in the dark were plotted on various sets of axes—J vs V, log(J) vs (V), dJ/dV vs V, and dV/dJ vs [J]⁻¹—and these curves were used to provide information about device operation. Devices exhibiting excessive series resistance (>10 Ω -cm²), shunting conductance (> 1 mS/cm²), or hysteresis (P_{max} (upsweep) -

 P_{max} (downsweep)I > 0.15mW/cm² in the light) were rejected as were devices whose dark J-V characteristics could not be described with a simple diode (apparent diode quality factor >2.0). Minimum acceptable V_{oc} and FF were 0.74 V and 0.59, respectively. A total of 16 devices meeting these criteria were selected for testing. Of these devices, four were stressed only with temperature (no electrical or light stress), one was stressed with temperature and electrical bias (0.5)

Volts), and the remaining 11 were stressed with temperature, illumination (~70 mW/cm²) and electrical bias (see Tables 4.11 and 4.12). Illumination was provided by tungsten filament spot lamps and was therefore quite "red" compared with the AM1.5 Global spectrum. The intensity was estimated from the short circuit current of the CdTe cells mounted in the stress test station.

Table 4.11 Electrical bias and temperature stress conditions for illuminated devices ($\sim 70 \text{ mW/cm}^2$).

	82°C	92°C	112°C
-0.5 V		√	
J_{sc}	1	√	V
$R_L = 70 \text{ W}$	\forall		√
V_{∞}	7	1	√
+2.5 mA		V	

Table 4.12 Electrical bias and temperature stress conditions for devices stressed in dark.

	72°C	88°C	104°C
none	7	2	7
-0.5 V		 \(\forall \)	
+2.5 mA		√	

J-V data was recorded at various intervals during the stress testing. In addition, devices were removed and room temperature J-V (@ AM1.5 Global illumination and dark) and spectral response were also recorded prior to and at various times during stress testing (Table 4.13). Total time under stress was 720 hours.

Table 4.13 Frequency and types of measurements made on stressed devices.

Hrs. under stress	0		4	24	4	48	67	109	196	550	720
J-V (@ std. illum. & temp.)	1		1	1 1	·	1	1	1	√	√	V
J-V (@ stress cond.)	1							√			V
QE (with & w/o bias light)	1 1	1			Π			7			V

4.3.3. Experimental Results

Tables 4.14 to 4.19 show the evolution of the basic J-V parameters as a function of time under the various stress conditions. One point to note is that with all of the devices, their output increased (especially J_{sc}) between the initial test and after four hours stress. This probably happened because the device was not given sufficient time to recover (anneal) after mounting in the individual test structure before the initial test was done. Because of this, wherever possible, the four-hour stress point will be used as a comparison.

Table 4.14 Basic J-V parameters of devices stressed @ 82° C & ~70mW/cm² illumination for the electrical bias and amount of time indicated (*based on an estimated area of 0.6 cm^2).

Elec.bias	hrs.	0	4	24	48	67	109	196	550	720
										_
	$\overline{V_{\infty}}$	0.793	0.829	0.786	0.790	0.818	0.783	0.777	0.773	0.772
V_{∞}	FF	67.3	66.7	65.1	61.8	63.2	59.9	56.6	58.6	59.7
	J _{sc} *	15.2	17.6	17.8	17.3	17.9	17.6	17.9	17.7	17.6
	h*	8.1	9.7	9.1	8.5	9.3	8.3	7.9	8.0	8.1
						•				
	$\overline{V_{\infty}}$	0.783	0.802	0.804	0.799	0.800	0.803	0.796	0.792	0.776
R _L =70 Ω	FF	63.5	64.3	64.7	64.1	62.8	61.5	62.1	60.5	57.3
	J_{sc}^*	17.2	19.7	20.3	19.0	20.2	19.8	20.0	20.1	19.4
	h*	8.5	10.2	10.5	9.8	10.1	9.8	9.9	9.6	8.6
	$\overline{V_{\infty}}$	0.798	0.795	0.789	0.785	0.778	0.792	0.769	0.748	0.743
J_{sc}	FF	66.1	66.4	66.1	65.8	65.5	65.4	63.8	60.6	60.6
	J_{sc}^*	15.1	17.6	17.6	17.4	17.2	17.3	17.2	16.9	16.9
	h*	8.0	9.3	9.2	9.0	8.8	8.9	8.4	7.7	7.6

Table 4.15 Basic J-V parameters of devices stressed @ 92° C & ~ 70mW/cm^2 illumination for the electrical bias and amount of time indicated (*based on an estimated area of 0.6 cm^2).

Elec.bias	hrs.	0	4	24	48	67	109	196	550	720
	V_{∞}	0.809	0.824	0.760	0.751	0.719	0.732	0.743	0.751	0.750
+2.5 mA	FF	69.2	66.7	61.2	61.7	58.9	58.9	59.9	57.7	56.9
	\overline{J}_{sc}^*	17.3	19.7	19.9	19.5	19.7	19.6	19.5	19.2	19.0
	h*	9.7	10.9	9.3	9.0	8.3	8.5	8.7	8.3	8.1
	V_{∞}	0.787	0.819	0.723	0.703	0.703	0.707	0.704	0.724	0.721
V_{∞}	FF	65.0	63.4	58.5	58.6	58.9	59.3	59.6	59.0	59.4
	J_{sc}^*	17.6	20.7	20.9	20.5	20.6	20.5	20.5	20.4	20.4
	h*	9.0	10.8	8.8	8.5	8.5	8.6	8.6	8.7	8.7
	V_{∞}	0.809	0.800	0.771	0.765	0.756	0.771	0.750	0.738	0.734
J_{sc}	FF	69.1	68.0	63.0	62.9	60.3	62.7	59.9	57.9	57.5
	J _{sc} *	15.6	17.6	17.8	17.3	17.4	17.5	17.4	17.5	17.3
	h*	8.7	9.6	8.6	8.3	7.9	8.5	7.8	7.5	7.3
										**
	V_{∞}	0.818	0.791	0.753	0.735	0.723	0.699	0.693	0.662	0.670
-0.5 V	FF	70.7	65.5	57.5	57.0	56.6	57.2	53.1	60.4	59.9
	J _{sc} *	17.4	19.7	17.8	16.1	15.9	14.7	19.4	11.2	11.6
	h*	10.0	10.2	7.7	6.7	6.5	5.9	7.1	4.5	4.7

Table 4.16 Basic J-V parameters of devices stressed @ 112° C & ~ 70mW/cm^2 illumination for the electrical bias and amount of time indicated (*based on an estimated area of $0.6~\text{cm}^2$).

Elec.bias	hrs.	0	4	24	48	67	109	196	550	720
	V_{∞}	0.797	0.817	0.787	0.781	0.780	0.786	0.778	0.776	0.776
V_{oc}	FF	68.0	65.9	61.0	60.2	59.5	59.4	58.2	56.7	57.0
	J_{sc}^*	16.8	18.9	19.2	18.8	18.7	18.7	18.7	18.3	17.8
	h*	9.1	10.2	9.2	8.8	8.7	8.7	8.5	8.0	7.9
	V_{∞}	0.793	0.815	0.810	0.804	0.801	0.801	0.790	0.780	0.784
R _L =70 Ω	FF	67.4	70.0	67.5	66.8	64.6	57.7	64.2	48.5	58.0
	J_{sc}^*	14.9	17.0	17.0	16.8	16.8	16.8	16.8	16.6	16.7
	h*	8.0	9.7	9.3	9.0	8.7	7.8	8.5	6.3	7.6
		-					-			
	V_{∞}	0.800	0.791	0.773	0.766	0.759	0.762	0.744	0.732	0.729
J_{sc}	FF	68.0	64.8	60.2	57.9	56.3	56.8	52.9	50.2	49.0
	J_{sc}^*	15.9	17.7	17.7	17.3	17.2	17.1	16.5	15.4	15.8
	h*	8.7	9.1	8.2	7.7	7.3	7.4	6.5	5.7	5.7

Table 4.17 Basic J-V parameters of devices stressed @ 72° C & dark with no electrical bias (0 V) and amount of time indicated (*based on an estimated area of $0.6~\text{cm}^2$).

hrs.	Q	4	24	48	67	109	196	550	720
V_{∞}	0.811								
FF	70.1	70.1	67.5	67.8	67.3	68.4	62.1	66.6	66.5
J_{sc}^*	15.4	17.8	18.1	17.3	17.3	17.3	17.5	17.7	17.4
h*	8.8	10.1	9.8	9.3	9.2	9.6	8.7	9.4	9.1

Table 4.18 Basic J-V parameters of devices stressed @ 88° C & dark for the electrical bias and amount of time indicated (*based on an estimated area of 0.6 cm²).

Elec.bias	hrs.	l O	4	24	48	67	109	196	550	720
	V_{∞}	0.806	0.834	0.836	0.828	0.822	0.813	0.799	0.790	0.787
+2.5 mA	FF	69.4	69.0	67.6	65.9	64.3	59.9	62.1	59.1	57.1
	J _{sc} *	15.8	17.7	17.6	17.4	17.5	17.5	17.7	17.3	17.5
	h*	8.9	10.2	10.0	9.5	9.3	8.5	8.8	8.1	7.9
	V_{∞}	0.803	0.813	0.815	0.814	0.813	0.820		0.810	0.806
0 V	FF	68.8		67.2	67.1	66.7	67.1	67.1	63.8	65.0
	J _{sc} *	14.1	15.9	16.1	15.9	15.9	15.9	16.0	15.8	15.9
	h*	7.8	8.9	8.8	8.7	8.6	8.7	8.7	8.2	8.3
	V_{∞}	0.801	0.782	0.784	0.778	0.777	0.782	0.777	0.779	0.775
0 V	FF	69.4	64.4	64.3	64.3	64.0	64.3	64.6	64.0	63.5
	J_{sc}^*	15.7	17.6	17.7	17.4	17.5	17.6	17.7	17.4	17.6
	h*	8.7	8.8	8.위	8.7	8.7	8.8	8.9	8.7	8.6
	V_{∞}	0.808	0.786	0.765	0.761	0.758	0.766	0.747	0.742	0.689
-0.5 V	FF	69.0	65.5	61.4	60.2	59.7	58.4	50.4	55.8	53.7
	J _{sc} *	15.6	17.3	17.3	16.9	16.9	16.6	16.3	16.2	14.5
	h*	8.7	8.9	8.1	7.7	7.7	7.4	6.1	6.7	5.4

Table 4.19 Basic J-V parameters of devices stressed @ 104° C & dark with no electrical bias (0 V) and amount of time indicated (*based on an estimated area of $0.6~\text{cm}^2$).

hrs.	0	4	24	48	67	109	196	550	720
Voc	0.808	0.743	0.7411	0.738	0.738	0.747	0.741	0.749	0.750
FF	69.1	46.0	48.4	48.6	49.1	49.2	48.8	50.4	51.1
J_{sc}^*	16.7	18.2	18.5	18.2	18.3	18.3	18.3	18.3	18.3
h*	9.3	6.2	6.6	6.5	6.6	6.7	6.6	6.9	7.0

From these tables it can be seen that there is a reduction of V_{oc} and FF in all cases (the precipitous loss in FF for the device @104°C was caused by the development of a shunt) (Table 4.19). However, J_{sc} loss was only seen in the two samples that were stressed under illumination and held in reverse bias, -0.5 V @ 92°C (Table 4.15) or at 112°C and J_{sc} (Table 4.16).

To examine these effects in more detail, the J-V curves of the devices stressed at 92°C under illumination are shown in Figures 4.16-4.19.

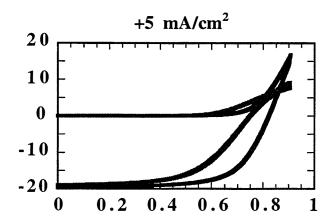


Figure 4.16 Illuminated and dark J-V characteristics of device stressed with illumination at 92°C and 2.5 mA forward bias.

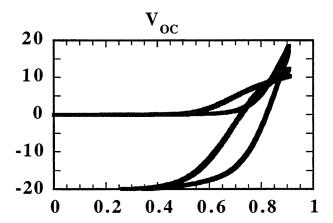


Figure 4.17 Illuminated and dark J-V characteristics of device stressed with illumination at 92 $^{\circ}\text{C}$ and at $V_{oc}.$

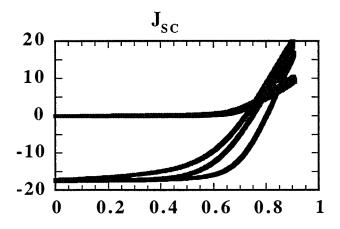


Figure 4.18 Illuminated and dark J-V characteristics of device stressed with illumination at 92°C and at $J_{sc}\text{.}$

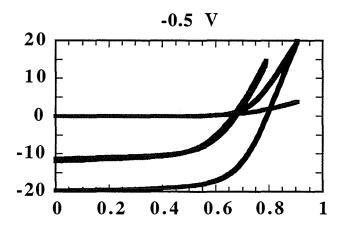


Figure 4.19 Illuminated and dark J-V characteristics of device stressed with illumination at 92°C and -0.5 V reverse bias.

From the J-V curves shown it can be seen that the reduction in V_{oc} is not due to either shunting or $J_L(V)$ effects, and therefore is caused by an increase in J_o . There is also a large increase in the dark series resistance in addition to the evidence of blocking contact behavior of the devices stressed at 2.5 mA forward bias and V_{oc} . To examine further the loss of light generated current seen in the -0.5 V reverse biased sample, it is useful to look at the QE's of this sample shown in Figures 4.20 and 4.21.

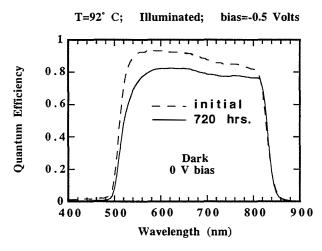


Figure 4.20 QE (without voltage or light bias) of device stressed with illumination at 92°C and -0.5 V reverse bias.

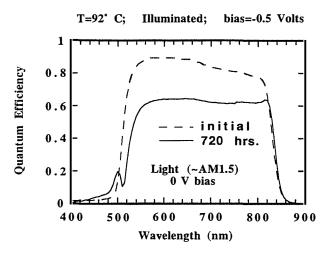


Figure 4.21 QE (with ~AM1.5 light bias and no voltage bias) of device stressed with illumination at 92°C and -0.5 V reverse bias.

Although more striking with light bias, these measurements show an almost panchromatic loss in quantum efficiency in the region that the CdTe absorbs light.

4.3.4 Conclusion

In the specially prepared CdTe devices that have been subjected to stresses beyond normal operating there appears to be changes that are associated with stress temperature and electrical bias. It is not clear whether there is a dependence on illumination level. One effect is promoted by reverse bias and affects primarily the bulk CdTe properties as indicated by the severity of the light-dark crossover of the J-V curves. Another effect is promoted by forward bias and results in the strengthening of a reverse diode. Finally, there are changes in both the light generated current and J_0 whose magnitudes are also bias and light dependent. The results reported herein are from workin-progress. The data were recorded on a limited data set, 16 samples, and using a single method of device preparation. Additional experiments as well as other samples prepared by various groups are necessary to confirm or refute these results.

4.4 CdTe-CdS Alloys

4.4.1 Background

Evidence that the commonly used recrystallization heat treatment in the presence of CdCl₂ at 400°C to 430°C promotes interdiffusion between the CdTe and CdS layers in CdTe/CdS solar cells has been reported by several groups [4.30–4.33]. A quantitative understanding of the interdiffusion process requires knowledge of the properties of the CdTe-CdS alloy system. Ultimately the interdiffusion process is limited by the solubilities of S in CdTe and of Te in CdS. The lowest temperature data points on published CdTe-CdS pseudo-binary phase diagrams [4.34] indicate that, at 650°C, a miscibility gap extends from xJ[S]/([S]+[Te])=0.16 to 0.86. At the typical temperatures used in recrystallization heat treatments, ~415°C, the miscibility gap should be even wider due to the reduced influence of entropy on the free energy of the system.

Despite the wide miscibility gap, some groups have been able to fabricate single-phase thin films of $CdTe_{1-x}S_x$ with x in the middle of the miscibility gap [4.35–4.38]. In order to reconcile the existence of these films with the equilibrium phase diagrams, it must be assumed that these films

were either metastable or kinetically limited. Thus, sufficient heat treatment should cause such films to segregate into two phases with compositions at either end of the miscibility gap. At 415°C, however, a prohibitively long time would be needed to complete the segregation process without the use of an external agent such as CdCl₂ to increase the atomic mobility.

The goal of this work was to measure the extent of the miscibility gap at 415°C by using CdCl₂ to hasten the phase segregation process. The bandgap dependence on atomic composition and solubility limits derived from the study of co-evaporated CdTe_{1-x}S_x films were then compared to the material properties of actual solar cell device structures in order to demonstrate the importance of these parameters in the interdiffusion process.

4.4.2 Experimental and Analysis

Thin films of CdTe_{1-x}S_x with thicknesses of 2 to 3 μ m were grown on glass and In₂O₃:Sn (ITO) substrates by co-evaporation of CdS and CdTe at substrate temperatures of 200°C and 250°C. Energy dispersive spectroscopy (EDS) was used to measure the average atomic composition of each film. Bragg-Bretano geometry x-ray diffraction (XRD) analysis with Cu K_a radiation was used to determine the structures of the phases within the films. Precision lattice parameters of each phase within the films were derived by Nelson-Riley-Sinclair-Taylor (NRST) reduction of the d-spacings. Vegard's law was then used to transform the precision lattice parameters into atomic compositions. The optical transmission and reflection of the films were measured and used to estimate the absorption constant, a. The linear portion of (ahn)² versus hn was extrapolated to obtain an optical bandgap.

Two CdCl₂ heat treatment methods were employed to promote the phase segregation process. In the "wet" method, CdCl₂ was deposited directly on the film [4.39]. In the "vapor" method, CdCl₂ was kept at distance ≈ 0.1 mm away from the film surface [4.40]. In both cases, the CdCl₂ and film were treated in air at 415°C to 420°C.

CdTe/CdS solar cell device structures were fabricated for materials characterization. The device structures consisted of a 4-5 µm CdTe absorber layer and a ~2500Å CdS window layer deposited by vacuum evaporation onto ITO/Coming 7059 glass substrates. The CdS was subjected to a 10 minute CdCl₂ vapor pre-treatment prior to deposition of CdTe. Following CdTe deposition, the CdTe/CdS structure was given a 20 minute vapor CdCl₂ post-treatment. Devices with efficiency exceeding 10% were made on regions of the CdTe/CdS structures not being used for materials analysis which verified the quality of these structures. XRD and optical analysis was performed on the structures in order to quantify the range of alloy compositions. Since the alloy composition in such structures is generally non-uniform, high resolution XRD profiles of the zincblende (511) peak were used to examine the extent of non-uniformity. To account for systematic shifts in the peak position due to instrumental and other errors, NRST reduction was performed on the maxima of all detectable zincblende peaks to obtain a precision lattice parameter, and then the position of the maximum of the (511) peak was adjusted to match this lattice parameter. At the angle of the (511) peak, this technique is sensitive to a depth of approximately 3 µm in CdTe. In order to probe the alloy composition in the region of the junction, the CdTe layer was thinned to ~2 μm by etching in a buffered solution of K₂Cr₂O₇ and H₂SO₄, commercially available as Dichrol.

4.4.3 Results

Co-evaporated CdTe_{1-x}S_x thin films

As-deposited films were produced with overall atomic compositions ranging from x = 0 to 0.45. XRD analysis revealed that films with x < 0.3 were predominately single phase having the zincblende structure. Films with 0.35 < x < 0.45 contained the wurtzite modification, although the

presence of a small amount of material with the zincblende structure was suggested by a small peak at a d-spacing corresponding to the (111) peak of pure CdTe. Figure 4.22 shows that the composition of the dominant phase in each as-deposited film determined by XRD analysis closely matched the average composition of each film determined by EDS analysis even when the average composition was well within the miscibility gap. This demonstrates that each phase can exist with compositions within the miscibility gap.

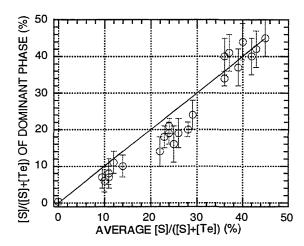


Figure 4.22. Composition of the dominant phase of each as-deposited alloyed film plotted against the composition averaged over all phases in the film. The solid line indicates where the two compositions are equal.

For most of the as-deposited films, plots of $(ahn)^2$ verses hn featured a notable linear region which could be extrapolated to estimate the optical bandgap. The bandgap variation with composition is compared to other works in Figure 4.23. Particularly good agreement with reference [4.37], which used similar analysis techniques to this work, was noted.

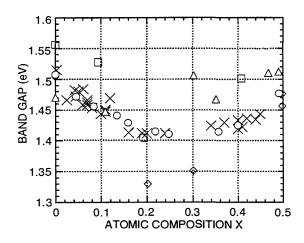


Figure 4.23. Measured bandgaps of as-deposited $CdTe_{1-x}S_x$ thin films as a function of x as reported in this work (X), and references 6 (triangles), 7 (diamonds), 8 (circles), and 9 (squares).

As expected, upon heat treatment in the presence of CdCl₂ at 415°C, the films segregated into two phases. The rate of phase segregation was found to depend on the average composition of the films, but the final composition of each of the phases was independent of this factor as shown in Figure 4.24. Likewise, the vapor and surface methods of CdCl₂ treatment resulted in different rates of phase segregation but the same final composition. This suggests that the solubility limits are not significantly dependent on the incorporation of small amounts of CdCl₂. If this is the case, then the compositions of the two phases after heat treatment may be taken as measurements of the solubility limits of S in CdTe and Te in CdS, respectively. The 415°C solubility limit of S in CdTe is, thus, $x = [S]/([S] + [Te]) = 0.058 \pm 0.003$, and the solubility limit of Te in CdS is $y = [Te]/([S] + [Te]) = 0.03 \pm 0.01$.

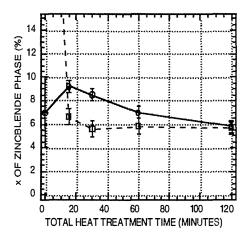


Figure 4.24. Composition of the zincblende structured phase in a film with average atomic composition [S]/([S]+[Te])=10.8% (circles) and one with [S]/([S]+[Te])=40.3% (squares) as a function of cadmium chloride treatment time.

Alloy composition of solar cell absorber layers

In order to quantify the degree of interdiffusion occurring in the processing of high efficiency devices, extensive XRD analysis was performed on CdCl₂ treated CdTe/CdS structures. The precision lattice parameter obtained by NRST reduction indicates that the majority of the absorber material has a composition of $x = 0.6 \pm 0.3\%$. As shown in Figure 4.25a, a high resolution scan of the (511) peak on a 4.7 µm thick film resulted in a symmetrical profile with a width close to the instrument function of the diffractometer. This profile indicates the CdTe layer is relatively and uniformly sulfur free to depth of ~3 \text{ \text{\mu}m.} In order to probe the composition closer to the junction, the absorber layer was chemically thinned to ~2 µm by etching in Dichrol. Although the positions of maxima of the XRD peaks were the same as before etching, the (511) peak displayed a wide shoulder as shown in Figure 4.25b extending to lower lattice spacing as expected for CdTe_{1-x} S_x . For reference, the expected positions of the maxima of the (511) peak for a film containing no sulfur and one containing the solubility limit of sulfur are also indicated in Figure 4.25. These results indicate that device structures contain alloy compositions ranging from the solubility limit near the junction to virtually no sulfur near the back contact. Comparable results were found for device structures provided by Solar Cells, Inc. (SCI) and the University of South Florida (USF), indicating that the solubility limit derived from the study of co-evaporated CdTe_{1-x} S_x films applies to several fabrication and heat treatment methods.

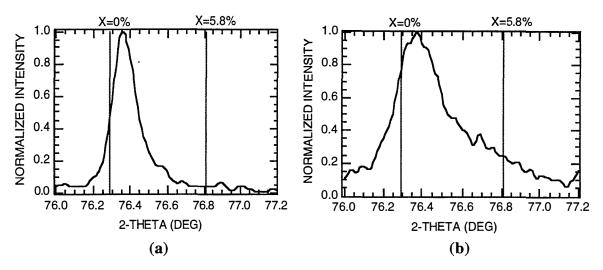


Figure 4.25. High resolution XRD scan of the (511) peak of (a) the 4.7 μ m thick absorber layer of a CdTe/CdS solar cell structure and (b) the same peak after chemically etching the absorber layer to 2 μ m.

A plot of $(ahn)^2$ verses hn of a CdTe/CdS device structure is shown in Figure 4.26 both before and after heat treatment. Before heat treatment, the absorption constant is close to that of a pure CdTe film (grown on ITO). After heat treatment, the curve shifts towards lower energy. Also plotted for comparison is the absorption of a CdCl₂ heat treated, co-evaporated CdTe_{1-x}S_x film on ITO for which the atomic composition of the zincblende phase was uniformly at the solubility limit of S in CdTe. As expected, the absorption of the device structure does not exceed that of the alloy at the solubility limit.

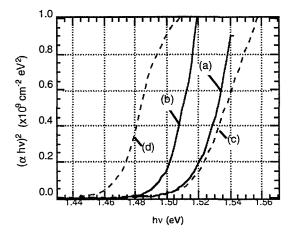


Figure 4.26. Absorption coefficient vs. photon energy for a CdTe/CdS structure (a) before and (b) after heat treatment. These curves are expected to lie between the absorption coefficients of (c) pure CdTe on an ITO substrate and of (d) a CdTe_{0.9}S_{0.1} film that has been made to phase segregate by CdCl₂ treatment.

Alloy composition of solar cell window layers

A measurement of the alloy composition in the window layer of a completed device structure was made possible by selectively etching away the absorber layer by etching with Dichrol. CdCl₂ pretreatment of the CdS prior to deposition of CdTe has been shown to decrease the diffusion of Te

into the CdS during the CdCl₂ post-treatment [4.41]. To explore the variability in the degree of Te diffusion into the window layer, devices were fabricated on CdS subjected to various pre-treatment conditions. Table 4.20 summarizes the pre-treatment conditions used and the results of EDS and XRD analysis of the exposed window layers. The window layer that received the longest CdCl₂ treatment was nearly the same shade of yellow after stripping away the absorber layer as it was before deposition of the CdTe, while the other windows were more orange. This color difference is due to a loss in transmission at around 530 nm on the films which were either not pretreated or were weakly pretreated (Figure 4.27). In devices this loss reduces the short circuit density by ~1 mA/cm² and has been previously described [2.12]. EDS analysis was quantitatively difficult due to minor x-ray peaks of Cd and In overlapping with the Te peaks. However, as indicated in Table 4.20, the EDS and XRD analysis both indicate a trend in the amount of Te in the window layers, with the one that received no pre-treatment containing the most Te and the one with the strongest pre-treatment containing the least amount of Te. Furthermore, the amount of Te in the window that received no pre-treatment roughly agrees with the solubility limit of S in CdTe derived from the study of co-evaporated films.

Table 4.20. Description of various pre-treatments applied to the CdS before CdTe deposition and heat treatment, and the results of XRD and EDS analysis after etching away the absorber layer.

Pre-treatment o	f CdS		Color of	[Te]/([S]+[Te])		
description	1 21 1		window after		from EDS	
	(μg/cm ²)	(min)	etching	(%)	(%)	
none	none	none	orange		2.5±0.5	
weak	18	10	orange/yellow	<0.6	1.5±0.5	
strong	80	30	yellow	<0.5	<0.5	

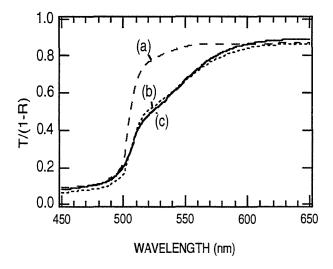


Figure 4.27. Optical transmission corrected for reflection of CdTe/CdS structures that have undergone a CdCl₂ heat treatment followed by a selective etch to remove the CdTe layers. Prior to deposition of CdTe, the CdS received the treatments defined in Table 4.20: (a) strong, (b) weak, and (c) none.

The growth of metastable or kinetically limited CdTe-CdS alloyed films with atomic compositions within the miscibility gap was demonstrated. The heat treatment of these films in the presence of CdCl₂ resulted in phase segregation. Solubility limits of Te in CdS and S in CdTe were found by measuring the atomic compositions of the wurtzite and zincblende phases within the heat treated films. The alloy compositions found in actual solar cell device structures were found to be consistent with these results. The concentration of sulfur in the absorber layer reached but did not exceed the solubility limit of S in CdTe. Pre-treatment of CdS prior to deposition of CdTe limited the diffusion of Te into the window layer. However, a window layer that did not receive pre-treatment contained Te at a concentration near the solubility limit of Te in CdS.

References Section - 4

- 4.1. R.W. Birkmire, J.E. Phillips, W.A. Buchanan, S.S. Hegedus, B.E. McCandless, W.N. Shafarman, and T.A. Yokimcus, Final Report of NREL Subcontract XN-0-10023-1, NREL, Golden, CO, 43 (March, 1993).
- 4.2. R.W. Birkmire, J.E. Phillips, W.A. Buchanan, S.S. Hegedus, B.E. McCandless, W.N. Shafarman, and T.A. Yokimcus, Annual Report of NREL Subcontract XAV-3-13170-1, NREL, Golden, CO, 84 (March, 1994).
- 4.3. R.W. Birkmire, J.E. Phillips, W.A. Buchanan, S.S. Hegedus, B.E. McCandless, W.N. Shafarman, and T.A. Yokimcus, Annual Report of NREL Subcontract XAV-3-13170-1, NREL, Golden, CO, 37 (January, 1995).
- 4.4. G.B. Harris, *Phil. Mag.*, **43**, 113 (1952).
- 4.5. H.P. Klug and L.E. Alexander, *X-ray Diffraction Procedures*, John Wiley and Sons, New York, 594 (1974).
- 4.6. O. Knacke, O. Kubaschewski, and K. Hesselmann (Eds.), *Thermochemical Properties of Inorganic Substances*, Springer-Verlag, Dusseldorf, 411 (1991).
- 4.7. B.E Warren, X-ray Diffraction, Dover Publications, New York, 260 (1969).
- 4.8. D.G. Jensen, B.E. McCandless, and R.W. Birkmire, Proc. 1996 MRS Conference, San Francisco.
- 4.9. P.V. Meyers, C.H. Liu, and M. Doty, "Method of Making Photovoltaic Cell with Chloride Dip," US Patent 4,873,198 (1989).
- 4.10. R.W. Birkmire, B.E. McCandless, and S.S. Hegedus, *Int. J. Solar Energy* 12, 145 (1992).
- 4.11. J. Britt and C. Ferekides, Appl. Phys Lett. **62**(22), 2851 (1993).
- 4.12. A. Compaan and A. Bhat, Int. J. Solar Energy 12, 155 (1992).
- 4.13. R.W. Birkmire, J.E. Phillips, W.A. Buchanan, S.S. Hegedus, B.E. McCandless, W.N. Shafarman, and T.A. Yokimcus, Final Report of NREL Subcontract XN-0-10023-1, NREL, Golden, CO, 43 (March, 1993).
- 4.14. B.E. McCandless, H. Hichri, and G. Hanket, Proc. 25th IEEE (this conference) (1996).
- 4.15. T.X. Zhou, N. Reiter, R.C. Powell, R. Sasala, and P.V. Meyers, Proc. 1st World Conference on Photovoltaic Energy Conversion, Hawaii, 103 (1994).
- 4.16. *Ullmann's Encyclopedia of Industrial Chemistry*, F. Ullmann, Weinheim, Fed. Rep. Germany: VCH Verlagsgesellschaft; Deerfield Beach, FL, VSJ Publishers, 283 (1985).
- 4.17. Kirk-Othmer Encyclopedia of Chemical Technology, (3rd Ed.), Wiley, New York, Vol. 12, 983 (1978).

- 4.18. R.W. Birkmire, J.E. Phillips, W.A. Buchanan, S.S. Hegedus, B.E. McCandless, W.N. Shafarman, and T.A. Yokimcus, Annual Report of NREL Subcontract XAV-3-13170-1, NREL, Golden, CO, 84 (1994).
- 4.19. B.E. McCandless, Y. Qu and R.W. Birkmire, Proc. 1st World Conf. on Photovoltaic Energy Conversion, 107 (1994).
- 4.20. G.B. Harris, Phil. Mag. 43, 113 (1952).
- 4.21. J. Saraie, H. Kato, N. Yamada, S. Kaida, and T. Tanaka, *Phys. Stat. Sol.* (a) **39**, 331 (1977).
- 4.22. A.F. Fahrenbruch, "Ohmic Contacts and Doping of CdTe Solar Cells," *Solar Cells* **21** 399 (1987).
- 4.23. Y.S. Tyan, "Semiconductor devices having improved low-resistance contacts to p-type CdTe and method of preparation," US Patent 4,319,069 (1980).
- 4.24. H. Uda, S. Ikegami, and H. Sonomura, "Te-metal contact on evaporated CdTe film for a CdS/CdTe solar cell," *Sol. Energy Mater.* **35**, 293 (1994).
- 4.25. Zhou, T.X, "Fabrication of Stable Large Area Thin Film CdTe Photovoltaic Modules," NREL Subcontract ZR-1-11059-1, Final Technical Report (1995).
- 4.26. A. Fahrenbruch and J. Sites, Personal Communication.
- 4.27. G. Stollwerk and J.R. Sites, "Analysis of CdTe Back-Contact Barriers," Proc. 13th European PVSEC (1995).
- 4.28. T.X. Zhou, N. Reiter, R.C. Powell, R. Sasala, and P.V. Meyers, "Vapor Chloride Treatment of Polycrystalline CdTe/CdS Films," Proc. 1st World Conf. on Photovoltiac Energy Conversion, 103 (1994).
- 4.29. B.E. McCandless, Yi Qu, and R.W. Birkmire, "A Treatment to allow contacting CdTe with different conductors", Proc. 1st World Conf. on Photovoltaic Energy Conversion, 107 (1994).
- 4.30. R.W. Birkmire, B.E. McCandless, and S.S. Hegedus, *Int. J. Solar Energy* **12**, 145 (1992).
- 4.31. I. Clemminck, M. Burgelman, M. Casteleyn, J. De Poorter, and A. Vervaet, 22nd IEEE PVSC, Las Vegas, 1114 (1991).
- 4.32. M.E. Özsan, D.R. Johnson, D.W. Lane, and K.D. Rogers, 12th EC PVSEC, Amsterdam, 1600 (1994).
- 4.33. D.M. Oman, K.M. Dugan, J.L. Killian, V. Ceekala, C.S. Ferekides, and D.L. Morel, *Appl. Phys. Lett.* **67**, 1896 (1995). p. 1896.
- 4.34. S. Nunoue, T. Hemmi, and E. Kato, J. Electrochem. Soc. 137, 1248 (1990).
- 4.35. D. Bonnet, Phys. Stat. Sol. (a) 3, 913 (1970).
- 4.36. R. Hill and D. Richardson, *Thin Solid Films* 18, 25 (1973).

- 4.37. K. Ohata, J. Saraie, and T. Tanaka, Japan. J. Appl. Phys. 12, 1641 (1973).
- 4.38. S.K.J. Al-Ani, M.N. Makadsi, I.K. Al-Shakarchi, and C.A.Hogarth, J. Mat. Sci 28, 251 (1993).
- 4.39. B.E. McCandless and R.W. Birkmire, Solar Cells 31, 527 (1991).
- 4.40. R.W. Birkmire, H. Hichri, R. Klenk, M. Marudachalam, B.E. McCandless, J.E. Phillips, J.M. Schultz and W.N. Shafarman, 13th NREL PV Program Meeting (1995), AIP Conf. Proc. **353**, 353 (1996).
- 4.41. B.E. McCandless and S.S. Hegedus, 22nd IEEE PVSC, Las Vegas, 967 (1991).

5.0 ABSTRACT

This report describes results achieved during the third phase of a four year subcontract to develop and understand thin film solar cell technology related to CuIn_{1-x}Ga_xSe₂, a-Si and its alloys and CdTe. Accomplishments during this phase include:

- fabrication of 15% efficient $CuIn_{1-x}Ga_xSe_2$ cells over a wide range of Ga compositions (x \leq 0.5).
- fabrication of uniform single phase Cu(Ga_xIn_{1-x})Se₂ films and solar cells from the selenization of Cu-In-Ga precursors with the optical bandgap and device results expected for the precursor composition.
- development of μc n-layers which have allowed fabrication of a-Si devices with FFs as high as 72%.
- completion of the analysis and measurements that quantify the improvement in performance of a-Si solar cells due to optical enhancements from a wide range of TCO texture substrates and back reflectors.
- development of uniform and reproducible vapor phase CdCl₂ treatments for CdTe/CdS films that have translated into greater consistency in device performance.
- development of a HCl vapor treatment of CdTe/CdS films that promote changes in the structure of the films similar to those treated with CdCl₂.

In addition to these in-house activities, IEC has maintained an active role in the collaboration with over ten different PV and thin film research and development organizations.

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