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High-Performance Porous Silicon Solar Cell Development

Final Report
1 October 1993 - 30 September 1995

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1617 Cole Boulevard
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ABSTRACT

The goal of the program was to demonstrate use of porous silicon in new solar cell structures. Porous silicon technology has been developed at Spire for producing visible light-emitting diodes (LEDs). The major aspects that we have demonstrated are the following:

- Porous silicon active layers have been made to show photovoltaic action
- Porous silicon surface layers can act as antireflection coatings to improve the performance of single-crystal silicon solar cells
- Porous silicon surface layers can act as antireflection coatings on polycrystalline silicon solar cells

One problem with the use of porous silicon is to achieve good lateral conduction of electrons and holes through the material. This shows up in terms of poor blue response and photocurrents which increase with increasing reverse bias applied to the diode.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

Page

LIST OF FIGURES (Concluded)

LIST OF TABLES

1 INTRODUCTION AND SUMMARY

1.1 Porous Silicon

1.1.1 Background

Spire has developed an electrochemical processing technique for preparing silicon samples with nanostructural carrier confinement properties, e.g. porous silicon.[1,2] Quantum size effects in the material apparently lead to an increase in the optical gap energy, corresponding to the energy of carrier confinement. We have used this unique material to demonstrate photoluminescent emission throughout the visible spectrum under laser excitation. We have observed high intensity red light emission from samples with aqueous contacts. Most important, we have prepared stable visible light emitting diodes.[1] Since emission wavelengths throughout the visible spectrum have now been demonstrated with these porous silicon samples, it is suggested that the material is likely to be an ideal candidate for the development of new solar energy conversion devices, accurately matched to the terrestrial solar spectrum. Our objective was to build upon the exciting results of our silicon LED efforts, to produce high-performance silicon based photovoltaic devices, primarily by tailoring the properties of np junctions in the quantum-confined silicon structures.

1.1.2 Electrochemical Processing of Silicon

All of the silicon wafers etched in our processing laboratory in previous efforts are mounted in a specially designed jig.[3] This jig has a circular opening at the front to allow the samples to make full contact with the etching solution; an O-ring protects the backs of the wafers from the liquid. The electrical contact is made to the back of each wafer. The jig is lowered into the solution of hydrofluoric acid in ethanol, and current levels of 2 to 25 mA/cm^2 can be supplied for varying amounts of time. The anodic etching system is diagrammed in Figure 1.

It has been observed that the surfaces of the samples develop a discoloration due to the etching, which ultimately approaches black as the processing continues. This discoloration is due to the altered surface optical properties of the porous silicon films, which are on the order of 1 μm thick. When the surfaces of the etched wafers are scraped with a blade, a yellowish-brown powder is typically obtained, indicating a shift of the absorption edge of our material into the visible.

1.1.3 Application to Solar Cells

At present, the main approaches to the production of high efficiency solar cells rely on silicon, the workhorse of the photovoltaics industry, although GaAs is also given much consideration. Efficiencies exceeding 20% have been achieved with both materials,[4] but costs still remain above competitive levels. GaAs possesses a direct bandgap which provides strong optical absorption and hence a short absorption length requirement of only a few microns; however, GaAs is a very costly material, and a non-absorbing GaAs substrate must be provided for mechanical support. Silicon is abundant in the earth's crust and therefore less expensive than GaAs, but its poor optical absorption properties (basically an indirect bandgap) lead to the requirement of very thick solar cells. Consequently, high efficiency silicon solar cells require complicated and costly processing procedures. However, since porous silicon material exhibits such intense photoluminescence it appears as if this form of silicon has acquired a direct bandgap.

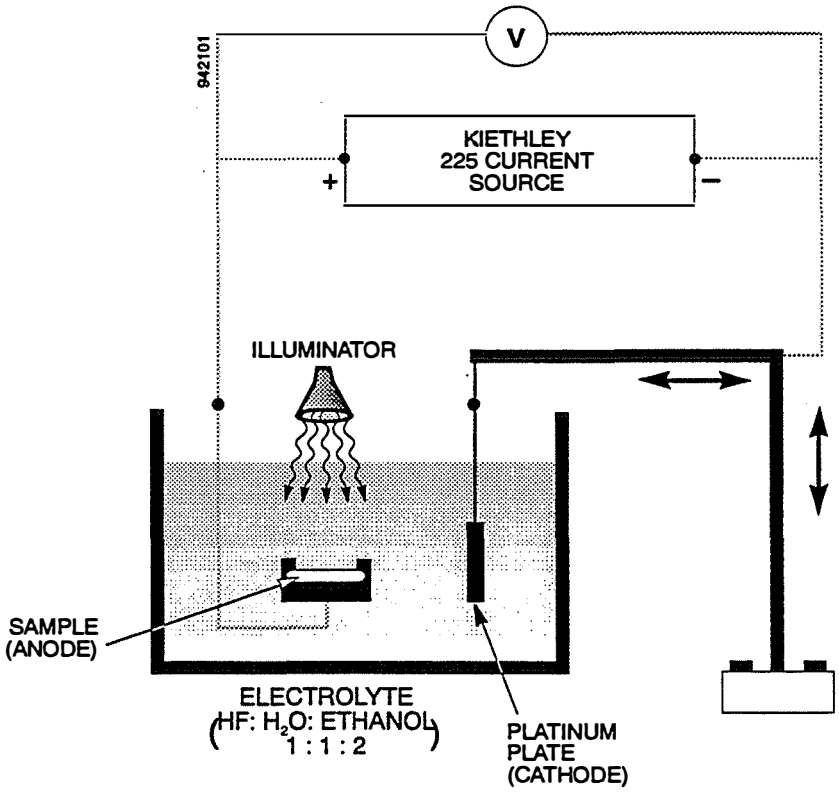

Figure 1 *Schematic diagram of the anodic etching system used at Spire for fabricating porous silicon samples.*

The possibility therefore exists that by a relatively simple, quick, low cost etching process, a thin film of highly absorbing silicon can be formed, with a band edge and absorption length comparable to that of expensive GaAs. Development of solar cell structures in this new form of silicon could lead to enhanced single junction cells, and even more interesting, all silicon tandem junction cells.

1.1.4 Photovoltaic Effects in Porous Silicon Samples

We are presently aware of three reports of photovoltaic responses in porous silicon. Anderson and co-workers at SUNY-Buffalo[5] have prepared photodiodes by placing an aluminum contact onto the surface of electrochemically processed p-type silicon, with the etched film exceeding 4 μm in thickness. They determined a quantum efficiency of 97%, which they attribute to excellent light trapping characteristics of the porous silicon, and low surface recombination velocity at the surface of the quantum confined material. However, the open circuit voltage was only about 0.2V. The current-voltage characteristics indicated a large series resistance effect, which caused a reduced short circuit current; a reverse bias of about -1.5V was needed to approximately saturate the photogenerated current.

Smestad, Kunst and Vial[6] used a platinum needle to make a contact to electrochemically etched p-type silicon, and report a photovoltaic response. Under simulated AM1.5 conditions, V_{oc} was limited to 0.36V, although Smestad has earlier suggested[7] that illuminated porous silicon should yield higher photovoltages than bulk silicon. Low values of open circuit voltages are usually due to the presence of large dark currents,[8] which is consistent with our determination of significant surface

state densities at the heterojunction interface formed on porous silicon.[2] We therefore contend that a different approach is necessary to produce high efficiency solar cells with porous silicon material.

Recently, a group at NREL described their efforts with applying porous silicon technology to the preparation of photovoltaic devices.[9] Their approaches included using the porous silicon for surface texturing to enhance light trapping, using the wider bandgap of porous silicon to provide a surface field to reduce recombination losses, and seeking to have photoluminescence in porous silicon down-convert incoming ultraviolet light to visible for better response. Indeed they found that the presence of porous silicon greatly decreased the reflectivity of silicon wafers, bringing it as low as 1.5% at 500 nm. However, they also determined that the presence of porous silicon actually reduced the minority carrier lifetime for cells having p and n point contacts on the rear surface. No attempts to form junction diodes in the porous silicon were reported in that work.

At Spire, we have tested our ITO/porous silicon diodes for photovoltaic response. We determined that a photocurrent in such devices was only generated if a reverse bias is applied.[10] At zero volts (short circuit), there is zero current. We explained this problem in terms of two separate barriers to current flow, one at the silicon/porous silicon interface, and the other at the ITO/porous silicon interface. The difficulty lies with electron transport. Because the effective bandgap of porous silicon is larger than that of bulk silicon, minority electrons generated in the bulk cannot reach the ITO without the application of reverse bias. Thus a different structure is required.

1.2 Program Approach

This program relies on forming a contact to a thin region of non-QC porous silicon on the surface of the wafer, such material being present above quantum confined porous silicon. It has been shown that heavily p-type silicon etches in a different manner than material with lower doping concentrations: the etching proceeds so rapidly, due to the high density of holes available, that a very coarse structure featuring micron sized "wires' results after etching.[11] Such material maintains the bandgap of bulk silicon, *i.e.,* there is no quantum confinement effect. Consequently, one can make an ohmic contact to this heavily doped p-type etched silicon as easily as to bulk material. Below this heavily doped region, we need lightly p-type silicon, followed by lightly n-type silicon (the substrate). The QC-porous silicon is formed in this lightly doped region.

Therefore, we shall start with an n-type substrate. We shall implant boron into the surface at energies which give a graded concentration, from high to low with distance into the wafer. Thus a pn junction is created.

The sequence for anodizing through the pn junction to form a quantum confined junction is shown in Figure 2. The surface p^+ region etches rapidly, without forming any quantum confined structures. However, when the lightly p-type region is reached, standard porous silicon is formed. Basically, the chemistry which occurs at the surface of the silicon requires that positive charges (holes) be transported to the surface. Since the hole concentration in n-type silicon is far too small, the etching ceases when we arrive at the junction. We photogenerate the required holes for etching the n-type substrate by exposing the sample to ultraviolet light illumination. Once the pn junction has been passed, illumination is required until we have etched sufficient material.

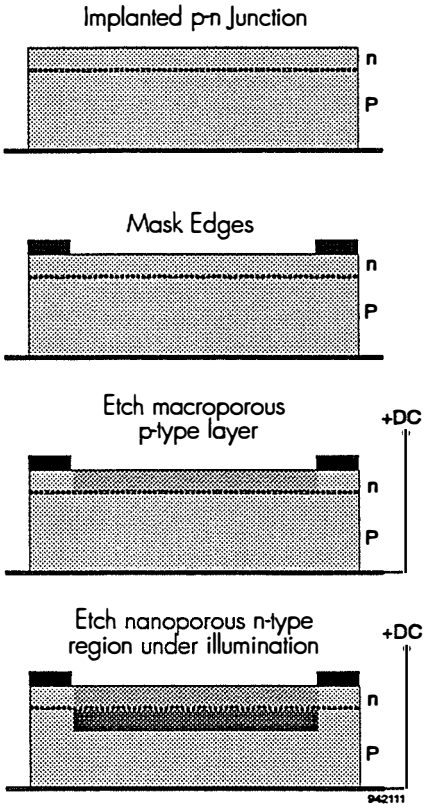

Figure 2 *Sequence for electrochemical etching through an ion-implanted junction in silicon.*

Figure 3 shows the desired structure of the quantum wires in detail. It is expected that incoming photons will undergo multiple reflections before being absorbed in the wires. Hence, the placement of the pn junction relative to the depth of the etch is a critical parameter in these devices.

1.3 Program Objectives

The overall objective was to determine the advantages inherent in harnessing the porous silicon technology developed at Spire for producing enhanced silicon-based solar cell structures. The approach is based upon Spire's outstanding results in the development of porous silicon LEDs. The final theoretical improvement in single cell response can be judged from the work of Nell and Barnett, shown in Figure 4, which gives the AM1.5G solar spectrum, and shows that while the maximum efficiency of bulk silicon is 24%, porous silicon with a bandgap of 1.5 eV could produce a conversion efficiency as high as 28%.[12]

The first-year tasks concentrated on the formation of np junctions in bulk crystalline silicon. Spire developed the technology for the formation of quantum confined structures with increased optical gaps and fabricated pn junction solar cells. Several techniques to provide low-resistance ohmic contacts to the surface of porous silicon were explored and a preliminary evaluation of the properties of fabricated devices was carried out. In a single cell structure, anodization is required to proceed through the pn junction formed in the silicon wafer. The objective was to determine the proper electrochemical environment for accomplishing this task. Two critical parameters are physical location (depth below surface) of the pn junction, and the thickness of the porous silicon film.

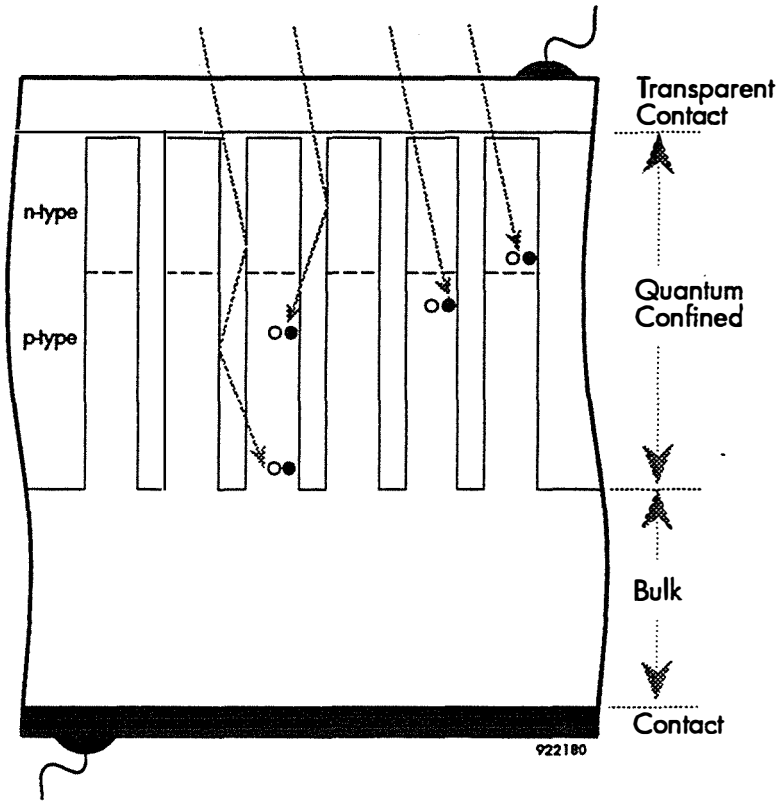

Figure 3 *Schematic of porous silicon solar cell.*

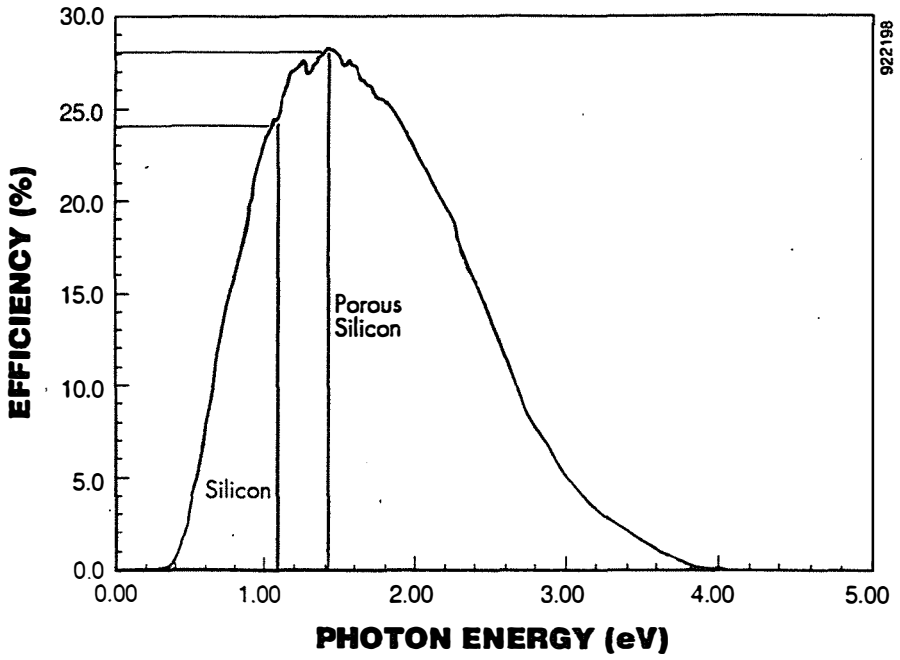

Figure 4 *Single junction solar cell efficiencies for the standard AM1.5 global spectrum, comparing bulk silicon and porous silicon.*

We explored methods for making an ohmic contact to the surface p-type material. We investigated standard metal film contacts that are known to work for bulk p-type silicon, such as titanium/palladium/gold (three layer metallization) and aluminum. The goal was to minimize any voltage losses at this interface due to undesirable Schottky barrier formation.

In year two we continued to optimize solar cells using porous silicon pn junctions, and then devoted our efforts to exploring use of porous surface layers to act as antireflection coatings on single- and poly- crystalline silicon cells.

2 RESULTS AND DISCUSSION

2.1 Junction Formation

We began our research by obtaining fifty commercial N-type silicon substrates for fabricating a batch of preliminary porous Si-based device structures on them. These wafers had a resistivities of between 2.6 to 2.8 Ω-cm. These resistivity levels correspond to a donor concentration of 2 to 3×10^{15} cm^{-3} in the substrates.

Our first task was to produce pn silicon junction for solar cell fabrication structures. Therefore, we used Spire's standard ion implantation procedures to create a highly doped N-type layer at the rear surface to assure an ohmic contact to the back. Phosphorous ions were implanted at two depths to provide high carrier concentrations. Our baseline condition was two doses of 5×10^{15} P^+/cm^2 implanted first an energy of 50 keV, and then at 150 keV. The calculated phosphorus implantation profile is shown in Figure 5.

To form the a P-on-N junction, we next introduced boron acceptors into the top surface of the wafers, also by ion implantation. Three boron implants were used, each with a dose of 5×10^{15} B^+/cm^2. The first implant at 25 keV brings the surface concentration of the first 200 nm to greater than 4×10^{20} cm^{-3}. Such highly P-type material will not form a quantum confined layer, but will have a good electrical conductivity enabling formation of ohmic contact. The other two boron implants at higher energies of 75 and 150 keV produce the P^- layer which would become QC porous silicon, along with the N^- material just below it. The simulated depth profile of the triple implant boron in silicon is shown in Figure 6.

Following the phosphorous an boron implantation, the wafers were then annealed in nitrogen at 900°C for 25 minutes to recover the implant damage and to activate the dopants, and thus form a PN junction structures.

After the PN junctions were produced, the next step was to prepare these samples for electrochemical etching to produce porous Si surface layers. In order to achieve a uniform porous Si material, it is required that an ohmic contact be made to the entire rear surface of the substrates. Therefore, we used an in-house electron-beam evaporator to metallize the rear surface. Based on our experience in forming ohmic contacts to n-type silicon, we used a triple metallization technique in which a 1000Å of Ti, 1000Å of Pd, and 5000Å of Au metal were evaporated on the rear side, respectively. After metal deposition, the wafers were sintered in a furnace at 400°C in nitrogen to ensure the formation of rugged ohmic contacts.

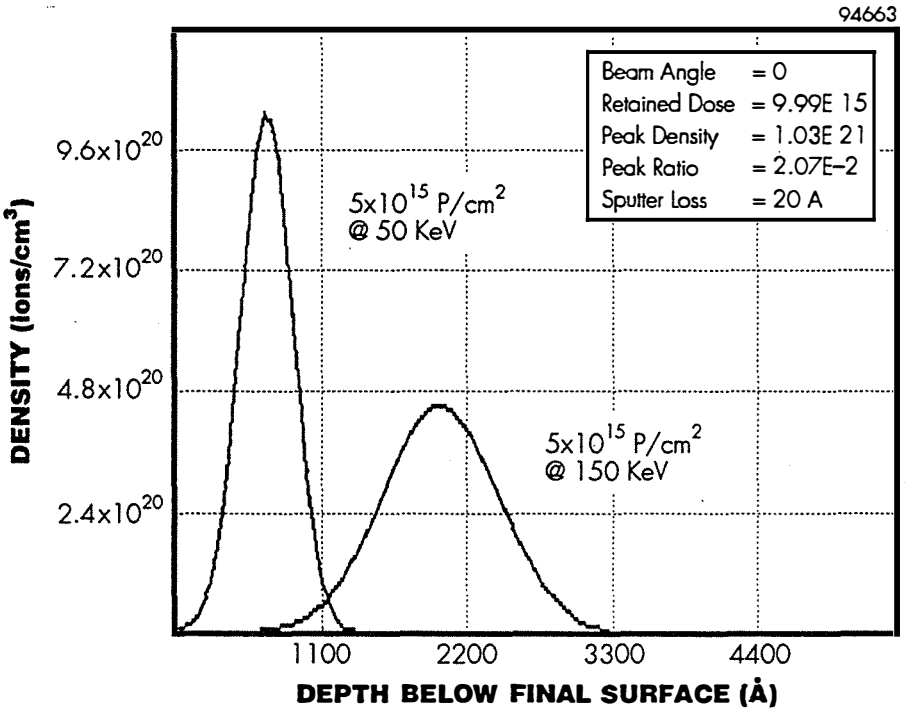

Figure 5 *Profile of phosphorus implantation in n-type silicon to provide ohmic contact.*

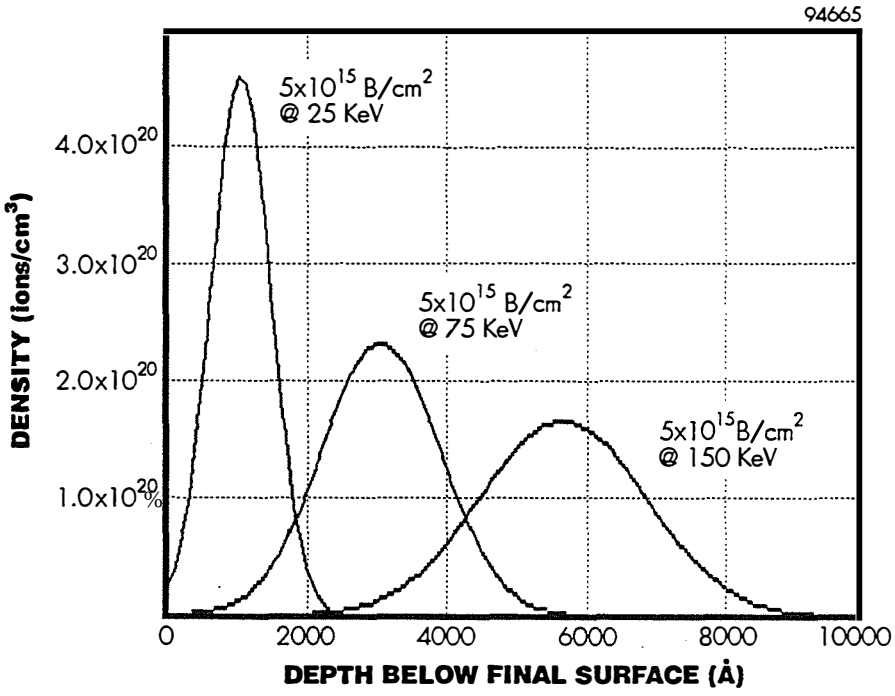

Figure 6 *Profile of boron implantation in n-type silicon to provide pn junction prepared by ion implantation.*

2.2 Porous Silicon Formation by Anodic Etching

In this task, we extensively studied the optimization of anodic etching parameters for producing porous homojunction p-on-n Si samples. The electrolyte used was a 1:1:2 mixture of $HF:H_2O:C_2H_5OH$. We attempted to optimize three major parameters, *e.g*, anodization current (current density), anodization time, and the illumination condition under which the samples were etched. Table I gives a list of the four-inch diameters p-on-n Si wafers which were anodically etched under varying conditions. These wafers were etched using the system described previously in Section 1.

As indicated in Table 1, the samples were etched with an applied current of 50 or 100 mA for periods of up to three hours. In several instances, we began anodization of the sample initially under room light only, and then continued with etching under illumination from an ultraviolet lamp. This etching sequence was used because we had anticipated that the p-type surface layer would be readily etched in dark (or room light) while the n-type material below would require UV illumination to generate holes needed for the chemical reaction. We monitored the voltage between the cathode (C) and anode (A) during the etching procedure to determine the anodization rate of samples. We observed that the p-type surface layer begins to etch at a relatively high rate under room light (indicated by low V_{AC}), but after about six minutes the etch rate decreases drastically (indicated by very high V_{AC}). We speculated that the sudden increase in the anode-cathode voltage (V_{AC}) was indicative that the p-type layer had been etched and the n-type layer, which does not etch in room light, had been exposed. Hence, at this point we turned the UV lamp on and continued the electrochemical etching. Indeed we observed that soon after the UV illumination the V_{AC} dropped drastically and the sample began to etch, again.

Photoluminescence study of the etched samples revealed that macroporous P^+ layer does not emit significant visible light while the nanoporous N-type layer underneath emits a very bright yellow/orange light. This was further confirmed by physically removing the P^+ layer and observing the luminescence of the N-type layer.

2.3 Initial Device Fabrication and Testing

As a first effort to study the photovoltaic application of porous Si-based devices, we fabricated and compared the behavior of two groups of devices. In the first group, which itself consisted of two different structures (ITO/porous Si heterojunction and np porous silicon homojunctions) we initially formed a porous Si surface layer and then deposited a metallic contact on the top. In fabricating the second group of devices, we first formed an ohmic contact to the bulk single-crystal surface layer and then anodically etched the samples to form porous silicon layers.

2.3.1 Characterization of Devices with Contacts Deposited After Anodization

2.3.1.1 Characterization of Heterojunction N-on-P ITO/Porous Silicon Devices

The first devices we tested for photovoltaic behavior were ITO on p-type porous Si heterojunction LEDs. Previously, we had demonstrated for the first time visible light emission from these structures. These diodes had been formed by depositing ITO (an N-type wide-band gap semiconductor) onto the surface of anodically etched p-type silicon. The electrical characterization

Table 1 *List of the wafers and anodic etching conditions used to produce porous P-on-N silicon structures.*

Wafer Number	Anodization Current (mA)	Anodization Time (min.)		
		Under Ambient Light	Under High Intensity UV	Under Low Intensity UV
156 - 1A	100	2.0	28.0	–
156 - 2A	100	6.5	2.5	–
156 - 3A	100	6.0	114.0	–
156 - 4A	100	35.0	10.0	–
156 - 5A	100	5.0	115.0	–
156 - 6A	100	120.0	–	–
156 - 7A	50	5.0	–	90
156 - 8A	100	10.0	–	100
156 - 9A	100	–	–	180
156 - 10A	100	–	30.0	–
156 - 11A	100	–	30.0	–
156 - 12A	100	–	30.0	–
SUD - 1A	100	–	37.0	–
SUD - 2A	100	–	60.0	–
SUD - 3A	100	–	15.0	–

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of these devices indicated no photocurrent under incandescent illumination unless a reverse bias was applied to the device. Dark and illuminated current-voltage (I-V) characteristics for a representative ITO/ porous silicon device are given in Figure 7. It can be seen that the photocurrent increases in magnitude as the light intensity is increased, and that the photocurrent saturates at about -2V reverse bias. Figure 7 also shows the I-V characteristics for a device prepared on the same substrate, but in a region of the wafer which had not been etched. There is clearly a photocurrent at zero bias for ITO/bulk silicon devices.

Figure 8 shows the model for this behavior. For bulk silicon devices, the presence of surface states at the SiO_2/p-silicon interface affects the band bending, and results in a potential barrier of 0.25 eV in the silicon. A photovoltaic effect is observed because the electric field at the interface drives photogenerated minority carriers (electrons) from the silicon into the ITO, where they are collected. This result is similar to an earlier report on ITO/p-silicon solar cells.[13]

The situation is quite different for the ITO/porous silicon devices. Hence the quantum confinement energy shifts the positions of the states in the bands, effectively eliminating the conduction band states that would normally allow the passage of electrons to the ITO at zero applied bias. Holes are also reflected from a barrier in the valence band, but this barrier is beneficial. According to the band model of Figure 8, both holes and electrons are constrained to move into the bulk silicon, where they are mutually annihilated. Thus no photovoltaic effect is manifested. In principle, this problem can be overcome by placing a pn junction in the porous silicon, rather than creating a heterojunction on the surface with ITO. The elimination of the ITO/porous silicon interface is expected to allow a photocurrent to pass at zero bias.

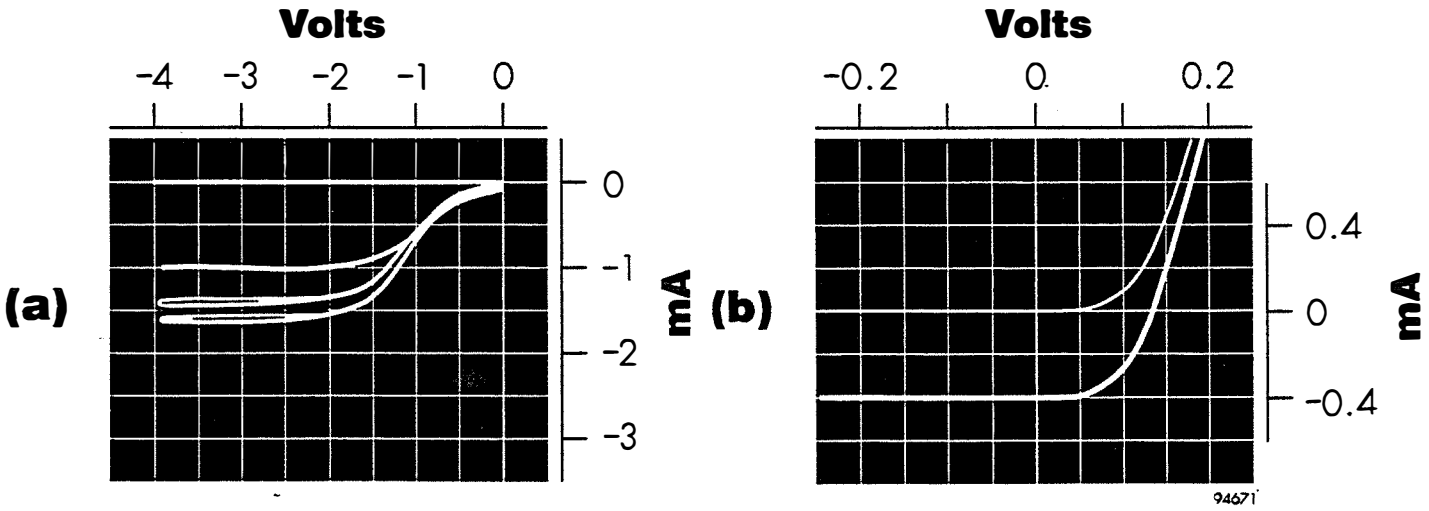


Figure 7 *Effect of white light illumination on the current-voltage characteristics of ITO-contacted silicon devices. a) Junction formed with porous silicon does not exhibit a photocurrent at zero bias; b) junction formed on bulk silicon generates photocurrent at zero bias.*

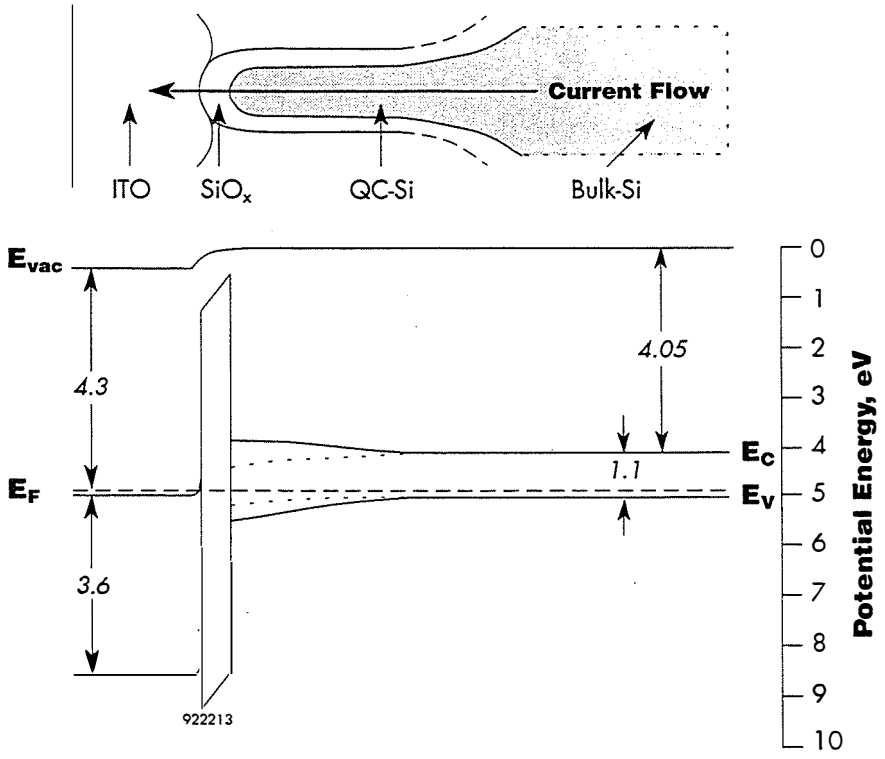


Figure 8 *Energy band model for porous silicon in contact with ITO.*

2.3.1.2 Characterization of Preliminary Homojunction P-on-N Porous Silicon Devices

Following the characterization of ITO/porous Si heterojunction cells, we proceeded to deposit metal dot contacts onto the surface of the PN homojunction porous Si structures described in Section 2.2. The contacts were formed by triple Ti/Pd/Au metal evaporation onto the sample through a shadow mask with circular windows 1.5 mm^2 in diameter. These devices were illuminated with an incandescent light. Indeed, a photovoltaic effect was observed. The current-voltage characteristics are shown in Figure 9. First, it is clear that in the dark, the device exhibits rectifying behavior that can be expected from a pn junction. Dark current levels in reverse bias are below the instrument resolution limit on this scale. The photocurrent under white light illumination increases as the light intensity is raised. For the porous silicon device shown, a photocurrent of about 2 μA was generated. The largest open circuit voltage that was measured was 0.11 volts. The low value of V_{oc} is consistent with the small photocurrent.

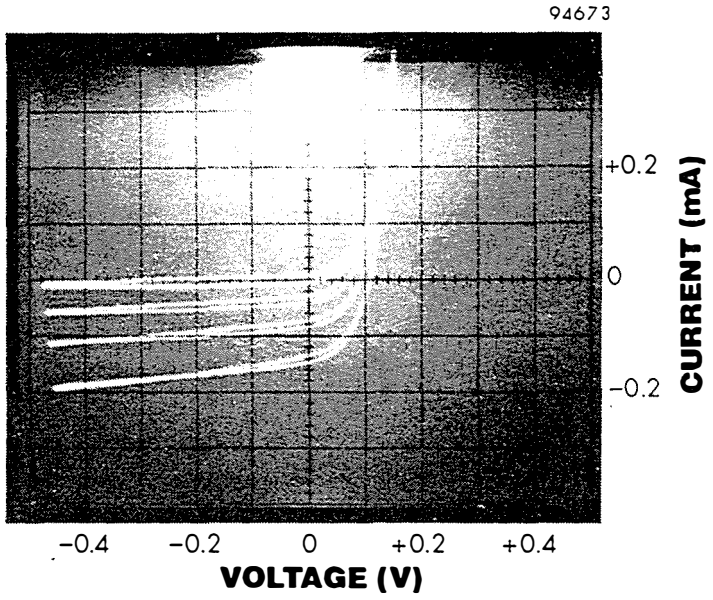


Figure 9 *Current-voltage characteristics of porous silicon diode exhibiting photovoltaic characteristics.*

We explain the situation as follows. The metal contact is very thick, and cannot pass any light. The only light that is available for generating a photocurrent must be absorbed in the regions around the opaque contact. However, the surface p^+ region is composed of vertical wires, making horizontal carrier transport a difficult problem. We suspect that the only photocurrent that we are seeing is generated by light which is scattered under the contact, and absorbed in material below the metal.

A possible way to improve this situation would be to provide a transparent contact material over the entire p-type surface. This conductor would allow the current flowing vertically to be collected and moved to the side, across the surface. We point out that our initial result seems quite promising; in contrast to the ITO/porous silicon devices, we now see a photocurrent at zero bias.

2.3.1.3 Characterization of Devices with Contacts Deposited Before Anodization

As an alternative approach, we prepared several bulk silicon wafers with top metal contacts prior to any electrochemical treatment. Figure 10 shows a dark and illuminated (white light) characteristics of a representative device. Each device was fabricated with a circular Ti/Pd/Au dot as a non-transparent contact. The active area of these devices was 0.45 mm^2. Consideration of the characteristic indicates that there is no measurable shunt leakage current.

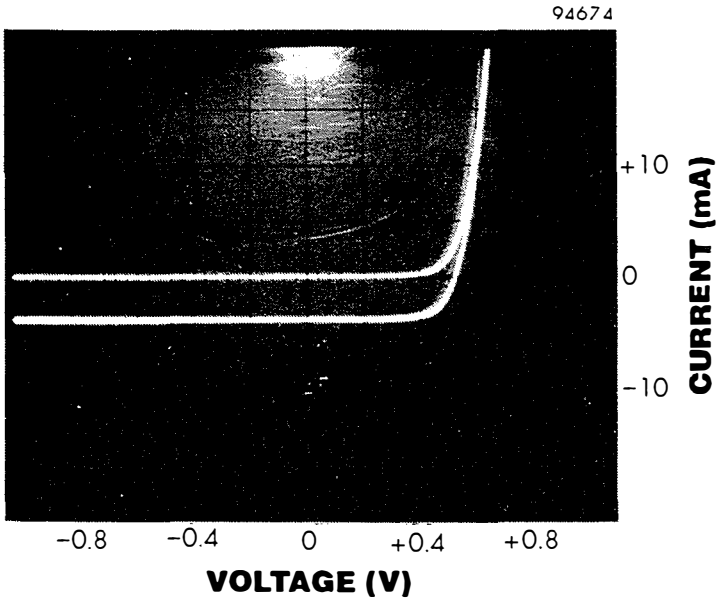


Figure 10 *Current-voltage characteristics of bulk implanted silicon solar cell, with Ti/Pd/Au contact to top surface p-layer.*

After testing was complete, these devices were subjected to our standard electrochemical etching procedure. The metal contact was not disturbed by the etching. After the procedure was completed, the samples were dried, and re-evaluated. They were tested under the same white light intensity as before. We found that the photocurrent had increased markedly. This is shown in Figure 11. There is still no measurable shunt leakage. However, the fill factor shows some degradation.

We then tested the selected devices with our calibrated solar simulator, using AM1.5 (global) illumination. The results are shown in Figures 12 and 13. The bulk silicon device is shown in Figure 12. The measured short circuit current, 17.42 mA/cm^2, is low because no attempt was made to provide an anti-reflection coating. The fill factor was 66.3%, indicating that we are having some series resistance problems. The measured efficiency was at 6.4%. It is clear that we have not optimized our processing at this stage. On the other hand, Figure 13 shows the results for a device which had the surface converted to porous silicon. The sample has a short circuit current of 30.07 mA/cm^2, which appears to be related to the light-trapping properties of porous silicon. With this larger photocurrent, we measure an open circuit voltage of 0.563V. However, the fill factor for this cell is reduced to 51.9%. It is not clear what is responsible for this reduction, but it was found for majority of devices we tested. The measured efficiency of the best device with the porous silicon surface, measured under AM1.5 (global) conditions, was 8.79%.

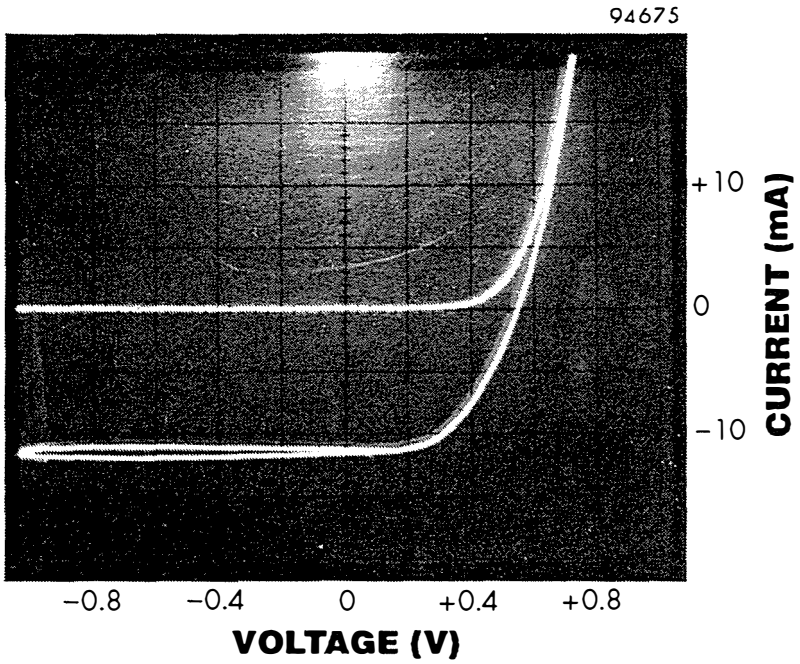


Figure 11 *Current-voltage characteristics of implanted silicon solar cell after formation of porous silicon on upper surface.*

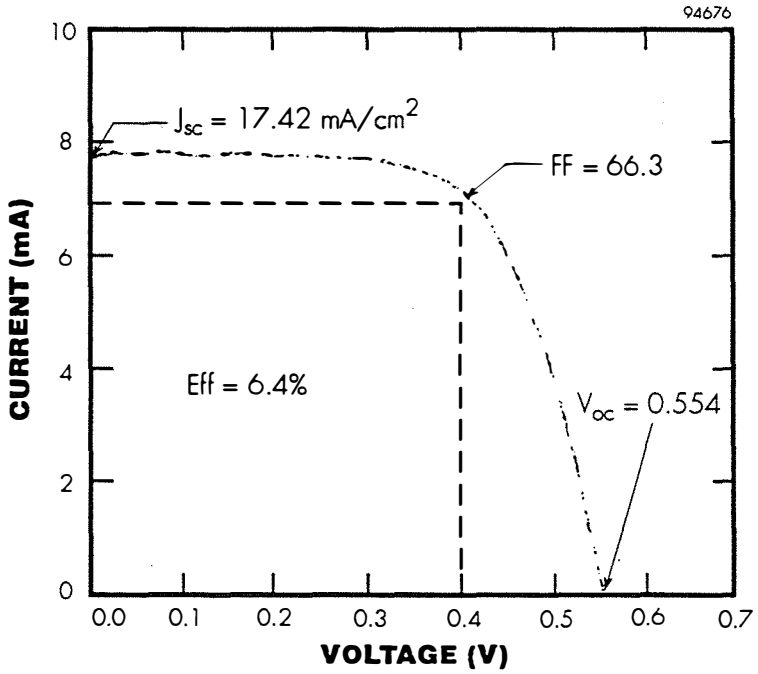


Figure 12 *Simulated AM1.5 (global) response of bulk silicon solar cell.*

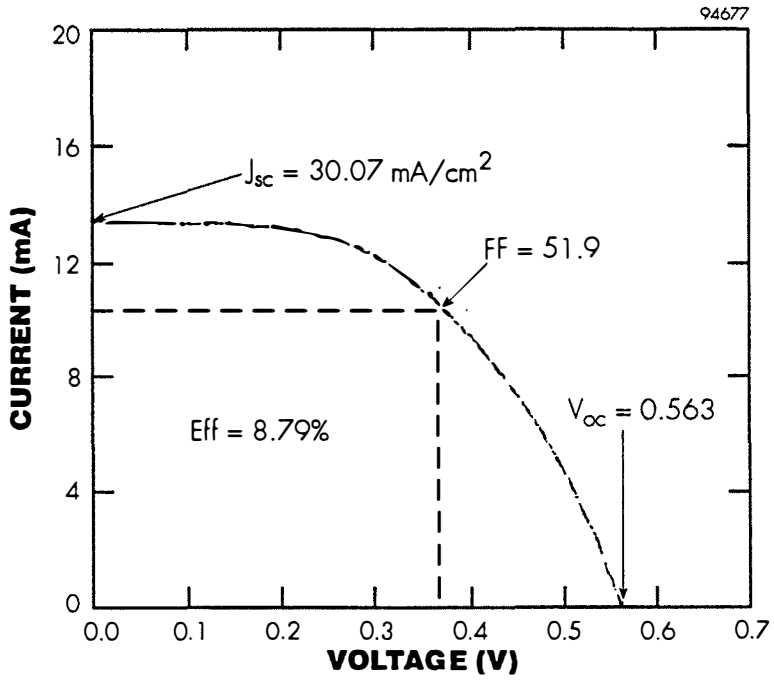


Figure 13 *Simulated AM1.5 (global) response of silicon solar cell with porous silicon surface.*

We then measured the spectral response and the reflectance of the two types of devices. Figure 14 shows these characteristics for the bulk silicon device. The reflectance is in the range of 30 to 40%, which causes a significant reduction in the external quantum efficiency. For comparison, Figure 15 shows these characteristics for the device with the porous silicon surface. The reflectance throughout most of the visible region has been reduced to 10% or less. The internal quantum efficiency is at the 90% level from about 600 to 1000 nm. Therefore, we have shown that porous silicon makes an effective anti-reflection coating for silicon solar cells.

It should be noted that the spectral response of the cell with the porous silicon surface is basically similar to any bulk silicon solar cell. Therefore, most of the current is being generated in the bulk substrate material.

Finally, we measured the dark I-V characteristics of both types of devices. To avoid series resistance problems, we measured V_{oc} vs J_{sc} at various illumination levels. The results are shown in Figures 16 and 17. Notice that the two characteristics are basically identical. In fact, the n=1 branches of both characteristics yield values of J_{01} which are 4.7 and 5.2 x 10^{-12} A/cm^2. Therefore, we find that our electrochemical processing procedure does not appear to degrade the lifetime of the carriers at the front surface of the diodes. This seems plausible if the porous silicon indeed has a larger band gap than the bulk material, leading to the formation of an effective minority carrier mirror.

It should be noted that the spectral response of the cell with the porous silicon surface is basically similar to any bulk silicon solar cell. Therefore, most of the current is being generated in the bulk substrate material.

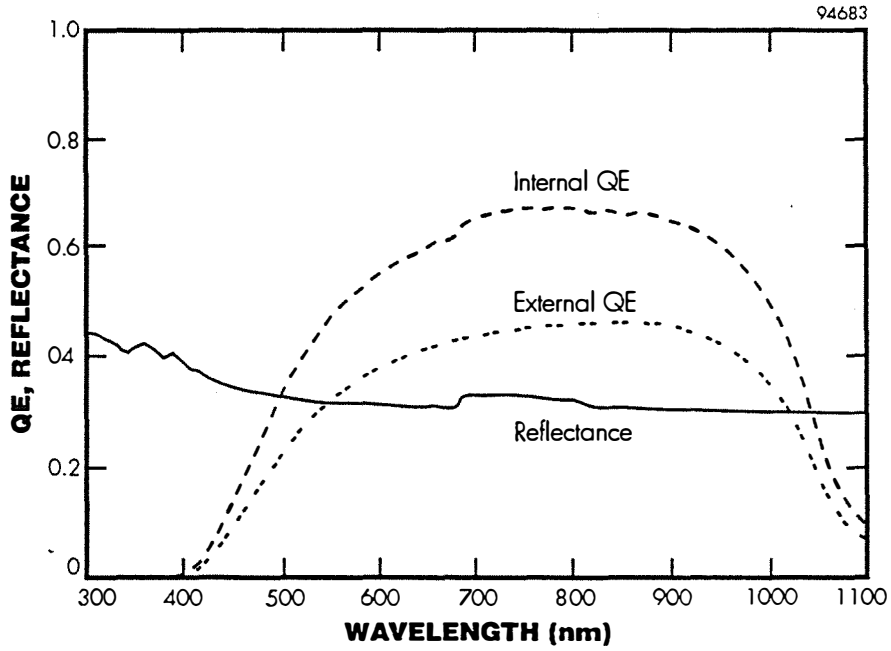


Figure 14 *Measured optical reflectance and quantum efficiency spectra for bulk silicon solar cell.*

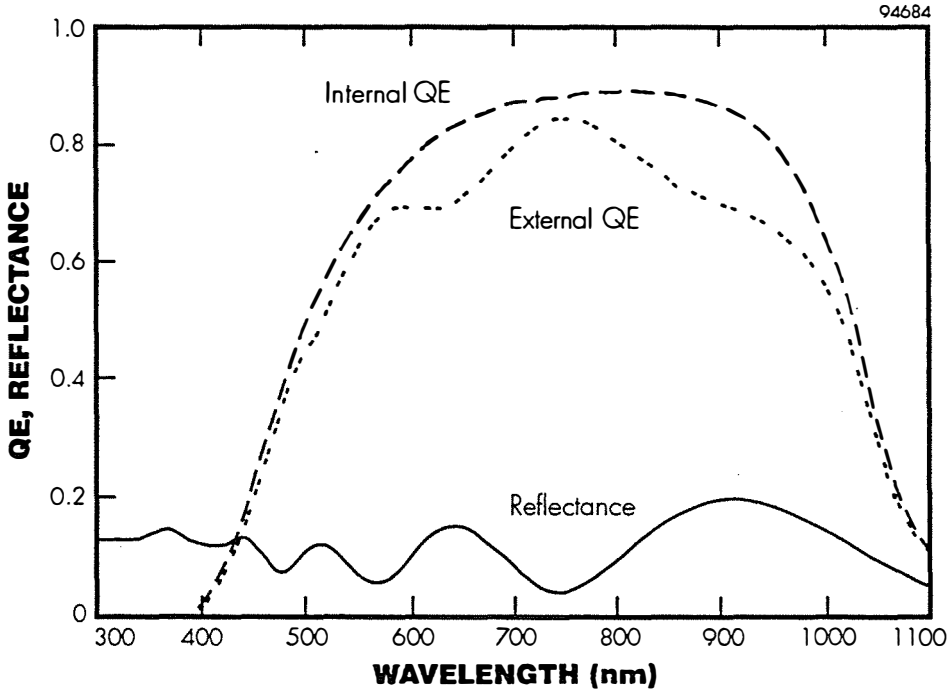


Figure 15 *Measured optical reflectance and quantum efficiency spectra for a solar cell with porous silicon surface layer.*

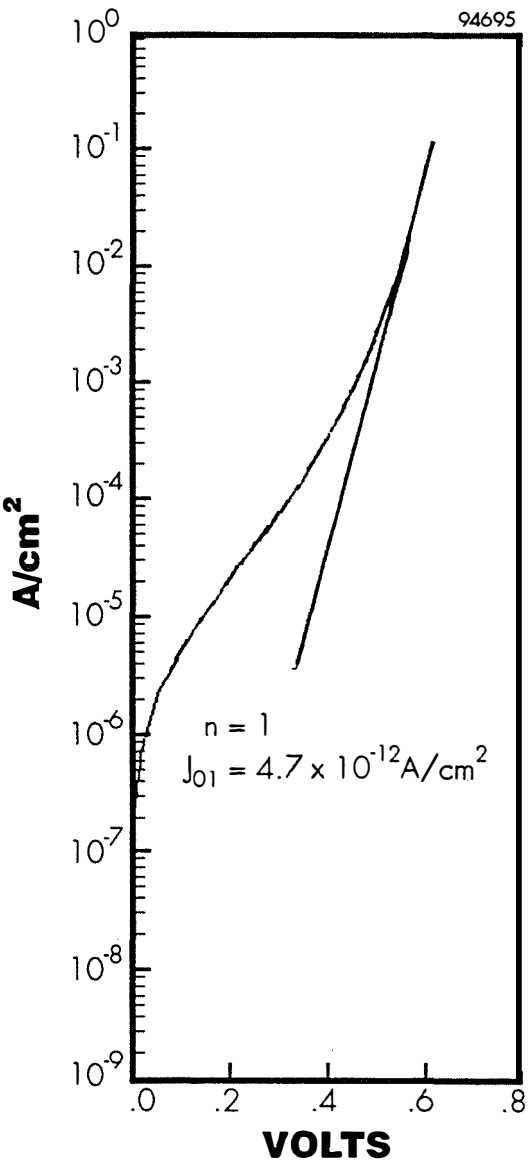


Figure 16 *Dark current-voltage characteristic of bulk silicon solar cell.*

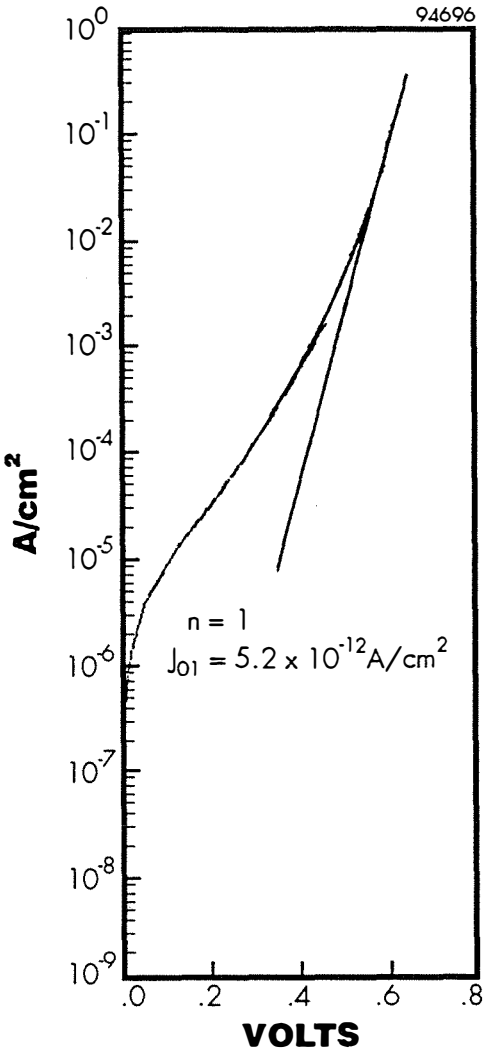


Figure 17 *Dark current-voltage characteristic of silicon solar cell with porous silicon surface.*

2.4 Fabrication of Porous Si Photovoltaic Cells with Improved Design

In the previous section, we described formation of pn junctions in Si substrates by ion implantation, where preliminary devices were fabricated with circular metal contacts deposited through a shadow mask. The use of a simple shadow mask allowed quick turnaround time for the samples, permitting us to demonstrate the feasibility of using porous silicon in solar cells, especially its application as an excellent anti-reflection coating, bringing quantum efficiencies up to the 90% level. We then proceeded to process more silicon wafers and fabricated devices with improved designs for the electrodes.

2.4.1 Wafer Preparation

In the new devices, the junctions were formed using the same ion implantation schedule used for fabricating the preliminary devices. The wafers used in this study included two groups of N-type Si substrates. The first group consisted of wafers with electrical resistivity of about 3 Ω-cm (carrier concentration about 1×10^{15} cm^{-3}), the same as the wafers used for fabricating the previous pn junction cells with shadow masked dot contact. However, we also used a second group of control

N-type substrates with higher (5000 Ω-cm) resistivity and lower carrier concentration (about 1×10^{13} cm^{-3}). It is well known that the surface morphologies of porous Si layers depends strongly on the resistivity of the substrate. We have decided to use the substrates with low carrier concentration because we anticipated a possible difficulty in photolithographically patterning the substrates with higher carrier concentrations.

To assure ohmic contacts at the rear surface, we implanted excess phosphorus into the backs of each wafer. The first phosphorus implantation was with a dose of 5×10^{15} ions per cm^2, with an energy of 50 keV, followed by the same dose at 150 keV. This implantation gives a phosphorus concentration exceeding 10^{20} ions/cm^3 in the first 100 nm, graded with distance in from the surface to about 300 nm. After annealing, metal contacts were applied over the entire back of the wafer, consisting of 100 nm of Ti, 100 nm of Pd, and finally 600 nm of gold. These rear contacts proved to be completely ohmic.

Boron was implanted with doses of 5×10^{15} cm^{-2} into the front sides of the wafers to create the pn junction. The first boron implant at 25 keV serves to bring the hole concentration in the first 200 nm below the surface to the 5×10^{20} cm^{-3} level. Such highly p-type material has been found to etch in a macroporous manner, yielding columns with widths of several microns, and no photoluminescence. This surface material behaves like ordinary bulk silicon, and is used for providing an ohmic contact to the front surface.

Two other boron implantations at higher energies, 75 and 150 keV, served to distribute the boron over a greater range, and therefore result in lower net concentrations of holes below the first 200 nm. This more lightly p-type material can form quantum confined silicon structures, as can the lightly n-type substrate. We have determined that when the heavily p-type surface material is scraped off, then the remaining porous silicon indeed exhibits photoluminescence.

2.4.2 Electrode Configuration

In the new improved device design we attempted to avoid the excessive shadowing that was encountered with circular dot contacts evaporated previously through a shadow mask. The problem is clearly illustrated in Figure 18. Because the surface of the silicon was macroporous, lateral collection of current over to the dot was impeded by the physical voids between the columns of silicon. This lack of good lateral conductivity reduced the collected current.

The design for the new gridded contact is shown in Figure 19. This is a well established design for small (centimeter size) solar cells. The grid lines are 20 μm wide, and their period is 500 μm. Two device sizes available, are one and four cm^2 in total area. A solid contact tab is provided at one edge. Figure 20 is a close-up photomicrograph of the metallization on a completed device. To fabricate these devices, the porous silicon wafers were masked and patterned using conventional photolithographic steps. The metal contact (Ti/Pd/Au) was then evaporated onto the sample. Finally, the excess metal was removed using a lift-off process. As anticipated, we encountered difficulties in spin-casting a uniform photoresist on the porous surfaces made on low-resistivity Si substrates. On the other hand, the wafers with semi-intrinsic doping were patterned without any problem. We believe that because the porosity of the higher resistivity structures is higher, therefore the photoresist penetrates and adheres easier on the sample which allows a uniform distribution.

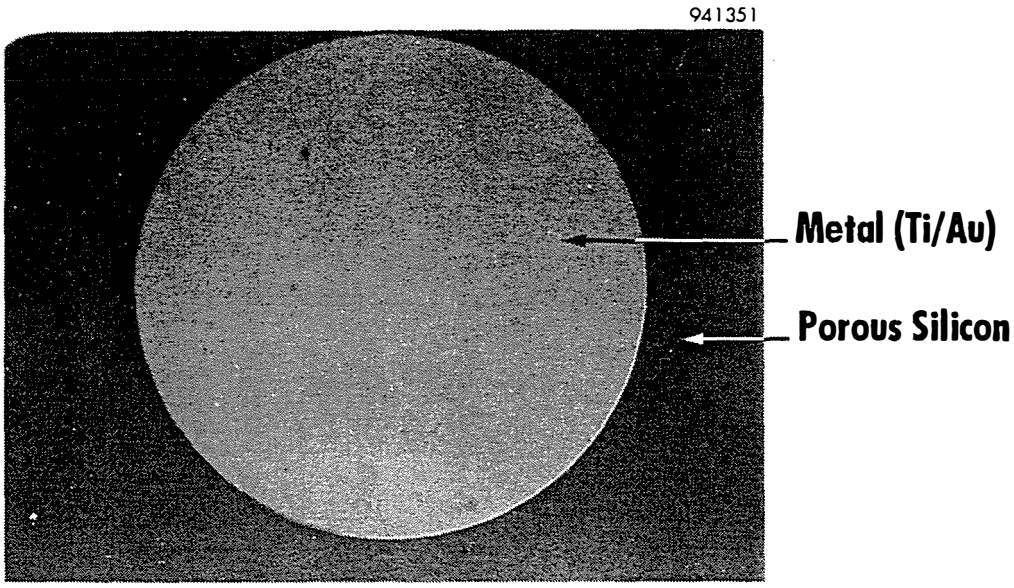


Figure 18 *Solar cell device featuring dot contact.*

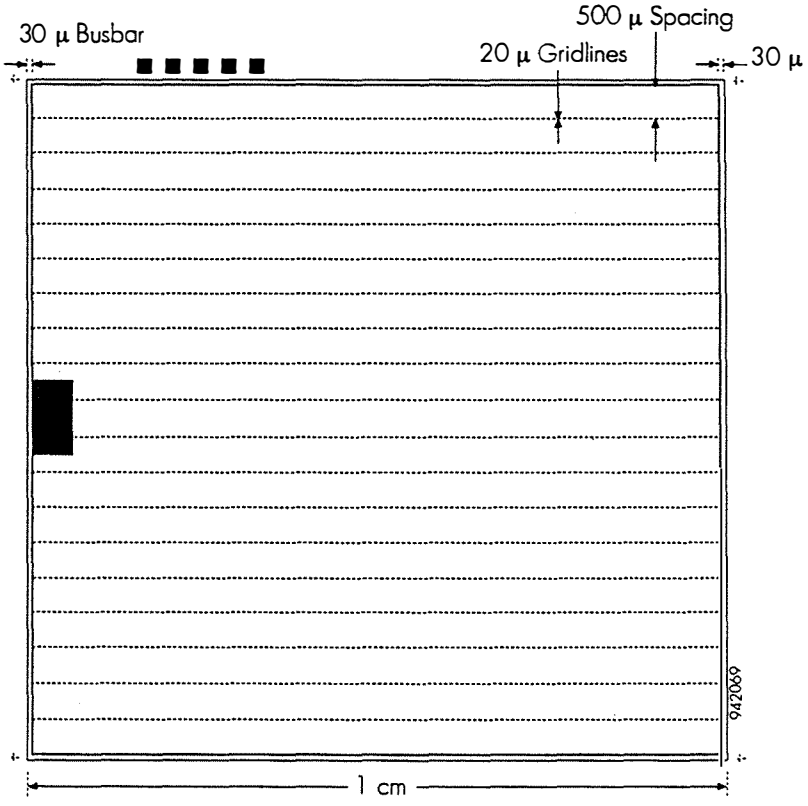


Figure 19 *Solar cell contact dimensions.*

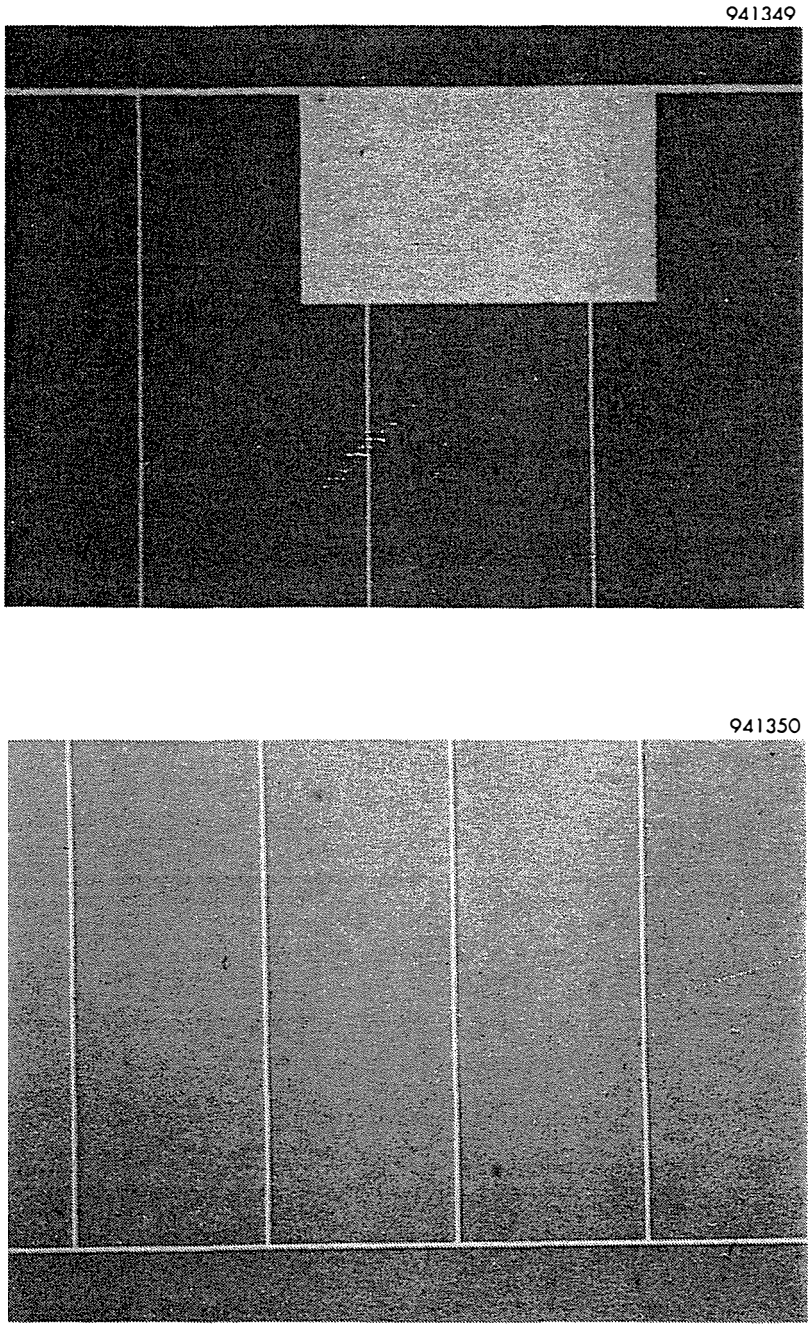
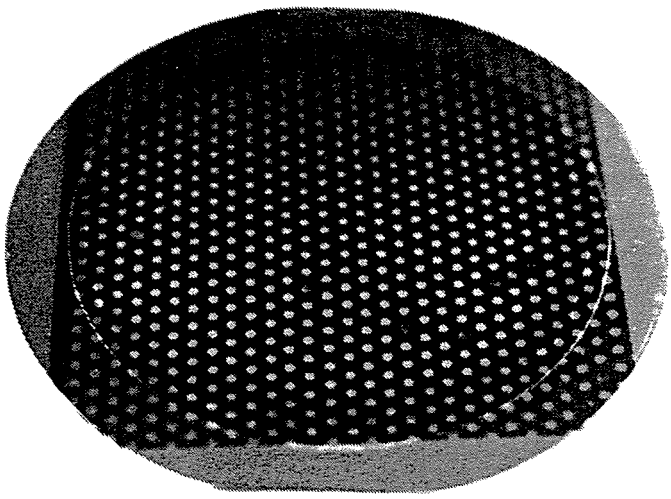


Figure 20 *Details of grid structure on new solar cells: a) contact tab; b) busbar along opposite edge.*

Figure 21 shows a comparison of an older wafer with dot contacts, and a new wafer with gridded metallization. The dark circular area in the center region is porous silicon. The black texture of the porous silicon aids substantially in light trapping, which improves the collection efficiency.



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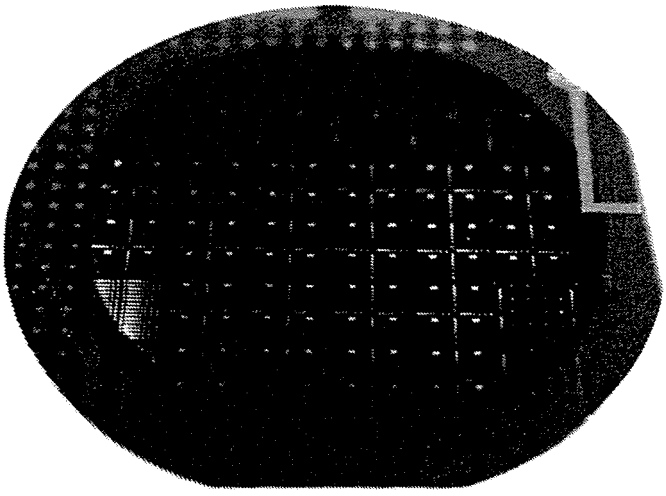


941348

Figure 21 *Photographs of porous silicon solar cells with a) dot contacts deposited through a shadow mask, b) an improved gridded contact formed photolithographically.*

2.4.3 Device Characterization

Using an in-house dicing machine, individual cells were all cut a one square centimeter specific size. The devices were then subjected to various electrical and optical tests.

2.4.3.1 Bulk Silicon pin Solar Cells

For comparison, several devices were prepared using bulk (non-porous) silicon as a control. Because the doping level in the substrate was low, these may be considered as pin devices. The dark and illuminated I-V characteristics are shown in Figure 22. The device exhibited J_{sc} = 22 mA and V_{oc} = 600 mV under illumination with an incandescent lamp. Figure 23 presents the I-V characteristics in a Log (I) vs. V format. In the range of approximately 0.25 to 0.45 V, the curve can be fit to the standard expression,

$$J = J_0 \exp\left(\frac{qV}{nkT}\right) \qquad \textbf{(1)}$$

where we find that n = 2. However, in the region of the open circuit voltage, the characteristics deviated significantly from this form. The deviation does not appear to fit a model based on current control by series resistance once the junction has achieved the flat-band condition. In fact, referring to Figure 24, it can be seen that in the region of 0.5 to 2 V, the characteristic plotted as log (I) vs log (V) is not linear. The higher voltage characteristic may be dominated by space charge injection effects due to the low carrier concentration in the bulk substrate.

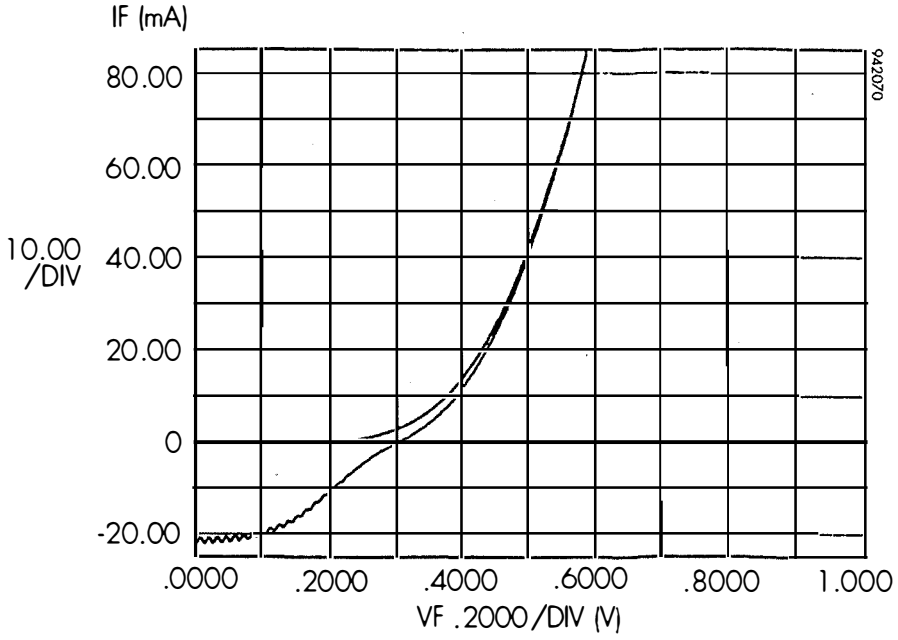
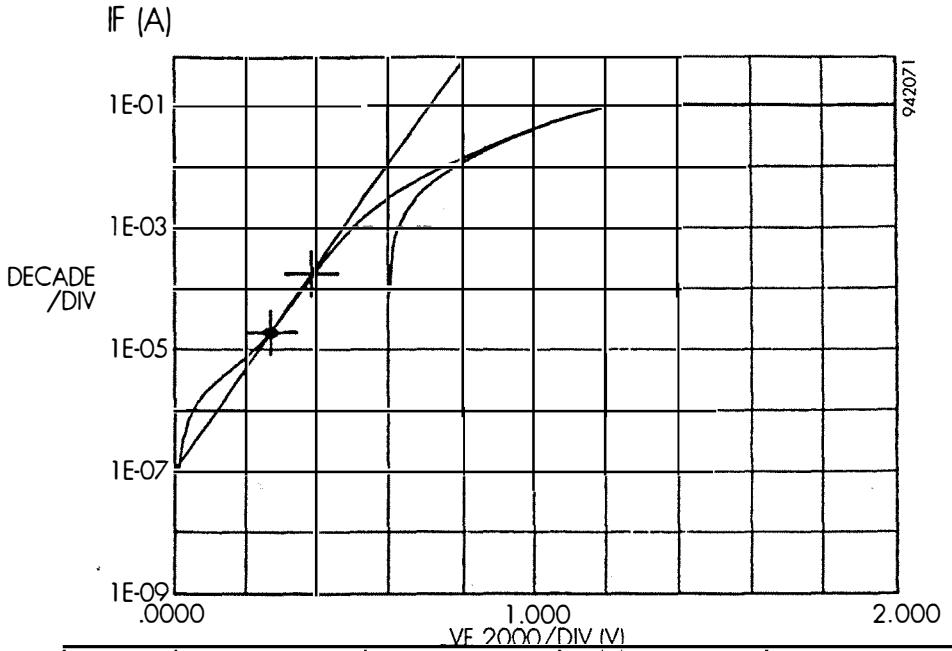
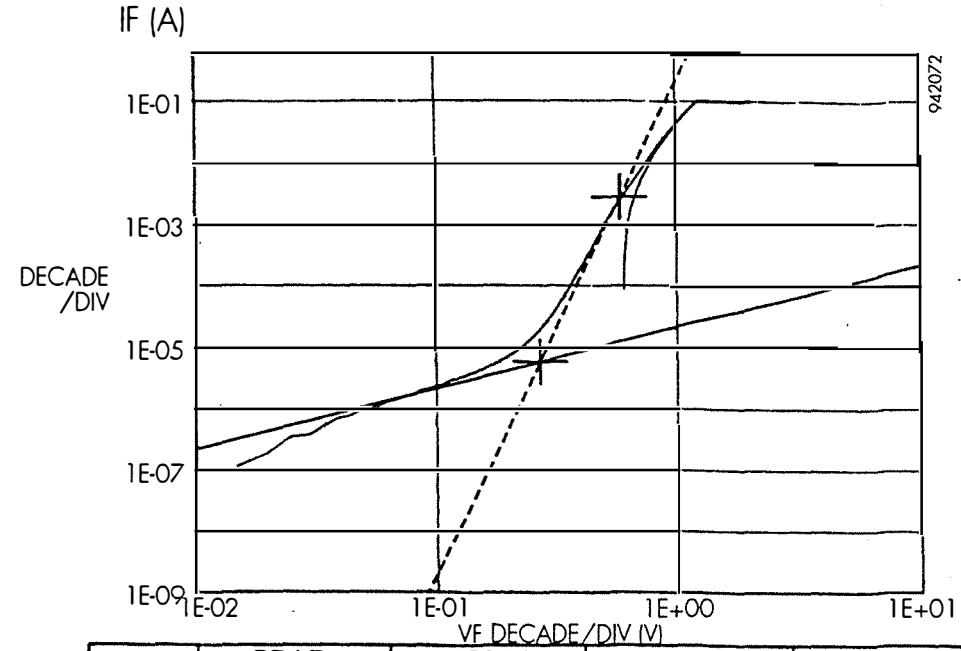


Figure 22 *Current-voltage characteristics of bulk (non-porous) solar cell device featuring low-doped substrate.*



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	8.38E+00	119E-03	833E-03	104E-09
LINE2				

Figure 23 *Characteristic of Figure 22 plotted as log (I) vs V.*



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.00E+00	999E-03	45.6E+03	21.7E-06
LINE2	8.00E+00	125E-03	1.20E+00	229E-03

Figure 24 *Characteristic of Figure 22 plotted as log (I) vs. Log (V).*

2.4.3.2 Porous Silicon pin Photovoltaic Cells

Several of the low-doping concentration wafers were subjected to anodic etching, after implantation, followed by the application of fingered metal contacts. An example of the type of I-V characteristics which we encountered are shown in Figure 25 (the noise is instrumental in nature). The open circuit voltage under white-light illumination is about 0.34V. Figure 26 presents the data over a much larger span of voltage. Two items are of interest. First, there is a significant increase in current with reverse bias, something often seen with amorphous silicon pin solar cells. Furthermore, the dark and the illuminated characteristics cross, again reminiscent of amorphous silicon. This observation indicates that superposition fails. That is, the illuminated I-V characteristic is not the difference between the photogenerated current and the dark current. Failure of the superposition principle in solar cells often indicates that the photogenerated current is voltage dependent, and that space charge injection effects may be present. An increase in photocurrent with reverse bias often occurs if there is a barrier to carrier collection, which can be overcome by reverse bias.

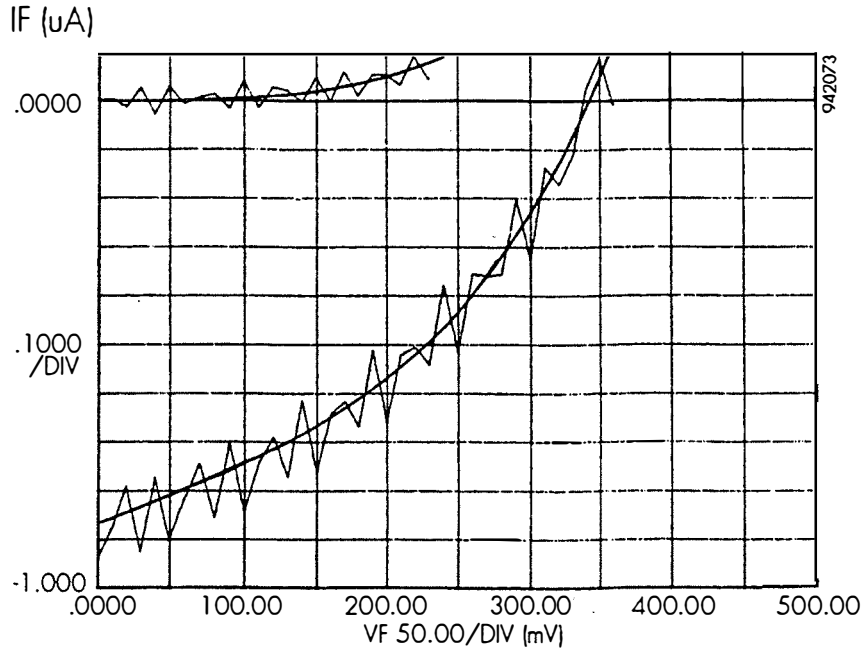


Figure 25 *Characteristics of porous silicon pin solar cells under white light illumination.*

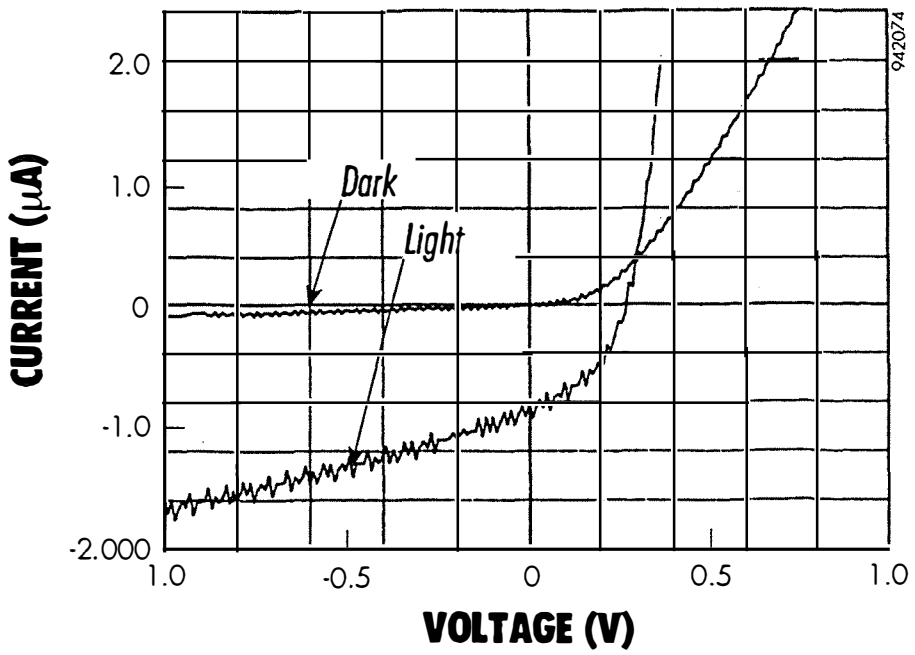


Figure 26 *Extended current-voltage characteristics, indicating failure of the superposition principle and a voltage-dependent photocurrent.*

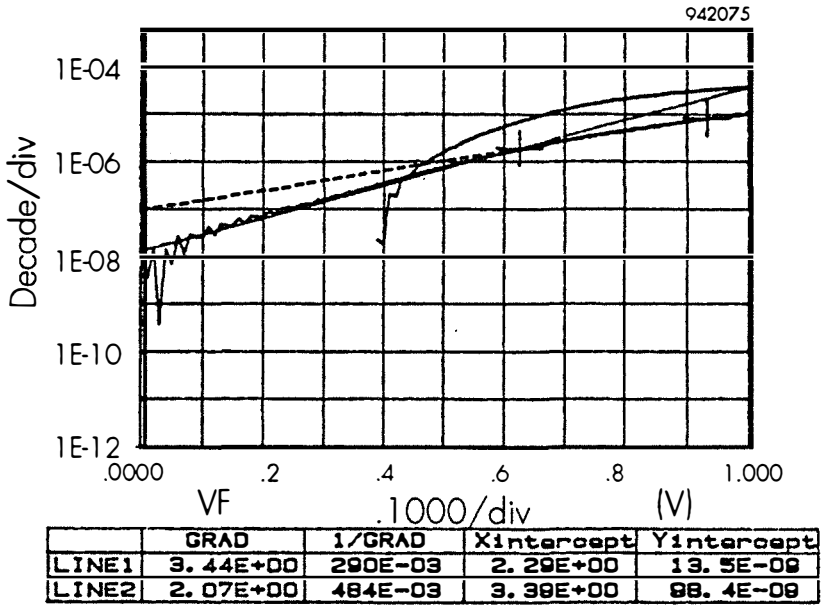
The log (I) vs. V characteristics of one of our pin cells is shown in Figure 27. In the range of 0 to about 0.6 V, the characteristic can be fit by an ideality factor of 4.88. We usually find ideality factors around 5 or larger for all of our porous silicon devices, whether configured as solar cells or LEDs. Using the data from Figure 27, we attempted to calculate the open circuit voltage. (V_{oc} can be read directly from the plot because the illuminated characteristic terminates at V_{oc}). For this device, we found $J_{sc} = 1 \times 10^{-6}$ A while extrapolation of the dark characteristic gives $J_0 = 1.35 \times 10^{-9}$A. Using:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_0}\right) \qquad \textbf{(2)}$$

Upon substituting the known values, we find that V_{oc} should be 0.54 V, much larger than measured. This finding strongly suggests that the light is affecting the "dark current." In Figure 28, we have plotted log (I) vs. log (V). Between 0.1 and 1 V, the current is proportional to the voltage squared, an indication of space charge injection. At higher applied bias we appear to hit a trapped filled limit, and then another $I = \alpha V^2$. It is not clear if the space charge effects are in the porous silicon or in the bulk substrate.

2.5 Electroplated Contacts

We considered that a major limitation on cell performance is the problem of properly contacting the entire porous silicon surface. For example, an evaporated metal film will only cover the outer surface of the porous region. Consequently, we have developed an improved method for making intimate contact to porous silicon. The method relies on electroplating.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	3.44E+00	290E-03	2.29E+00	13.5E-09
LINE2	2.07E+00	484E-03	3.39E+00	88.4E-09

Figure 27 *Characteristics of porous silicon pin device presented as log (I) vs. V.*

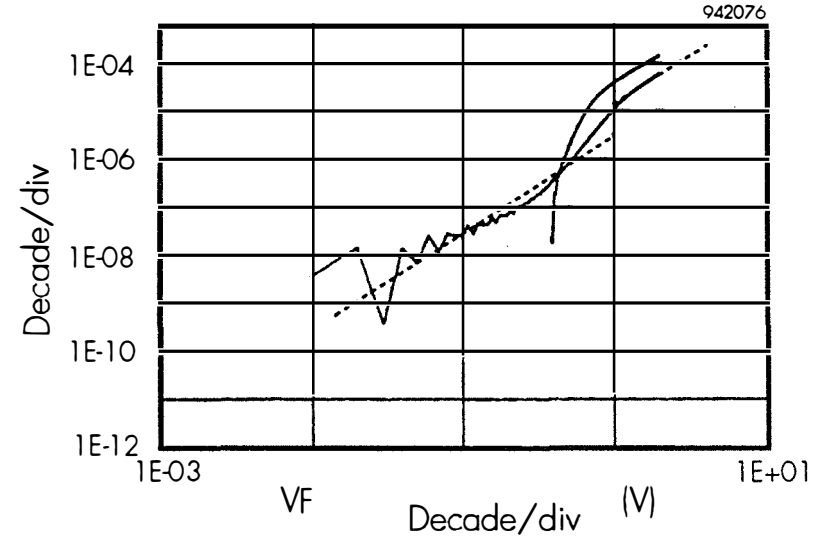


Figure 28 *Characteristics of porous silicon pin device plotted as log (I) vs. log (V).*

2.5.1 Electroplated Copper Contacts

After the standard anodic etching of an n-type wafer was completed, the platinum counter electrode was removed, and replaced by a copper electrode. The polarity of the bias was adjusted to make the copper an anode, and the cathode. Copper was found to dissolve readily in the electrolyte, and to plate out over the porous silicon surface. Because the copper ions were introduced into the solution, they can be expected to plate out even inside the pores.

Figure 29 shows the dark I-V characteristics of a Cu/PS/n-Si device. Rectifying behavior is clearly evident. The effect of exposure of the device to different intensities of white light is shown in Figure 30. There is a definite photovoltaic effect present. However, the fill factor is very poor. The characteristics are shown over a greater span of voltage in Figure 31. It can be seen that a reverse bias provides a great increase in photogenerated current.

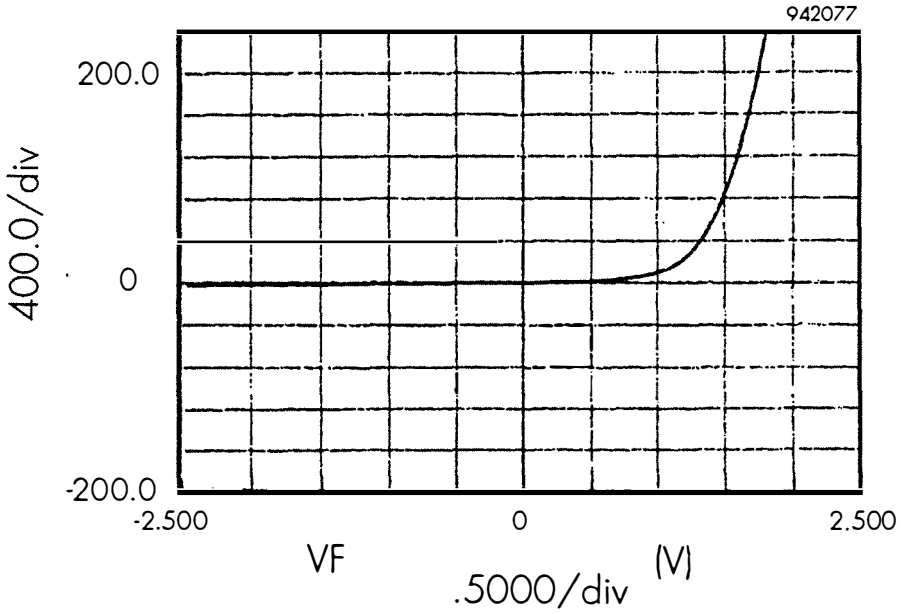


Figure 29 *Dark I-V characteristics of copper/porous silicon/n-type silicon device.*

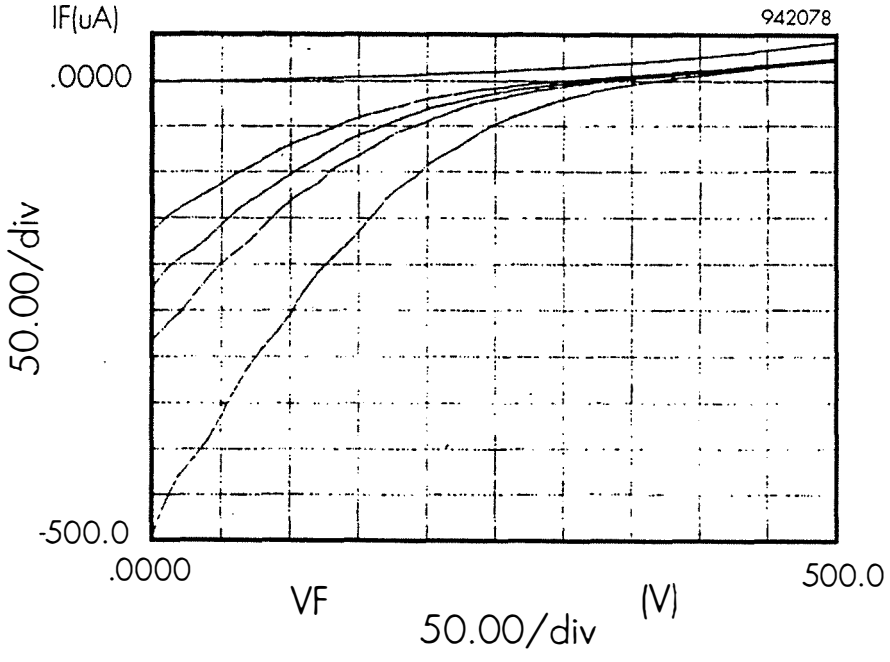


Figure 30 *Illuminated I-V characteristics of copper/porous silicon/n-type silicon cell.*

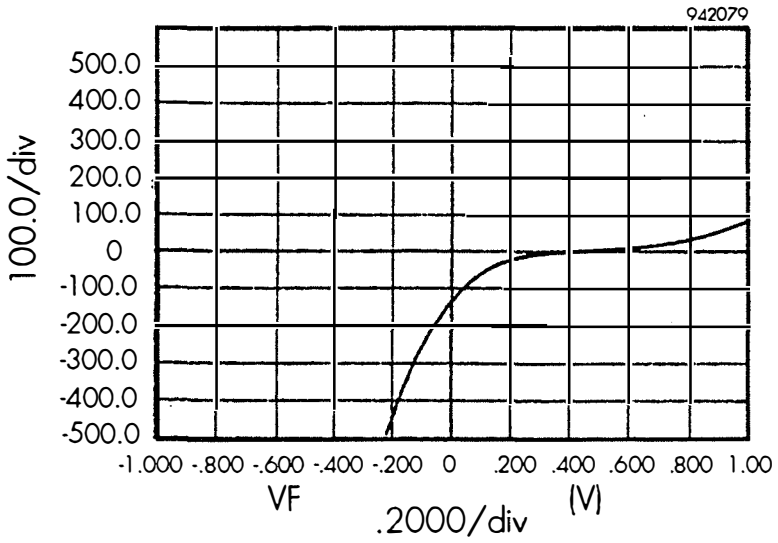


Figure 31 *I-V characteristics of copper/porous silicon/n-type silicon cell over extended voltage range.*

Figure 32 gives light and dark current-voltage characteristics in the range of -2.5 to +2.5 V. It appears as if the magnitude of the photocurrent may tend to saturate at about -2.5 V, where the current has reached 2 mA. It is also seen that the light and dark characteristics do not cross. Therefore, this device shows improved behavior compared to the previous ones.

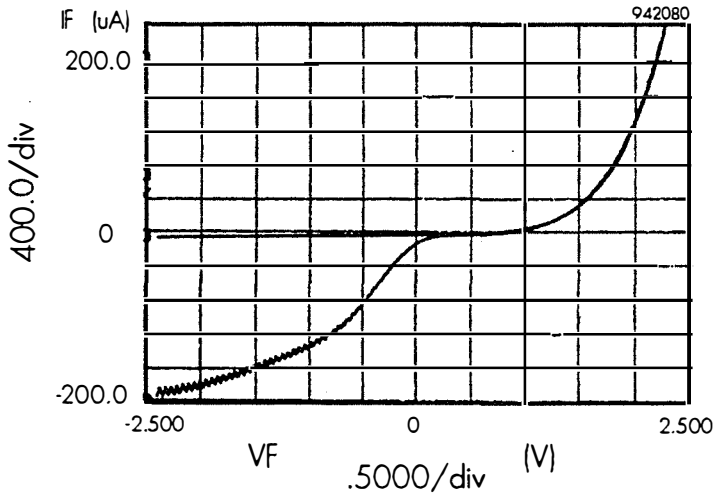
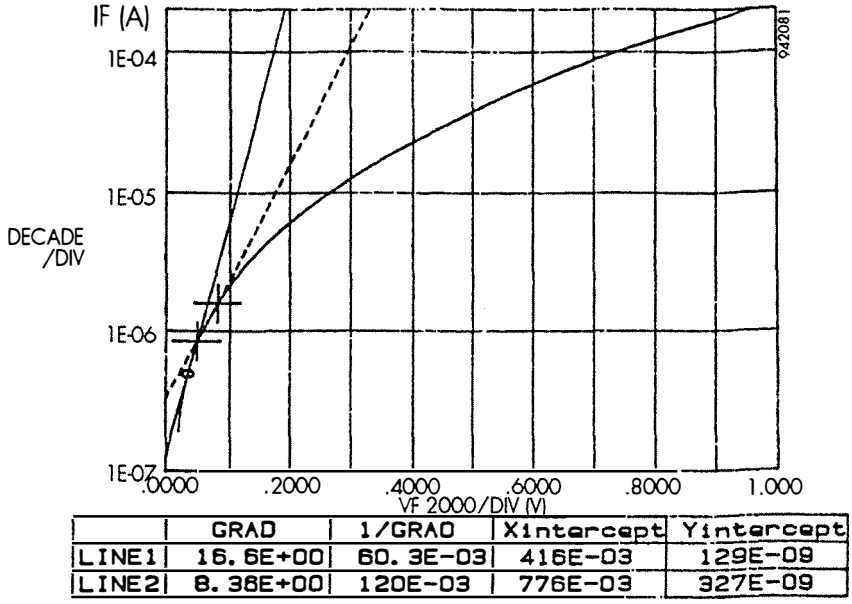


Figure 32 *Comparison of light and dark current-voltage characteristics of Cu/PS/n-type silicon solar cell.*

The log (I) vs. V plot is given in Figure 33. It may be possible to fit the standard diode equation at low voltages. We indicate lines with ideality factors of one and two. However, at larger biases, the curve deviates greatly from these values. As a check on the mechanism of current flow, we have plotted log (I) vs. log (V) in Figure 34. At biases exceeding about 0.5 V, we find $I \sim V^3$. This could be modeled by space charge limited current mechanism. We may question where space charge could be injected: certainly not in the doped silicon substrate. It would appear that currents must be passing directly through the nominally insulating porous silicon, and that at high current levels, the space charge exceeds the doping concentration.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	16.6E+00	60.3E-03	416E-03	129E-09
LINE2	8.38E+00	120E-03	776E-03	327E-09

Figure 33 *Log (I) vs V plot for Cu/PS/n-type silicon device.*

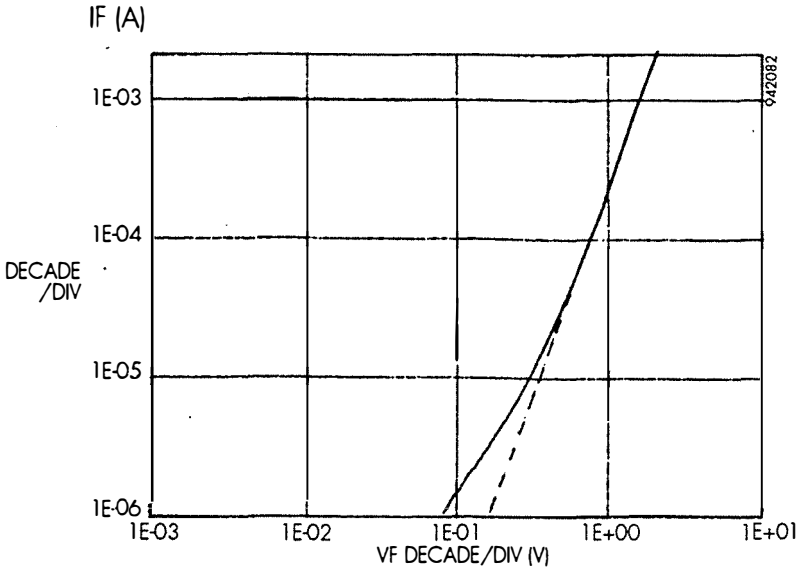


Figure 34 *Log (I) vs. Log (V) plot for Cu/PS/n-type silicon device.*

2.5.2 Electroplated Indium Contacts

A set of pn junction cells were prepared by growing an epitaxial film of phosphorus doped n-type silicon onto p-type silicon substrates. The epitaxial layer was about 1 micron thick, and the phosphorous doping concentration was 1 x 10^{16} cm^{-3}, except for the top 1000Å, which was doped at the 1 x 10^{20} cm^{-3} level to provide a good contact. The grown wafers were then subjected to our standard electrochemical etching procedure.

Under illumination, the etching was allowed to proceed through the junction, into the p-type substrate. Upon completion of the anodization procedure, $InCl_3$ was added to the solution, and the polarity of the electrodes was reversed. As the porous silicon was made to be cathodic, indium was electroplated throughout the pores.

Light and dark current-voltage characteristics are shown in Figure 35. V_{oc} is about 0.33 V, while I_{sc} is about 3 μA. The light and dark curves cross in forward bias. Figure 36 shows the I-V characteristics over the range of voltages from -25V to +25V. It is clear that at large reverse biases, a very large photocurrent, about 2 mA, is generated.

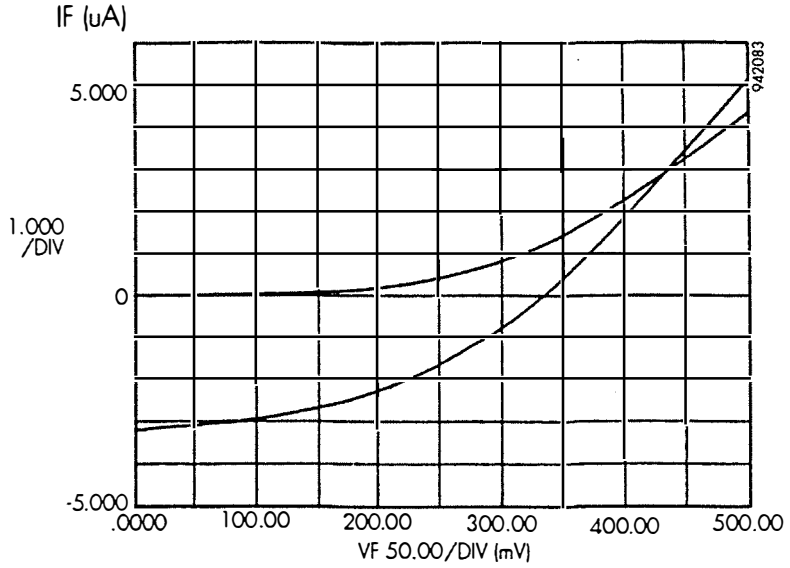


Figure 35 *Light and dark current-voltage characteristics of an epitaxial n-on-p porous silicon device with indium electroplated contacts.*

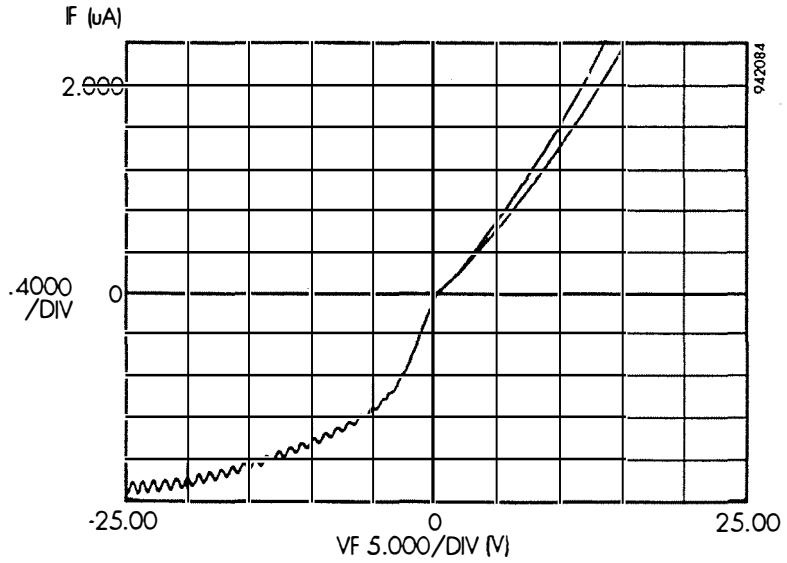


Figure 36 *Characteristics of the device shown in Figure 35 presented over a large span of voltage.*

Finally, the incandescent white light was modified with glass filters, and the I-V characteristics were re-measured. The results are shown in Figure 37. Three filters were found to have no effect on the photocurrent: a 3-67 orange filter which cuts off at 545 nm, a 2-63 red filter which cuts off at 585 nm, and a 2-61 filter which cuts off at 605 nm. However, use of a 4-96 cyan-colored filter which only passed wavelengths from 360 nm to 600 nm obliterated the photocurrent. A 1-75 clear filter which cuts off the infrared up to about 850 nm and a 7-56 black filter which only transmits below 800 nm gave about the same reduced levels of photocurrent. The transmission characteristics of the filters are shown in Figures 38 and 39. Clearly, the device is not sensitive to either green or blue light. All of the current is generated at wavelengths longer than 600 nm. For this sample, it appears that the porous silicon is able to absorb all the green and blue portions of the spectrum, but unless a reverse bias is applied, the current cannot be collected.

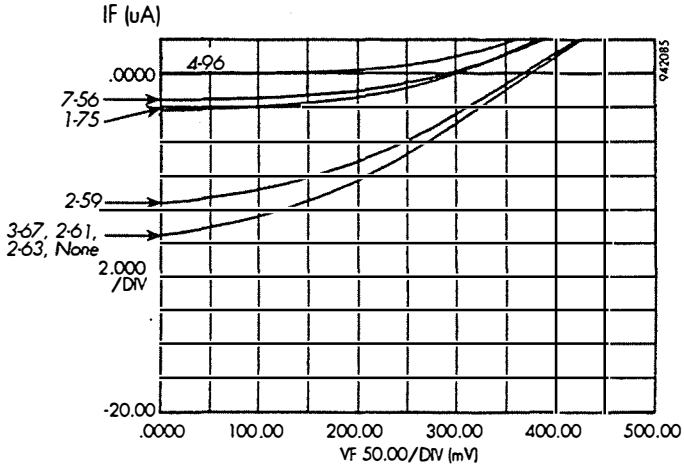


Figure 37 *Current-voltage characteristics of n-on-p porous silicon device with indium contact film taken with filtered light.*

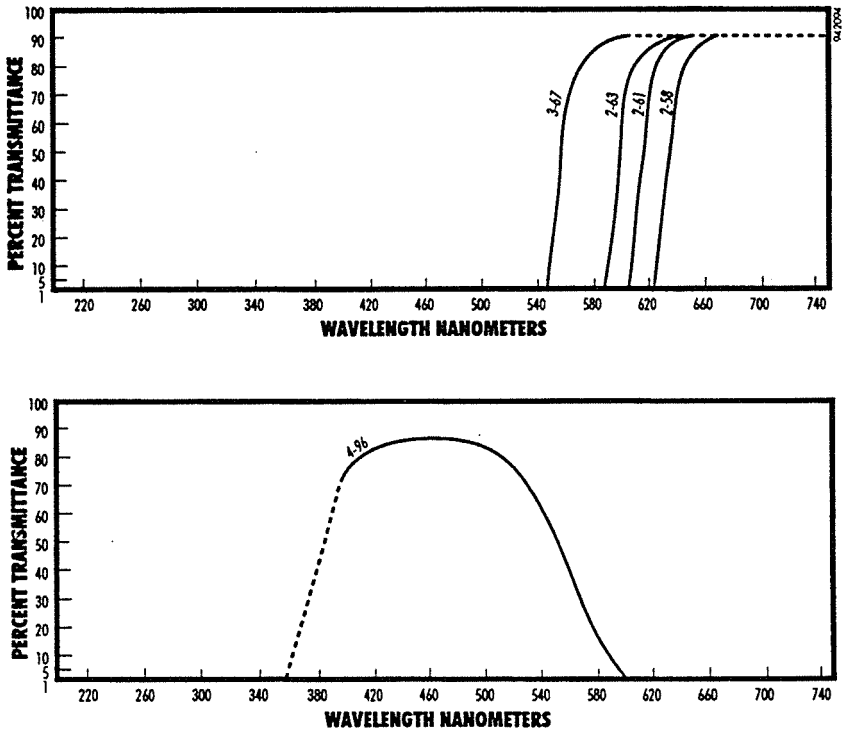


Figure 38 *Transmission characteristics of 3-67, 2-63, 2-61, and 4-96 filters.*

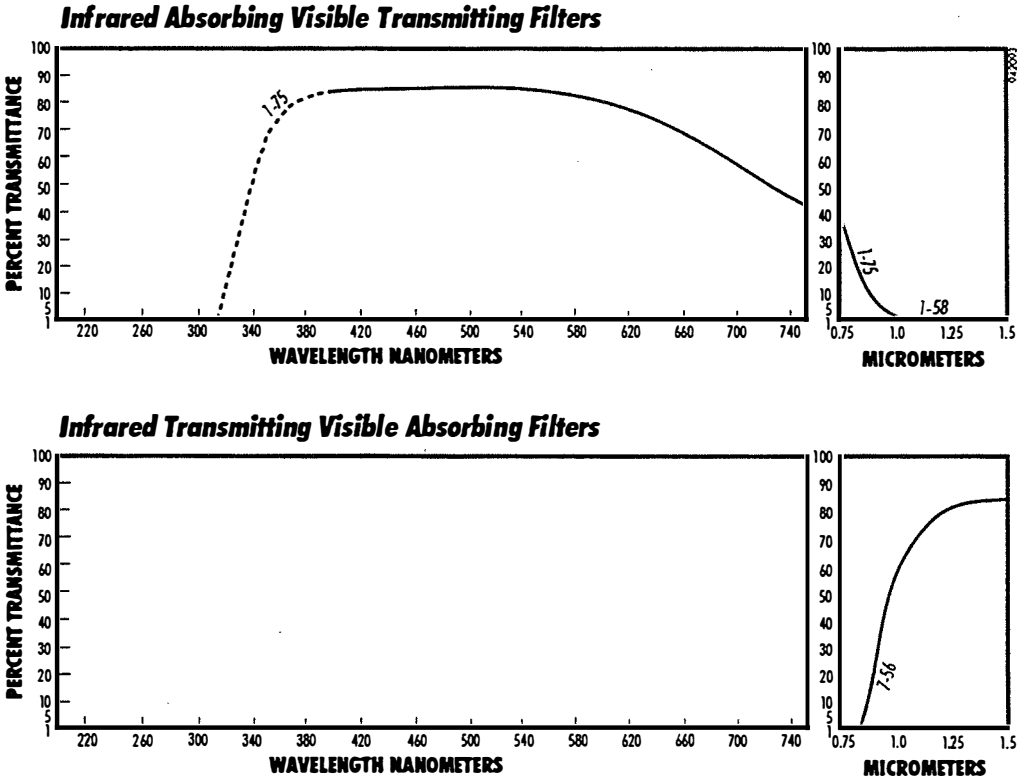


Figure 39 *Transmission characteristics of 1-75 and 7-56 filters.*

2.6 Electroluminescence

Catalano recently noted the crossover of photovoltaic materials technology to flat panel displays.[14] Pursuing this approach, we have observed several of our solar cells under forward bias, in the dark. Electroluminescence has been observed, as shown in Figure 40. The sample consists of a low doping density n-type substrate with a surface p-type region create by implantation of boron. The device has standard finger electrodes deposited by photolithographic procedures. The entire device lights up red, indicating that minority carriers, both holes and electrons, are being injected into the quantum confined region. Because there exists macro-porous (non-quantum confined) silicon on the top surface, light emission is stronger from around the edges of the sample. The fact that we can inject and transport both carrier types through our porous silicon gives us assurance that we can also collect minority carriers in the photovoltaic mode.

Let us note the importance of the semi-insulating substrate in providing uniform light emission throughout the sample: In highly conducting substrates, charges rapidly travel into the porous silicon just below the contact, giving only pinpoints of electroluminescence. With a high resistivity substrate, charges can fill the entire p^+ emitter before they can be injected under larger forward bias.

2.7 Improved Porous Silicon Solar Cells with Electroplated Indium Shadow-mask Dot Contacts

The starting wafers are P+ Si (≈ 0.01 ohm-cm), with a thick N region (≈ 0.1 ohm-cm) grown epitaxially. The porous Si was made using deep electrochemical etching which penetrated the N-P junction. During porous Si formation, a very thin layer of indium was deposited on the surface by *in-situ* electroplating. This layer is to improve lateral conduction. Onto this, ≈ 2000Å transparent indium-tin-oxide (ITO) was deposited (by ion-beam-assisted deposition) as 6 mm (0.28 cm^2) round dots through a shadow mask. Back contact was made with full-area metallization. The 5-μm junction depth is misleading. With a surface having deeply etched "pores,", much of the junction area is a lot closed to the actual surface than 5 μm.

Figure 41 show an I-V measurement of this device. The "light" curve was tested under uncalibrated microscope illumination. As reported previously, the light and dark curves cross under forward bias, indicative of a voltage-dependent photogenerated current. The dark I-V curve shows an increase in current with increasing reverse bias, indicating a barrier to charge collection.

Figure 42 shows the same data, plotted on an expanded scale. We see that the open-circuit voltage is 0.414 volts, and the short-circuit current is 1.4 mA, or 5 mA/cm^2 current density. This is a three orders-of-magnitude increase over devices made previously without the electroplated indium layer. This large increase in photocurrent is attributed to improved conduction properties of the In-coated Si "wirelike" features. Similarly, the open-circuit voltage has increased from a previous value ≈ 0.3 volts to ≈ 0.4 volts.

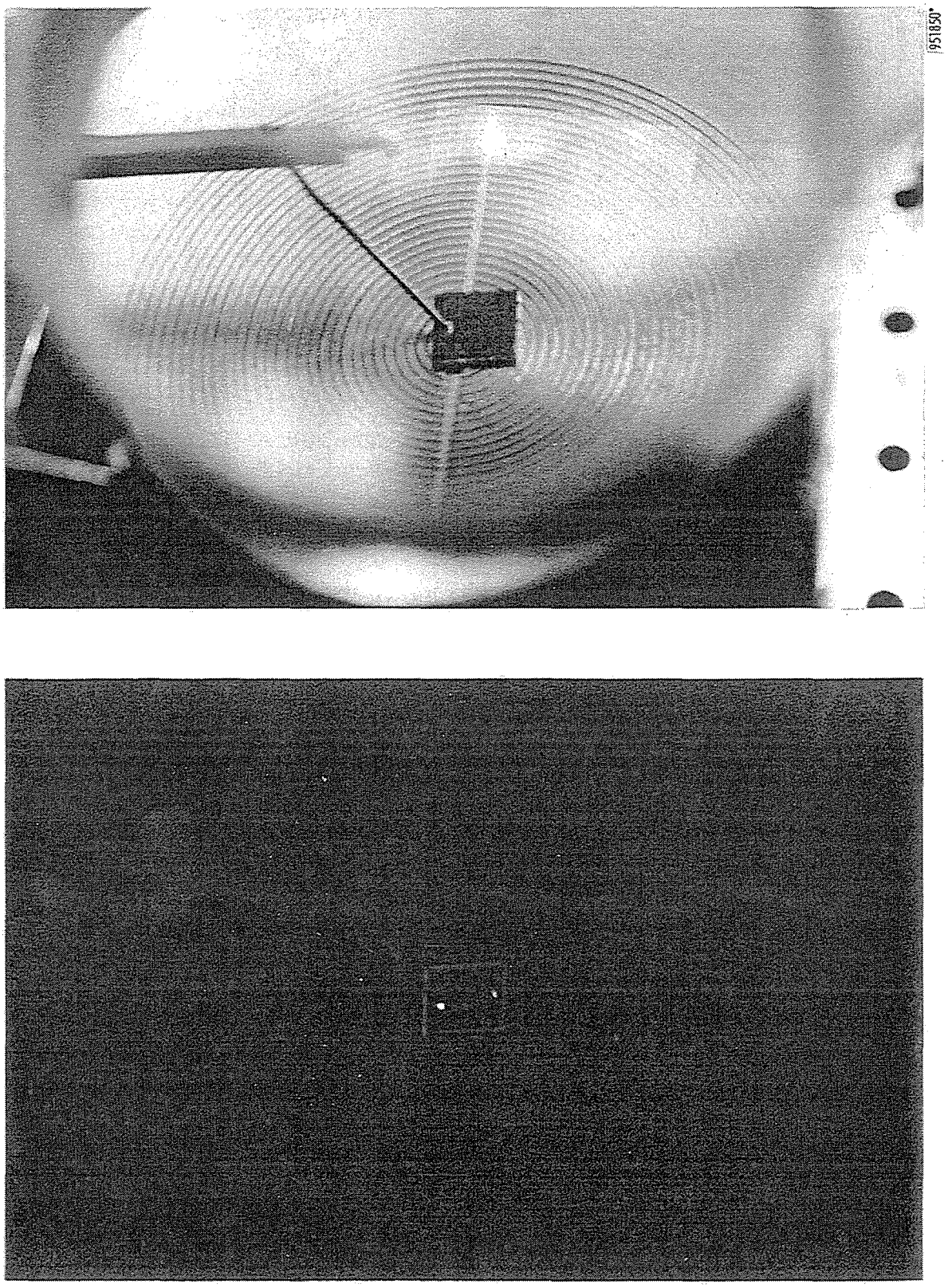


Figure 40 *Porous silicon solar cell operated as a light-emitting diode. (a) Configuration of the device under test; (B) electroluminescence.*

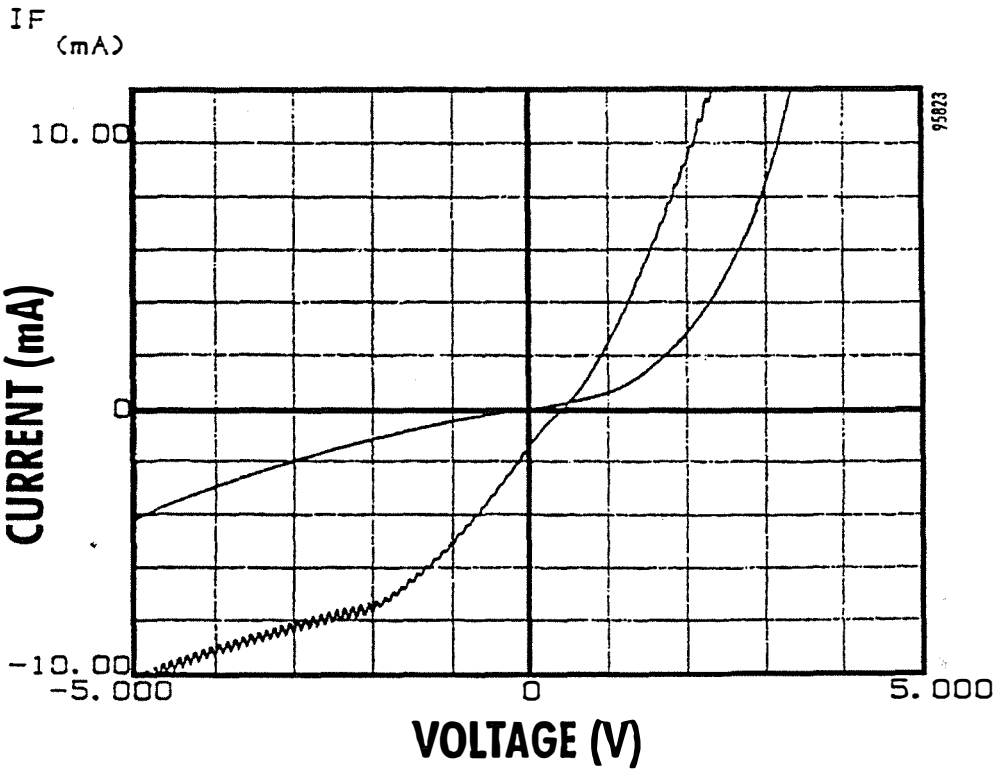


Figure 41 *Dark and light I-V measured data for an ITO-contacted porous Si solar cell with a thin layer of electroplated In. The oscillations at reverse bias voltages are an artifact of noise problems in the instrumentation.*

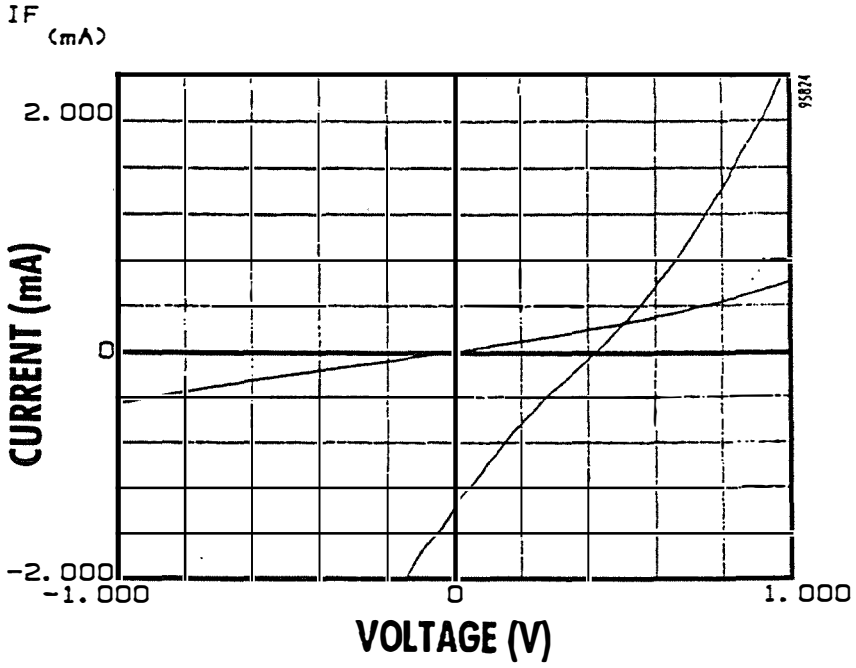


Figure 42 *Expanded scale showing dark and light I-V measured data for an ITO-contacted porous Si solar cell with a thin layer of electroplated In.*

2.8 Polycrystalline Layers

Polycrystalline Si is an important solar cell material, and texture etching is a significantly needed technology. Texture etching of polycrystalline Si cells to form an antireflection (AR) coating is not possible by conventional means; these etches rely on well-defined crystal directions to achieve the anisotropy which produces the textured, light-trapping surface morphology.

To address this need, we have performed experiments to achieve a non-reflective, light-absorbing surface on polycrystalline Si. The material used in our study is cast and sliced P-type polycrystalline Si. The average grain size is ≈ 5 mm. A thin, porous, texturized surface layer is formed by chemical etching in hydrofluoric acid (HF) - nitric acid - water (1:3:5), or alternatively by electrochemical etching in HF-ethanol with an applied bias. The most nonreflective surface was made by electrochemical etching at a current density of ≈ 100 mA/cm^2 for a few minutes. Etching for a longer time at lower current density results in a less black surface.

Figure 43 shows a polycrystalline Si surface before and after applying the porous Si electrochemical etch process. For this sample, a current density of 100 mA/cm^2 was used. The mottled appearance is due to the grains reflecting light at various angles. Optimization of this process should result in even blacker surfaces on polycrystalline Si.

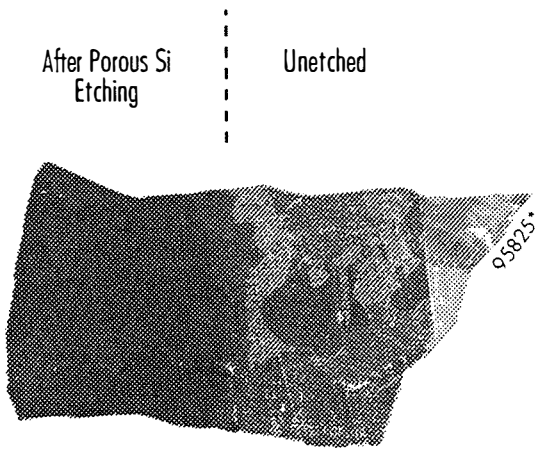


Figure 43 *Polycrystalline Si surface, with and without a porous Si layer formed by electrochemical.*

These preliminary experiments showed that we can greatly reduce surface reflectivity on polycrystalline Si wafers by forming a thin porous-Si layer by chemical etching. Next we tried to show that a porous surface layer on a polycrystalline solar cell actually improves performance by acting as an AR-coating/surface-passivation layer.

Towards this end we received several polycrystalline solar cells, courtesy of Dr. John Wohlgemuth of Solarex, Frederick, MD. These cells are their standard production vintage, but with no AR coating. These N-on-P cells have a junction depth of ≈ 0.5 μm, so the porous surface treatment must be held to less than that depth. We applied TiPtAu ohmic-contact metallization to the backs, after covering the front and edges with photoresist for protection. An unexplained ohmic-contact problem prevented us from making cells usable for our etching experiments.

Polycrystalline Si cells, with metallization but without AR coating, were also received from Dr. Simon Tsuo of NREL. These cells are N-on-P structures (junction depth ≈ 0.35μm) made over ten years ago at Exxon Research Laboratories from a Czrochalski ingot where the single-crystal growth failed and turned polycrystalline. Due to the shallow junction depth. these cells were not used in our porous Si experiments.

Three polycrystalline Si solar cells (≈ 10 - 40 cm^2 each) were cut from one large standard, AR-coated (ITO-coated) Solarex solar cell 4" wafer. In each case efficiency was measured [1] with the ITO AR coating in place, then [2] with the ITO removed, and finally [3] with the surface treated by our porous Si etch process. For the first cell, the I_{sc} dropped from 341 mA to 284 mA upon removal of the ITO. The porous Si etch treatment partially restored the current to 308 mA. Unfortunately this treatment degraded the fill factor, from about 0.74 to 0.56, so that the efficiency was reduced with the porous treatment, even though the current was partially recovered. Results of this experiment are shown in Figure 44.

On the second cell, similar tests were conducted. We tried to make the porous surface more absorbing by etching for a longer time. This significantly degraded the current (step 2 to step 3 went from 282 to 70 mA) and the voltage, indicating that the porous material penetrated the pn junction. Results of this experiment are shown in Figure 45. On the third cell, results were similar.

Another polycrystalline Si solar cell without AR coating was used in the next trial. On this wafer, a porous surface was formed, being careful not to penetrate the junction. This shallow etch did improve all solar cell parameters, but only slightly; the very shallow etch made the surface slightly less reflective than the bare wafer, but not nearly as black as for a longer etch treatment. Results of this experiment are shown in Figure 46.

We have learned that the porous-Si surface treatment needs to be ≈ 0.5 μm deep to make a good, AR coating with low reflectivity. For this design, the junction depth needs to be initially ≈ 1 μm; on such cells, we feel that we could optimize the porous surface process to yield reasonable efficiency gains. By consuming the top ≈ 0.5 μm with the porous etch treatment, the final junction depth would remain at essentially 0.5 μm, thus preserving the basic cell design. Unfortunately, during this program we were not able to secure any polycrystalline cells with junctions this deep.

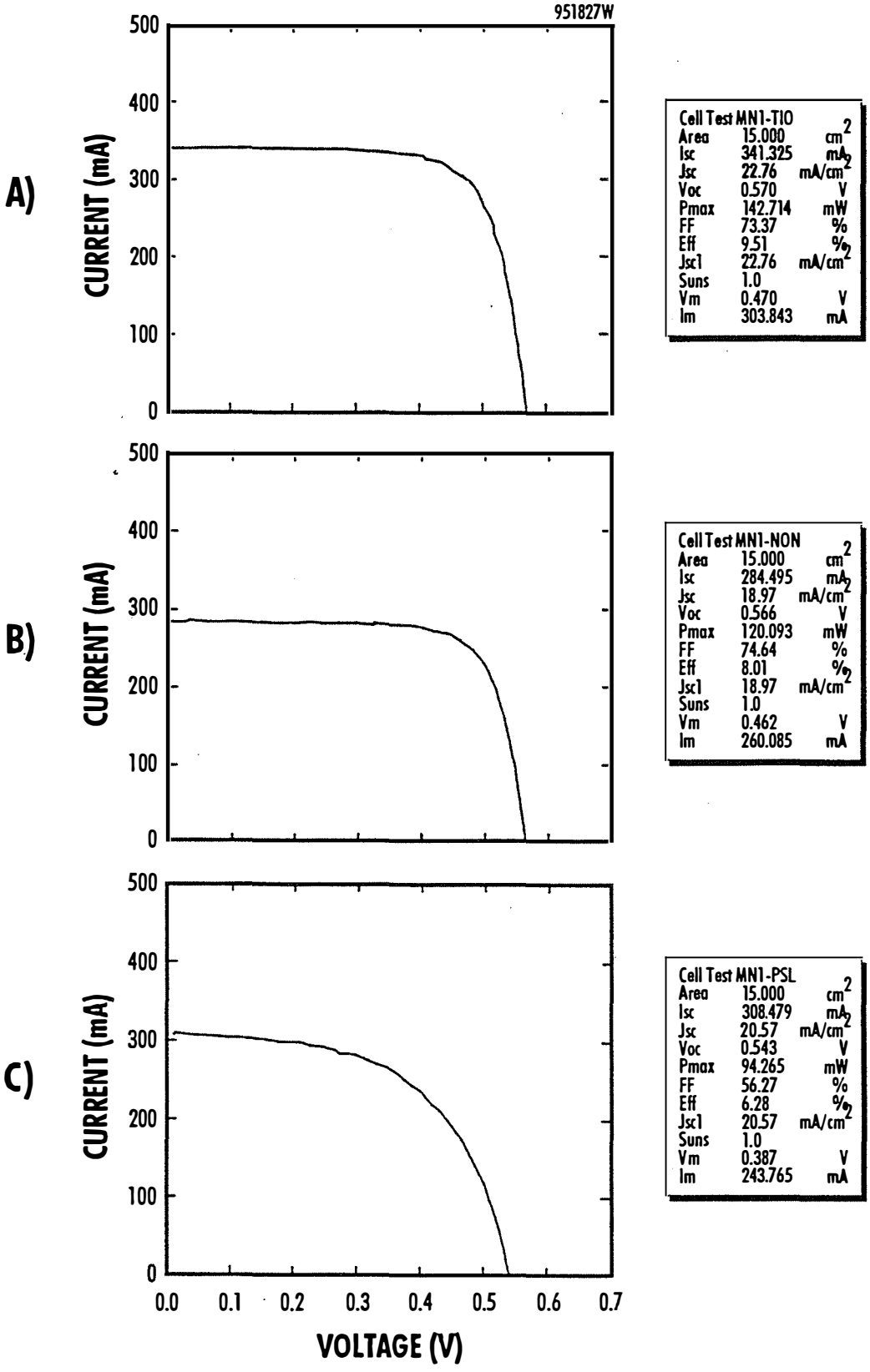


Figure 44 *Results of our first attempt to improve a polycrystalline Si solar cell (Solarex material) with a porous-Si etch surface treatment. AM 1.5, Global, 100 mW cm^{-2}. [a] with ITO AR coating in place; [b] after removing the ITO; [c] after forming porous Si surface onto the cell of step [b].*

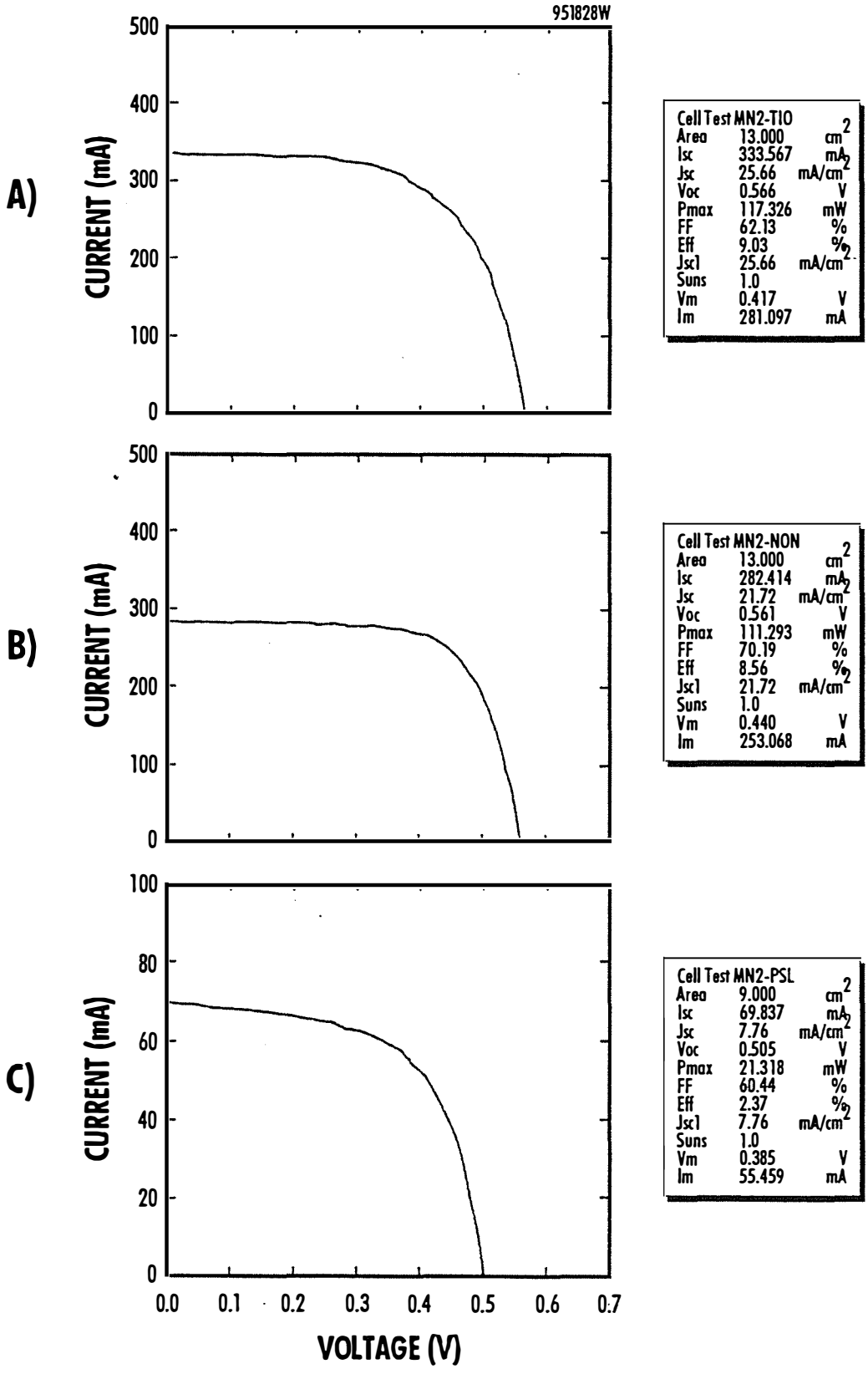


Figure 45 *Results of our second attempt (deeper etch) to improve a polycrystalline Si solar cell (Solarex material) with a porous-Si etch surface treatment. AM 1.5, Global, 100 mW cm^{-2}. [a] with ITO AR coating in place; [b] after removing the ITO; [c] after forming porous Si surface onto the cell of step [b].*

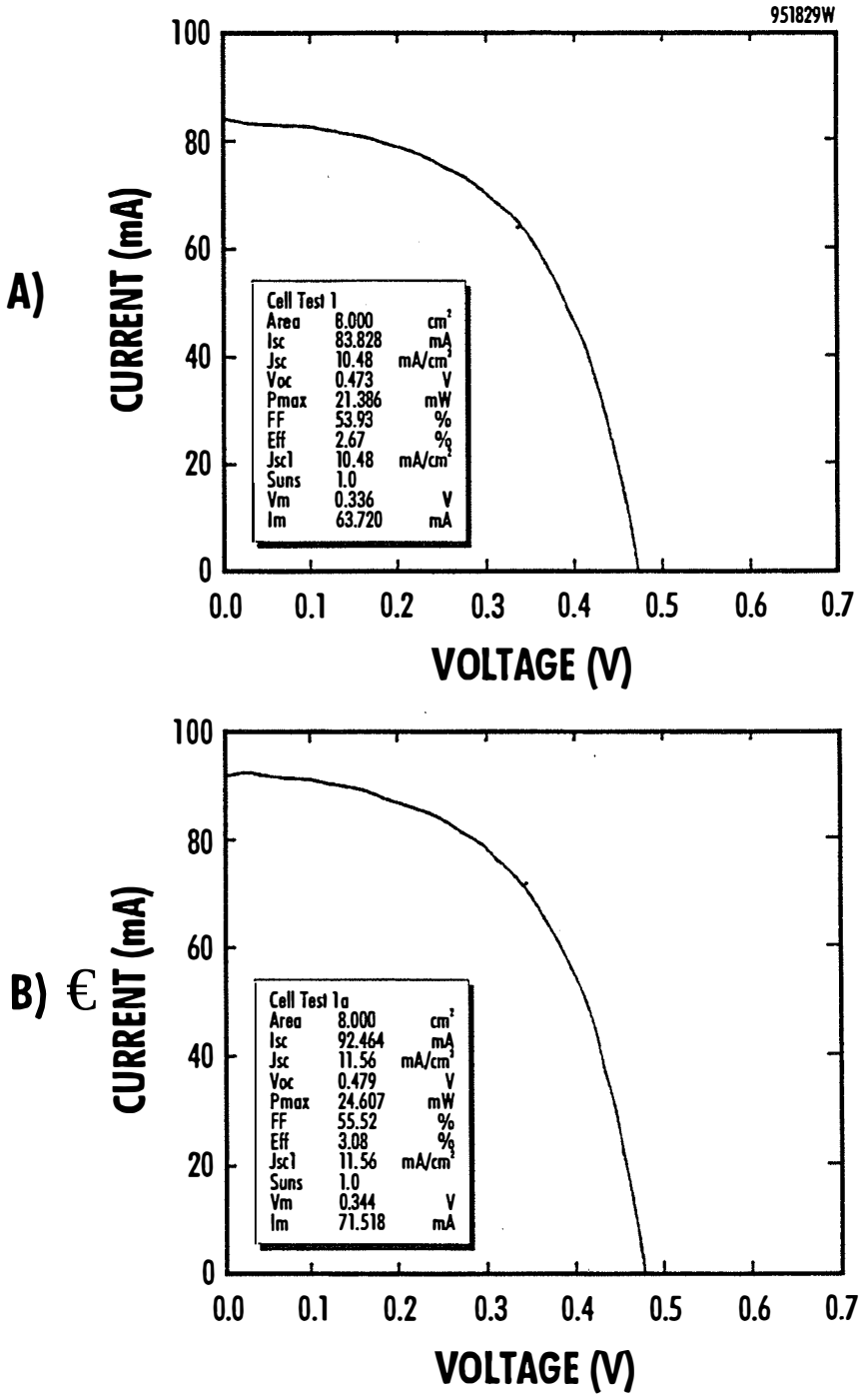


Figure 46 *Results of another attempt (shallow etch) to improve a polycrystalline Si solar cell (Solarex material) with a porous-Si etch surface treatment. AM 1.5, Global, 100 mW cm^{-2}. [a] bare polycrystalline Si cell; [b] after a shallow porous Si etch treatment.*

3 ACKNOWLEDGEMENTS

The author wishes to acknowledge the following: [at Spire] Mr. Nader Kalkhoran for carefully conducting most of the porous silicon solar cell fabrication and testing, Dr. Paul Maruska (the initial principle investigator) for conceiving the program, Dr. Ward Halverson for program management, [at Solarex] Dr. John Wohlgemuth for supplying polycrystalline Si solar cells, and [at NREL] Dr. Simon Tsuo for polycrystalline Si cells and helpful discussions, and John Benner for supporting this research.

4 PUBLICATIONS

During this two-year program, two papers were published and presented at conferences; they are enclosed as appendices. "High Performance Porous Silicon-Based Solar Cells," by Nader M. Kalkhoran, S.M. Vernon, H.P. Maruska, and W.D. Halverson, was presented at the Fall 1994 meeting of the Materials Research Society in Boston. "High Performance Porous Silicon Solar Cell Development," by S.M. Vernon, N.M. Kalkhoran, H.P. Maruska, and W.D. Halverson, was presented at The First World conference on Photovoltaic Energy Conversion in Hawaii, December 1994, and published in the IEEE proceedings from this meeting.

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APPENDIX A

HIGH PERFORMANCE POROUS SILICON SOLAR CELL DEVELOPMENT

HIGH PERFORMANCE POROUS SILICON SOLAR CELL DEVELOPMENT

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ABSTRACT

We have fabricated Si solar cells from porous Si/bulk Si structures. Two cell types, having the junction within the porous Si or within the bulk Si, were studied. We have seen clear evidence of the photovoltaic effect in porous Si, although currents and voltages are low, due to spreading resistance problems. On a non-AR-coated bulk Si p-n junction solar cell, formation of a porous Si surface layer increases both internal- and external quantum efficiency (QE) by functioning both as a light-trapping antireflection coating and an effective minority-carrier mirror. Current-voltage (I-V) data indicate that the porous Si layer does not lead to an increase in dark current.

INTRODUCTION

The goal of this research is to demonstrate a new solar cell based on porous Si. Porous Si technology has been developed mainly for producing visible light-emitting diodes (LEDs). Since in porous Si, electrical power injection can produce visible light, the obvious question is how to realize the converse, namely, visible light input, electrical output. Fig. 1 shows the porous Si solar cell concept.

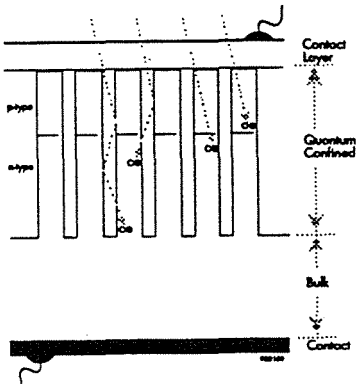

Fig. 1 Porous Si solar cell concept. "Wire" structure leads to quantum confinement and light-trapping effects.

Porous Si can upgrade the performance of single junction Si-based solar cells by more correctly matching the solar spectrum due to the increased band gap. Development of photovoltaic junctions in porous Si will allow for the creation of all-Si monolithic tandem solar cells, ultimately capable of achieving one-sun conversion efficiencies ≈ 30%. The light-trapping and surface-passivation effects of porous Si are also of interest.

We have developed an electrochemical processing technique for preparing Si samples with nanostructural carrier confinement properties, *e.g.* porous Si.[1,2] Since porous Si exhibits intense visible photoluminescence it appears that direct bandgap material is formed.

Photovoltaic Effects in Porous Si Samples

Anderson and co-workers at SUNY-Buffalo[3] prepared photodiodes with an Al contact on the surface of a 4-μm thick porous Si film. Quantum efficiency was 97%, attributed to excellent light trapping by the porous Si, and low recombination velocity at the surface of the quantum confined material. However, the open circuit voltage (V_{oc}) was only ≈ 0.2V. Smestad, Kunst and Vial[4] used a Pt needle to make contact to electrochemically etched p-type Si, and report a photovoltaic response. Under AM1.5 conditions, V_{oc} was 0.36V, although Smestad[5] has earlier suggested that illuminated porous Si should yield higher photovoltages than bulk Si. Recently, a group at NREL described their efforts with applying porous Si technology to the preparation of photovoltaic devices.[6] They found that the presence of porous Si greatly decreased the reflectivity of Si wafers, bringing it as low as 1.5% at 500 nm. However, they also determined that the presence of porous Si actually reduced the minority carrier lifetime for cells having p and n point contacts on the rear surface. No attempts to form junction diodes in the porous Si were reported.

EXPERIMENTAL

Researchers have examined the structure of quantum-confined porous Si and have shown it to possess irregularly shaped islands of ≈10 to 30Å dimensions.[7] It is expected that incoming photons undergo multiple reflections before being absorbed in the wires. Hence, the placement of the pn junction relative to the depth of the etch is a critical parameter in these devices.

Two types of porous Si structures have been formed and used in our solar cell studies. The first, designed to study the effect of a porous Si surface, with the junction undisturbed in the bulk Si, was prepared as follows: We first formed P+/N junction, ≈0.75 μm deep in N-type ≈ three ohm-cm Si by ion implantation of boron. An N+ back surface was created by ion implantation of phosphorus (5×10^{15} cm^{-2}). Wafers were annealed in nitrogen at 900°C for 25 minutes. We used a simple shadow mask to form the top ohmic dot contacts (1.5 mm diameter). Metallization

is Ti/Pd/Au on front and back. Since the front-contact dot is opaque, only the current from photogeneration close to the dot area gets collected. Next thin porous Si was formed by chemical etching the area between the top contacts to a depth of ≈0.25 μm. The spectral response, being that of bulk Si, confirms that the porous layer is thinner than the junction depth. See Fig. 2a. Control cells were formed identically, but with no porous surface layer.

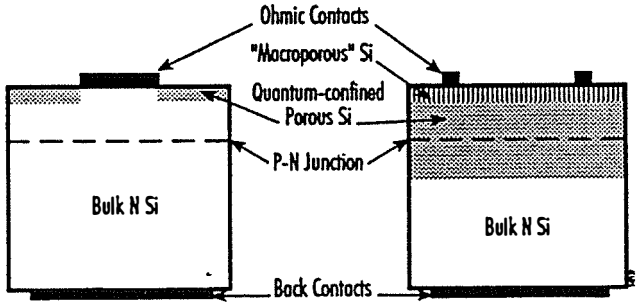

Fig. 2 a) Cell structure with shallow porous Si surface layer. Metal grid contact is to the bulk Si, which contains the junction. b) Cell structure with deep porous Si layer, containing the p-n junction. Metal grid contact is to the porous Si.

Using the second structure, we studied cell properties where the junction is in porous Si material. A junction was formed by ion implantation, similar to above. It should be noted that the P++ surface layer is so highly doped that the rapid etching causes the top few hundred nanometers to become "macroporous," not quantum-confined, Si. This material, having columns that are microns, not angstroms, formation. In this experiment two conductivity levels of Si were used: N-type ≈ three ohm-cm Si, and high-resistivity n^- Si, ≈5000 ohm-cm. Junction depth varies somewhat with Si n-type resistivity since the boron p-type implant recipe was kept constant. Anodic etching with UV illumination was used to form porous Si to a few micron deep. Top metallization was applied, using either a shadow-mask dot or photolithographically defined evaporated grid lines. Only the high-resistivity wafers were successful in allowing the formation of solar cells where the photoresist for narrow grid lines would flow properly to form a uniform pattern. The dot contacts were only done on the three-ohm-cm waters. See Fig. 2b. Control cells with narrow grid lines were formed identically, but with no etching to form the porous material.

Porous Si can be formed to a depth of a few thousand angstroms, by simple chemical etching of conventional Si, using an HF:H_2O: HNO_3 mixture. To produce porous Si to a greater depth, anodic etching is used. For n-type Si material, illumination is required to photogenerate the holes needed for anodization. Formation of quantum-confined porous Si is best done in lightly doped p-type layers. For anodic etching, Si wafers are mounted in a specially designed jig,[8] (Fig. 3) with electrical contact made to the back of each wafer. The process uses a solution of hydrofluoric acid and water in ethanol and a current density of several mA/cm^2.

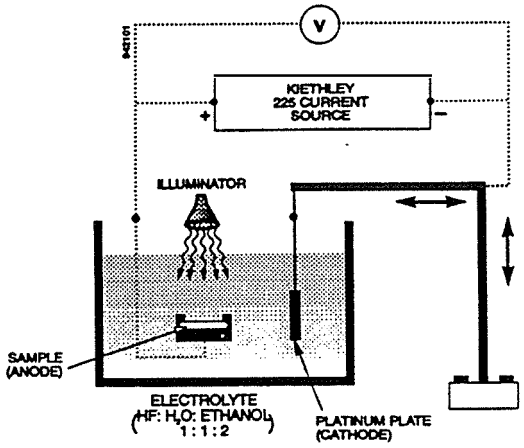

Fig. 3 Anodic etching system used to fabricate porous Si.

RESULTS

Experiment 1: Thin Porous Si Layer on Top of Bulk Si Junction; Metal Dot Contact to Bulk Material

In these devices, a circular Ti/Pd/Au dot as a non-transparent front ohmic contact was formed to the bulk Si before etching to form a shallow surface layer of porous Si. Dark and illuminated characteristics of the cells were measured before and after the porous Si etch step. I-V data reveal that the metal contact was not disturbed by the etching. We found that the photocurrent had increased markedly after the porous Si had been formed.

Using AM1.5G illumination, the bulk Si cell has a measured J_{sc} of 17.42 mA/cm^2 without anti-reflection coating. The fill factor is 66.3%, indicating that we are having some series resistance problems. The measured efficiency was 6.4%. It is clear that we have not optimized our processing at this stage. Fig. 4 shows the results for a device which had the surface converted to porous Si. The sample has J_{sc} ≈ 30.07 mA/cm^2, which appears to be related to the light-trapping properties of porous Si. With this 70% larger photocurrent, we measure V_{oc} of 0.563V. However, the fill factor for this cell is reduced to 51.9%. The measured AM1.5G efficiency of the best device with the porous Si surface is 8.79%.

We measured spectral response and reflectance of the two types of devices. Fig. 5 shows characteristics for the bulk Si device, with and without a porous Si surface. Without AR coating, reflectance is in the range of 30 to 40%. For a device with a porous Si surface, reflectance throughout most of the visible region has been reduced to 10% or less. Also, the internal quantum efficiency is now

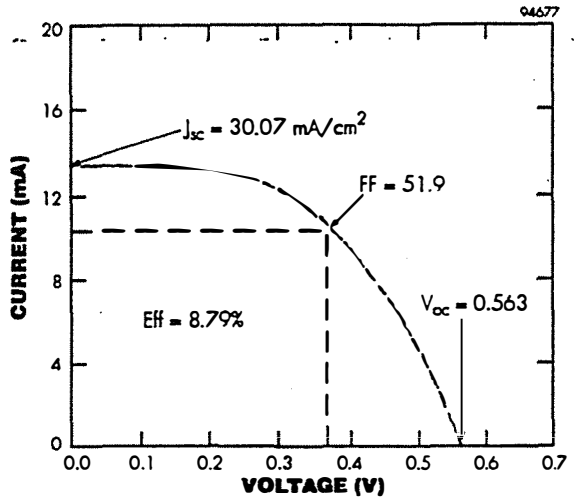

Fig. 4 AM1.5 (global) response of bulk Si solar cell with porous Si surface.

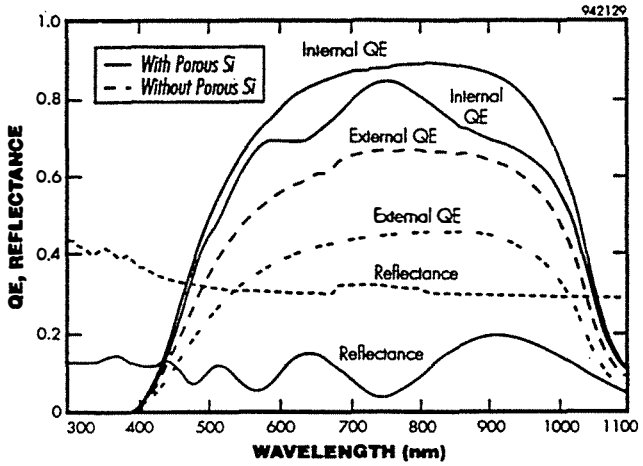

Fig. 5 Measured optical reflectance and quantum efficiency spectra for bulk Si solar cell, with and without porous Si surface layer.

at ≈ 90% from about 600 to 1000 nm. Therefore, we have shown that porous Si makes an effective anti-reflection coating and front-surface passivation for Si solar cells.

It should be noted that the spectral response of the cell with the porous Si surface is basically similar to any bulk Si solar cell. Therefore, most of the current is being generated in the bulk substrate material.

Finally, we measured the dark I-V characteristics of both types of devices. The two characteristics are basically identical. In fact, the n=1 branches of the two curves yield J_{01} values of 4.7 and 5.2 x 10^{-12} A/cm^2. Therefore, we find that our electrochemical processing does not appear to degrade the lifetime of the carriers at the front surface of the diodes. This seems plausible if the porous Si indeed has a larger band gap than the bulk material, leading to the formation of an effective minority carrier mirror.

Experiment 2: Junction within the Deep Porous Si; Dot Contact to Porous Si on Top

In these devices, we formed deep porous Si which penetrated the junction, before the application of the front ohmic contact. Characterization was performed with uncalibrated incandescent (microscope light) illumination. A photovoltaic effect was clearly observed. The I-V characteristics are shown in Fig. 6. In the dark, the device exhibits rectifying behavior, as can be expected from a pn junction. Dark current levels in reverse bias are below the instrument resolution limit on this scale. The photocurrent under white light illumination increases as intensity is raised. For the porous Si device shown, a photocurrent of about 2 μA was generated. The largest V_{oc} measured was 0.11 volts. The low value of V_{oc} is consistent with the small photocurrent.

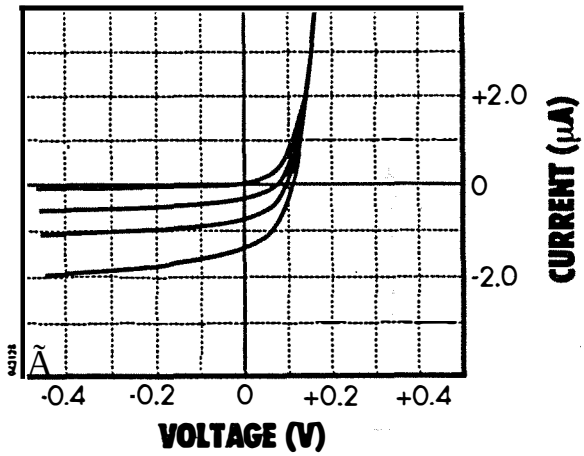

Fig. 6 Current-voltage characteristics of porous Si diode exhibiting photovoltaic characteristics.

We explain the situation as follows. The metal contact is very thick, and cannot pass any light. The only light that is available for generating a photocurrent must be absorbed in the regions around the opaque contact. However, the surface p^+ region is composed of vertical wires, making horizontal carrier transport a difficult problem. We suspect that the only photocurrent we are seeing is generated by light which is scattered under the contact, and absorbed in material below the metal.

A possible way to improve this situation would be to provide a transparent contact material over the entire p-type surface. This conductor would allow the current flowing vertically to be collected and moved to the side, across the surface. We point out that our initial result seems quite promising, because in contrast to previous ITO/porous Si devices, we now see a photocurrent at zero bias.

Experiment 3: Junction within the Deep Porous Si; Metal Grid Lines on Top

Solar cells were attempted on both 3 ohm-cm and 5000 ohm-cm Si substrates with porous Si formed several microns deep. The photoresist adhered well to the high-resistivity wafers, but was problematic on the higher doped ones. The cells on high-resistivity Si are essentially PIN diodes.

Illuminated porous Si cell data are shown in Fig. 7. The V_{oc} is about 0.3V. There is a significant increase in current with reverse bias, something often seen with amorphous Si PIN solar cells. Furthermore, the dark and the illuminated characteristics cross, again reminiscent of amorphous Si. This observation indicates that superposition fails. That is, the illuminated I-V characteristic is not the difference between the photogenerated current and the dark current. Failure of the superposition principle in solar cells often indicates that the photogenerated current is voltage dependent, and that space charge injection effects may be present. An increase in photocurrent with reverse bias often occurs if there is a barrier to carrier collection, which can be overcome by reverse bias. Also, with the low-doped Si, photogenerated carriers may be modulating the series resistance.

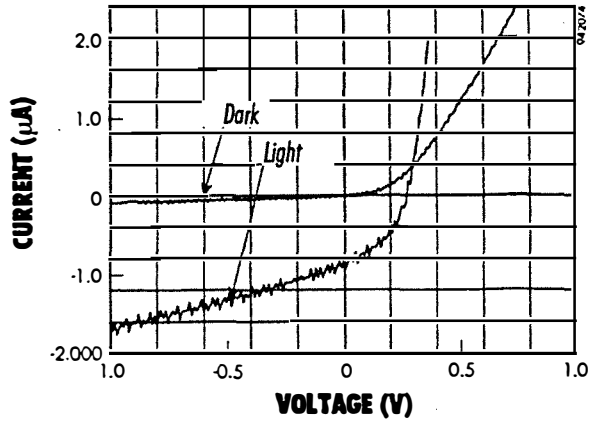

Fig. 7 Current-voltage characteristics, indicating failure of the superposition principle and a voltage-dependent photocurrent.

It is well known that under certain preparation conditions, amorphous Si solar cells exhibit a voltage dependent photocurrent. Trapped charges can reduce the internal electric field in a PIN device, and amorphous Si typically has zero diffusion length. When red light penetrates deeply into the amorphous Si i-region, the carriers are generated in a low field region and become trapped; they recombine without contributing to the photocurrent. Thus the red spectral response is poor or even zero. However, with a reverse bias applied, a field appears across even the deepest regions of the i-layer. This field serves to separate the photogenerated hole-electron pairs before they can be trapped and lost to recombination. Thus the red response is voltage dependent. Generally, the blue response is not voltage dependent because there is always enough of an electric field at the n-i junction.

This field dependence causes the light and dark I-V curves to cross, indicating a failure of the superposition principle. We find the same thing with porous Si solar cells. It appears that the photogenerated carriers formed by blue and green light in the porous silicon are getting trapped at the surface states. If the analogy with amorphous Si is correct, under reverse bias, the blue and green response should improve. We have observed large increases in photocurrent from porous Si under reverse bias.

CONCLUSIONS/SUMMARY

We have shown that porous Si is an interesting material for solar cell applications. The anti-reflection/surface passivation aspects of porous Si layers on bulk Si solar cells have been demonstrated, yielding a 70% increase in photocurrent with no increase in dark current. Photovoltaic effects of porous Si active layers have been observed. Open-circuit voltage of $\approx$ 0.3V has been measured, with short-circuit current increasing with reverse bias. Spreading resistance problem and charge trapping in porous Si are the problems to be overcome for future advances.

ACKNOWLEDGMENTS

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APPENDIX B

HIGH PERFORMANCE POROUS SILICON-BASED SOLAR CELLS

HIGH PERFORMANCE POROUS SILICON-BASED SOLAR CELLS[1]

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ABSTRACT

We have fabricated Si solar cells from porous Si/bulk Si structures. Two cell types, having the junction within the porous Si or within the bulk Si, were studied. We have seen clear evidence of the photovoltaic effect in porous Si, although currents and voltages are low, due to spreading resistance problems. On a non-AR-coated bulk Si P-N junction solar cell, formation of a porous Si surface layer increases both internal- and external quantum efficiency (QE) by functioning both as a light-trapping antireflection coating and an effective minority-carrier mirror. Current-voltage (I-V) data indicate that the porous Si layer does not lead to an increase in the dark current.

INTRODUCTION

The goal of this research is to demonstrate a new solar cell based on porous Si. Porous Si technology has been developed mainly for producing visible light-emitting diodes (LEDs). Since in porous Si, electrical power injection can produce visible light, the obvious question is how to realize the converse, namely, visible light input, electrical output. It is anticipated that porous Si can upgrade the performance of single junction Si-based solar cells by more correctly matching the solar spectrum due to the increased bandgap. Development of photovoltaic junctions in porous Si will allow for the creation of all-Si monolithic tandem solar cells potentially capable of achieving conversion efficiencies greater than 30%. The light-trapping and surface-passivation effects of porous Si are also of interest.

We have developed an electrochemical processing technique for preparing Si samples with nanostructural carrier confinement properties, *e.g.* porous Si.[1,2] Since porous Si exhibits intense visible photoluminescence it appears that direct bandgap material is formed. Anderson and co-workers at SUNY-Buffalo[3] prepared photodiodes with an Al contact on the surface of a 4 μm thick porous Si film. Quantum efficiency was 97%, attributed to excellent light trapping by the porous Si, and low recombination velocity at the surface of the quantum confined material. However, the open circuit voltage (V_{oc}) was only ≈ 0.2V. Smestad, Kunst and Vial[4] used a Pt needle to make contact to electrochemically etched p-type Si, and reported a photovoltaic response. Under AM1.5 conditions, V_{oc} was 0.36V, although Smestad[5] had earlier suggested that illuminated porous Si should yield higher photovoltages than bulk Si. Recently, a group at NREL reported their results on applying porous Si technology to the preparation of photovoltaic devices.[6] They found that the presence of porous Si greatly decreased the reflectivity of Si wafers, bringing it as low as 1.5% at 500 nm. However, they also determined that the presence of porous Si actually reduced the minority-carrier lifetime for cells having p and n point contacts on the rear surface. No attempts to form junction diodes in the porous Si were reported.

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EXPERIMENTAL

In this work, we have used two types of porous Si structures in our solar cell studies. The first structure, as shown on Figure 1a, was designed to study the effect of a thin porous Si surface layer as an antireflection (AR) coating on a bulk Si PN junction cell. To fabricate this device, we first formed P^{++}/ N junction about 0.75 μm deep in an N-type Si wafer (3 Ωcm) by ion implantation of boron. An N^{+} back surface was created by implantation of phosphorous ions. Wafers were annealed in nitrogen at 900°C for 25 minutes. We used a simple shadow mask to form the top ohmic dot-contacts (1.5 mm diameter). Metallization is about 1 μm thick opaque Ti/Pd/Au on front and back. A thin porous Si AR coating was formed next by stain etching of the area surrounding top dot-contact to a depth of about 0.25 μm in a 1:3:5 mixture of $HF:HNO_3:H_2O$.

The second type of structures we studied were cells with PN junction in the porous Si layer. A junction was formed by ion implantation, similar to above, prior to the formation of porous silicon. It should be noted the P^{++} surface layer is so highly doped that the rapid etching causes the top few hundred nanometers to become non-quantum-confined " mesoporous" Si. In this experiment, two conductivity levels of Si were used: N-type Si 3 Ωcm and high resistivity N^{-}-type Si >5000 Ωcm. Junction depth varies somewhat with Si N-type resistivity since the boron P-type implant recipe was kept constant. Anodic etching with UV illumination was used to form porous Si to a few microns deep. Top metallization was applied, using either a shadow mask (Fig. 1b) or photolithographically-defined evaporated grid lines (Fig. 1c).

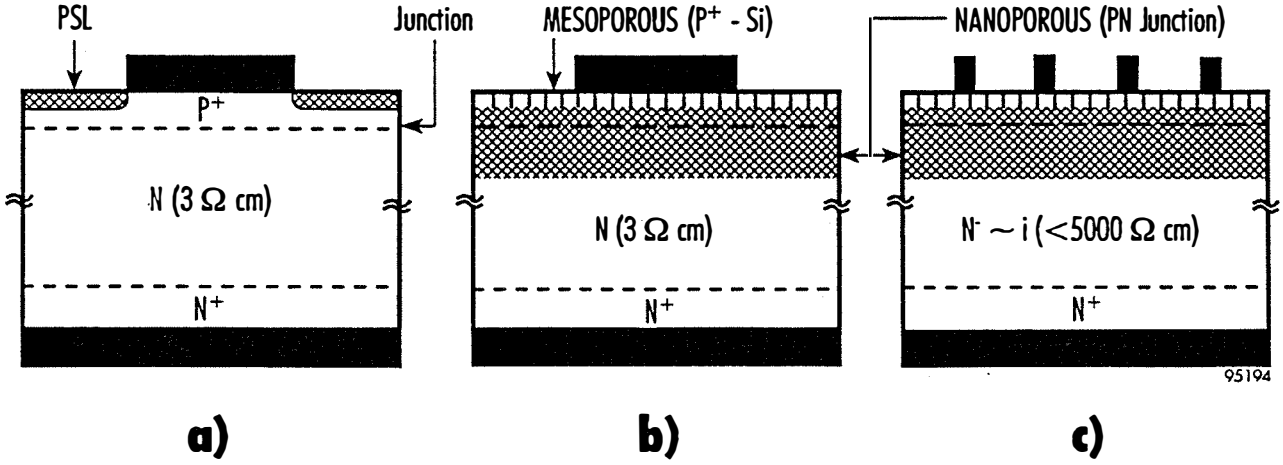

Figure 1 *Cell structure with a) a shallow porous Si antireflection coating with a dot-contact to bulk PN junction, b) a deep porous PN junction with dot-contact on top, and c) a deep porous PIN structure with metal-grid contact on top.*

RESULTS

Experiment 1: Bulk Si PN Junction Cells with a thin Porous Surface

As above-mentioned, in these devices, a circular Ti/Pd/Au dot as a non-transparent front ohmic contact was formed to the bulk Si before etching to form a shallow surface layer of porous Si. Dark and illuminated characteristics of the cells were measured before and after the porous

Si etch step. I-V data reveal that the metal contact was not disturbed by the etching. We found that the photocurrent had increased markedly after the porous Si had been formed. Using AM1.5G illumination, we measure a J_{sc} of 17.42 mA/cm^2 in the control bulk Si cell without porous surfaces or AR coating (Figure 2a). The fill factor is 66.3%, indicating that we are having some series resistance problems. The measured efficiency is 6.4%. It is clear that we have not optimized our processing at this stage. Figure 2b shows the results for a device which had the surface converted to porous Si using stain-etching. The sample has J_{sc} = 30.07 mA/cm^2, which appears to be related to the light-trapping properties of porous Si. With this 70% larger photocurrent, we measure V_{oc} of 0.563V. However, the fill factor for this cell is reduced to 51.9%. The measured AM1.5G efficiency of the best device with the porous Si surface is 8.79%.

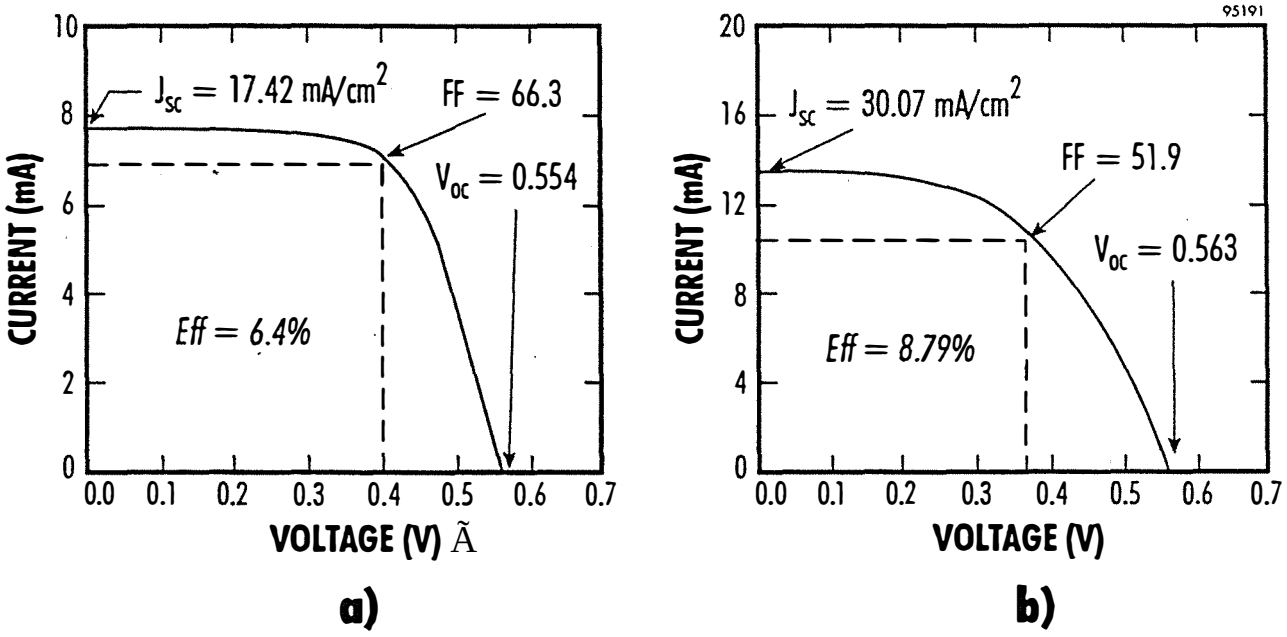

Figure 2 æ *AM1.5 (global) response of bulk Si solar cell a) without, and b) with a porous Si surface layer.*

We measured spectral response and reflectance of the two types of devices. Figure 3 shows characteristics for the bulk Si device, with and without a porous Si surface. Without AR coating, reflectance is in the range of 30 to 40%. For a device with a porous Si surface, reflectance throughout most of the visible region has been reduced to 10% or less. Also, the internal quantum efficiency is now at ≈ 90% from about 600 to 1000 nm. Therefore, we have shown that porous Si makes an effective anti-reflection coating and front-surface passivation for Si solar cells. It should be noted that the spectral response of the cell with the porous Si surface is basically similar to any bulk Si solar cell. Therefore, most of the current is being generated in the bulk substrate material.

Finally, we measured the dark I-V characteristics of both types of devices. The two characteristics were basically identical. In fact, the n=1 branches of the two curves yield J_{01} values of 4.7 and 5.2 x 10^{-12} A/cm^2. Therefore, we find that our electrochemical processing does not appear to degrade the lifetime of the carriers at the front surface of the diodes. This seems plausible if the porous Si indeed has a larger bandgap than the bulk material, leading to the formation of an effective minority-carrier mirror.

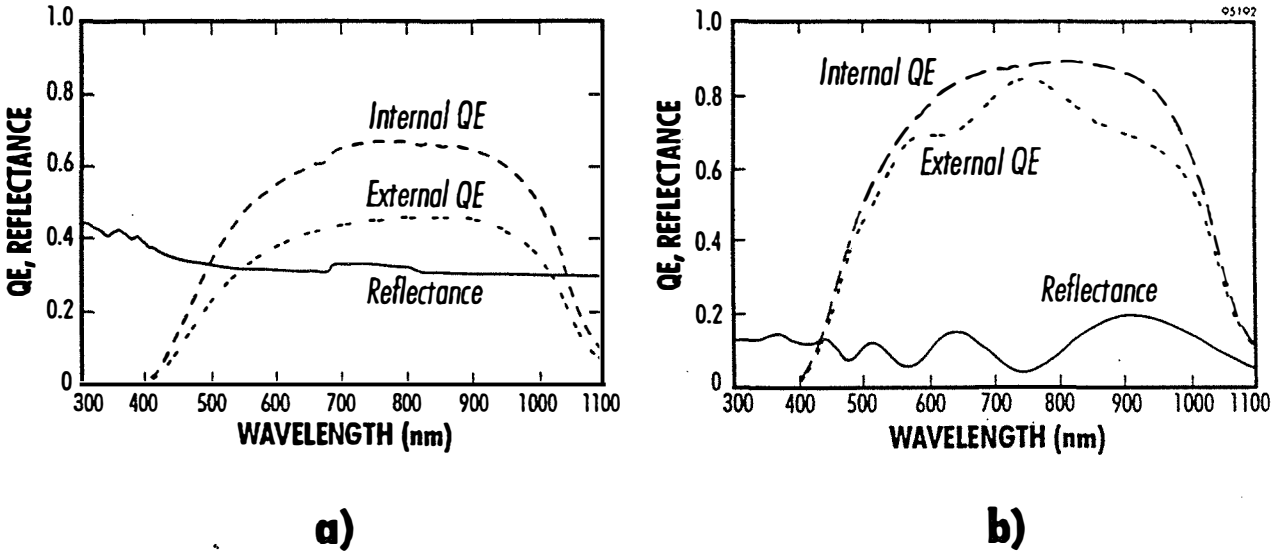

Figure 3 *Measured optical reflectance and quantum efficiency spectra for bulk Si solar cell, with and without porous Si surface layer.*

Experiment 2: PN Junction in a Thick Porous Si Layer

In these devices, we formed by anodic etching deep porous Si which penetrated the junction, before the application of the front ohmic contact. Characterization was performed with uncalibrated incandescent (microscope light) illumination. A photovoltaic effect was clearly observed. The I-V characteristics are shown in Figure 4. In the dark, the device exhibits rectifying behavior, as can be expected from a PN junction. Dark current levels in reverse bias are below the instrument resolution limit on this scale. The photocurrent under white light illumination increases as intensity is raised. For the porous Si device shown, a photocurrent of about 2 μA was generated. The largest V_{oc} measured was 0.11 volts. The low value of V_{oc} is consistent with the small photocurrent.

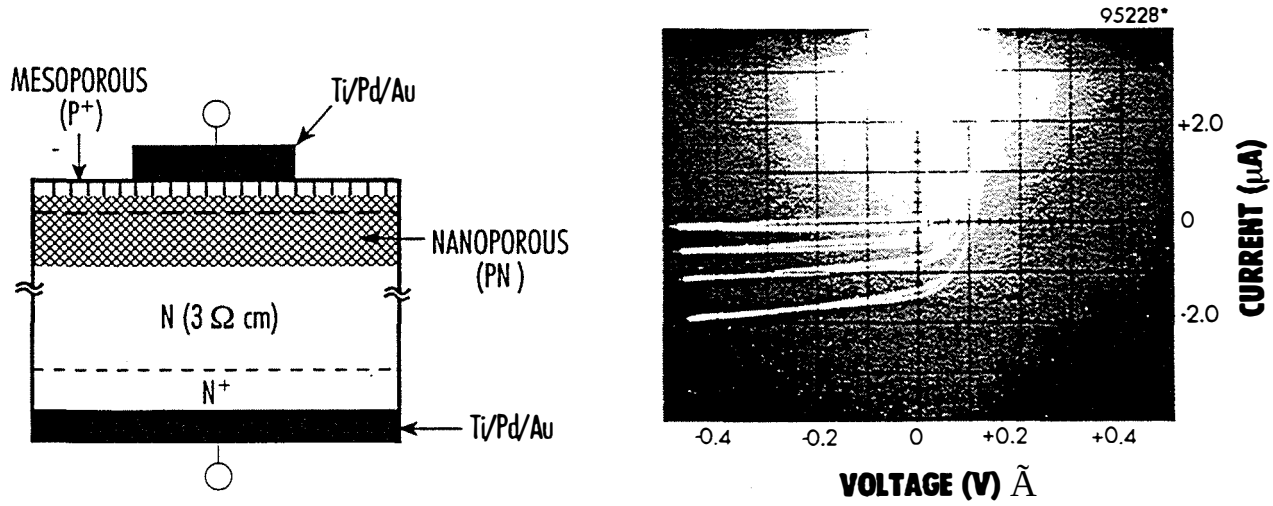

Figure 4 *Current-voltage characteristics of porous Si diode exhibiting photovoltaic behavior.*

We explain the situation as follows. The metal contact is very thick, and cannot pass any light. The only light that is available for generating a photocurrent must be absorbed in the regions around the opaque contact. However, the surface p^+ region is composed of vertical wires, making horizontal carrier transport a difficult problem. We suspect that the only photocurrent we are seeing is generated by light which is scattered under the contact, and absorbed in material below the metal.

A possible way to improve this situation would be to provide a transparent contact material over the entire p-type surface. This conductor would allow the current flowing vertically to be collected and moved to the side, across the surface. We point out that our initial result seems quite promising, because in contrast to previous ITO/porous Si devices, we now see a photocurrent at zero bias.

Experiment 3: PIN Junction in a Thick Porous Si Layer

Illuminated porous Si cell data for porous PIN structures are shown in Figure 5. The V_{oc} is about 0.3V. There is a significant increase in current with reverse bias, something often seen with amorphous Si PIN solar cells. Furthermore, the dark and the illuminated characteristics cross, again reminiscent of amorphous Si. This observation indicates that superposition fails. That is, the illuminated I-V characteristic is not the difference between the photogenerated current and the dark current. Failure of the superposition principle in solar cells often indicates that the photogenerated current is voltage dependent, and that space charge injection effects may be present. An increase in photocurrent with reverse bias often occurs if there is a barrier to carrier collection, which can be overcome by reverse bias. Also, with the low-doped Si, photogenerated carriers may be modulating the series resistance.

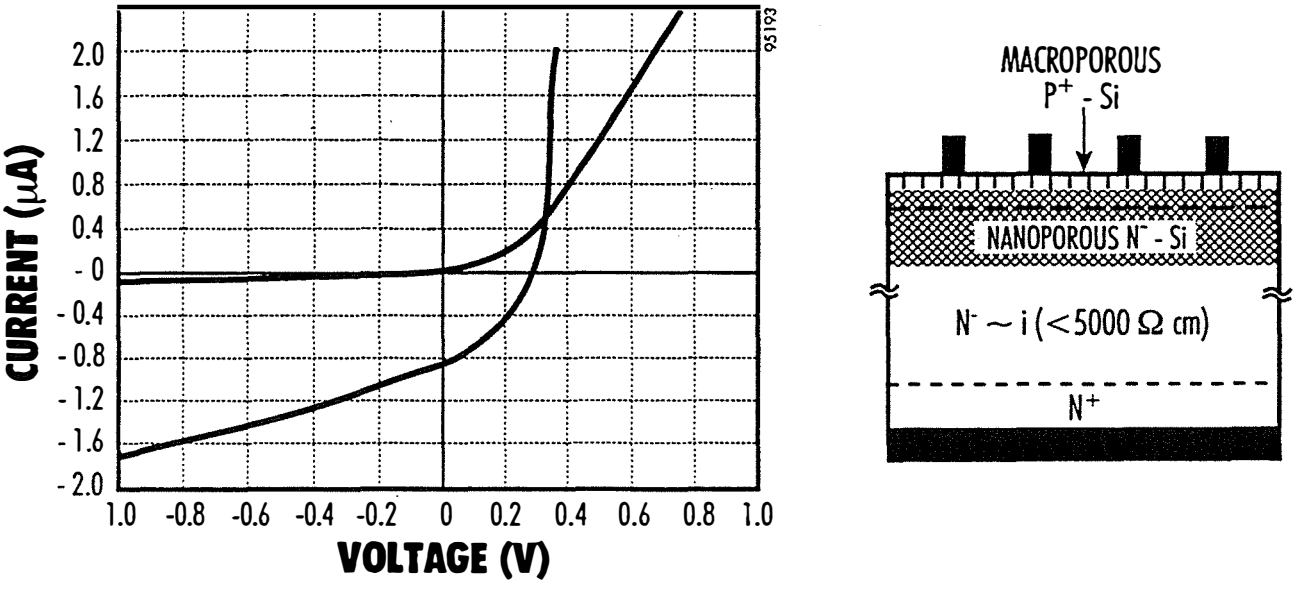

Figure 5 *Current-voltage characteristics, indicating failure of the superposition principle and a voltage-dependent photocurrent in porous PIN structures.*

It is well known that under certain preparation conditions, amorphous Si solar cells exhibit a voltage dependent photocurrent. Trapped charges can reduce the internal electric field in a PIN device, and amorphous Si typically has zero diffusion length. When red light penetrates deeply into the amorphous Si i-region, the carriers are generated in a low field region and become trapped; they recombine without contributing to the photocurrent. Thus the red spectral response is poor or even zero. However, with a reverse bias applied, a field appears across even the deepest regions of the i-layer. This field serves to separate the photogenerated hole-electron pairs before they can be trapped and lost to recombination. Thus, the red response is voltage dependent. Generally, the blue response is not voltage dependent because there is always enough of an electric field at the n-i junction.

This field dependence causes the light and dark I-V curves to cross, indicating a failure of the superposition principle. We find the same thing with porous Si solar cells. It appears that the photogenerated carriers formed by blue and green light in the porous silicon are getting trapped at the surface states. If the analogy with amorphous Si is correct, under reverse bias, the blue and green response should improve. We have observed large increases in photocurrent from porous Si under reverse bias.

CONCLUSIONS/SUMMARY

We have shown that porous Si is an interesting material for solar cell applications. The antireflection/surface passivation aspects of porous Si layers on bulk Si solar cells have been demonstrated, yielding a 70% increase in photocurrent with no increase in dark current. Photovoltaic effects of porous Si active layers have been observed. V_{oc} of $\approx$ 0.3V has been measured, with short-circuit current increasing with reverse bias. Spreading resistance problem and charge trapping in porous Si are the problems to be overcome for future advances.

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The goal of the program was to demonstrate the use of porous silicon in new solar cell structures. Porous silicon technology has been developed at Spire for producing visible light-emitting diodes (LEDs). We demonstrated the following major aspects: porous silicon active layers have been made to show photovoltaic action; porous silicon surface layers can act as antireflection coating to improve the performance of single-crystal silicon solar cells; porous silicon surface layers can act as antireflection coatings on polycrystalline silicon solar cells. One problem with the use of porous silicon is the inability to achieve good lateral conduction of electrons and holes through the material. This problem shows up in terms of poor blue response and photocurrents that increase with reverse bias applied to the diode.

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