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Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvements

Semiannual Technical Report 1 January 1996 - 30 June 1996

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Frederick, Maryland

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1617 Cole Boulevard
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PREFACE

This Semiannual Technical Progress Report covers the work performed by Solarex for the period January 1, 1996 to June 30, 1996 under DOE/NREL Subcontract # ZAI-4-11294-01 entitled "Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvements". This is the third Semiannual Technical Report for this subcontract. The subcontract is scheduled to run from December 8, 1993 to December 7, 1996.

The following personnel at Solarex have contributed to the technical efforts covered in this report.

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In addition, Solarex has been supported by the staff at the Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI). ARRI staff working on the subcontract include:

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EXECUTIVE SUMMARY

The objective of this three-year program is to advance Solarex's cast polycrystalline silicon manufacturing technology, reduce module production cost, increase module performance and expand Solarex's commercial production capacities. Two specific objectives of this program are to reduce the manufacturing cost for polycrystalline silicon PV modules to less than $1.20/watt and to increase the manufacturing capacity by a factor of three. To achieve these objectives, Solarex is working in the following technical areas:

CASTING

The goal of the casting task is to develop the ability to cast ingots that yield four bricks with a cross-section of 15 cm by 15 cm with at least equivalent material quality as now achieved for 11.4 cm by 11.4 cm bricks. This represents a 73% increase in the useable silicon obtained from each casting.

WIRE SAWS

The goal of the wire saw task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μm centers at lower cost per cut than achieved today on the ID saws. This represents a 50% increase in the useable silicon obtained from each cast and a 50% increase in the yield of wafers per purchased kilogram of Si feedstock.

CELL PROCESS

The goal of the cell task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. The developed process must be compatible with automated manufacturing at large volumes.

MODULE ASSEMBLY

The goal of the module assembly task is to modify Solarex's present module assembly system to increase throughput by 100% and decrease the labor requirement by 50%. The Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI) is to work with Solarex to model the present automated module assembly system and to recommend modifications to increase throughput and reduce labor.

FRAMELESS MODULE DEVELOPMENT

The goal of the frameless module task is to develop and qualify a frameless module design incorporating a lower cost back sheet material (less than $0.05/square foot) and user friendly, low cost electrical termination (less than $1.00/module). Since PVMaT is designed for large systems, modules can be designed to mount directly onto the support structure without integral frames.

AUTOMATED CELL HANDLING

The goal of the automated cell handling task is to develop automated handling equipment for 200 μm thick 15 cm by 15 cm polycrystalline silicon wafers and cells with a high yield (less than 0.1% breakage per process handling step) at a throughput rate of at least 12 cells or wafers per minute.

ACCOMPLISHMENTS

Accomplishments during the reporting period include:

- Began conversion of production casting stations to increase ingot size.
- Operated the wire saw in a production mode with higher yields and lower costs than achieved on the ID saws.
- Purchased and installed an additional wire saw.
- Developed and qualified a new wire guide coating material that doubles the wire guide lifetime and produces significantly less scatter in wafer thickness.
- Completed a third pilot run of the cost effective Al paste back surface field process, verifying a 5% increase in cell efficiency and demonstrating the ability to process and handle the BSF paste cells.
- Environmental qualification of modules using cells produced by an all print metallization process.
- Optimized the design of the 15.2 cm by 15.2 cm polycrystalline silicon solar cells.
- Demonstrated the application of a high efficiency process in making 15.2 cm by 15.2 cm solar cells.
- Demonstrated that cell efficiency increases with decreasing wafer thickness for the Al paste BSF cells.
- Qualified a vendor supplied Tedlar/EVA laminate to replace the combination of separate sheets of EVA and Tedlar backsheet.
- Demonstrated the operation of a prototype unit to trim/lead attach/test modules.
- Demonstrated the operation of a wafer pull down system for cassetting wet wafers.
- Presented three PVMaT related papers at the 25th IEEE Photovoltaic Specialist Conference.

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1.0 INTRODUCTION

The goal of Solarex's Crystalline PVMaT program is to improve the present Polycrystalline Silicon manufacturing facility to reduce cost, improve efficiency and increase production capacity. Key components of the program are:

- Casting of larger ingots.
- Use of wire saws to cut thinner, larger size wafers with less kerf loss.
- Transfer of higher efficiency cell processes to manufacturing.
- Increased automation in module assembly.
- High reliability mounting techniques for frameless modules.
- Automated handling of large, thin wafers.

The results of these efforts will be to reduce the module cost per watt to less than $1.20/watt, to increase the production capacity of Solarex's Frederick plant by a factor of 3 and to provide larger, higher efficiency modules that reduce the customer's balance of systems cost. All of this is to be achieved without sacrificing the high reliability already achieved with the crystalline modules in use today.

The rationale behind the Solarex program is to use as much as possible of the present equipment and processes, making improvements that lead to larger sizes, better utilization of materials, higher efficiencies and reduced labor requirements. In this way the maximum increase in capacity and reduction in cost can be achieved with justifiable capital investments in equipment modifications. Specific areas to be addressed in the program are discussed briefly below.

When the PVMaT Program began, Solarex was casting ingots from which 4 bricks, each 11.4 cm by 11.4 cm in cross section were cut. The stations themselves are physically capable of holding an ingot that would be large enough to cut 4 bricks 15 cm by 15 cm in cross-section or 9 bricks 11.4 cm by 11.4 cm. Task 12 involved making the modifications in equipment and process necessary to cast larger ingots. This effort will lead to an increase in the production capacity of Solarex's casting stations and reduce the labor content.

Wire saws can be used to cut thinner wafers with less kerf, than is possible on the Internal Diameter (ID) saws. The program goal is to reduce the center to center cut distance from 600 microns on the ID saw to 400 microns on the wire saw. This will result in a 50% increase in solar cell and module output from the same silicon feedstock purchased and cast. That is, with the same amount of feedstock material and the same casting capacity Solarex will be able to increase its output of PV modules by 50% (on top of the increase achieved by casting larger ingots). In addition, wire saws can also be utilized to cut larger wafers, something ID saws can not do.

Finally, wire saws have a much higher production capacity than ID saws. One wire is producing as many wafers as 16 ID saws. To increase capacity with wire saws requires a much smaller capital investment than would be required to achieve the same increase with ID saws. The major issue with wire saws was the ability to reduce the variable cost to cut a wafer. This has been successfully demonstrated. Efforts under task 13 involve continued cost reductions particularly in the areas of slurry formulation and automation of the wafer clean-up process.

In this program, Solarex is working on the transfer of high efficiency cell technologies from the laboratory to production. Issues involved in the successful transfer include process cost, ability to scale to large volume, adaptability to automation and the degree to which each step integrates into the overall cell process sequence. Therefore, it is necessary as a part of this program to evaluate each component of the sequence that has proven effective at increasing cell efficiency to determine the most cost effective cell process sequence. Specific areas under investigation during the second year include:

- Optical Coupling
  - mechanical texturing
  - chemical texturing

- Passivation/Gettering á
  - phosphorous gettering

- Back Surface Field (BSF) Formation
  - Al paste BSF

The goal of the Task 14 cell effort is to increase average cell efficiency (as obtained from a production line, not just from the laboratory) to 15% as measured at STC (Standard Test Conditions - 1000 W/m^2, AM1.5, 25° C). This must be achieved with an integrated process sequence that lowers the overall module $/Watt manufacturing cost.

At the start of this PVMaT Program, Solarex had a first generation automation system in use at the Frederick facility for tabbing, matrixing and lay-up of the PV modules. During Task 4 the system was evaluated to determine how it could be modified to increase production throughput, yield and process control and to minimize production labor and cost. To assist with this effort, the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington served as a subcontractor. ARRI has assisted Solarex in analysis, modeling and development of handling concepts to improve the operation of the module assembly area. In Task 9 the assembly area was modified as modeled, leading to a doubling in assembly capacity. Task 15 efforts are now underway to design a module assembly system that will again double the manufacturing capacity of this area.

Solarex modules use low iron tempered glass as a superstrate and Ethylene Vinyl Acetate (EVA) as the encapsulation system. No change is proposed in this encapsulation system to maintain the module reliability. However, a reduction in the cost of the backsheet was achieved during Task 5 without negatively impacting the module reliability.

Today most PV modules are sold with a frame to provide means for mounting the module and a junction box for electrical connection. This frame is the largest single contributor to module cost. In large systems, the support provided by the system structure is adequate making the module frame redundant. Eliminating this frame can reduce the module selling price by more than $0.50/Watt. During Task 10, testing of a candidate frameless module mounting schemes was completed and this mounting technique was utilized in a large scale PV system at SMUD.

Similarly, the junction box adds appreciable cost to the module, while requiring additional labor for system assembly. In Task 10, a simpler electrical termination scheme costing less than $1.00 per module was tested and qualified for use.

Task 5 also included the design of a nominal 122 watt module using 36- 15.2 cm by 15.2 cm solar cells. Tasks 10 and 15 include qualification of the design through accelerated environmental tests (CEC-503, IEC-1215, UL 1703, and IEEE-1262) and design of the automated equipment necessary to finish the module.

An important issue for many crystalline silicon PV manufacturers is the ability to handle thinner and larger wafers through the production line. Task 11 and 17 are addressing this issue. Once again, Solarex is supported in this effort by ARRI, whose background and experience is ideally matched to the task of developing handling methods for parts such as the large thin wafers to be used in this program. ARRI has perform detailed analysis and modeling of the requirements for thin wafer handling. Prototype wafer handling stations have been built and tested. Design of production units is now underway.

The results of this program will be the modification of today's polycrystalline production facility to:

- Increase production capacity by a factor of three
- Reduce the "profitable" selling price.

Solarex plans to continue an aggressive market development program that would support the increased capacity obtained as a result of this program.

2.0 BASELINE PROCESS AND PRODUCTS

Solarex's Crystalline Silicon Technology is based on use of cast polycrystalline silicon wafers. The process flow used at the beginning of this PVMaT program is shown in Table 1. The primary product was a module with 36 solar cells each 11.4 cm x 11.4 cm, that produces 60 or 64 Watts under Standard Test Conditions (STC).

Table 1
Baseline Cast Polycrystalline Si Process Sequence

Casting

ID Wafering

Cell Process
(Thick Film Print)

Module Assembly

Lamination

Finishing

The various segments of Solarex's module manufacturing process as practiced at the beginning of this PVMaT program are described below.

Casting

Solarex has developed and patented a directional solidification casting process specifically designed for photovoltaics[1]. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semicrystalline silicon ingot. In house manufacture of low cost, high purity ceramics is a key to the low cost fabrication of Solarex semicrystalline wafers[2].

The casting process is performed in Solarex designed casting stations. The casting operation is computer controlled. There are no moving parts (except for the loading and unloading) so the growth process proceeds with virtually no operator intervention.

Wafering

Wafering was done with Internal Diameter (ID) saws. These are the same saws that are used in the semiconductor industry to wafer single crystal CZ ingots. Solarex has many years of experience with these ID saws, resulting in low labor and process costs. This is a mature technology with little opportunity for significant increases in productivity or reduction in kerf loss.

Cell Process

The cell process sequence is based on the use of Thick Film Paste (TFP) metallization, where a commercially available screen printed silver paste is applied as the current carrying grid on the front of the solar cell. This process has been designed to be as cost effective as possible. The high temperature process steps including diffusion, firing of the front print paste and Chemical Vapor Deposition (CVD) of a TiO_2 antireflective (AR) coating are all performed in belt furnaces.

Polycrystalline cells processed through this line have an average cell efficiency of 12.5 to 13% at STC. There are many modifications to this process sequence that can increase cell efficiencies. However, many of these modifications would actually increase the total dollar per watt module cost rather than decrease it. Detailed cost analyses indicate what changes in cell processing can lead to both higher cell efficiencies and lower dollar per watt module cost.[3,4] Implementation of these changes require laboratory verification of the candidate process sequences as well as improvement in the accuracy of the input cost data.

Module Assembly

The first part of the module assembly sequence is to solder two solder plated copper tabs onto the front of the solar cells. Each tab is soldered in 4 places for reliability and redundancy. Solarex uses automated machines to perform the tabbing. Tabbed cells are then laid up into a 36 cell matrix by a robot. The tabs are then soldered to the backs of the solar cells using automated equipment. Each tab has 2 back solder joints.

Module Lamination

The module construction consisted of a low iron, tempered glass superstrate, EVA encapsulant and a 3 part Polyethylene-Mylar-Tedlar backsheet. A single sheet layer of Tedlar replaced the 3 part backsheet during the first year of the program. The lamination process, including the cure, is performed in a vacuum lamination system. Then the modules are trimmed and the leads are attached. Finally, every module is flash tested to determine its STC power output.

Finishing

Most modules are sold with a frame to protect the edges and provide a means of mounting. Solarex uses an extruded aluminum frame that is attached both with a butyl rubber adhesive between frame and glass as well as with 2 screws in each corner of the frame. The framing process is performed by an automatic, robotic framing system.

Most modules are also sold with a junction box to protect the output wiring and provide the terminals for electrically connecting the module to the balance of the system. The area where the lead wires are attached to the module is potted to protect the laminate from moisture incursion. The junction box is then attached to the module with adhesive to seal it to the back of the laminate.

3.0 PVMaT PROGRAM EFFORTS

The following sections detail the progress made during the first six months of 1996.

3.1 TASK 12 - POLYCRYSTALLINE SILICON CASTING IMPROVEMENTS

The original goal of the casting task was to develop the ability to cast ingots that yield four 15 cm by 15 cm bricks with at least equivalent material quality as was achieved for the standard 11.4 cm by 11.4 cm bricks. This was demonstrated in the laboratory during the first two years of the program, yielding equivalent quality ingots with a 73% increase in the useable silicon obtained from each casting.

Most of Solarex's products are still based on the use of 11.4 cm by 11.4 cm solar cells, so an effort was undertaken to develop casting of ingots large enough to produce 9 x 11.4 cm by 11.4 cm bricks. Such an ingot requires approximately 20% more silicon than the PVMaT ingot. The initial efforts to cast these "mongo" ingots required changes in the insulation and receiver, but utilized the same pour crucible as the PVMaT ingot.

Recent laboratory efforts have involved the optimization of the casting process for these larger ingots. Several iterations of heater and insulation design have been guided by experimental results from brick lifetime measurements and cell results. Material with equivalent quality to the standard size ingot has been obtained.

Based on these experimental results a cost analysis was performed to determine whether expansion of the casting stations was economic. The analysis indicated that the casting capacity could be doubled. The cost of this added capacity would be 20% of the cost required to add a similar amount of capacity by purchasing new casting stations. Based on these results, Solarex has begun to modify the production casting stations to the larger configuration. Manufacturing will be switching to Mongo ingots during the later half of 1996.

3.2 TASK 13 - WIRE SAW IMPROVEMENTS

The goal of this task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μm centers at lower cost per cut than achieved today on the ID saws. This represents a 50% increase in the useable silicon obtained from each cast and a 50% increase in the yield of wafers per purchased kilogram of Si feedstock.

3.2.1 Wire Saw Operations

Solarex is utilizing an HCT wire saw in this program. The saw has successfully demonstrated the ability to cut a variety of wafer sizes including 11.4 cm by 11.4 cm, 11.4 cm by 15.2 cm and 15.2 cm by 15.2 cm on centers from 500 μm down to 400 μm. The saw has been operated in a production mode, producing as many wafer as 16 ID saws at better yields and lower per wafer cost than the ID saws. This saw has been so successful that Solarex has procured an additional HCT wire saw.

The major efforts during the second year were to:

- prepare detailed process specifications for the saw and then release it to manufacturing for 24 hour a day operation.

- identification and procurement of another HCT wire saw.

- Development of an improved wire guide coating that doubled the wire guide life while reducing the deviation of wafer thickness, especially toward the end of wire guide life.

3.2.2 Demounting and Cleaning

After wafers have been cut on the wire saw they must be removed from the hold down plate, placed in cassettes and cleaned. Today this process is done manually. An automated process is necessary to reduce cost and increase yield especially as the volume of wire saw wafers increases and the thickness of the wafers decreases.

ARRI has performed set of experiments to gain a quantitative understanding of the forces involved in wafer separation under both dry and wet conditions. Results of these tests were reported in the second Annual Report of this contract[4]. They found that the presence of water between the wafers increases dramatically both the sliding and normal forces required for separation. In the sliding tests, the separation force is greatest under semi-wet conditions. When the water layer is thick, the force required to separate the wafers is much lower. Normal separation pull forces, however, are strongest under a fully wet condition. The pull forces required to separate semi-wet and wet wafers are well within the breakage-causing range, as happened with several of the samples tested.

These results indicate that it would be best to dry the wafers before destacking. However, the present cleaning solvent dries slowly. When we began evaluating the use of a solvent that would dry more quickly, we realized that evaporating slowly is an important feature of the solvent, since it raises the flash point and minimizes the release of organic vapors into the air. Therefore, use of a more rapidly drying cleaning solvent is not recommended.

ARRI then proceeded to develop prototype equipment to destack wafers into cassettes that could be utilized on wet or semi-wet wafers. In this design the stack of wafers lies horizontally. A roller presses against the first wafer in the stack, pulling it downward through a slot into a cassette. The cassette is then index to accept the next wafer. This concept has the following advantages:

- It requires a single indexing slide rather than say a robotic pick and place.
- It requires relatively simple equipment.
- It is a rapid process with a low cycle time.
- It is highly energy efficient since it uses gravity to place the wafer in the cassette.

A prototype wafer pull down system has been built and tested. This concept worked very well for both dry and wet wafers. The prototype has operated through thousands of cycles without breaking any wafers and with successful feeding of a single wafer more than 99.95% of the time. A full production machine will be built based on this design.

3.3 TASK 14 - HIGH EFFICIENCY CELL DEVELOPMENT

The goal of this task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. While a number of approaches to achieving high efficiency have been reported, many of these utilize processes and material that are not likely to be cost effective when applied to cast polycrystalline silicon in a manufacturing environment. The key to achieving the goal of this task is to select modifications to the present process that increase efficiency while lowering the cost per watt. That is, the increased cost of the process is less than the value of the increased power produced by the improvement.[5] During the period cover by this report, the major cell task efforts were in the areas of back surface fields (BSF), development of an integrated cell process and optimization of the design for the 15.2 cm by 15.2 cm solar cell. Each of these areas is discussed below:

3.3.1 Back Surface Field Formation

In the first Annual Report[6] of this program, we reported that an aluminum paste back surface field (BSF) could be used to cost effectively increase cell efficiency by approximately 5%. In the second Annual Report[4] of the program we reported on manufacturing trials, environmental qualification of cells made with the Al paste in a module package, evaluation of the impact of cell thickness and development of an all screen printed process. Efforts during this reporting period included:

- Development and environmental qualification of an all print metallization system.
- Continued work on a single fire process.
- Set-up and initial pilot operation of a prototype production system (auto-printer and belt furnace) for producing a significant quantity of BSF cells on a continuous basis.

The initial back surface field work utilized Solarex's standard back spray process on top of the fired aluminum paste. This is not the most cost effective sequence, since both back spray and the BSF process provide enough back conductivity to produce high efficiency cells. Therefore we began work on a process to replace backspray with a screen printed Ag-Al paste grid. Table 2 shows the comparison of using either back spray or back print over the Al paste BSF back. These cells were measured in the standard fashion with the back on a metallic test block. While both processes yield good cells, the back spray cells do have a better fill factor.

Table 2
Backspray versus Back Print over BSF

	Efficiency (%)	Jsc (mA/cm^2)	Voc (mV)	FF (%)
Backspray	13.2	31.1	582.6	73.1
Back Print (1)	13.11	31.0	581.8	72.6
Back Print (2)	13.03	31.0	582.0	72.1

Configuration 1 had the Ag beneath the Al
Configuration 2 had the Ag on top of the Al

To better understand the performance of these cells, the cells were remeasured using back probes where solder bonds would normally go rather than a test block. The change in measured

performance is shown in Table 3. This back print pattern does not provide as much conductive path as the back spray process.

Table 3
Change in Performance with Probes versus Test Block

	Change in Efficiency (%)	Change in Jsc (%)	Change in Voc (%)	Change in FF (%)
Back Spray	0.1	-0.1	-0.3	0.5
Back Print (1)	-2.1	0	-0.4	-1.7
Back Print (2)	-2.3	-0.1	-0.5	-1.7

To convince ourselves that the reduced fill factor for the all print system was real, we fabricated cells via the two processes and then matched the best 36 cells. Table 4 shows the cell results, while Table 5 shows the module results. The difference in cell fill factor translates directly into a difference in module fill factor.

Table 4
Cells from Backspray versus Back Print Trial

	Efficiency (%)	Jsc ($mAmp/cm^2$)	Voc (mV)	FF (%)
Back Spray	13.65	31.0	584.4	75.3
Back Print	13.51	31.1	584.4	74.4
Difference (%)	-1.0	0.1	0	-1.1

Table 5
Modules from Backspray versus Back Print Trial

	Efficiency (%)	Jsc ($mAmp/cm^2$)	Voc (V)	FF (%)
Back Spray	14.22	32.19	21.3	74.5
Back Print	14.01	32.22	21.3	73.5
Difference (%)	-1.5	0.1	0	-1.5

Analysis of the fill factor loss shows that it is the thick sprayed metal parallel to the direction of current flow (and the interconnect ribbons) that is responsible for the better fill factor of the sprayed cells. The print system will now be modified to increase the conductivity in that direction.

Modules made with the all print metallization system were subjected to environmental qualification testing per IEC-1215 and IEEE-1262 with the addition of a second 200 thermal cycles as required for Solarex's 20 year warranty. The BSF modules successfully completed the testing with all power losses well below the maximum allowable by IEC-1215 with no measurable differences between the BSF and standard cell modules subjected to qualification at the same time.

The Al paste BSF work reported above involved a process with separate firings for the back and front pastes. It would be less expensive, require less equipment and eliminate the potential of the second firing causing metal beading problems, if the front and back pastes can be fired simultaneously. A Design of Experiment trial was performed to optimize the parameters of the single fire process. The optimized process was then used in a split lot trial to compare the single fire with the two fire process. The results are shown in Table 6. The two fire process produced better efficiency cells. Unless there are changes made to the formulations of the pastes, we will have to stick with the two fire system to achieve optimum performance.

Table 6
Two Fire versus Single Fire BSF Process

Process	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Two Fire	13.28	4.023	583.4	73.5
Single Fire	12.92	3.927	580.3	73.7

3.3.2 Integrated Cell Sequence

A high efficiency integrated cell process sequence that includes mechanical texturing, surface passivation, phosphorus gettering and back surface field formation has been developed. Cells were fabricated on 130 cm^2 multicrystalline silicon wafers and then encapsulated with EVA and low iron glass using Solarex's baseline encapsulation process. Solar cells with an encapsulated cell efficiency of nearly 15% were obtained. Encapsulated cell results are presented in Table 7.

Table 7
Performance of Encapsulated Cells from Integrated Process Sequence

	Efficiency (%)	Jsc ($mAmp/cm^2$)	Voc (mV)	FF (%)
Planar Poly	14.0	32.28	599	72.5
Integrated	14.88	33.04	600	75.1

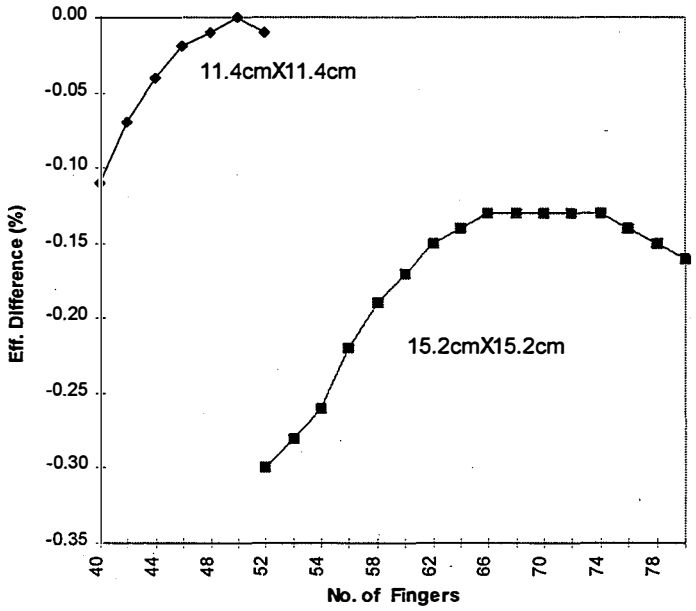
3.3.3 15.2 cm by 15.2 cm Solar Cell Design

In the second Annual Report[4] of the program we reported on the preliminary design of the grid pattern for the 15.2 cm by 15.2 cm solar cell. The model predicted optimal performance for the same grid spacing as utilized on the 11.4 cm by 11.4 cm solar cells. With that design, the model predicts that the efficiency will drop from 12.83% for the 11.4 cm by 11.4 cm solar cell to 12.61% for the 15.2 cm by 15.2 cm solar cell.

The program goal, however, is to use shallow emitters, a back surface fields, mechanical texturing and emitter surface passivation to increase cell efficiencies. Adding these steps to the process sequence results in an increase of at least 10% in the short circuit current of a cast multicrystalline cell. The grids for these higher efficiency cells must be reoptimized to take into

account the higher current density and to compensate for the increased path length due to mechanical texturing. Figure 1 illustrates the predicted variation in efficiency as a function of the number of fingers for 130 cm^2 and 230 cm^2 high efficiency cells. Because of the higher current density, longer path length and higher emitter sheet resistance, the high efficiency, large area cells require more grid lines.

Figure 1
Calculated Cell Performance as a Function of Grid Lines for the Integrated Process Sequence



3.4 TASK 15 - AUTOMATED MODULE ASSEMBLY

The goal of this task is to modify Solarex's present automated matrix and module lay-up system to increase throughput by 100% and decrease the labor requirement by 50%. To assist Solarex in analyzing how this equipment can be improved to increase capacity and reduce labor, the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington is serving as a subcontractor.

During the first year of the contract ARRI modeled and analyzed the manufacturing process. As a short term goal they identified changes necessary to increase module assembly production capacity by 40% to meet Solarex's short term business plan. These changes were successfully implemented during that year[6].

The second phase of the program Solarex and ARRI developed a new factory concept that would allow for incremental increases to meet the shorter term capacity requirements and would ultimately result in achieving Solarex's announced goal of tripling the module assembly capacity. The plan was based on replacing the back solder robots with XY positioners to increase the number of solder bonds made at one time from 2 to 4, thereby increasing the through-put by

nearly a factor of two. This modification was implemented during the second year of the program[4].

During this period ARRI continued to support Solarex to improve and streamline the module assembly operation. Areas of emphasis are:

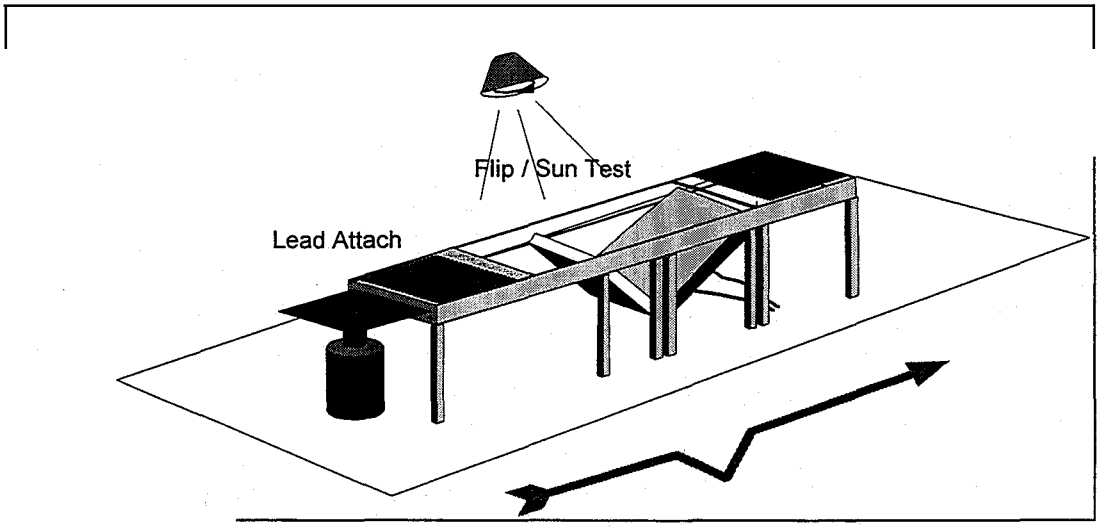
EVA handling

The properties of the EVA we use today will not allow us to roll it out and cut it directly onto the glass. Our EVA vendor, Springborn, has now developed a process that allows EVA to be used directly off of a roll. This approach can now be built into future designs.

Trim/Lead Attach

ARRI designed a prototype work station for inspection, lead attach and testing without requiring operators to lift large modules. The prototype system consists of a rotating table for trimming, a conveyor for lead attach, a flip station for large modules and a section for flash test and visual inspection. See Figure 2. The prototype was delivered to Solarex for testing. During testing several problems were identified including tearing of the backsheet on the rollers and a tendency for operators to hit their hand on the support structure during the trimming operation. These issues are being addressed in the design of a production unit.

Figure 2
Trim/Lead Attach/Test Work Station



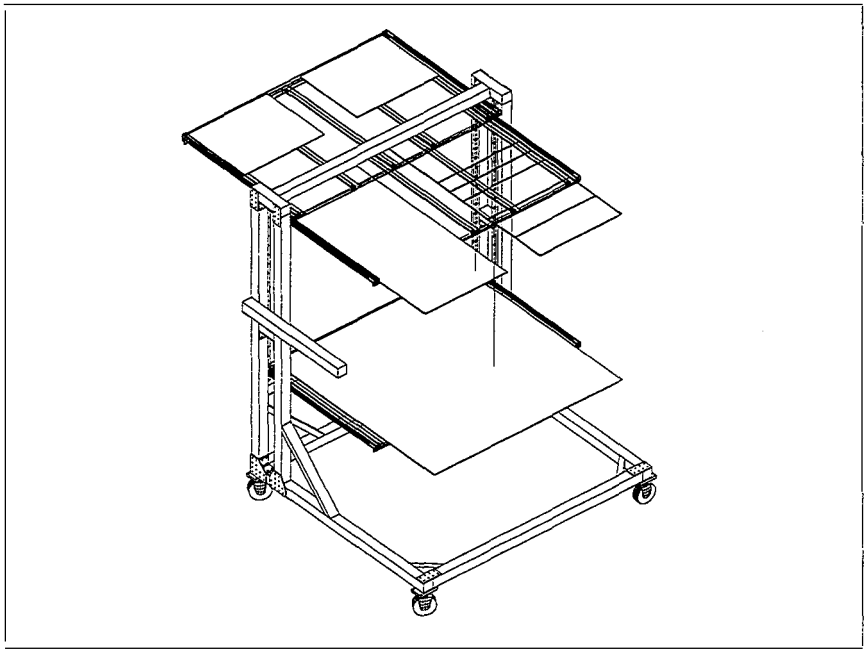
Module Transfer Cart

ARRI designed a common module transfer cart to be used to transfer modules from the laminator through the framing operation to reduce operator lifting of the modules. The cart has 20 shelves that slide in and out. The cart is shown in Figure 3, with only 3 shelves drawn in for clarity. The bottom and the second from the top shelves are shown in the position where the operator will

load the laminates, while the top shelf is shown rolled back in the storage position. To unload, the manipulator can grip each laminate after rolling back the shelf immediately above it.

The prototype cart has been delivered to Solarex, but it too large to be used on the production floor as it is arranged today. During the next planned expansion the aisles between equipment will have to be increased to provide space for the cart to move.

Figure 3
Laminate Cart



Framing

ARRI recommended a number of changes to the framing robot system that would decrease the cycle time. They constructed a prototype of a framing feeder/dispenser system shown in Figure 4. In this system the frame pieces are fed off onto a fixture that pushes them under the butyl dispenser and then hands them off to the robot. This concept is designed to reduce the framing cycle time from 150 seconds to 80 seconds per module.

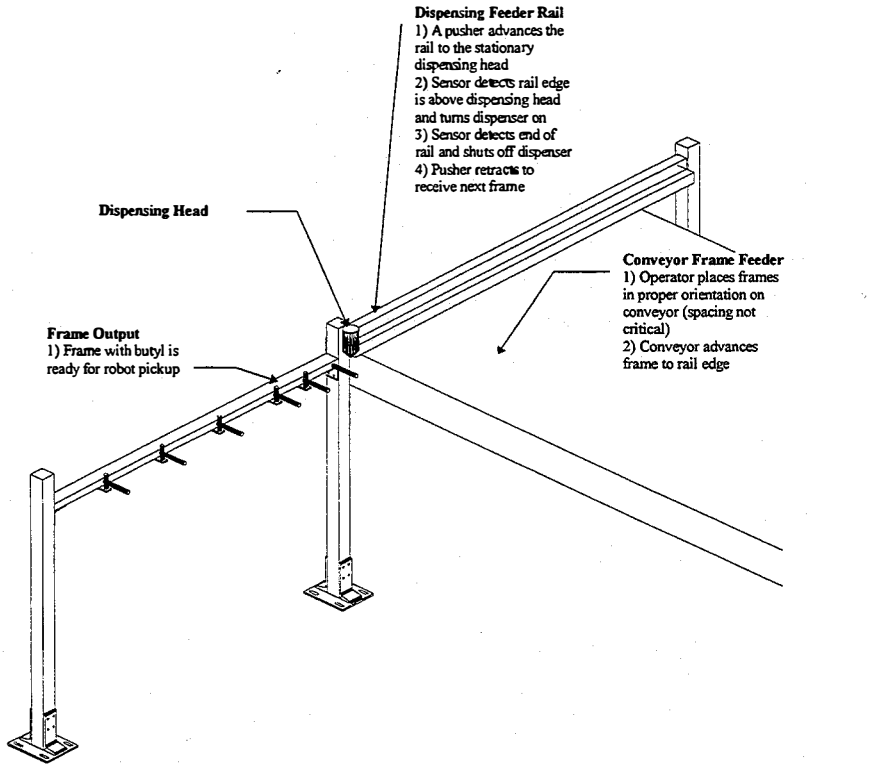
The prototype validated the concept. A production unit is now being designed.

Soldering

One of the key process steps involved in determining module reliability is the process of soldering the interconnect ribbons to the solar cells. The selection of a soldering process is also an important factor in the design of the module assembly system. ARRI performed a detailed literature search to gain a better understanding of soldering techniques. Three main areas of soldering technologies were searched; 1) Hot bar reflow soldering, 2) LASER soldering and 3) Focused Infrared (IR) soldering. It is clear from the information found in this search that the

electronics manufacturing industry is driving the use of the (3) technologies we looked at; LASER Soldering, Focused IR and Hot bar Reflow. These reflow technologies in this industry are characterized as Localized Reflow Applications. While most of the soldering in the electronics manufacturing industry is achieved using mass reflow techniques (IR ovens, wave solder, etc.) there is a real need for soldering localized areas on a printed circuit board (PCB) such as with attaching fine-pitch electronic devices to the PCB. The literature provided information on the (3) reflow technologies as used in the electronics industry to attach fine-pitch surface mount components.

Figure 4
Framing Feeder/Dispenser



Below is a list of the advantages and disadvantages of the Hot Bar Vs LASER and Focused IR reflow processes.

Hot bar Reflow

Advantages

- The hot bar itself is an effective way of compensating for lead coplanarity issues
- Low cost equipment
- Users confidence in ability to control the temperature profile

Disadvantages

- Need for tool changes for different component configurations
- Black carbon build up on bottom surface of blade affecting heat transfer and blade flatness

- Potential lead/pad damage from force of blade on component *
- Lack of temperature uniformity across the hot bar and residual induced stresses

*á On a specific application to attach a surface mount device using a hot bar reflow system a 10° C temperature difference was recorded as a result of changes in the applied force of the heater bar from 4 - 13 lb. This equates to a 1° C change per 0.88 lb. of force. The majority of this temperature change was noted in the 4 - 8 lb. range.

LASER and Focused IR Reflow

Advantages

- Precise control of local heat energy
- Less risk for lead/pad damage or induced stresses from heater bar
- Doesn't require tool changes for different component sizes
- Yields superior solder joints exhibiting less brittleness and greater mechanical integrity **
- Accurate and concentrated focused light beam
- No tool maintenance

**Detailed studies have been done comparing the integrity of solder joints for mass IR reflowed parts and Laser reflow parts using the higher melting alloy (221° C) of Sn-96.5% / Ag-3.5%. The conclusions have been that greater superheating, such as laser versus mass IR, result in greater amounts of dendritic Cu_6Sn_5. Intermetallic in this form contributes to solder hardness (and probably strength) without degrading fatigue performance. Also the finer distributions of Ag_3Sn in the eutectic produced by lower heat input and faster cooling following solidification (such as for laser vs. mass IR reflow) result in higher hardness. Although this comparison is between mass IR and laser reflow there is a correlation between hot bar and laser reflow as to the superheating rate differences of the two processes. The heating rate of the hot bar is much slower than that of the laser which has a heating rate in the range of 0.1 seconds per solder joint.

Disadvantages

- Newer technology
- Equipment costs
- Inability to compensate for lead coplanarity
- Safety aspects in the manufacturing area in regards to the reflected radiation

There are three types of lasers used today; 1) the Nd:YAG which has been the most commercially used for soldering systems, 2) the CO_2 which has been successfully applied to the production of soldered joints and 3) GaA1As laser diodes that were recently developed due to the advancements in semiconductor physics. From the point of view of joint formation the biggest difference between the different types of lasers lies in the wavelength of operation. For the application of reflowing pretinned parts with only flux added, a short wavelength energy device is required. This can be obtained from the Nd:Yag or the laser diode devices, where the shorter wavelength is more strongly absorbed by metal surfaces. The laser diode has one distinct advantage over the Nd:YAG in that it has an extremely high efficiency of around 30% (electrical-to-optical), compared to 1% for the Nd:YAG. In this case, approximately an 85 watt electrical power is necessary to give a laser output of 25 W, whereas the Nd:YAG laser consumes 2500 W for the same output. The lower energy losses of the diode laser means there is no need for an expensive and space consuming cooling system. The compactness of the laser

diode make it readily available for integrating into automatic equipment.

From our literature and vendor search the use of laser diode for the reflow soldering process seems feasible. There is very little interest in the focused IR process which is reflected in the information available from the search. Therefore, we will be studying the performance of the hot bar reflow and laser soldering systems as they are applied to thin polycrystalline silicon solar cells.

3.5 TASK 16 - FRAMELESS MODULE DEVELOPMENT

In this task Solarex will develop and qualify a frameless module design incorporating a lower cost back sheet material (less than $0.05/square foot) and user friendly, low cost electrical termination (less than $1.00/module).

3.5.1 Backsheet

A key component in frameless module design is the backsheet, since the electrical termination and the support system itself must adhere to the backsheet. This offered an additional opportunity to reduce cost from the 3 part backsheet being used at Solarex at the start of this PVMaT Program.

During the first year of the program, three candidate materials were selected for evaluation[6]:

- Pigmented Chlorinated polyethylene (CPE)
- Affinity polyolefin
- Thin Tedlar - polyvinyl fluoride

Each of these materials successfully completed environmental qualification testing to IEC 1215 and IEEE 1262 and successfully passed in-house simulated UL fire tests. Each material was then exposed directly to a equivalent of 2 years UV in Phoenix, AZ. All of the materials except for the CPE shown no degradation after the UV exposure. The CPE samples turned a dark black color with evidence of leaching of green pigment from the samples exposed to UV. Based on these results we have dropped CPE as a candidate back sheet.

Large area samples of white pigmented polyolefin were provided by Richmond Technology. This material was utilized as a backsheet in the standard EVA lamination process. After lamination all of the samples had numerous pin holes through the back sheet. Most of these pin holes occurred directly over solder bonds, although others appeared over back tabs, but not where they were soldered. It appears that the polyolefin gets too soft at the lamination temperature and is easily punctured by any irregularities that occur behind the cells. Unless we can find an inexpensive way to strength the polyolefin, it will not work as our back sheet.

We are now left with only single sheet thin Tedlar as a candidate material. Tedlar does meet all of the technical requirements of a back sheet and Solarex has been using a single layer Tedlar backsheet now for several years. However, Tedlar will not meet the $0.05/square foot cost goal of this PVMaT program. However, it does represents at least a 70% reduction in back sheet cost over the three part material that Solarex was using at the beginning of this PVMaT program.

Both Springborn and Richmond Technologies have provided us with samples of Tedlar/EVA laminate. By obtaining the Tedlar/EVA already bonded together, it reduces handling costs and may allow us to use thinner EVA and thinner Tedlar to further reduce cost. Modules with the Tedlar/EVA laminate have now successfully completed environmental qualification testing to IEC 1215 and IEEE 1262 and are qualified for use at Solarex.

3.5.2 Electrical Termination

In the last Annual Report, we reported on the selection of a butt crimp connector and SPC Technology type PHS black polyolefin shrink tubing for electrical termination of the module[4]. These connectors have successfully passed all of the requirements of IEC 1215 and IEEE 1262. Samples continue to perform well in extended outdoor testing.

3.5.3 Mounting System

During the first year of the program, we selected 3M's Very High Bond (VHB) Tape to attach the back of the module directly to metal cross members[6]. A prototype system was built at the Solarex facility in Frederick, Maryland. Performance of the tape in this system was carefully monitored. The success of this system led Solarex to use this mounting system to build several large PV arrays. However, recently we have experienced significant problems related to the use of the 3M VHB tape.

There appear to be two problems related to the use of this tape adhesive. The first occurs when the tape is not properly applied to the module. The second occurs when the modules are mounted such that there is a constant force tending to twist the modules off of the beams. In both cases, some of the modules have peeled loose from the mounting beams.

We are now switching from the tape to an RTV adhesive. The RTV itself is actually cheaper than the tape. Our original selection of the tape was to speed up installation since the RTV requires curing time before it can be installed. What we have found in the actual installation of systems, is that the modules can be panelized several days before installation so that the panels are ready when the installation crew arrives. This appears to reduce the total time required to install the array.

A test array using RTV has been out as long as the test array with tape and it is doing fine. We have now installed several more test systems at Frederick using the same mounting concept, but with RTV as the adhesive. We are continuing to monitor the performance of these systems.

3.6 TASK 17 - Automated Thin Cell Handling

In this task Solarex will develop automated handling equipment for 200 μm thick 15 cm x 15 cm polycrystalline silicon wafers and cells that has high yield (less than 0.1% breakage per process handling step) and can handle at least 12 cells per minute. ARRI is under subcontract to assist Solarex in the development of handling methods and equipment for large thin wafers and cells.

ARRI undertook a study of commercial and academic information sources related to the handling of silicon wafers. The purpose of this literature search is to gain an understanding of the

wafer handling methods that are commercially available, or documented in the open research literature, in order to assist in an upcoming wafer end-effector design effort for Solarex.

The literature search has been conducted at the following levels:
- Articles from industry periodicals and trade magazines.
- Articles from technical conference proceedings.
- Articles from academic journal publications.
- Literature from manufacturers of wafer handling equipment.

Trade periodicals and conference proceedings found to contain related information are:
- Solid State Technology
- Material Handling Engineering
- Semiconductor International

Academic journals and conference proceedings found to contain related information are:
- Journal of Vacuum Science Technology
- IEEE Control Engineering Series
- IEEE Transactions on Semiconductor Manufacturing
- IEEE Micro
- Microcontamination
- Applied Surface Science
- Vacuum

All searches in wafer handling have appeared exclusively in the context of semiconductor manufacturing. While the PCB/SMT manufacturing industry shares many common aspects with the solar industry in the area in question, there are significant differences as well. Semiconductor wafers have a circular shape, which gives them better cassette-insertion compliance than square-edged wafers used in solar cell processing. The semiconductor industry enjoys strong standardization in the sizes and mechanical interfaces of both wafers and handling equipment such as cassettes, making the handling equipment compatible among manufacturers and still giving rise to competition and improvement in the designs. Typical wafer sizes are 100 mm, 150 mm and 200 mm diameter; a recent push to higher diameters of 300 mm and above is now prompting renewed interest into single-wafer handling processing versus batch processing.

Semiconductor manufacturing is extremely sensitive to contamination (class 1 environment capability is normal), making vacuum grippers a preferred solution over other kinds of holding devices. The gripper jaws are allowed to come in full contact with the "back" face of the wafer, which is simply a featureless substrate. Non-vacuum methods involve arms that "push" the wafers in and out of their slot in the cassette, and are typically used in transfer and inspection operations; such arms come in contact with *both sides* of the wafer in a small ring-shaped section in the periphery of the wafer.

The use of vacuum not only avoids particulate generation due to the lack of mechanical friction, but also actually assists with the evacuation of contaminants. The typical gripper design in semiconductor wafer sorting and transfer machines consists of flat prongs with embedded vacuum ports flush with the surface or slightly below it. This provides a greater surface-to-surface contact between the gripper and the wafer than using vacuum cups alone, which likely helps to restrict movement of the wafer during transport and minimizes breakage due to bending of the wafer. Vacuum sensors are used to detect that the wafer is latched onto the jaws.

No compliance devices (spring-loading) are apparent in the manufacturers' literature, the probable reason being that the physical location of the wafers is well known, and that the wafer can be attracted to the jaw through an air gap. Perhaps from the same rationale, there is no indication of contact or proximity sensors being used to detect the amount of force imparted on the wafer as it is approached by the jaw, though there is mention of force sensing to avoid wafer fracture in the case of jamming during lateral motion. It is noted that the machines examined deal with the placement of wafers in and out of cassettes exclusively, where their location is known and stable. For a case like Solarex's, where automated equipment must pick up wafers from a stack of variable height, a combination of force and proximity sensing in the direction normal to the wafer plane is likely to be of key importance.

An ongoing concern about contamination has prompted research in more sophisticated non-contact transfer methods such as electrostatic chucks and magnetic levitation devices. Much of this research, in fact, applies to mechanical transfer devices in general — where the goal is to eliminate sources of friction and lubrication — rather than to the wafers themselves. Regardless, for the foreseeable future this research seems confined to laboratory prototypes.

4.0 SUMMARY

The Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvement Program has lead to the development of and/or improvements in processes, products and equipment. The following developments from this program have either been implemented or are in the process of being implemented in manufacturing:

- Casting of larger ingots;
- Use of wire saws in operations;
- Addition of a back surface field to the cell line;
- Introduction of a larger cell (11.4 cm by 15.2 cm) into commercial production;
- Doubling of production capacity in the module assembly area;
- Qualification of a lower cost back sheet;
- Qualification of a lower cost electrical termination system; and
- Use of frameless modules in a number of PV systems.

At this time in the program, we believe that all of the objectives of this PVMaT program will be met. Our analysis indicates that through the year 2000, Solarex will save $5.00 for every dollar it invested in PVMaT and our customers will save approximately $7.00 for every dollar that NREL invested in this PVMaT Program.

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PROGRESS IN SOLAREX CRYSTALLINE SILICON PVMaT PROGRAM

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ABSTRACT

The objectives of this NREL sponsored Photovoltaic Manufacturing Technology (PVMaT) Program are to advance Solarex's cast polycrystalline silicon manufacturing technology, reduce module production cost in half, increase module performance and expand Solarex's commercial production capacity by a factor of three. To meet these objectives Solarex has: 1) Modified the casting process and stations to grow larger ingots; 2) Developed wire saws to cut wafers on as little as 400 μm centers; 3) Developed a laboratory process to increase cell efficiencies to 15% using back surface fields, mechanical texturing and gettering; 4) Modified the casting, wires saw and cell processes in order to fabricate larger (15.2 cm by 15.2 cm) wafers and cells; 5) Improved the automated assembly of modules, reducing labor requirements and increasing throughput; 6) Developed a frameless module with a lower cost backsheet and a simple, low cost electrical termination system; and 7) Determined the stress levels leading to wafer breakage and designed equipment for automated handling of thin wafers.

CASTING

The original goal of the casting task was to develop the ability to cast ingots that yield four 15 cm by 15 cm bricks with at least equivalent material quality as was achieved for the standard 11.4 cm by 11.4 cm bricks. This was demonstrated in the laboratory, yielding equivalent quality ingots with a 73% increase in the useable silicon obtained from each casting.

Most of Solarex's products are still based on the 11.4 cm by 11.4 cm solar cell, so a decision was made to develop a casting process for ingots that are large enough to yield nine 11.4 cm by 11.4 cm bricks. This process has now been demonstrated in the laboratory. Production casting stations are now being modified for casting of these larger ingots. Casting capacity will be doubled at a cost of less than 20% of the cost that would be required to add a similar amount of capacity by purchasing new casting stations.

WIRE SAWS

The goal of this task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μm centers at lower cost per cut than achieved today on the ID saws.

Solarex is utilizing an HCT wire saw in this program. The saw has successfully demonstrated the ability to cut a variety of wafer sizes including 11.4 cm by 11.4 cm, 11.4 cm by 15.2 cm and 15.2 cm by 15.2 cm on centers from 500 μm down to 400 μm. The saw has been operated in a semi-production mode, producing as many wafer as 16 ID saws at better yields and lower per wafer cost than the ID saws. This saw has been so successful that Solarex has procured a second HCT wire saw.

After wafers have been cut on the wire saw they must be removed from the hold down plate, placed in cassettes and cleaned. Today, this process is done manually. An automated process is necessary to reduce cost and increase yield especially as the volume of wire saw wafers increases and the thickness of the wafers decreases. As a first step to better understand what is involved in removing wet wafers from a stack, the Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI) performed a series of tests to evaluate the difficulty of separating wafers. [1]

In the first experiment the amount of force necessary to pull wafers apart was measured as a function of how wet the wafers are. The results are shown in Table 1. The more water between the wafers, the harder it is to separate the wafers.

Rather than pull wafers apart, it is possible to slide them apart. The second experiment measured the dynamic sliding friction of wafers as a function of how wet the wafers are. The results are shown in Table 2. For this case the required separation force is greatest for semi-wet wafers. Once the wafers are coated with water they slide relatively easily over each other.

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Table 1: Normal Separation Force

Test #	Dry (grams)	Semi-wet (grams)	Wet (grams)
1	7	2274	>5700
2	3	2018	>5700
3	12	2381	5101
4	16	1907	>5700
5	7	1864	>5700
6	6	1369	5573
Avg.	9	1969	>5700

Table 2: Dynamic Friction Force

Test #	Dry (grams)	Semi-wet (grams)	Wet (grams)
1	111	2149	219
2	104	2053	208
3	102	2041	171
4	118	2589	105
5	114	2257	159
6	126	1976	208
Avg.	112	2178	178

Based on the results of the second experiment, a prototype machine was developed in which a roller pulled the first wafer in a horizontal stack downward through a slot into a cassette. This concept worked very well for both dry and wet wafers. The prototype has operated through thousands of cycles without breaking any wafers and with successful feeding of a single wafer more than 99.95% of the time. A full production machine will be built based on this design.

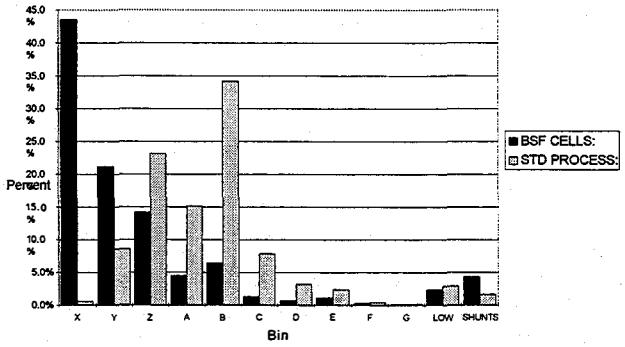
CELL PROCESS

The goal of this task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. Solarex's cell process is based on the use of thick film paste metallization. This is a low cost process. The PVMaT program objective is to determine which modifications or improvements can lead to both higher cell efficiency and lower dollar per watt module manufacturing cost. Several processes have been evaluated separately and then incorporated into an integrated process sequence.

Back Surface Field

Previous laboratory experiments demonstrated that an aluminum paste back surface field (BSF) can increase cell efficiency by approximately 5%. [2] Two BSF manufacturing trials have now been completed, with more than 25,000 BSF cells produced with all processes except BSF performed in production using production processes, equipment and personnel. The average cell efficiency for all of the BSF cells was 5.3% higher than for the non-BSF cells produced during the same time period. Figure 1 shows the bin distribution for both the BSF cells and the standard production cells produced during this time period. The X bin has the highest efficiency with G bin the lowest. Over 40% of the BSF cells were in the highest efficiency bin, compared to less than 1% for the standard process cells.

Figure 1: Distribution Comparison, BSF versus Standard Production



The cells from the BSF manufacturing trials were incorporated into modules using the automated assembly equipment. While some process and equipment parameters had to be modified for the BSF cells, no major problems were encountered. The 5.3% BSF efficiency enhancement translated from cells to modules. Modules made during these trials were subjected to environmental qualification per IEC-1215 (Crystalline Silicon Terrestrial Photovoltaic Modules - Design Qualification and Type Approval) and IEEE-1262 (IEEE Recommended Practice for Qualification of Photovoltaic (PV) Modules). The BSF modules successfully completed the testing with all power losses well below the maximum allowable by IEC-1215 with no measurable differences between the BSF and standard cell modules subjected to qualification at the same time.

Part of the PVMaT plan is to reduce wafer and material cost by using thinner wafers cut on the wire saw. One of the advantages of the BSF process is its ability to increase the efficiency of thinner cells. The 5% efficiency gain observed for BSF cells with today's cell thickness increases to nearly 10% for the thinner cells under development in this program. [3]

Mechanical Texturing

An improved method for evaluating the performance of an optical coupling surface in terms of its performance on solar cells has been developed in this program. [4] The model predicted that chemical and mechanical texturing would increase the short circuit current and maximum power of encapsulated solar cells by approximately 3% over planar cells made on the same material with the same cell process. To verify the model, matched polycrystalline wafers were processed with and without

mechanical texturing. The matched cells were measured, encapsulated and remeasured. The results are given in Table 3. Mechanical texturing resulted in a 3.0% gain in encapsulated cell efficiency, as predicted by the model using reflectance measurements.

Table 3: Mechanical Texturing versus Planar Controls

Cell Structure	Unencapsulated Efficiency (%)	Unencapsulated Jsc (mA/cm^2)	Encapsulated Efficiency (%)	Encapsulated Jsc (mA/cm^2)
Planar	12.75	29.7	12.96	30.3
Mech. Tex.	13.19	30.7	13.35	31.1
Difference	3.4%	3.4%	3.0%	2.6%

Efforts are now underway to develop a tool that can texture a large area wafer in a single or a few passes.

Phosphorous Gettering

We investigated the use of phosphorous gettering in conjunction with the use of a back surface field, as a function of position of the wafers in the ingot and with a variety of surface preparation techniques. [5] For the best set of parameters, phosphorous gettering increased the average short circuit current and efficiency by 2.7% over the non-gettered controls.

Integrated Cell Process Sequence

Back surface fields, mechanical texturing and phosphorous getting increase cell efficiencies. An integrated cell process sequence has been developed to include these efficiency enhancing processes in a cost effective manner. The results for encapsulated single cell packages are shown in Table 4. This group of cells nearly met the program efficiency goal of 15%.

Table 4: Integrated Semicrystalline Cell Process Sequence (Encapsulated Cells)

Sample	Efficiency (%)	Jsc (mA/cm^2)	Voc (mV)	FF (%)
Planar	14.00	32.28	599	72.5
Mech. Tex.	14.56	32.90	597	74.1
Mech. Tex. + Gettered	14.88	33.04	600	75.1

Large Area Cells

A cell size of 15.2 cm by 15.2 cm was selected to have one dimension in common with Solarex's commercial 11.4 cm by 15.2 cm solar cell. Modeling of the larger cell lead to a design that retains two buss bars with six solder joints on the front of each interconnect versus 4 solder joints on the front of each interconnect on the standard 11.4 cm by 11.4 cm cell. Details of the modeling, grid design and expected performance for the 15.2 cm by 15.2 cm cell are presented in Reference [6]. Initial cell efficiencies have exceeded 13%.

MODULE ASSEMBLY

The initial goal of this task was to modify Solarex's module assembly system to increase throughput by 100% and decrease the labor requirement by 50%. The throughput goal has now been modified to increase by 200% to meet Solarex's manufacturing requirements.

Solarex subcontracted to the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington to review and model the automated module assembly system in operation at the beginning of this PVMaT Program and to make recommendations for improving the equipment and/or process flow. The first step in this task was the development of a process flow chart detailing all of the module assembly steps. ARRI used this information to model and analyze the manufacturing process. As a short term goal the changes necessary to increase production capacity by 40% were identified and implemented during the first year of the contract.

The second phase of the program was designed to meet the initial PVMaT contract goal of increasing capacity by a factor of 100% from the original 1993 baseline. Solarex and ARRI developed two Factory of the Future concepts to meet this requirement. AT&T's discrete event simulation package called Witness was used to evaluate each scenario. The Witness software is capable of modeling resource interactions in detail and providing an accurate representation of the factory using statistical analysis. The Witness software provided an analysis of the capacity and resource requirements of the two Factory of the Future concepts.

Witness predicted that each of the two scenarios would increase throughput by more than 100% and would reduce the labor content per module by more than 50%. However, neither concept could meet Solarex's publicly announced polycrystalline expansion program designed to triple capacity by 1999. To meet this expanded capacity requirement, Solarex and ARRI developed a new factory concept that would allow for incremental increases to meet the shorter term capacity requirements and would ultimately result in the required tripling of module assembly capacity. The plan was based on replacing the back solder robots with XY positioners to increase the number of solder bonds made at one time from 2 to 4, thereby increasing the throughput by nearly a factor of two. This modification has now been implemented and the

XY positioners are operating at the throughput level predicted.

The new factory configuration and Solarex's projected module build plan through 1999 were then used as inputs to the Witness program. As the volume of products ramps up, the model predicts when the various pieces of equipment reach maximum capacity. This analysis was utilized to develop a capital investment budget for the crystalline expansion. The implementation of this plan is now underway with capacity double what it was at the beginning of the PVMaT program, with a second doubling scheduled to be completed by 1999.

FRAMELESS MODULE DEVELOPMENT

The goal of this task is to develop and qualify a frameless module design incorporating a lower cost back sheet material (less than $0.05/square foot) and user friendly, low cost electrical termination (less than $1.00/module). Since PVMaT is designed for large systems, the modules were designed to mount directly onto the support structure without integral frames. The first step was the design of a compatible support structure and the identification of 3M Very High Bond Tape for mounting the modules to the structure. This mounting concept has now been successfully used for a number of systems including the 100 kW system at SMUD's Hedges substation.

Backsheet Development

A module backsheet specification was prepared and utilized in discussion with potential vendors. Three experimental back sheet materials pigmented chlorinated polyethylene (CPE), affinity polyolefin and polyvinyl fluoride (Tedlar) were selected for evaluation. Mini-modules of all three materials successfully passed environmental qualification to IEC-1215 and IEEE-1262. All three materials also successfully passed an in-house simulated UL fire test.

Each of the candidate materials was then exposed to concentrated sunlight equivalent to 2 years of exposure in Phoenix, AZ. We estimate that the normal UV exposure of the back sheet is no more than 10% of direct exposure, so this test should represent 20 years of UV on the back of the module. All of the materials except for the CPE exhibited no degradation after the UV exposure. The CPE samples turned color with evidence of leaching of pigment. Based on these results CPE was dropped as a candidate back sheet material.

Large area samples of white pigmented polyolefin were obtained and utilized as backsheets in the standard EVA lamination process. After lamination all of the samples had numerous pin holes through the back sheet. These pin holes occurred directly over back tabs, both at solder joints and in areas with no solder joints. Polyolefin gets too soft at the lamination temperature and is easily punctured by any irregularities that occur behind the cells.

We are now left with only Tedlar as a candidate material. Tedlar does meet all of the technical requirements of a back sheet. Based on the PVMaT results, Solarex switched manufacturing to a single layer Tedlar backsheet. However, Tedlar will not meet the $0.05/square foot cost goal of this PVMaT program, although it does represents at least a significant reduction in back sheet cost over the three part material that was used before the PVMaT program.

Electrical Termination

For electric termination, we need a system that has low material cost, but also does not require appreciable labor for field assembly. Junction boxes and weather tight quick connects, that would meet the environmental requirements, are not available in the price range of interest. We then selected and qualified a system using pig tail wires that are connected via a butt crimp connector and protected with polyolefin shrink tubing. These connectors have successfully passed all of the environmental testing requirements of IEC-1215 and IEEE-1262 without measurable change in internal contact resistance or leakage current during wet hi-pot testing at 2750 volts. This electrical termination system meets the technical requirements and the cost goals of the program.

AUTOMATED CELL HANDLING

The goal of the automated cell handling task is to develop automated handling equipment for 200 μm thick 15 cm by 15 cm polycrystalline silicon wafers and cells with a high yield (less than 0.1% breakage per process handling step) at a throughput rate of at least 12 cells or wafers per minute. ARRI is also supporting Solarex in this task.

Wafer Fracture Testing

ARRI began this effort by studying the strength and fracture behavior of Solarex cast polycrystalline wafers. A four point bend test and a cantilever test were devised and used to measure the mechanical strength of the wafers. The scatter in measured strengths was modeled using Weibull statistics, and a distribution of the probability of failure as a function of strength was determined. The ultimate strength in bending for the polycrystalline wafers was found to be 119.3 MPa. In addition, the Young's modulus was found to be 168.8 GPa and the Weibull modulus was calculated to be 9.56.[7]

Simulation of Wafer Handling

A finite element model was then developed to determine the distribution of stress and deflection in a wafer based on the applied load. This model along with the Weibull modulus can be used to determine the probability of

breakage of the wafer under the specified load. The model was used to simulate a typical wafer handling situation, to estimate the maximum load that can be applied during handling and the corresponding probability of failure.

Handling Equipment

Two different approaches to wafer handling have been evaluated. The first approach slides wafers off a horizontal stack into a cassette. It has been successfully demonstrated for use with both dry and wet wafers and is being implemented in the wire saw process. However, because of the sliding action, this approach will not work with diffused cells.

A second approach uses air pressure to lift wafers off of a stack and load them into a cassette without mechanical contact. A prototype unit was built and tested using cast semicrystalline wafers. While the prototype worked successfully at times, this is a sensitive and hard to control process. Other approaches to handling of thin solar cells are now being investigated.

SUMMARY

The Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvement Program has lead to the development of and/or improvements in processes, products and equipment. The following developments from this program have either been implemented or are in the process of being implemented in manufacturing:

- Casting of larger ingots;
- Use of wire saws in operations, with one on line and a second on order;
- Addition of a back surface field to the cell line;
- Introduction of a larger cell (11.4 cm by 15.2 cm) into commercial production;
- Doubling of production capacity in the module assembly area;
- Qualification of a lower cost back sheet; and
- Qualification of a lower cost electrical termination system.

We expect that more PVMaT development efforts will be transferred to manufacturing before the end of the program.

At this time we believe that all of the objectives of this PVMaT program will be met. Our preliminary analysis indicates that through the year 2000, Solarex will save $5.00 for every dollar it invested in PVMaT and our customers will save approximately $7.00 for every dollar that NREL invested in this PVMaT Program.

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DEPENDENCE OF CELL PERFORMANCE ON WAFER THICKNESS FOR BSF AND NON-BSF CELLS

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ABSTRACT

This paper reports on the results of a set of experiments designed to study the relationship between cell thickness and efficiency for cast polycrystalline silicon solar cells. Cells without back surface field are less efficient as they get thinner. Short circuit current, open circuit voltage and fill factor all decrease as the non-BSF cells get thinner. However, cells made with an aluminum paste back surface field show the opposite relationship; thinner cells are more efficient. This higher efficiency for thinner BSF cells is the result of higher short circuit current and higher fill factor. The physics behind these results are discussed.

INTRODUCTION

Aluminum paste back surface fields (BSF) are often used to increase cell efficiencies. In the NREL sponsored PVMaT program a BSF process has been developed that yields a 5 to 6% increase in efficiency on cast polycrystalline silicon.[1,2] One component of the effort to reduce the cost of PV modules is the use of wire saws to cut thinner wafers for improved silicon utilization. A brick of silicon can produce 50% more wafers if a wire saw is used to cut 200 μm thick wafers, rather than using ID saws to cut standard thickness (275 μm) wafers. In this paper we report on the effect of wafer thickness on cell performance for cells processed with and without Al paste back surface fields.

EXPERIMENTAL PROCEDURE

Polycrystalline silicon wafers were prepared over a thickness range of 200 to 300 μm. They were sorted into two groups. One group was processed through Solarex's production line using the standard process sequence that includes Solarex's patented diffusion process [3], screen printed silver paste front contacts, a TiO_2 anti-reflective coating and Solarex's patented back metallization system [4]. The second group had identical processing except for the addition of an aluminum paste back surface field. Each cell was weighed before the first metallization step to determine its thickness.

EXPERIMENTAL RESULTS

Figure 1 is a plot of efficiency versus thickness for non-BSF cells. Table 1 gives the average values for efficiency, short circuit current, open circuit voltage and fill factor as a function of thickness. As non-BSF cells get thinner they are less efficient. The lower efficiency is driven by lower short circuit current, lower open circuit voltage and slightly lower fill factor.

Figure 1: Efficiency versus Cell Thickness for Non-BSF Cells

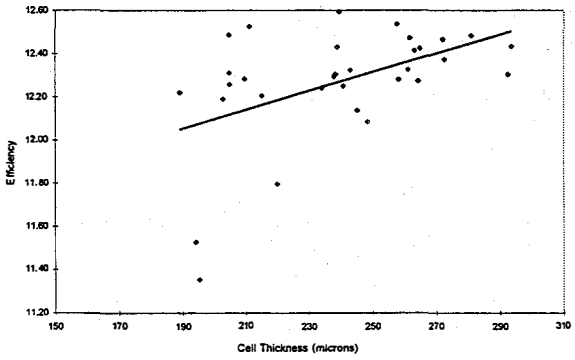

Table 1: Performance versus Thickness for Non-BSF Cells

Thickness μm	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
300	12.53	3.724	585.5	74.7
275	12.42	3.714	584.1	74.5
250	12.31	3.704	582.6	74.2
225	12.20	3.694	581.2	73.9
220	12.10	3.684	579.8	73.6

Figure 2 is a plot of efficiency versus thickness for the BSF cells. Table 2 gives the average values for efficiency, short circuit current, open circuit voltage and fill factor as a function of thickness. As BSF cells get thinner they are more efficient. The higher efficiency is driven by higher short circuit current and higher fill factor.

Figure 2: Efficiency versus Cell Thickness for BSF Cells

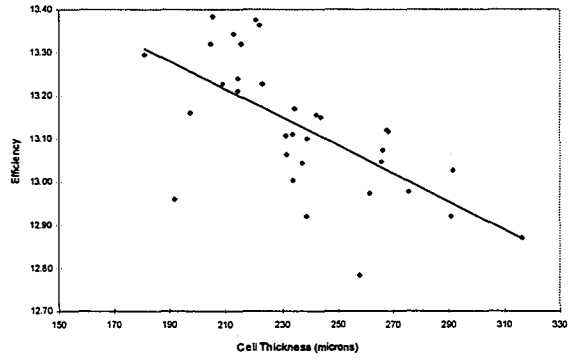

Table 2: Performance versus Thickness for BSF Cells

Thickness μm	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
300	12.91	3.903	589.6	73.2
275	12.99	3.910	589.6	73.5
250	13.08	3.918	589.5	73.8
225	13.16	3.925	589.4	74.1
220	13.24	3.933	589.3	74.4

Table 3 shows the percentage difference in measured parameters between the back surface field cells and the non-BSF cells of the same thickness. While the back surface field process produces an efficiency improvement of approximately 5% for standard thickness cells, the improvement increases to nearly 10% for 200 μm thin cells. The major component of the efficiency improvement is current collection, as thin BSF cells have better short circuit current than thick BSF cells, while thin non-BSF cells have lower short circuit current than thick non-BSF cells. The presence of the BSF clearly improves the voltage. The open circuit voltage of the BSF cells appears to be insensitive to thickness, while the non-BSF cells lose some voltage as they become thinner.

The fill factor follows the same relationship as the efficiency. The non-BSF cells have lower fill factors as they get thinner, while the BSF cells have higher fill factors as they get thinner. However, in this case the best fill factor occurs for the standard thickness non-BSF cells. This is not surprising since the front contact firing process has been optimized to this cell geometry. Thinner standard cells and BSF cells will undergo a different thermal profile than the standard thickness non-BSF cells. The presence of fired Al paste on the BSF cells probably means that thinner BSF cells heat up more like thicker non-BSF cells. Optimization of the firing process to the different cell geometries should improve the fill factors to make them all closer to value obtained for the standard thickness non-BSF cells.

Table 3: Difference in Measured Parameters between BSF and non-BSF Cells as a Function of Thickness

Thickness μm	Efficiency (%)	Isc (%)	Voc (%)	FF (%)
300	3.02	4.80	0.71	-2.11
275	4.59	5.29	0.94	-1.31
250	6.20	5.78	1.18	-0.51
225	7.83	6.26	1.41	0.30
220	9.49	6.76	1.65	1.12

Modeling

The PC-1D computer program [5] has been utilized to model cell performance as a function of thickness. Initially the performance of non-BSF cells was modeled as a function of thickness. Using materials parameters that are consistent with independent measurements, PC-1D was able to accurately model the short circuit current as a function of thickness. Some of the parameters used in the model are given in Table 4. With these parameters PC-1D was able to predict the measured open circuit voltage for thick cells, but it only predicts a 1 mV decrease in open circuit voltage compared to the 5 to 6 mV actually measured during the experiment. The larger difference in open circuit voltage could be process related as we believe the fill factor is.

Table 4: PC-1D Parameters for Fit of Isc to Thickness for Non-BSF Cells

Parameters	Value
Bulk Resistivity	1.0 Ohm-cm
Diffusion Length	135 μm
Front Surface Recombination Velocity	10^4 cm/sec
Back Surface Recombination Velocity	10^7 cm/sec
Back Surface Reflection	20%

Addition of the BSF could improve cell performance via four mechanisms:

1. The Al paste provides a highly reflecting back layer, that enhances the long wavelength response of the cells. Sandia measured an internal back surface reflectance of 58.5% on Solarex BSF cells versus approximately 20% they measured on the sprayed back cells.
2. ^ The BSF process results in a significant reduction in the back surface recombination velocity, also enhancing the long wavelength response of the cells.
3. ^ The heavy p doping at the rear of the cell repels electrons away from the rear surface toward the p-n junction. This is the BSF process that results in

higher open circuit voltages and enhanced long wavelength response of the cells.

4. ^ Improved minority carrier lifetime as a result of Al gettering in the p-type silicon base. [6]

PC-1D was utilized to evaluate the impact of each of these 4 mechanisms.

Enhanced reflection - Increasing the back reflection improves cell short circuit current, contributing approximately 20% of the increase in going from the non-BSF to the BSF process. Enhanced back reflection does not effect the relative relationship between thick and thin cells, so it is not the mechanism that causes BSF cells to be more efficient when thinner. Enhanced back reflection also does not improve cell voltage appreciably.

Back Surface Recombination Velocity - Reducing the back surface recombination velocity from the high value used for modeling the non-BSF cells, leads to improved current and voltage. Without changing any of the other material parameters given in Table 4 that were used to model the non-BSF cells, a reduction in back surface recombination velocity from 10^7 cm/sec down to 10 cm/sec can account for approximately 40% of the current increase and half of the voltage increase actually produced by the BSF process. When the back surface recombination velocity drops below approximately 2,000 cm/sec, thinner cells begin producing more short circuit current than thicker cells.

Back P^+ Junction - PC-1D provides a variety of dopant profiles for use in modeling a back P^+ junction. When optimized, several of these profiles predict the level of current gain observed experimentally from the BSF. However, in all cases when the model predicts the correct current for one particular BSF cell thickness, it over estimates the difference in short circuit current and open circuit voltage between BSF cells of varying thickness. Each P^+ junction profile that correctly models the experimental increase in short circuit current from the BSF process, also predicts that thinner BSF cells would have an open circuit voltage that is 6 to 8 millivolts higher than the thick cells, which is not observed experimentally. Either the particular aluminum alloy process utilized does not produce a P^+ junction that is a major component of the enhanced cell performance or the PC-1D program, as applied, did not correctly model the back P^+ junction.

Improved Bulk Lifetime - Both the BSF induced increase and the thickness dependence of short circuit current for the BSF cells can be accurately modeled by assuming that the BSF process increases the back optical reflection from 20 to 60%, increases the minority carrier diffusion length from 135 μm to 190 μm and decreases the back surface recombination velocity from 10^7 cm/sec to 400 cm/sec. These parameters yield a modeled open circuit voltage that is somewhat higher than actually observed, but a small increase in the shunt diode reduces the BSF cell voltage to the correct level, with little dependence on cell thickness as observed.

SUMMARY

This work has shown that the addition of an Al paste back surface field can increase the efficiency of thin polycrystalline silicon solar cells by nearly 10%. The increased efficiency is due to increased optical reflection from the Al on the rear surface of the cell, reduced back surface recombination velocity and an apparent increase in the minority carrier diffusion length in the base of the cell.

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Process Development Toward a 15% Efficient 230 cm^2 Screen Printed Multicrystalline Silicon Solar Cell

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ABSTRACT

In commercial production, Solarex's baseline multicrystalline solar cells are 130 cm^2 in area with an average efficiency of approximately 13%. One of the goals of Solarex's Photovoltaic Manufacturing Technology (PVMaT) program (sponsored by NREL), is the development of a cost effective cell process to achieve an average cell efficiency of 15% on large area substrates. In this paper the details of the efforts to scale up the area of the cells from 130 cm^2 to 230 cm^2 and the details of the development of an integrated high efficiency cell process sequence are reported.

INTRODUCTION

Solarex has been producing 11.4 cm by 11.4 cm multicrystalline silicon solar cells for nearly ten years. These 130 cm^2 cells are produced in large quantities at an average cell efficiency of approximately 13%. One of the goals of Solarex's NREL sponsored Photovoltaic Manufacturing Technology (PVMaT) program is the development of a cost effective cell process for producing large area cells with an average cell efficiency of 15%. [1, 2,3] In this paper the details of the efforts to scale up the cell area from 130 cm^2 to 230 cm^2 and of the development of an integrated process sequence (IPS) designed to achieve 15% cell efficiencies are reported.

To take into account the increased current collection requirements because of the 75% larger cell area, the front gridline pattern was carefully modeled. The addition of efficiency enhancement techniques (shallow emitter, back surface field and mechanical texturing) results in an increase in the short circuit current density, which was also included in our model .

LARGE AREA CELL DESIGN

Baseline Process

The cell process sequence is based on the use of Thick Film Paste metallization, where a commercially available screen printed silver paste is applied as the current carrying grid on the front of the solar cell. Production cells are 11.4 cm by 11.4 cm in size with two bus bars and 40 top contact fingers. When applied to cast multicrystalline silicon this process sequence produces an average cell efficiency of approximately 13%.

Design Criteria

In the design of the larger cell, several design criteria were utilized. Since no change to the screen printing process was envisioned, the contact finger width was not changed. In order to maintain the performance of the resultant modules, a similar spacing between solder joints on both front and back of the cells was utilized.

Cell Design

The front metal grid designs for the present baseline 11.4 cm by 11.4 cm cell and the larger 15.2 cm by 15.2 cm cell were modeled using PC based software packages developed at Solarex. The designs were optimized for the total power output as a function of the front grid design. The power loss components included shadowing, resistive loss due to the current flow in: 1) the diffused region, 2) the grid lines, and 3) the bus bars and 4) the interconnect tabs. Table 1 shows the optimum designs and performance parameters for 2 and 3 bus bar 230 cm^2 cells. The best performance and a broader high efficiency response surface are predicted from a two (2) bus bar design with wider busses over-tabbed with interconnect ribbon of the same width.

Table 1: Optimum Cell Parameters obtained for 3 bus bar and 2 bus bar designs on 230 cm^2 cells

No. of Bus Bars	3 Bus Bar Design	2 Bus Bar Design
Bus Width	0.18 cm	0.24 cm
No. of fingers	50	53
Coverage	9.2 %	9.2 %
Fill Factor	74.5 %	74.7 %
Efficiency	12.57 %	12.61 %

The optimized cell design parameters and predicted performance for both the 130 cm^2 and 230 cm^2 cells

fabricated using the standard cell process are given in Table 2. The response surface for the 2 bus 15.2 cm by 15.2 cm large area cell is plotted in Figure 1.

Table 2: Optimized Cell Design for 130 cm^2 and 230 ^ cm^2 area cells ^
Cell Design optimized for Jsc=31.5 mA/cm^2, ^ Voc=0.590 V and n-factor = 1.2

	130 cm^2	230 cm^2
No. of Bus Bars	2	2
Bus Width	0.18 cm	0.24 cm
No. of Fingers	40	53
Finger Width	0.01778 cm	0.01778 cm
Active Area Coverage	9.2%	9.2%
No. of Solder joints per bus	4	6
Predicted Fill Factor	76.0%	74.7%
Predicted Efficiency	12.83%	12.61%

HIGH EFFICIENCY CELL DESIGN

Introduction of a shallow emitter, a back surface field, mechanical texturing and emitter surface passivation to the cell process sequence results in an increase of at least 10% in the short circuit current of a cast multicrystalline cell. The grids for these higher efficiency cells must be reoptimized to take into account the higher current density and to compensate for the increased path length due to mechanical texturing. Figure 2 illustrates the predicted variation in efficiency as a function of the number of fingers for 130 cm^2 and 230 cm^2 high efficiency cells. Because of the higher current density, longer path length and higher emitter sheet resistance, the high efficiency cells require more grid lines.

Figure 1: Predicted Efficiency for 15.2 by 15.2 Cell as a Function of Grid Design (2 Buss Bar Design)

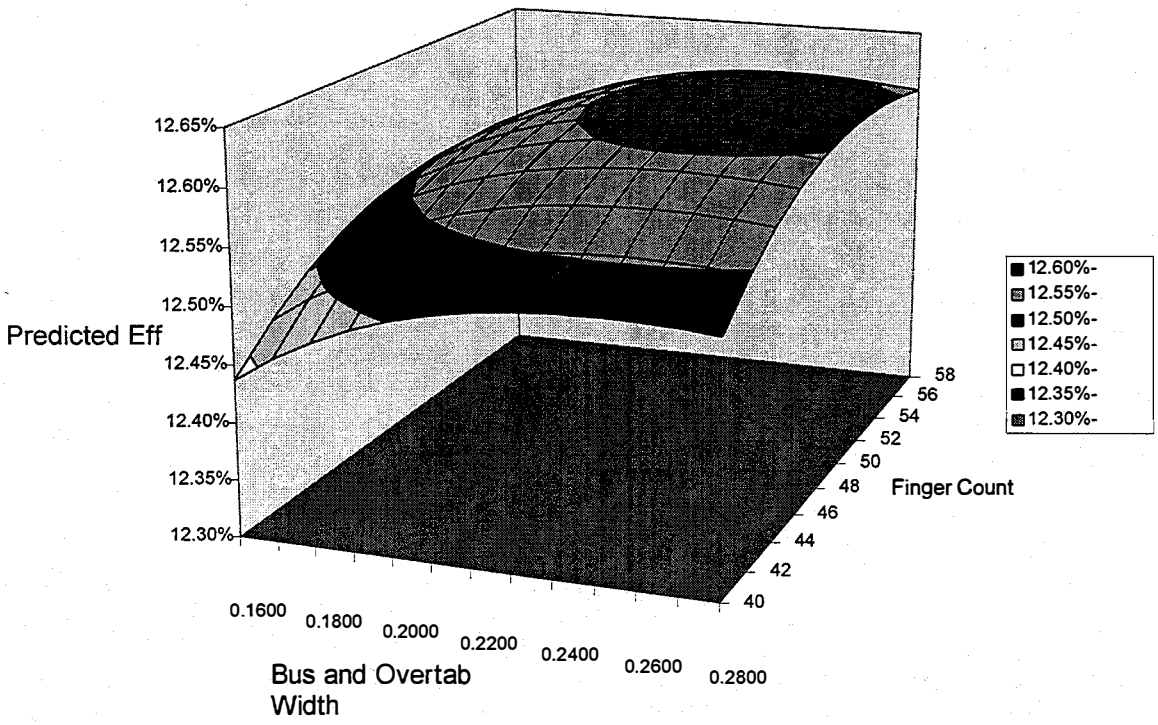
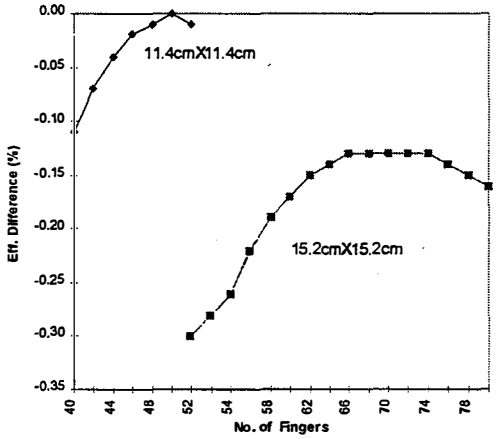


Figure 3 Cell Performance as a function of Number of Fingers for the Integrated Process Sequence



CELL AND MODULE FABRICATION

Baseline Large Area Cells

Cells were fabricated on 230 cm^2 substrates and encapsulated with a low iron glass superstrate and an Ethylene Vinyl Acetate (EVA) encapsulant per Solarex's standard process. The first 36 cell module had a maximum power under standard test conditions (1000 W/m^2, AM1.5, 25° C) of 108 watts with a cell efficiency of 13%. In Table 3 the parameters of this module are compared to that of a typical production module made using 11.4 cm by 11.4 cm solar cells. The efficiency of the module with 15.2 cm by 15.2 cm cells is virtually identical to a typical production module made with 11.4 cm by 11.4 cm solar cells, although the fill factor is slightly lower as predicted by the model.

Table 3: Comparison of Module Performance

	Module with 130 cm^2 cells	Module with 230 cm^2 cells
No: of cells	36	36
Aperture Area (cm^2)	4680	8280
Voc (V)	21.3	21.0
Jsc (mA/cm^2)	30.8	31.0
Eff (%)	13.0	13.0
FF (%)	73.0	72.0

Integrated Cell Process Sequence Development

A high efficiency integrated cell process sequence that includes mechanical texturing, surface passivation, phosphorus gettering and back surface field formation has been developed. Cells were fabricated on 130 cm^2 multicrystalline silicon wafers and then encapsulated with EVA and low iron glass using Solarex's baseline encapsulation process. Solar cells with an encapsulated cell efficiency of 15% were obtained. Encapsulated cell results are presented in Table 4.

Table 4: Performance of Encapsulated 11.4 cm by 11.4 cm multicrystalline solar cells

	Planar Controls	Mech. Texture	Integrated Process
Eff. (%)	14.46	14.73	15.06
Isc (A)	4.24	4.33	4.35
Voc (mV)	599	597	600
FF (%)	72.4	74.1	75.1

A preliminary group of 15.2 cm by 15.2 cm cells were processed using back surface field, mechanical texturing and oxide passivation, but not phosphorus gettering or the grid pattern optimized for the integrated process sequence. These cells were then laminated into one cell mini-modules. One of these mini-modules was measured at Sandia to have an STC efficiency of 13%, with a current density of 32.11 mA/cm^2 , an open circuit voltage of 585 mV and a fill factor of 69.2%. The fill factor is lower than normal, because this cell had a grid pattern designed for a planar cell rather than one optimized for the higher current and longer path length of a mechanically textured cell.

SUMMARY

It has been demonstrated that by using an optimized front contact pattern, the efficiency of the cells should decrease by no more than 0.2% when the cell area increases by 75%. Cell efficiencies up to 15% have been achieved on 130 cm^2 cells using an integrated high efficiency process sequence. The mechanical texturing, back surface field and oxide passivation steps have been transferred to and successfully demonstrated on the larger 230 cm^2 cells. With an optimized front contact design, efficiencies in excess of 14% are expected on the larger cell.

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13. ABSTRACT *(Maximum 200 words)*

Two specific objectives of Solarex's program are to reduce the manufacturing cost for polycrystalline silicon photovoltaic modules to less than $1.20/watt and to increase the manufacturing capacity by a factor of three. This report highlights accomplishments during the period of January 1 through June 30, 1996. Accomplishments include: began the conversion of production casting stations to increase ingot size; operated the wire saw in a production mode with higher yields and lower costs than achieved on the ID saws; developed and qualified a new wire guide coating material that doubles the wire guide lifetime and produces significantly less scatter in wafer thickness; completed a third pilot run of the cost-effective Al paste back-surface-field (BSF) process, verifying a 5% increase in cell efficiency and demonstrating the ability to process and handle the BSF paste cells; completed environmental qualification of modules using cells produced by an all-print metallization process; optimized the design of the 15.2-cm by 15.2-cm polycrystalline silicon solar cells; demonstrated the application of a high-efficiency process in making 15.2-cm by 15.2-cm solar cells; demonstrated that cell efficiency increases with decreasing wafer thickness for the Al paste BSF cells; qualified a vendor-supplied Tedlar/ethylene vinyl acetate (EVA) laminate to replace the combination of separate sheets of EVA and Tedlar backsheet; demonstrated the operation of a prototype unit to trim/lead attach/test modules; and demonstrated the operation of a wafer pull-down system for cassetting wet wafers.

14. SUBJECT TERMS	15. NUMBER OF PAGES
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