NREL/SR-520-22535 • UC Category: 1280 • DE97000209

Large-Area Silicon-Film™ Panels and Solar Cells

Phase I Annual Technical Report July 1995 - December 1995

J.A. Rand, A.M. Barnett, J.C. Checchi,
J.S. Culik, S.R. Collins, D.H. Ford,
R.B. Hall, E.L. Jackson, C.L. Kendall,
and A.M. Trabant
AstroPower, Inc.
Newark, Delaware

NREL technical monitor: R. Mitchell

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of
the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC36-83CH10093

Prepared under Subcontract No. ZAF-5-14271-3

January 1997

NOTICE

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (423) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 487-4650

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

Table of Contents

List of Figures

Introduction

AstroPower is establishing a low cost manufacturing process for Silicon-Film™ solar cells and panels by taking advantage of the continuous nature of the Silicon-Film™ technology. Under this effort, each step used in Silicon-Film™ panel fabrication is being developed into a continuous/in-line manufacturing process. The following benefits are expected: an accelerated reduction of PV manufacturing cost for installed systems; a foundation for significantly increased production capacity; and a reduction in handling and waste streams. The process development will be based on a new 31-cm wide continuous Silicon-Film™ sheet. Long-term goals include the development of a 24W, 30 cm x 60 cm Silicon-Film™ solar cell and a manufacturing capability for a 384W, 4' x 8' Silicon-Film™ panel for deployment in utility-scale applications.

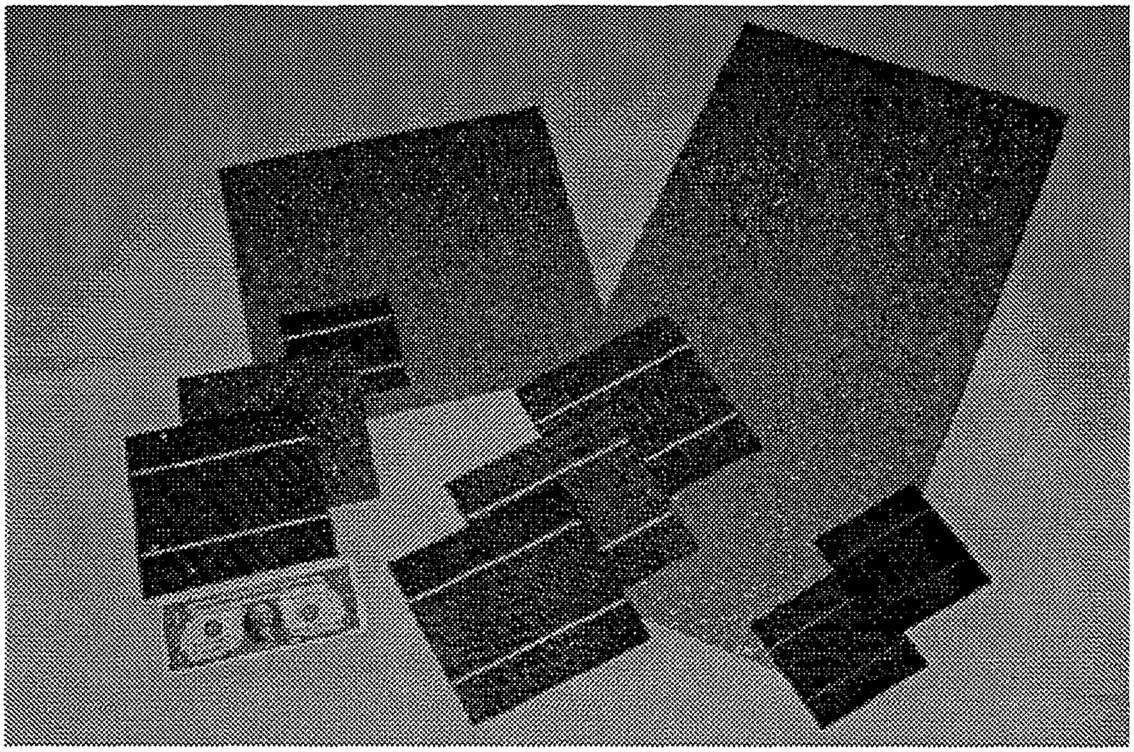


Figure 1. Photograph demonstrating the different sizes of Silicon-Film™ sheets and solar cells. Included are 100 cm^2 and 240 cm^2 solar cells, and sheets 30 cm x 30 cm and 30 cm x 60 cm.

Continuous Processing

One objective of this program is to propagate the continuous sheet fabrication process down through the process stream. Figure 2 illustrates a continuous process that generates solar cells that are nominally 30 cm x 60 cm in size. It is envisioned that at some future point all solar cell processes could be carried out while the silicon substrate is in sheet form. The solar cell can then be sized at the last step, just before incorporation into a large panel or smaller module. The achievement of continuous processing will lead to lower cost per watt by reducing labor, as well as improving control, quality, and yield.

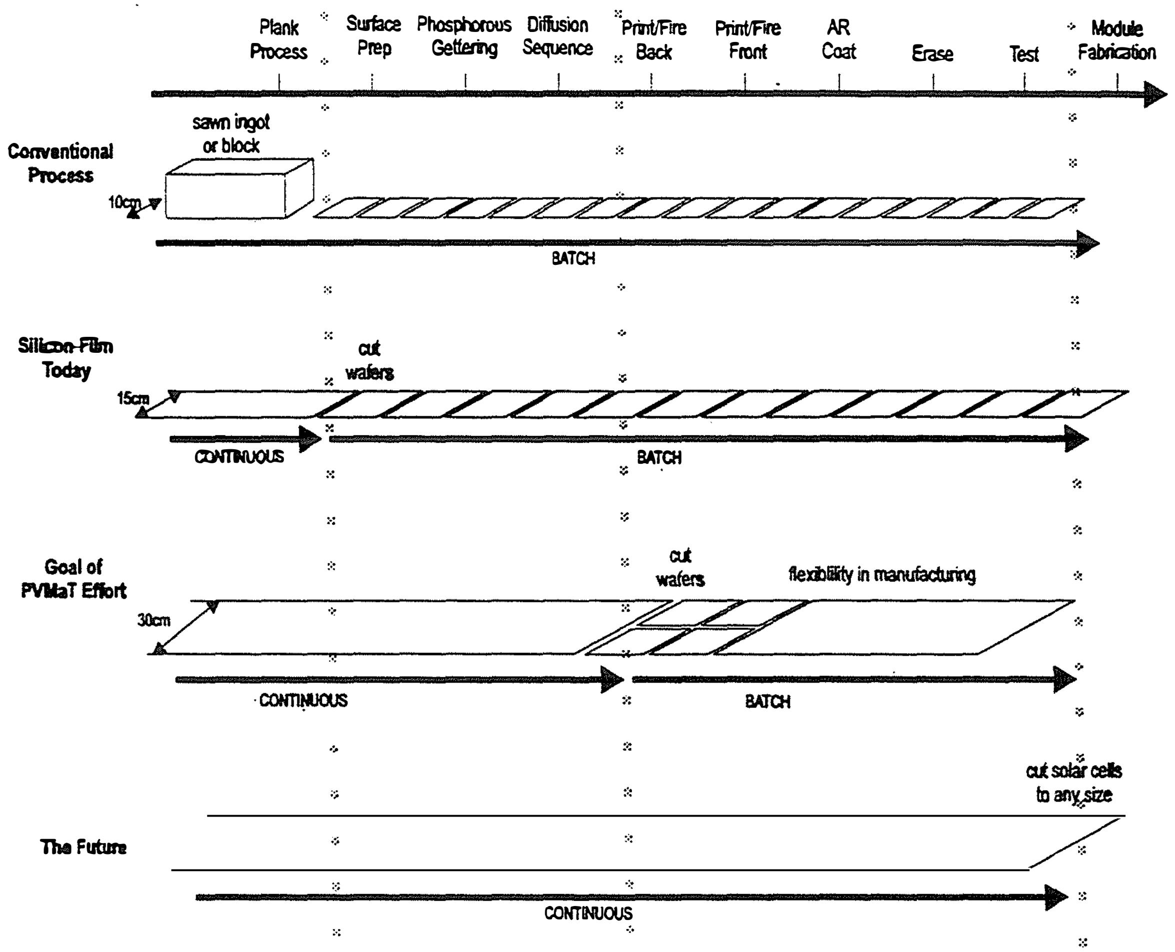


Figure 2. The history and future for in-line, continuous manufacturing technologies at AstroPower.

The issue of optimal solar cell size will be addressed during the proposed project. The final selection of a solar cell size will be determined by the economics of the manufacturing process. The point at which a sheet is sized to a discrete solar cell will be analyzed from an economic perspective as well.

There are many steps required to fabricate a solar cell from the bare silicon/substrate sheet, each requiring process development and engineering. Under this program the first three process steps will be made continuous. These processes are the preparation of the silicon substrate sheet surface, gettering, and diffusion of the emitter layer. These steps will be developed in a modular fashion so that they can be joined together when completed.

The development of a continuous diffusion process will include a number of advanced features. Design rules require developing coating and dopant drive-in processes compatible with both discrete wafer and continuous sheet processing. Under this effort, AstroPower is investigating phosphorous dopant sources with key advantages in reducing processing costs and minimizing environmental impact. Like all Silicon-Film™ manufacturing efforts, the diffusion process and associated equipment are being engineered using advanced design and development systems (e.g. response surface methodologies and computer aided design) to allow immediate adaptability to large-scale production settings. Careful attention is being paid to blue response and the ability to make ohmic ohmic contact with screen printed contacts.

Large Area Solar Cell

The flexibility of the fully developed Silicon-Film™ solar cell product is illustrated in Figure 3. The solar cell process will operate continuously and fabricate processed material that will result in solar cell sizes up to 30 cm x 60 cm. The actual size of the solar cells and panels will depend on the specific customer applications. As indicated, the market segments addressed include a 384 watt utility-scale panel, a 100 watt commodity power module, and a broad range of specialty modules.

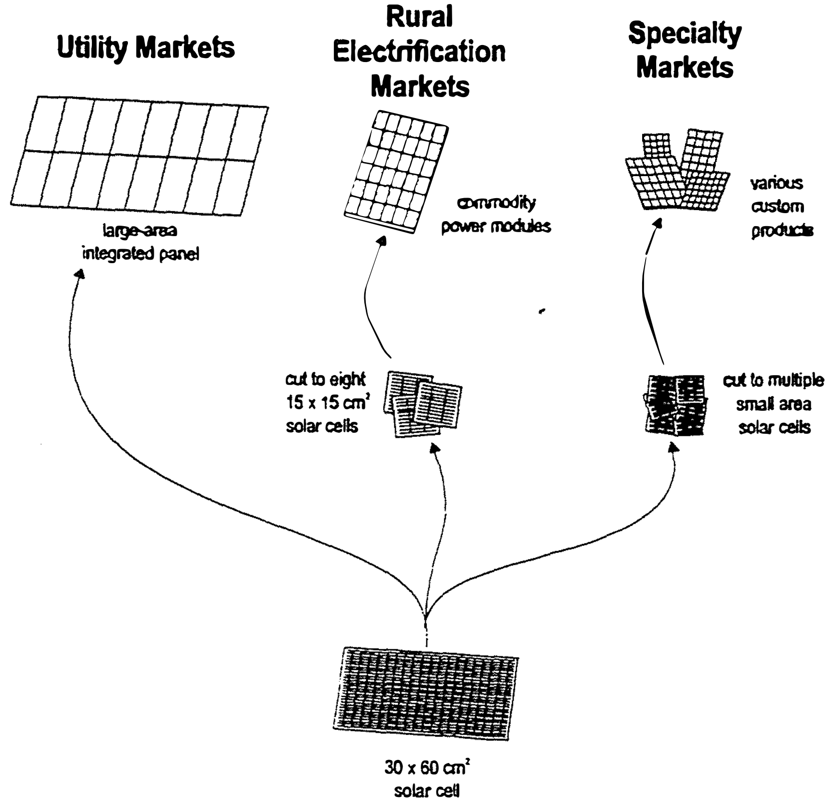


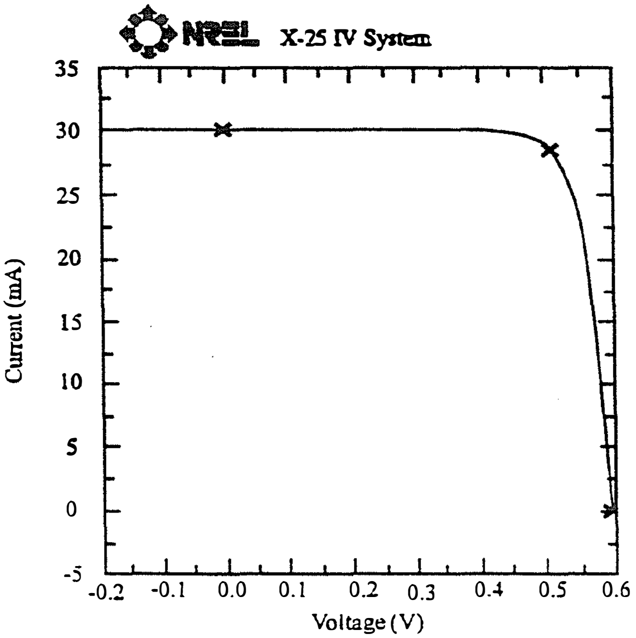
Figure 3. Flexibility of a 30 cm x 60 cm solar cell in meeting several different PV markets.

In preparation for these large solar cells, novel processing techniques are being investigated. A sheet diffusion process, as mentioned earlier, and new metallization techniques are being investigated that will lend themselves to a large area solar cell fabrication process. Very large prototype solar cells (1800 cm^2) are expected in late 1996.

Solar Cell Performance

The quality of Silicon-Film^{TM} material, and the maturity of the solar cell processing have continued to progress and is reflected in increased solar cell efficiencies. Under the present effort, our work is organized to 1) evaluate advanced processing techniques such as bulk gettering and surface passivation in laboratory-sized solar cells (1.0 cm^2), then 2) transfer those results to production-sized solar cells. A laboratory optimization effort has recently been completed and an efficiency of 14.6% was verified at NREL on a 1.0 cm^2 solar cell (see Figure 4). That solar cell was fabricated with an experimental post growth treatment that removed impurities from the grown material.

Performance on production-sized solar cells (240 cm^2) has reached a verified efficiency of 12.2% [1]. An effort is now underway to evaluate transferring technology learned on the laboratory-sized solar cells to increase performance on the larger wafers.



V_{oc} = 0.5966 V

I_{sc} = 30.14 mA

J_{sc} = 30.14 mA/cm^2

Fill Factor = 81.00%

V_{max} = 0.5086 V

I_{max} = 28.63 mA

P_{max} = 14.56 mW

Efficiency = 14.6%

Figure 4. I-V curve for a laboratory-sized 1.0 cm^2 solar cell fabricated with Silicon-Film^{TM} material fabricated with an advanced process sequence.

New Panel Products

AstroPower has completed the design and testing of a new 320W photovoltaic panel. The panel utilizes Silicon-Film™ solar cells in large-area frameless laminates. The laminates are directly attached to a structural steel member. A schematic of the panel is shown in Figure 5. Structural issues for the new 320W panel were investigated in detail. Work involved: analyzing the design (with the assistance of a Professional Engineer), fabricating prototypes, environmental exposure, and performing mechanical loading tests. A summary of the work is presented below. A complete drawing package for the panel was generated and sent to Niagara Mohawk in planning for a 120kW array to be installed in 1996. Niagara Mohawk also cost shared the panel development effort.

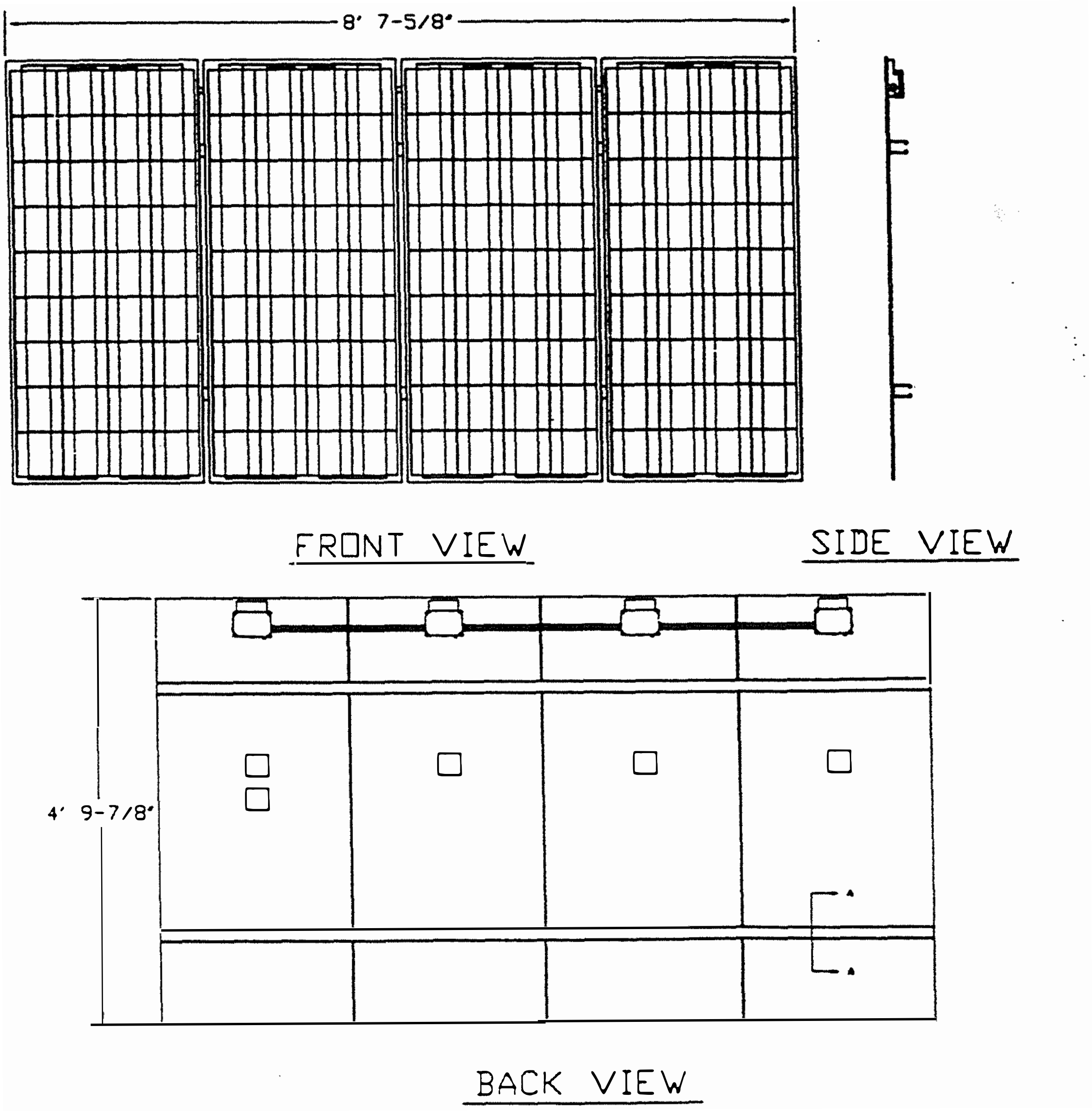


Figure 5. Schematic of a panel.

Design

The panel design was developed with assistance of Jefferson Shingleton, P.E. Mr. Shingleton has experience in the mechanical design and fabrication of a number of other photovoltaic installations. The design involved a Product Preliminary Analysis of a photovoltaic panel. A loading analysis was performed to identify candidate product structural design loading conditions. Final product design was based on the following codes and standards:

NiMo Design Standards
New York State Building Code
ASCE 7-93 Minimum Design Loads for Buildings and Other Structures
JPL Block V
UL 1703
PVUSA Interim Qualification Criteria
UPVG Outline Specifications

Preliminary linear structural analyses was performed to estimate the panel rail and module glass stresses developed within the module. The estimated steel and glass stresses were compared to the allowable glass stresses as described by the ASCE and the glass manufacturer.

Environmental Exposure and Mechanical Loading Test

Test structures were fabricated for environmental exposure testing. The structures utilized a laminate and structural support members as described in the drawing package. Only one laminate at a time was tested due to size constraints in our environmental chamber.

A number of testing sequences have been performed. Different attachment methods between the galvanized steel support rails and the tedlar back sheet of the laminate were used. Attachment methods used either double coated acrylic foam tape, or a silicone adhesive, or both.

The test structure was subjected to 20 cycles of: 10 hours at 85°C (85% relative humidity) and 20 minutes at -40°C. The test structure was then subjected to the Mechanical-Loading Test. Early testing resulted in failure at the foam/adhesive interface within the tape, and failure at the adhesive/steel interface for the silicone. After some experimentation, a combination of specialized tape and silicone products were found to survive the humidity/freeze cycling.

Utilizing the revised adhesive, the test structure successfully completed the mechanical loading test. That test involves subjecting the panel to a static load of 30 pounds per square foot for a period of 30 minutes. The test structure was 10 square feet, requiring 300 pounds.

Prototype Panel Fabrication

Based on the testing reviewed, changes were made to the procedures used in panel fabrication. Prototypes that follow the details in the drawing package were fabricated. A photograph of the completed panel is shown in Figure 6. Prototypes were supplied to Niagara Mohawk in late 1995 and plans are in place to ship a panel to NREL in January 1996.

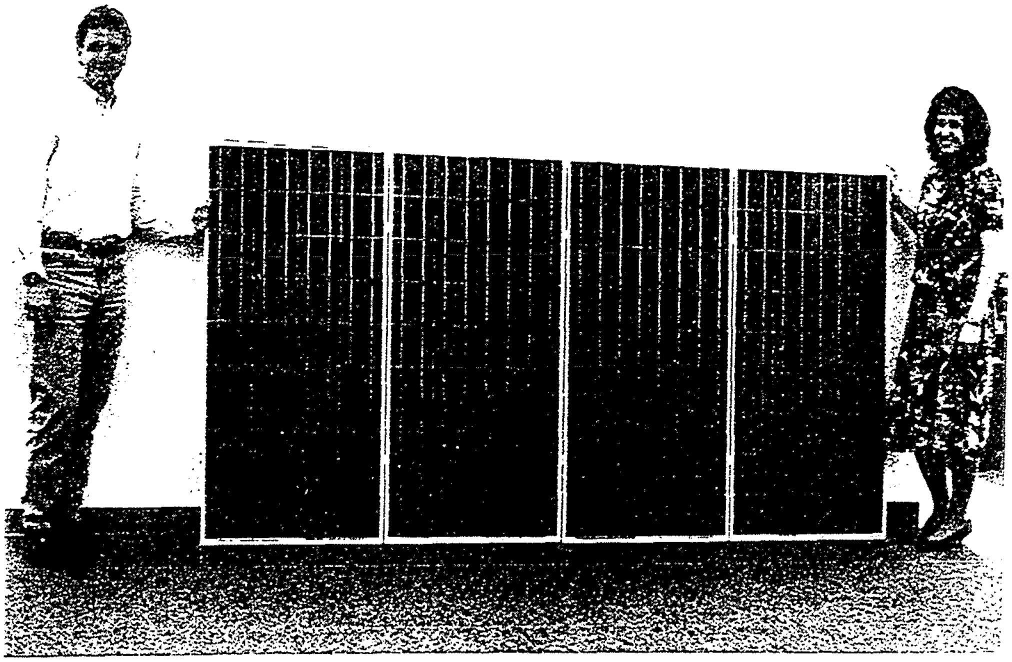


Figure 6. Photograph of a prototype Silicon-Film 320W panel.

Solar Cell Performance

Process Description

To establish a benchmark for Silicon-Film™ material quality, "high performance" solar cells are routinely fabricated. The process is exercised on 1.0 cm^2 and 240 cm^2 devices. Although advanced processing, such as passivation and evaporated contacts are used, the sheet material is fabricated in the production equipment. This exercise is designed to provide direction to our production processing development, especially in the area of diffusion and gettering. The process for high performance solar cells is as follows;

1. Chemical Polish Etch
2. RCA Clean
3. Deposit 4 microns of Al by E-beam
4. Diffusion/Getter Heat Treatment
5. Aluminum Etch
6. Chemical Polish Etch (remove gettered impurities)
7. RCA Clean
8. Diffusion
9. Passivation Oxide
10. Evaporated Contacts (Ti/Pd/Ag)
11. Double Layer ARC.

Early processing utilized a "deep" emitter diffusion sequence, with junction depths approximately 0.6 microns. The "deep" diffusion was followed by a RF plasma hydrogenation step to increase bulk lifetime. The plasma introduced surface damage that was removed in a controlled emitter etch back process. The emitter etch back was also used to optimize the emitter sheet resistance. Although somewhat successful, this sequence did not eliminate the emitter damage, and blue response was lower than could be achieved without the hydrogentation step.

The most recent 1.0 cm^2 deliverables were fabricated with an optimized diffusion/passivation sequence that eliminated the hydrogenation. A combination of increased material quality (increased bulk minority carrier diffusion length) and effective gettering have minimized the gain from hydrogenation.

This process is better suited to large area cells and production processing. Plans are in place now to transfer this technology to the AP225 solar cells.

Increasing Blue Response

Previous work on establishing high performance Silicon-Film™ devices established the need to improve spectral response in the blue end of the spectrum. The existing high performance device process utilized an etched emitter diffusion (to control surface concentration of phosphorus) and a PECVD SiO_2 passivating layer. Surface recombination at the silicon surface was suspected as driving the poor blue response.

A thermal SiO_2 passivating process was developed to investigate this phenomena. The results of that investigation are shown in Figure 7. Experimental sequences were carried out at 800 and 850°C. The data for 850°C indicates that surface recombination is no longer limiting blue response. This process has been incorporated into our existing high performance process and has significantly increased device current.

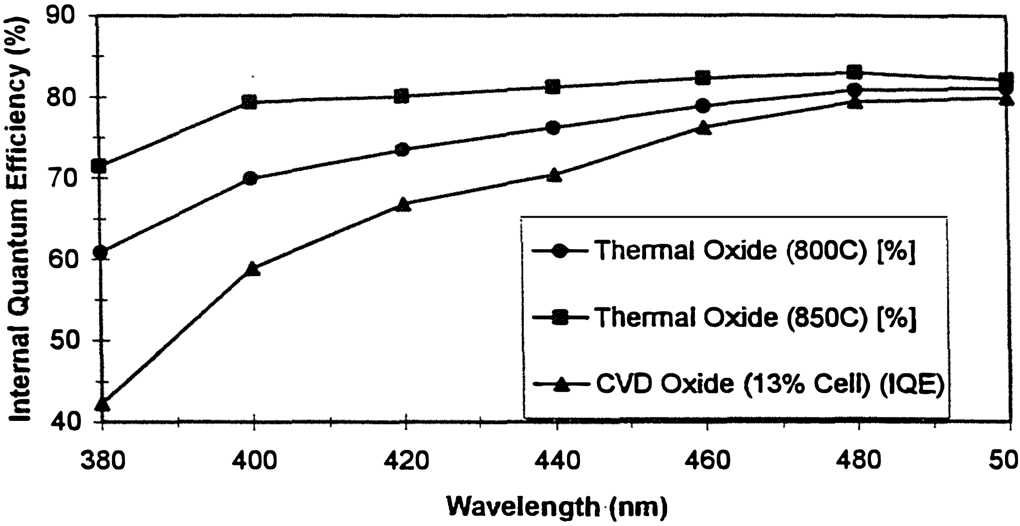


Figure 7. Internal quantum efficiency of Silicon-Film™ materials subjected to a number of different surface passivation schemes.

Solar Cell Process Development

Surface Preparation

Production-scale surface preparation before diffusion of AP-225s includes dry abrasive blasting followed by a series of wet chemical etches, cleaning solutions, and rinses. The etching and cleaning solutions include baths of sodium hydroxide, hydrochloric acid, and hydrofluoric acid with extended de-ionized cascading rinses in between. The process is batch mode with 50 wafers in upright cassettes in each batch.

Problems with the current method include:

i. deep surface damage caused by dry abrasive,
ii. high material costs per wafer,
iii. low throughput, and
iv. manual operation.

The secondary problems associated with manual operation include the potential hazard of operator exposure to chemicals, high labor costs, and inherently inconsistent solar cell performance. Our approach was to address each of the above four identified problems individually. The results are summarized in the following sections.

Dry Abrasive Blasting Alternatives

Our first area for improvement was identified as dry-blasting. The present dry-blast technique removes the top four micrometers of the as-grown sheet. However, the resulting damage to the underlying silicon is substantial requiring chemical removal of the damaged silicon. Our approach was to investigate several abrasive surface treatments with the goal of removing thin layers of silicon while minimizing damage to underlying silicon. The following abrasive surface treatments were investigated:

I. angle of impact, velocity of particle in dry-blasting,
II. abrasive filament brushing,
III. high pressure water jetting,
IV. planar abrading with abrasive coated open weave fabric,

These alternatives are being compared to our present dry-blasting technique for pre-wet chemistry surface preparation. This method which provides the most uniform removal while imposing less damage will be utilized.

Lower Material Costs

Sodium hydroxide is the main component in AstroPower's wet-chemical surface preparation processing line. It acts both as a degreaser and as a silicon etch to remove surface damage. Due to the purity requirements, consumption rates, and waste disposal costs, sodium hydroxide has historically dominated the material costs of the wet-chemical process. Consequently, we have investigated reducing sodium hydroxide costs through reducing purity requirements and the quantities required. These investigations are described below.

Over the past several months, we have converted to several lower purity chemicals for silicon wafer etching/cleaning and associated waste disposal. Lower purity items include sodium hydroxide and various acids and bases used for neutralization. No relationship between sodium hydroxide purity and resulting solar cell performance has been detected. It is assumed that the additional impurities in the lower purity sodium hydroxide are flushed away by the chemical baths subsequent to sodium hydroxide. In addition, the lower purity neutralizing agents were not found to affect the efficiency of the neutralizing process. The lower purity chemicals have affected a 67% reduction in material costs per wafer in surface preparation.

Shorter etch times and lower concentrations of sodium hydroxide were also investigated, however, resulting wafer surface texture was not acceptable. Therefore, no changes in sodium hydroxide etch parameters were realized. Note that the alternative to dry-blasting, abrasives in a liquid/gas stream, described above offers the potential for shorter etch times due to reductions in surface damage. Hence, we will continue our investigation of shorter etch times in conjunction with the new abrasive surface treatment in the near future.

Wet-Etch Process and Equipment

Considerable effort has been made to specify an optimized wet-etch process and associated equipment to achieve high throughput (1000 wafers per hour), improved process control, and improved operator safety. We have investigated three different options: (i) *automation of our present conventional batch process* where cassettes of wafers are brought in and out of open tanks of solutions, (ii) *enclosed batch units* where cassettes of wafers are loaded into a single unit that performs all the cycles of the etching/cleaning process, and (iii) *continuous wet-etching* where wafers are loaded onto a continuous belt and are immersed or sprayed with the appropriate solution or rinse.

In specifying such equipment, it became obvious that we needed to optimize other areas of the solar cell process that dictate etching parameters and equipment specs. For example:

- the abrasive surface removal method and the gettering process determine how much of the silicon surface to remove via etching,
- as more silicon is removed using sodium hydroxide, the silicon becomes more textured which affects the definition of a screen-printed line.

This continues to be an active area of development at AstroPower with equipment purchases planned for 1996.

Continuous In-Line Diffusion

Work during this period resulted in a phosphorus-based liquid dopant source that is low cost, non-toxic, and stable. We have developed a high-throughput technique to uniformly apply this material to AP225 wafers; this process will handle the largest solar cell area anticipated, with dimensions of 30 cm x 60 cm. We have also begun work to specify a companion system that will be capable of diffusing this dopant source across large-area wafers. Process efforts during this period have generated response surfaces of sheet resistance as a function of time, temperature, and furnace atmosphere. The system has the capability to operate in a continuous fashion, in-line with a gettering step, or other downstream steps.

Overview of Previous Diffusion Process

Prior to this work, the Silicon-Film™ wafer diffusion process was performed as a batch-type process using an 8-inch diameter diffusion tube furnace; 200 wafers are processed per batch. The diffusion sequence takes about 2 hours per batch and consumes over 20 kW-hr of electrical power and 1700 liters of gas, primarily nitrogen. The dopant source is semiconductor-grade liquid $POCl_3$ (99.999%). In the present tube furnace diffusion process sequence, much of the time at temperature is used to ensure that dopant phosglass is uniformly deposited across the wafers and throughout the length of the diffusion boat.

Problems with the tube diffusion method for AP225 wafers include low throughput, high material cost per wafer processed, and non-uniformity across the wafer. In addition, the uniformity of the process will degrade as the area of the Silicon-Film wafer increases. Secondary problems associated with the present process include the potential hazard of operator exposure to corrosive materials, high labor costs, high energy costs, and inherently inconsistent throughput and yield.

Process Options

To replace the batch-type diffusion processing, we are interested only in continuous processes capable of throughput rates in excess of 24 m^2 of sheet area per hour. Processes must economically use material, and should not introduce any additional hazards. In addition, the process and equipment must be "scalable", that is, it must be capable of diffusing the larger-area wafers (30 cm x 60 cm) as well as AP225 wafers. The new diffusion process should utilize low-cost, widely-available, non-hazardous materials.

Typically, diffused layers are formed in a two-step process. In the first step, impurities are introduced into the semiconductor surface and minimal diffusion into the semiconductor occurs. This process is called the *predeposition step*. The dopant impurities are then diffused deeper to provide a suitable concentration. This second step is called the *drive-in diffusion* step [2].

Pre-deposition Process Development

The goal of the "pre-dep" procedure is to deposit P_2O_5 onto the silicon surface, preferably only the front, in a continuous process. Although gaseous sources, such as phosphine and $POCl_3$, are technologically mature, the material hazards (phosphine is highly toxic, and $POCl_3$ decomposes to produce corrosive and noxious hydrochloric acid gas) and costs associated with these sources make them unsuitable for our needs. Also, gaseous sources in tube furnaces are fundamentally limited as the area of the wafers increases. Solid sources and liquid ("spin-on") diffusion sources are inherently safe, since they produce P_2O_5 only at diffusion temperatures, and they are capable of producing uniform diffusions across large areas. Both solid and spin-on liquid sources can be utilized to diffuse only one side of a wafer. However, a big problem with solid sources is that they require proximate contact and virtually static conditions to uniformly transfer dopant to a wafer surface. Although it should be possible to procure solid source wafers that will diffuse large areas, the cost is prohibitive.

"Spin-on" liquid sources would appear to be the only viable option for obtaining uniform large area diffusions. However, liquid dopant sources presently available are expensive and are prone to rapid decomposition. As a result, we have chosen to develop a new diffusion source with the following properties: liquid; low cost; non-hazardous; and stable. Deposition of dopant from a liquid source is almost instantaneous. To meet the throughput requirement of 24 m^2 per hour, an in-line dopant applicator ("doper") system would need to run at the equivalent speed of 60 cm/min for 15.5-cm wide wafers, or 30 cm/min for 30-m wide wafers. During this period we have designed and assembled a dopant deposition system that is capable of uniformly applying dopant to wafers as large as 30 cm x 60 cm, and tested it with AP225 wafers.

Drive-in Process Development

For a continuous drive-in process, the heat source can be a pusher furnace or a belt furnace. Physically, the pusher furnace would have the wafers standing upright (that is, on edge, as in a tube furnace), while the belt furnace would have the wafers flat on the belt.

Both pusher furnaces and belts furnaces are widely available. If a long residence time or a small footprint is required, then a pusher furnace would be most appropriate. And the process is very similar to the "drive-in" process that is used with gas diffusions performed in tube furnaces. However, the overall cost of a pusher furnace process would be greater than that of a belt furnace since "diffusion boats" would still need to be loaded and unloaded, and the power consumption (due to losses from the large opening of the furnace) would be high. Belt furnaces may have a larger footprint than a pusher furnace, but the heat losses will be much lower and task required to load and unload the furnace is greatly simplified. Recently published results [3] indicate that "rapid thermal processing", with a time at temperature of only a few minutes, is capable of producing diffused emitters of good quality. As a result, we have focused our efforts on developing a drive-in process that is based on a belt furnace rather than a pusher furnace concept.

In order to achieve a rapid heating rate, it is necessary to use a belt that is light in weight compared to the mass of the silicon wafers. The thermal isolation between the temperature zones will be critical. Assuming these requirements are achieved, the furnace should be compact. For a furnace width of 24 inches (61 cm), which is a common size for an infrared belt furnace, two 30-cm wide wafers will pass though. At a rate of 60 cm/min, a 30-second process will occur within a 12-inch heat zone. Heating the wafer to the drive-in temperature and cooling it will require additional furnace length. However, we believe that the overall length of a drive-in belt furnace will be less than 20 feet, even with a moderately slow cooling rate.

During this period we have begun to develop specifications for the "drive-in" operation using our liquid dopant system. Using the design-of-experiment (DOE) program ECHIP, we have generated response surfaces of sheet resistance as a function of drive-in time, temperature, and furnace atmosphere for single-crystal silicon wafers. For this work, wafers were quickly loaded into and unloaded out of a tube furnace. The response surface shown below in Figure 8, indicates that a 30 ohm/sq diffusion is obtainable at relatively short times. Cell results for wafers diffused under these conditions were comparable to solar cells that were produced with a $POCl_3$ tube furnace diffusion. These results strongly suggest that a high-temperature, quick drive-in process is feasible, in which "belt furnace"-like conditions can provide an emitter sheet resistance compatible with downstream processing.

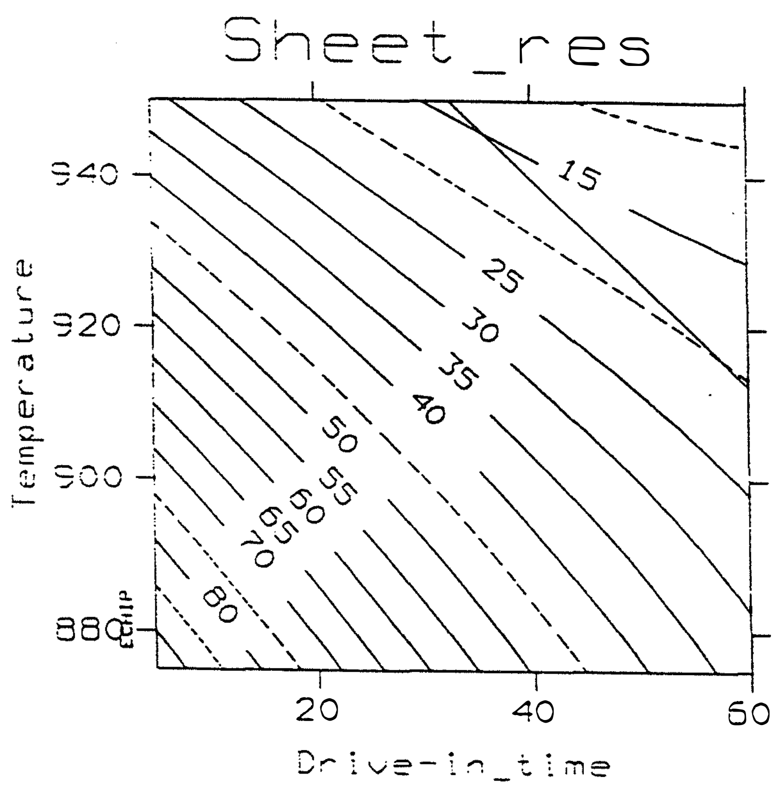


Figure 8. Response surface of sheet resistance as a function of drive-in time and temperature, with nitrogen ambient atmosphere.

Response surface verification experiments, conducted on production-level lots of single crystal solar solar cells, demonstrated that device performance from the prototype continuous feed diffusion process should be very similar to that of current batch-type processing. Neither emitter nor bulk material performance degradation was evident, as interpreted from the external quantum efficiency curves in Figure 9. In addition, the within-lot variation in sheet resistance and solar cell performance was comparable to, or in some cases better than, control lots using batch-type diffusion. The continuous-feed diffusion used in the verification experiment was 100% compatible with existing downstream processing; no modifications to any subsequent process were necessary.

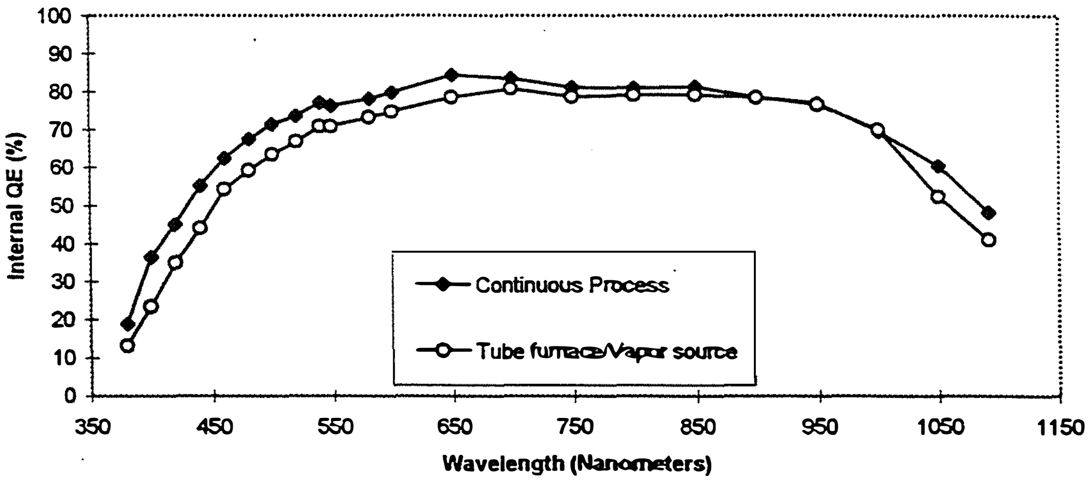


Figure 9. External quantum efficiency curves of typical single crystal silicon solar cells, diffused using batch-type and prototype continuous-feed processes.

Development of 16.5 cm Wide Sheet Process

The 16.5 cm wide sheet process continues the transition to a fault-tolerant, low-cost manufacturing process. The AP225 solar cell (240 cm^2) has been the main product of this process. Figure 10 shows a photograph of the sheet product leaving the Silicon-Film™ machine. Under the PVMaT-2a program a 17.1 kW array was fabricated for the PVUSA program. That array was installed in November 1994, and has been operating without fault for the past year. Plans are now in place to fabricate a 120 kW array for the Niagara Mohawk Power Company. This array will use the AP225 solar cell in the new large area panel format reviewed earlier.

Early in 1995 a number of important changes were made to the Silicon-Film™ machine. These changes include increasing throughput by 60%, enhancing reliability, and increasing material quality. With these changes complete, production volume of AP225 solar cells began to grow in the second half of 1995 (Figure 11). Growth in production volume is scheduled to continue into 1996, and into the foreseeable future.

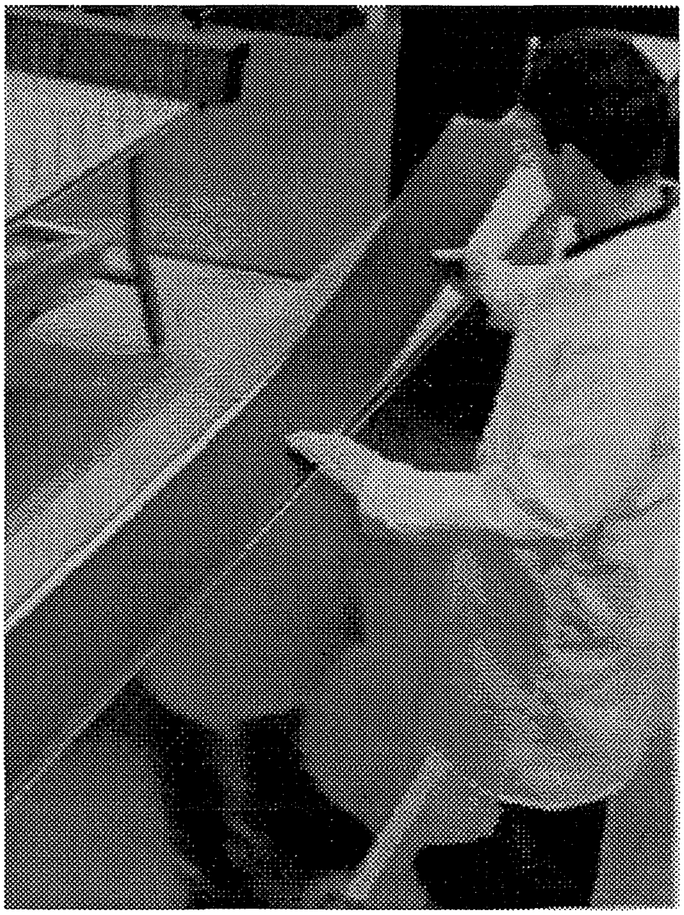


Figure 10. Silicon-Film™ sheet material.

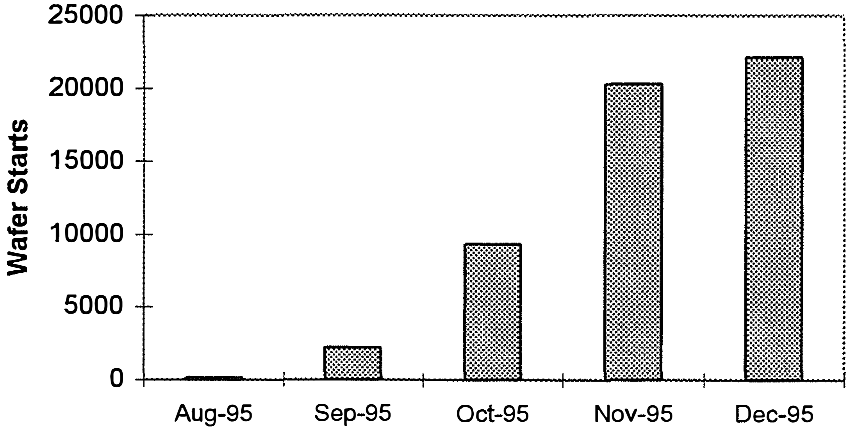


Figure 11. Quantity of Silicon-Film™ AP-225 solar cells entering the cell process line.

Lifetime Measurement

An investigation into contactless lifetime measurements is underway. The goal of this effort is to rapidly determine the minority-carrier lifetime of the as-grown Silicon-Film™ material.

Previously, we attempted to get this information using a commercially-available transient microwave photoconductivity decay (uw-PCD) system. This system was not able to generate any meaningful data since the transient signal was either completely absent or too small to accurately resolve. Lower frequency RF photoconductivity techniques are more suitable for heavily doped materials. We have recently acquired test equipment from Dr. Ron Sinton (Ron Sinton, Consultant) that provides a measurement of steady-state RF-photoconductivity. Using this equipment, strong photoconductive signals were measured on Silicon-Film™ material. Efforts are underway to develop a clear model for understanding the signal data generated. These initial data indicated that the measured signal correlated with lifetime on CZ control wafers, as theory would predict. Results for the polycrystalline Silicon-Film™ were not straightforward. For the limited sample tested, the signal did not appear to correlate with the lifetime.

Further testing is planned. We will plan to work with NREL to develop a model that allows us to better understand the results.

30 cm Wide Silicon-Film™ Sheet Production

The construction, installation, and testing of the new Silicon-Film™ Wide-Body machine was completed during this effort. Silicon-Film™ sheet material with a width of 31 cm was generated. Initial runs revealed the necessity for thermal profile tailoring at the outer edges of the plank to achieve optimized thermal growth parameters across the entire sheet width. Equipment changes were made and previously inherent film stress in the sheet was eliminated, resulting in the production of a 31 cm wide continuous flat sheet.

Early success in device performance was demonstrated by small area test structure solar cell data shown in Figure 12. The 0.2 cm^2 “mesa” solar cells were fabricated in a quick turn-around process that does not utilize a front contact metalization. Contact is made by directly probing the emitters, leading to lower voltages than seen in full solar cell processing. The 14 small area test structures were fabricated on a strip of sheet material that spanned from the center of the sheet to one edge. Uniformity of the devices was very good, and overall performance was comparable to test structures fabricated on the prototype Silicon-Film™ production machine (presently generating 16.5 cm wide material).

Parameter	*Median* *(of 14 cells tested)*	*Range*
Voc	500 mV	475 - 511 mV
Jsc	17.5 mA/cm^2	16.9 - 18 mA/cm^2
Ln (Diffusion Length)	34.5 μm	31.7 - 37.4 μm

Figure 12. Initial small area test data from very wide Silicon-Film™ sheet.

The nominal 31 cm wide sheet that generated the results shown in Figure 12 had grain sizes on the order of 500-800 microns. Silicon-Film™ material presently grown in the prototype production machine at 16.5 cm wide has grain sizes on the order of 1.5-2.0 mm. Continued optimization of the wide sheet thermal parameters is planned to increase the grain size for improved electrical properties. Experiments will also be run varying the sheet width to optimize performance, material yield, and throughput.

Continuous ribbon exiting the Silicon-Film™ Wide-Body machine is sectioned into nominal 31 cm x 102 cm planks for handling purposes. Solar cells will be fabricated on this entire area and sawn to size upon completion. For improved yields in the future, larger planks will be sectioned, eventually resulting in continuous production.

The first wide sheet material is called for in the fourth quarter of the contract (7/96), and the first solar cells are expected in the fifth quarter (10/96). We are planning to reach these milestones ahead of the original schedule.

Conclusion

AstroPower has succeeded in improving its material and processing capabilities during the first phase of this 3 year contract. Key results include the demonstration of a 14.6% efficient Silicon-Film™ solar cell. This laboratory result (1.0 cm^2) provides needed direction to the development and optimization of continuous, in-line, production processes. The continuous nature of the Silicon-Film™ sheet fabrication process is being extended into the solar cell processing sequence. Plans are in place to make the wafer cleaning, gettering, and diffusion steps all continuous during the scope of this program.

The changes in diffusion have become a necessity, as the size of solar cells being developed grows beyond the range that any conventional furnace can support. Under development now is a 1800 cm^2 solar cell (2 sq. ft.). These advances will accelerate the reduction of PV manufacturing cost for the Silicon-Film™ product.

References

[1] 13TH NREL Photovoltaics Program Review, (May 1995), AIP Conference Proceedings 353, American Institute of Physics, Woodbury, New York, 1995, p.283.

[2] A.S.Grove, Physics and Technology of Semiconductor Devices, John Wiley, New York, NY, 1967, p. 43.

[3] P.Doshi, A.Rohatgi,M.Ropp,Z.Chen,D.Ruby, and D.L.Meier, "Rapid Thermal Processing of High-Efficiency Silicon Solar Cells with Controlled In-Situ Annealing", First WCPEC, (1994), p.1299.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE January 1997	3. REPORT TYPE AND DATES COVERED Phase I Annual Technical Report, July 1995 - December 1995

4. TITLE AND SUBTITLE

Large-Area Silicon-Film™ Panels and Solar Cells; Phase I Annual Technical Report, July 1995 - December 1995

5. FUNDING NUMBERS

C: ZAF-5-14271-3
TA: PV705101

6. AUTHOR(S)

Rand, J.A.; Barnett, A.M.; Checchi, J.C.; Culik, J.S.; Collins, S.R.; Ford, D.H.; Hall, R.B.; Jackson, E.L.; Kendall, C.L.; Trabant, A.M.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

AstroPower, Inc.
Solar Park
Newark, Delaware 19716-2000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

SR-520-22535

DE97000209

11. SUPPLEMENTARY NOTES

NREL Technical Monitor: R. Mitchell

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

UC-1280

13. ABSTRACT *(Maximum 200 words)*

This report describes AstroPower's success in improving its material and processing capabilities during the first phase of this 3-year contract through the Photovoltaic Manufacturing Technology (PVMaT) program. Key results include the demonstration of a 14.6%-efficient Silicon-Film™ solar cell. This laboratory result (1.0 cm^2) provides the direction needed to develop and optimize continuous, in-line production processes. The continuous nature of the Silicon-Film™ sheet fabrication process is being extended into the solar-cell processing sequence. Plans are in place to make the wafer cleaning, gettering, and diffusion steps all continuous during the scope of this program.

14. SUBJECT TERMS

photovoltaics ; large-area solar cells ; solar cell performance ; continuous processing ; Silicon-Film

15. NUMBER OF PAGES
24

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102