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Light-Trapped, Interconnected, Silicon-Film™ Modules

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1 INTRODUCTION

1.1 Project Overview

AstroPower is developing a module manufacturing technology based on a film-silicon technology. AstroPower, as a Technology Partner in the Thin-Film Partnership, is employing its Silicon-Film™ technology toward the development of an advanced thin-silicon-based, 400 watt, 4 ft x 8 ft (2.97 m^2) photovoltaic panel product for use in power applications. This module will combine the design and process features of the most advanced thin-silicon solar cells with light trapping. These solar cells will be integrated into a low-cost interconnected array.

This advanced product includes the following features:

- silicon layer grown on a low-cost substrate,
- a 50-micron thick silicon layer with greater than 100 micron diffusion lengths,
- light trapping due to back-surface reflection,
- back surface passivation,
- 900 cm^2 interconnected sub-module.

The 50-micron thick silicon layer achieves high solar cell performance and can lead to a sub-module conversion efficiency as high as 19%. These performance design features, combined with low-cost manufacturing using relatively low-cost capital equipment, continuous processing and a low-cost substrate, will lead to a panel cost of less than $1.00/watt.

The three year project involves five tasks and builds on present processes and capabilities. Tasks I and II are intended to increase module efficiency by optimizing the sub-module and sub-element material properties and structure. Tasks III and IV are intended to reduce the cost of module integration by improving the module fabrication processes and module efficiency, and understanding encapsulation and reliability issues. Task V is intended to improve the technical base supporting the manufacturability of the near-term product by developing prototype manufacturing processes.

During the first year program, the following results were achieved:

- a confirmed 13.8% efficient, thin solar cell fabricated on a low-cost substrate,
- demonstration of films grown on barrier-coated substrates which, after being subjected to a phosphorous gettering process, exhibited diffusion lengths greater than 250 μm,
- development of a new, low-cost substrate and barrier coating which supports the growth of thin film of silicon,
- demonstration of optical confinement in 60-μm thick films with 80 μm diffusion lengths.

During the second year of the program, our efforts were focused on the first three tasks, with emphasis on Task III: the development of key sub-module fabrication processes. Key results of the second year program include:

- development of a new thin-film growth concept process based on attaching the low-cost substrate to the thin silicon layer after film growth,
- development of a new technique to achieve light trapping in thin layers of silicon based on pigmented high-temperature glass materials,
- development of key sub-module fabrication processes, including contact grid design, sub-element isolation and screen-printed interconnection.

1.2 Technical Approach

The solar cell sub-element device structure (Figure 1b) consists of a thin (35–50 μm) polycrystalline silicon layer which is grown on a low-cost substrate material. The thin layer/low-cost substrate approach results in lower cost by minimizing the use of relatively expensive silicon feedstock material. Diffusion lengths equivalent to twice the device thickness are required to assure high carrier collection throughout the bulk of the base layer, enabling the use of imperfect materials and increased doping levels for improved solar cell voltage and fill factor.

Thin films grown on an insulating substrate allow the fabrication of large-area, series-interconnected sub-modules (see Figure 1a) [1]. The sub-module design incorporates a method of partitioning the thin-film photovoltaic layer into sub-elements and reconnecting them as a series connected array. The sub-module design also incorporates conductivity enhancement to minimize the power loss associated with lateral current flow through the thin base layer.

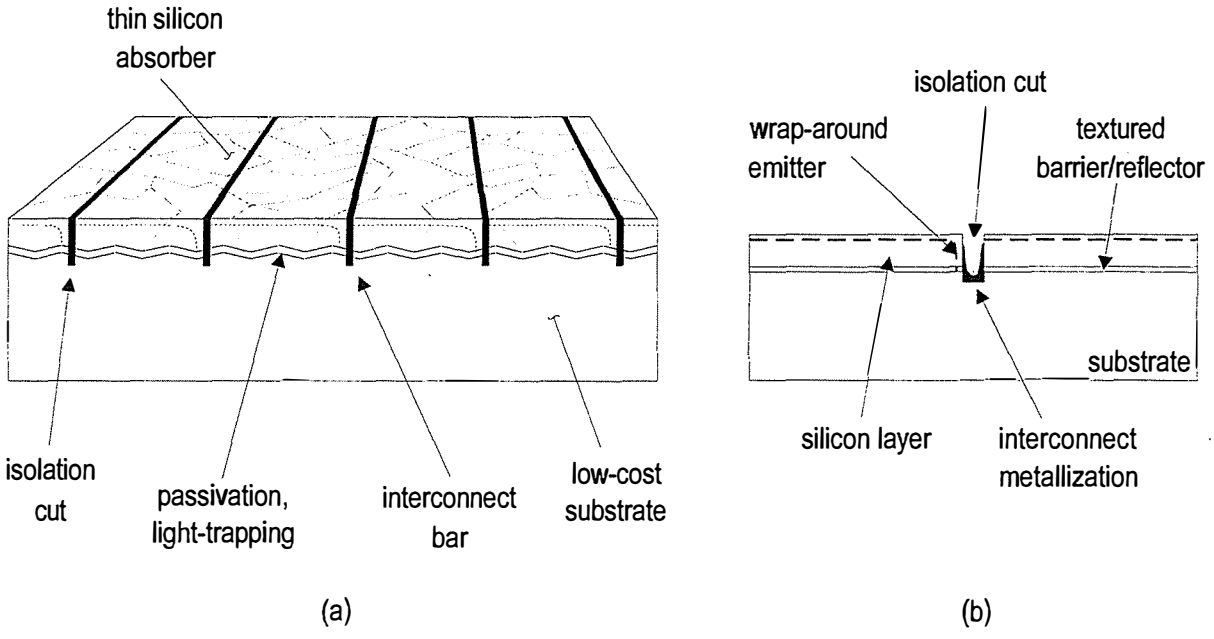


Figure 1. (a) Solar cell sub-module device structure and (b) sub-element device structures.

The solar cell device structure incorporates light trapping and back-surface passivation to improve energy conversion efficiency. Light trapping is achieved by using a diffuse reflector located at the back surface of the thin film, resulting in enhanced optical absorption of weakly

absorbed light and improved current generation. Electrical passivation of the back surface is achieved by developing the barrier layer to minimize surface recombination velocity at the barrier/silicon interface. Back-surface passivation results in improved current plus improved voltage and fill factor by minimizing the reverse saturation current.

2 TECHNICAL PROGRESS OF THE SECOND-YEAR PROGRAM

2.1 Film Growth Development

A significant amount of progress was made in the area of film growth during the first year of this program. During this effort, layers as thin as 60 μm, with grains as large as 1 mm were grown on a new barrier-coated substrate [2]. Also, the average diffusion length of devices processed with phosphorous gettering exceeded 100 μm, and several devices exhibited diffusion lengths greater than 250 μm. Efficiencies as high as 13.8% were measured in solar cells fabricated in this material. During the first part of the second year, we focused on improving the uniformity of grain morphology and thickness over large area (> 500 cm^2). Near the end of second year of the program, an alternative method of forming a thin layer of silicon on a low cost substrate was evaluated. This approach is described below.

Growth with Subsequent Substrate Attachment. In this approach, the substrate would be added to the thin (100 μm), freestanding film immediately after the growth process. One of the significant advantages of this method is that the temperature requirements on the substrate material would be relaxed, increasing the number of materials suitable for the substrate. Also, access to the back surface is available after the film growth, which expands the number of back-surface passivation and back surface reflectors suitable for the structure.

Figure 2 shows how a sub-module could be formed with this approach. Much of the fabrication can be completed before the substrate is attached. If the contact structure is properly arranged, the final isolation and interconnection can still be performed monolithically.

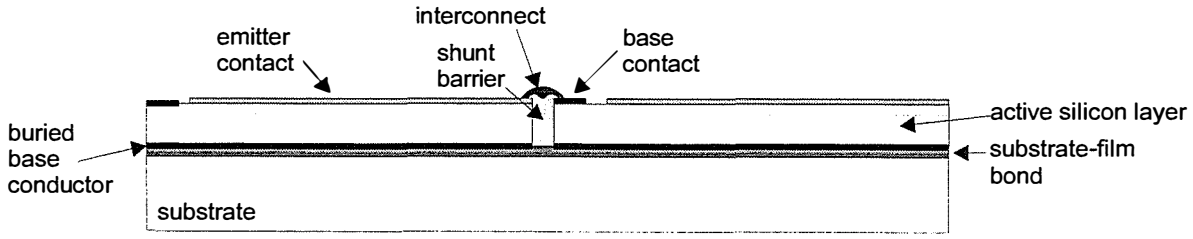


Figure 2. Monolithic sub-module based on attaching the substrate to a thin freestanding film of silicon.

Previous efforts have indicated that it may be practical to grow thin, substrate-free films (~100-μm thick) by the Silicon-Film™ process [3]. In the previous effort, freestanding films of 100–125 μm were grown with minority carrier diffusion lengths between 48 and 61 μm after

gettering. We have fabricated and tested several 0.5 cm^2 devices based on this substrate-attach paradigm. Initial device efficiencies range between 10–12%.

As stated above, one of the advantages of this approach is that it makes more substrate materials available. For example, sintered aluminum nitride wafers are not compatible with the Silicon-Film™ process if the film is to be grown directly on the AlN wafer. However, the AlN wafer is compatible with a lower-temperature substrate attachment process which allows thin layer to be supported through subsequent processing.

AlN wafers illustrate the advantage of reflective substrate materials which would improve the current generation of the thin silicon solar cell by reflecting weakly absorbed light back into the silicon layer. Figure 3 shows the reflectivity of an AlN wafer and a thin silicon layer to which the AlN wafer has been attached. The escape reflection noted on the graph indicates that light is being reflected by the substrate at the back surface and is escaping through the front surface.

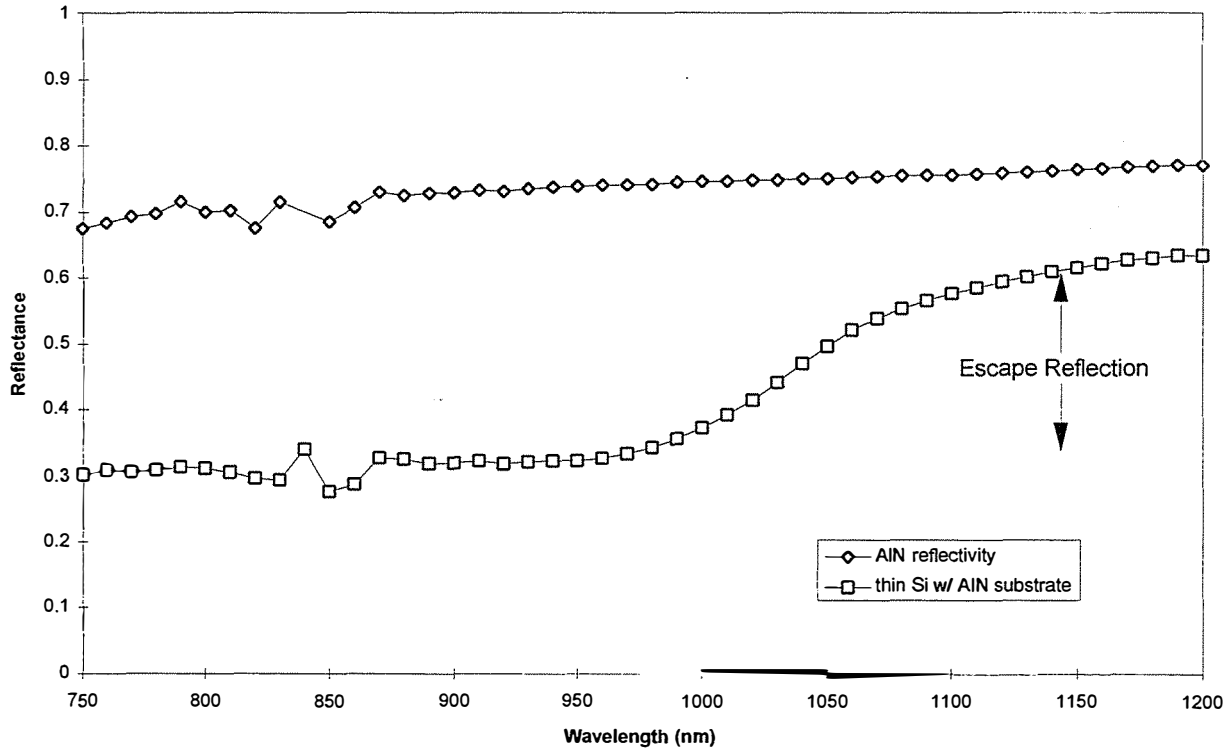


Figure 3. Reflectivity of AlN wafer and of a thin silicon layer with an AlN wafer attached to the back surface.

2.2 Sub-Element Process Development

In the first year program, a sub-element efficiency of 13.8% was achieved. The same baseline solar cell fabrication sequence was used for all processing in the second year program [4]. A new technology was developed to improve the light trapping in the thin silicon solar cell. This technology is based on the use of pigments in a high-temperature glass medium. The concept is explained in more detail in the following.

Light Trapping with Pigmented-Glass Layers [5]. "Pigmented materials" consist of two substances of different refractive index. The "pigment" is in the form of small particles, usually of high refractive index. The "medium" is a binder, usually of low refractive index, throughout which the pigment is dispersed. Paint is a good example of a pigmented material. If the particle size and refractive indices are carefully chosen, light interacts very strongly with and is strongly scattered by the pigment. The result is a broadband and highly diffuse reflecting material.

Figure 4 illustrates the general principle of light trapping through the use of pigmented materials. Adjacent to the back surface, the pigmented material acts as a reflector, scattering weakly absorbed light back into the thin silicon layer. Furthermore, the reflector scatters the light in a diffuse pattern, and the escaping light can be perfectly reflected again at the front surface, back into the silicon layer, by the phenomenon of total internal reflection. In this case, light will travel a much greater distance than the thickness of the silicon layer and the absorption of light will therefore be enhanced.

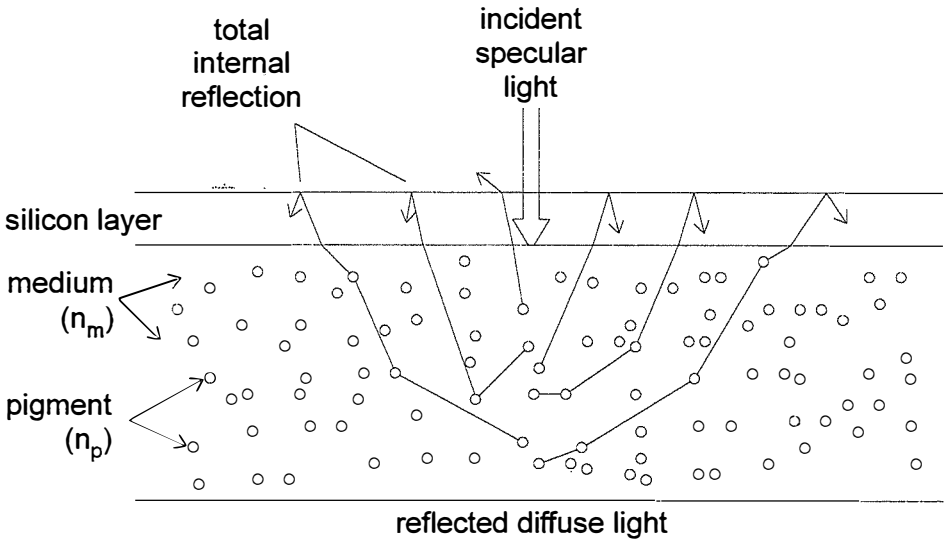


Figure 4. The concept of pigmented materials for light trapping in thin films of silicon.

The scattering phenomenon is described by Mie Scattering Theory [6]. When the pigment particle size is optimized (at near the wavelength of light), the scattering efficiency is

highest as illustrated in Figure 5.† This is due to the strong electromagnetic interaction between the scattering particle and the light that occurs when the particle size is similar to the wavelength of light.

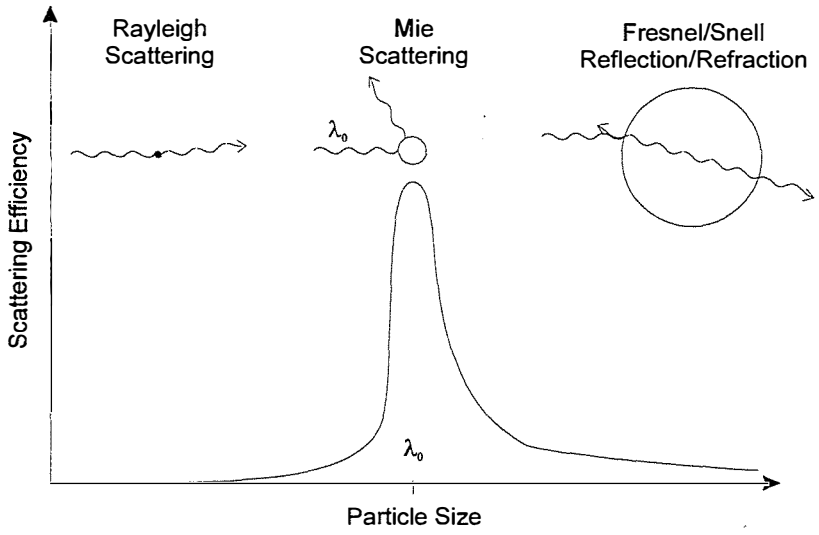


Figure 5. Relative scattering efficiency as a function of pigment particle size.

Mie theory describes how an electromagnetic plane wave interacts with a dielectric sphere when the sphere diameter is approximately equal to the wavelength of light. The incident light excites one or several electromagnetic modes within the sphere. Figure 6 illustrates the electric and magnetic field lines of the first three electromagnetic modes. The electromagnetic oscillations of the sphere then excite secondary electromagnetic waves (of the same wavelength) outside of the sphere. If the sphere size is optimal, the effect is analogous to a quarter-wavelength optical coating. The interference results in backward reflection of the incident wave. At larger sphere sizes, the incident wave excites multi-pole modes, and a smaller fraction of the incident wave is reflected backward. In the limiting case (i.e., a very large sphere), the backward reflected wave is given by Fresnel theory.

† When the pigment particle size is either much larger or much smaller than the wavelength, Fresnel Refraction Theory and Rayleigh Scattering Theory explain the scattering behavior.

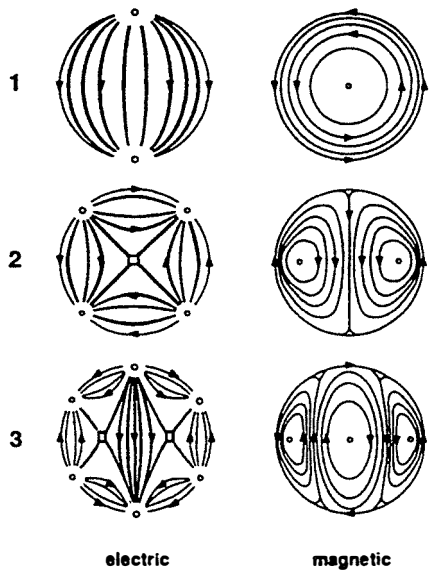


Figure 6. The first three partial electric and magnetic modes of oscillation within a dielectric sphere excited by light incident normal to the page [6].

Achieving a high degree of optical confinement is complicated by the fact that, at least for films grown on substrates, access to the back surface is limited after the film is grown. Substrate removal and subsequent application of a reflector seem incompatible with low-cost, high-throughput manufacturing. Therefore, arrangement for optical confinement must be made before the film is deposited. This almost certainly restricts metallic reflectors from all but the very lowest-temperature film growth techniques because, in general, most highly-reflective metals are unstable at higher temperatures. On the other hand, dielectric layers, either single layers or multiple layer reflective stacks (i.e., Bragg reflectors), are more stable at higher temperatures. However, these types of reflectors either suffer from low reflectivity (i.e., about 15% for single-layer dielectric-silicon interface), or limited wavelength range (typical of a Bragg-type reflector).

Pigmented materials are capable of high reflectivity over a broad wavelength range, and their diffuse pattern of reflection is preferred for light trapping. A wide variety of high-temperature materials like silica, silicon nitride, silicon carbide, and related glassy materials could allow compatibility with high growth temperatures. A reflecting material could be applied and fired on a substrate material like enamel paint, or a suitable pigment could be added directly to the substrate, making it reflective. Furthermore, pigmented materials have potential for low cost. White paint, for example, costs approximately \$0.50 per m^2.

The science and technology of pigmented materials, especially paint, are well known [e.g., 7]. The following design rules can be used to achieve high reflectivity.

1. There is an optimal pigment particle size for the wavelengths of interest.
2. A high ratio of pigment-medium refractive indices is desired.

3. There is an optimal pigment volume fraction.
4. Low absorption coefficient and high scattering coefficient are desired for both media.

During the second year of this program, the application of pigmented materials was explored. An optical model [8] was developed to predict the optical enhancement factor of thin silicon layers with pigmented reflectors. The optical enhancement factor is the ratio of effective optical thickness to actual thickness. It is an often-cited figure of merit for light-trapping schemes. Yablonovitch and Cody [9] derived an expression for the upper limit to the equivalent optical thickness for light uniformly distributed within the silicon. They predicted that, for weakly absorbed, uniformly distributed light in a layer with an ideal front anti-reflection coating and perfect rear reflector, the optical enhancement factor for silicon is $Z = 4n_{Si}^2$, where n_{Si} is the refractive index of the silicon layer. For silicon, the optical enhancement factor approaches 50 for weakly absorbed light.

An analogous expression for thin layers of silicon with scattering back-surface reflectors

$$Z = 2L_{eff}n_{refl}^2,$$

where L_{eff} is the effective path length (normalized to the silicon layer thickness) of diffuse light traveling in the silicon layer and n_{refl} is the effective refractive index of the pigmented material (approximately equal to the medium's refractive index). For the special case where $n_{refl} = n_{Si}$, the effective optical path length, L_{eff} equals 2, and this equation reduces to Yablonovitch and Cody's original expression.

From this expression, it is evident that a high refractive index for the medium of the back scattering reflector is desired. If a glass material is used as the medium, the refractive index of the pigmented glass would be approximately between 1.5 and 1.6. This leads to an optical confinement factor of approximately 5. This represents a modest improvement in optical confinement and techniques to improve this figure will be explored in the coming year.

Several pigmented glass materials were constructed by mixing glass paste precursors with titanium dioxide powder. Figure 7 shows a mock up of a thin silicon film grown on a substrate coated with a pigmented glass material. The film has been cut away to reveal the underlying reflective coating. The reflectivity curve of a similar coating is shown in Figure 8. The measured external reflectivity of the layer is about 90% over the wavelength range between 750 and 1200 nm. The bulk or internal reflectivity of the pigmented glass (that which is corrected for the effect of the surface reflectivity) is above 95% over this wavelength range. When in contact with silicon, the reflectivity of the pigmented glass/silicon interface is predicted to be about 95% over this wavelength range.

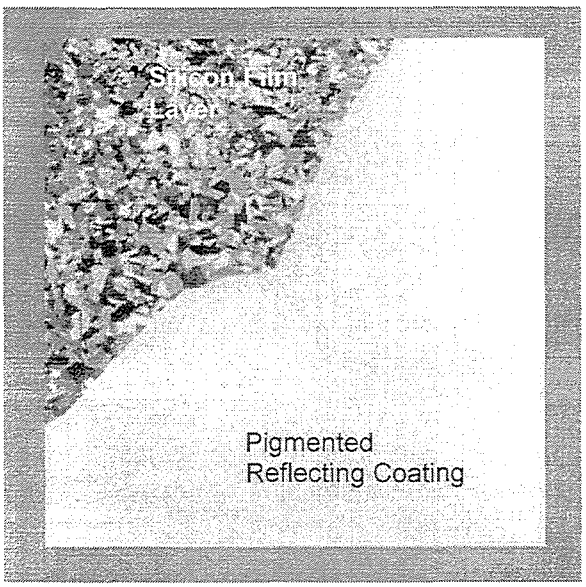


Figure 7. The silicon layer is cut away to show the underlying pigmented reflecting coating on the substrate.

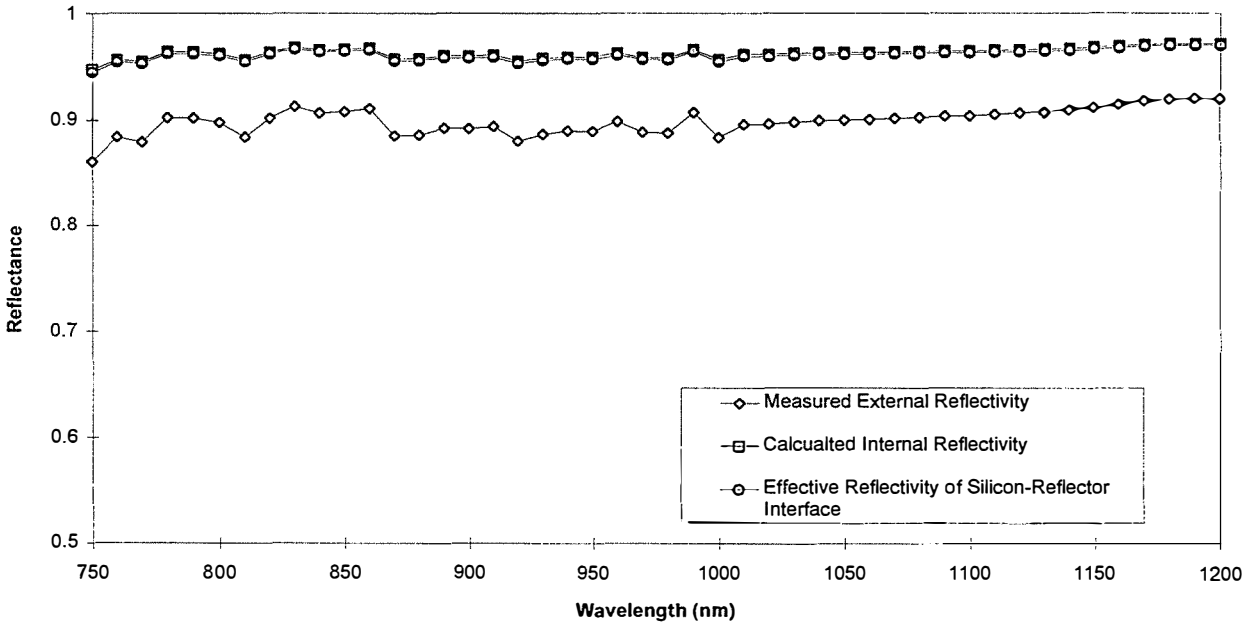


Figure 8. Measured external, calculated internal reflectivity of pigmented glass barrier layer. Also included is the predicted silicon/pigmented glass interface reflectivity.

During the coming year, we will continue to develop this concept for use in thin-film silicon solar cells.

2.3 Sub-Module Design Issues

Most of the design issues for the integrated sub-module relate to the conductor grid structure. There are three possible configurations: all grids on the top surface, emitter grids on the top surface/buried base grids, and all buried grids. During the second year of this program, we evaluated, constructed and tested the first two sub-module configurations. The key issues are discussed in the following paragraphs.

All Grids on the Top Surface. Figure 9 shows the layout of one sub-cell of this configuration. The emitter and base contacts/conductors conduct current laterally across the sub-element to the interconnect metallization located over the isolation cut. The different type conductors are staggered from one sub-element to the next to allow easy interconnection of the base of one sub-element to the emitter of the adjacent sub-element (to the right side in Figure 9).

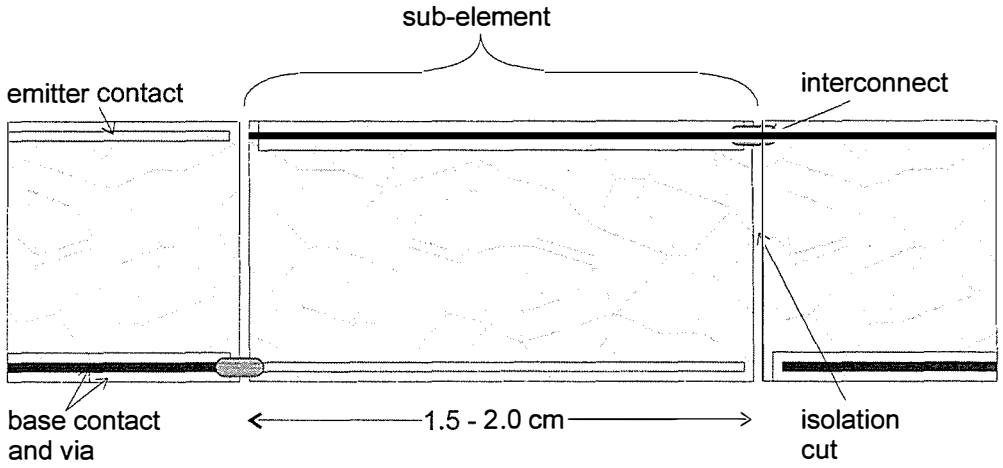


Figure 9. Plan view of sub-module grid structure when all grids are located on the top surface.

The advantage of this configuration is that the base conductors can be applied after the thin film of silicon has been grown on the substrate, and existing, well-developed metal contact metallization techniques (namely aluminum evaporation or aluminum-glass screen print paste) can be used. The major disadvantage is that, when on the top surface, the base conductor contributes to the overall shading loss of the grid structure. This problem is exacerbated by the need to form a via through the emitter to allow the base conductor to contact the base layer without shunting to the emitter. (The base contact and via arrangement are shown in Figure 9.) This increases the effective shading of the base conductor and can result in a total shading loss that is greater then twice that of a standard silicon solar cell contact structure. Therefore, optimization of the grid design is required for minimal losses.

A model was developed to predict the parasitic series resistance and shading losses. Series resistance losses arise from lateral conduction in the emitter and base, grid conductors and interconnect metallization, and contact resistance effects between the grid conductor and the

silicon layers. Figure 10 defines the relevant geometric quantities used in the model. Sample equations describing the major series resistance and shading losses are included in the Appendix.

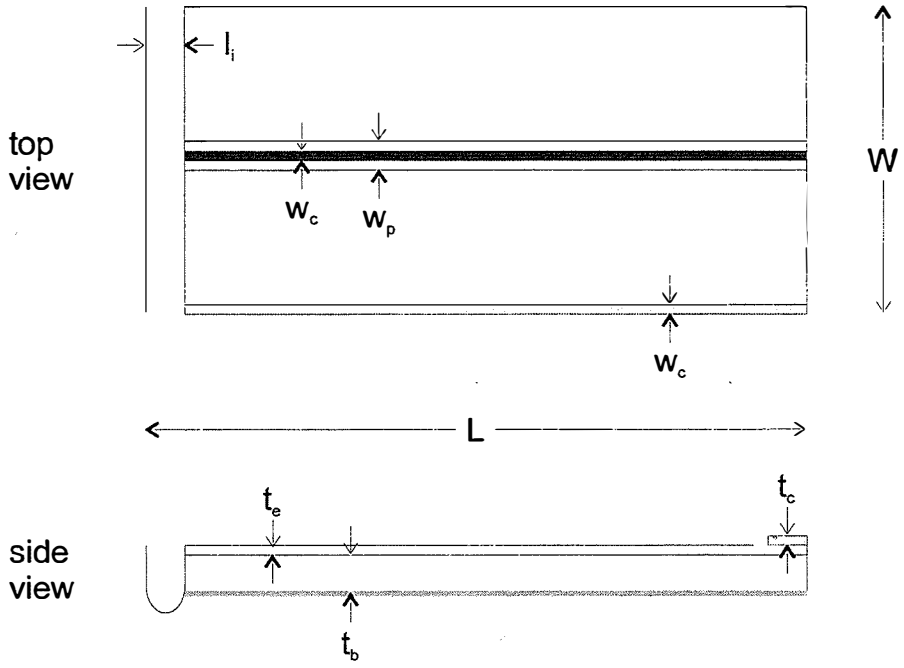


Figure 10. Geometric details of the sub-module used for modeling parasitic series resistance and shading losses.

Using conservative design rules (see Table 2) for conductor width, thickness, conductivity, etc. leads to relatively high predicted total power loss of 18–20%. Table 1 summarizes the contribution of various loss mechanisms for the design rules listed in Table 2.

Table 1. Contribution of various loss mechanisms to the total predicted power loss of the all-grids-on-top configuration.

Loss Mechanism	% Loss (of Total Available Power)
Emitter Series Resistance	1.88
Base Series Resistance	0.45
Emitter Grid Series Resistance	0.44
Base Grid Series Resistance	0.47
Total Grid Contact Resistance	4.85
Interconnect Metal Resistance	0.30
Interconnect Metal Shading	0.52
Kerf-related Shading	0.80
Emitter Grid Shading	3.70

Base Grid and Via Shading	6.89
Total Losses	20.46

Table 2. Fabrication parameters used in the summary presented in Table 1.

Fabrication Parameter	Symbol	Value
Emitter Sheet Resistivity (ohm/sq.)		35
Base Sheet Resistivity (ohm/sq.)		6.7
Grid Width, Height (μm)	w_c, t_c	150, 15
Base Via Width (μm)	w_p	300
Grid Resistivity (ohm-cm)		5e-6
Grid Contact Resistivity (ohm-cm^2)		.01
Isolation Kerf (μm)	l_i	150
Grid-Grid Spacing (cm)	W	0.360
Sub-Element Length (cm)	L	1.57

Emitter Grids on the Top Surface/Buried Base Conductor. The relatively high shading loss associated and the series resistance associated with locating the base contact on the front surface can be eliminated by burying the contact below the thin silicon active layer. In the case where the film is grown on the substrate, the buried base conductor must be incorporated before the film growth step. In the case where the substrate is attached to the film after growth, the base conductor can be incorporated after the film growth step, and existing, well-developed metal contact metallization techniques can be used. The interconnection metallization is relatively more complicated in this configuration, because connection must be made from the front emitter to the buried base contacts. Figure 11 illustrates this configuration.

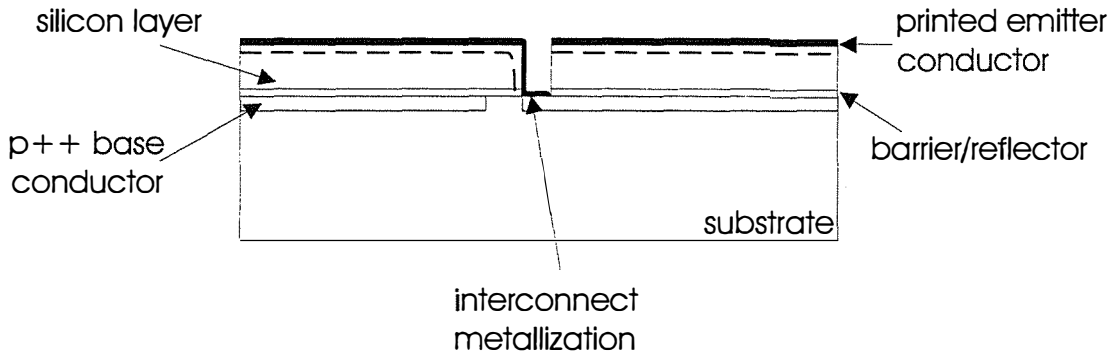


Figure 11. Side view of structure incorporating buried base contacts. Connection is achieved by feeding the interconnect metal through the isolation trench.

This configuration was modeled to compare the total parasitic losses. Using the same conservative design rules for conductor width, thickness, conductivity, etc. leads to lower predicted total power loss of 9–11%. Table 3 summarizes the major contributing loss mechanisms of this configuration.

Table 3. Contribution of various loss mechanisms to the total predicted power loss of the emitter grids on the top surface/buried base conductor configuration.

Loss Mechanism	% Loss (of Total Available Power)
Emitter Series Resistance	2.37
Base Series Resistance	1.32
Emitter Grid Series Resistance	1.88
Base Grid Series Resistance	0.02
Total Grid Contact Resistance	0.19
Interconnect Metal Resistance	0.30
Interconnect Metal Shading	0.52
Kerf-related Shading	1.80
Emitter Grid Shading	2.41
Base Grid and Via Shading	0.00
Total Losses	10.81

2.4 Sub-Module Process Development and Results

Most of the fabrication steps for the sub-module are identical to those used in standard silicon solar cells, for example, emitter diffusion, emitter passivation and anti-reflection coatings. Several additional fabrication steps are required, however, including top-side base contacts, sub-element isolation and interconnect metallization. The development of these fabrication steps is discussed in the following paragraphs.

Top-Side Base Contacts. Sub-modules with top-side base contacts were examined because of the relative ease of forming the sub-element interconnection with both conductors located on the top surface. An oxide diffusion mask was used to reveal the base layer on the front surface. The diffusion mask was applied before the wafer was diffused, and after the diffusion step, the oxide was removed by chemical etching in dilute hydrofluoric acid. The oxide diffusion mask is patterned lithographically by screen printing an etch-resistant paste on the wafer.

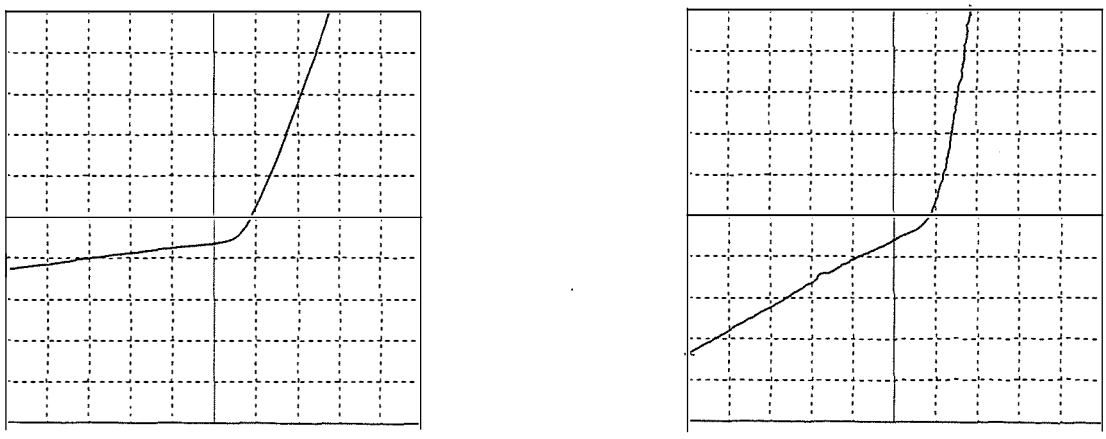
One of the key issues is printing the base contact within the via area. Sufficient width for the base via is required to prevent accidental electrical contact between the base contact and the emitter. This would result in severe shunting. At the same time, it is desirable to minimize the base via width to reduce the effective shading losses of the via.

We examined conventional, screen printed glass-paste-based materials for the top-side grid conductors. Because of the lithography limitations of screen printed conductors, the conductors are relatively wide (w_c >100 μm). This leads to relatively high shading losses. Further, the via opening through the emitter, w_p, must be relatively large for alignment purposes.

Alignment of the p-contact within the p-via is generally good across the entire area of completed sub-modules. However, in some areas of the sub-module the p-via pattern is not complete due to two factors. First, the surface of the polycrystalline wafer is highly textured due to the anisotropic etch used in surface preparation. Second, the wafer is not uniformly flat. Therefore, some additional work is needed to improve the print quality of the p-via. It is likely that switching to a isotropic etch, like the CP etch, and improving the wafer flatness by optimizing the growth conditions can improve the print quality of the p-via.

Individual sub-elements of a working sub-module were tested for voltage, current, shunt resistance and series resistance characteristics. A completed sub-module was partitioned into an array of small-area test solar cells by scribing through the emitter with a dicing saw. Each solar cell is 0.64 cm^2 and contains one emitter grid and one base grid.

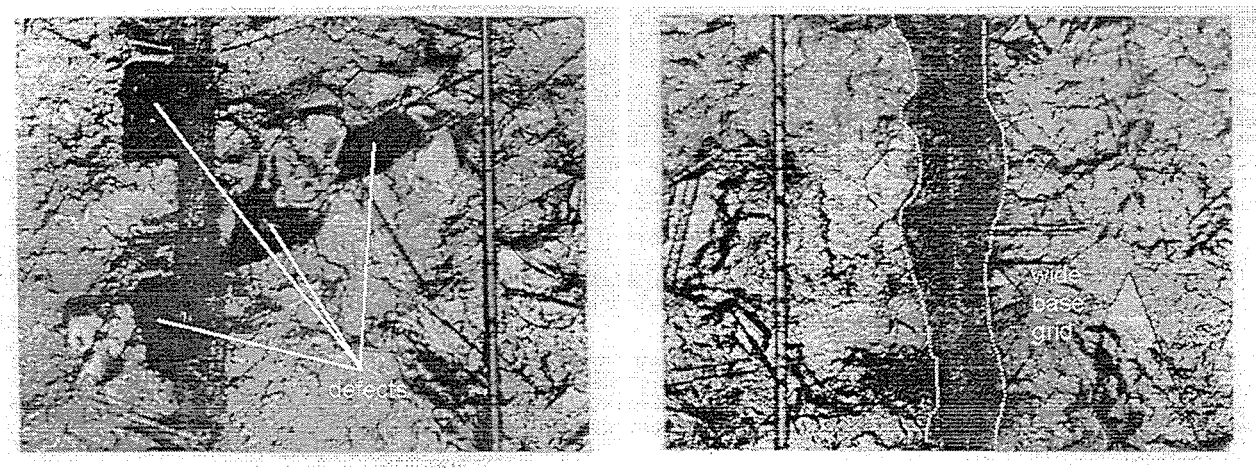
Two typical current-voltage curves, measured at one sun, are shown in Figure 12. The curves reveal both shunt- and series-resistance losses. The shunt resistance is about 600–900 Ω-cm^2 in the "best case" solar cells. This represents a loss of 0.2–0.3 mW/cm^2 or about 4–7 percent of the available power. The series resistance is about 7–10 Ω-cm^2 in these solar cells, representing a loss of 0.7–1.0 mW/cm^2 or 15–22 percent of the available power.



(a) *(b)*

Figure 12. Typical I-V curves measured on small-area sub-elements: (a) best case and (b) worst case curves. The horizontal scale is 0.5 mV/div, and the vertical scale is 10 mA/div.

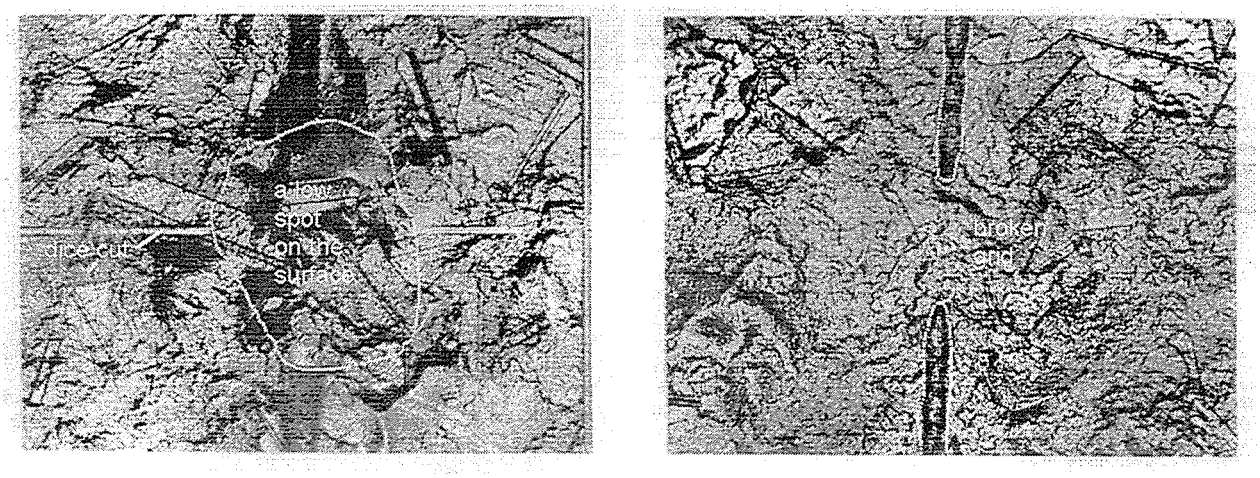
The low shunt resistance in some "worst case" solar cells is caused by a few failure mechanisms. Devices with small bumps were badly shunted. This is a rare material defect and is not a concern. On a few devices, the base contact was poorly printed. A conduction path to the emitter exists where the wide base contact overlaps the emitter. This rarely occurred. A third shunt problem was caused by incomplete dicing isolation. Because of the surface roughness, the dicing cuts were not complete on some devices. The effects are illustrated in Figures 13a, 13b and 14a. We expect to eliminate these losses by attention to detail in the fabrication sequence.



(a) *(b)*

Figure 13. Photomicrographs showing two causes of shunts in the small area sub-elements: (a) material defects and (b) wide base grids. (50X)

High series resistance in other "worst case" solar cells are caused by broken base or emitter grids (see Figure 14b). Several causes may be responsible for this problem, e.g. surface roughness, dry ink on the print screen, or non-optimized print conditions. This effect occurred mostly at the wafer edges, suggesting that the screen print process requires optimization.



(a) *(b)*

Figure 14. Photomicrograph showing (a) incomplete isolation causing a shunt, and (b) a broken emitter grid causing high series resistance. (50X)

Sub-Element Isolation. Two techniques are well suited for isolating the grown film into sub-elements: dicing and laser scribing. Both have excellent control over trench depth and width and both have sufficient throughput. During the second year, we utilized dicing with good success. Typical trench depths exceed 250 μm and typical trench widths were 40–45 μm.

Interconnection Metallization. We explored interconnection materials based on screen printable conducting polymers and conducting glass-frit-based pastes. Ideally, a high viscosity, conducting material would be printed directly over the isolation groove, however, an inert plastic or polymer material can alternately be used to planarize the isolation trench, relaxing viscosity the requirements on the conducting material. Figure 15 shows the resulting metallization after printing and firing of a medium-viscosity conducting glass-frit-based screen print-able paste. It can be seen that over the top corners, the conductor is very narrow and broken in some cases.

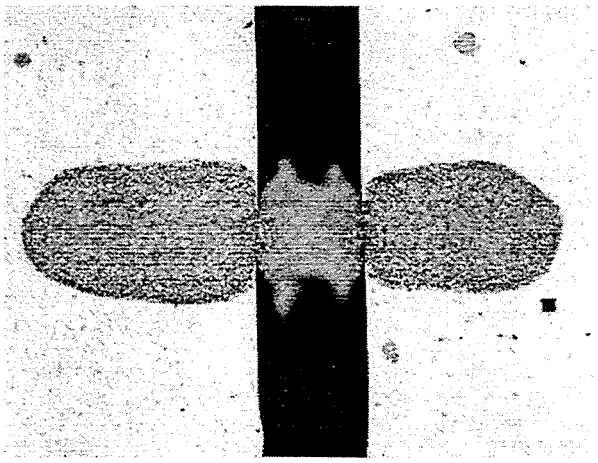


Figure 15. Printed and fired glass-frit-based, conducting interconnect metallization illustrating narrowed conductors (100X).

Higher viscosity glass-frit pastes improved the situation, however, the result was not satisfactory. A copper-loaded epoxy paste with a high viscosity has demonstrated the desired interconnection over a diced isolation trench. Figure 16 shows the initial conductive trace after curing.

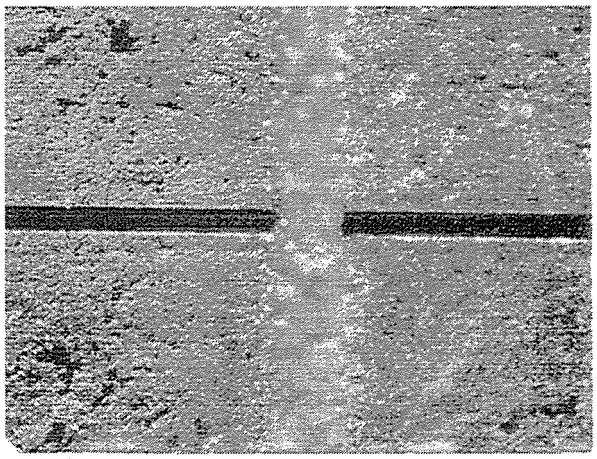


Figure 16. Initial print-over interconnect bridging of a diced trench with high viscosity conductive epoxy (60X).

The copper-loaded epoxy has been very successful for forming a conducting interconnect across deep, diced trenches. Full development of the screen printing parameters and curing cycle of the copper-loaded epoxy interconnects led to the printed interconnects shown in Figure 17

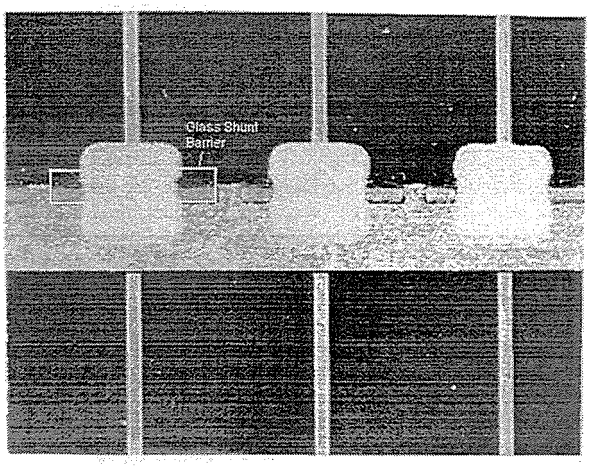


Figure 17. Photograph of interconnect metallization. The squares are the printed copper-loaded epoxy interconnect metallization. The vertical lines are the emitter grid conductors and the horizontal bar is the base bus conductor.

One of the problems with the copper-based epoxy is that it makes a weak ohmic contact to diffused n-type and bulk p-type silicon and can potentially shunt the device. To alleviate this problem, a transparent, non-conducting glass shunt barrier is incorporated into the structure. The seal glass is applied to areas where a shunt can occur. For example, contact between the emitter contact and the base layer (inside the isolation trench) would shunt the sub-element. the glass shunt barrier is outlined in Figure 17.

Two glasses, Ferro 11-036 and Electro Science Labs D4035, which are fired at 420°C and are thermally matched to silicon were examined. Electrical tests indicate that the seal glass makes an effective insulator to the diffused emitter. We have also determined that the glass is effective at filling the isolation trench, helping to planarize the surface of the wafer, aiding the screen printing of the copper-loaded interconnect epoxy.

Figure 18 shows a completed sub-module structure. An I-V characteristic of one sub-element of this sub-module is shown in Figure 19.

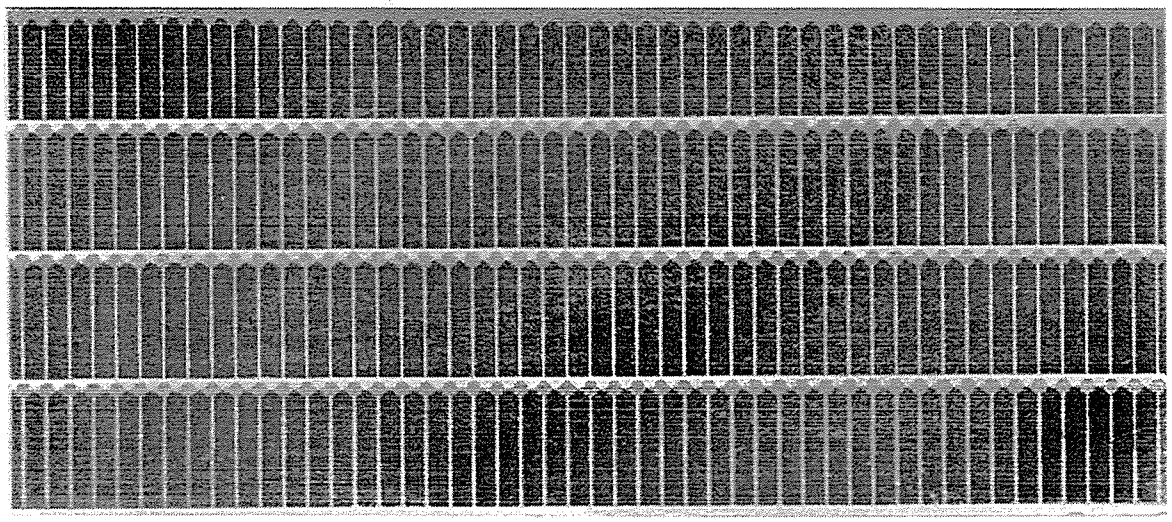


Figure 18. Photograph of four elements of first completed sub-module.

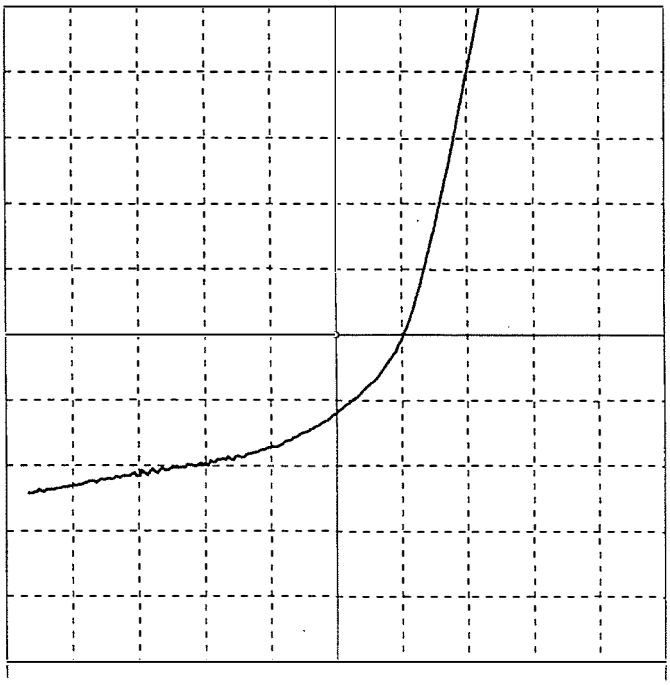


Figure 19. I-V characteristic of first completed sub-module.

3 SUMMARY AND THIRD-YEAR OBJECTIVES

The third-year program will focus on continued development of the substrate for light-trapping and passivation properties. We will continue to explore the concept of attaching a substrate to thin (100 μm) freestanding layers of silicon. The pigmented reflector concept will also be developed. The feasibility of incorporating all-buried-contact schemes with the attached substrate and pigmented reflector concepts will be determined. A second area of focus will be the continued development of the basic fabrication technologies related to the formation of the monolithically integrated sub-module. This includes techniques for sub-element isolation, interconnection, and conductivity enhancement. Finally, manufacturing technologies will be adopted or developed for key fabrication processes.

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Appendix: Sample design equations for all-contacts-on-top sub-module

Equations describing the major series resistance and shading losses are below. Figure 10 defines the variables used.

Emitter Resistance Loss (in W/segment)

$$P_{R,e} = \frac{2}{3} \cdot {J_{mp}}^2 \cdot \left(W - \frac{w_p}{2} \right)^3 \cdot \left(L - l_i \right) \cdot R_{sh,e}$$

Base Resistance Loss (in W/segment)

$$P_{R,b} = \frac{2}{3} \cdot {J_{mp}}^2 \cdot \left(W \right)^3 \cdot \left(L - l_i \right) \cdot R_{sh,b}$$

Emitter Grid Resistance Loss (in W/segment)

$$P_{R,eg} = \frac{1}{3} \cdot J_{mp}{}^2 \cdot (L)^3 \cdot \frac{w_{eg}}{(w_{eg} \cdot L)^2} \cdot R_{sh,eg}$$

Base Grid Resistance Loss (in W/segment)

$$P_{R,bg} = \frac{1}{3} \cdot J_{mp}{}^2 \cdot (L)^3 \cdot \frac{w_{bg}}{(w_{bg} \cdot L)^2} \cdot R_{sh,bg}$$

Isolation Trench Shading Loss (in W/segment)

$$P_{S,i} = J_{mp} \cdot V_{mp} \cdot W \cdot l_i$$

Emitter Grid Shading Loss (in W/segment)

$$P_{S,eg} = J_{mp} \cdot V_{mp} \cdot L \cdot w_{ceg}$$

Base Grid and Via Shading Loss (in W/segment)

$$P_{S,bg} = J_{mp} \cdot V_{mp} \cdot L \cdot w_p$$

Total Device Power (in W)

$$P = \left(J_{mp} \cdot V_{mp} \cdot L \cdot W - \sum P_R - \sum P_S\right) \cdot (\#\_of\_segments)$$

Key Variables not Defined by Figure 10

J_{mp}, V_{mp}	Max. Power current and voltage
$R_{sh,e}$, $R_{sh,b}$, $R_{sh,eg}$, $R_{sh,bg}$	Sheet resistivity of emitter, base, emitter grids and base grids
w_{eg}, w_{bg}	Width of grid: emitter and base

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13. ABSTRACT *(Maximum 200 words)*

AstroPower is developing a module-manufacturing technology based on a film-silicon technology. AstroPower, as a Technology Partner in the Thin-Film PV Partnership, is employing its Silicon-Film™ technology to develop an advanced thin-silicon-based product. This module will combine the design and process features of the most advanced thin-silicon solar cells with light-trapping. These cells will be integrated into a low-cost interconnected array. During the second year of the 3-year project, AstroPower's emphasis was on developing key submodule fabrication processes. Key results of the work include developing a new thin-film growth concept process based on attaching the low-cost substrate to the thin silicon layer after film growth; developing a new technique to achieve light-trapping in thin layers of silicon based on pigmented high-temperature glass materials; and developing key submodule fabrication processes, including contact grid design, subelement isolation, and screen-printed interconnection.

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