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Advanced Processing of CdTe- and $CuIn_xGa_{1-x}Se_2$- Based Solar Cells

Phase I Annual Subcontract Report, 18 April 1995 - 17 April 1996

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Introduction

The main objective of this project is to develop high efficiency CdTe solar cells based on processing conditions that are favorable for manufacturing purposes. This objective stems from the fact that while nearly 16% efficiencies have been achieved for laboratory devices, these were fabricated using processes that have certain disadvantages for a manufacturing environment; for example the use of borosilicate glass substrates, high processing temperatures, and chemical bath processes.

The first major issue being addressed is the use of soda lime glass substrates in place of the borosilicate glass often used for laboratory devices. In order to use soda lime (SL) glass substrates the CdTe deposition process - close spaced sublimation (CSS) - must be optimized at low substrate deposition temperatures. The high efficiencies achieved with CSS have been partly attributed to improved junction properties as a result of the high processing temperatures (about 600°); however, this was possible due to the fact that the borosilicate glass substrates used for solar cell fabrication can withstand these high temperatures. It would be desirable to lower the deposition temperatures in order to utilize soda lime glass substrates. During the late stages of the previous project, the optimization of the cell fabrication procedure - mainly the CdTe deposition process which is the only high temperature process - lead to CdTe solar cell efficiencies of 13.5%; these cells were fabricated on soda lime glass and met the low temperature deposition conditions (<550°C). The efficiency was further advanced to 13.9% (during this phase of the project). These results were achieved on two different types of soda lime glass substrates. In both cases the devices exhibited state of the art V_{OC}'s and ff's. The current densities were about 10% below what was obtained previously on borosilicate glass, primarily due to the differences in the optical properties of the glass. Since then, emphasis has been placed on achieving higher J_{SC}'s. The approach has been to gradually decrease the thickness of the CdS in order to collect more of the nearly 7 mA/cm^2 current available for energies higher than the bandgap of CdS. This has also been the main theme of one of the CdTe Thin Film Partnership teams.

Another task is to consider/evaluate alternative window layers/TCO's that could replace CdS. Since the junction properties of CdTe cells is believed to be beneficially influenced by the alloying between the CdTe and CdS at the metallurgical junction, this task appears to be the most challenging and difficult to accomplish.

This report presents results on work performed on the above issues during the first phase of this project. Emphasis is placed on processing and how it affects device performance. While the objective is to optimize processing in order to meet the manufacturing constraints, work has not been limited within these processing requirements. For example, one of the tasks is to optimize/fabricate CdTe cells by keeping all processing temperatures below 550°C; even though the majority of the devices are fabricated to meet this condition, temperatures as high as 620°C are frequently used to help understand better the effect of processing parameters.

Cell Fabrication Procedures:

The CdTe solar cell structures are of the commonly used superstrate configuration. The variations in device parameters and structures are given below:

The processes used for the deposition of the semiconductor layers are:

Process	Material
CBD, CSS, and rf sputtering:	CdS
CSS:	CdTe
rf sputtering:	ZnO
CSS:	ZnSe

The main process/device variations are in the following areas:

CdTe deposition temperature:	450-630 °C;
CdS thickness;	600 - 2500 Å (depending on deposition process);
CdS deposition process:	CSS, CBD, rf-sputtering;
Glass substrates:	borosilicate and soda lime (SL) glass.

More details on the complete device fabrication procedures can be found elsewhere[1]. Devices fabricated on soda lime glass substrates are prepared using CBD CdS films of various thicknesses, and a wide range of CdTe deposition temperatures. All other devices fabricated to study the potential of CSS CdS, ZnSe, and ZnO, are fabricated on borosilicate glass substrates.

The other major processing steps after the deposition of CdTe, annealing in the presence of $CdCl_2$ and the contacting process, are only varied/optimized when these are believed to have been influenced by changes in other processing areas. For example, while attempting to lower the CdTe deposition temperature, it was found that the grain structure of these films underwent a dramatic change[1]. At that time, the contacting procedure - in particular the chemical treatment of the CdTe surface - was revisited and re-optimized in order to ensure that the treatment was still effective and was not leading to the formation of shunting paths by etching along the grain boundaries. The post deposition heat treatment ($CdCl_2$) was also revisited, when film peeling occurred during the early stages of SL glass substrate evaluation.

CdTe Cells on Low Cost Substrates

Up until the early stages of this project a number of inexpensive glass substrates were being considered. These were typically processed using two processing schemes:

(I) a low temperature (LT) process, optimized using borosilicate glass substrates, and

(II) a high temperature (HT) process which is almost identical to the one that produced devices with efficiencies over 15%.

The low/high temperatures mentioned above refer to the CSS CdTe deposition, which is the only deposition process in our cell fabrication scheme, for which temperatures exceed 500°C. The most suitable type of substrate was found to be the type used by the CdTe industry, and is

manufactured by Libbey Owens Ford (LOF). Other types of glass presented problems ranging from poor film adhesion, to glass cracking and breaking. In some cases the deposition of SnO_2 depended on the side of the glass on which the SnO_2 layer was deposited; this was apparently due to the fact that one of the two glass sides was rich in tin. Although they showed signs of softening when heated at temperatures of 600 °C or higher, the LOF substrates were by far superior and the least problematic. The TO coated LOF glass is available in several thicknesses and sheet resistivities (R_{SH}); 3 mm/20 Ω/□, and 3 mm/15 Ω/□ are the two types of LOF glass used for this work.

The 20 Ω/□ substrates are typically coated with a layer of doped SnO_2, to reduce R_{SH} to 10 Ω/□ or less, and a layer of undoped SnO_2 layer. The 10 Ω/□ substrates are only coated with an undoped SnO_2 layer. The CBD CdS layer is deposited to the desired thickness by timing the process based on calibration runs. Cadmium Telluride is deposited over a range of deposition conditions that cover the temperature range of 460-620 °C, that have been previously optimized to yield high V_{OC}'s.

As reported previously, solar cells prepared on inexpensive glass substrates have yielded V_{OC}'s and ff's similar to those obtained with borosilicate glass substrates. The main drawback of the soda lime glass substrates remains their poor transmission, which is up to 10% lower, depending on the thickness of the glass and the properties of the SnO_2 layer. The highest J_{SC} for CdTe cells reported to date was 26.21 mA/cm^2, while the highest efficiency cells had a J_{SC} of 25.0 mA/cm^2[2,3]. The most obvious solution to further increase J_{SC}, is the use of thinner CdS films. However, accomplishing this task is a major challenge. The difficulty associated with this approach is that both the ff and V_{OC} decrease with decreasing CdS thickness; this problem becomes severe for thicknesses below 800-1000 Å. The most accepted explanation for the poor performance of CdTe/CdS cells fabricated using thin CdS films is based on the properties of the CdTe/SnO_2 junction, which is inferior to CdTe/CdS; the deposition of CdTe on "thin" CdS may lead to the CdTe coming in direct contact with SnO_2, possibly due to the presence of pinholes in CdS, leading to the formation of CdTe/SnO_2 junctions which "shunt" the CdTe/CdS. Although pinholes present a problem, the characteristics of certain devices suggest that this may not necessarily be the only important issue.

The approach taken in order to study and improve CdTe cells prepared on soda lime glass has been rather simple. A set of "local optimum" processing conditions in the low (450-560 °C) and high (>560 °C) temperature regimes, has been established. Devices are typically being fabricated by varying the CdS thickness and the processing temperatures. Although, the objective is to use the lowest temperature possible, which is required in order to avoid problems associated with the soda lime glass, the CdTe deposition temperature has been found to influence among other things the junction properties, and therefore SL CdTe cells are processed routinely at both low and high temperatures. This is similar to the approach taken for the work regarding the CSS CdS films to be discussed later.

Processing Temperatures - CdS Thickness

As already mentioned above, the CdS thickness has been found to be critical to device performance. The CdS thickness (of the CBD CdS films) is controlled by varying the deposition time. The process is frequently calibrated but nevertheless, the film thickness has been found to be within ±50-70 Å of the expected value. For this reason, instead of using the estimated thickness of the as-deposited CdS, the SR of cells at 450 nm is used as a "measure" of the CdS thickness. It should be noted that the SR in this region (400-500 nm) could be influenced by other factors; but in general it has been found to be a good indicator of the CdS thickness, in particular when this is reduced during the fabrication process. Figure 1 shows the typical behavior of the ff and V_{OC} as a function of the CdS thickness. This figure has appeared in a previous report[1] with the single difference being the new point (circled) that corresponds to the 13.9% device; this is the best device fabricated to date (during this phase of the project) using soda lime glass substrates. The improvement in performance was solely due to an increase in J_{SC} of about 0.6 mA/cm^2.

The following two sections discuss several sets of CdTe cells fabricated using

(a) a constant CdS thickness (about 800-900 Å), and

(b) a range of CdS thicknesses (600-800 Å).

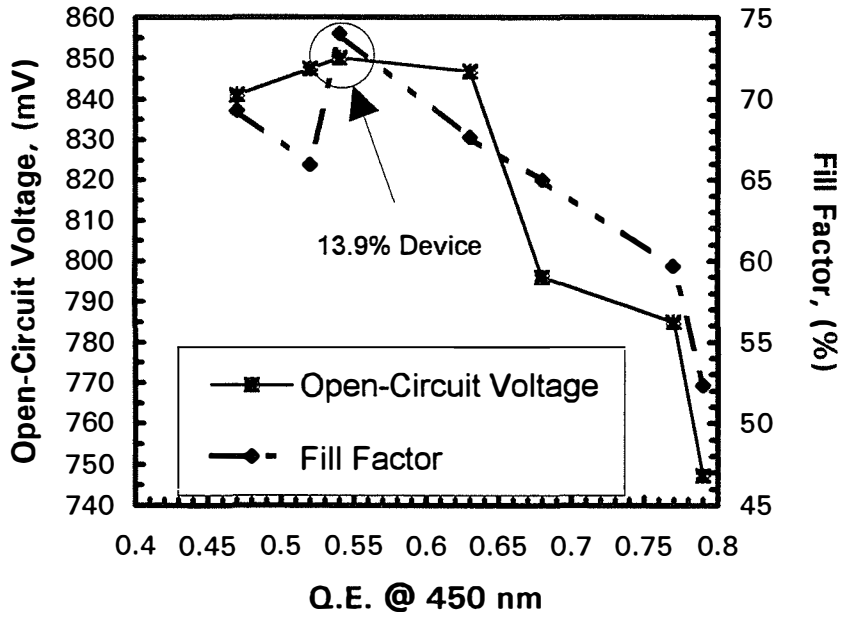


Figure 1. The Open-Circuit Voltage and Fill Factor as a function of the QE @ 450 nm.

Constant CdS Thickness

Our baseline CBD CdS deposition process can accommodate a maximum of four substrates. Devices discussed in this section have been fabricated using CdS films from the same run to

ensure minimum CdS thickness variation among the cells under consideration. Figure 2 shows the SR of a set of four samples prepared on soda lime glass substrates. Although all four samples were prepared using CdS of the same (starting) thickness, the SR in the 400-500 nm region suggests that the thickness for two of these films is slightly smaller. The formation of an interfacial CdS_xTe_{1-x} layer has been verified by many,[4-6] and therefore some thinning of the CdS films is always expected, depending on the extent of interdiffusion between the CdTe and CdS. The results of figure 2 are due to the fact that the "thin" CdS devices were fabricated using high processing temperatures that lead to the consumption of a larger portion of the CdS film. The CdS thickness for the "thick" CdS devices is what should be expected if only a very small amount of CdS had been "used up" during the fabrication process. The "expected" thickness (or blue response) is based on transmission measurements of the CdS films. This behavior is typical with very few exceptions, suggesting that the final thickness of the CdS films and the formation of the CdS_xTe_{1-x} is determined to a certain extent by the CdTe deposition temperature. The solar cell parameters for this group of cells (three cells per substrate) are listed in table I. Neglecting the variations in J_{SC} which could be associated with errors in the cell area measurements, the ff and V_{OC} appear to be insensitive to the "final" CdS; this is the thickness range where devices with high V_{OC}'s and ff's can be routinely fabricated.

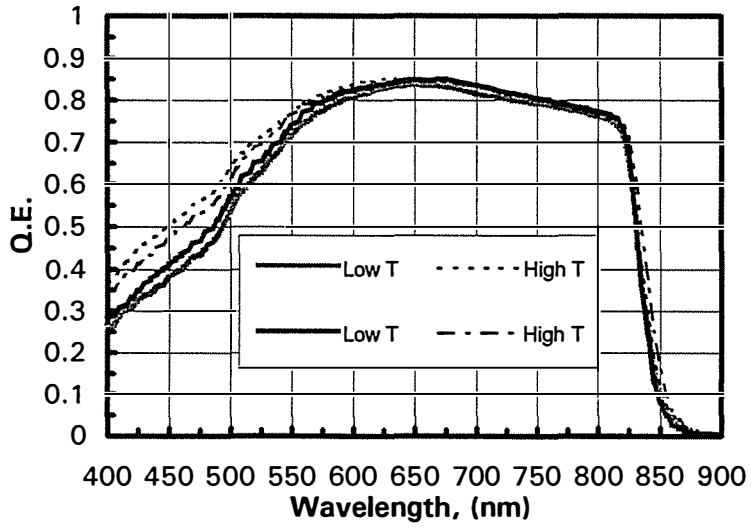


Figure 2: The SR of CdTe cells fabricated at different deposition temperatures.

Table I: The photovoltaic parameters of the cells of figure 2.

Processing Temperature	V_{OC} (mV)		FF (%)		J_{SC} (mA/cm^2)	
Low	830	839	71	71	20.6	19.0
Low	832	841	71	74	20.8	20.3
Low	833	837	71	73	20.4	19.8
High	839	834	73	71	20.0	21.1
High	839	834	72	71	21.1	21
High	836	828	71	69	21.2	21

The portion of the CdS that appears to have been "used up" for the three HT devices is believed to have been distributed only near the metallurgical junction region; unlike other deposition technologies for which sulfur can be found in large amounts (2-3% and possibly higher) throughout the CdTe films affecting the bandgap of CdTe[7]. It is not clear yet as to how much sulfur and how deep into the CSS-CdTe the layer this element can be found. High temperature USF devices have been previously characterized using XRD by the group at IEC (Brian Mc Candless) as part of our TFP activities[7]. The measurements detected no S in the CdTe layer if the USF devices. As mentioned above, the diffusion of sulfur into the CdTe layer is often associated with a shift in the long wavelength response of CdTe cells. A closer examination of the long wavelength region for the devices of figure 2 reveals, that the two HT devices exhibit a slight shift of about 5 nm towards longer wavelengths; this is shown in figure 3. Based on the limited information from the IEC XRD measurements, it is assumed that the amount of S (if any) present in the HT CdTe films is very small, and not enough to cause a bandgap change.

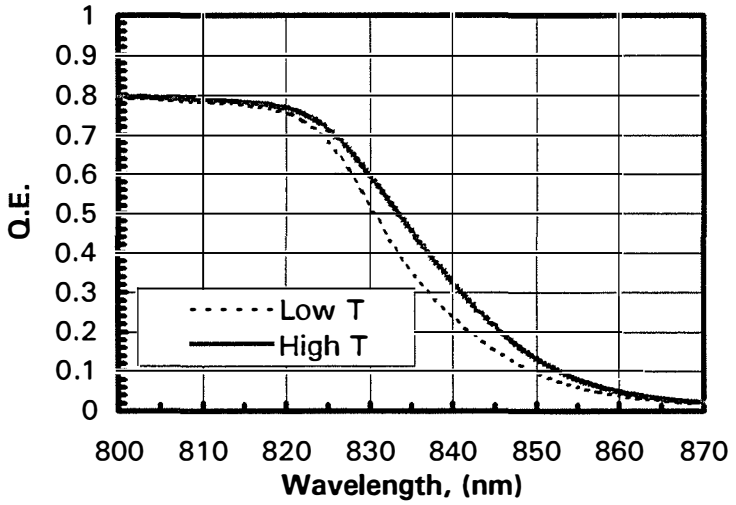


Figure 3: The 800-850 nm region of the SR of two of the devices of figure 2.

The net acceptor concentration for these devices was calculated from C-V measurements. The low temperature devices exhibited a constant carrier concentration of 10^{14} cm^{-3} while the HT device exhibited an increase in carrier concentration with reverse bias from about 5 x 10^{13} to 3 x 10^{14} cm^{-3}. The gradual increase could be attributed to either diffusion of the back contact dopants into the CdTe, or a small S amount into the CdTe that the XRD could not detect. Based on the carrier concentration and XRD measurements, it appears that the small shift in the long wavelength response of the cells could be due to "improved" collection in the HT devices. Modeling of the SR response in this region, indicated that small shifts such as the one shown in figure 3, could be due to small variations in the depletion width. To verify this, the SR of one such device was measured at zero and 1 volt reverse bias and is shown in figure 4. This shift is very small and any increase in J_{SC} would be insignificant, but the issue of S diffusion in CdTe beyond the metallurgical junction region and to what extend this influences the material properties and cell performance may be important. Recent DLTS measurements indicated that certain traps

in CdTe are only present near the front of the device (they could not be found near the back contact end of the device.) These results are very preliminary and due to the complexity of the samples and the measurement itself they must be verified prior to drawing any conclusions.

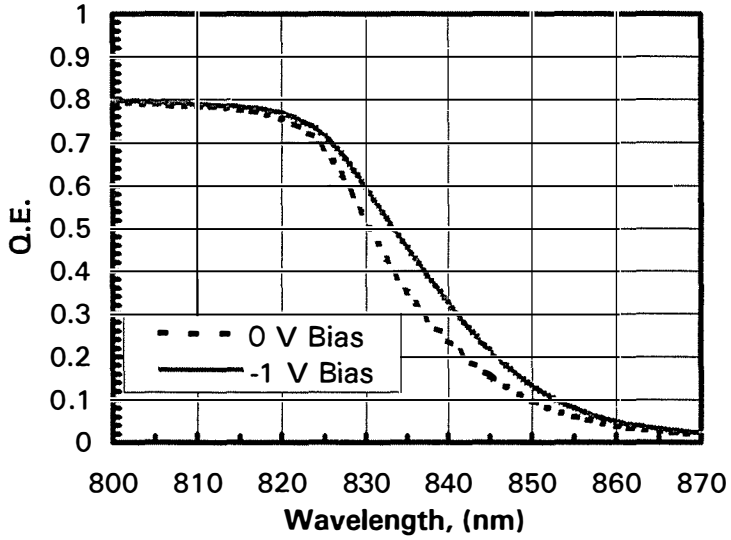


Figure 4. The SR near the CdTe absorption edge for zero and 1 volt reverse bias.

Varying CdS Thickness

Several sets of cells were prepared using processing conditions similar to the ones used for the set described in the previous section; the main difference is that the thickness of the CdS was intentionally varied to cover a range of thicknesses similar to those represented figure 1. The SR for this group of cells is shown in figures 5 and 6. Figure 5 shows the SR for devices that have been processed at low temperatures. The variation (decrease) in thickness is apparent from the blue response of the cells which shows the expected increase. The devices in figure 6 have been processed at high temperatures. As was the case with the previous set of cells, the CdS appears to have "thinned" considerably. In fact, the response for two of those devices suggests that there is no CdS left. Since the starting thickness of the CdS is different for these two cells, this implies that the ternary CdS_xTe_{1-x} compound may be different for the two devices with regards to thickness and/or composition. Table II shows the effect of the processing temperature and the CdS thickness on V_{OC}, ff, and R_{SH} for this set of cells . The open-circuit voltage for the LT cells remains essentially unchanged , while the ff shows a gradual increase as the CdS thickness increases. The HT cells show an increase in both the ff and V_{OC} as the CdS thickness increases. The thicknesses shown on these two figures are those expected from timing the CBD process and as mentioned above they could be within ± 50-70Å.

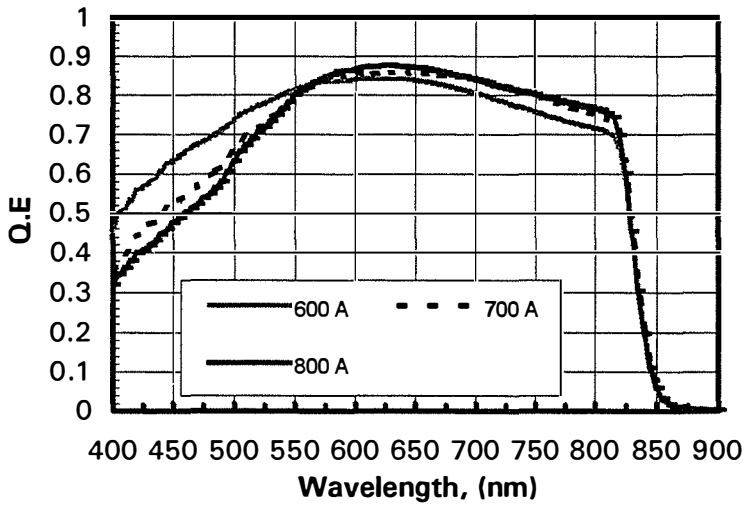


Figure 5: The SR of devices prepared with CdS of three different thicknesses and processed at low temperatures.

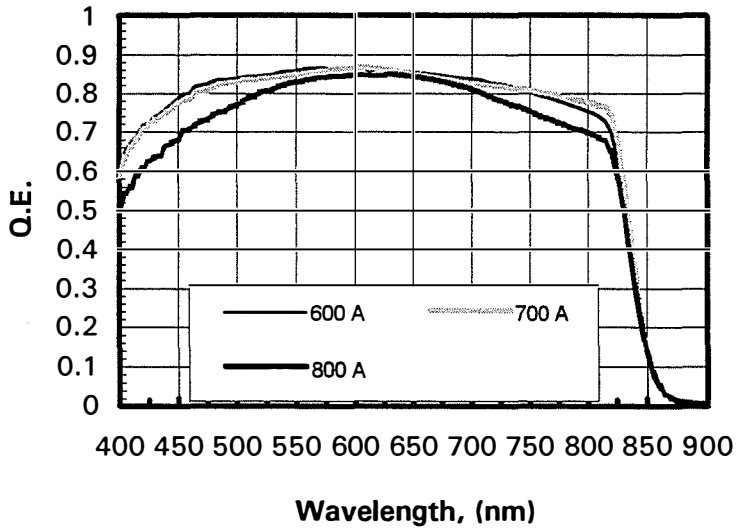


Figure 6. The SR of devices prepared with CdS of three different thicknesses and processed at high temperatures.

Table II: Solar cell parameters for the devices of figures 5 and 6.

Processing Temperature	CdS Thickness(Å)	V_{OC} (mV)	FF (%)	R_{SH} (Ω-cm^2)
Low	600	848	66.52	665
Low	700	846	67.66	1040
Low	800	841	68.96	800
High	600	756	52.62	500
High	700	791	60.86	800
High	800	802	65.74	650

Both ff and V_{OC} trends are considered to be "typical" behavior. However, as indicated above, the SR of the HT devices suggests that the "final" CdS thickness for two of these devices is essentially the same (the third device is also very similar). This result is very interesting in that it suggests that although the apparent final CdS thickness may be the same, the starting thickness of these films is critical in achieving improved performance. The ff and V_{OC} of the HT device fabricated with the 800 Å CdS film improved by 5% and 10 mV respectively, over the 700 Å device, while the SR of the two suggests that J_{SC} is essentially the same. These results verify once more the importance of the CdS_xTe_{1-x} layer, but also suggest that the composition and/or thickness of this layer must be closely studied. Careful alloying of the CdTe and CdS near this critical device region could lead to the desired high V_{OC}'s and ff's for "small" CdS thicknesses.

Based on the above results, a set of cells was fabricated with the objective to use different starting thicknesses but end up with the same blue response (final CdS thickness). This task was not easily achieved suggesting that additional work in this area is needed. Another possibility for the difficulty in reproducing these results is that the CdTe deposition temperature may not be the dominant processing variable that affect the interdiffusion and therefore the $CdCl_2$ heat treatment should also be considered. The SR of two such devices is shown in figure 7. The cells were prepared using different starting CdS thicknesses but were processed under low and high temperature conditions. The device parameters for the two cells are shown in table III. The LT cell exhibits a higher V_{OC} which can be partly explained by the lower J_O. Devices such as the LT device (V_{OC}=846 mV; thin CdS) are not easily reproducible; nevertheless these data suggests that high V_{OC}'s and thin CdS can coexist; the next step is to improve the ff of these devices.

Table III. Solar cell parameters for the devices shown in figure 7.

	Low T	High T
V_{OC}, (mV)	846	795
J_{SC}, (mA/cm^2)	21.4	21.7
FF, (%)	65.4	65.2
η	11.84	11.25
A	1.65	1.62
J_O, (A/cm^2)	6.2×10^{-11}	1.0×10^{-10}

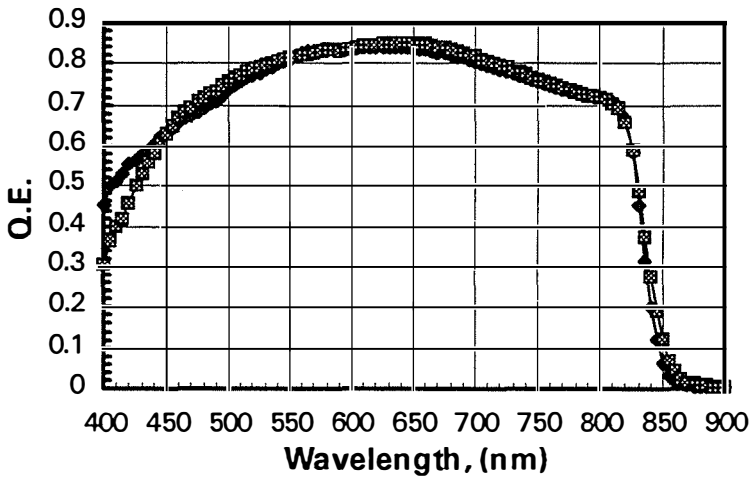


Figure7. The SR of devices prepared with CdS films of different starting thicknesses.

Device Parameters

The dark Ln I-V characteristics for several devices fabricated under low and high temperature conditions for several CdS thicknesses are shown in figures 8, 9, and 10. These represent what is considered "typical" behavior for HT and LT devices. The HT devices exhibit a considerable amount of shunting as indicated by the low voltage section of the I-V, as well as higher J_O. The shunt resistance under one sun conditions (calculated form the slope of the I-V at zero bias) has a great impact on the ff, especially when it drops below about 1000 Ω-cm^2. Figure 11 shows the shunt resistance as a function of the CdS thickness for about 50 high and low temperature devices. Considerable scattering is evident in both cases (this may be due to the fact that the CdS thickness is based on the value estimated from the deposition conditions), but it is clear that for LT cells R_{SH} is above 1000 Ω-cm^2, and for the HT it is below this value. The same figure shows the effect of R_{SH} on the ff. The ff is essentially unchanged, 70$^+$% for R_{SH} values above 1000 Ω-cm^2, but decreases drastically for R_{SH} values below 1000.

Extrapolating device parameters such as A and J_O from the I-V data is often hindered by excessive shunting and or high series resistance. Assuming a constant A and J_O these parameters were measured for the devices shown in figures 8-10; these are the best estimates depending on the extent of the linear portion of the I-V characteristics. A was about 1.6-1.65 for both the low and high temperature devices. J_O was lower for the low temperature devices 2-6 x 10^{-11} A/cm^2; J_O for the HT devices was in the 2-7 x 10^{-10} A/cm^2 range.

Figure 8. Dark I-V for devices prepared at high and low temperatures;
CdS thickness=600 Å

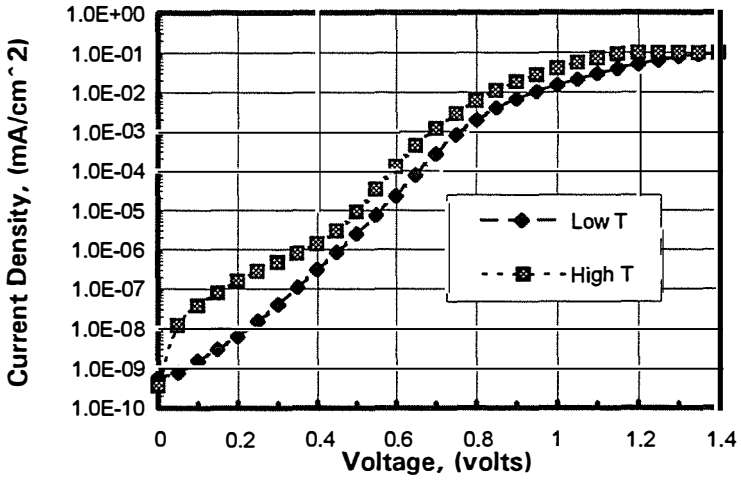


Figure 9. Dark I-V for devices prepared at high and low temperatures;
CdS thickness=700 Å

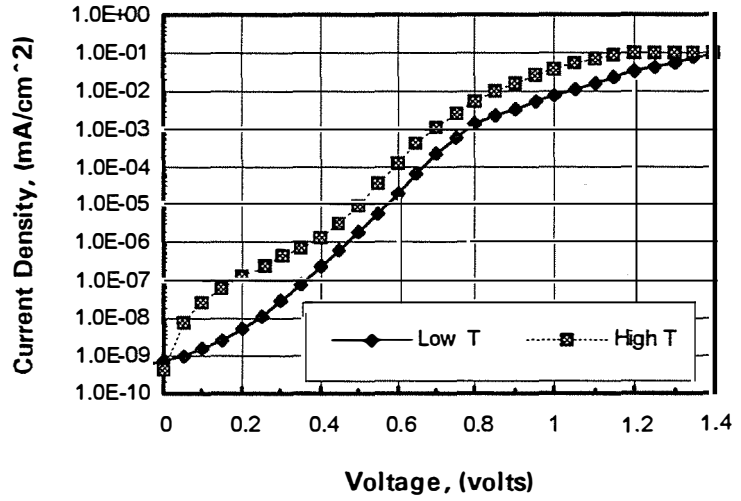
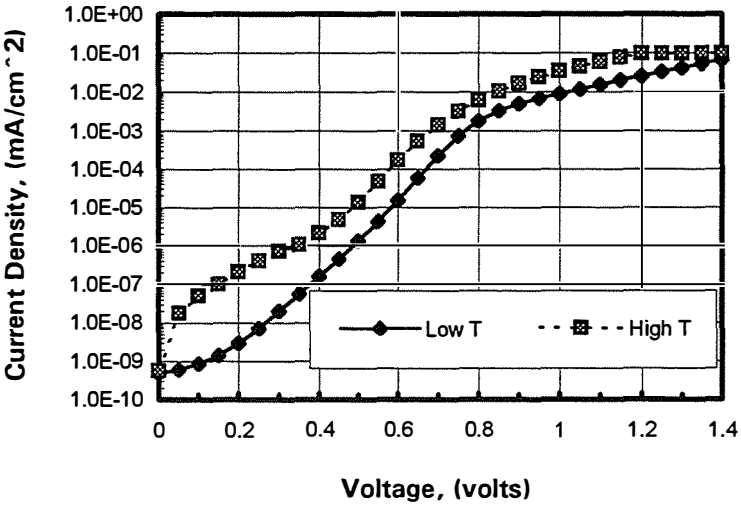


Figure 10. Dark I-V for devices prepared at high and low temperatures;
CdS thickness=800 Å



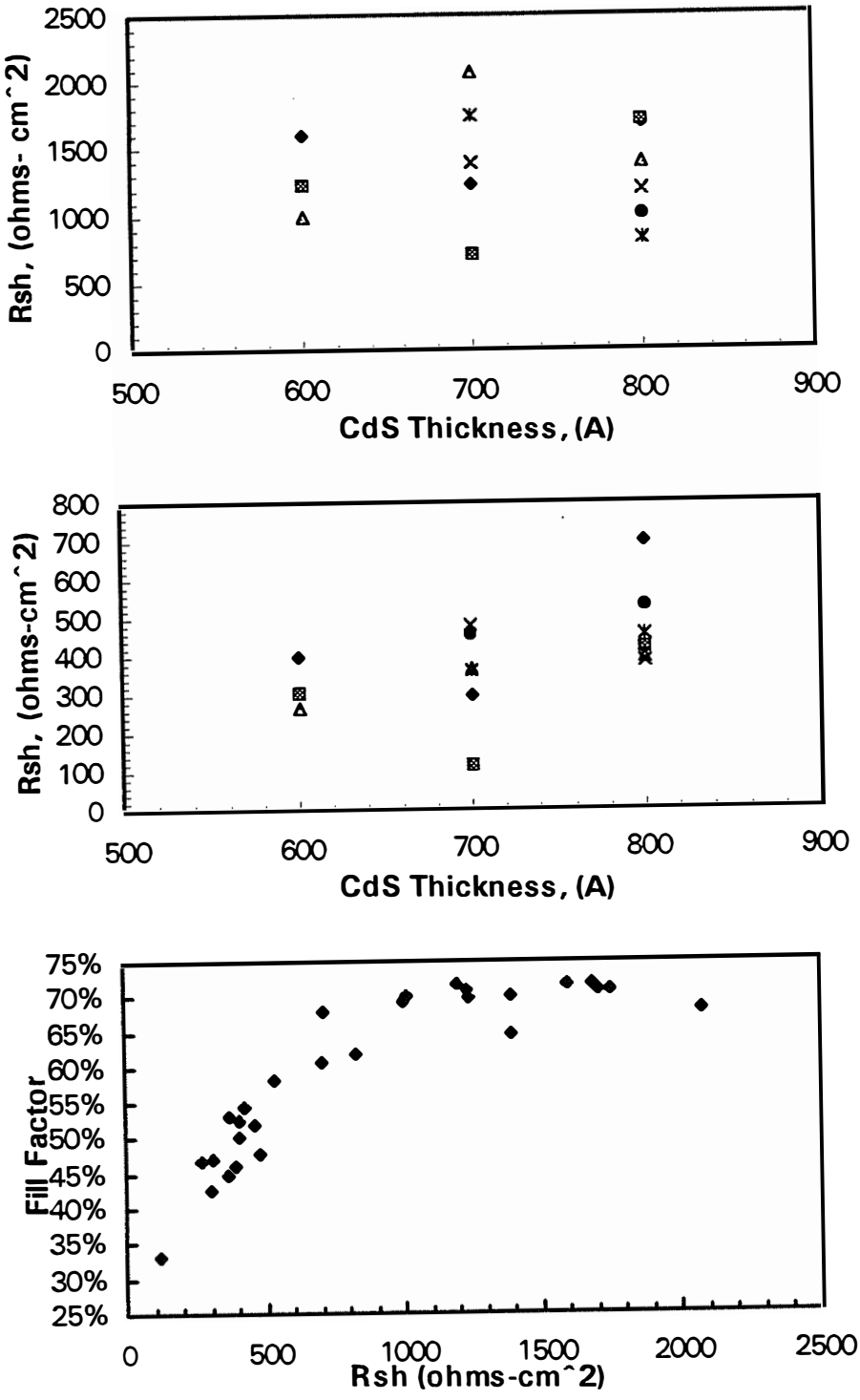


Figure 11: **Top:** R_{SH} vs CdS thickness; LT cells

Middle: R_{SH} vs CdS thickness; HT cells

Bottom: FF vs R_{SH}

CSS Cadmium Sulfide

Among the CdS deposition technologies, CBD appears to be a popular technique for laboratory devices. It is simple, inexpensive, and most importantly it is capable of producing pinhole free thin CdS films. Nevertheless, material utilization, throughput, and the liquid waste produced by this process, are issues that limit its potential as a possible candidate for manufacturing. Therefore the close spaced sublimation process was chosen as an alternative technology for the deposition of the CdS layer.

The main objective is to develop device quality CSS CdS films in order to achieve high cell efficiencies - at the same levels and beyond of what was previously achieved with CBD CdS. The approach taken was to evaluate/optimize the process with emphasis placed on depositing continuous thin (600-800 Å) films in order to maximize J_{SC}. Although the eventual goal is to utilize these films with low cost substrates, most of the work is being carried out on borosilicate glass substrates. Work with soda lime substrates is already underway but all results presented in the following sections are for CSS CdS films prepared on borosilicate substrates.

The following sections discuss the effect of two process parameters on film properties and device performance : (a) the deposition temperature/profile and (b) ambient.

Deposition Temperature:

The cell efficiencies achieved with CBD CdS are partly due to the small grain size of these films that is small enough to allow the deposition of pinhole free "thin" CdS films. Early work on CSS CdS films indicated that the grain size could be varied over a rather wide range (few tenths of a μm up to 2 μm) depending on the deposition parameters. The grain size of CSS CdS films depends, among others on the surface properties of the substrate, the reactor pressure, the ambient, and the substrate temperature. At the early stages of this work the grain size of CdS was varied by adjusting the total reactor pressure. The improvement in the pinhole density resulted in some improvement in device performance (in particular V_{OC}), but V_{OC}'s were limited; the typical V_{OC}'s were in the 700-800 mV range. Since, the "pinhole" issue is often thought to be the main limiting factor it was deemed necessary to further study the effect of other process parameters (in addition to the total reactor pressure.)

It has been previously found that temperature profiling could greatly influence the grain size and orientation of CSS CdTe films[8]. Figures 12 and 13 show two of the most commonly used/studied profiles for this work. For the profile shown in figure 12 the substrate and source are heated at the same rate and held at the same temperature for a few minutes; after this pre-heating period the source temperature is raised to a higher temperature to initialize the growth. For the profile shown in figure 13 the source and substrate are also heated at the same rate but the substrate is heated to a higher preheating temperature; the growth is initialized by lowering the substrate temperature while raising the source temperature. Representative films obtained from these two profiles are shown below each profile in figure 14.

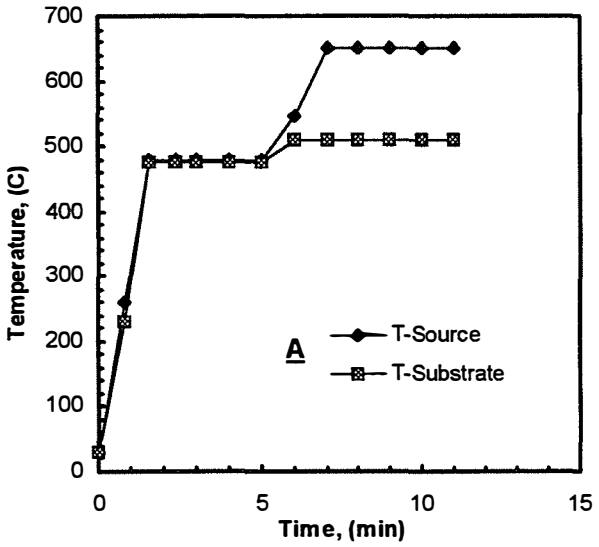


Figure 12. Temperature profile A.

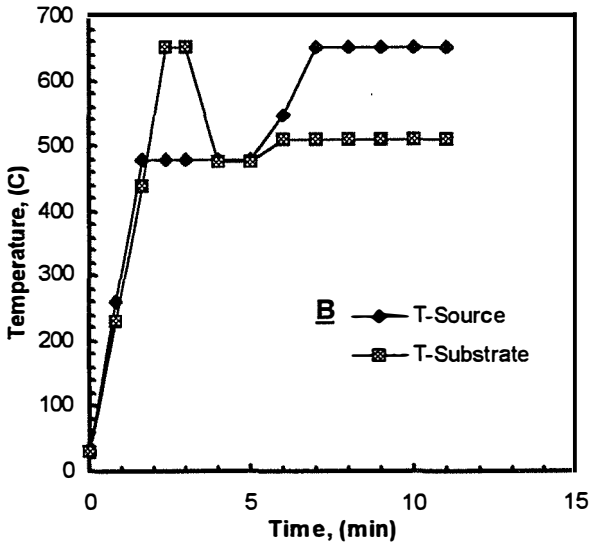


Figure 13. Temperature profile B.

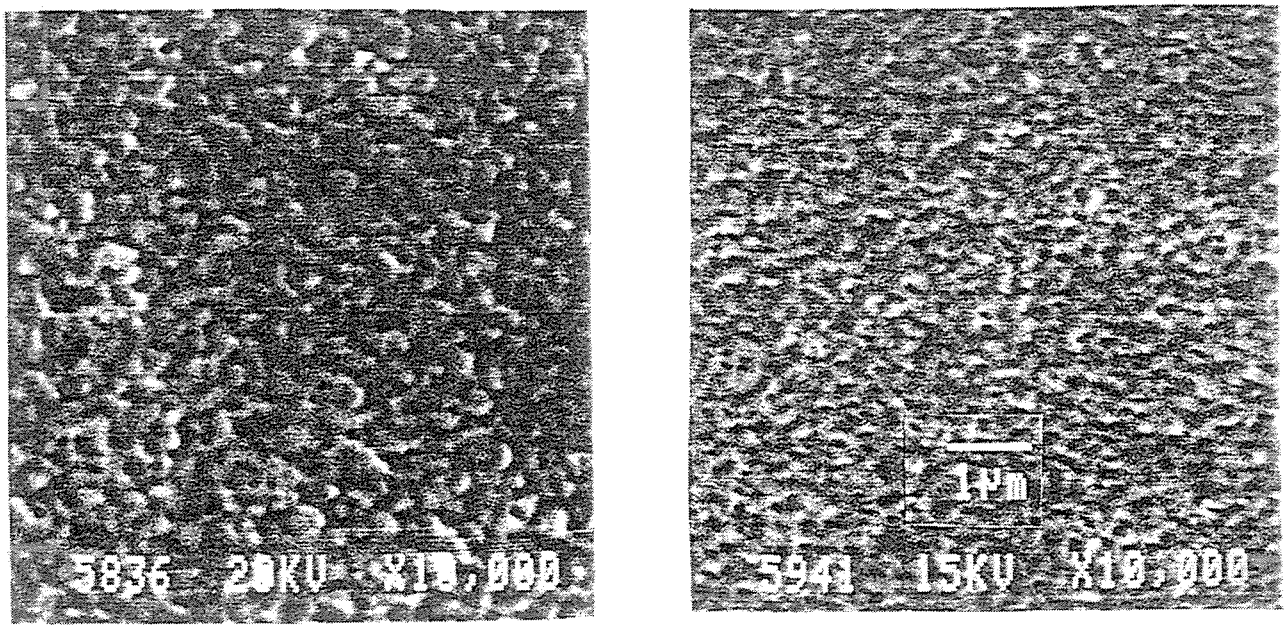


Figure 14. SEM micrographs for the two profiles of figures 12 and 13.

The film that corresponds to profile A consists of relatively larger grains and has a rather high pinhole density. However, the profile B film seems denser and has a much lower pinhole density. Solar cells fabricated with profile B CdS films have consistently exhibited higher V_{OC}'s, once again underlining the negative impact of pinholes in CdS

The Effect of Oxygen:

Oxygen is known to behave as an acceptor in several II-VI semiconductors (CdTe, CdS, ZnS, ZnSe etc.). The deposition of CSS CdS in O_2 ambient was originally considered based on previous work that suggested that its presence during the deposition process enhances solar cell performance[9]. The addition of a small amount of O_2 was found to have a profound effect on the grain size/structure of the films and the deposition rate. This effect is shown in figure 15 where. Both films shown were deposited using similar deposition rates. The film deposited in the presence of O_2 (left) exhibits a much smaller grain size than the film grown without O_2 (right) and most importantly appears to be completely free of pinholes.

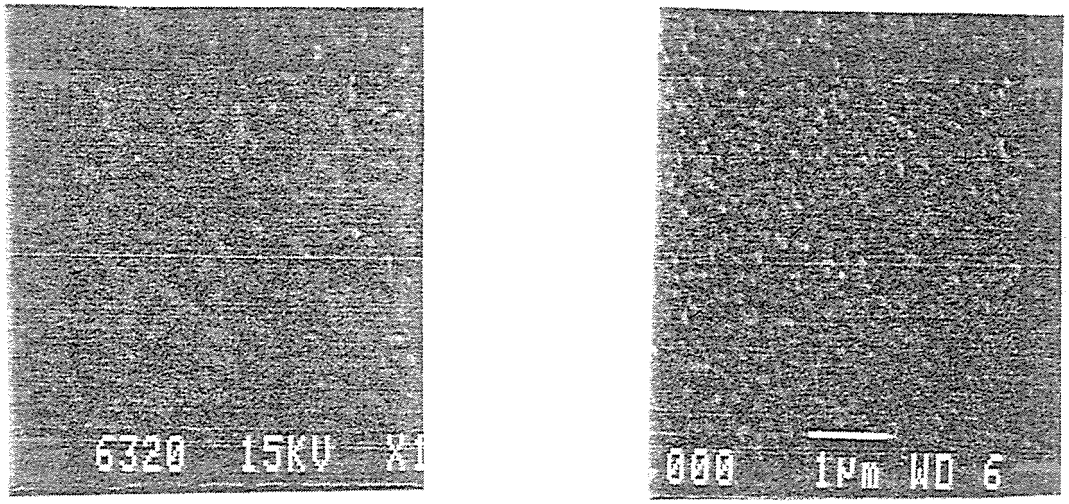


Figure 15. SEM micrographs of films deposited with (left) and w/o (right) O_2.

A set of CdS films prepared under varying concentrations of O_2 has recently been studied by XRD; the analysis was performed by Brian McCandless of IEC. The measurements revealed that a second phase identified as CdO is present. This was found only in films that were grown in ambient with high O_2 concentrations. The incorporation of O_2 in CSS CdS has also been verified by photoluminescence (PL) measurements[10]. Additional PL results will be presented in a later section.

CdS Thickness - Oxygen Ambient:

The effect of O_2 on solar cell performance was rather dramatic. The effect of the CSS-CdS thickness on device characteristics was not surprising since it followed the expected trends but it revealed the importance of O_2. Controlling the thickness of CSS CdS is somewhat more difficult than it is when the CBD process is used and therefore the Q.E. @ 450 nm is again used as a measure of the CdS thickness. The O_2 and thickness effects are shown in figures 16 and 17; note that the x-axis is the quantity (1 - Q.E. @ 450) nm. Cells fabricated using CdS films prepared without O_2 exhibit somewhat similar behavior as that depicted earlier in figure 1. However, it should be noted that for the same thicknesses V_{OC} is lower in this case, and the maximum value obtained is about 780 mV; 800 mV is the maximum V_{OC} obtained for CdS grown w/o O_2. The same is true for the ff; the overall trend is similar, but the highest values obtained are lower than those in figure 1. For cells fabricated with CdS deposited in the presence of O_2, V_{OC} has reached values of 840-860 mV and ff's of 72-75% have been obtained (both quantities are as high as those obtained form CBD CdS). However, the decrease in the ff and eventually V_{OC} begins at larger thicknesses than it does for the CBD CdS. The efficiencies of the devices shown in figure 16 are in the 10-11% range, while the efficiencies for the cells of figure 17 are over 13.5%.

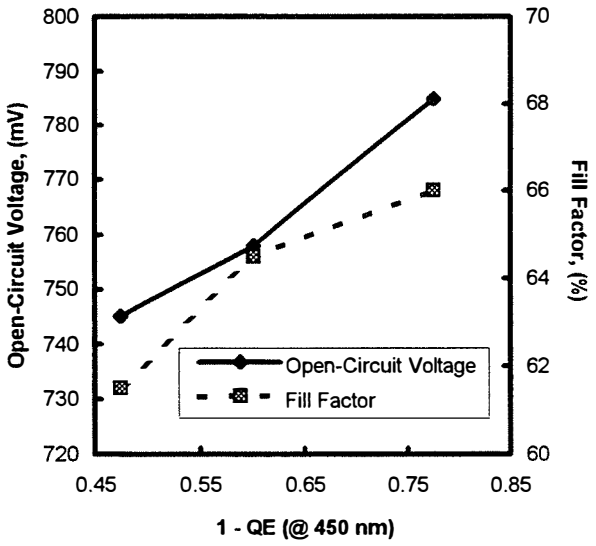


Figure 16. V_{oc} and ff vs (1-QE @450) for CdS films grown in He.

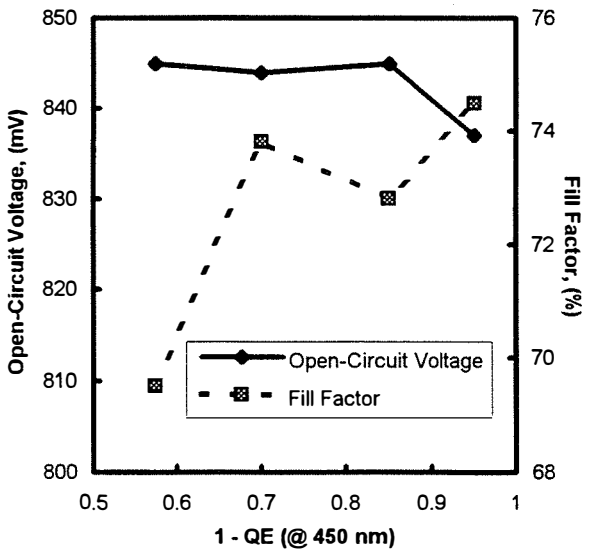


Figure 17. V_{oc} and ff vs (1-QE @450) for CdS films grown in O_2.

The current data implies that additional optimization and improvements in the quality of the CSS CdS films is necessary prior to reaching higher J_{SC}'s without losses in the ff and V_{OC}. The best device fabricated to date using CSS for the deposition of both the CdS and CdTe layer exhibited a 14.2% efficiency (V_{OC}=853 mV, J_{SC}=21.7 mA/cm^2, ff=76.5%). The low current is due to reasons discussed earlier (i.e. the thickness of CSS CdS films). The ff obtained for this device is the highest yet obtained for any CdTe cell fabricated in our lab, suggesting that once the issue of J_{SC} is resolved these devices should reach at least the same efficiency levels obtained with CBD CdS.

Photoluminescence Studies

The improvement in device performance realized by using CdS films grown in an O_2 ambient could not be associated only with the fact that the O_s films are pinhole free. Efforts to use thick (3000-4000 Å) CdS films grown in O_2 free ambient (these films based on their large thickness should be free of pinholes) did not result in any additional improvements. To better understand the effect of O_2 on the properties of CSS-CdS PL measurements were carried out at 4 and 77 K. Preliminary results indicated that the spectrum of CdS:O_2 films included an oxygen related transition not present in O_2 free films have been presented elsewhere[10]. Since then additional measurements have been performed and these results are shown in figure 18 which shows the spectra of three CdS films prepared using varying O_2 concentrations. The CdS:O_2 films contain a PL band at about 850 nm whose intensity increases with increasing O_2 concentration (the amount of O_2 during the deposition). The PL band located at about 630 nm decreases with increasing O_2 concentration. It is too early to draw any conclusions on the direct correlation of these impurity centers with device performance. It is however, suggested that the role of O_2 is not limited to obtaining pinhole free films. Understanding the role of these centers will be further complicated by the fact that the CdS films most likely undergo through more changes during the subsequent fabrication steps. Currently, the effect of annealing on the PL of CdS films is under investigation.

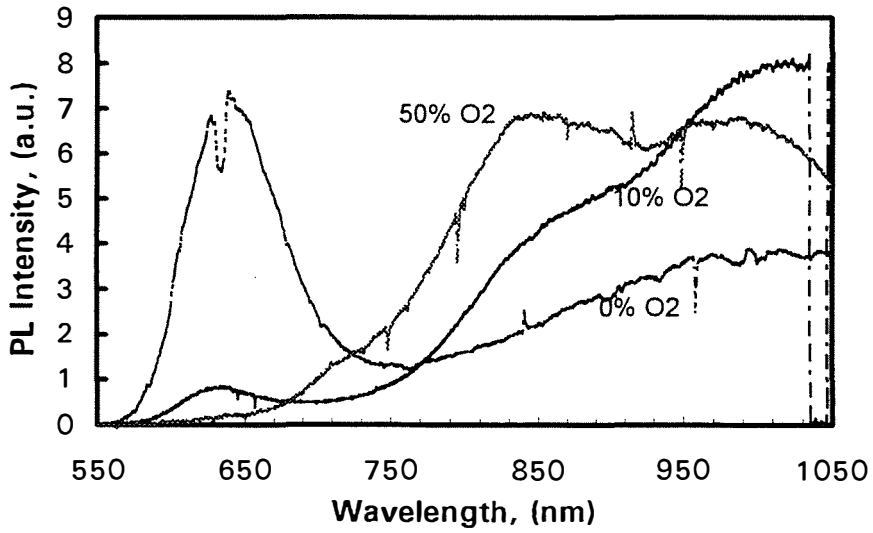


Figure 18. PL spectra for CSS-CdS films.

Window/TCO Layers

Another objective of this project is the study of alternative window materials and TCO layers. Wide bandgap semiconductors such as $Zn_xCd_{1-x}S$, ZnS, and ZnSe were chosen as possible candidates. All three materials have bandgaps greater than CdS and therefore offer the advantage that higher J_{SC}'s can be achieved. Unfortunately, discontinuities in the conduction band due to differences in electron affinities could yield high considerable barriers to electron flow[11].

However, interface alloying could lower such barriers and minimize their effect on carrier flow. Although $Zn_xCd_{1-x}S$ was considered to be the best of the three candidates, attempts to prepare this semiconductor by modifying the CBD CdS process did not succeed. Focus was then shifted to ZnS (prepared by sputtering) but CdTe/ZnS devices exhibited very poor characteristics.

Zinc selenide was thought to be the most "complex" window material due to the fact that intermixing between CdTe and ZnSe could lead to the formation of interface layers that could prove to be detrimental to device performance[12]. These devices were also prepared under low and high temperature processing conditions in order to determine whether the interdiffusion could be controlled. However, it did not appear that the processing temperature was critical since under both low and high temperature processing CdTe/ZnSe devices exhibited very poor characteristics. Spectral response measurements revealed that some devices exhibited a relatively sharp cut off at about 625 nm, suggesting the formation of another compound that absorbs light but does not contribute to the photocurent. Attempts to minimize the formation of this compound ranged from lowering all processing temperature to 450 °C to eliminating all annealing steps. Most devices exhibited V_{OC}'s in the range of 400-550 mV.

Device performance for CdTe/ZnSe cells improved after thinning the ZnSe layer considerably; this was the only way to avoid the formation of "light blocking" compounds. It appears that the thin ZnSe layer is consumed by alloying but there is not enough material to form the light absorbing compound. Figure 19 shows the SR of two CdTe/ZnSe devices. The gradually decreasing SR is that of a device prepared with thick ZnSe. After removal of the CdTe the optical transmission measurements of the interface compound (which exhibited extremely good adhesion to the SnO_2 substrate) was measured, and it was found that it follows the same trend observed in the SR. The second SR corresponds to the best CdTe/ZnSe device fabricated to date. This cell exhibited a Voc ff and J_{SC} of 726 mV, 58%, and 21.3 mA/cm^2 respectively corresponding to a 9% efficiency. Based on the behavior exhibited by CdTe/CdS devices with respect to the CdS thickness and processing temperature, a similar approach will be followed for the CdTe/ZnSe devices in an attempt to determine whether further improvements are possible.

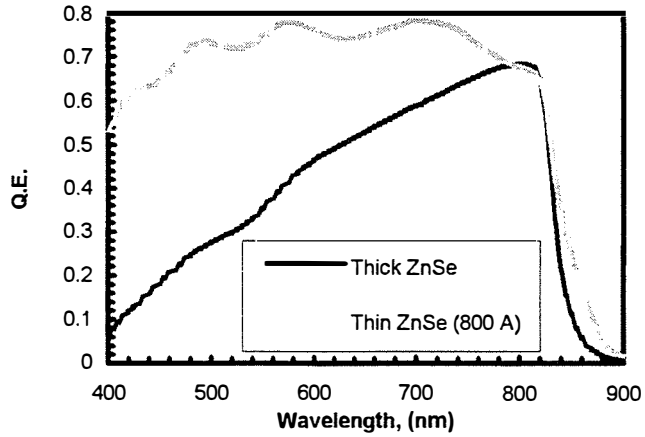


Figure 19. SR for CdTe/ZnSe devices.

Zinc oxide deposited by rf sputtering from a ceramic ZnO target is being considered as an

alternative TCO to SnO_2. ZnO/CdS/CdTe structures have been prepared using CdS films prepared by either rf sputtering or CSS; since ZnO is soluble in alkali solutions, CBD CdS could not be used. Although, V_{OC}'s in excess of 800 mV have been obtained suggesting that ZnO could be a viable TCO candidate for CdTe solar cells, all devices fabricated on ZnO/7059 glass to date have exhibited very high series resistances. This appears to be related to the ambient of the CSS CdS and/or CdTe which contains O_2. Heating of the ZnO substrates in the O_2 environment of the CSS process results in an increase in the resistivity of the films by as much as two orders of magnitude. The best CdTe/CdS cell prepared to date on ZnO coated glass exhibited V_{OC}, ff, and J_{SC} of 802 mV, 63%, and 22 mA/cm^2 respectively. In order to address the issue of the ZnO instability, annealing experiments are being carried out to determine whether this layer can be improved to withstand the processing environment of the CdS and CdTe technologies.

Thin Film Partnership Activities

The CdTe Efficiency Team has focused on the "thin" CdS issue. USF has been responsible for coordinating these activities, providing samples to the other team participants who are actively involved in this effort. All activities to date have focused on fabricating devices with certain specifications and evaluating them in order to identify differences, similarities, and limitations among the several CdTe technologies. Although the activities focused on electrical and optical studies the team is preparing to begin material studies, that will help us unravel some of the critical issues associated with the device interface. USF has provided the TO/glass substrates to be used for fabricating the cells and CSU has performed all the electrical and optical measurements. The team has decided to generate another set of cells (specified CdS thicknesses) while the devices fabricated previously are currently being used for material studies.

Conclusion

As a result of further process optimization the efficiencies of CdTe cells fabricated on soda lime glass substrates have reached the 13.9% efficiency level, while the CSS CdS films have been used for the fabrication of devices that exhibited 14.2% efficiencies; see figures 20 and 21.

The study of the effect of the processing temperatures and the CdS thickness indicated that the CdS thickness must be optimized along with the CdTe deposition temperature. It has also been demonstrated that high V_{OC}'s can be achieved for cells with thin CdS. The extend of interdiffusion at the CdTe/CdS interface is believed to be affected by a number of processing steps. In our process the dominating parameter appears to be the deposition temperature of CdTe and not the $CdCl_2$ treatment. It is also critical that the CdS thickness is such to allow the correct amount of alloying to take place at the junction depending on the deposition temperature. It seems possible to achieve high V_{OC}'s at both low and high temperatures if the "right" starting CdS thickness is used. Work in this area will continue, with emphasis placed on reducing the deposition temperatures even further, and achieve high V_{OC}'s, and ff's for "thin CdS films.

Temperature profiling during the deposition of the CSS CdS films is important in reducing the pinhole density. However, the temperature profiling alone and thick CdS films did not lead to

state-of-the-art performance. It was necessary that O_2 be added during the deposition. Photoluminescence measurements and XRD were used to identify the presence of O_2 in CdS. Incorporation of O_2 in the CdS films - although not clear yet - is believed to be critical to enhancing device performance. Further work on CSS CdS films will focus on better understanding the role of O_2, study the effects of various heat treatments on the properties of the CdS and solar cell performance, and transferring this technology to soda lime glass substrates.

Work on TCO/window layers has been difficult. This was expected based on the fact that the performance of the CdTe/CdS devices so greatly depends on the alloying between the CdTe and CdS. Unless work on the windows currently studied produces more encouraging results in the short term, alternative materials will have to be sought.

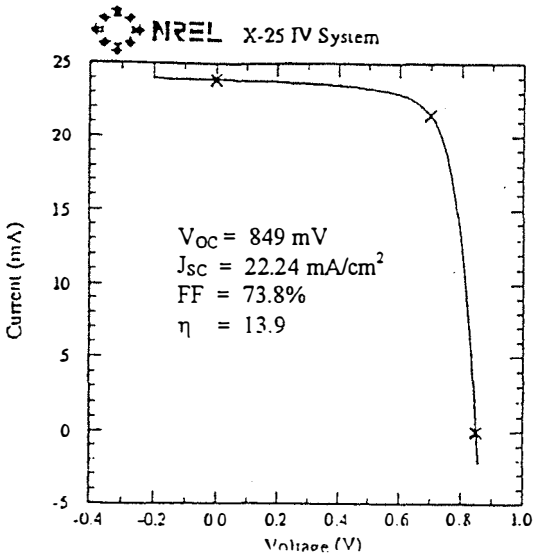


Figure 20. Light I-V of a CdTe cell fabricated on soda lime glass.

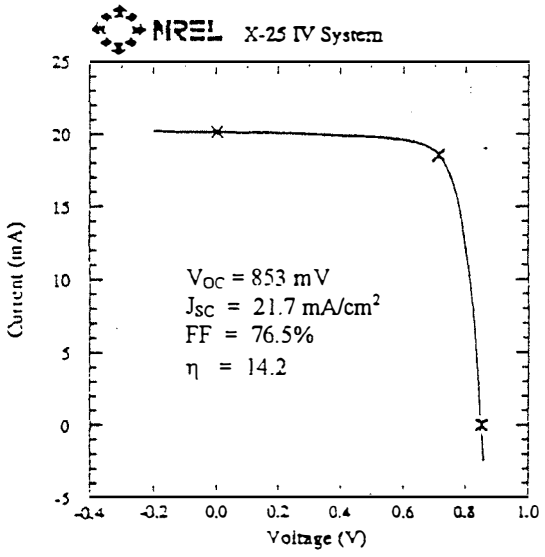


Figure 21. The light I-V of a CdTe/CSS-CdS cell.

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PART II

CIGS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

This project continues our efforts to develop a manufacturing friendly process for CIS. We have discussed our approach in detail previously(1), and an update will be provided in the next section below. The key aspects of our process is that it is all-solid-state and avoids tight control of elemental fluxes. Thus we are trying to find pathways to state-of-the-art performance that do not involve what we believe to be non-manufacturable procedures. We wish to point out, however, that much of our guidance and inspiration comes from the results achieved by these higher level processes.

In our previous efforts we did not incorporate Ga in our films, as we wanted to first understand the simpler CIS-based device. Using our simple "coat and cook" process we were able to achieve efficiencies in the 9 - 10% range which compared favorably with then state-of-the-art values of 12% for non-Ga devices. Under this project we started introducing Ga into our process. In this report we discuss the significant advancements in performance which we have achieved during the first year. We also discuss the generic understanding of semiconductor formation which we have acquired and the role of Ga in both film formation and device performance. Since this is a fully integrated project, we endeavor to connect device performance back to processing details and will report our findings accordingly.

Since it is becoming increasingly clear that semiconductor formation and junction formation are not independent steps in device fabrication, we also continue efforts to further understand and improve our junction options. We report below results on variations in CdS deposition and on novel deposition techniques for ZnO. As will be discussed, these activities contribute to the progress we are making with device performance and are necessary to fully evaluate the semiconductor. *There is no generic CIGS or generic junction formation process that can be used to properly evaluate each other at this time.*

PROCESS DESCRIPTION

The "coat and cook" process which we favor is illustrated in Fig. 1 and will be referred to as M1. This is a simple two-step process involving deposition of elemental precursors in step 1 and an anneal at near atmospheric pressure in step 2. The advantages of this process are apparent and have been discussed previously(1). Our best non-Ga devices(9 - 10%) have been made with this process.

In Fig. 2 is shown process M2 which involves controlled Se flux during the anneal. This adds an additional dimension of process control with only a modest reduction in manufacturability. With the additional complexities which come with the addition of Ga we find that the added dimension of control is at least helpful and may eventually be found to be necessary.

The primary variable for the processes is the precursor. The precursor is formed in step 1 by sequential deposition of the elements following deposition of the Mo contact. The order in which they are shown in the figures is not necessarily favored, and T may be increased above room temperature. Ga can be added to M1 as well. Its inclusion brings the number of elements to 4 and

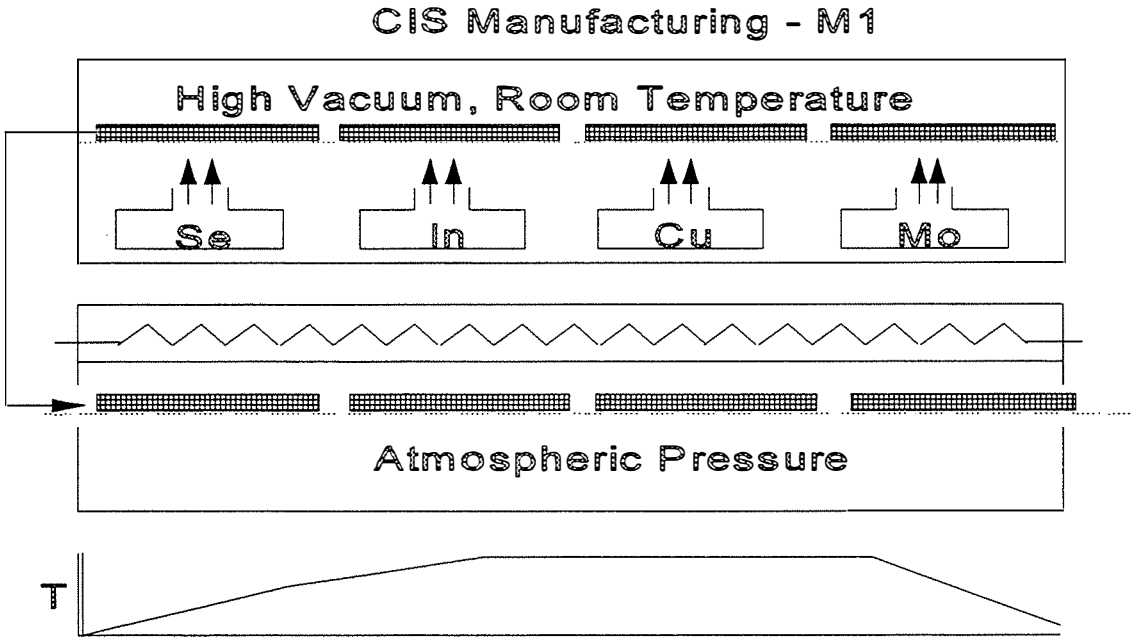

Figure 1. Process M1(coat and cook) for CIS.

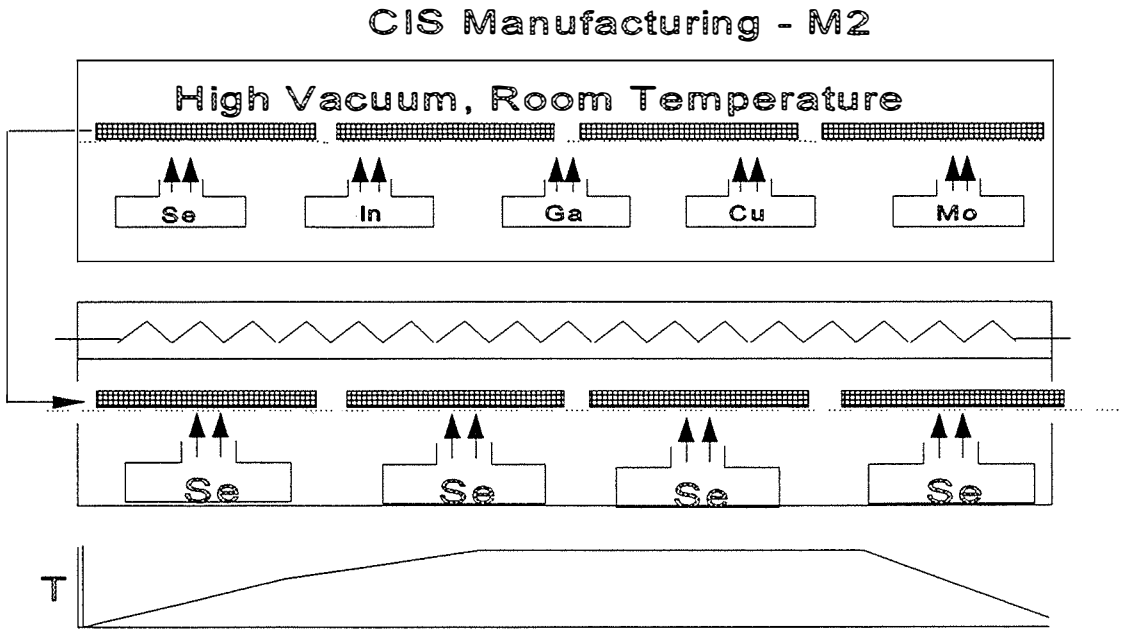

Figure 2. Process M2 using Se flux anneal for CIGS.

correspondingly increases the number of possible perturbations for the precursor. The anneal profile is the second major variable. Although it is depicted spatially here as temperature, its key attributes are time and temperature. The third major variable is the presence of Se during step 2. In M1 its presence is determined by that carried in with the precursor and the details of the arrangements within the anneal chamber. The level of control is minimal. In M2 Se flux is controlled throughout the anneal. The added complexities due to Ga in formation of the final surface are particularly targeted by this added control. The primary variables for the two processes are summarized below(P - precursor, T - anneal profile, Se - Se flux profile).

Process	Primary Variables
M1	P , T
M2	P , T , Se

Table 1. Primary variables for precesses M1 and M2.

Although this seems simple, given the large number of possible P's, and the continuous nature of T and Se, the number of combinations is extremely large. Needless to say, finding the way takes considerable effort and patience. We have mapped out a large segment of this fabrication space and have gained considerable generic insights. In the following sections we report these and the progress in device performance resulting therefrom.

PERFORMANCE ADVANCEMENT DUE TO Ga

In the absence of Ga our devices were limited by low Voc's (400 - 425 mV) while maintaining consistently high Jsc's (35 - 40 mA/cm^2). Thus our primary expectation from Ga was increased Voc. The realization of this expectation is summarized in Table 2 below for three different precursors.

Range	PI	PIIA	PIIB
E_G	1.0 - 1.1	0.95	1.1
Voc	450 - 500	450 - 480	540 - 560
Jsc(no AR)	25 - 30	33 - 39	25 - 28
FF	.58 - 62	.60 - .68	.68 - .73
Best Efficiency	9.5	12.0	10.2

Table 2. Device performance parameters for three precursors.

Precursor 1(PI) consists of sequential layers, Cu/In/Ga/Se, and was processed by M1. This is our

standard precursor for non-Ga devices which have a band gap of .95 eV. The higher E_G for PI of 1.0 -1.1 eV indicates that Ga was incorporated in the film and raised Voc. But, there was a concomitant loss in Jsc resulting in no net increase in efficiency over our non-Ga devices. Precursor II consists of the same ingredients as PI, but these are pre-reacted before going into the step 2 anneal. PII

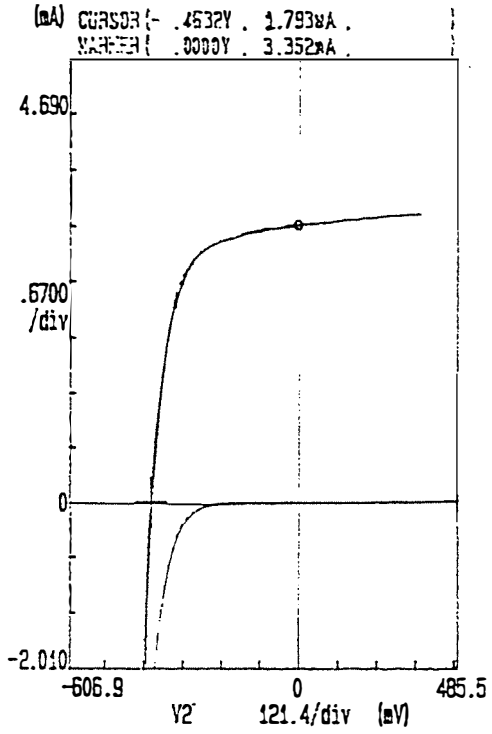

Figure 3. Power curve for device from type PIIA precursor.

devices are also processed with M2. For PIIA devices, although there was no increase in E_G, Voc increased with only a modest loss in Jsc. This resulted in an advancement in efficiency to 12.0% with Voc = .463, FF = .66 as shown in Fig 3. Jsc was determined to be 39.2 mA/cm^2 by integration of the spectral response. (None of these devices has an AR coating). The increase in Voc without an increase in E_G has important implications which will be discussed further below. PIIB which is another variation of PII had the biggest effect on Voc. It also produced additional improvement in FF. A power curve for one of these devices is shown in Fig. 4. Taken together these indicate a significant improvement in the surface properties of our devices. This has been a major objective for this project, and we feel that we have now demonstrated notable progress toward its accomplishment. *We also note that achievement of 12% efficiency represents accomplishment of the primary milestone for Phase I of this project.*

In Fig. 5 we show a plot of Voc versus E_G for representative high efficiency devices from the literature and for PI and PII devices. The literature devices are primarily made by coevaporation or selenization with H_2Se. The solid line is a least squares fit to the data and thus indicates expected

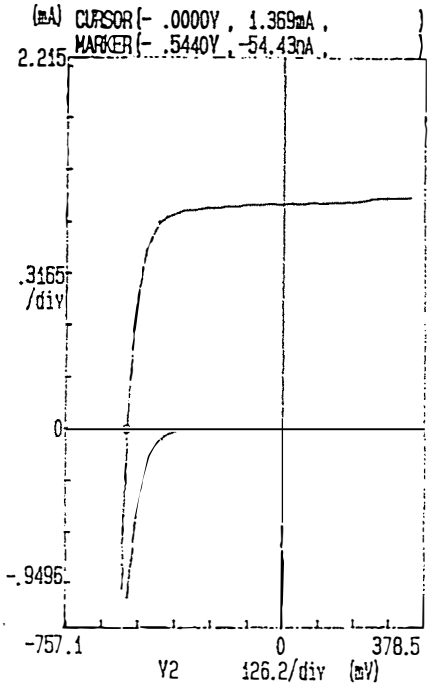

Figure 4. Power curve for device from type PIIB precursor.

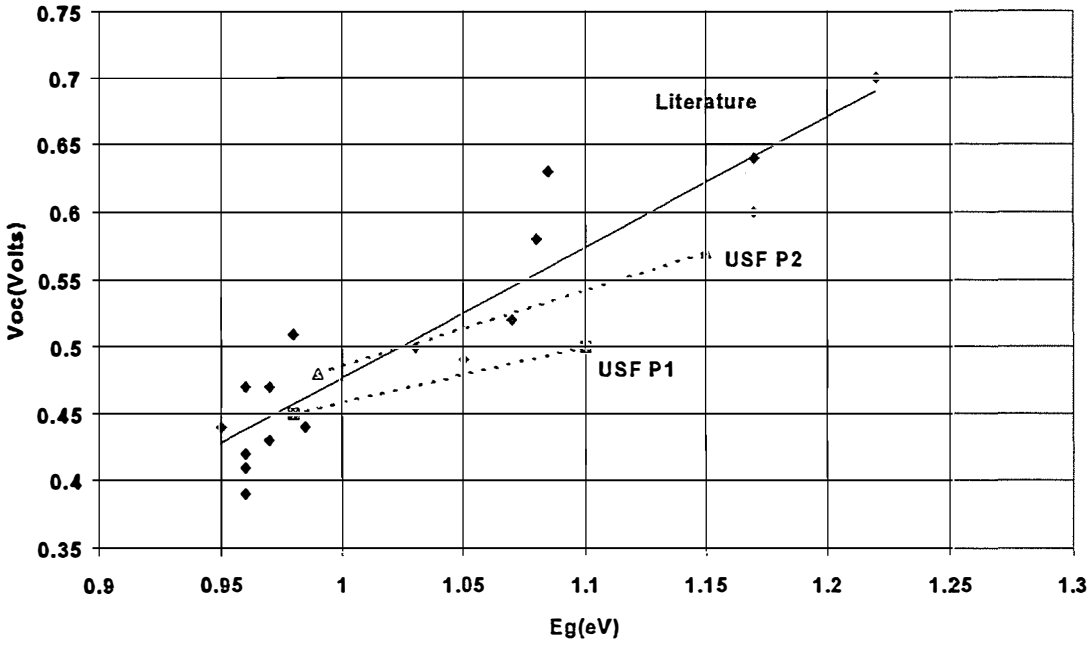

Figure 5. Voc vs. E_G for representative high efficiency devices from the literature and USF devices for precursors PI and PII.

Voc's as a function of E_G for state-of-the-art devices. As can be seen, for $E_G < 1$ our devices are typical. However, since the highest efficiency devices are made for $1.1 < E_G < 1.2$, we are endeavoring to move our band gap into that range. As can be seen, for both PI and PII we start falling below the curve at higher E_G, however, PII now has a steeper slope with increasing E_G and offers more promise of further improvements in surface properties. We also wish to note that these devices are fabricated on common soda lime glass literally purchased at the hardware store. We also have not used Na_2S which is known to help increase Voc by allowing greater control over Na levels.

Referring back to Table 2. we note that the progress with surface properties has come at a cost to Jsc. The interrelationships among the key parameters which we have been observing will be discussed in further detail below. However, given the similarities of PIIA and PIIB we expect to combine the best properties of each in a single device. Thus the PIIB device in Fig. 4 above would have an efficiency of 15% with the Jsc of the PIIA device in Fig. 3. Needless to say, this is a major focus of our current efforts.

SURFACE/BULK OPTIMIZATION

Throughout this project the major challenge has been to simultaneously optimize bulk and surface properties. In this section we present results, observations and speculations regarding this complex issue. Ga has had a major impact in terms of adding complexity as well as enhancing performance. However, we are now confronted with perhaps an equal role for junction formation. That is, we are finding that there is no generic junction formation process that works equally well for all CIGS semiconductors. In addition to the already complex interrelationship between surface and bulk during semiconductor growth, there is an additional interrelationship between the semiconductor and the junction formation process. Understanding and controlling each of these is critical to performance. The status of our progress with these issues is presented below.

The Role of Gallium

Prior to adding Ga to our devices we were confronted with surface/bulk tradeoffs as manifested by inverse Jsc versus Voc dependence. These devices were made primarily with process M1. The results of one of the early M1 runs with Ga are shown in Fig. 6. The run that this device is from consisted of a 3" x 4" substrate onto which an array of devices was fabricated. The Cu/(In + Ga) ratio was also graded somewhat across the substrate. The J_{sc} values are determined by integration of the spectral response under light bias using NREL reference cells. As can be seen, the V_{oc}'s ranged from 400 - 500 mV a notable increase over non-Ga devices. However, in spite of the scatter in the data there is obviously an interdependence between J_{sc} and V_{oc}. The initial increase of Jsc with Voc is attributed to favorable incorporation of Ga. Starting at 450 mV we then see a decline which is much greater than that expected from increases in E_G. From these results we concluded that the process modifications made to incorporate Ga led to a deterioration of our space charge region properties. This reduced Jsc relative to non-Ga devices. As small quantities of Ga were added the surface defects were passivated which improved both Jsc and Voc. As the Ga level increased further, the turndown in Jsc was the result of introduction of new defects by Ga. Some of these defects may be associated

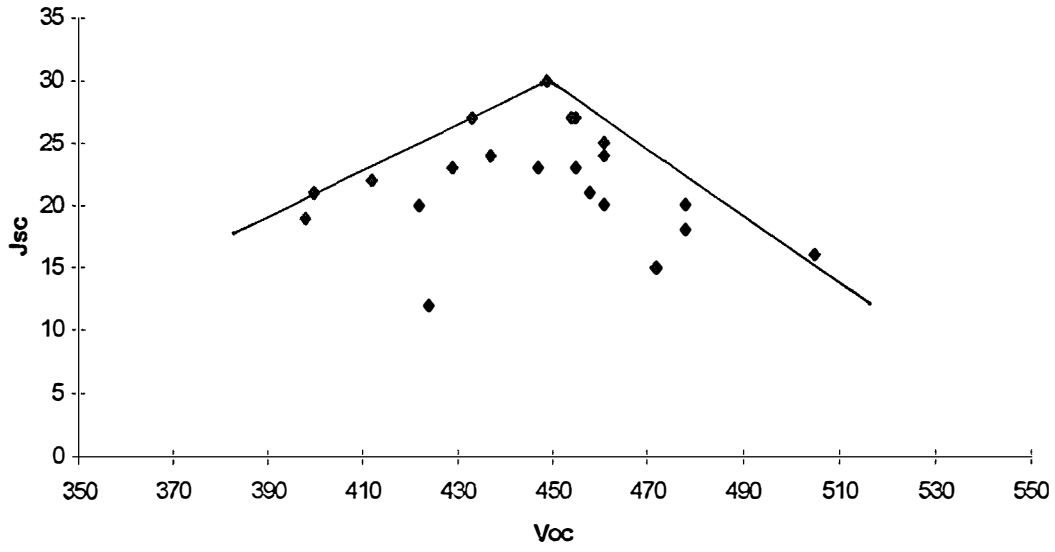

Figure 6. Jsc/Voc tradeoff for process M1.

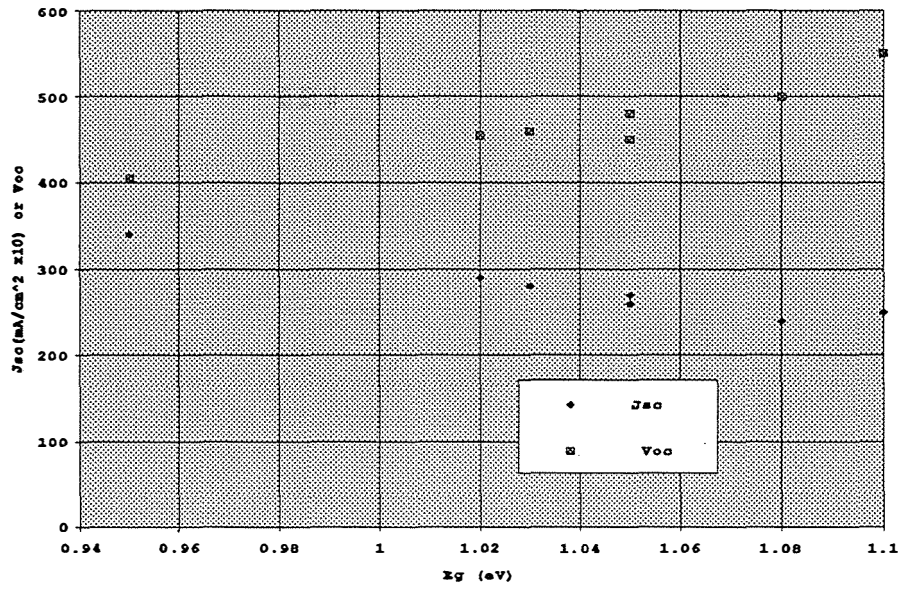

Figure 7. Voc and Jsc dependence on E_G for type PII precursor runs using process M2.

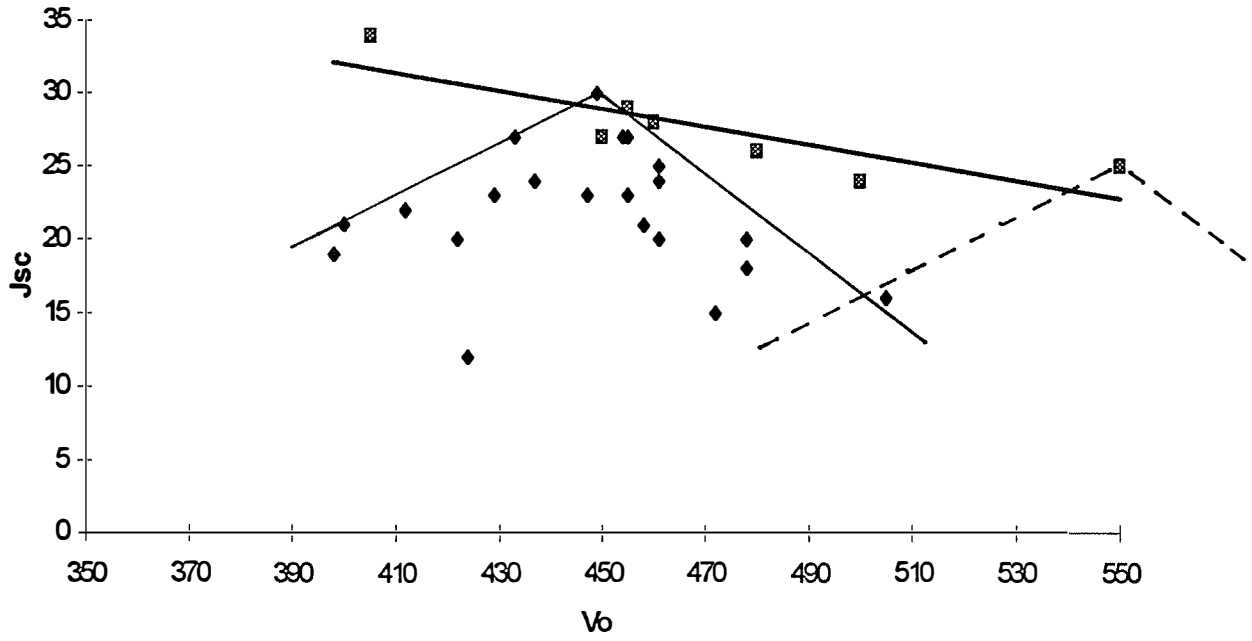

Figure 8. Comparison of Jsc/Voc tradeoff for M1(◆) and M2(■).

with improperly bonded Ga, while there is also evidence that properly bonded Ga may also act as a defect. It is also likely that microscopic phase inhomogeneities are present and contributing to complex behavior.

Although these early experiments with Ga in process M1 were leading to advancements in performance, the added complexities could be better handled with increased process control. We thus switched to process M2 as the primary one for understanding the role of Ga. Our initial efforts with M2 focused on accommodating Ga into the process in such a way as to not deteriorate the surface of films by using minimal Ga. This led us to precursor PII which could produce devices with trace Ga, no change in E_G, and performance equivalent to non-Ga devices. The M2PII combination was then used to systematically study the effect of Ga. The data in Fig. 7 is from a series of runs. As can be seen, E_G can be increased from 0.95 eV and Voc of 400 mV up to 1.1 eV with an accompanying increase in Voc up to 550 mV. Thus ∇ Voc/ $\nabla E_G \approx 1$, the expected ideal. Therefore, as far as surface properties are concerned, for this series Ga had no negative influence. The decline in Jsc with increasing E_G suggests otherwise for bulk(space charge layer) properties. While this decline remains troublesome, a comparison of this data with that for process M1 in Fig. 8 shows considerable improvement for this new process. The devices with Voc of 550 mV are slightly more efficient than

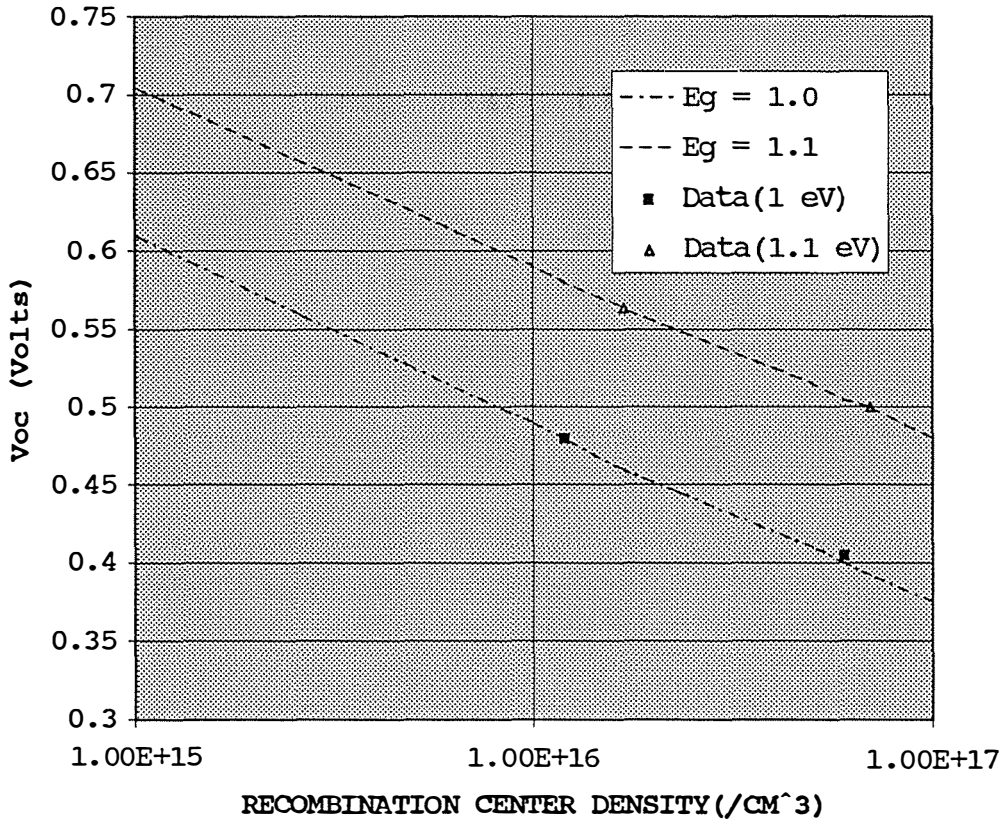

Figure 9. Simulation of dependence of Voc on recombination center density.

those at lower Voc, and as will be discussed further below, it is important to continue improving Jsc at higher Voc's.

It is interesting to compare the two sets of data on a relative basis. The PII series allowed greater control and hence ability to separately tune surface and bulk properties. This resulted in improved performance at both low and high Voc relative to M1. Since the M1 data is from a single run it clearly shows the tradeoff that must be endured given the lack of control. However, we are hopeful that what we learn from the M2PII runs will teach us how to shift the peak for M1 to higher Voc as indicated by the dashed lines. Thus we will be able to transfer performance advances to the desired M1 process. Our thoughts at this point are that the In level at the surface is a key element in the behavior of the M1 surface. Experiments are under way to further our understanding of this important issue.

Surface Quality

We have previously reported the use of a SRH based recombination model to guide device development(2). The key aspects of the model are that Voc generation is dominated by recombination in the space charge layer and that the principal recombination zone is near the metallurgical interface

with CdS. Thus advances in Voc are expressed in terms of recombination center density(RCD) reduction as shown in Fig.9. The dashed lines are simulations from the model for band gaps of 1.0 and 1.1 eV, and the symbols are data. The parameter set chosen for the simulations is typical of data in the literature. The key parameters are the RCD's and capture cross sections for electrons and holes which determine the recombination lifetimes. Since these have not been independently measured, we choose a neutral atomic cross section of 1×10^{-15} cm^2 for both holes and electrons. The RCD is then calculated by the model to fit the measured Voc. A RCD of 1×10^{16} $/cm^3$ thus results in a recombination lifetime of about 2.5×10^{-9} sec. This is in good agreement with lifetimes measured in our devices by the DBOM technique(3).

Improvements in Voc are thus an indication of progress in improving surface quality by reducing the RCD. The data point in Fig. 9 at Voc = .405 is the highest for non-Ga devices. The data point on the Eg = 1.0 eV line at .480 indicates the improvement in surface properties to date due to the addition of Ga, but in the absence of a band gap change. We speculate that trace quantities of Ga are remaining in the recombination zone and reducing point defect based recombination centers. As discussed above, we are able to add Ga and cause a change in Eg as well. The upper curve and data points represent our accomplishments with that approach. As can be seen, there is nearly a 1-1 increase in Voc due to the band gap change. However, devices with Eg = 1.0 have a slightly lower RCD thus far. This raises an interesting and important question. Can Ga be incorporated substitutionally for In without increasing recombination? Results to date suggest that this may work, but only up to a certain Ga level. Further work is required to answer this question more generally.

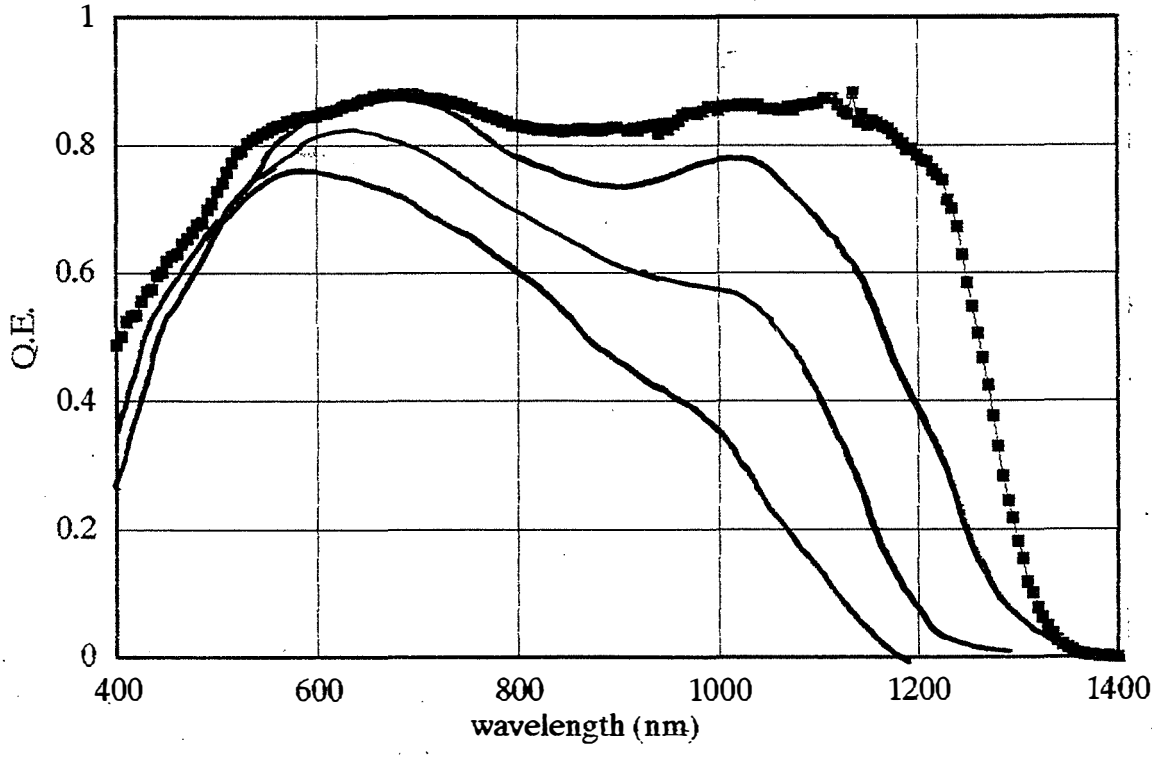

Figure 10. Quantum efficiency spectral response for devices with increasing Ga levels.

Another manifestation of the effect of Ga is seen in spectral response data(Fig. 10). As Ga is added to increase the band gap, there is a systematic deterioration of the quantum efficiency(Q.E.) spectral response. As can be seen, the slope of the absorption edge gets shallower, and the slope above the absorption edge increases. This is thought to be a complex interplay between absorption and collection phenomena and adds another insight to the consequences of Ga incorporation. The same Ga which is deteriorating the spectral response is nevertheless leading to increases in Voc. In reconciling this with the SRH model we tentatively conclude that the spectral response behavior is in part driven by electron transport, while lifetimes are nearly unaffected. Thus Ga increases the band gap while not significantly changing lifetimes which results in increased Voc. At the same time the incorporated Ga is decreasing the electron mobility resulting in poor collection of carriers generated deep in the space charge region or beyond its edge. Additional experiments are under way to further our understanding of these phenomena. Similar observations have recently been made by the IEC group(4).

In comparing these results we note that through variations in our deposition techniques we can controllably determine the role played by Ga. That is, we can have it replace In or just be available for point defect control. In the latter case the process is also self-regulating. That is, excess Ga not needed to passivate point defects apparently moves to the rear of the device and helps form the Mo interface. When a larger band gap is desired, we can activate the Ga to have it substitute for In. This understanding and the control which it allows is critical to further improvements in performance. We also point out that further refinement of these techniques involves interplay with Se. Our current efforts are focused on furthering understanding of these important interactions. The 12% result reported above is a consequence of these efforts.

JUNCTION FORMATION

The primary emphasis of this project has been on developing improved deposition techniques for the semiconductor. We have used a "generic" junction formation process throughout these efforts. This process consists of CBD CdS and sputtered ZnO. It is becoming clear that these techniques are not generic in that there is interaction between the semiconductor and the junction formation process. That is, we are not just adding a contact layer to the CIGS, but are modifying the CIGS surface as we form the junction. Consequently we must recognize that the junction optimization process might have to be matched to the semiconductor. While this further complicates our efforts, it is important that appropriate attention be paid to this issue. The NREL Thin-Film Partnership team has started to organize itself around such issues and devote resources accordingly. As a member of one of the junction teams we have dedicated some of our resources to participate in these activities. Some early results from these efforts are presented below.

CBD CdS

The effect of time in the CdS bath on performance is shown in Fig. 11. t1 is about five minutes of growth time after reaching the growth temperature(about 75° C). t2 is about seven minutes. The results are for an array of devices containing a Cu gradient and two levels of Ga. For devices

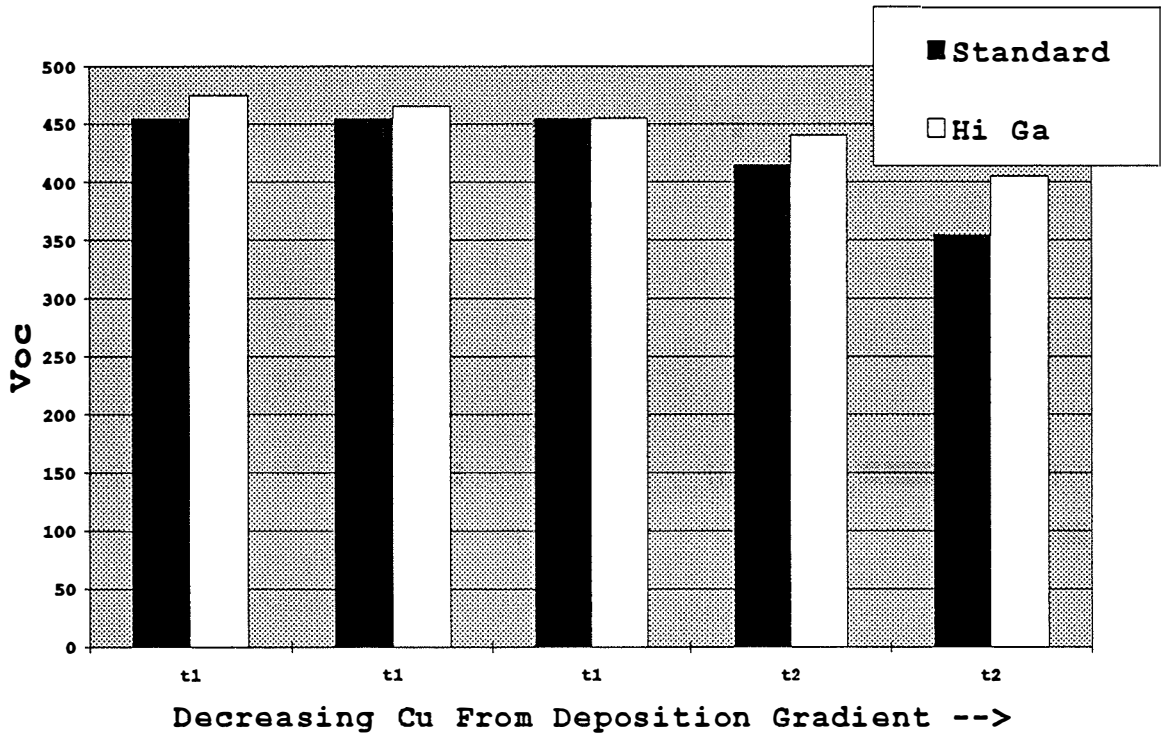

Figure 11. Effect of time in CdS bath(t2 > t1) for an array of devices containing a Cu gradient and two levels of Ga.

containing the standard level of Ga there is a significant drop in performance due to the longer t2. It is also apparent that there is an effect due to the Cu gradient. When the Ga level is raised(by about 15%) the effect of the t2 exposure is diminished. This is somewhat counter intuitive in that a deficiency of Cu is countered by adding Ga. The mechanisms at work during CBD growth can not be revealed from such limited results. But they do send a strong message that device performance is a significant function of the details of the CBD procedure. Interpretation of the results from Fig. 11 regarding the effect of Cu gradients and Ga levels could be quite different if only t1 or t2 data were available. It is clear that optimization of device performance requires efforts with junction formation as well as with semiconductor growth.

ZnO

ZnO, even more so than CdS, has been considered as a passive component in device performance. An aspect of ZnO to the contrary is the need for an undoped layer next to the CdS. Given the thinness of CdS, it is likely that the space charge layer extends through it and into the undoped ZnO layer. Since it is widely thought that recombination in the space charge layer is the dominant device mechanism, it is then necessary to consider that at least part of the ZnO layer is "active". In a previous phase of this project we had reactively sputtered ZnO under development. We found that there were certain processing advantages that it offered relative to the standard process and that these

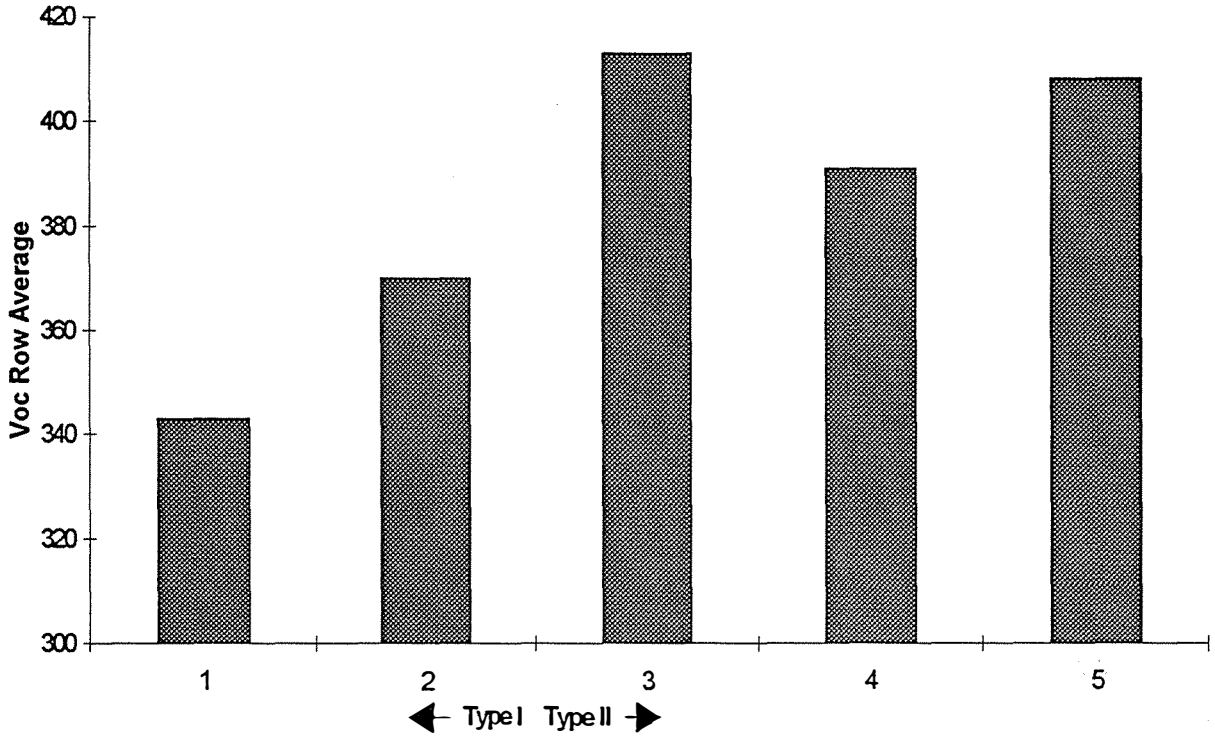

Figure 12. Effect of two types of undoped ZnO on device performance.

might contribute to advances in performance. Using these insights we modified the deposition technique for the undoped ZnO layer and realized significant improvement in performance for some devices. A typical result for some of our earlier lower voltage devices is shown in Fig. 12. The results are averages for a row of 5 devices for a 5 x 5 array from a single run. The first two rows were processed with standard ZnO(Type I) and the next three with our modified intrinsic layer process(Type II). The advantage of the latter is obvious. After doing side-by-side comparisons for a number of runs we found that Type I, while not always inferior to Type II, was never better. We thus adopted Type II as our standard, and it is the process that was used for the high performance devices reported above.

Another interesting aspect of our devices that we believe is related to Type II ZnO is that they do not require post deposition anneals. We are continuing to study the complex interplay between all of the layers of the devices. We are convinced that as our understanding develops better options for junction formation and performance will be forthcoming.

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The main objective of this project is to develop high-efficiency CdTe solar cells based on processing conditions favorable for manufacturing processes. This report presents the results on work performed during the first phase of this project. One of the major issues addressed is the use of soda-lime glass substrates in place of the borosilicate glass often used for laboratory devices; another task is the preparation of Cu(In,Ga) Se_2 solar cells by selenizing suitable precursor films. Emphasis is placed on processing and how different reaction schemes affect device performance. It was found that different reaction schemes not only change the bulk properties of $Cu(In,Ga)Se_2$, but also its surface properties, which critically affect device performance. Although the objective is to optimize processing to meet the manufacturing constraints, work has not been limited within these requirements.

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