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CHARACTERIZATION OF BICRYSTAL GRAIN BOUNDARY PROPERTIES USING DEVICE STRUCTURES

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ABSTRACT

This work centers on the use of small (2 mm × 2 mm) photovoltaic devices to determine the electrical characteristics of selective grain boundaries. The ESP bicrystal sheet growth method allows crystal orientation to be determined prior to growth and as such is an excellent tool for selective examination. Photolithographic techniques of a special pattern and mesa etching were used to isolate areas on and around the grain boundaries for device characterization. Spreading resistance measurements over and next to the grain boundaries, as well as characterization, were used to study electrical effects of these grain boundaries.

INTRODUCTION

The fact that many low-cost silicon growth techniques for solar cell applications produce multigrained material has increased both the awareness and importance of understanding grain and grain boundary effects. While these boundaries have been characterized extensively on a microscopic level (1,2), little has been done to date to establish a method of characterizing the effects on photovoltaic devices of different grains and grain boundaries. The intent of this study is to demonstrate one such technique for examining these effects.

Sheet growth of solar cell materials usually generates multicrystalline structures having various grain orientations. One very important aspect of this study has been to demonstrate that the growth of specific grain orientations is reproducible. A recent sheet growth technique (3,4,5) called edge-supported pulling (ESP) allows defined bicrystals to be grown conveniently. The orientations of two crystals on one sheet can be predetermined by seeding at the beginning of growth. The grain boundary between the two desired orientations and its effect on the performance of the device is examined predominantly by means of a small device structure.

Before device fabrication, some characterization of grain boundary electrical activity can be determined using a spreading resistance technique. This technique examines the carrier concentration on either side of the grain, as well as the resistance across the grain boundary. The spreading resistance method provides a rough estimate of electrical activity across the grain boundary.

The bicrystals are then processed into solar cells, using conventional cell processing techniques. A special top metallization pattern that is capable of either intersecting or running parallel to the grain boundary is applied photolithographically. Mesa etching delineates the individual devices, permitting selective characterization of the grain boundaries. These patterns are also used to examine the bulk characteristics of the crystals grown by the ESP method. A comparison of the device locations is then made to determine the boundary effects.

Two other techniques were utilized in this study: electron channeling to indicate crystal orientation and electron-beam-induced currents (EBIC) to examine in greater detail the boundary effects. Since most multicrystal growth techniques do not produce such well-defined grain orientations, we also demonstrate this technique on a cast polysilicon material.

EXPERIMENTAL

Bicrystal material is grown by ESP using two 20- to 25-mm seed crystals on a graphite holder. The graphite holder, with filaments extending beyond the seeds, is immersed into molten Si and slowly withdrawn. The seeds used for this study had [110] or [112] surface normals on one side and growth directions within 30 degrees of [112] or [110], respectively, on the other side. These seeds were chosen based on observations of preferred orientations during unseeded growth as well as on what appears to be a blockage of spurious grain boundaries on ESP ribbons seeded with these orientations. Figure 1 is an illustration of the arrangement for the ESP growth, showing the seeds mounted on the filaments. The bicrystal is grown until it degenerates either from multiple grain formation or interference from grains that nucleate at the filament edges and grow inward.

After growth, the bicrystals are lapped and polished to obtain a uniform surface and thickness.

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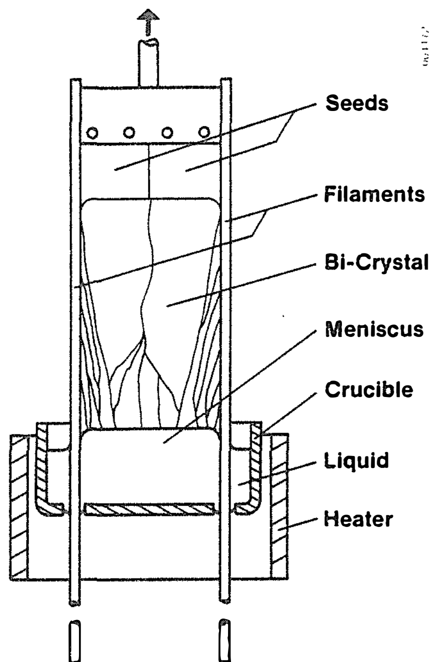


Figure 1. **Diagram of ESP Puller Used for Bicrystal Growth**

The polish removes the visual evidence of the grain boundary, so a brief (~15 seconds) Secco etch (6) is used to delineate the grain boundary. This is important both for spreading resistance and alignment of the top metallization. Spreading resistance on the samples is typically done at four locations: two runs on either side of the grain boundary in clear, single-crystal regions; one pass across the boundary; and one pass with each of the two tips (separated ~50 μm) straddling the boundary. Figure 2 is a photomicrograph of a bicrystal showing the four spreading resistance tracks.

The bicrystals, which are doped either n- or p-type to 2 Ω-cm resistivity, are then processed using typical solar cell device techniques. First, all samples are thoroughly cleaned. For p-type materials, the junction is formed by diffusion from a $POCl_3$ source in a tube furnace. The n-type material has its junction formed from drive-in of a spin-on boron dopant. In both cases, a junction depth of 0.3 μm is achieved. After the back parasitic junction is removed by chemical etching, the back contacts are evaporated onto the sample: 2 μm of Al on the p-type material and 1 μm of Ti-Pd-Ag on the n-type silicon. A photoresist (Shippley 1350) is applied to the fronts, and a mask aligner is used to align the pattern. The pattern consists of a single finger, 50 μm wide, on a 500-μm-square contacting pattern. The pattern alternates the finger direction by 90 degrees so it is possible to align the fingers both perpendicular (bisecting) and parallel to the grain boundary, allowing grain boundary effects on current generation in the device to be determined. The top contacts of Ti-Pd-Ag are evaporated; then, lift-off of the photoresist leaves the defined metallization. Photoresist is reapplied, and a mask which opens up a rectangular 2-mm × 2-mm pattern is aligned around the metallization. After a hard bake, the sample is etched in a 3-1-2 etch for 10 seconds, which creates moats ~ 20 μm deep that define each cell area. The final result, illustrated in Figure 3, shows the 2-mm-square devices with top contacts and moats. These devices are then tested for their I-V characteristics on the completed cells.

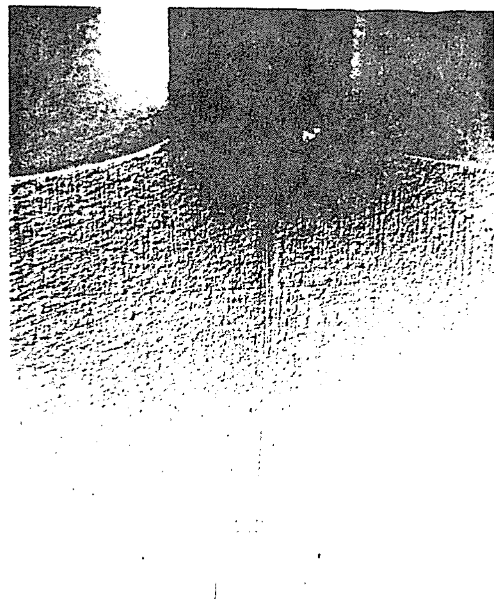


Figure 2. Micrograph of Bicrystal Sample (Spreading resistance probe marks visible)

Processing of the cast polysilicon materials produced several interesting devices. To further characterize these devices, EBIC was used to examine their current generation. EBIC confirmed the results obtained on the devices, and electron channeling revealed their grain orientations.

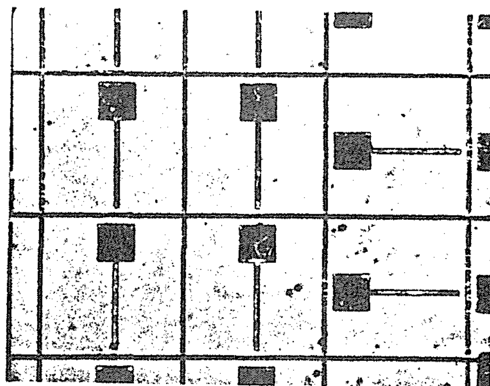


Figure 3. Sample Devices (with Moats) on Single-Crystal Silicon

RESULTS

The ESP growth technique provided excellent bicrystals for use in this study. Grain boundaries typically were several cm long and were either straight or exhibited few directional changes. The exception to this was that attempts to grow a [112] 10-degree bicrystal resulted in growth of multiple boundaries almost immediately.

Spreading resistance measurements differed across various boundaries. Figure 4 shows the spreading resistance data across a [110] 10-degree rotation boundary; Figure 5 provides more detail and shows typical results for each of the four traces (across, one on either side, and straddling). Results from a [112] 30-degree rotation showed little difference in spreading resistance, while a plot across a bundle of nonparallel grain boundaries showed enhanced spreading resistance (Figure 6). The spreading resistance measurements correlated with what we observed in the completed devices: certain boundaries between rotations, and the orientation of the grains on either side, may affect the devices in various ways, from insignificantly to very noticeable differences in performance.

Device measurements were made using an ELH simulator and computerized data acquisition system. The measurements on the single-boundary material produced by ESP showed little effect, regardless of orientation. Figure 7 shows three typical I-V curves for cells parallel, perpendicular to, and off the grain boundary. The only significant results were observed when multiple boundaries were examined; these results, with a corresponding micrograph of the tested area, are shown in Figure 8. In this example, the roughly 200 boundaries

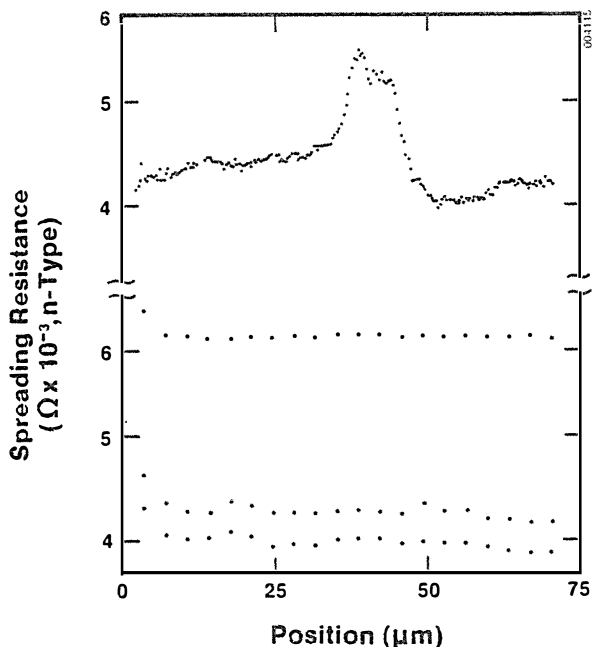


Figure 4. Spreading Resistance Across Bicrystal Boundary

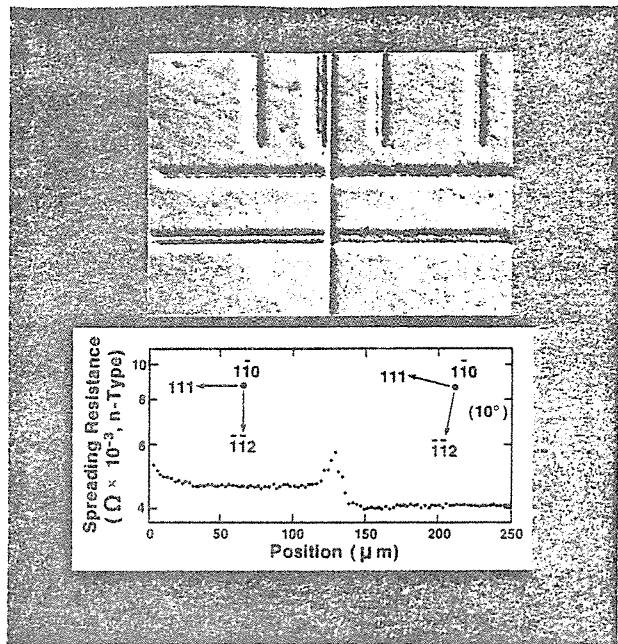


Figure 5. Spreading Resistance Across, Straddling, and on Either Side of the Bicrystal Boundary

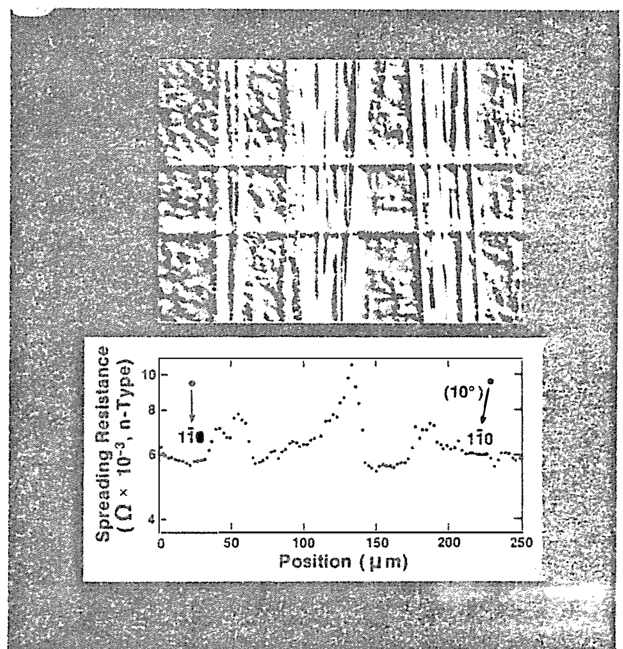
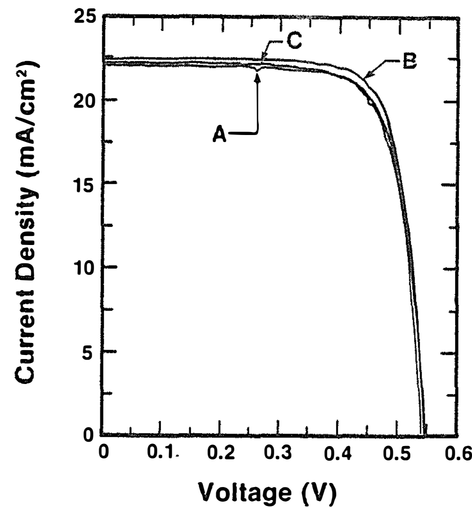


Figure 6. Spreading Resistance Across Bicrystal Sample with Grain Bundles



	A Off Grain Boundary	B On Grain Boundary Parallel	C On Grain Boundary Perpendicular
V_{oc}	0.546 V	0.546 V	0.543 V
I_{sc}	0.9 mA	0.9 mA	0.9 mA
J_{sc}	22.1 mA/cm²	22.5 mA/cm²	22.2 mA/cm²
V_{mp}	0.453 V	0.447 V	0.452 V
I_{mp}	0.8 mA	0.8 mA	0.8 mA
P_{max}	0.4 mW	0.4 mW	0.4 mW
FF	0.76	0.77	0.75
Eff	9.1%	9.4%	9.1%

Figure 7. I-V Curves of Typical Device Performance on Bicrystal

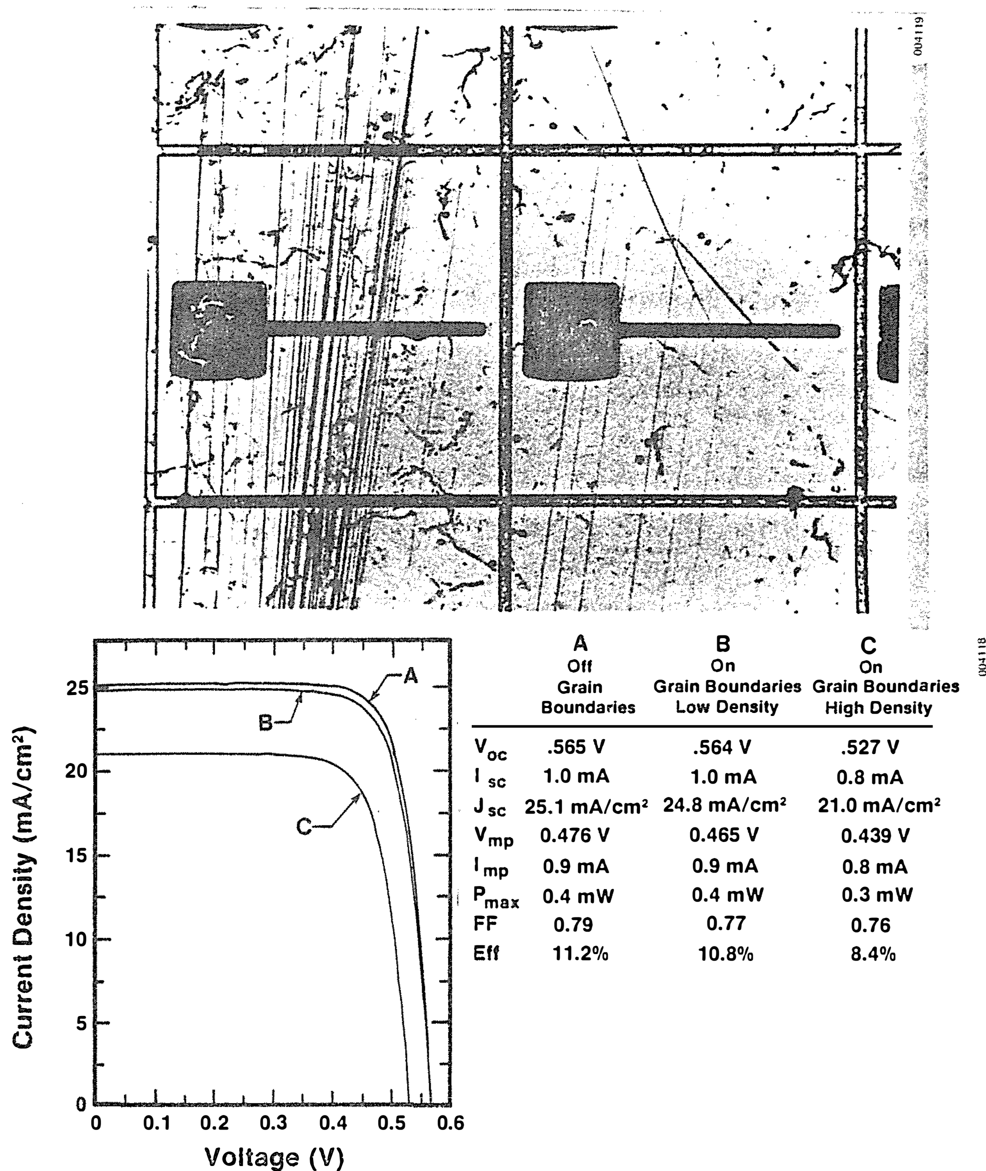
degrade the cell performance. This degradation is seen primarily in the short-circuit current, with some degradation also noted in the open-circuit voltage and fill factor.

Greatly different results, however, were observed on studies of the cast polysilicon samples. Figure 9 shows a sample of the cast material with devices on the grain boundaries. The I-V curves for three cells on this device indicated substantial performance differences, as shown in Figure 10. While the curve for the cell off-grain on the left side is 30% worse than the single-crystal control wafer processed at the same time, it is much superior to that of the off-grain cell on the right. The cell with metallization perpendicular to the boundary represents an average value of the two contributing grains.

Two techniques were used on the cast silicon to determine the orientation of the two grains and their current collection characteristics. Grain orientation was determined using electron beam channeling, a technique described elsewhere (7). The channeling indicated the orientation of the right grain was ~40 degrees off the [112]; the orientation of the left grain was ~12 degrees off the [100]. The results of the EBIC are shown in Figure 11. This EBIC, done on the cell that straddles the grain boundary, clearly indicates the lower current collection of the right grain. Surprisingly, the difference between the left and right grains on the device structure is not in current, but in voltage and fill factor. This discrepancy is presently being analyzed.

DISCUSSION

A systematic approach to analyzing grains and grain boundaries has been detailed in this study. The approach capitalizes on the ESP technique in growing a well-defined bicrystal grain boundary typical of the boundaries found in sheet-grown silicon. The electrical properties of the grain are analyzed first by spreading resistance, where it is evident from the results that some boundaries, such as along the [110] axis, exhibit a strong spreading resistance, while others show little effect. Using small (2-mm x 2-mm) cell structures was not effective in isolating changes across the single bicrystal structures grown for this study. The reasons for this may lie in the inaccuracy of the measurement system, or it may be that the limited number of orientations studied simply do not have highly active grain boundaries. This is an interesting possibility in itself, as the orientations studied are those most likely to be



	A Off Grain Boundaries	B On Grain Boundaries Low Density	C On Grain Boundaries High Density
V_{oc}	.565 V	.564 V	.527 V
I_{sc}	1.0 mA	1.0 mA	0.8 mA
J_{sc}	25.1 mA/cm²	24.8 mA/cm²	21.0 mA/cm²
V_{mp}	0.476 V	0.465 V	0.439 V
I_{mp}	0.9 mA	0.9 mA	0.8 mA
P_{max}	0.4 mW	0.4 mW	0.3 mW
FF	0.79	0.77	0.76
Eff	11.2%	10.8%	8.4%

Figure 8. I-V Curve and Sample Showing Device Performance Degradation with Bundle Quantity

generated in sheet-grown cells which to date have demonstrated good efficiencies compared with single-crystal cells.

The real advantage of the small cell technique appears in its ability to isolate areas on multicrystalline materials. We have shown that its use on cast materials clearly indicates the differences in electrical performance between various grains. The EBIC analysis is certainly capable of a higher resolution, but it is a technique that not all Si material producers can use. The discrepancy between the cells having a lower voltage and fill factor but similar currents, and EBIC studies, which indicated dissimilar currents, represents an interesting area of study. Explanations may hinge on differences in processing parameters between grains or differences in surface characteristics.

The diagnostic small cell structure presented here is a quick, relatively easy way to analyze grains within multigrained materials. This convenience is necessary for most material manufacturers, and it is important to future studies of grains and their differences.

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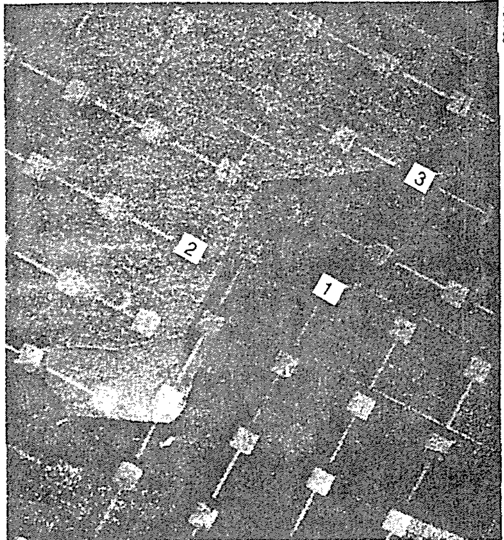


Note: See Figure 10 for an explanation of 1, 2, and 3 above.

Figure 9. Devices Patterned on Cast Material

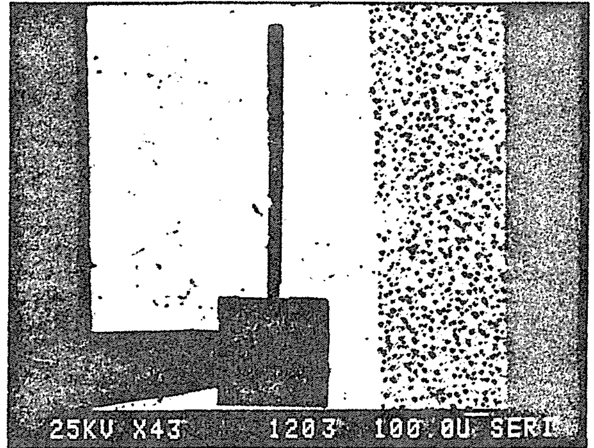
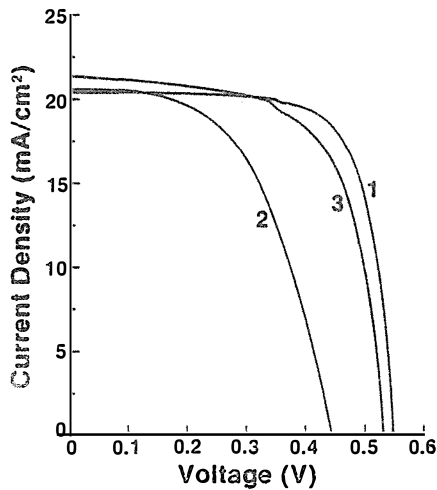


Figure 11. EBIC Representation of Grain Boundary of Cast Material



	1 Off Grain Left	2 Off Grain Right	3 Perpendicular
V_{oc}	0.548 V	0.443 V	0.527 V
I_{sc}	0.8 mA	0.8 mA	0.9 mA
J_{sc}	20.3 mA/cm²	20.5 mA/cm²	21.4 mA/cm²
V_{mp}	0.449 V	0.291 V	0.421 V
I_{mp}	0.7 mA	0.7 mA	0.7 mA
P_{max}	0.3 mW	0.2 mW	0.3 mW
FF	0.73	0.53	0.65
Eff	8.1%	4.8%	7.3%
	94 Ω/□	86 Ω/□	
	3.3 Ω-cm	2.9 Ω-cm	

Figure 10. I-V Curve on Three Regions of Cast Material

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