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Final Technical Report
14 December 1995 - 31 December 1996

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Executive Summary

The progress made at Solarex is shown below for both device and module efficiencies from the inception of the CIS research program to the present. A rapid improvement in efficiency is apparent, culminating in a the fabrication of a 15.5% efficient device (total area) and a 13% efficient submodule (aperture area). The device represents the highest efficiency device measured by NREL for any industrial source. The module represented a new world record for ***any thin film module*** at the time of its measurement.

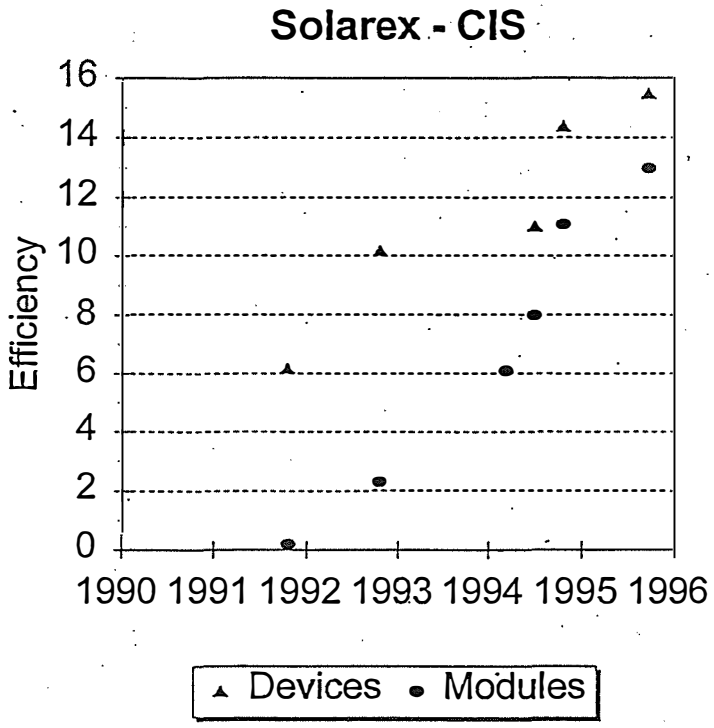

Figure (executive summary). *Progress in the Solarex CIS program in terms of device and module efficiency.*

The factors leading to these results included improvements in absorber layer quality, transparent contacts, scribing and module formation processes. Although not evident in the graph above, other elements critical to commercialization of CIS based PV were also successfully attacked, including reduction of absorber deposition times into the range of 10 to 20 minutes and the successful scale up of the absorber deposition process to greater than 500 cm^2. Other requisite processes saw continued development, such as a rapid, low cost method for transparent window deposition.

Subsequent to the demonstration of 13% module efficiency, scribing techniques were further improved which resulted in a reduction in shunt losses, and higher module fill factor. This improvement, and the concomitant gain in fill factor would yield efficiencies approaching 14% on modules having a short circuit current and open circuit voltage comparable to the record module.

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4. Introduction

4.1 Historical Perspective and Challenges

Devices based on copper-indium-diselenide (CIS), or related gallium-containing alloys (CIGS), whose efficiency approaches 18% (total area basis) have now been demonstrated [1,2]. Additional to the potential of high efficiency, this material system also allows for PV products which are stable, robust, potentially low cost and benign from a toxicological standpoint. Thin film CIS or CIGS having suitable electronic qualities has been deposited on low cost substrates by a variety of methods. Modification of electronic properties such as band gap using ternary alloys has been accomplished [3], thus making the system versatile as well as robust.

The initial contract for CIS work at Solarex was from November, 1990 until June, 1995. Many important developments took place during a lapse of several months between the first contract and the present contract. For continuity and completeness work done during this lapse will be included in this report, even though some of those results have been described in an addendum to the final report for the first contract.

In the initial contract, the effort at Solarex was largely dedicated to building equipment and requisite processes for CIS cell and module fabrication. Generally processes were developed and optimized using small area cells, and eventually scaled up to 1000 cm^2 substrate size. Some submodule work was completed during the first contract, but a significant fraction of the total effort was expended to evaluate several different approaches to absorber deposition techniques. The features desired from the absorber deposition process have been described in the earlier contract report, and absorber deposition processes which satisfied these criteria had been partially developed by the end of the first contract.

During the time covered by this report the emphasis was largely on integration of the techniques and processes developed earlier, in the form of module development and demonstration. There was also continued scale-up and refinement of some processes, and a continued search for more cost-effective processes. Work on the absorber deposition to scale up the substrate size and to increase the process speed will be described. Work to develop reactive sputtering of Zn to give a viable, low cost and fast method of transparent contact formation was also done. Bandgap modification of the absorber layer was undertaken, following calculations which predict an advantage in module conversion efficiency for larger bandgap absorbers.

4.2 General Structure - Devices and Modules

DEVICES:
Solar cells were fabricated using the device structure:
light ⟹ Ni-Al grid/ZnO:Al/i-ZnO/CdS/CI(G)S/Mo/Glass
as shown in Figure 4.2-1.
The Mo back contact was deposited on soda lime glass substrates by DC magnetron sputtering.
The absorber layer was deposited by either by sputtering or thermal evaporation of constituents onto Mo/glass substrates, forming CIGS.

A cadmium sulfide (CdS) layer, approximately 50 nm thick, deposited by chemical bath deposition (CBD), formed a buffer layer with the absorber material. On top of the CdS, a zinc oxide (ZnO) bilayer was deposited. The bilayer was composed of an intrinsic ZnO (i-ZnO) layer approximately 50 nm thick, followed by a conductive ZnO (d-ZnO) layer, 400 - 1000 nm thick. The d-ZnO layer had a typical sheet resistance of 10-20 ohms/square and 88-94% integrated transmission in the visible spectra.

A metal grid pattern has been designed for effective current collection with the described window layer. The grids are a bilayer of Ni-Al, both deposited by e-beam evaporation through a metal mask. A photograph of a typical grid pattern is shown in Figure 5.4.1-4.

MODULES:
The CIGS module made at Solarex has a ZnO:Al/i-ZnO/CdS/CIGS/Mo/glass structure, with light incident on the top ZnO contact. Serial interconnects between module segments are formed by three separate scribes; 1) the substrate scribe through the Mo, 2) the interconnect scribe through the absorber and CdS layers, and 3) the front contact scribe through the ZnO (and absorber) layers. The scribes in the Mo and ZnO layers electrically isolate the top and bottom segment contacts from the adjacent segment. The scribe through the absorber layer forms an interconnect between the top contact of one segment and the bottom contact of the adjacent segment as shown in Figure 4.2-2.

The Mo contact substrate scribe was made using a laser, while the front contact scribe was made through mechanical means. Either laser or mechanical scribing techniques were used to form the serial interconnects. In order to minimize module power losses, optimization of several parameters were necessary. They included; 1) top contact resistivity and transparency, 2) segment width, and 3) scribe or interconnect width.

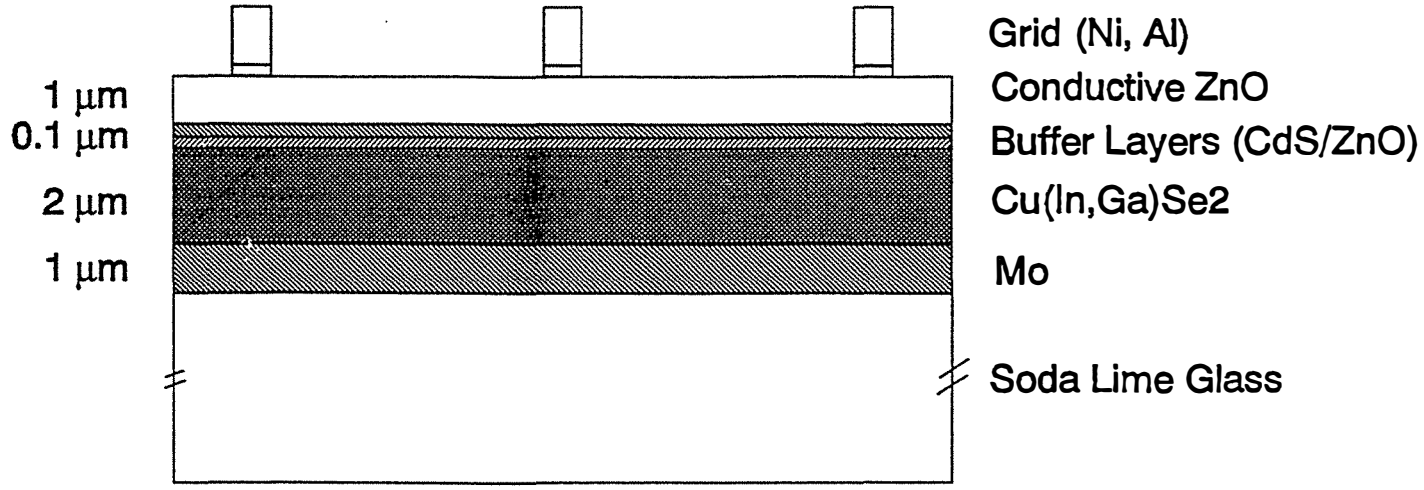


Figure 4.2.1 *Schematic view of $Cu(In,Ga)Se_2$ based solar cell device structure.*

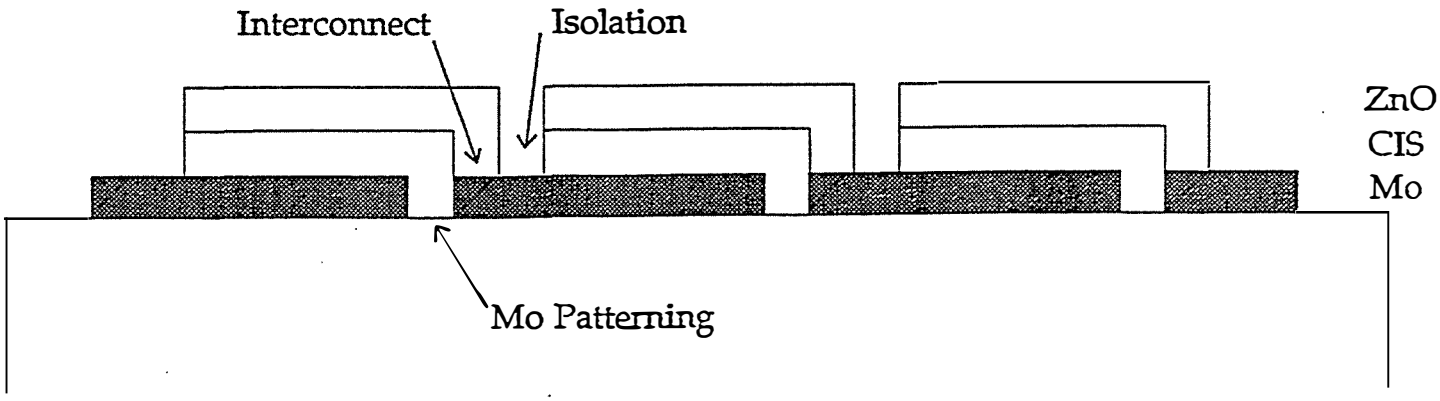


Figure 4.2.2 *Schematic view of standard module patterning structure.*

5. Technical Program

5.1 Overview

The goal of the program, originally intended to be three years in duration, was to develop all the processes and technologies required for low cost, manufacturable, large area CIS based modules. The program was parsed into one-year phases, each having tasks related to (1) Substrate, Contacts, Window Layers, (2) CIGSS or CIGS Absorber Layer, (3) Devices and Matrices of Devices and (4) Submodules, Interconnects and Module Processing.

Phase 1 was expected to address performance enhancement using devices and small submodules (3" x 3" substrates). Critical issues, such as substrate cleaning and preparation, Mo deposition and scribing were to be explored. Absorber optimization, including bandgap modification through the addition of Ga or S was to be investigated. Work to optimize buffer layers and window layers was scheduled, including exploratory work to develop a "dry process" for Cd-free (or alternate) buffer layers. Module processing was also to be developed, including evaluation and development of alternate schemes for forming module interconnects.

Major milestones for Phase 1 included;

1) Selection of the "best" processes for absorber deposition considering source material, physical vapor-deposition method, and process sequence.

2) Demonstration of a 15% efficient device, and a chain of ten adjacent devices having 13% average efficiency.

3) Fabrication of functional submodules on 3" x 3" substrates.

4) Achievement of a 12% efficient 2.5" x 2.5" submodule.

5) Establishment of an absorber deposition process having excellent tolerance to process variations and to defects.

6) Fabricate matrices of devices on 9" x 9" substrates.

All of the above milestones for Phase 1 were met or exceeded. Notable results include the fabrication of a 15.5% efficient device (total area basis) and a 13% efficient submodule (aperture area basis), confirmed by NREL to satisfy milestones 2 and 4 respectively. Regarding the last milestone in Phase 1, single 9" x 9" substrates were not used, however, matrices of devices were fabricated over a 9" x 9" area using nine 3" x 3" substrates in single depositions. These typically resulted in devices over the entire 9" x 9" area having efficiencies in the range of 12% to 14%.

Work in Phase 2 was expected to scale up and address cleaning issues for larger (9" x 9") substrates, to pursue and optimize the Na interaction with CIGS if appropriate, to evaluate reproducibility of the Mo contact and to minimize the required Mo thickness for submodules. The reproducibility, uniformity and stability of window layers for 9" x 9" substrates was to be evaluated. One of the most critical tasks to be accomplished in Phase 2 was the scale-up of the "best" absorber deposition process to 9" x 9" size, and to evaluate the resulting large area films for process tolerance, defect tolerance and spatial uniformity. Work was then expected to proceed with evaluation of 9" x 9" areas using devices and modules, leading to routine processing of 9" x 9" modules in statistically significant quantities and evaluation of yield and reproducibility of large area modules.

Some of these milestones were met before the contract was ended. Specifically, the critical task of absorber deposition on 9" x 9" area substrates was successfully accomplished, and evaluated on a preliminary basis for uniformity. Some work was performed on the role of Na in the absorber layer, but the device and submodule work done to date indicated that the introduction of Na in addition to what was available from the glass substrate was unnecessary to meet the performance goals. The uniformity of the window layer on 9" x 9" substrates was determined to be satisfactory, and the reproducibility and stability seemed adequate in cursory tests.

Phase 3 was devoted to optimization of cost and performance of constituent layers of large area modules with respect to source purity, deposition rates and fabrication times, and materials utilization. Thorough evaluation of process yields, costs and performance was scheduled during this phase.

Despite discontinuation of the contract at an early date several important inroads were also made on Phase 3 tasks. Dramatic reductions in absorber layer deposition times (to 10 to 20 minutes) were developed and demonstrated to produce CIGS of good quality. In addition a faster and more cost effective process for deposition of highly conductive ZnO for window layer use was demonstrated

5.2 Window Layers

The window layers were deposited in the following sequence:

1) first, a CdS buffer layer was deposited by CBD to a nominal thickness of 50 nm,
2) next, the i-ZnO layer, approximately 50 nm, was deposited on the CdS by RF Sputtering, this layer is often considered part of the buffer layer, and
3) the final window layer, a low resistance ZnO (d-ZnO) film, was RF sputtered, film thicknesses ranged from 400 nm to 1000 nm; this layer provided the optical transmission and electrical conductivity needed for solar energy conversion and current collection.

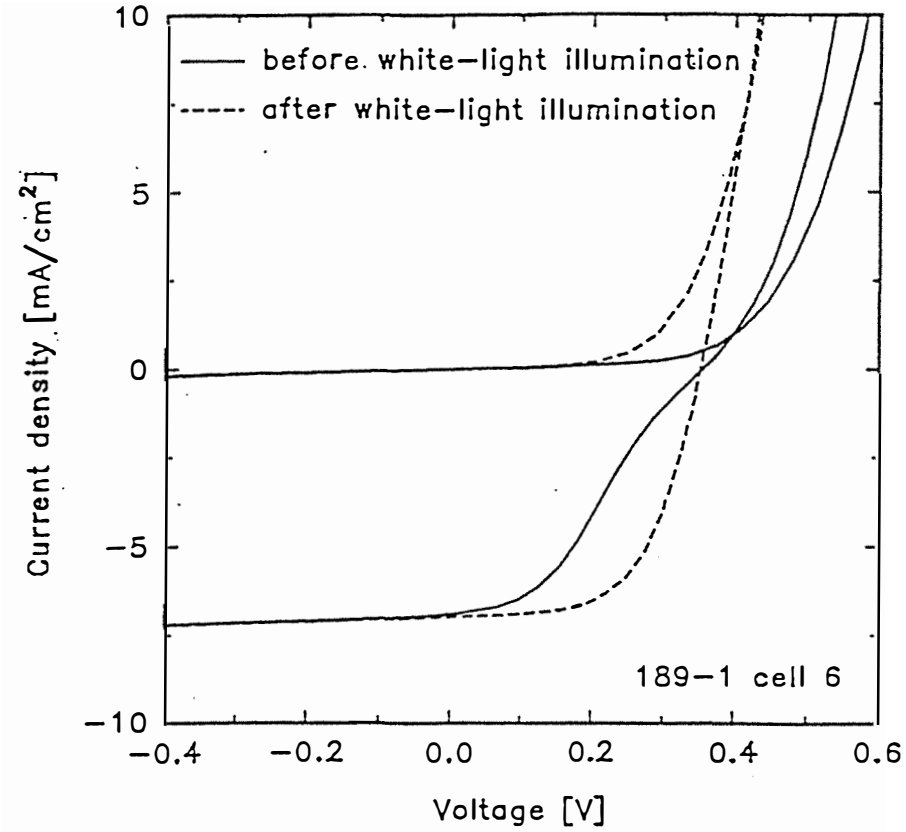
The precise role the CdS and i-ZnO buffer layers play in solar cell design is not completely understood, but some form of buffer layer appears to be a necessary component of a successful solar cell. In Phase 1 of this contract, the interactive role of the buffer layers, as well as improvements in the electrical and optical properties of the d-ZnO layer were to be explored.

5.2.1 The Buffer Layers

The CdS buffer layer was deposited by a CBD process [4,5]. It is a batch chemical process that provides exceptional coverage and the reasonable control of the thin film thicknesses needed for CIS devices and modules. Uniform coverage up to 1000 cm^2 has been demonstrated.

At Solarex, two variations of the CBD process have been used. Both CBD processes have similar chemical make-up and vary only in when and how the chemicals are mixed. In collaborations with Colorado State University and Pennsylvania State University [6,7], it has been shown that one CBD process was responsible for a non-standard junction behavior as seen in the J-V characteristics of CIGS devices. The difference in junction behavior occurred when the device illumination was void of photons that could be absorbed in the CdS layer (< 550 nm). This resulted in a 'kinked' appearance in the J-V characteristics. Examples of J-V plots are shown in Figure 5.2.1-1a and 1b. Here the J-V curves are plotted for (1a) dark and red light after white light illumination and (1b) as a function of the time the device was exposed was kept in the dark after exposure to white light. (Measurements made a Colorado State University). A more extensive discussions of the physics of this non-standard diode behavior can be found in References 6 and 7.

a)



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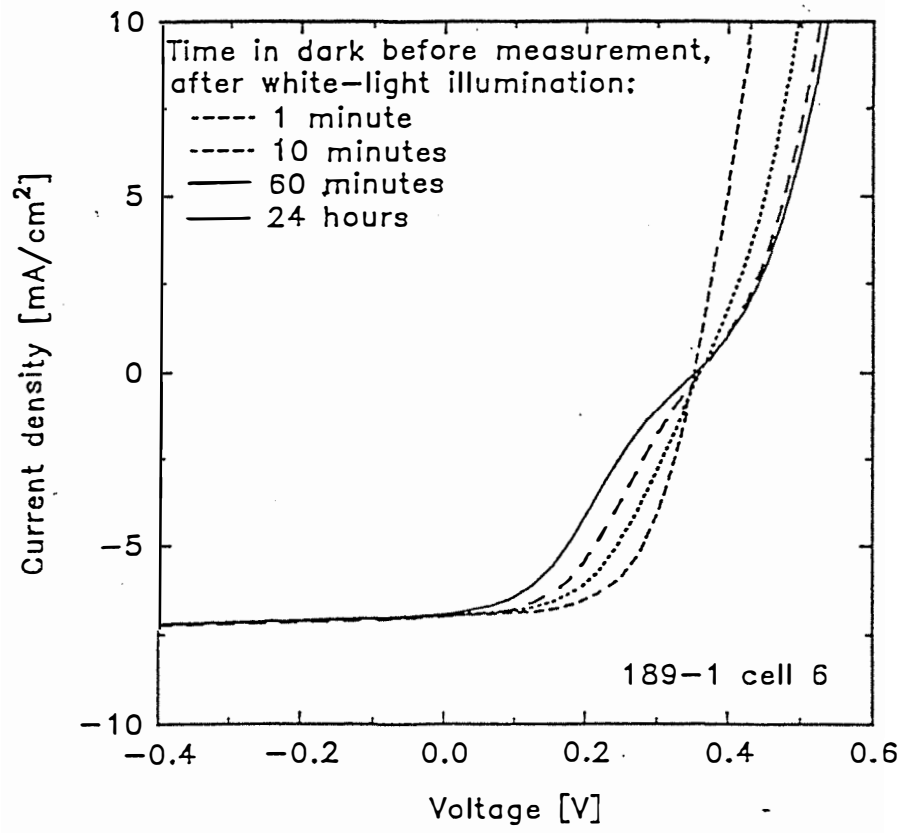


Figure 5.2.1-1. *a) Dark and red light J-V curves before and after white light illumination. b) Red light J-V curves as a function of the time after white light illumination. (Measurement made at Colorado State University)*

Understanding how the i-ZnO layer interacts with CdS and CIGS is essential in obtaining the maximum efficiency available from modules and devices. Also of interest is the possible elimination or replacement of the CdS buffer layer with a 'dry' chemical process. Intrinsic ZnO is a possible alternative. For typical solar cell applications, the intrinsic ZnO layer was deposited from either an undoped pure ZnO target in the presence of an argon plasma or from an aluminum doped ZnO target where oxygen was contained in the sputtering gas. Although both films had similar optical and electrical properties on glass substrates, and both were very transparent and highly resistive, when part of a device, their behavior was very different [8].
To better understand the role of the i-ZnO layer, films with and without oxygen in the plasma gas, were tested on devices made using different thicknesses of CdS. Device efficiencies are summarized in Table 5.2.1-1 and the J-V characteristics, as a function of CdS thickness are shown in Figure 5.2.1-2.

CdS b:ZnO	none	very thin	thin	thick	very thick
none	dead	9.48	11.37	12.31	11.98
with O_2	dead	5.88	10.52	12.49	12.26
without O_2	6.52	11.28	11.45	12.53	11.90

Table 5.2.1-1. *Solar cell efficiency averages of 15 to 20 device for each CdS thickness and each high resistive i-ZnO layer deposition process. (Details between the efficiencies for the different CdS thicknesses should not be concluded as each CdS deposition is performed on a different sample of CIGS).*

When the CdS was thick, the device was not only insensitive to the source of i-ZnO, but also to the need of the i-ZnO film. As the CdS becomes thinner, the presence of oxygen in the plasma gas began to have detrimental effect on the photovoltaic properties, as seen in the lower device efficiencies when compared with the oxygen free situation. And in the extreme case of a CdS-free device, the only marginally successful results occurred when the i-ZnO was deposited from a pure argon plasma. The data suggests that not all intrinsic zinc oxides are equivalent and that for supplantation of CdS, ZnO made in oxygen-free conditions may be superior to that made with oxygen present. Further refinement of the process is necessary if i-ZnO is to be considered as a suitable substitute to CdS.

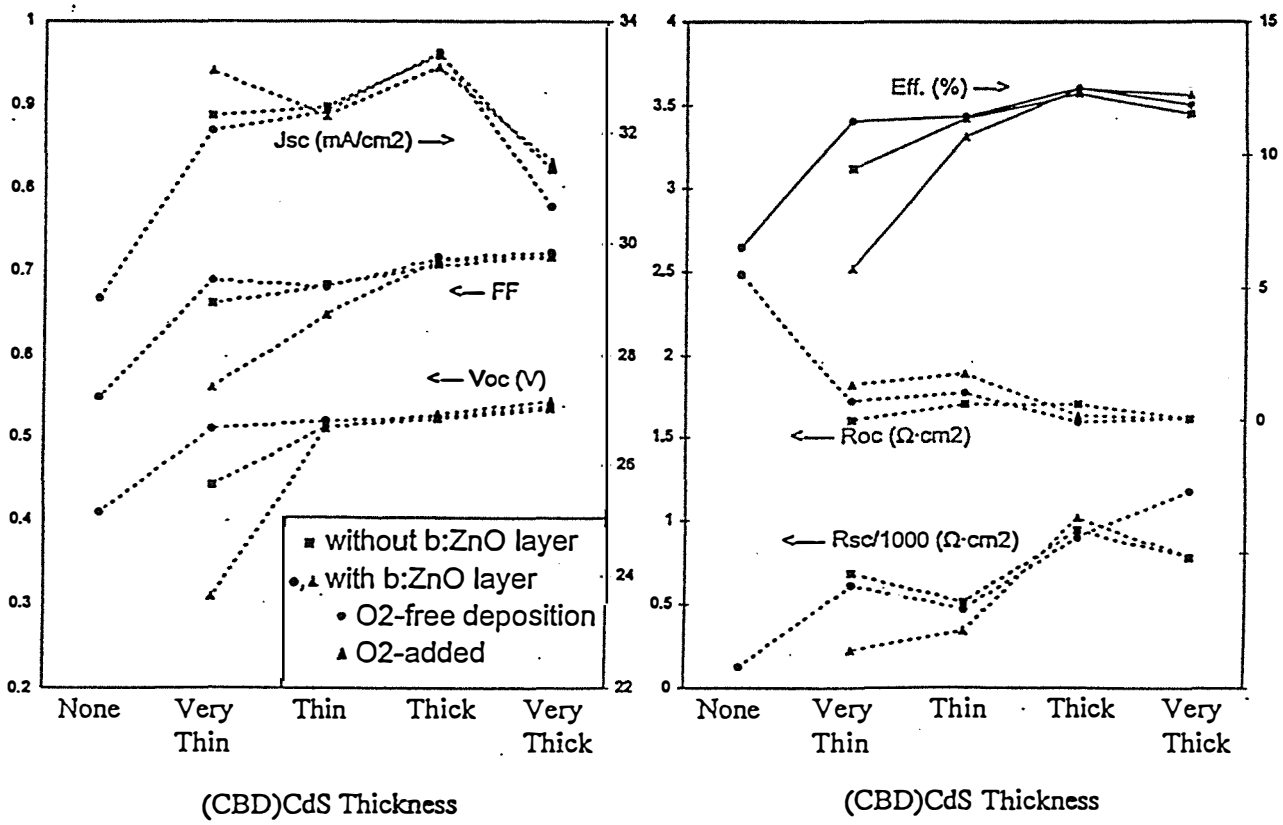


Figure 5.2.1-2. *The photovoltaic parameters of cells made with two types of high resistivity ZnO and using several thickness of CBD CdS.*

5.2.2 The TCO: Low Resistivity ZnO Layer

For typical device and module applications, a low resistivity ZnO film was RF sputtered from a doped ZnO target. The electrical and optical properties of the films were controlled by alterations in the film thickness and dopant concentration. Highly conductive ZnO films can be made, but at the expense of the long wavelength transmission where free carrier absorption effects dominate [8]. Plots of current loss vs. sheet resistance were used to analyze the co-dependent behavior of ZnO's optical and electrical properties. Current loss is defined as the integration over the wavelength of the measured film's optical absorption multiplied by the available solar spectrum and by the quantum efficiency of a typical device, i.e., an absorber of 1.17 eV. An example of a current loss plot for three different RF sputtering processes of d-ZnO is shown in Figure 5.2.2-1. In this Figure it is seen that conductivity, comes at the expense of optical transmission resulting in significant current loss. In order to gain a better understanding of the behavior of d-ZnO, research focused on the following areas: 1) how do are the film requirements for modules and devices differ, 2) how does d-ZnO behave on substrates other than glass and 3) is there a fast, low cost alternative to RF sputtered ZnO presently used.

In module fabrication, the need for a conductive ZnO layer with exceptional optical transmission cannot be overemphasized. Unlike a device where a narrowly spaced grid pattern provides adequate current collection, a module requires a much more conductive front contact since its lateral current collection abilities are restricted by the width of the segments. Until an absorber with a sufficiently wide bandgap, can be made, this problem will exist. Section 5.3.1 of this report, explores the potential advantages of using wide bandgap absorbers along and how the d-ZnO requirements effect the PV characteristics such absorbers.

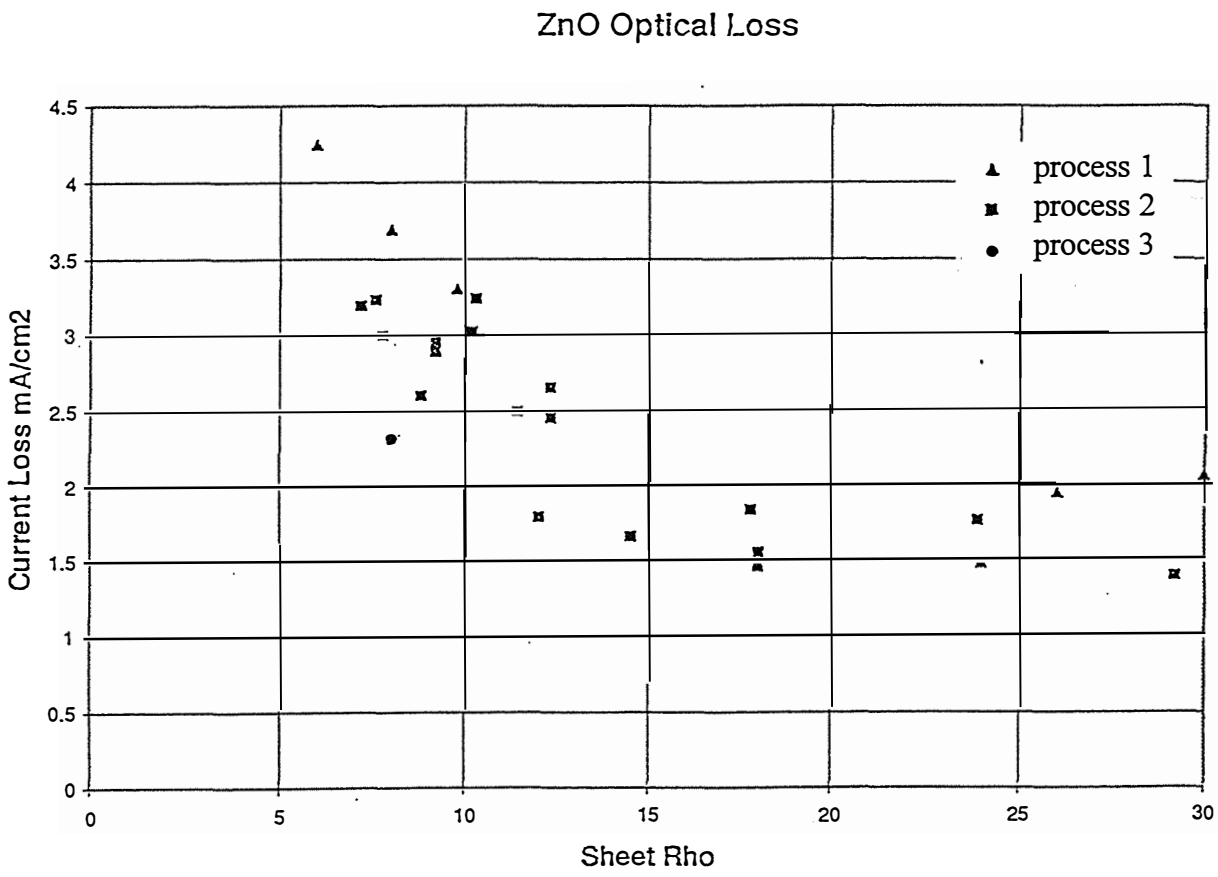


Figure 5.2.2-1. *Characterization of the optical versus electrical properties of transparent conductive d-ZnO. The current loss is calculated such that zero current loss corresponds to zero optical absorption of the film.*

Very often the quality of the d-ZnO film was established for a glass witness piece, with the presumption that what was deposited on the absorber layer was of similar behavior. This was not the case. In Figure 5.2.2-2, a SEM micrograph of d-ZnO grown on molybdenum and CIGS surfaces clearly showed different morphologies for the different substrate material. Although not shown, films grown directly on glass resemble those grown on molybdenum. Differences were also seen in XRD measurements, Figure 5.2.2-3, that show d-ZnO grown on glass to be highly (002) oriented, while films grown on CIGS have a more random orientation concurring that the ZnO is of different crystal structure.

These differences extend into the electrical and optical properties as well. Substrate effects on the conductivity and optical absorption of d-ZnO were seen when d-ZnO, deposited on: 1) glass, 2) thick CdS and 3) thin CdS substrates were compared. The thin CdS being the thickness normally used for devices and the thick CdS being twice that amount. In Figure 5.2.2-4, a Box And Whisker plot shows the statistical dependence of the sheet resistivity on substrate type. In this plot, the median value is shown by the central horizontal line, the large box is the estimated limit of mean to a 95 % confidence limit and the small 'whiskers' represent the extrema in data. The samples with thick and thin CdS also had, on average, 35 % and 84 %, higher sheet resistance, respectively, than the glass substrate.

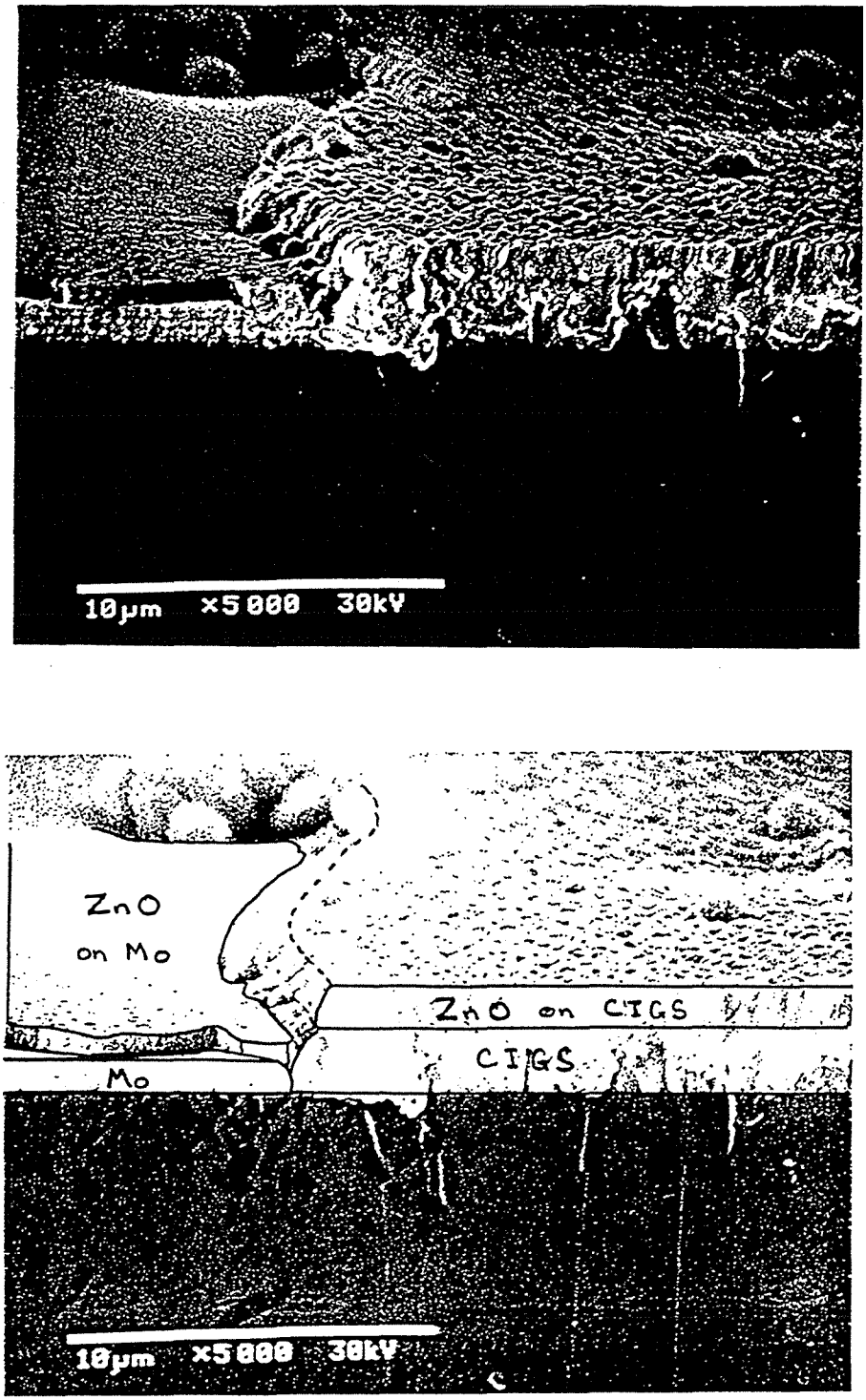
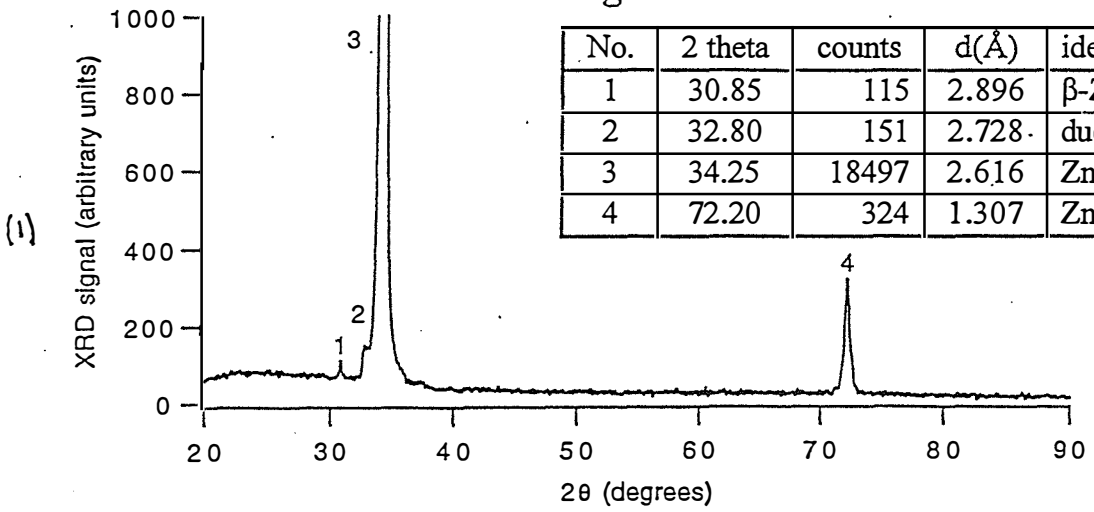
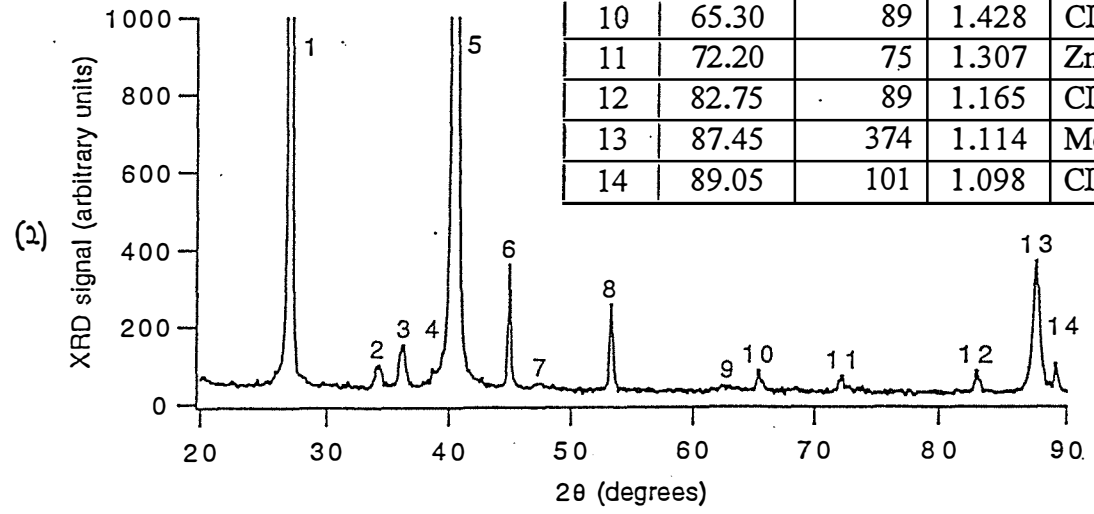


Figure 5.2.2-2. *SEM micrograph of d-ZnO on CIGS and Mo/glass substrates.*

Fig. 2



No.	2 theta	counts	d(Å)	identification
1	30.85	115	2.896	β-ZnO(002)
2	32.80	151	2.728	due to W
3	34.25	18497	2.616	ZnO(002)
4	72.20	324	1.307	ZnO(004)



No.	2 theta	counts	d(Å)	identification
1	27.05	4938	3.294	CIGS(112)
2	34.25	106	2.616	ZnO(002)
3	36.35	157	2.469	CIGS(211)
4	38.70	91	2.325	due to W
5	40.45	6995	2.228	Mo(110)
6	44.90	363	2.017	CIGS(220)
7	47.55	58	1.911	ZnO(102)
8	53.15	260	1.722	CIGS(312)
9	62.85	50	1.477	ZnO(103)
10	65.30	89	1.428	CIGS(400)
11	72.20	75	1.307	ZnO(004)
12	82.75	89	1.165	CIGS(424)
13	87.45	374	1.114	Mo(220)
14	89.05	101	1.098	CIGS(336)

Figure 5.2.2-3. *XRD patterns of (1) d-ZnO/glass substrate and (2) d-ZnO/CIGS based device, the main ZnO peaks are (002) at 34.2° and (004) at 72.2°.*

Improvements in the long wavelength transparency occurred when the d-ZnO was deposited on CdS substrates. Since the ZnO on CdS was also less conductive, the question arose concerning the possible reduction in free carrier density. In comparing the amplitude of the change in sheet conductivity to that of the long wavelength absorption, and assuming equal film thickness, it appears questionable that all of the differences lie in the free carrier density. The idea that the sheet conductivity for the ZnO on the CdS can be compensated by producing thicker films which would result in the same IR optical properties as ZnO on bare glass is criticized. In Figure 5.2.2-5, the optical absorption at 1300 nm is plotted as a function of sheet conductivity. Although the statistics to noise ratio is poor, the three types of samples appear to distinguish themselves and the following argument is made:

If it is true that the dominant absorption mechanism at 1300 nm is that of free carriers and the absorption coefficient (α) can be written [9]:

$\alpha = (n/\mu)f(x_1)$ where $f(x_1)$ is a function independent of n, μ and d

n = free carrier density
μ = mobility
d = film thickness
e = electron charge

The film absorption is $A = 1 - \exp(-\alpha d) \approx \alpha d$ for $\alpha d << 1 \Rightarrow A \approx (nd/\mu)f(x_1)$ (1)

If the sheet conductivity is θ_s then $\theta_s = nd\mu e$, then $\Rightarrow nd = \theta_s/\mu e$ (2)

therefore, when $A \approx \alpha d$ then $A \approx \theta_s \mu^{-2} e^{-1} f(x_1)$ and then define $g(x_1) \equiv e^{-1} f(x_1)$

which leads to the approximation: $\Delta A/\Delta\theta_s \approx \mu^{-2} g(x_1)$ for $\alpha d << 1$ (3)

Equation (3) is graphically represented in Figure 5.2.2-5 where A is plotted versus θ_s for a given wavelength (1300 nm) with sufficiently small values of A (A is as large as 0.5 in Figure 5.2.2-5 but the approximation is still considered acceptable). For a given value of μ, variations of nd will result in the linear behavior of A versus θ_s. Different values of μ will lead to different slopes of the linear relationship, which in all cases intercept the origin. Linearization of the data sets of Figure 5.2.2-5, suggested that the ZnO grown on CdS coated substrates differ from ZnO grown on bare glass by more than the resulting film thickness and free carrier densities alone. It is suspected that a decrease in free carrier mobility occurs when CdS is present.

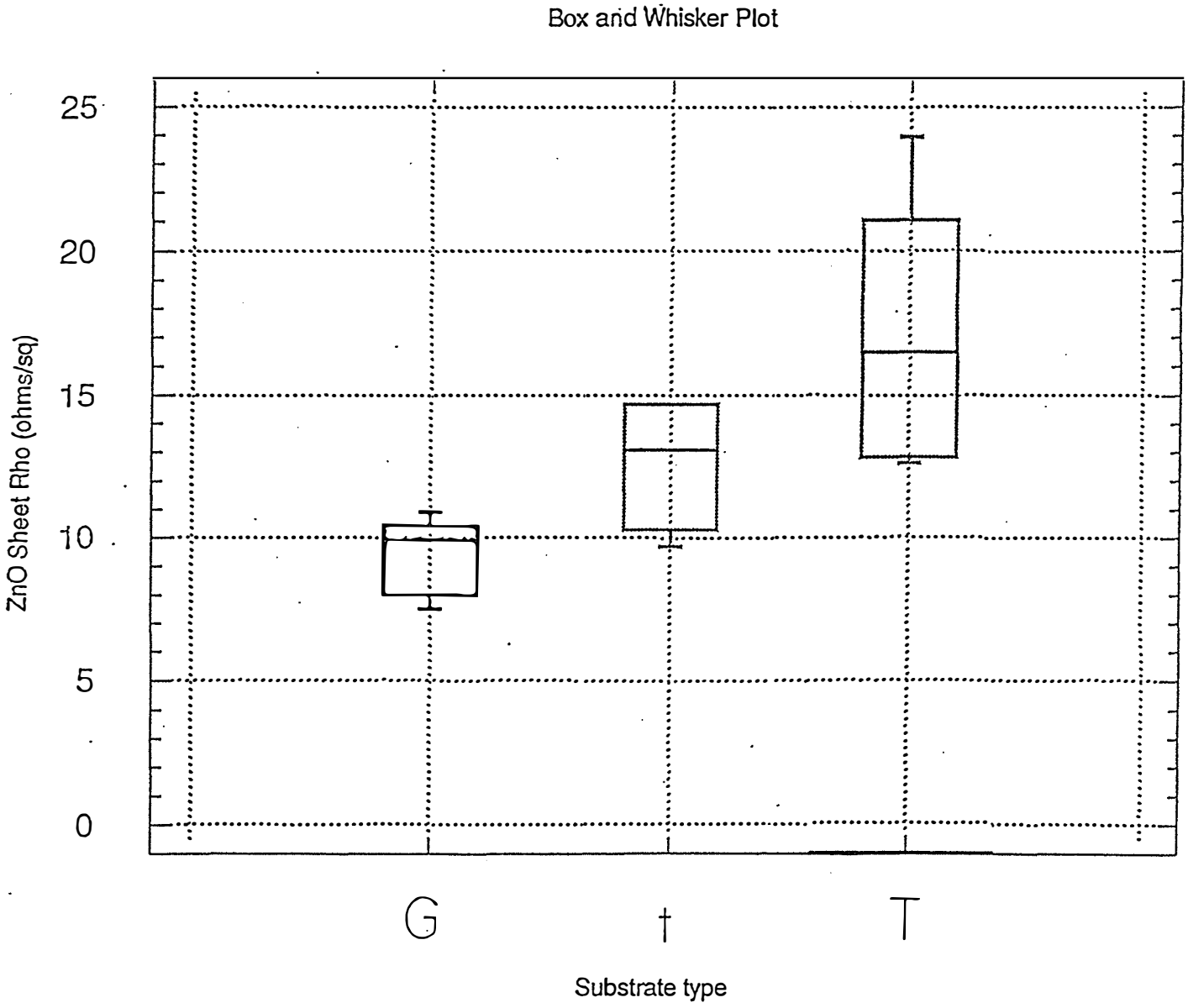


Figure 5.2.2-4. *Box and whisker plot of the statistical dependence of sheet resistivity on the substrate type. The statistical sample size and substrate type are identified as: G - glass substrate, 15 samples; t - thin CdS substrate, 6 samples; and T - thick CdS substrate, 6 samples.*

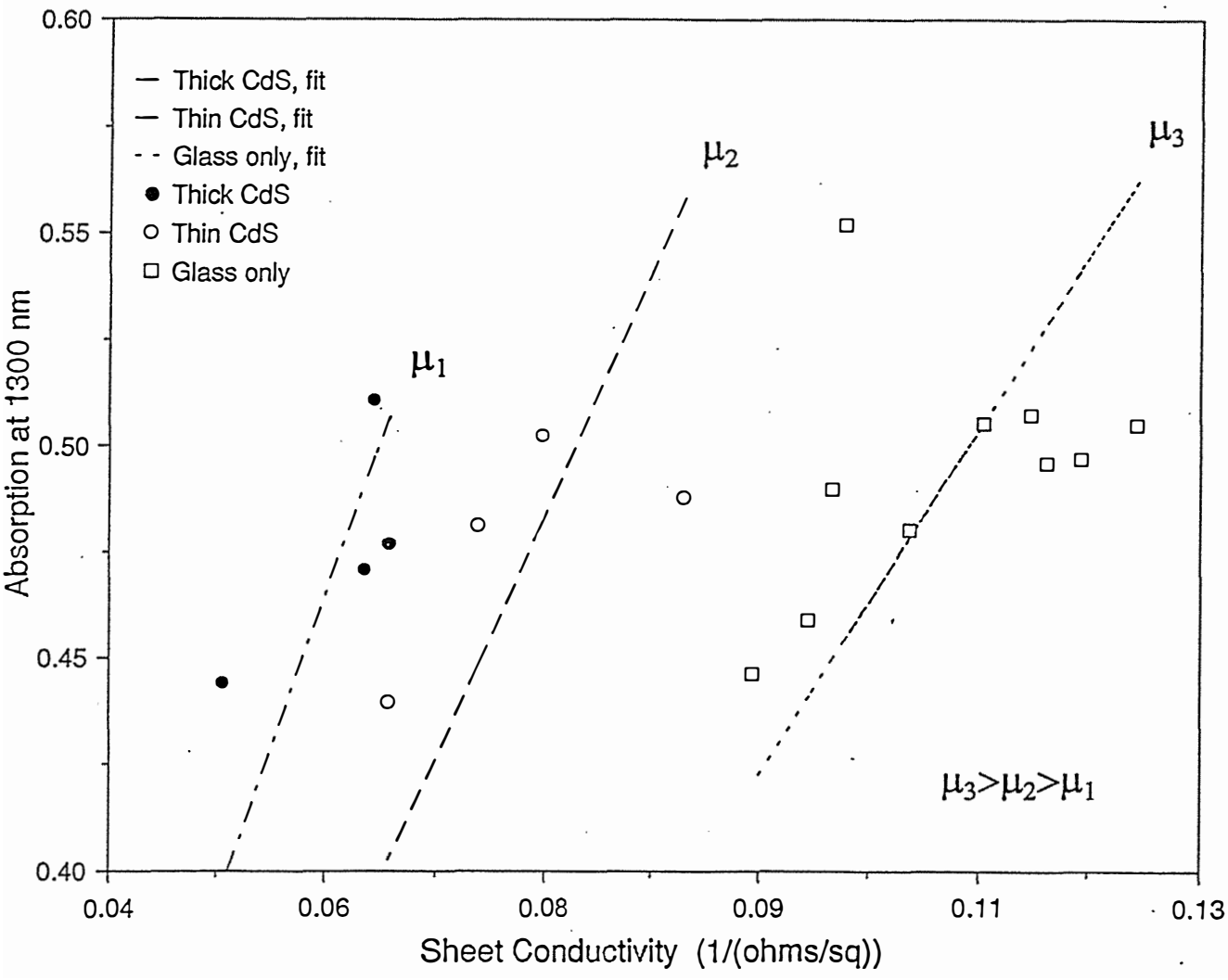


Figure 5.2.2-5. *Optical absorption of low resistivity ZnO films at 1300 nm versus sheet conductivity for G, t, and T samples of Figure 5.2.2-4. If each linear fit represent variation of nd for constant values of* μ *then,* μ_1 μ_2 *and* μ_3 *are ordered as shown in the bottom right corner of the plot.*

In an effort to improve ZnO quality, while reducing material costs and deposition times, reactive sputtering of a metallic zinc target in a plasma containing a partial pressure of oxygen was investigated. The reactive process yielded films with sheet resistance as low as 3.4 ohms/square and excellent optical transmission in the visible spectrum. In Figure 5.2.2-6, the optical characteristics of a reactively sputtered ZnO film is shown. Figure 5.2.2-7 compares the current loss behavior of the reactive process with that of the RF sputtered process normally used in device and module fabrication. The reactively sputtered ZnO films have current losses comparable to or better than those RF sputtered from a ceramic ZnO target. Optical losses in the infrared region are still a significant problem with both processes, but avoidable through the use of a wide band gap absorber layer. A module, using a top contact with a sheet resistivity of 3.4 ohms/square would have excellent current collection, permitting the use of wider segments and fewer interconnects.

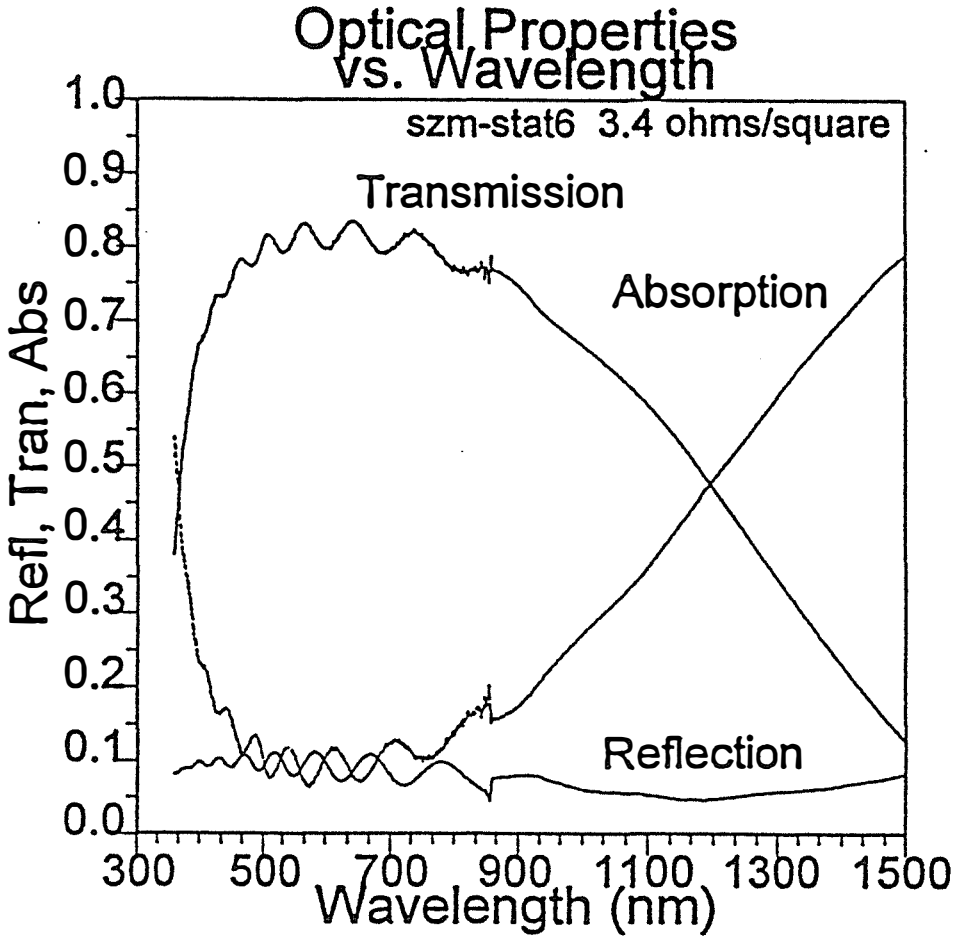


Figure 5.2.2-6. *Optical absorption, transmission and reflection of a highly conductive reactively sputtered ZnO film.*

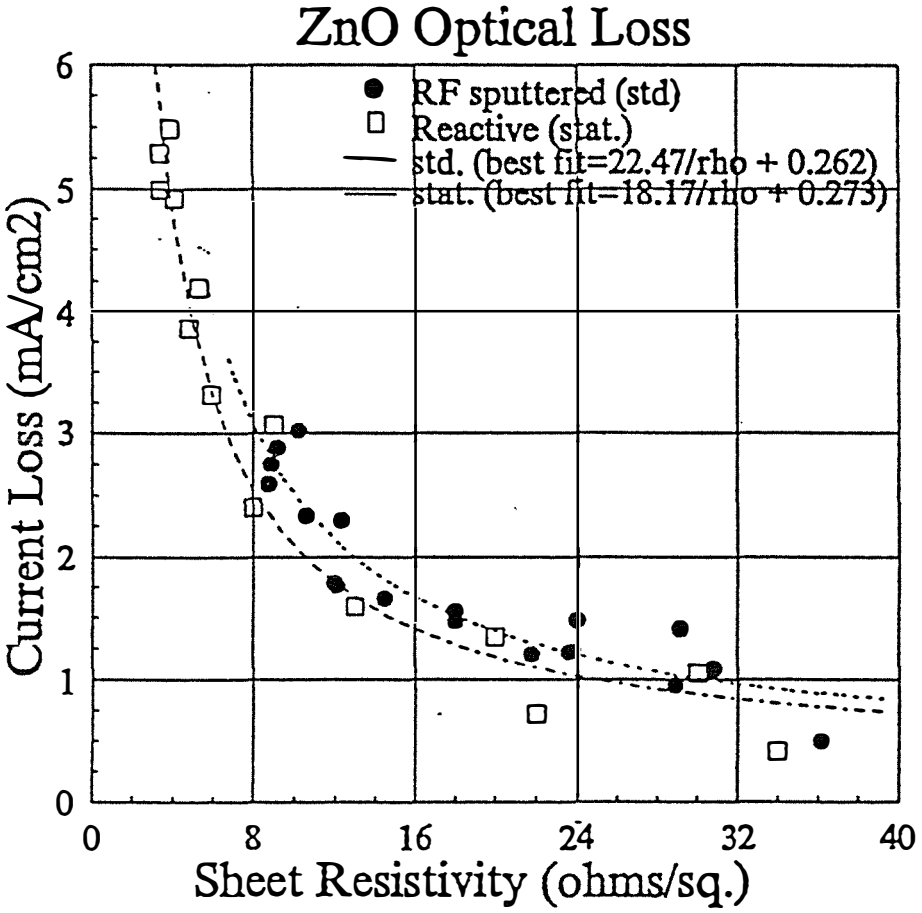


Figure 5.2.2-7. *ZnO current loss due to optical absorption of (1) a reactively sputtered ZnO film and (2) a RF sputtered ZnO film.*

5.3 Absorber Layers

The absorber layer deposition methods investigated earlier at Solarex included sputtering from the metallic constituents followed by selenization, sputtering and/or evaporation of binary compounds along with elemental constituents sequentially followed by selenization and co-evaporation of elemental components concurrent with selenization. The latter process most easily yielded CIGS devices and modules having high efficiency. Additionally, the adhesion and tolerance to variation and substrate defects was very good, and the factors governing cost and scalability did not present undue difficulty. This latter process was selected over the others as a focus of efforts after consideration of all factors.

5.3.1 Absorber Bandgap Modification

The bandgap adjustment obtained by addition of Ga represented one variable which was addressed through calculation and experimentation. From a device point of view, it may appear that little is to be gained by raising the bandgap of the absorber above 1.16 eV because the photon flux present in the solar spectrum which is not absorbed becomes significant. From the standpoint of modules, however, lateral collection effects through the front contact are also a significant factor. A wide bandgap absorber producing a higher voltage output but with less current at the maximum power point is desirable in that case. Module structures having a large segment width are desirable to minimize total area loss and manufacturing throughput, and the desirability of higher bandgap absorbers increases for larger values of segment width. The magnitude of this effect is shown in Figure 5.3.1-1 for three different bandgap absorbers and two values of module segment width using a calculation model described elsewhere [10]. In this Figure, the absorber material is assumed to yield devices having 15% efficiency irrespective of bandgap. This work has been described in more detail [8]. The advantage of larger bandgap absorbers for module structures is due in part to a reduced current density carried laterally in the window contact (thus reduced lateral voltage drops), and in part due to a reduced response to long wavelength excitation where the ZnO window contact is most absorbing. This latter effect is shown in Figure 5.3.1-2. It is apparent that a substantial gain in module efficiency will result through the use of a larger bandgap absorber in a module structure having reasonable segment widths.

Recently there has been much progress in making high quality, large bandgap CIGS [3] as evidenced by small area devices exhibiting > 15% efficiency with over 700 mV Voc. The absorber deposition process used at Solarex has been adjusted to incorporate more Ga, and has also yielded promising results. Arrays of devices have been made under various conditions which have Ga/(In+Ga) of between 0.40 and 0.50. Figure 5.3.1-3 shows the J-V characteristic of a larger bandgap device with almost 700 mV Voc and 14.6% (total area) efficiency. The effect of all process parameters during absorber deposition at increased levels of Ga have not been fully determined, and the bulk of the modules fabricated at Solarex have been with absorber material having about 25% - 30% Ga/(In+Ga) and a bandgap of 1.16 eV. Nevertheless, the addition of Ga appears to be a promising path toward increasing module efficiency, and, concurrently reducing requirements for narrow segment widths in module structures.

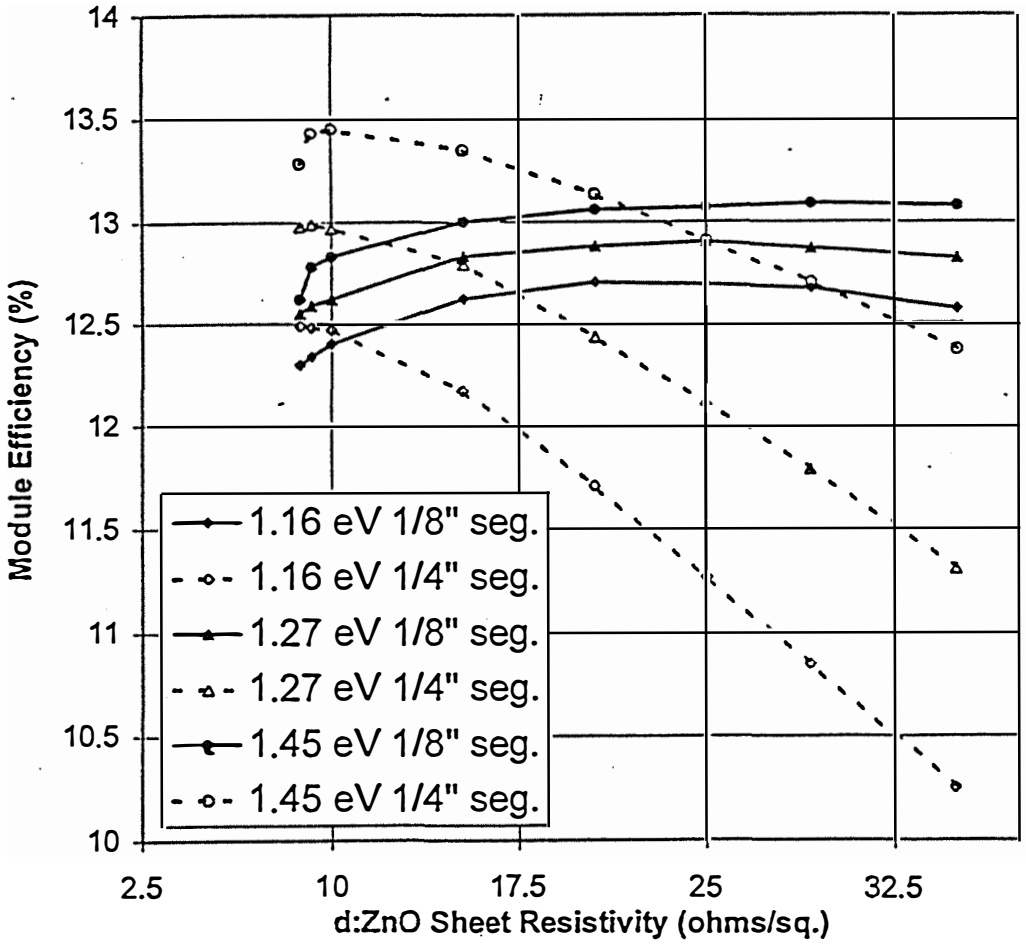


Figure 5.3.1-1. *Expected module efficiency vs. ZnO sheet resistivity for 1/8" and 1/4" segment widths and for three different absorber bandgaps (1.16 eV, 1.27 eV and 1.45 eV).*

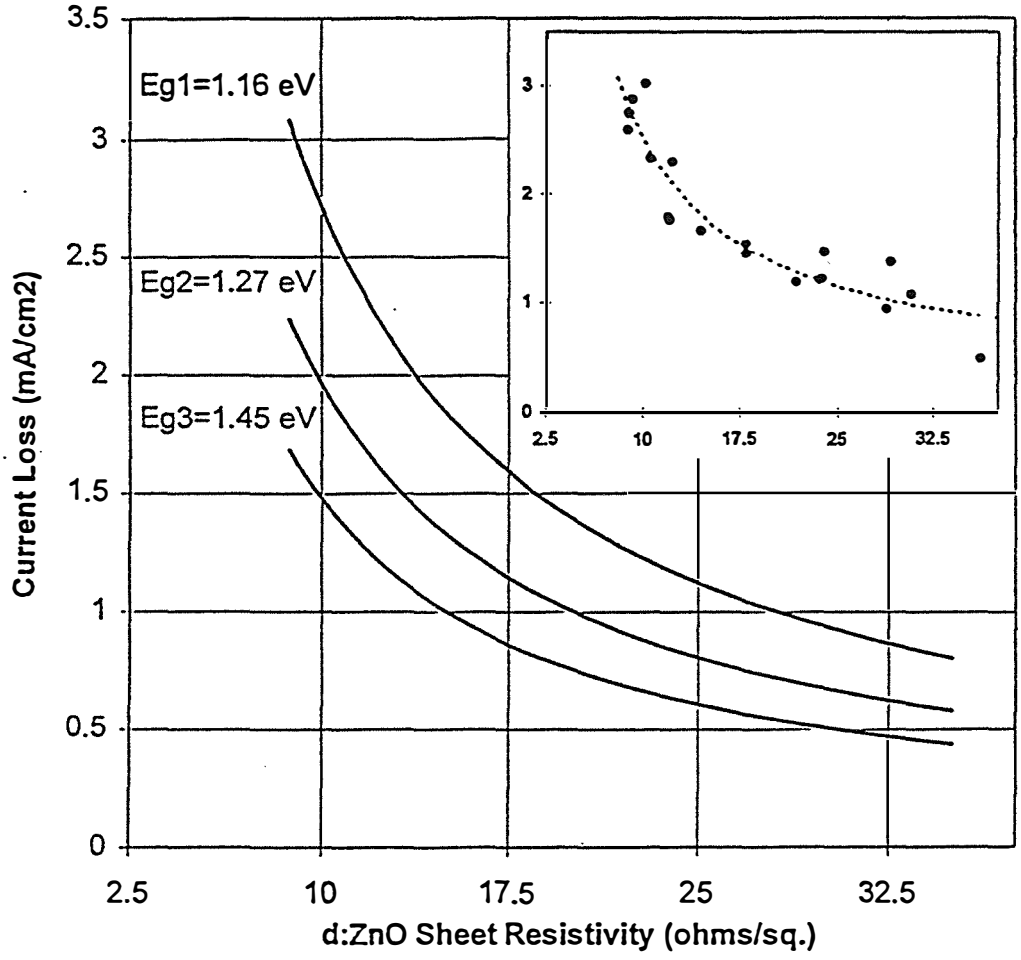
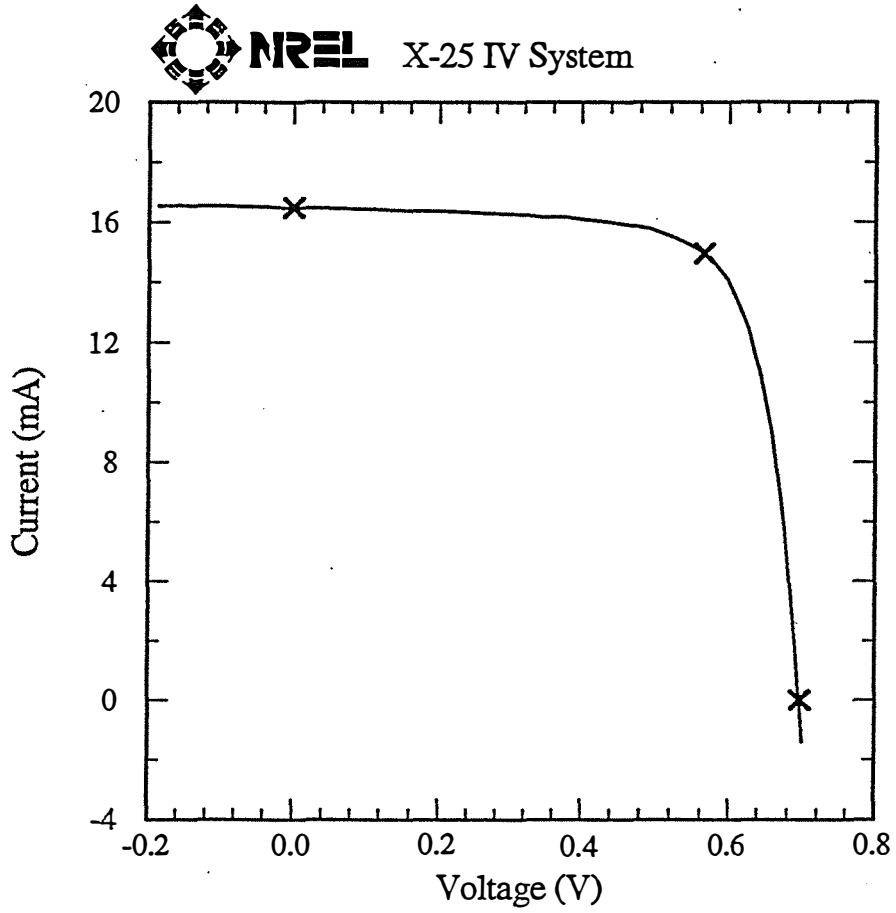


Figure 5.3.1-2. *Calculated current loss due to optical absorption in the ZnO window layer vs. sheet resistivity for three different absorber bandgaps (1.16 eV, 1.27 eV and 1.45 eV). Inset shows the analytical regression of the QE(λ) characteristics of the three different bandgap absorbers.*

Solarex $ZnO/Cu(In,Ga)Se_2$

Sample: SA97C (Top)
Dec 11, 1996 3:54 PM
ASTM E 892-87 Global

Temperature = 25.0°C
Area = 0.5807 cm^2
Irradiance: 1000.0 Wm^{-2}



V_{oc} = 0.6973 V
I_{sc} = 16.49 mA
J_{sc} = 28.39 $mAcm^{-2}$
Fill Factor = 73.51 %

V_{max} = 0.5653 V
I_{max} = 14.95 mA
P_{max} = 8.451 mW
Efficiency = 14.6 %

After 10 minute soak @ P_{max}., 2 minute cool.

Figure 5.3.1-3. *Current - Voltage characteristics of a small area device which has a high gallium content (wide bandgap) absorber.*

5.3.2 Absorber Process Requirements

Time and temperature are two factors of importance to the development of a commercial process for CIGS based PV modules. In a production sequence the absorber deposition step is potentially a rate limiting step. Thus, there is a clear benefit to reducing the time required to deposit the CIGS layer. Toward this end, the standard deposition process used at Solarex was simplified by the elimination of ramps in temperature and flux rates wherever possible. Additionally, total flux rates of the constituents were increased sufficiently to allow deposition of the entire CIGS layer (typically 1.5 - 2.0 microns thick) in 10 to 20 minutes [11]. The time cited here excludes substrate heat-up and cool down times, and any incidental time spent by the substrate in a chalcogen flux, as during cool down. Figure 5.3.2-1 shows the J-V behavior of the best small area cell whose CIGS layer was deposited in 20 minutes. The total area efficiency of 15.2% clearly indicates that it is possible to maintain high absorber layer quality while minimizing the deposition time required for that layer. Cell efficiencies resulting from deposition schedules of 10 minutes were comparable to the result obtained with 20 minute deposition time. More typical results for 10 and 20 minute absorber deposition times are shown for small area devices in Figures 5.3.2-2 and 5.3.2-3. Thus, this CIGS deposition process appears capable of meeting the high throughput required for commercial viability.

Temperature is important because difficulties such as substrate breakage and warping are greatly influenced by the substrate temperature. The viscosity of glass is nearly exponential with its temperature and typical substrate temperatures used in CIGS processing usually approach the annealing and strain points of soda-lime glass. Thus it is possible for thermally induced stresses, usually due to non-uniform substrate temperature, to create permanent deviations in the substrate flatness. In turn, any significant loss of substrate flatness greatly complicates subsequent module processing steps, such as scribing operations. Secondary factors exacerbated by high substrate temperature requirements include heat-up and cool-down times, heat dissipation from equipment and power consumption. At the high processing temperatures used in the standard process at Solarex for CIGS deposition, improvements in equipment design ultimately allowed the deposition of CIGS onto 9" x 9" substrates while maintaining substrate warping to 1 mm or less from edge to edge. However, lower ultimate substrate temperatures are desirable to minimize all of the above effects.

Accordingly, some preliminary investigation was made of the impact of reduced substrate deposition temperature on material quality, as evidenced by small area device efficiency. Figure 5.3.2-4 shows the efficiency of devices made using CIGS deposition at reduced temperatures. The maximum temperature monitored on the process equipment was 500 C, 475 C and 450 C for the three runs as denoted in the Figure. It should be noted that the substrate temperature was difficult to assess accurately in this apparatus, and the true substrate temperature was probably somewhat lower than that indicated. Secondly, even the highest temperature shown in this series (500 C) was lower than that used in the "standard" process at Solarex. This data indicates that, while there does appear to be a loss of device efficiency with reduction in temperature, the functional dependence is not rapid or catastrophic over a significant range. It is all the more remarkable in that the cells in

this series had a relatively high gallium content (Ga/(Ga+In) ~ 0.35), and higher gallium content CIGS might be expected to require deposition temperatures higher than those normally used for CIS [3]. On a preliminary basis, reduction of substrate temperature appears to be a viable option in a production scenario to minimize problems originating with thermal requirements during the absorber deposition step.

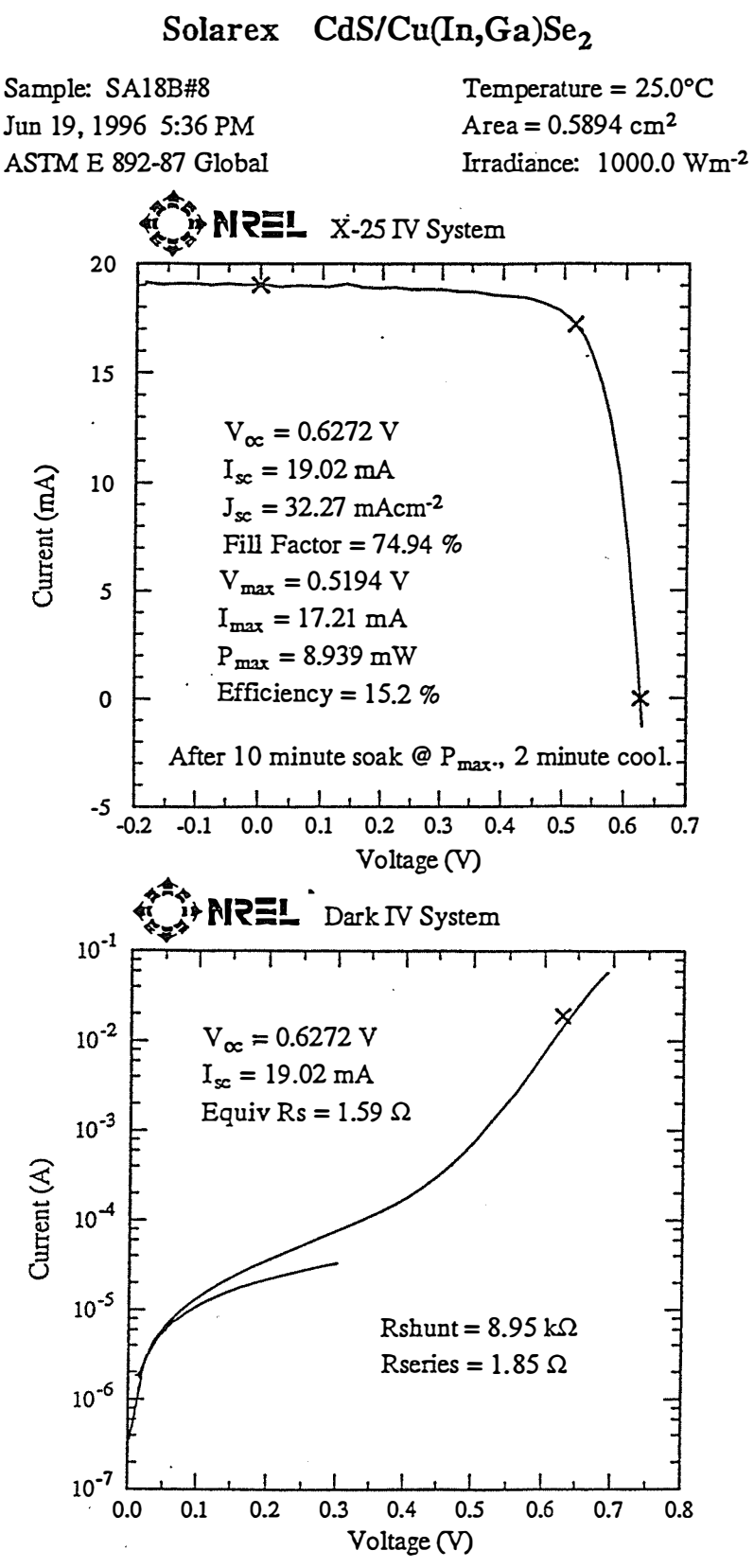


Figure 5.3.2-1. *Current - Voltage characteristics of a small area device made using a total deposition time for CIGS absorber layer (metal fluxes only) of 20 minutes.*

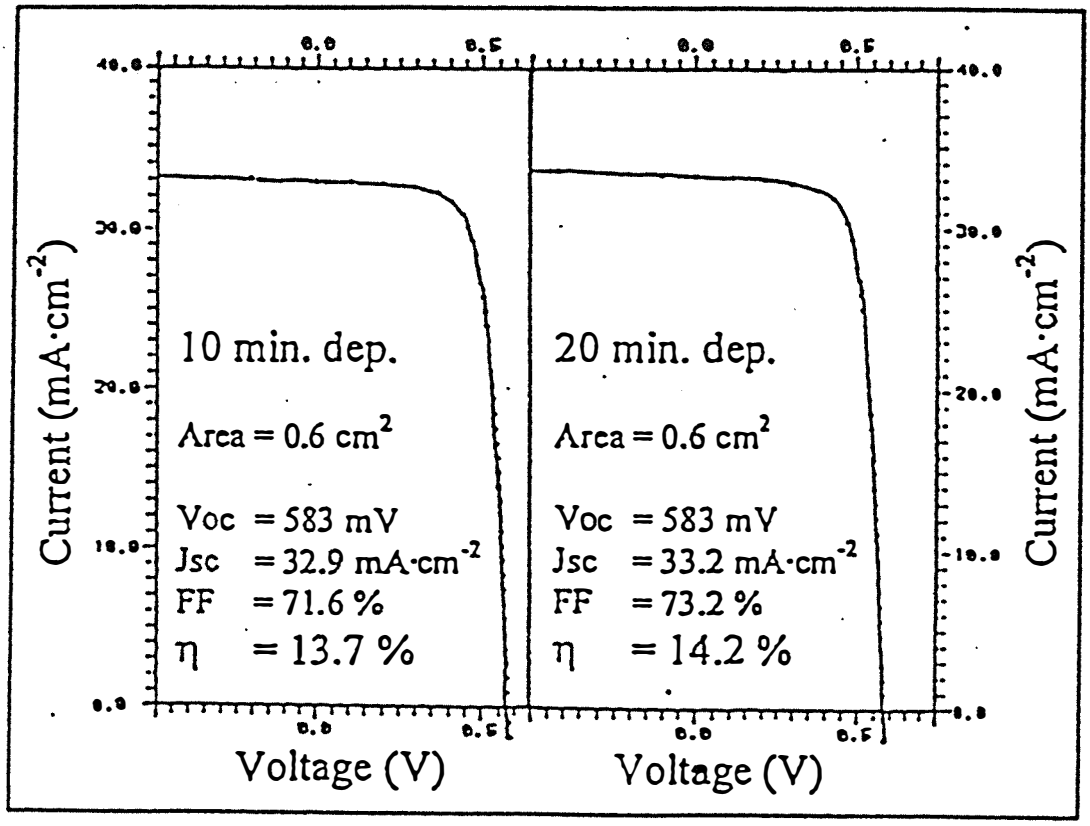


Figure 5.3.2-2. *A comparison of the current - voltage characteristics of small area devices made using absorber deposition times (metal fluxes only) of 10 and 20 minutes.*

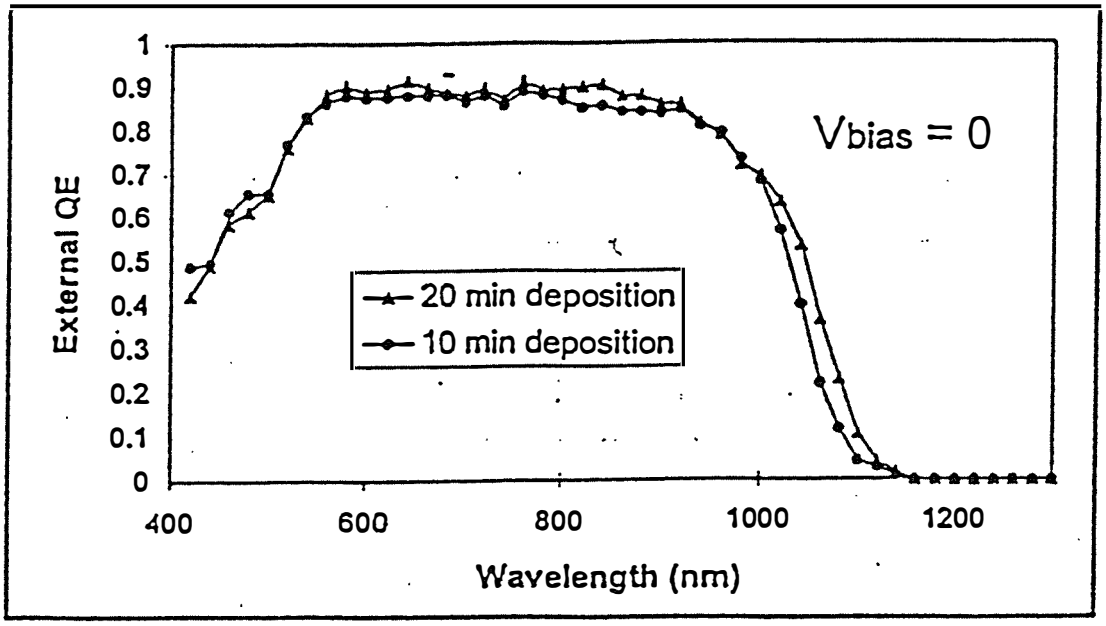


Figure 5.3.2-3. *A comparison of the quantum efficiency of the small area devices (J-V shown above) made using absorber deposition times (metal fluxes only) of 10 and 20 minutes.*

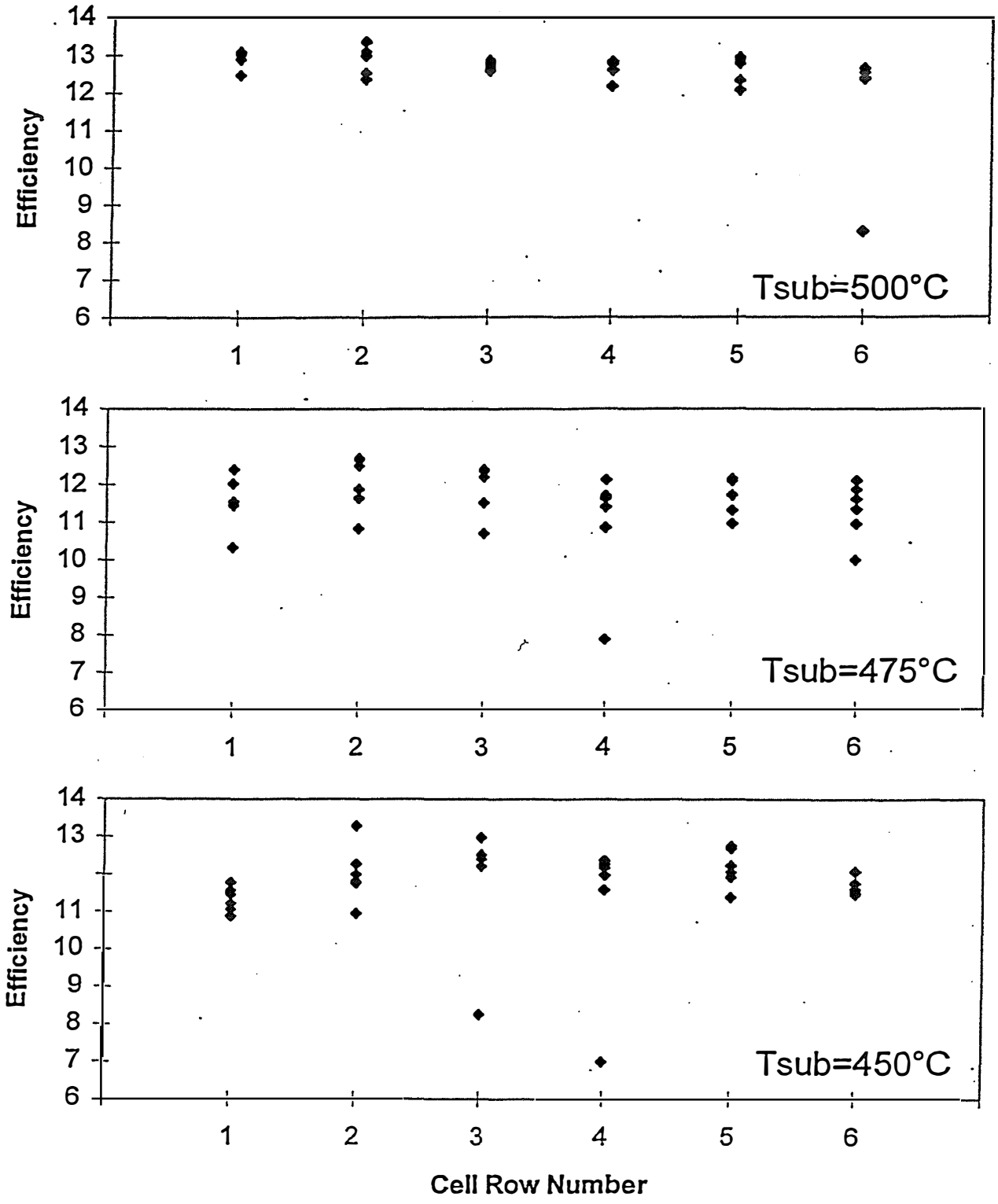


Figure 5.3.2-4. *The distribution of small area device efficiencies (in %) vs. cell position on the substrate for three different substrate temperatures during CIGS deposition. In each plot 36 cell are represented, which were arranged in a 6" x 6" matrix on the substrate.*

5.3.3 Absorber Deposition for Large Area

The scale-up to large substrate size of all process steps required for CIS based PV is paramount to the commercialization of product based on this materials system. As reported in the previous final report for the CIS subcontract, all requisite steps have been scaled up or demonstrated at Solarex up to 1000 cm^2 substrate size, except the process for absorber layer deposition. This final step presented a challenge in many respects. Simple control of the substrate temperature, and achievement of temperature uniformity sufficient to prevent substrate warping presented a first order difficulty. Equipment and process constraints disqualified the use of a chamber which would approximate an isothermal environment typical of ovens or muffle furnaces. Substrates of 9" x 9" size were raised to temperatures exceeding 500 C using heat flux predominantly from one side of the substrate. As stated earlier, improvements in equipment eventually allowed processing of the 9" x 9" size substrates at these temperatures during CIGS deposition with very good temperature control and a resulting edge-to-edge substrate warp of about 1 mm or less.

A second challenge existed in obtaining adequate compositional uniformity of the CIGS layer over the 9" x 9" substrate area. Several relatively simple means of improving compositional uniformity had been conceived at Solarex, but none of these were implemented due to lack of time. Despite this, the compositional uniformity over the above substrate area appeared adequate to meet or exceed the program goals. This was due, in part, to the compositional tolerance of the CIGS process itself. Figure 5.3.3-1 shows the device efficiency as a function of variation in Cu/(In+Ga) ratio. This data and previous evidence indicated the viability of module fabrication in a wide process window, extending from about 0.98 down to about 0.72 in terms of Cu/(In+Ga) ratio. The composition of an absorber layer covering a 9" x 9" (522 cm^2) substrate is shown in Figure 5.3.3-2 as a contour plot. Although the composition was slightly copper-rich in one area, it is apparent that the total variation in composition was within acceptable limits. Additional evidence which more strongly shows the sufficiency of compositional uniformity was shown in a following section in which nine 3" x 3" substrates, covering a 9" x 9" total substrate area, simultaneously had CIGS deposited using the same equipment and process as for above. These substrates were typically processed into seven submodules and two substrates of devices. Both the submodules and the devices showed excellent performance over the entire area, often in the 12% to 13% efficiency range.

Lack of time prevented final fabrication of a functional CIGS module on the 9" x 9" substrates, however the CIGS absorber depositions on scribed 9" x 9" Mo/glass substrates appeared visually very uniform, free of obvious defects and well adherent. Figure 5.3.3-3 shows a CIGS layer deposited on a 9" x 9" substrate at Solarex. No particular further difficulties were anticipated in completing the processing to finished 9" x 9" modules.

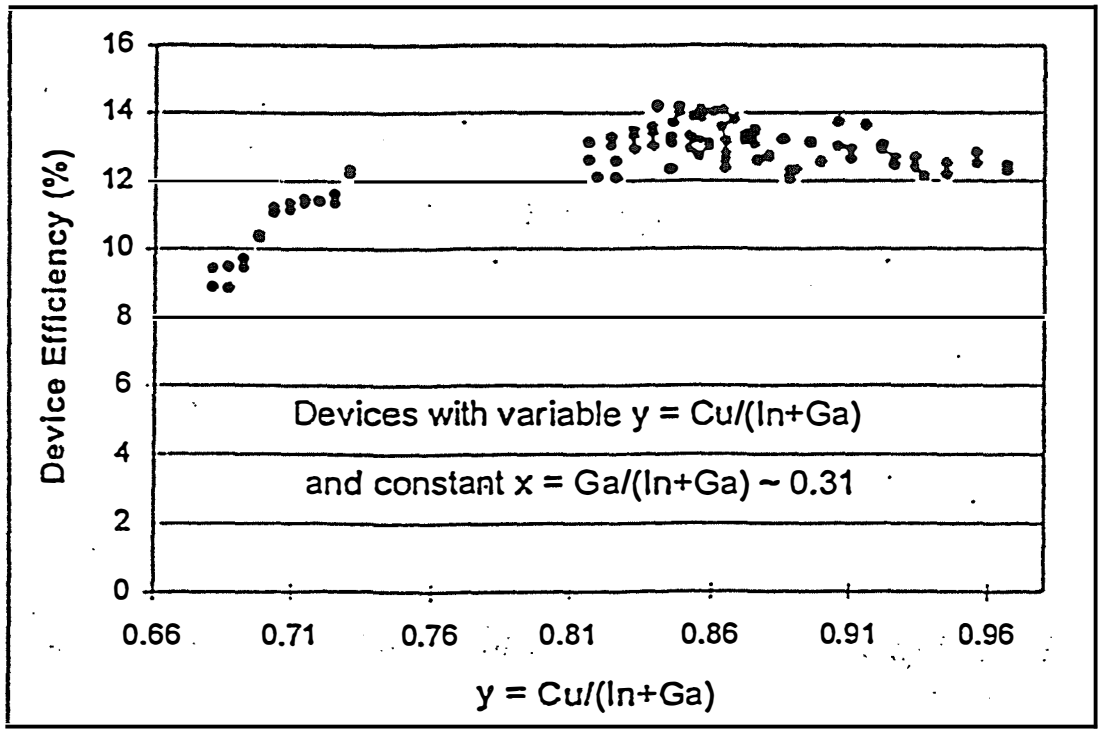


Figure 5.3.3-1. *A scatter plot of small area device efficiencies as a function of Cu/(In+Ga) ratio showing compositional tolerances.*

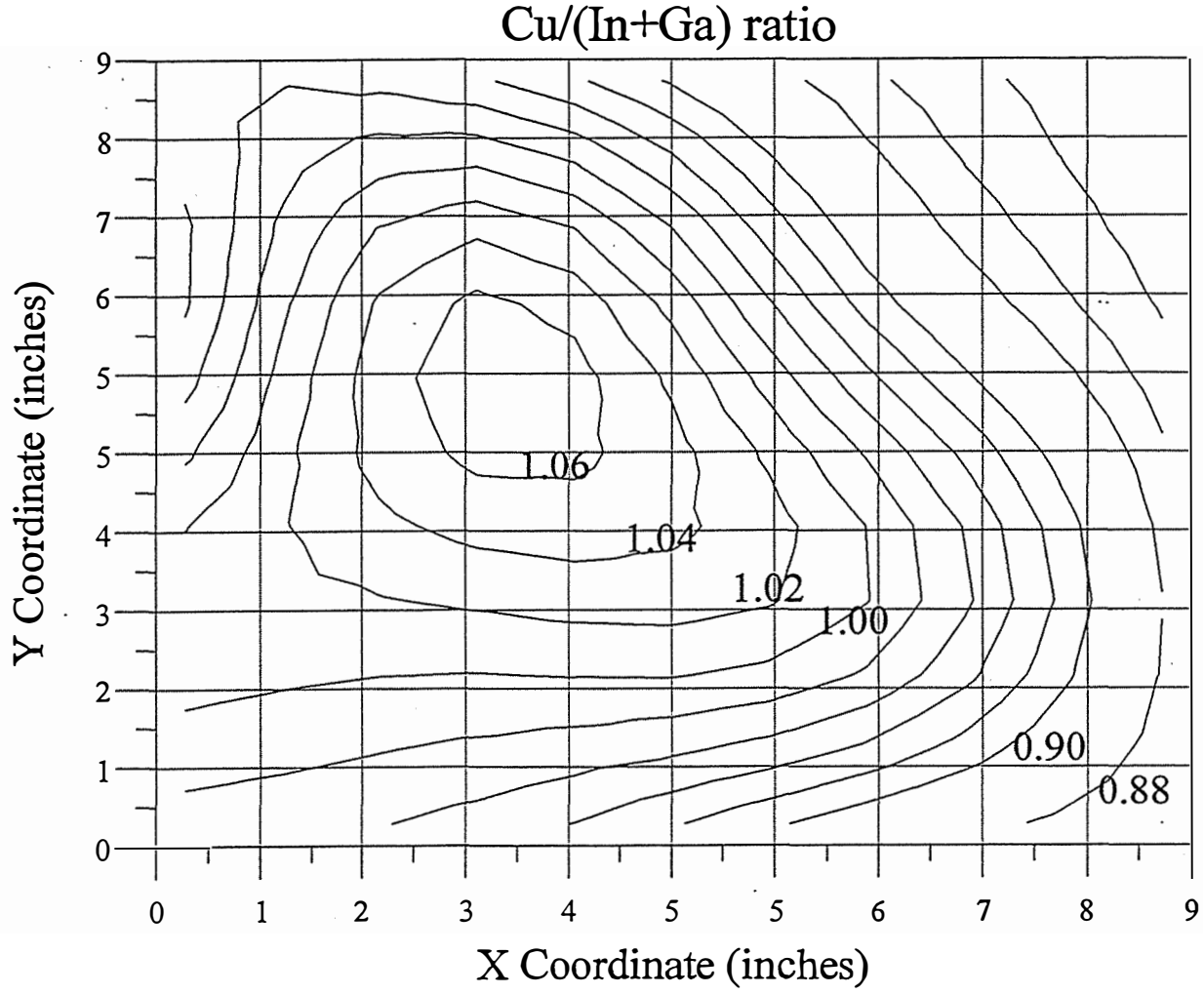


Figure 5.3.3-2. *A contour plot of Cu/(In+Ga) ratio as determined by EDS measurements of a CIGS absorber deposited on 9" x 9" substrate.*

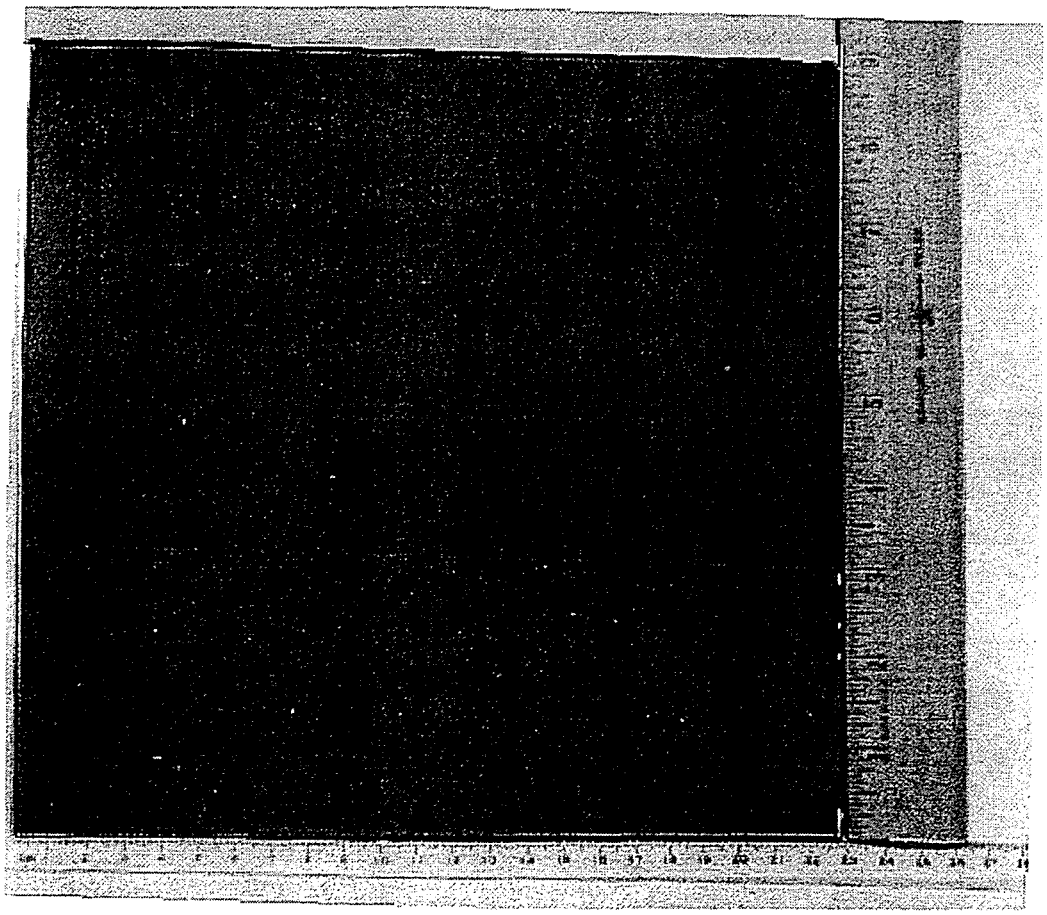


Figure 5.3.3-3. *A photograph of a CIGS absorber deposited on a scribed Mo/glass 9" x 9" substrate.*

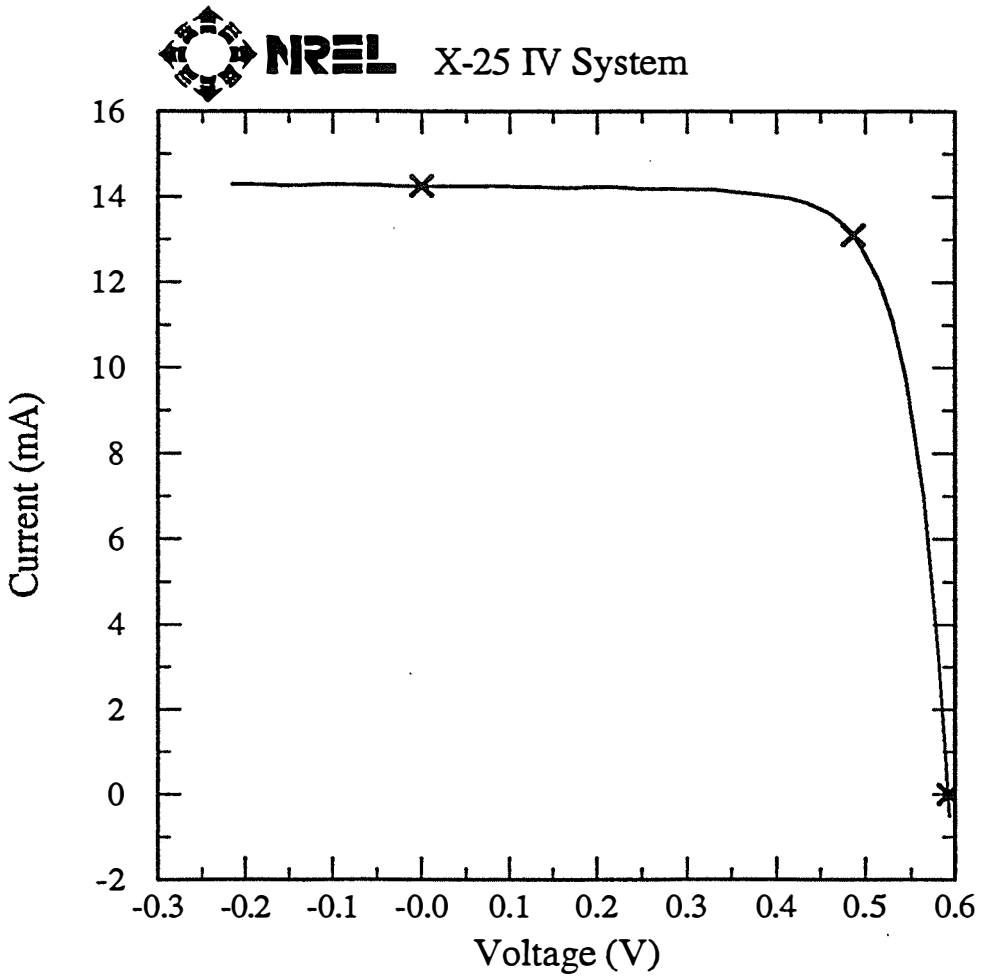
5.4 Device and Module Results

Small area device efficiency has increased up to 15.5%, as shown in Figure 5.4-1, mostly through incidental or tangential means. No particular effort was dedicated solely to device efficiency improvement. Small area device performance parameters were simply used as the metric for the development and optimization of processes for CIGS based PV module fabrication. For instance, the 15.5% efficient device shown in Figure 5.4-1 was not optimized for device performance in that it had a 10 to 15 ohms/square ZnO window layer. With the grid on the cell providing short lateral collection distances the device would almost certainly have exhibited higher efficiency with a more highly resistive (and more transparent) window layer. The window layer was used was selected solely on the basis of module considerations.

Solarex ZnO/CdS/CIGS

Sample: E154-3-D7
Oct 17, 1995 8:45 AM
ASTM E 892-87 Global

Temperature = 25.0°C
Area = 0.4127 cm^2
Irradiance: 1000.0 Wm^{-2}



V_{oc} = 0.5924 V
I_{sc} = 14.25 mA
J_{sc} = 34.54 $mAcm^{-2}$
Fill Factor = 75.62 %

V_{max} = 0.4871 V
I_{max} = 13.11 mA
P_{max} = 6.385 mW
Efficiency = 15.5 %

Figure 5.4-1. *J-V characteristics of a 15.5 % device.*

5.4.1 Module Loss Analysis

Module losses were attacked in two ways: through detailed calculation and minimization of known, systematic losses in the module structure, and by comparison of actual module performance to equivalent measures of device performance. Examples of the latter approach include comparison of module to device short circuit current densities, open circuit voltages and quantum efficiencies. Table 5.4.1-1 compares the photovoltaic parameters of the best device and module is shown below.

	best device	best sub module	Δ(abs.)	Δ(%)
x=Ga/(In+Ga)	0.24	same	0	0
Eg(x) (eV)	1.16	same	0	0
Voc (mV)	592.4	580 /seg	12.4	~2.1
Jsc (mA/cm^2)	34.54	33.8	0.74	~2.1
FF	0.7562	0.6626	0.0936	~12.4
η (%)	15.5	13.0	2.5	~16.1

Table 5.4.1-1. *Photovoltaic parameters of the best device and best submodule made using the same absorber material.*

It was evident that there was very little loss in the module fabrication methods used in terms of short circuit current and open circuit voltage. This indicated an absence of severe shunts or gross spatial non-uniformities in absorber and contact behavior. Comparison of the quantum efficiency of the module to the device, shown in Figure 5.4.1-1, corroborated the similarity between device and module behavior. The small difference that does exist in short circuit density between the device and module in the Table above was likely due to differences in reflection losses and area losses. The reflection loss would be expected to differ as the module was encapsulated under glass/EVA, which would render a MgF_2 reflection coating less effective than when applied directly to the device. Relative area losses are difficult to estimate, but in one case are due to a metallic grid and in the other are due to monolithic interconnects.

The significant loss in performance in going from device to module occurred in fill factor. Detailed calculation of systematic module losses was made using a model. The model calculated the expected J-V behavior of a module structure based on the measured behavior of a small area device which was representative of the absorber and contacting layers. The aggregate current-voltage behavior of a module segment was taken as the sum of currents due to finite elements of area distributed over the module segment, but each operating at differing voltage. The variation in

operating voltage as a function of lateral distance on the module segment from the interconnect occurred due to the lateral voltage drop in both the front and back contacts. In practice, the front contact dominated the effect, since its sheet resistance was typically much larger than that of the Mo back contact (approximately 0.2 ohms/square). The model also accounted for interconnect resistance, interconnect area loss and optical loss in the front transparent contact. This approach is described in more detail elsewhere [10, 12]. This model was used very effectively to estimate the optimum module segment width, and to examine the sensitivity and impact of sheet resistivity on module segment width. Calculations made using this module indicated that module efficiencies would be possible, using the present processes and module fabrication methods, which were only about one percentage point lower in efficiency than that of devices made with the same materials layers. Figure 5.4.1-2 shows the expected module efficiency as a function of segment width and front contact resistivity for uniform CIGS absorber and contact layers which would result in 14.4% efficiency if processed into small area devices.

Still other methods were used to analyze module losses which were non-systematic, e.g. the appearance of random shunting in module segments. One means was the use of scanning optical beam induced current (OBIC) characterization of modules. This work indicated that, at least in some instances, the appearance of shunting in module segments was not random, and tended to occur predominantly near one side of the segment interconnect. This effect is shown in Figure 5.4.1-3 in a diagram provided by individuals at Colorado State University where this analysis was carried out.

OBIC was also used to examine the impact of bubbles trapped in the EVA between the module surface the glass cover sheet. Data indicated that these bubbles were of little consequence, except for cosmetic appearance. Attempts were made to use the OBIC method to gauge the spatial uniformity of CIGS encapsulated modules. It was clear that OBIC could discern spatial variations in module performance. However, the true magnitude and impact these variations on module performance, and an understanding of typical behavior was difficult. Analyses of spatial variation of absorber and contacting layers using matrix coverage by devices invariably indicated that spatial variation was not a problem. An example of device mapping of an area of absorber is shown in Figure 5.4.1-4. Most of the devices in these matrices which are of below average performance are suspected to be due to physical damage (and shunting) of the device induced by J-V measurement of the device itself.

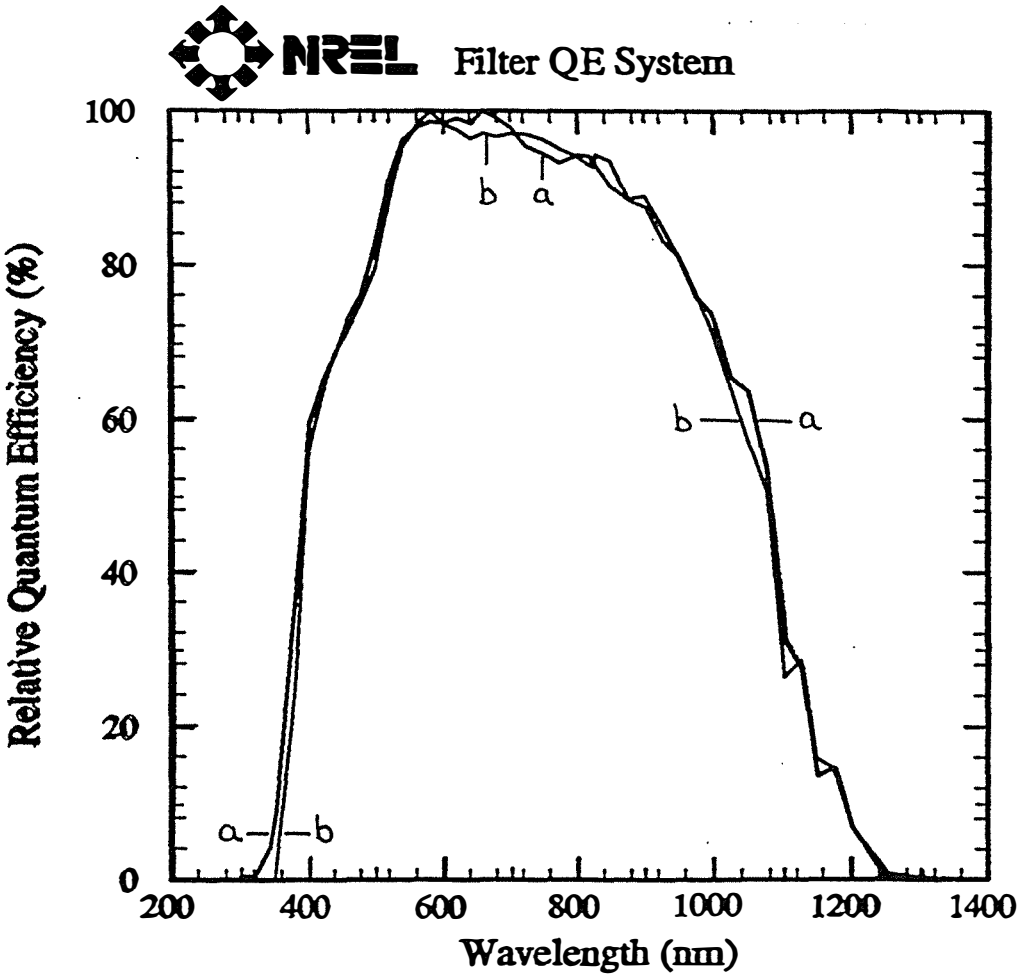


Figure 5.4.1-1. *A comparison of the relative quantum efficiency of the (a) best device and (b) submodule made using the same process. It must be noted that each measurement is normalized independently and cannot be compared in amplitude.*

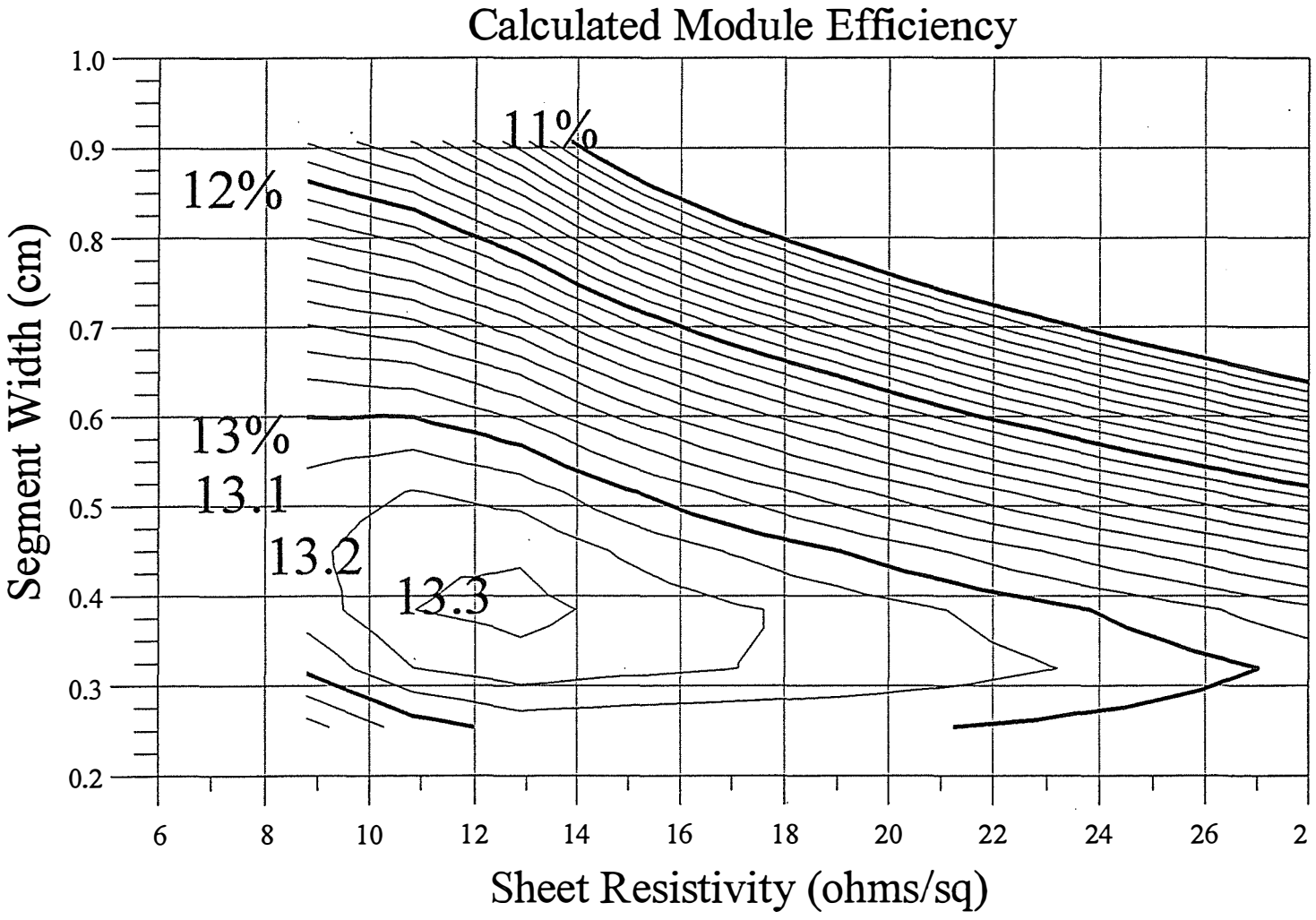


Figure 5.4.1-2. *The expected aperture area module efficiency as a function of front contact sheet resistivity and segment width, based on absorber and contacting layers capable of 14.4% device efficiency. Interconnect width is taken to be 0.03 cm and interconnect and back contact resistivity are negligible.*

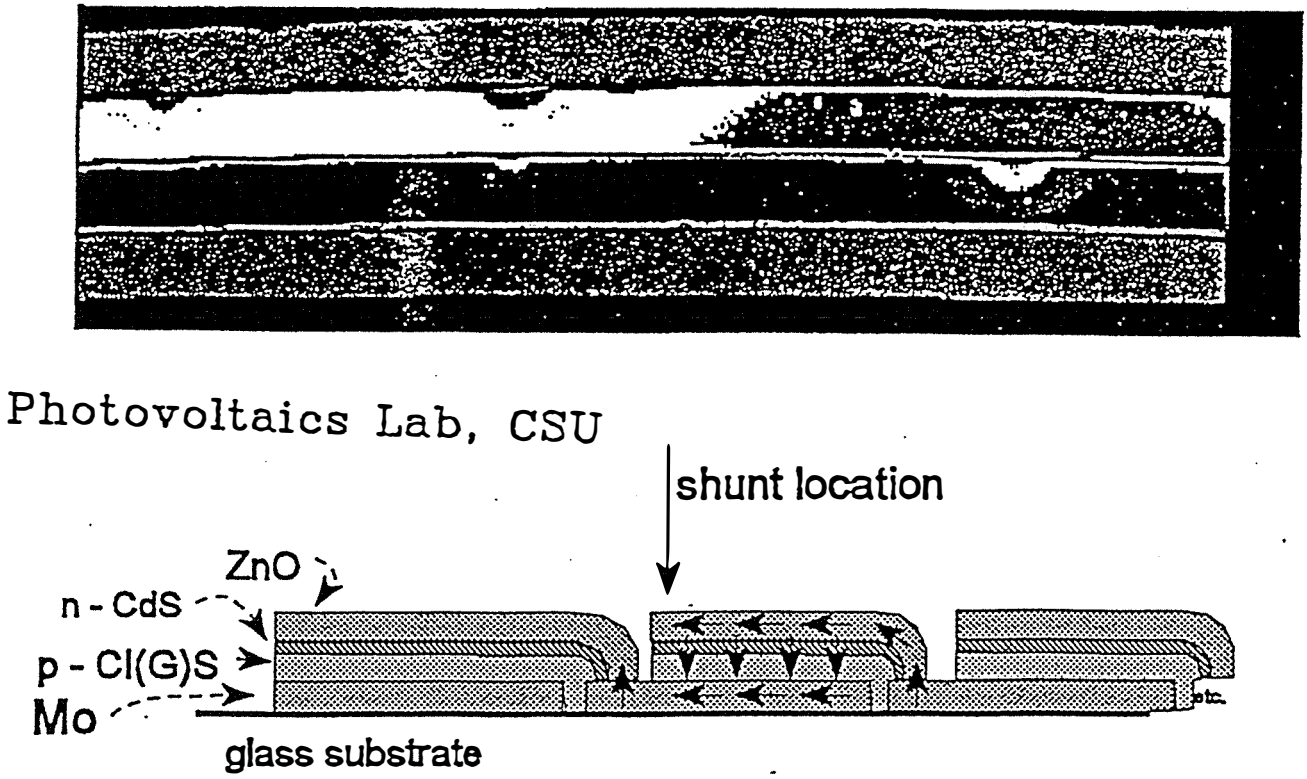
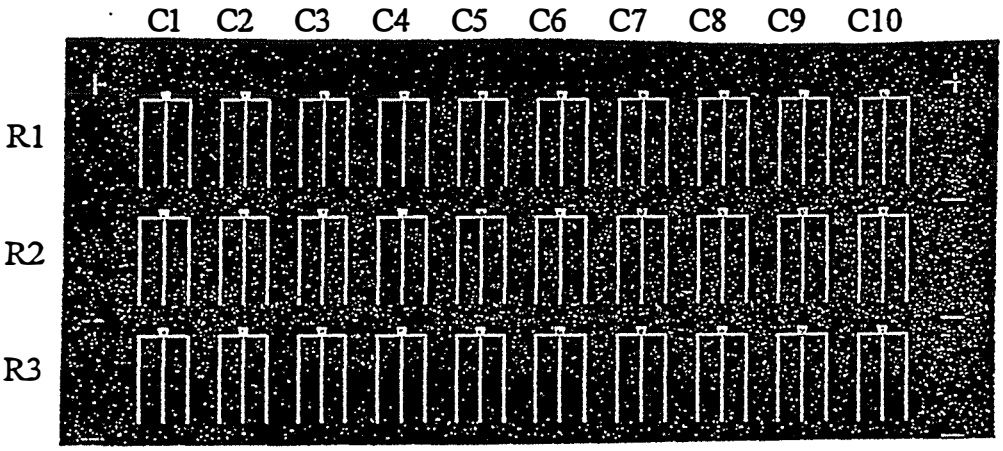


Figure 5.4.1-3. *Photocurrent response to blue laser OBIC scans of module segments and a schematic diagram showing the relative location of the shunts.*



Position of the 30 cells on the sample

SA18A	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	12.1	14.1	14.3	14.8	15.3	15.3	14.8	10.5	9.8	13.5
R2	14.1	14.4	14.6	14.5	15.2	14.0	14.0	14.4	11.6	13.6
R3	12.9	14.2	14.6	15.0	14.8	15.1	14.9	14.3	13.7	6.8

Efficiency (%) versus position

SA18A	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	596	610	616	622	632	635	633	614	603	618
R2	604	609	615	609	623	620	617	616	598	605
R3	602	610	614	619	620	619	616	609	606	531

Voc (mV) versus position

SA18A	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	65.4	72.9	71.6	72.6	73.3	73.1	73.0	54.7	53.3	72.7
R2	72.8	72.7	72.8	72.7	73.5	68.3	69.5	73.0	62.5	71.4
R3	66.7	71.9	72.3	73.3	72.7	72.2	73.1	72.9	72.4	41.1

FF (%) versus position

Figure 5.4.1-4. *Spatial uniformity of device performance, showing efficiency, V_{oc} and fill factor for adjacent devices across a 3 inch wide substrate.*

5.4.2 Submodule Results and Improvements

The highest efficiency submodule produced at Solarex is shown in Figure 5.4.2-1. This 40 cm^2 , 20 segment submodule was measured at NREL to have an aperture area efficiency of 13.0%, and a Voc of 11.61 volts, a short circuit current of 68.29 mA and a fill factor of 66.26%. Results of the detailed analysis of module losses described in the previous section indicated that the fill factor of a module of this design should have been higher. Further measurements confirmed the existence of a shunt mechanism operating between adjacent segments which reduced the fill factor. Indeed, the shunt characteristic was visible in the slope of the module I-V curve approaching 0 volts bias, and was more severe than expected based on the shunt contributions intrinsic to a representative small area diode and those expected due to lateral collection effects.

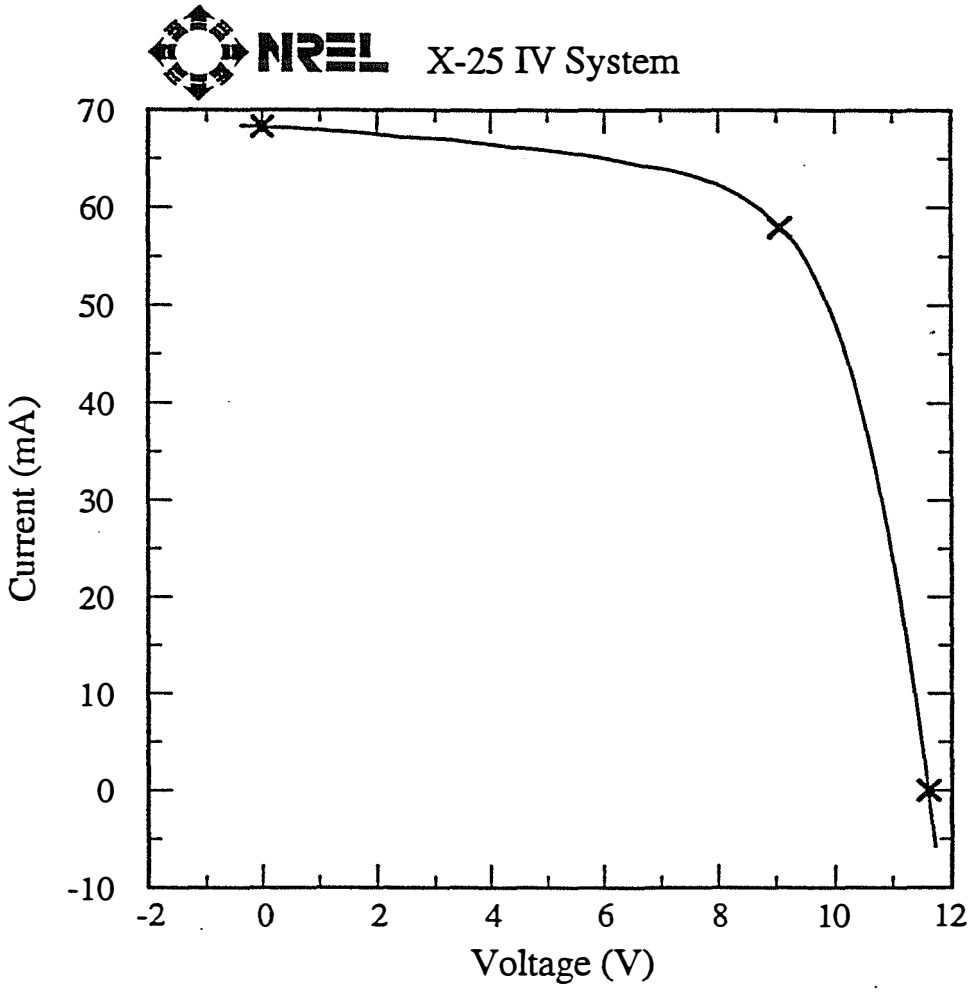
The additional shunt contribution was attributed to a path due to the present design of the monolithic module interconnect. Subsequent to this, the monolithic module interconnect scheme was modified to largely eliminate the additional shunt. The effects of this modification were immediately evident in increased module fill factors. Figure 5.4.2-1 shows the performance of PV devices and modules made in a single absorber deposition. The fill factors of all but one module in this set of seven modules exceeded that of the "champion" 13% efficient module, and three submodules had fill factors exceeding 70%. This performance was remarkable considering that the average device fill factor, taken from two 3" x 3" substrates processed as devices, was only 70.4 and 74.1%. These results were, however, closer to that expected for this module design from the detailed modeling described earlier.

The implication is that the elimination of the additional shunt path by modification of the interconnect design increases the fill factor by > 6%. This modification had no impact on module Jsc or Voc. Thus a module having the open circuit voltage and short circuit current measured for the "champion" module, but having the improved interconnect design and improved fill factor, would be expected to have an efficiency approaching 14%. The results shown in Figure 5.4.2-1 also indicate the sufficiency of the equipment and processes for the achievement of high efficiency modules having 9" x 9" size (522 cm^2).

Solarex MgF_2/glass/ZnO/CdS/CIGS/Mo Submodule

Sample: E157-6-7
Nov 8, 1995 4:22 PM
ASTM E 892-87 Global

Temperature = 25.0°C
Area = 40.40 cm^2
Irradiance: 1000.0 Wm^{-2}



V_{oc} = 11.61 V
I_{sc} = 68.29 mA
J_{sc} = 1.690 $mAcm^{-2}$
Fill Factor = 66.26 %

V_{max} = 9.062 V
I_{max} = 57.97 mA
P_{max} = 525.3 mW
Efficiency = 13.0 %

Figure 5.4.2-1. *The illuminated J-V characteristics for a monolithic submodule having 13% aperture area conversion efficiency. This 40 cm^2 submodule is comprised of 20 segments and is encapsulated using EVA and a MgF_2 coated cover glass.*

SUBSTRATE (1,1) Submodule : 15 segments Voc = 0.559 V/seg. Jsc = 31.3 mA/cm^2 FF = 0.702 **=> η = 12.3%**	**SUBSTRATE (1,2)** Submodule : 15 segments Voc = 0.575 V/seg. Jsc = 31.2 mA/cm^2 FF = 0.704 **=> η = 12.6%**	**SUBSTRATE (1,3)** Device Array Average : Voc = 0.576 V Jsc = 30.8 mA/cm^2 => η = 12.5% FF = 0.704 Best : Voc = 0.580 V Jsc = 31.6 mA/cm^2 => η = 13.0% FF = 0.708
SUBSTRATE (2,1) Submodule : 15 segments Voc = 0.572 V/seg. Jsc = 30.9 mA/cm^2 FF = 0.701 **=> η = 12.4%**	**SUBSTRATE (2,2)** Submodule : 15 segments Voc = 0.577 V/seg. Jsc = 31.8 mA/cm^2 FF = 0.674 **=> η = 12.4%**	**SUBSTRATE (2,3)** Submodule : 15 segments Voc = 0.591 V/seg. Jsc = 30.8 mA/cm^2 FF = 0.669 **=> η = 12.2%**
SUBSTRATE (3,1) Device Array Average : Voc = 0.572 V Jsc = 31.4 mA/cm^2 => η = 13.3% FF = 0.741 Best : Voc = 0.580 V Jsc = 31.4 mA/cm^2 => η = 13.6% FF = 0.749	**SUBSTRATE (3,2)** Submodule : 15 segments Voc = 0.587 V/seg. Jsc = 30.6 mA/cm^2 FF = 0.682 **=> η = 12.3%**	**SUBSTRATE (3,3)** Submodule : 15 segments Voc = 0.576 V/seg. Jsc = 30.3 mA/cm^2 FF = 0.660 **=> η = 11.5%**

Figure 5.4.2-2. *The performance of a matrix of nine substrates processed into devices and submodules. All substrates were deposited in a single absorber layer run covering a 9" x 9" area.*

6.0 Conclusions

Although several desirable processes remain to be achieved, such as a heterojunction formation step which is Cd-free and vacuum-compatible, this work has shown that high efficiency PV product based on thin film CIGS is eminently within reach. The key factors of viable high speed and large area deposition processes for the absorber layer and high speed, low cost processes for the transparent front contact have been developed in this program. As a result, thin film module efficiency has crossed the 13% level for the first time. Given the demonstrated efficiency, stability and scalability of PV modules based on this materials system, and the documented low cost of the constituents it seems likely that this system will dominate the photovoltaic marketplace at some point in the future.

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13. ABSTRACT *(Maximum 200 words)*

This report describes the progress made at Solarex for both device and module efficiencies from the inception of the CIS research program to the present. A rapid improvement in efficiency is apparent, culminating in the fabrication of a 15.5%-efficient device (total area) and a 13%-efficient submodule (aperture area). The device represents the highest efficiency device measured by NREL for any industrial source at that time. The module represented a new world record for any thin-film module at the time of its measurement. The factors leading to these results included improvements in absorber layer quality, transparent contacts, scribing and module formation processes. Other elements critical to the commercialization of CIS-based photovoltaics were also successfully attacked, including reduction of absorber deposition times into the range of 10 to 20 minutes and the successful scale-up of the absorber deposition process to greater than 500 cm^2. Other requisite processes saw continued development, such as a rapid, low-cost method for transparent window deposition. Subsequent to the demonstration of 13% module efficiency, scribing techniques were further improved that resulted in a reduction in shunt losses and higher module fill factor. This improvement, and the concomitant gain in fill factor, would yield efficiencies approaching 14% on modules having a short-circuit and open-circuit voltage comparable to the record module.

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