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CIS Photovoltaic Technology

Annual Technical Report
12 January 1996 - 11 January 1997

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Princeton, New Jersey

National Renewable Energy Laboratory
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A national laboratory of
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Preface

This report describes work performed during the second year (January 12, 1996 - January 11, 1997) of a three-phase, three-year, cost-shared subcontract with NREL entitled "CIS Photovoltaic Technology". The subcontract is one component of the NREL Thin Film Partnership Program. Remarkably high efficiencies (15 - 17.6%) have been demonstrated for small area $Cu(In,Ga)Se_2$ devices in the U.S., Europe and Japan. A major objective of this program is to demonstrate the preparation of high quality CIGS material over large areas (0.43 m^2) using novel equipment and processes that are adaptable to high throughput manufacturing. Using this material, prototype CIGS PV modules will be produced. Research results generated by other components of the Thin Film Partnership Program will be incorporated as required.

Needless to say, the results described here could not have been achieved without the diligent efforts of the EPV research and engineering staff. Other institutions and individuals have also contributed significantly. At NREL we would like to thank S. Asher, H. Field, A. Franz, R. Matson, A. Mason, and A. Swartzlander for invaluable material and device characterization, T. Coutts, T. McMahon, and J. Tuttle for helpful technical discussions, and especially R. Noufi for his consistent help to industry to advance CIGS technology. On the program side, we are indebted to H. Ullal and K. Zweibel for their unflagging interest and support. We have benefited also through interaction with individuals at Colorado State University, the Institute of Energy Conversion /University of Delaware, and Princeton University.

Summary

Thin film photovoltaic modules based on $Cu(In,Ga)Se_2$ have been shown to possess attributes that should enable them to compete effectively with silicon-based modules, and that should ultimately allow realization of a much lower $/Wp cost figure. These attributes are stability, high efficiency, and low materials cost. Energy Photovoltaics has explored novel CIGS formation recipes that can be implemented on a unique pilot line constructed to coat substrates 4300 cm^2 in area. One particular feature of this line is the use of proprietary linear sources capable of downwards evaporation.

After experimentation with several types of recipe, a so-called "hybrid" process was found to simultaneously yield the desired combination of properties, namely good adhesion, device efficiency, uniformity, and reproducibility. The steps involve precursor formation, compound formation, and termination. Diagnostic techniques used to study and improve the CIGS films included spatial mapping of thickness, composition (using Auger analysis), resistance, V_{OC} and I_{SC}. The last three items are determined by quick tests designed to provide rapid feedback on plate quality. Problem areas were broken down and isolated through use of techniques involving substitution of different pieces of equipment for certain processing steps. For example, pilot line precursors were selenized in both the pilot line and smaller scale R&D equipment.

At the device level, significant results were obtained using alternative buffer layers, direct ZnO devices, and chemical treatment of the CIGS. A new method was developed and transferred to NREL to enable measurement of device specific internal resistance.

Considerable effort was put into complete module fabrication, testing and analysis. A reliable procedure for laser scribing the molybdenum electrode was developed. The chemical bath deposition of the thin CdS layer was made more efficient in terms of material use. The bipolar sputtering process for large area ZnO was further optimized to yield films with 80% transmission and less than 30 ohms/square sheet resistance. And finally, a new, non-destructive technique was developed for obtaining local I-V curves at selected locations on a patterned plate.

A fully encapsulated 3156 cm^2 CIGS module sent to NREL for testing produced 19.7W in sunlight at 997 W/m^2 irradiance, corresponding to an aperture area efficiency of 6.25%. A later CIGS plate measured at EPV (3948 cm^2) produced 27.7W in sunlight at 998 W/m^2 irradiance, representing a 7.0% aperture area efficiency. A prototype 4-terminal a-Si/a-Si/CIGS module generated a total of 29.4W in sunlight (7.6%).

These solid achievements confirm the viability of EPV's approach and large area processing equipment. The next phase of work will concentrate on meeting or exceeding an average 8.0% aperture area efficiency for all processed modules. Plans include increasing the cell open-circuit voltage through tailoring of the Ga profile, elimination of light and thermal instabilities, and a more complete understanding and documentation of the process to ensure reproducible processing.

Table of Contents

List of Figures

List of Tables

Introduction

Photovoltaic panels are a useful and benign source of electricity. Worldwide use of such panels continues to rise, but could be accelerated if the manufacturing cost of the PV modules were to be reduced. The use of thin film semiconductors offers the best opportunity for significant cost reduction. This follows from the reduced raw materials cost, the ability of large area substrates to be fully coated, and avoidance of handling and interconnecting a large number of bulk wafers.

Copper indium diselenide and related alloys represent a class of materials with a demonstrated track record of high conversion efficiency, outdoor stability, and ability to be produced over large areas. Yet the absence of CIS modules in the marketplace points to difficulties with the technology that have not been fully conquered. The most important issue is finding a viable combination of CIGS formation route and manufacturing equipment that allows high yield, high throughput processing. Other goals include elimination of the use of hazardous materials, and engineering of the module to pass all of the standard qualification tests.

Energy Photovoltaics, Inc. (EPV) has pioneered the production of $Cu(In,Ga)Se_2$ PV modules using vacuum processing, and with the use of elemental Se rather than the poisonous gas H_2Se. Experience has shown that the use of non-vacuum deposition techniques is prone to various surface irregularities that ultimately limit yield and large area coating capability. Prior to this subcontract, EPV had achieved an efficiency of about 9% for unencapsulated CIS modules of about 200 cm^2. The focus of this subcontract has been to develop CIGS formation schemes that can be implemented on EPV's pilot line for production of 4300 cm^2 modules. Naturally, the goal has been to simultaneously achieve good adhesion, good efficiency, good uniformity, and good reproducibility.

Other programs include the development of large area zinc oxide transparent conductors, patterning of the layers, junction studies, novel diagnostics, computer modeling, encapsulation and testing. EPV has further constructively participated in several of the teams organized under the Thin Film PV Partnership Program, including the preparation and distribution of thin film samples.

1.0 Deposition and Monitoring of CIGS

EPV's manufacturing philosophy embraces all-vacuum deposition techniques such as evaporation and sputtering to provide high throughput and a high degree of film quality and process control. Metal films are deposited in the large area deposition equipment by DC magnetron sputtering with the plate translated past the sputtering target. The selenides and Se are delivered to the substrate from linear evaporation sources while the plate is translated along its long axis perpendicular to the long axis of the linear sources. The deposition can occur simultaneously with substrate heating, even with the glass substrate heated beyond its softening point. These deposition techniques are best suited toward the implementation of recipes involving sequential deposition and reaction stages [1].

The linear evaporation source developed by EPV is capable of continuous, high rate deposition of films with uniform quality and can easily be scaled up to coat substrates of almost any practical width. We have recently succeeded in implementing a means for the continuous reloading of source material without breaking vacuum. The manufacture of the source itself is uncomplicated and the materials comprising it are inexpensive and easily procured. These advantages are expected to help keep manufacturing costs low.

The design and use of the linear source is crucial for depositing films with uniform thickness along the length and across the width of a substrate. The linear source deposition pattern has been optimized empirically and with the aid of computer models. Previous publications have documented the progressive improvement in the uniformity of InSe films across the substrate [2,3]. Figure 1.1 shows the variation in thickness across the width of a plate for a Se film deposited from a linear source.

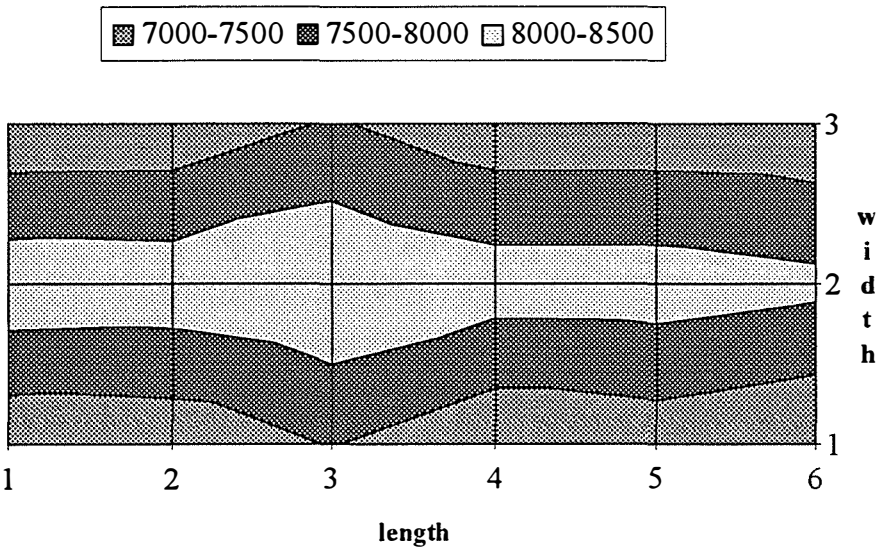


Figure 1.1: selenium thickness distribution over a standard-sized plate (Å).

Non-destructive techniques have been devised for quickly mapping the photovoltaic characteristics of all CIGS films deposited in the pilot line. These techniques provide timely feedback to the deposition process and accelerate module throughput by allowing us to cull plates

with poor characteristics. The CIGS resistance, open-circuit voltage and short-circuit current are routinely mapped over 25 points across the substrate at various points in the module processing sequence.

The usefulness of this approach is illustrated by the following example. Plate 740B was completed as a module and an illuminated IV measurement revealed a less than average power output. Review of the resistance map for this plate indicated that one end of the plate had very low resistance readings, indicative of Cu-rich CIGS (Figure 1.2). This was confirmed by reviewing the open-circuit voltage map, which showed very low values in the same region (Figure 1.3). Removal of this end of the plate led to a higher power output and significantly higher efficiency for the remaining section (see Section 7). The source of the nonuniformity was ultimately traced to an intermittent problem with the drive in the in-line sputtering system.

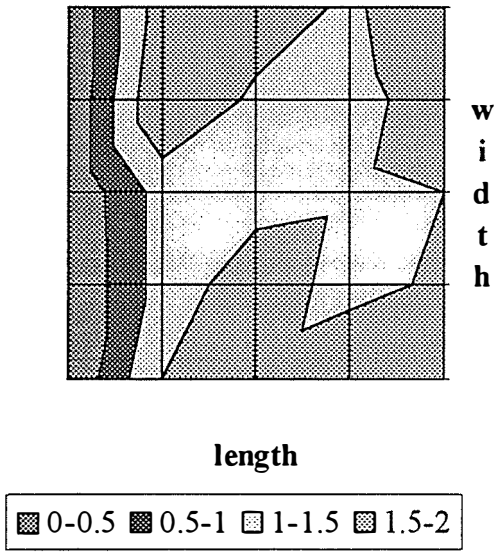


Figure 1.2: resistance map for plate 740B (in MΩ).

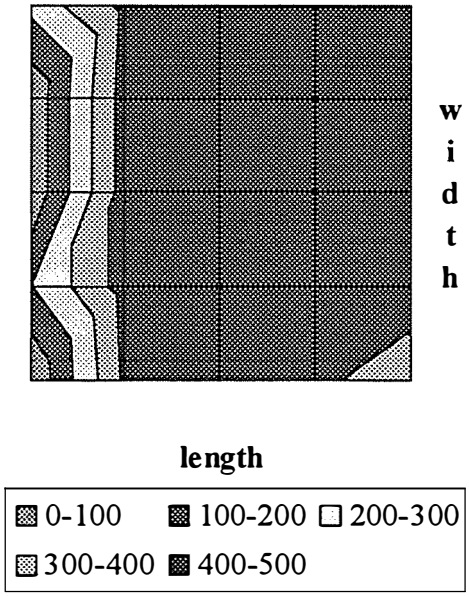


Figure 1.3: open-circuit voltage map for plate 740B (in mV).

A rapid, non-destructive technique for mapping the short-circuit current density of pilot line plates has also been developed. This technique has been invaluable in improving the CIGS deposition recipes used in the pilot line. Some recipes used in the past demonstrated good open-circuit voltage maps, but mapping of short-circuit current densities revealed values less than 15 mA/cm^2, even with bulk values of Cu/(In+Ga) close to ideal. Feedback from this mapping has led to improvements in CIGS quality. Plates are now routinely made with average short-circuit current densities greater than 30 mA/cm^2. Unfortunately, the mapping is unambiguous only on unpatterned plates; resistance losses in the Mo limit the accuracy of the technique away from the plate perimeter on patterned plates. The short-circuit density map for a typical unpatterned plate is shown in Figure 1.4. The symmetrical non-uniformities present are currently under investigation.

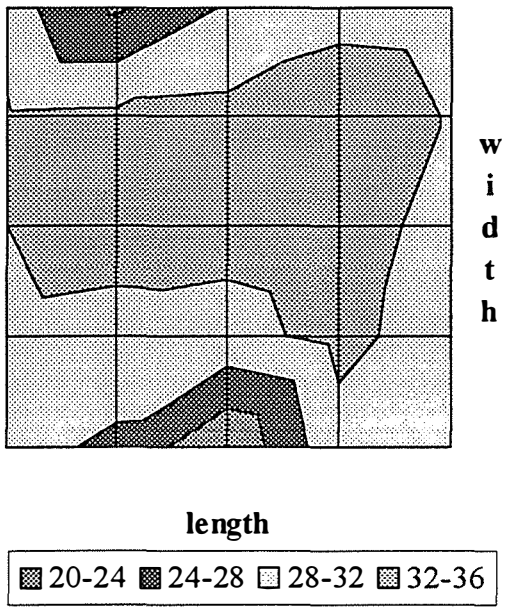


Figure 1.4: short-circuit current density map for plate 681 (mA/cm^2).

2.0 CIGS Analysis

2.1 Absorber Formation

The formation of CIS by the selenization of metallic precursors has been demonstrated to proceed via a sequence of intermediate reactions [4]. Understanding these intermediate reactions is critical to developing recipes that yield higher film quality, minimize processing time, and maximize Se utilization. The standard technique to determine what the intermediate products are and at what temperatures they form is stop the reaction at various points and assess the film crystallography by XRD. This technique provides valuable information but is limited by its punctuated nature. To aid in our recipe development, we have implemented a differential thermometry (DT) technique that allows time progressive reaction studies to be performed.

The technique consists of directly monitoring the film temperature of (Cu, In, Ga) films as they are being ramped in temperature and exposed to Se. To ensure accurate monitoring of the film temperature and to minimize thermal mass, the films are deposited directly onto a thin film RTD. The temperature is feedback controlled by an identical RTD (with no films) located adjacent to the first one. The resistances of the reference and sample RTDs are monitored in the four-wire configuration and the data is recorded on a PC. In one experiment, Cu and In were sequentially deposited by evaporation onto the thin film RTD. The relative thicknesses of the Cu and In films were adjusted to provide the slightly Cu-poor composition necessary for efficient devices. In another experiment, a film of In only was deposited with a thickness identical to the In film deposited in the first experiment. In both experiments, the films were annealed at 140°C for several minutes and then exposed to a Se flux of 3 nm/sec while the temperature was ramped at a constant rate to 530°C. After soaking at 530°C for several minutes, the RTDs were allowed to

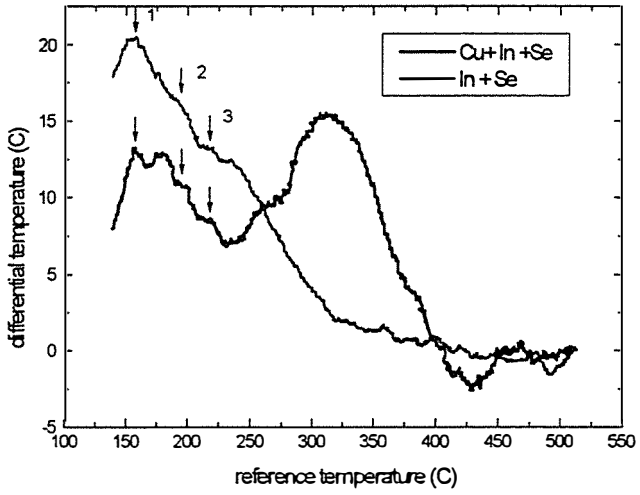


Figure 2.1: DT profiles of the selenization of (Cu,In) and In films.

cool to 140°C and then heated in a time-temperature profile identical to the first one, still using the reference RTD for feedback control. The temperature of the sample RTD during this second temperature ramp was then subtracted from its temperature during the first ramp. The difference is plotted versus the reference RTD temperature. The results of these experiments are shown in Figure 2.1.

A positive peak in the differential temperature indicates the occurrence of an exothermic reaction, a negative peak indicates an endothermic reaction. Changes in emissivity due to surface roughness, for example, may also be evident by this technique. At least three of the peaks appear to be common to both plots and may be attributed to the formation of indium selenides or oxides. Further analysis and a thorough literature review are necessary to definitively assign peaks to various reactions.

2.2 Adhesion and morphology

EPV has investigated two different materials (type I and II) to enhance the adhesion of CIGS films to the Mo substrate. Both materials lead to improved adhesion but very different device characteristics have been observed depending on the adhesion layer used. To further assess the differences between CIGS formed on the different materials, precursors were deposited in the pilot line sputtering system on each material type. Sections were cut off and converted to CIGS in an R&D reactor. The remainder of each plate was converted to CIGS in the Zeus. Adjacent samples of the precursors and the precursors converted to CIGS in both the R&D reactor and the Zeus were submitted for SEM and EPMA at NREL (R. Matson and A. Mason).

EPMA of the CIGS films made in the Zeus show similar Cu/(In+Ga) ratios (Table 2.1). SEM's show the precursor deposited on the type I adhesion layer to have a bumpy, non-uniform morphology compared to the precursor deposited on the type II adhesion layer which is also reflected in the CIGS films formed in the R&D reactor (Figure 2.2 - 2.7). However, the CIGS on the type II material shows the presence of voids at the Mo interface, which may account for its

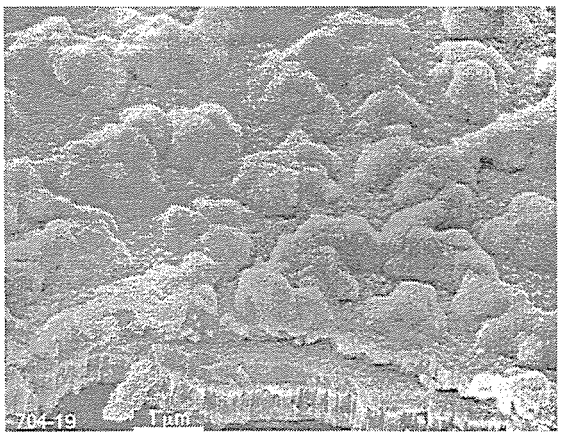


Figure 2.2: precursor with type I adhesion layer

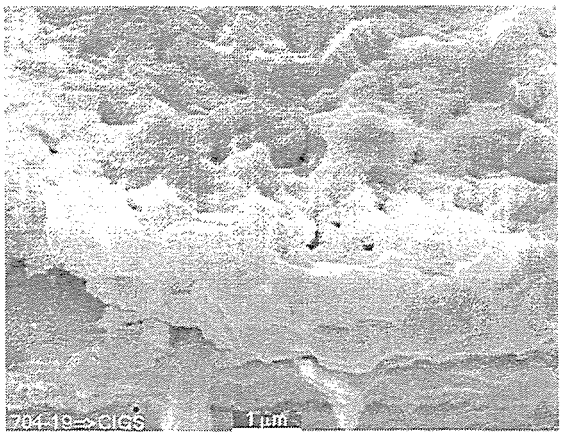


Figure 2.3: precursor with type I adhesion layer converted to CIGS in the R&D reactor

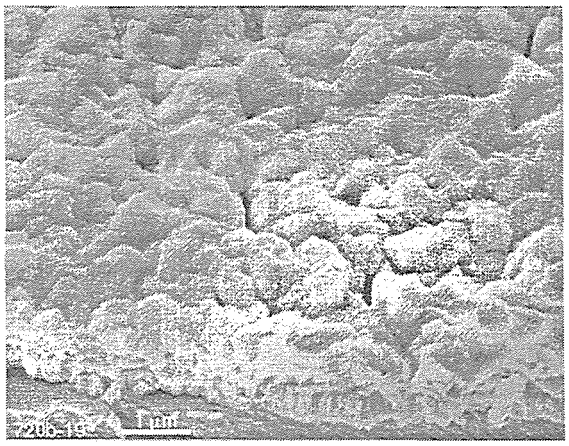


Figure 2.4: precursor with type II adhesion layer

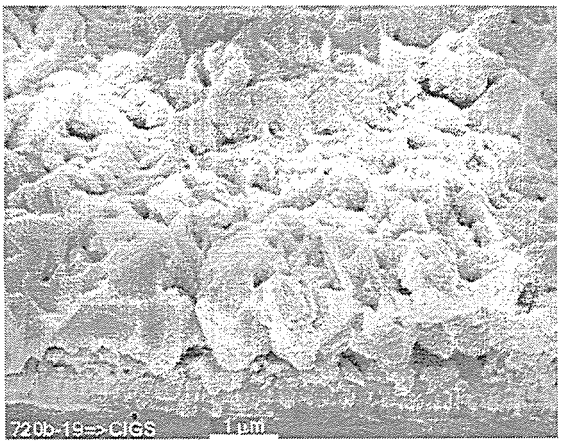


Figure 2.5: precursor with type II adhesion layer converted to CIGS in the R&D reactor

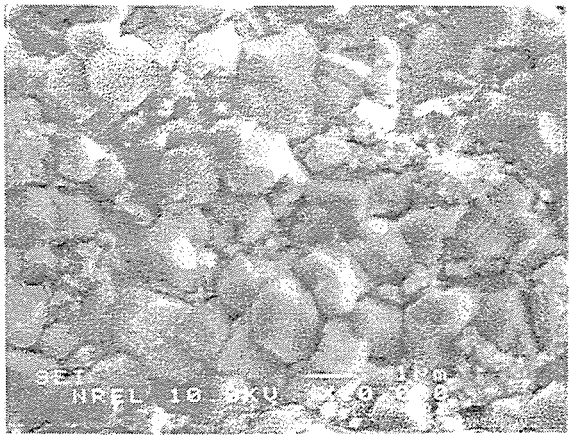


Figure 2.6: precursor with type I adhesion layer converted to CIGS in the Zeus

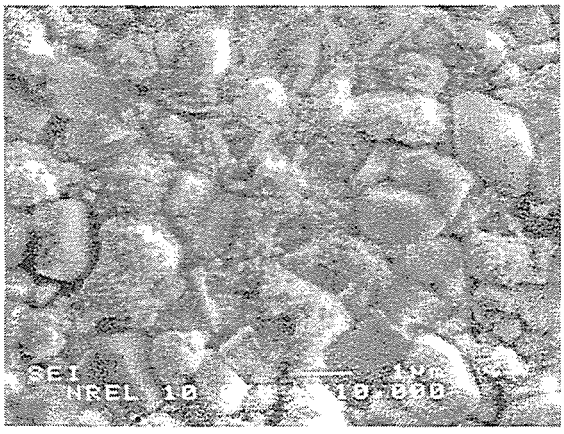


Figure 2.7: precursor with type II adhesion layer converted to CIGS in the Zeus

slightly inferior adhesion. The results of these analyses and comparison of devices formed on large-area films have led us to select the type I material for adhesion enhancement in current large-area CIGS formation recipes.

Table 2.1: EPMA at 20kVof CIGS films prepared in the Zeus.

sample	Cu	In	Ga	Se	Cu/(In+Ga)	Ga/(In+Ga)
704-18	24.29	23.43	0.95	50.34	0.957	0.077
720b-18	23.95	24.35	0.78	50.51	0.938	0.047

The CIGS films formed entirely in the pilot line were seen to be very different from the counterparts formed in the R&D reactor. Both CIGS films formed in the Zeus have a significant portion of the film surface covered by "mushrooms" of small-grained material growing from between large-grained (1μm) CIGS. The density of this coverage is significantly lower on the CIGS film formed on the type I adhesion layer. The differences in morphology between the CIGS films formed in the Zeus and R&D reactor is believed to be related to differences in Se delivery. The appearance of these "mushrooms" is not universal to all CIGS films prepared in the Zeus. An SEM of the CIGS surface from one of our better modules (740B) is notable for the absence of such structures (Figure 2.8).

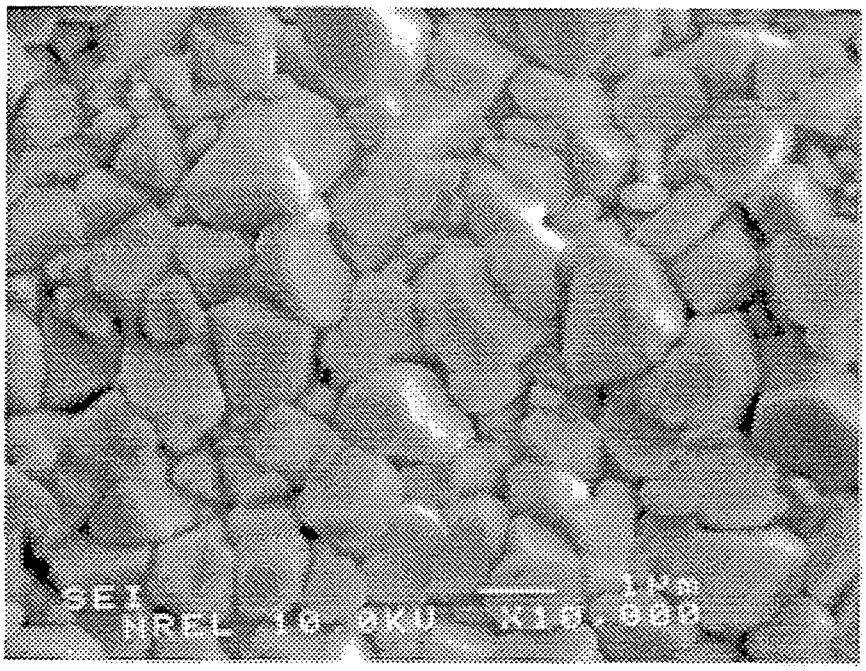


Figure 2.8: SEM of a CIGS film (740B) deposited in the pilot line (courtesy of A. Mason, NREL).

2.3 Composition

We periodically monitor the compositional uniformity of CIGS films deposited in the pilot line by EPMA. For example, samples were extracted from across the width of plate 740B, followed by removal of the CdS and ZnO by etching in a weak acid solution, and the samples were submitted for EPMA. The results of these analyses for Cu/(In+Ga) and Ga/(In+Ga) as a function of plate position are plotted in Figure 2.9. The deviations in Cu/(In+Ga) fall within the limits for good device performance. The ratio Ga/(In+Ga) as detected by EPMA is approximately 14%.

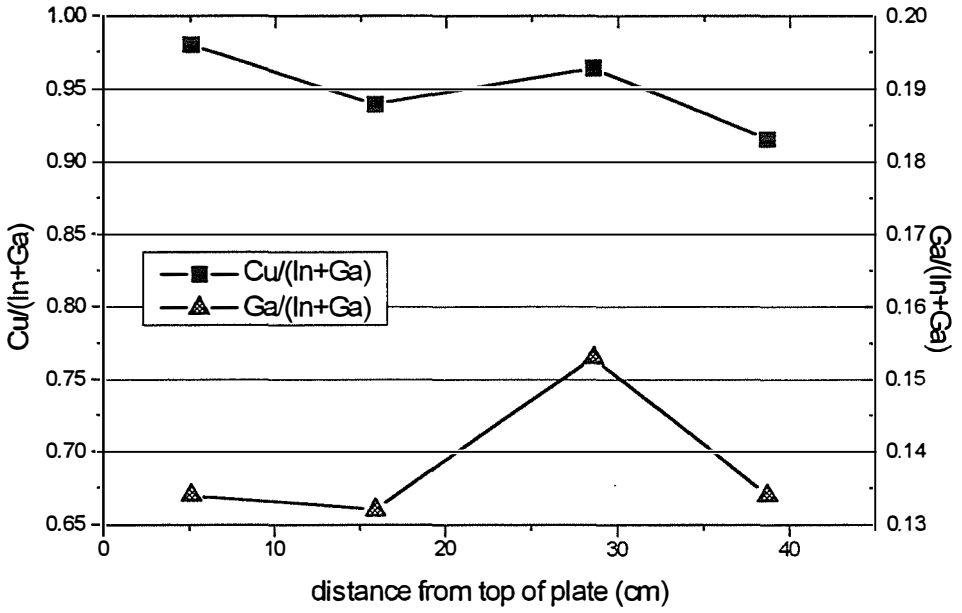


Figure 2.9: CIGS composition across the width of plate 740B as measured by EPMA at 20kV (courtesy of A. Mason, NREL).

The Ga, however, is distributed non-uniformly through the CIGS film. An Auger depth profile is shown in Figure 2.10 for a CIGS film removed from the same plate. The Ga was found to be exist primarily near the Mo back contact and at the surface of the film. We have tailored our deposition process to achieve this profile based on models that indicate such a profile is beneficial to device performance [5]. The subject of terminations is discussed further in Section 4.1.

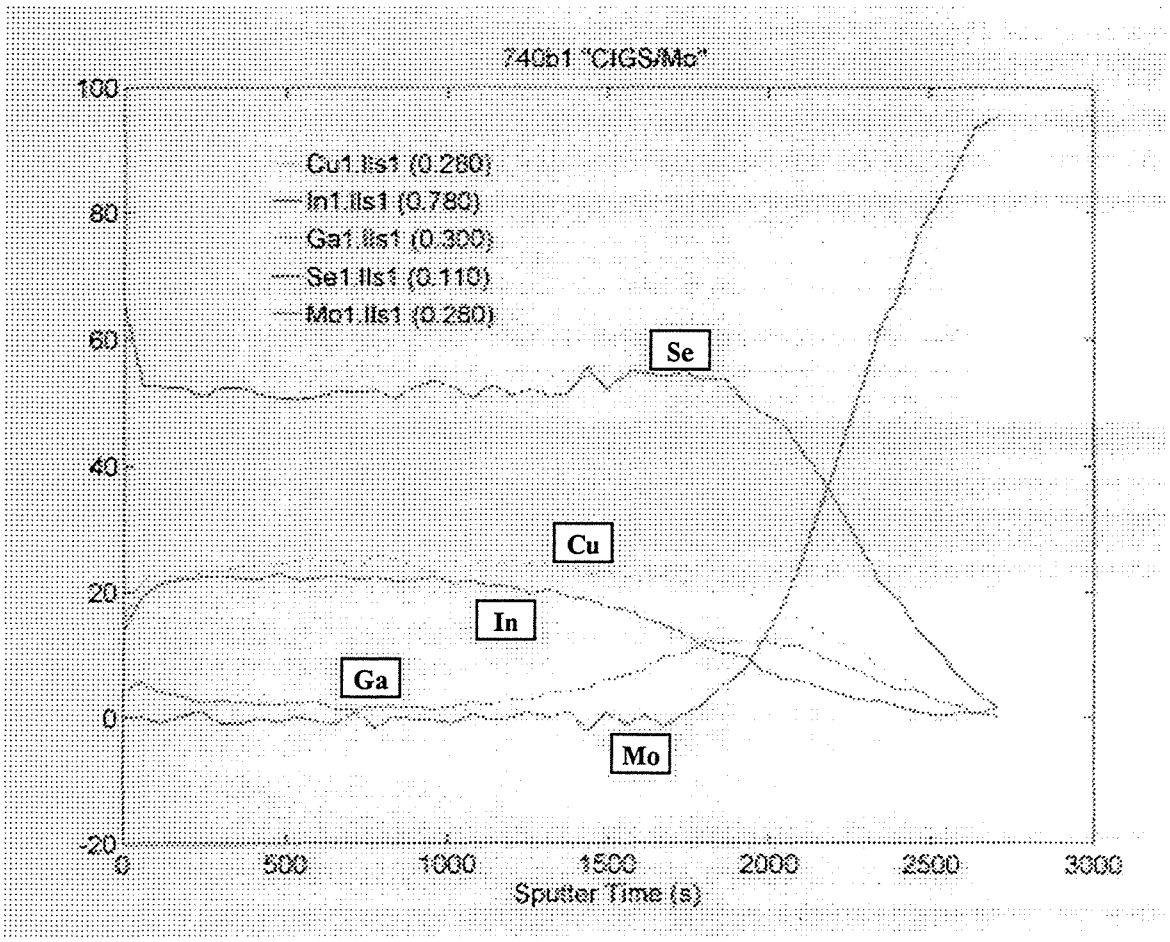


Figure 2.10: Auger depth profile of a CIGS film deposited in the pilot line (plate 740B). The approximate film thickness is 1.5 μm (courtesy of A. Swartzlander, NREL).

2.4 Impurities

Experiments was conducted to determine the effect of impurities on device efficiency. Two separate precursors were prepared by evaporation in an R&D system such that one had a higher concentration of impurities. This was achieved by not prebaking the system and evaporating the source materials at a higher system pressure than the standard method. All other deposition procedures were identical. The films were checked visually prior to selenization. The standard precursor, which terminates with an In film, was white in appearance, characteristic of a pure (un-oxidized) In film. The other precursor was gray in appearance, which has been correlated to an oxidized In film in prior experiments. The two films were selenized together and test devices were formed in the standard way with CBD CdS and ZnO. The IV characteristics are shown in Figure 2.11 and Table 2.2. The slightly oxidized precursor is clearly inferior to the standard precursor although the effect is not as dramatic as might be expected.

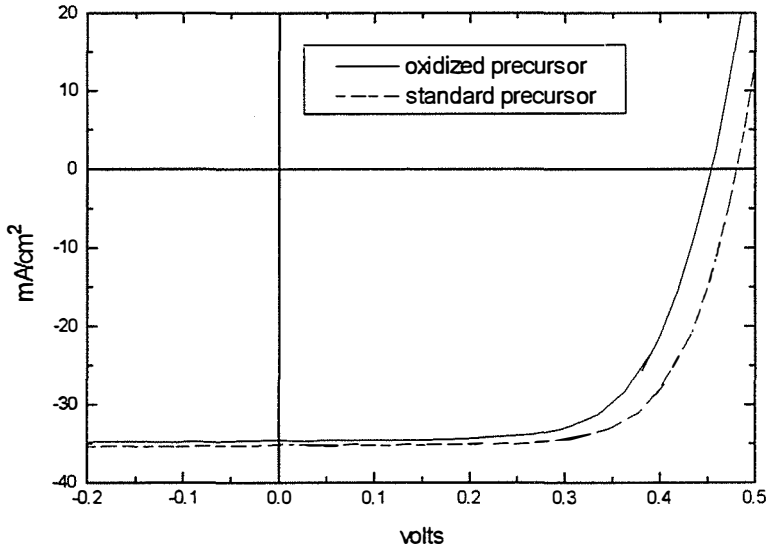


Figure 2.11: IV characteristics of CIGS devices prepared from standard and slightly oxidized precursors.

Table 2.2: device characteristics of CIGS devices prepared from standard and slightly oxidized precursors.

precursor	Voc (volts)	Jsc (mA/cm^2)	FF	Eff. (%)
standard	0.481	35.2	0.694	11.8
slightly oxidized	0.454	34.7	0.668	10.5

3.0 Junction Studies

Several groups have demonstrated efficient CIGS devices by replacing CdS with films of In_xSe_y, ZnSe, and other wide-bandgap materials [6,7]. We have investigated In_xS_y for this purpose because its bandgap is predicted to be larger than that of In_xSe_y and the potentially beneficial presence of sulfur near the junction. Another topic of interest is the use of chemical treatments of the absorber surface to improve device photovoltaic characteristics. Some potentially beneficial effects of such chemical treatments are the removal of CuSe and native oxides, passivation of the surface and grain boundaries or other modification of electronic properties in the vicinity of the junction. Understanding the effect of such treatments could lead to their replication using vacuum techniques.

3.1 In_xS_y buffer layers

In_2S_3 source material was evaporated to completion from a graphite effusion cell to avoid drifting of the source composition. Witness glass slides were located next to the Mo/CIS substrate during the deposition for optical and thickness measurements. The composition of the films deposited in this manner are unlikely to be stoichiometric In_2S_3 because of the lack of a significant

overpressure of S. Substrate temperatures were in the range 150°-250°C and film thicknesses ranged between 100-200nm. The transmission characteristics of In_xS_y films deposited on glass were found to be poor at a substrate temperature of 150°C and improved with increasing deposition temperature.

The illuminated JV characteristics of devices with standard window layers and In_xS_y buffer layers deposited on a common CIS film are listed in Table 3.1. The open-circuit voltages of the In_xS_y devices were consistently lower than the CdS device, but the J_{sc} and fill factor were similar in some cases. The quantum efficiencies of the best In_xS_y devices are lower than that of the CdS devices at wavelengths greater than 520nm but are greater at shorter wavelengths such that the short-circuit current densities are comparable. Improving the transmission characteristics of the In_xS_y films by optimizing the substrate temperature and film stoichiometry would allow thicker films to be deposited, with a potential improvement in device characteristics.

Table 3.1: JV characteristics of various device structures.

Device structure	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
CIS/In_xS_y/ZnO	382	34.7	62.5	8.3
CIS/CBD CdS/ZnO	431	34.3	65.5	9.7
CIS/ZnO	272	27.3	50.9	3.8

3.2 Surface Treatment

A novel surface treatment that consistently improves the photovoltaic characteristics of CIGS devices has been identified in the course of this investigation. The etchant is a cadmium-free compound, and the surface treatment consists of a brief dip in a heated solution of the compound, followed by a thorough water rinse. The improvement in efficiency was originally noted in direct CIS/ZnO devices where V_{oc} and fill factor were enhanced. Further experiments were conducted comparing the effect of the surface treatment on devices with the standard CIS/(CBD) CdS/ZnO structure and again there was a significant improvement in efficiency (Table 3.2). In many cases, this surface treatment also allows the use of significantly thinner CdS films, approximately 1/5 the standard thickness, with only a small reduction in efficiency. Further work is required to understand the effect of this surface treatment and replicate it in a vacuum process.

Table 3.2: JV Characteristics of CIS/CBD CdS/ZnO Devices.

Surface treated	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
no	389	28.0	60.9	6.6
yes	442	34.9	70.7	10.9

4.0 Device Analysis

4.1 Terminal evaporation stages

In contrast to experiments where we evaporate a significant percentage of the In-containing material at high temperatures to bring the film from the Cu-rich to the Cu-poor regime, we have also performed experiments where we deposit only a small amount of the total In at high temperature prior to cool down. With some CIS recipes, the devices significantly benefit from such terminations, with the effect seen primarily in the fill factor. Fig. 4.1 shows the FF of devices made on a film with a gradient in the ratio Cu/In across the substrate plane. Devices were made both on a region which received a termination layer of ~ 2% of the total In as well as on a region which received no termination. The FF is seen to decrease as the film becomes less Cu-poor for the device with no termination layer, while the FF is more constant across a wider compositional range for the device with the termination.

A high tolerance of device performance to variations in film composition is desired in manufacturing where a large module will display variations in composition and where the average film composition from module to module will also vary within some range. Proper engineering of the absorber surface may be a useful tool for achieving high compositional tolerance.

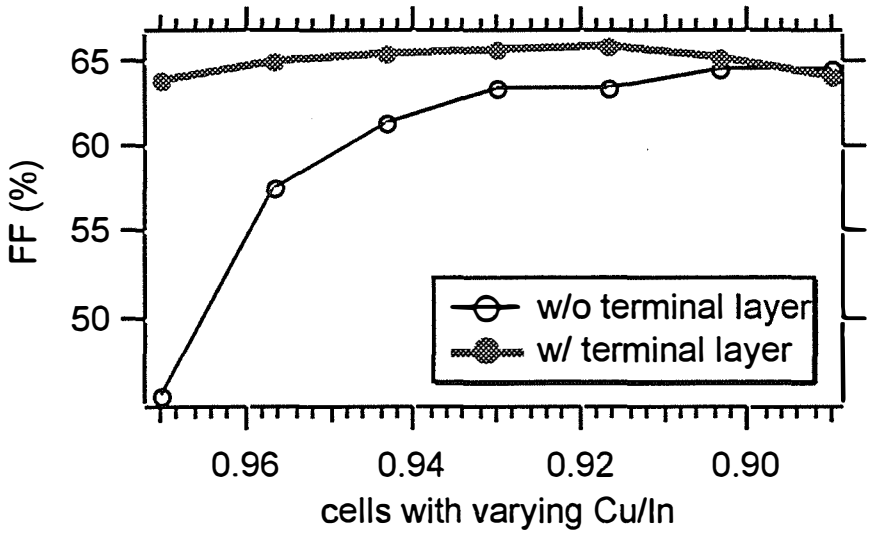


Figure 4.1: The FF of cells made on a compositional graded CIS film in regions with and without a terminal In-Se layer.

4.2 Pilot line precursor films

To accelerate the recipe development in the pilot line system, a program has been initiated to complete the formation of CIGS films from the pilot line in an R&D system. The R&D system allows for better control and monitoring than the pilot line provides. The importance of a variety of specific process parameters has been explored. The parameter space for several of the process steps has been found to be much larger than expected. For other process steps, the parameter space is smaller, and their limits have begun to be defined. It is encouraging to note that device

efficiencies of 10-12% were routinely made during the course of these experiments even though a wide range of processing parameters were explored, pointing out the inherent manufacturability of the process. The IV characteristics for the best device, with an efficiency of 12.7%, is shown in Figure 4.2.

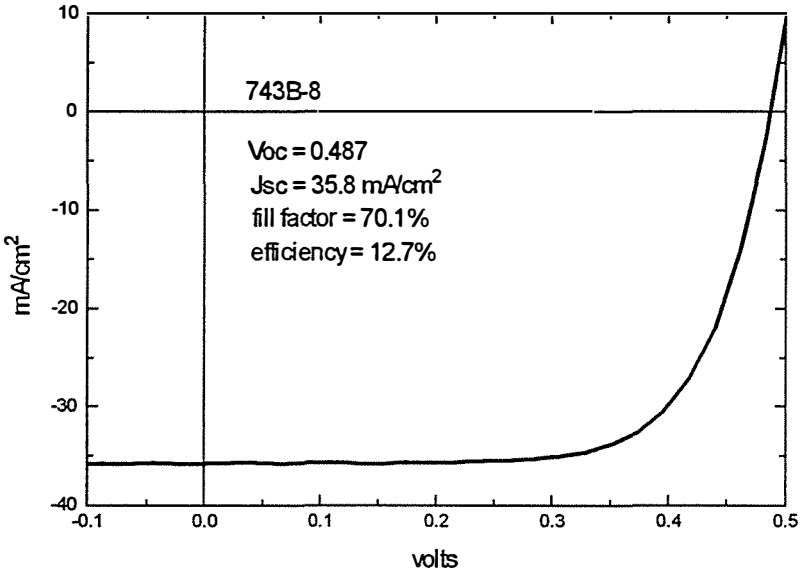


Figure 4.2: JV characteristics of a device made on a CIGS film formed in an R&D reactor using a pilot line precursor.

4.3 Throughput

The maximum processing time required for all module manufacturing steps is of considerable interest, particularly for those processes run in an in-line fashion. Most of the deposition processes can be accelerated simply by increasing temperature, power, or the number of deposition sources. For example, sputtering deposition rates can be increased by the application of greater power to a single cathode, or by adding additional cathodes. Evaporation rates can be increased by raising the source temperature or adding additional sources.

There is, however, little information available on the maximum reaction rates of metal and/or binary selenides with selenium to form CIGS. This information is critical to the proper design of manufacturing equipment to meet the desired throughput. Higher reaction rates would allow shorter reaction zones and lower capital costs required for vacuum equipment.

We have conducted experiments to gain insight about the potential tradeoffs involved with shorter selenization times. A standard precursor was prepared in the pilot line, sliced into sizes compatible with the R&D system, and the pieces were selenized for different times. The efficiency of devices made on the CIGS films is plotted in Figure 4.3 as a function of the total time of intentional Se exposure. This time does not include heat-up or cooldown times. A device efficiency of 10.5% was measured for the shortest Se exposure time attempted (4.5"). This

compares favorably with the device efficiency of 12.4% measured for a total Se exposure time of 33.4".

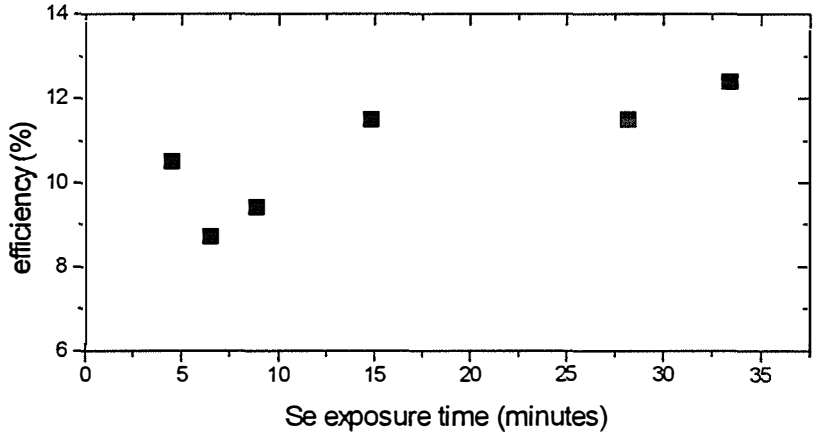


Figure 4.3: The efficiency of test devices formed from a CIGS precursor prepared in the pilot line for various selenization times.

4.4 Aging Studies

We have begun to investigate the effect of delays in processing between various deposition steps on device performance. This issue is important to understand for proper interpretation of experiments and for directing process flow in a manufacturing line. There are at least five intervals between process steps during which the influence of oxygen and water vapor on module performance may be important. They are 1) between Mo and precursor deposition, 2) between precursor deposition and CIGS formation, 3) between CIGS deposition and CdS deposition, 4) between CdS and ZnO depositions, and 5) between ZnO deposition and lamination.

Non-systematic observations lead us to believe that short delays between precursor deposition and CIGS formation are not serious. We have investigated the possible degradation of completed devices (with ZnO) during atmospheric, low-temperature (140°C) anneals and have identified processing conditions under which degradation does occur. The mechanism for the degradation is unknown, but it is not associated with interconnect resistance. Substantial degradation can also occur for delays between CdS and ZnO deposition if no special care is taken to protect the films. Figure 4.4 illustrates the degradation in device properties as a function of the interval of time between CdS and ZnO deposition for a single sample. The degradation was primarily in the device fill factor, with a slight drop in open-circuit voltage. Little or no effect on short-circuit current was observed. No special precautions were taken to protect the sample from normal environmental conditions during this period and no further degradation was observed once the sample was coated with ZnO. The efficiency of devices dropped by over 30% after 10 days; this is a substantial effect.

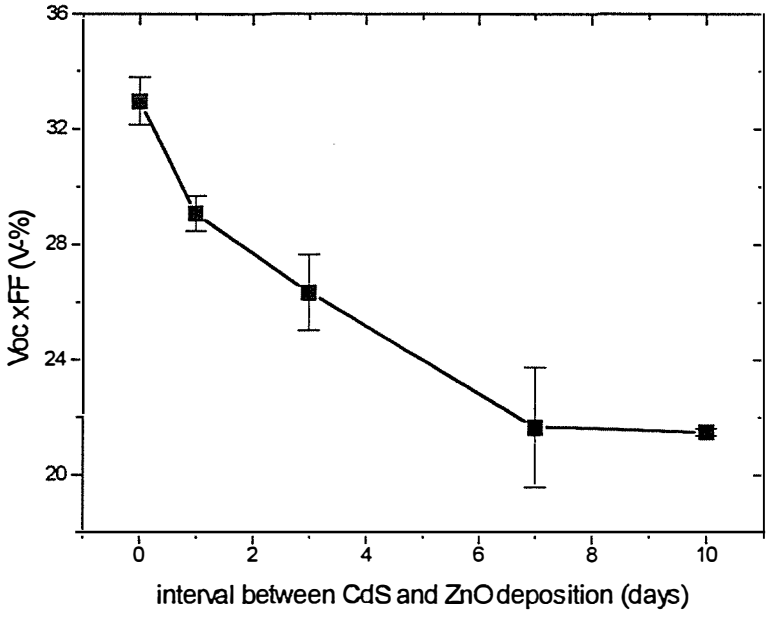


Figure 4.4: The Voc, fill factor product vs. the interval of time between CdS and ZnO deposition.

4.5 Measurement of Internal Resistance

A new method to determine the internal series resistance (vertical, not lateral) of thin film solar cells was developed. The method involves illumination of a small area of the cell with focused laser light sufficiently intense to make internal resistance effects easily observable. A description of the method and determination of the specific internal resistance in ohm cm^2 for CIS and CIGS cells has been published [8]. Similar equipment has now been set up at NREL to assist the failure analysis program.

5.0 Large Area Zinc Oxide

5.1 Quantification of Performance and Optimization Procedure

A further important task is optimization of the conducting ZnO applied to a CIGS module in order to maximize the module's efficiency. EPV currently employs pulsed bipolar sputtering of a $ZnO:Al_2O_3$ target in an Ar/O_2 atmosphere for coating 0.43 m^2 modules [9]. To a greater or lesser degree, all deposition variables affect the resulting ZnO:Al quality. Our approach to effective optimization has been a) to appropriately quantify the performance of different films, and b) to estimate performance of films prepared under new conditions to guide choice of future deposition parameters. A computer model that performs exact calculation of CIGS module efficiency for fixed CIGS parameters but with ZnO sheet resistance (R) and optical transmission (T) as input parameters is the tool that we have developed to quantify ZnO performance [10,11]. Using this program we find the iso-efficiency contours for CIGS modules as a function of ZnO R and T to be as shown in Figure 5.1. The open and closed circles represent measured R, T pairs for ZnO films on glass prepared using the large area process under various conditions (including O_2 flow) and with various thicknesses. The figure allows immediate identification of the most suitable films. Also shown in this figure are two heavy solid lines representing modeled R, T contours for films sputtered with two different oxygen flows (but under otherwise identical conditions) with film thickness as a variable parameter. Along these contours, film thickness increases from 0.5 μm to 3.0 μm. Curves such as these are used to select new deposition parameters. For example, for a given set of conditions, thickness should be chosen so that the heavy (R, T) contour is locally parallel to the iso-efficiency curves. In the presence of significant internal device series resistance, the iso-efficiency curves assume different slopes, as illustrated by the dotted lines in Figure 5.1. Under these conditions the ZnO should be thicker to limit excessive total resistance.

5.2 Influence of Scan Speed

To build up a ZnO:Al film of sufficient thickness to give the desired sheet resistance for use as the TCO on CIGS modules, multiple passes of the substrate under the cathode are generally performed. We may ask: Does film quality depend on the number of passes? Our earlier work had shown that a smaller number of slow scans gave superior properties than a large number of fast scans, and slow scans had been adopted. We have recently re-examined this area to determine if further improvements could be made. There are two aspects to the problem: 1) How does the conductivity of a single sublayer depend upon thickness, and 2) What is the relationship between final film conductivity and the conductivity of its constituent sub-layers? Two experiments were performed to investigate these questions.

In run IL104 a 38" long glass plate was fully coated with ZnO during a first scan under the cathode; for the 2nd scan only ¾ of the plate was coated; for the 3rd scan ½ of the plate, and for a 4th scan ¼ of the plate, resulting in 1, 2, 3, and 4 nominally identical sublayers in 4 different regions of the plate. Data from the 4 regions are shown in Table 5.1. The total film thickness (4 sublayers) was 6000 A, implying a sublayer thickness of 1500 A. Roughly speaking, the resistance fell with addition of sublayers according to a simple parallel arrangement of equal resistances (addition of conductances). However, a closer analysis reveals that the conductance contributed per sublayer increases significantly with the number of sublayers. Whether this

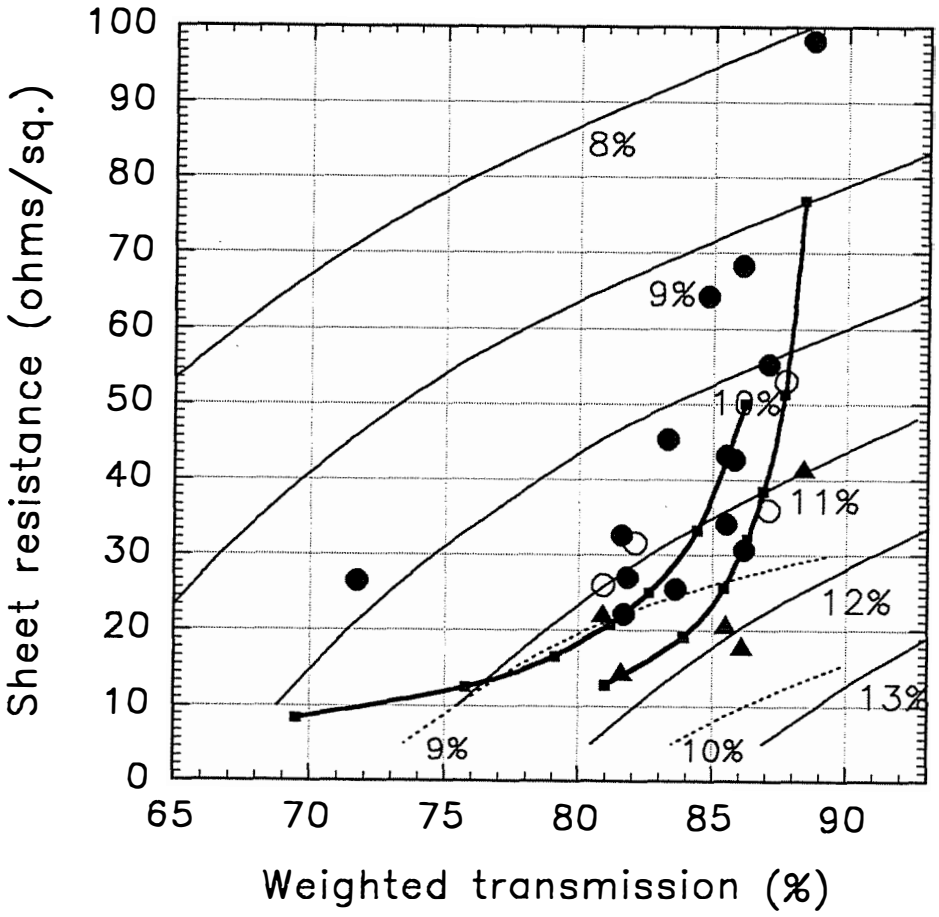


Figure 5.1 Iso-efficiency contours for CIGS modules as a function of zinc oxide sheet resistance and transmission

represents a reduction in impurities, increase in grain size, annealing, or reduction in boundary scattering is not clear.

Table 5.1. Resistance, conductance, and incremental conductance for ZnO films consisting of 1, 2, 3, and 4 nominally identically sublayers.

# of films	$R_\square$ ($\Omega/\square$)	$1000/R_\square$	avG/film	ΔG
1	187	5.35	5.35	5.35
2	86.4	11.57	5.79	6.23
3	56.2	17.79	5.93	6.22
4	40.8	24.51	6.13	6.72

In run IL105, 6 scans were made at the usual scan speed over one half of the plate, while 3 scans were made at approximately half the scan speed over the other half of the plate to maintain approximately the same film thickness. From Table 5.2 it can be seen that the film consisting of 3 sublayers had a substantially higher conductivity than the film consisting of 6 sublayers (229 vs. 179 Ω^{-1} cm^{-1}) and that, despite being slightly thinner, the 3 sublayer film had a sheet resistance usefully lower (by over 11%) than the 6 sublayer film. The weighted transmissions of these films were almost equal, the 0.7% inferior transmission of the 3 sublayer film being more than compensated for by the lower sheet resistance if the films are compared on an iso-efficiency contour plot for CIGS modules. It therefore appears that the large area ZnO can be further slightly improved through use of even slower scan speeds.

Table 5.2. Properties of 0.43 m^2 ZnO:Al films produced by pulsed bipolar sputtering of an oxide target including comparison of as-deposited and annealed films.

Run #	t (A)	condition	T_{IR} (%)	T_{VIS} (%)	T_W (%)	cond. $(\Omega\ cm)^{-1}$	$R_\square$ ($\Omega/\square$)
IL99	9,400	as dep.	72.8	69.5	71.7	401	26.5
IL100	8,800	as dep.	82.1	80.7	81.6	349	32.6
		annealed	80.9	81.0	80.9	517	22.0
IL101	11,300	as dep.	82.9	79.2	81.7	399	22.2
		annealed	81.7	81.5	81.6	615	14.4
IL102	8,550	as dep.	87.1	82.4	85.5	342	34.2
		annealed	86.1	84.2	85.5	568	20.6
IL103	11,100	as dep.	87.5	83.5	86.2	293	30.7
		annealed	85.9	86.3	86.0	506	16.4
IL104		as dep.	91.0	90.9	91.0		187(1)
			90.1	85.8	88.7		86.4(2)
			86.8	81.8	85.1		55.9(3)
			85.6	79.8	83.7		40.8(4)
IL105	9380	as dep.	91.2	82.5	88.3	179	59.5
	8280*	as dep.	89.4	84.2	87.7	229	52.7
IL107	5660	as dep.	87.6	81.2	85.5	409	43.2

* number of passes halved and scan speed approximately halved.

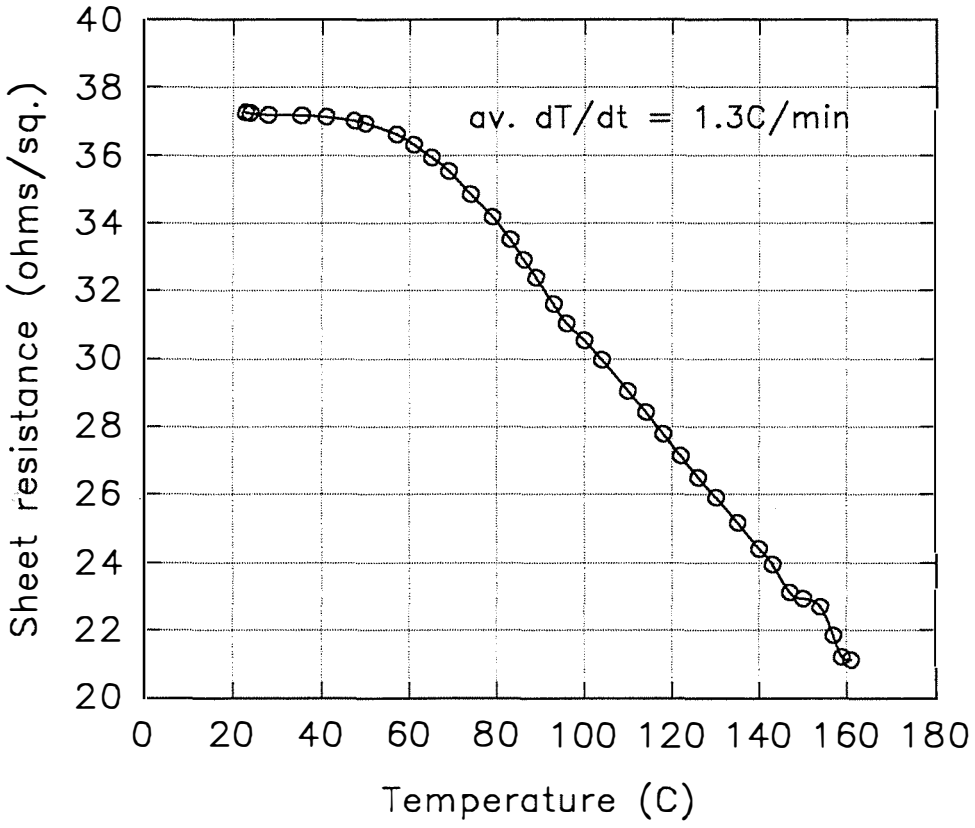


Figure 5.2 Sheet resistance of bipolar sputtered ZnO:Al during vacuum annealing

5.3 Annealing Behavior

Properties of some of the films prepared by pulsed bipolar sputtering from a bonded $ZnO:Al_2O_3$ target are shown in Table 5.2. Films sputtered from this target have exhibited large decreases in sheet resistance upon annealing (again see Table 5.2). Eight films have been annealed so far (2 in air in an oven at 110 °C, 5 in air at 130 °C under heat lamps, and 1 ramped to 160 °C under vacuum in a dewar) and all exhibited a similar decrease in sheet resistance. Annealing times were 1-2 hours. Data from the vacuum annealing are shown in Figure 5.2. Starting at about 60 °C, the film exhibited a steady decrease in resistance as its temperature was raised to 160 °C. The final resistance was 0.56 times the starting value. No increase in resistance has been observed during 2-3 weeks storage at room temperature, suggesting that the increased conductivity is permanent. Most importantly, a similar effect was found for ZnO deposited on CIS/CdS to complete the device structure. In this case, annealing under heat lamps for 110 minutes at 130 °C led to a decrease in sheet resistance from 25 Ω/□ to 15 Ω/□.

The effect of the annealing on optical transmission (for ZnO on glass) was found to be quite consistent - a small decrease in IR transmission coupled with a small increase in visible transmission such that the weighted transmission $(2\ T_{IR} + T_{VIS})/3$ was approximately constant or decreased by about 1% (see Table 5.2). The five solid triangles in Figure 5.1 represent (R, T) pairs for annealed ZnO films on glass. We have confirmed that a similar reduction in resistance is obtained for ZnO on CdS/CIGS. This implies that a useful improvement in ZnO quality on completed CIGS plates should be achievable by annealing.

5.4 Standard film properties

After completing the film optimization process a standard set of conditions for the large area ZnO was arrived at. Even so, it was found that scrubbing the target to remove powder resulted in a substantial increase in deposition rate which in turn necessitated an increase in the optimal oxygen flow. Relaxation of these parameters to steady state values took several weeks, during which time monitoring of the films and adjustment of the process were required to maintain optimal film properties. Standard film properties are shown in the table below.

Table 5.3 Properties of current large area ZnO:Al

Thickness (A)	Sheet resistance (ohms/sq.)	Conductivity $(ohm\ cm)^{-1}$	T_{VIS} (%)	T_{IR} (%)	T_W (%)
9000	27	412	80.0	82.7	81.8

5.5 Effect of Zinc Oxide Resistance on Module Fill Factor

Figure 5.3 shows the calculated dependence of CIS module fill factor upon ZnO sheet resistance, with irradiance as a variable parameter. Previously reported modeling efforts have shown that the optimal sheet resistance for high quality RF sputtered ZnO:Al on 0.5 cm wide CIS cells is about 12 ohms/square [10]. From Figure 5.3 we deduce that the use of 27 - 30 ohm/sq. ZnO would decrease the module fill factor at 1 sun from 0.65 to 0.58 or 0.57, a loss of 10-12%.

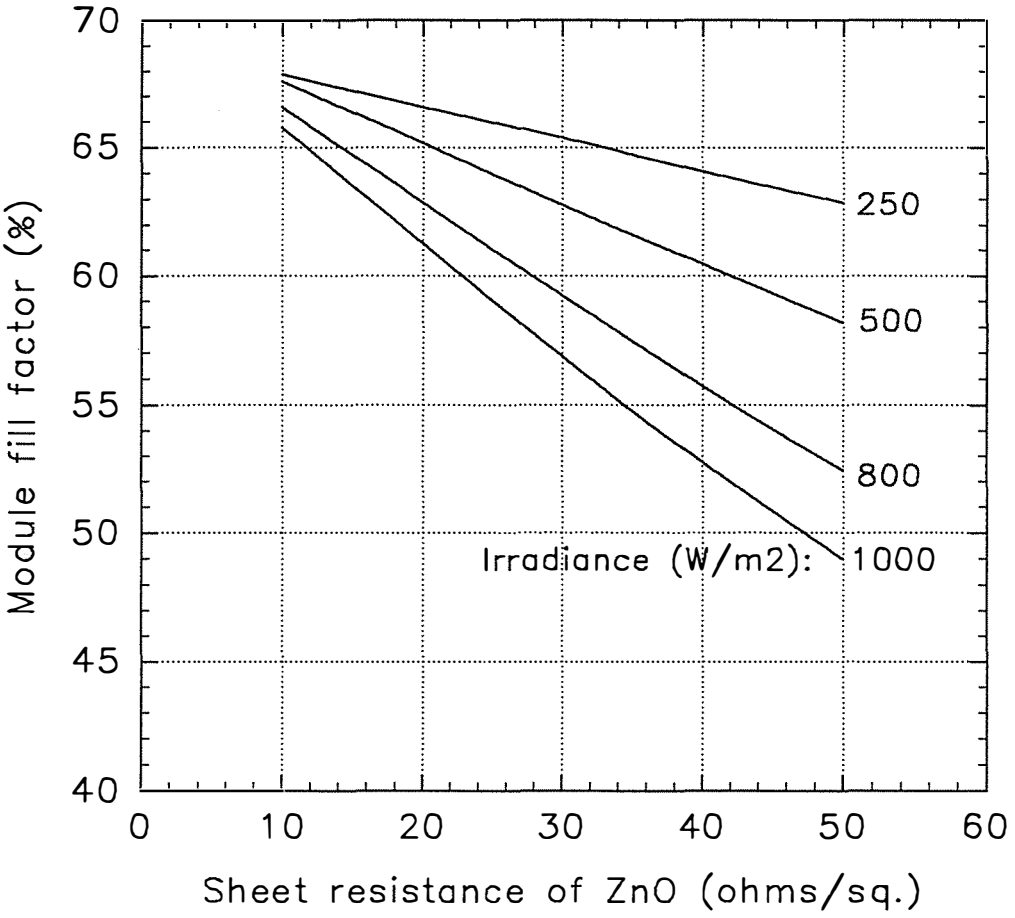


Figure 5.3 Calculated dependence of fill factor of modules utilizing high quality CIS on ZnO sheet resistance, at various levels of irradiance.

6.0 Module Formation

6.1 Process Sequence

The overall processing sequence for module formation is shown in Figure 6.1. Also shown are intermediate quality control procedures that can be applied as required. Several, although not all, of these are routinely performed.

Operation	QC
	Determine tin side
1.Wash glass	
2. Sputter Mo	
	Contactless sheet res.
3. Laser	
	Check isolation
4. Deposit precursor	
	Mass
5. Compound formation	
	Resistance
6. Deposit CdS	
	Color & transmission
7. Sputter ZnO (1)	
	Monitor R; diagnostic Voc, Isc
8. Pattern	
9. Sputter ZnO (2)	
	Monitor R
10. Pattern	
	Measure module I-V & diagnostic I-V
11. Prepare for lamination	
12. Vacuum laminate	
	I-V and visual inspection
13. Attach boot	
	I-V

Figure 6.1 Processing sequence and quality control procedures for CIGS module fabrication.

6.2 Patterning

The function of the first patterning step is to separate the Mo into isolated strips. Two methods have been successfully employed by EPV. The first method to be developed was a proprietary (non-laser) technique and small submodules up to 9.6% in efficiency were prepared using this method [3]. However, development of a viable laser patterning process for the Mo has now been

accomplished, and this process is currently preferred because of reduced area loss and greater reliability. The following parameters were optimized in order to achieve satisfactory laser scribing of Mo: glass orientation, laser wavelength, pulsed vs. continuous beam, beam power, table speed, and other factors.

The second and third patterning steps (exposure of Mo through cuts in the CIGS, and separation of the ZnO) are routinely made by mechanical scribing using one or more knife blades and plate translation.

6.3 Lamination

Preparation of the patterned CIGS plate for lamination includes attachment of metal foil bus bars, drilling of the substrate, and removal of films around the periphery of the substrate. The layout of a monolithic CIGS plate prior to lamination is shown in Figure 6.2. Lamination is performed in a vacuum laminator using fast cure EVA in sheet form. Electrical connections to the module are made via two strain-relieved, insulated wires that are connected to the foils under an environmentally protected boot of silicone RTV.

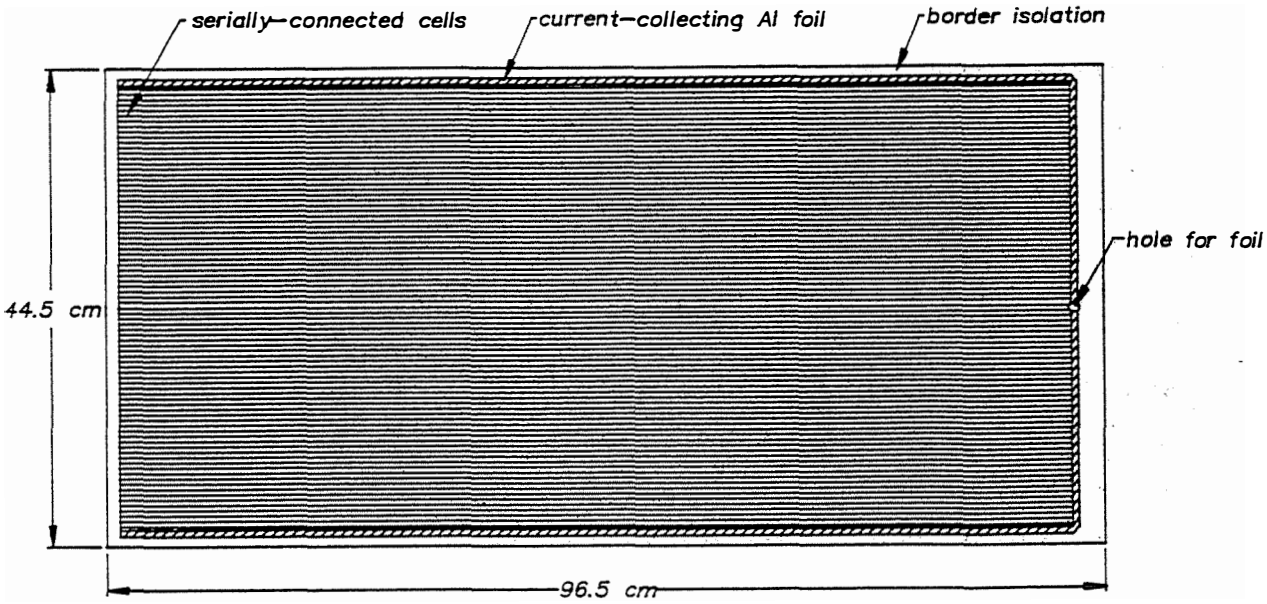


Figure 6.2 Layout of monolithic CIGS plate prior to lamination.

7.0 Module Performance and Analysis

7.1 I-V Equipment

Six types of I-V measurement on CIGS devices and modules are currently in use. Four of the six are interfaced to one particular computer fitted with A/D and D/A boards. The fifth is performed by a portable analog instrument, and the sixth is conducted on a computerized flash test system built for a-Si:H modules. The 6 measurements are listed below:

1. indoor module I-V using 8 halogen lamps
2. outdoor module I-V in sunlight (4-wire configuration)
3. indoor device I-V using single tungsten halogen lamp
4. indoor diagnostic I-V using halogen lamps
5. indoor or outdoor module P_{MAX} measurement (using an analog multiplier)
6. indoor module I-V in 2 ms using 3 xenon flash lamps

7.2 CIGS Module Performance

CIGS plate Z797 exhibited a P_{MAX} of 27.7 watts as measured in sunlight under essentially standard test conditions. This represents an aperture area (3948 cm^2) efficiency of 7.0%. The plate was shaded from direct sunlight and the back glass temperature was measured using a thin film Pt resistance element. The temperature was 26 ° C. The I-V curve shown in Figure 7.1 was measured immediately after uncovering the module. The V_{OC} of 37.2 V represents an average V_{OC}/cell of about 448 mV. The module fill factor of 54.5% is the best yet achieved for a large module. After allowing the module to reach an equilibrium temperature (about 39 ° C, in the presence of gusts of wind) a power output of 24.8 W was recorded. The temperature coefficients deduced from this quick experiment were I_{SC} - 0.02%/C, FF - 0.23%/C, V_{OC} - 0.58%/C, P_{MAX} - 0.81%/C. These coefficients are slightly higher than expected, and will be re-determined on windless days with other modules.

An earlier plate, Z740B, was laminated and sent to NREL for efficiency verification. Figure 7.2 shows the I-V curve obtained in sunlight for this module. The encapsulation employed EVA and a low-iron cover glass. The aperture area of this module was 3156 cm^2. It produced 19.7 watts at 997 W/m^2 (V_{OC} 37.4 V, I_{SC} 1.00 A, FF 52.6%) with an average V_{OC} per cell of 456 mV and an aperture area efficiency of 6.25%.

Figure 7.3 shows a histogram of module powers obtained for *all* processed plates with run numbers > 730. The remarkable progress made in module power subsequent to about run 700 is largely due to adoption of EPV's new "hybrid" process for CIGS formation, with contributions also from improved and thicker ZnO, lasering of Mo, and reduced area loss.

EPV's unique capability to produce both a-Si:H and CIGS monolithic PV plates prompted the fabrication of a number of exploratory a-Si:H/CIGS tandem modules. This was done by laminating an a-Si:H plate onto a CIGS plate to form a 4-wire module. Both single junction and double junction a-Si:H plates were used. For one particular a-Si/a-Si/CIGS module, I-V curves were obtained in sunlight for the following configurations: parallel connection of the two

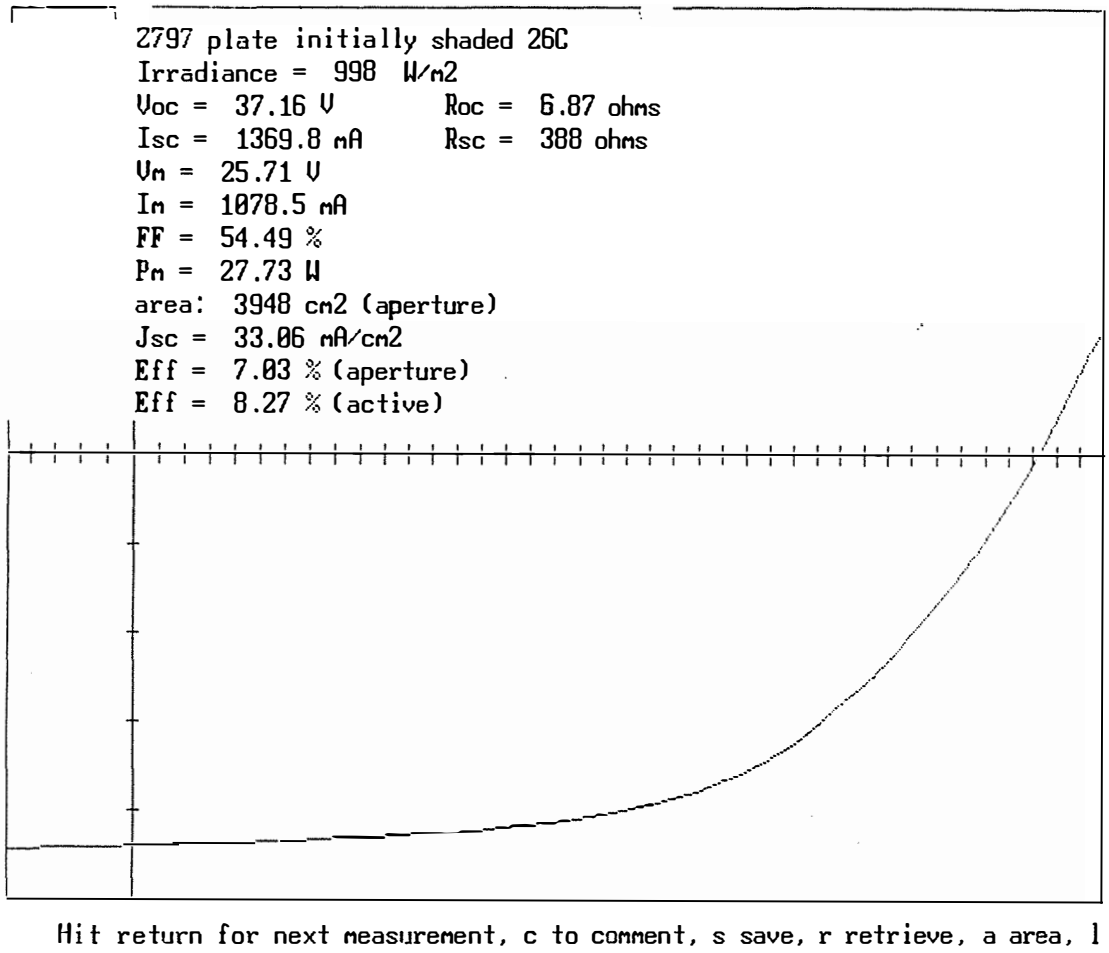
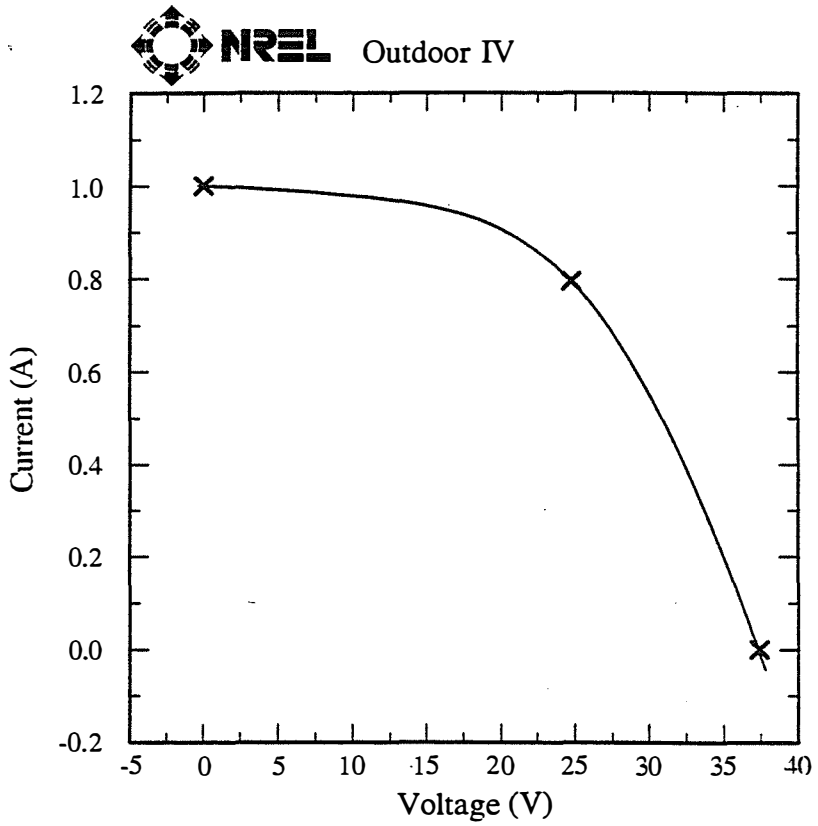


Figure 7.1 I-V curve in sunlight of a 7.0% CIGS plate producing 27.7 W (aperture area 3948 cm^2).

EPV CIGS Module

Sample: Z740B
Apr 3, 1997 1:53 PM MST
device Temperature = 24.9°C

area used = 3156.5 cm2
997.2W/m^2 fixed tilt
Si Ref. cell #294278



V_{oc} = 37.39 V
I_{sc} = 1.001 A
Fill Factor = 52.58 %
Efficiency = 6.25 %

V_{max} = 24.74 V
I_{max} = 0.7954 A
P_{max} = 19.68 W

device dimensions = 76.8x41.1 cm

Air temperature = 18.1°C, Air mass = 1.35, POA sun angle = 27.4°
total irradiance from K&Z CM11 = 999.2 W/m^2

Figure 7.2 I-V curve as measured by NREL in sunlight confirming 6.25% efficiency for a 3156 cm^2 glass-glass encapsulated CIGS module.

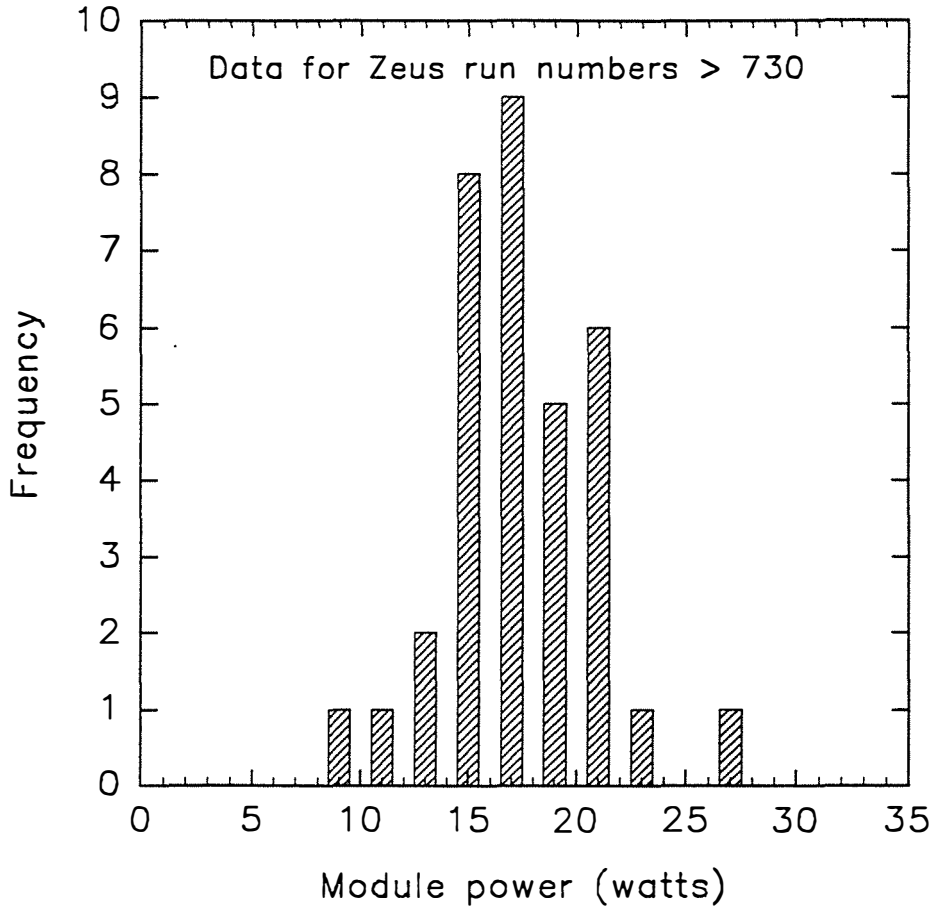


Figure 7.3 Histogram of module powers for all processed plates subsequent to run #730.

circuits, a-Si/a-Si component alone, and CIGS component alone (as filtered by a-Si/a-Si plate and EVA). The powers (normalized to 1000 W/m^2 incident) are shown in the Table below.

Table 7.1 Powers produced by a-Si/a-Si and CIGS circuits of a 4-wire a-Si/a-Si/CIGS module.

Configuration	Power (W)
Parallel connection	23.8
a-Si/a-Si alone	22.6
CIGS alone (filtered)	6.8
Sum of separate powers	29.4

The disparity between the sum of the separate powers (29.4 W) and the power produced under parallel connection (23.8 W) is due to the mismatch between V_{MAX} of the two circuits. For the a-Si/a-Si circuit the V_{MAX} was 31.4 V, while for the CIGS it was 17.9 V. It is noteworthy that the overall efficiency of the module connected to separate matched loads is 7.6%. Future work will address choice of more optimal tin oxide sheet resistance, adjustment of zinc oxide parameters, and correct a-Si and CIGS cell widths to achieve proper current matching in a series connection.

7.3 Diagnostic I-V

Following the third patterning step, foils are attached and the module I-V curve is measured. This measurement, however, gives little information about the uniformity of cell performance across the surface of the plate. Much valuable information would be gleaned if a local I-V curve could be obtained. Recall that early diagnostic measurements of open-circuit voltage and short-circuit current were described in Chapter 1, but fill factor could not be measured. For some time, therefore, for the purposes of analysis, small cells were defined by scribing the CIGS and opening an adjacent contact to the Mo, and were then measured in the usual way, thereby allowing determination of fill factor. More recently, a new measurement technique was devised and implemented to enable device fill factor and open-circuit voltage to be determined locally across a patterned CIGS plate and, most importantly, in a non-destructive manner.

Figure 7.4 shows the best I-V characteristic obtained so far using the new local diagnostic technique. The diagnostic was performed on CIGS plate Z797. The absolute V_{OC}, V_M, and FF values are 466 mV, 363 mV, and 69.2%. With an estimated current density of 34.1 mA/cm2, the intrinsic device efficiency is at least 11.0%, since the fill factor determination includes any interconnect resistance.

A fairly coarse mapping of V_{OC} and FF is shown in Figure 7.5 for the same plate. On the whole, the response was reasonably uniform. Nevertheless, the mapping clearly revealed that V_{OC} and FF declined significantly towards one of the long edges of the plate over a distance of 4 - 5 inches. No strong variations were observed along the long axis of the plate, although a small gradient was detected.

The data taken during such diagnostic testing can also be used to estimate the local ZnO sheet resistance. For plate Z797 this was found to be 26 - 28 ohms/square.

It is anticipated that, once this diagnostic technique is incorporated into routine plate monitoring, the data will be invaluable for prompting diagnosis and correction of non-uniformities in precursor stoichiometry, plate temperature, termination layer thickness, and possibly Se delivery. It will also serve to help quantify the relative contributions of intrinsic device fill factor and ZnO sheet resistance to overall module fill factor.

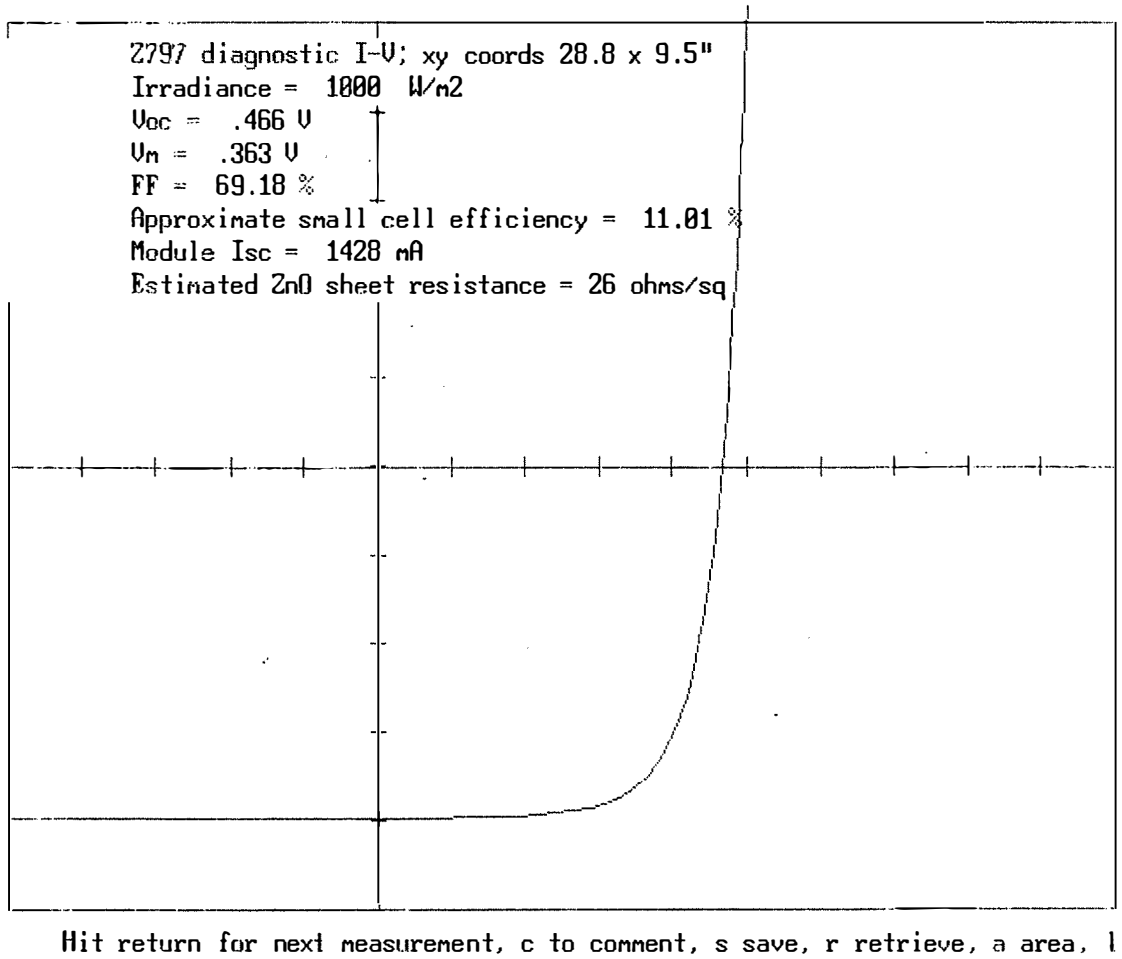


Figure 7.4 Local I-V curve obtained at a particular position on a full size CIGS plate demonstrating an intrinsic device fill factor of 69%.

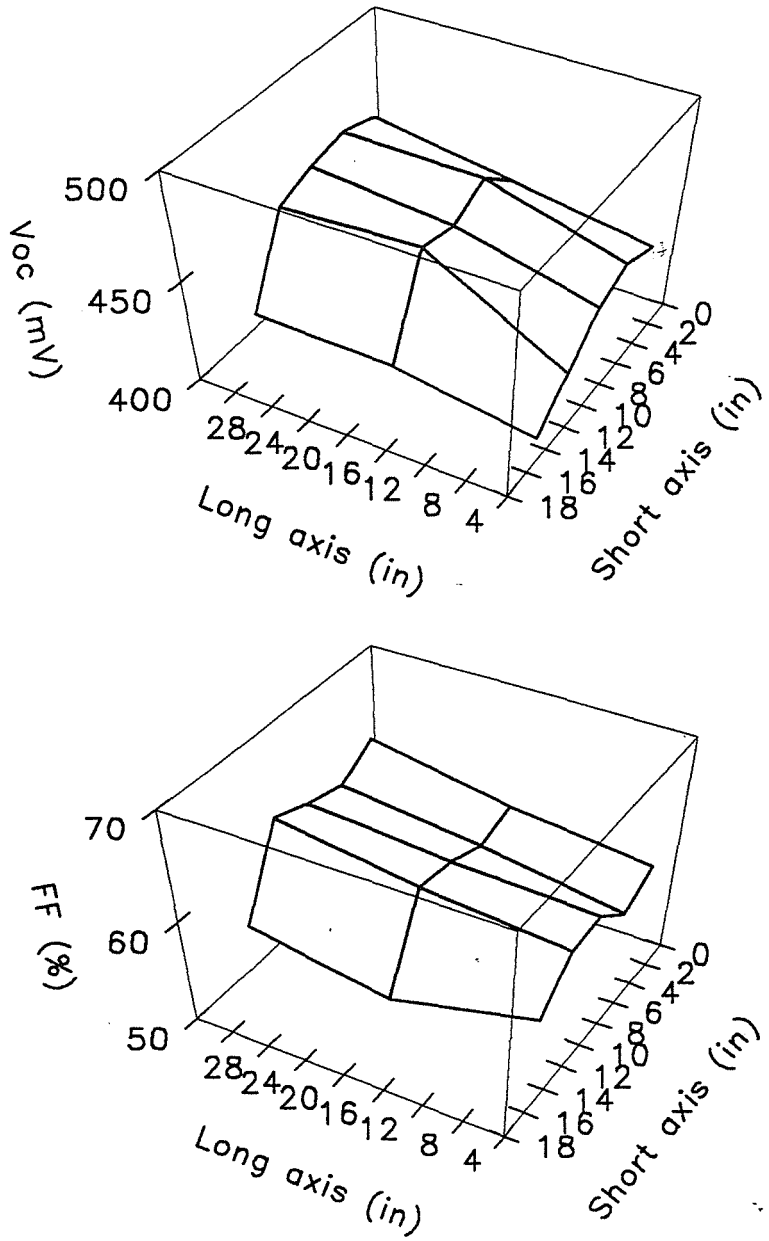


Figure 7.5 Non-destructive mapping of V_{OC} and FF for a full size CIGS plate using a new diagnostic technique.

7.4 Encapsulation and testing issues

It has been observed that some plates, after encapsulation, have lost a considerable amount of their power output compared to that originally generated by the unencapsulated plate. On the other hand, many plates do not degrade at all upon lamination, and some appear to increase slightly in power. To investigate these effects, I-V curves are run after each step during the preparation of the plate for lamination, after lamination, and after booting. The principal cause of the degradation appears to be exposure of the cell structure to elevated temperatures. We believe the degradation to be completely avoidable by appropriate CIGS formation and cell processing. Elimination of these effects will be an area of focus during Phase III. Despite optical losses after lamination, the slight improvement in some modules is believed to be due to a reduction of ZnO resistance through annealing.

CIS-based modules can also differ in their light soaking behavior. The principal effect is a dependence of measured fill factor upon the duration of light exposure after dark rest. In contradistinction to a-Si:H, the light soaking (if present) is universally in the direction of increasing fill factor with light exposure time. For modules that exhibit this effect, it is readily observed by recording successive I-V curves under steady light irradiation. A serious underestimate of the true, steady state fill factor can occur if such modules are measured after dark rest using a pulsed (flash) simulator. However, the best CIS and CIGS modules usually do not light soak, and repeated I-V curves made under continuous illumination then exhibit a decline in power output due to voltage loss upon heating. Again, we believe that identification and control of the relevant process parameters will eliminate the production of underperforming modules that light soak.

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13. ABSTRACT *(Maximum 200 words)*

This report describes work performed during the second year of a three-phase, 3-year, cost-shared subcontract . The subcontract is one component of the NREL Thin Film PV Partnership Program. Energy Photovoltaics, Inc. (EPV) explored novel CIGS formation recipes that can be implemented on a unique pilot line constructed to coat substrates 4300 cm^2 in area. One particular feature of this line is the use of linear sources capable of downwards evaporation. EPV experimented with several types of recipe, and a "hybrid" process was found to simultaneously yield the desired combination of properties—good adhesion, device efficiency, uniformity, and reproducibilty. At the device level, significant results were obtained using alternative buffer layers, direct ZnO devices, and chemical treatment of the CIGS, and a new method was developed and transferred to NREL to enable measurement of device-specific internal resistance. Also, considerable effort was put into complete module fabrication, testing, and analysis. A reliable procedure for laser scribing the molybdenum was developed, the chemical-bath deposition of the thin CdS layer was made more efficient in terms of material use, the bipolar sputtering process for large-area ZnO was further optimized to yield films with 80% transmission and less than 30 ohms/square sheet resistance, and a new, non-destructive technique was developed to obtain local I-V curves at selected locations on a patterned plate. A fully encapsulated 3156-cm^2 CIGS module sent to NREL for testing produced 19.7 W in sunlight at 997 W/m^2 irradiance, corresponding to an aperture-area efficiency of 6.25%.

14. TERMS

photovoltaics ; $Cu(In,Ga)Se_2$; CIGS ; Thin Film PV Partnership Program ; high-efficiency photovolataic devices ; high-throughput manufacturing

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