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Market-Driven EFG Modules

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PREFACE

This Annual Technical Progress Report covers the work performed by ASE Americas, Inc. for the period December 14, 1995 to December 13, 1996 under DOE/NREL Subcontract Number ZAF-6-14271-13 entitled "Market-Driven EFG Modules". This is the first Annual Technical Report for this subcontract. The subcontract is scheduled to run to December 13, 1998.

The following personnel at ASE Americas have contributed to the technical efforts covered in this report.

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CQB Associates
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Harvard University

SUMMARY

This report summarizes the progress made at ASE Americas Inc. during the first year (Phase I) of the planned 3 year program in Phase 4A2 on the development of technology to address its photovoltaic module manufacturing flexibility and cost reduction for its products. This program focusses on advancing manufacturing technology to reduce the thickness of EFG wafers from 300 to 250 microns, to raise EFG solar cell efficiency to be able to produce cells with average efficiency of 15.5% on 10 cm x 10 cm area wafers, and to simplify processes and reduce costs in interconnect and module manufacturing. This work includes the development of a novel and new environmentally safe and reduced cost diffusion glass removal process for the solar cell manufacturing line. The overall goal of the program is to reduce EFG module manufacturing costs by 25%. Module cost reductions of approximately 7% can be identified as a result of successes on the program in the first year. The work in Phase I has been subdivided into efforts in three areas: Task 1: Wafers, Task 2: Cells, and Task 3: Modules.

Task 1: Wafer Manufacturing

Efforts are underway to improve the electronic quality of silicon wafers produced by the EFG method for producing multicrystalline silicon. Tasks in this area include the reduction of impurity levels in the components of EFG furnace crystal growth furnaces, the exclusion of impurities from the ambient environment through the construction of enclosures around the growth furnaces, and the optimization of growth variables, e.g. growth speed and the gas composition within the furnaces. These improvements will reduce module cost solely by increasing the power output of the finished module, at a fixed manufacturing cost. A second effort in the wafer area is a project to automate the silicon feedstock sorting process, to reduce labor cost and prevent feedstock contamination. Another effort is the reduction of silicon consumption by growing thinner EFG tubes, which also will improve cell efficiency. Part of this effort requires improvements in laser cutting technology to reduce breakage of wafers and tubes during cutting, a problem which increases as wafer thickness decreases.

Improvements in graphite purity and feedstock sorting are estimated to have resulted in a 2.5% reduction in module manufacturing costs in the manufacturing line during Phase I.

Task 2: Cell Manufacturing

Work in the cell manufacturing area falls into three categories. The first consists of improvements in the cell itself, e.g. reduction of reflection losses and optimization of the emitter grid, to improve cell efficiency. The second is a direct reduction in manufacturing cost by a reduction of chemical consumption, waste treatment, and labor costs associated with the phosphorus diffusion glass removal process. The third is a change in cell design to simplify the process of interconnecting cells into strings for the manufacture of modules.

Cell efficiency improvements during the first year of this program are estimated to have contributed a 2.5% reduction in module manufacturing costs.

Task 3: Module Manufacturing

Improvements in module manufacturing are aimed at simplifying cell interconnection, reducing the time required for the lamination process, reducing cell breakage during lamination, reducing the cost of diode housings and junction boxes, and reducing both the cost of module frames and labor required to attach them to the module. Module performance will also be improved by making maximum use of light that strikes the areas between cells, most of which is normally lost.

The improvements in module framing and diode housings offer a potential of a 2% reduction in EFG module manufacturing costs in the second half of 1997.

Accomplishments

Accomplishments during the reporting period include:

Task 1: Wafers

- Improvements in graphite purity in EFG crystal growth furnaces, improving wafer quality
- Optimization of EFG crystal growth rate
- Increased die run length due to reductions in the use of carbon monoxide during EFG crystal growth
- Completion of engineering and design work for EFG growth furnace enclosures
- Feasibility demonstrated for the reduction of EFG wafer thickness from 300 μm to 275 μm
- Design and testing of a system to reduce costs of silicon feedstock sorting prior to EFG crystal growth
- Testing of new carbon dioxide and copper vapor lasers for improved cutting of EFG wafers from octagon tubes

Task 2: Cells

- Improvements in cell diffusion conditions resulting in increased cell efficiency
- The completion of process design for a new approach to remove phosphorus glass from diffused wafers, reducing chemical consumption and hazardous waste by 95%
- Testing and evaluation of the use of textured coatings to improve cell efficiency
- Improvements in EFG cell efficiency by optimization of metallization firing conditions
- Initiation of work on an optimized cell grid design
- Production of test samples of cells designed for interconnection on the rear side only
- Demonstration of average efficiencies over 14.0% on more than 5000 EFG cells during one two-week period

Task 3: Modules

- Testing of new encapsulants promising reduced lamination time and improved yield
- Initial design work completed on new module frames that are both less expensive and faster to attach to modules
- Completion of initial testing and design work for lower-cost module diode housing
- Concept developed for improved collection of light from area between cells in modules

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1.0 INTRODUCTION

The goal of the PVMaT program at ASE Americas is to reduce the manufacturing cost of modules based on cells made from wafers produced by the Edge-defined Film-fed Growth (EFG) method. Since these modules contain EFG cells, and those cells are made from EFG wafers, this program entails work throughout the three production areas of ASE Americas: Wafers, Cells, and Modules. Because the sequence of production is in that order - wafers are made into cells, and cells are then encapsulated into modules - that is the sequence in which the work will be presented in this report. However, because the goal is a reduction in module cost, it is perhaps easier to understand the overall plan of this program by examining it in the reverse sequence.

Making modules out of cells is the most expensive part of the manufacturing process, accounting for almost one-half of the cost of the finished product. A number of factors contribute to this expense. The first is the cost of module materials. The single largest materials expense in the finished module is the cost of the encapsulating glass, used on both the front and rear of ASE modules.

The second highest single materials cost in the module production area is for the frame, which at ASE is currently made by the extrusion process. This manufacturing process produces a very robust frame, but it is expensive, and, because the material must be cut to length, it must be assembled from four sections, requiring a considerable amount of labor. A less expensive method exists for making commercial window frames, called roll-forming, in which sheet metal is formed into the shape of a frame. Because working sheet metal is less expensive than melting and extruding metal, this method has a cost advantage, once the cost of customized tooling is amortized. At the past production levels of ASE Americas, those tooling costs would have been prohibitive, but production levels are now high enough to amortize the tooling investment in a reasonable time period, and reap a significant savings in the cost of framing materials. A further advantage to the method is that it is widely used in industry, and methods exist for the rapid assembly of the frames onto glass, promising reductions in labor cost.

The third highest single materials cost in the module manufacturing area at ASE is for the housing containing the protective diodes. A large part of this expense has been for a finned aluminum heat radiator, which ensures that the diodes always remain at safe temperatures. Recent work at ASE has led to the development of diode circuitry that produces less heat, and therefore does not require an aluminum radiator. This will lead to significant savings not only due to the elimination of the radiator, but also due to the elimination of the need for electrical isolation of the radiator from the internal circuitry.

The second most important component to modules cost, after materials, is assembly cost. The largest component of that is the cost of connecting individual cells to each other to create 'strings', currently performed by soldering the cells to flat copper ribbons, called 'tabs'. This is a process made difficult by the fact that the tabs must connect the front of one cell with the rear of the next, requiring a sort of weaving motion, and preventing the simultaneous connection of multiple cells. The current program is attempting to overcome this difficulty by permitting all interconnection to be performed from the rear side of the cells - a very ambitious undertaking,

and one which has not yet proven successful. The final major cost in module assembly is the vacuum lamination process, which is relatively slow for the high reliability encapsulant used at ASE Americas. The PVMaT program includes work on reducing lamination time by changing the process or the encapsulant itself. Consideration is being given to the use of lamination methods with much lower capital equipment costs than for the vacuum process.

Working backwards in the production sequence to the cell manufacturing area, it is apparent that the goals set for reducing module assembly cost require a different type of cell, one with all of the contacts on one side. This requires changes in the cell metallization pattern, and the development of printing equipment that can connect one side of the cell to the other, which is not achievable with standard commercial equipment. At the same time, the front metal grid is being redesigned to improve cell efficiency by reducing both shadowing and series resistance by reducing finger width and increasing the number of fingers. While this approach is widely known, the methods for accomplishing it are not simple, and require, among other things, changes in the silver paste used for printing the grid lines. It should be pointed out here that the relationship between cell efficiency and module cost is a direct one: more efficient cells produce more power (watts), and module price is based not on dollars per module, but on dollars per watt. If the cells in a module can be made to produce more watts, then the cost of glass, framing, etc. *per watt* also decreases, providing a great incentive for efficiency improvements. Accordingly, efforts are also being expended on the optimization of every step in the cell manufacturing process, to ensure maximum cell efficiency. The short term goal at ASE Americas is to raise average cell efficiency over the threshold of 14.0% (already achieved on large numbers of cells) , with the goal for the end of the program at 15.5%. In addition, reduced cost of production clearly affects cell cost and, eventually, module cost. One particular opportunity for such a cost reduction is in a radical departure from conventional processing for the removal of the phosphorus glass after wafer diffusion, which is being carried out as part of this PVMaT program.

Working backward one last time to the Wafer Fabrication area, it should be clear that cost savings can be achieved both by reducing the cost of the wafers themselves, and also by improving their electronic quality, which leads to higher cell efficiencies. One part of the program which addresses both aspects is the reduction of wafer thickness, which not only requires a smaller quantity of silicon, but also contributes to an increase in cell efficiency. A second part of the program is directly related - laser cutting of EFG growth tubes into wafers currently is a low yield operation on thin EFG tubes, and so improved lasers are necessary to the success of the thin wafer program. The remaining area of work in wafer fabrication is the improvement of wafer electronic quality, which requires both optimization of the growth process and stringent measures taken to prevent contamination of EFG tubes during growth. The latter effort encompasses preventing contamination both inside the growth furnace, from the materials from which the furnace is constructed, and preventing contamination from outside, by isolating the tube from the outside ambient air.

The program goal is to reduce module cost by 25%.

2.0 ASE TECHNOLOGY PRIOR TO THIS PROGRAM

In this section, we describe the processes used at the various manufacturing steps which result in the production of an ASE module. A few of these processes have been improved during the course of this PVMaT program, and so are no longer practiced as they were prior to the program. All such changes in the manufacturing process are described in section 3 of this report. The present section is somewhat detailed, in order to provide information important to the understanding of the following sections, and will be useful as a reference when reading those sections. An outline of the overall process is presented in Table 1. Items in that table which are presented in boldface represent process steps which are being re-engineered as part of the PVMaT program.

The technology used for manufacturing modules at ASE Americas is based on the unique EFG method for growing silicon in a closed hollow shape, which, in its current form, produces the equivalent of eight ribbons simultaneously, in the form of an octagonal tube. This tube, known as an 'octagon', has a wall thickness of 300 μm, and is grown to a length of approximately five meters. When that length is reached, the tube is detached from the die and removed from the furnace. A new seed is then lowered onto the die tip, and growth is resumed. This procedure is repeated many times, until the die deteriorates and no longer produces flat tubes, or some other furnace component fails. The tubes produced during this time are called a 'growth run'. After the run is ended, the furnace is cooled, and the section of the furnace containing consumable parts (the 'setup') is removed and replaced. The setup is then disassembled and rebuilt offline, and restocked into inventory for future use.

The growth furnaces are highly automated, so that several furnaces can be operated simultaneously by one operator. One of the features of the equipment that makes this possible is an automatic feedstock replenishment system, which monitors the weight of the growing tube and replenishes the melt with an amount of feedstock equal to the amount removed in the form of an octagon tube. In order for this equipment to operate properly, all feedstock must be within a certain range of particle sizes. This requires sorting the feedstock through a series of sieves, which is a manual operation (using an electrically powered shaker).

The EFG growth furnace itself is largely constructed of graphite, which is one of the few materials which can tolerate the high temperatures (1420°C) and which in its pure state does not contaminate silicon with harmful impurities. However, the commercial grades of graphite available for furnace construction do contain harmful impurities, and these must be removed by careful processing of all furnace parts before assembly into a growth furnace. The levels of impurities in EFG wafers are very dependent on the effectiveness of the graphite purification process.

During growth of the EFG tube, the hot portions of the tube are surrounded by an atmosphere of argon, to prevent oxidation of both the silicon and the graphite furnace parts. Added to this atmosphere was a very small amount of carbon monoxide (CO), which has at times been shown to improve the electronic quality of EFG wafers. The reason for this improvement has not been determined; it may be related to interaction between oxygen and carbon defects in the silicon, the

Table 1
ASE PV Module Manufacturing Process
(Boldface indicates steps being improved as part of this subcontract)

Sorting of silicon feedstock

Growth of EFG octagon tubes

Laser cutting of tubes into wafers

Silicon wafer etch

Phosphorus diffusion

Phosphorus glass removal

Hydrogen passivation

Anti-reflection coating

Metal printing (rear and front) and firing

Cell testing

Cell interconnection into strings

Module lay-up

Lamination

Module testing

Framing

Attachment of junction box and external wiring

Safety testing

pinning of dislocations, or the gettering of metallic impurities. The use of CO had serious consequences for the crystal growth process in high-volume manufacturing, however. CO reacts with silicon to form silicon monoxide (SiO), which is volatile at the temperatures required for crystal growth. SiO condenses at temperatures below 1100°C, and this condensation formed fibrous deposits on the cooler zones of the furnace. When these deposits reached a critical thickness, further operation of the furnace was no longer possible.

After an octagon tube is removed from a growth furnace, it is transported to another work station where a Neodymium-doped Yttrium Aluminum Garnet (Nd-YAG) laser cuts each face into square wafers, 100 mm in length and width. A fundamental problem with this process is that the rapid heating with each pulse of the laser generates microcracks along the wafer edges. Because silicon is a brittle material, those cracks have a tendency to propagate, causing the wafer to break during later processing.

After laser cutting, the wafers are etched. The etching process is followed by phosphorus diffusion, to create the junction which is the basis for operation of the solar cell. At ASE, this process is a continuous operation, as opposed to the batch operations used by other PV companies. Following the diffusion step is a second wet chemical process, in which the phosphorus glass that forms on the wafer during diffusion is removed. This is both a batch process, poorly matched to the preceeding continuous process in terms of material handling, and one which consumes a significant quantity of chemicals. More important than the purchase cost of those chemicals is the cost of further processing they must ultimately undergo to render them harmless before discharge.

The two processing steps following glass etch, hydrogen passivation and anti-reflection (AR) coating, employ proprietary technology and are rather highly developed, requiring only minor process optimization work to achieve their full potential as currently practiced.

After the anti-reflection coating is deposited, silver contact pads and an aluminum back surface field coating are applied to the rear of the cell, and the silver grid pattern is printed on the front. The grid consists of 32 fingers, each approximately 100 μm wide, and two busbars which collect current from the fingers and which are later bonded to tabs connecting the cell to others in a string. This grid is known not to be optimized. Fingers 60 μm wide have been obtained in development tests, and shadowing losses would be reduced significantly if it were possible to produce them on the manufacturing line, but that technology does not yet exist. An optimized grid using such narrow fingers would also contain more of them, on the order of 40. This would reduce series resistance losses in the cell, providing a further gain in efficiency.

After printing of the contact patterns on both sides of the cell, it is fired, bonding both contact layers simultaneously, and completing the cell. Following firing, each cell is tested individually, and binned according to current at peak power.

The cell interconnection process involves the attachment of solder-coated copper tabs by soldering them simultaneously to the front and back of one cell, followed by the feeding out of another length of tabbing and repetition of the process. Although basically efficient, the sequential nature of the process, combined with the time requirements for properly heating and cooling the solder bonds, place an upper bound on the production rate which is lower than desired for high-speed manufacturing. In current ASE technology, the interconnected cells, known as 'strings', are then manually laid-up on a sheet of glass with layers of encapsulant and power bus strips, producing the precursor to the final module. This assemblage is placed in a vacuum laminator, and subjected to a relatively long process during which air is removed and the encapsulant melted and reflowed to fill all internal spaces. After removal from the laminator, the 'laminate' is tested to ensure that its output power is within specifications.

The laminate becomes a module by being outfitted with an aluminum frame, a junction box or diode housing, and electrical cables for connection to other modules. The frame used at ASE is made of precisely extruded aluminum. Framing is labor intensive and not readily amenable to automation. The diode housing used on most ASE modules is then manually attached to the laminate using an adhesive. The diode housing is a custom-formed part which encloses the

protective diodes and dissipates heat generated during their operation (which normally occurs only if the module is exposed to uneven illumination - an unusual occurrence). The final step in module assembly is the electrical connection of the laminate to the diode or junction box circuitry, and the attachment of the cables used to connect the modules to one another. This step is followed by another power rating test, which determines the module's nameplate rating, and, finally, by a high voltage current leakage test.

3.0 PVMaT PROGRAM EFFORTS

In the following sections are detailed the efforts being pursued in pursuit of cost reduction of ASE modules, and the results of those efforts at the end of the first year of the program. The following few paragraphs provide an overview of the work being carried out on each of the process steps identified in Table 1 as being improved as part of the PVMaT effort.

Sorting of silicon feedstock

The sorting operation is being converted from a manual operation to an automated process, providing significant savings in labor, an improved level of safety, and a reduction of the potential for contaminating the feedstock.

Growth of EFG octagon tubes

Improvements in the graphite purification process have resulted in an improvement in the electronic quality of EFG wafers. Engineering work has been completed on a design for an enclosure to prevent leaks of outside air into EFG growth furnaces which can contaminate growing tubes and shorten the lifetime of furnace components. The enclosure will also prevent air currents from disturbing the tubes, which will result in flatter wafers. Process variable optimization studies have identified the optimal growth speed, which achieves a balance between requirements for high material quality and high production rates. A program of impurity analysis has developed the capability for relatively rapid determination of sources of wafer contamination. Investigation into the effects of carbon monoxide added during crystal growth have shown little improvement in wafer quality in the current system, contrary to previous findings. As a result of this finding, carbon monoxide additions have been terminated, resulting in large increases in growth run length.

Laser cutting of tubes into wafers

A new, low-cost, low-maintenance carbon dioxide laser was tested as a replacement for the Nd:YAG lasers currently in use. The initial tests showed promise, but indicated that cutting conditions are not optimal. Testing has also been performed using a copper vapor laser. However, satisfactory cutting rates were not achieved with this laser. Further testing of other carbon dioxide and copper vapor lasers is planned.

Phosphorus glass removal

A new approach to the removal of the phosphorus glass layer remaining after diffusion has been engineered and proven in laboratory demonstrations. The new process reduces chemical, waste treatment, deionized water, and labor costs, and streamlines material handling. A prototype unit to demonstrate this process on the manufacturing floor is currently being designed. A full-scale unit hardened for continuous service in the manufacturing environment is expected to be put into service in early 1998.

Anti-reflection coating

Development work is being carried out to introduce an additional process following the current AR coating process step to deposit a second coating for the purpose of reducing reflection. Unlike the coatings used in the industry today, this second coating would be relatively thick and textured to produce a matte surface. This coating would provide the benefits of texturing which in the past could only be produced on single crystal silicon surfaces. Previous work at Sandia National Laboratories has demonstrated efficiency improvements of as much as 0.5% absolute using this technique.

Metal printing and firing

Firing conditions for the current metallization pattern have been optimized, resulting in a gain in cell efficiency to over 14%. Work is continuing on reducing finger width and increasing the number of fingers to realize another significant efficiency gain. Metal printing methods are under development to permit the contacting of the front grid from the rear of the cell, simplifying cell interconnection.

Cell interconnection into strings

Simplified methods are being developed for interconnection, based on the new cell design with all contacts on one side.

Module lay-up

One of the interconnection schemes under development would result in **a reduction of the time required for module lay-up.**

Lamination

Efforts are being made to reduce lamination time by changing process conditions and/or encapsulant materials. A reduction of lamination time by 50% has already been demonstrated using current vacuum lamination equipment. Non-vacuum processes are also being investigated to replace this step with a very different process, using much less expensive equipment.

Framing

A low-cost frame is being developed to replace the expensive extruded aluminum frame currently in use. The new frame will also use lower-cost gasketing, and will have a reduced assembly time.

Attachment of junction box and external wiring

A new diode housing is being designed which will reduce the cost of this component by a factor of two.

3.1 TASK 1 - IMPROVEMENTS IN EFG WAFER PRODUCTION

3.1.1 Automated Sorting of Silicon Feedstock

A completed EFG octagon tube is over 200 mm wide and 4.6 m in length, and contains nearly 3 kg of silicon. Growing such a tube by the EFG method relies on the wetting of the tip of a shaped die by molten silicon, which requires that the melt level must remain constant. The way this is accomplished is by constant replenishment of the melt throughout the process of growing an EFG tube. The mass of the tube is measured at frequent intervals, and when a certain mass gain has been measured, an equal mass of granulated silicon is weighed out and delivered into the growth furnace through flexible tubing.

The feedstock material purchased by ASE for this process has variable geometry. Particles which are at the very low end of the distribution cause dust inside the growth furnace, which can interfere with the growth process. At the other extreme, very large particles tend to jam the feed tubes carrying the material to the furnace, eventually causing tube growth to cease. Because of these problems, all feedstock material is sorted to separate out particles in these size ranges.

At present, this sorting is performed by manual sieving, which is a labor intensive operation that is both tedious and costly. ASE is working to automate the particle sorting and redistribution process as part of the PVMaT program. It is anticipated that the automated process will provide the additional benefit of minimizing the amount of material rejected in sieving, resulting in a reduction in total silicon cost. Consultants have been retained to design a system to carry out the new automated process. A variety of designs were investigated, eventually resulting in the locating of equipment suitable for the task, as determined using actual ASE feedstock material. Current plans call for further testing of the equipment, and, assuming success in these tests, purchase and installation for production use during the coming year.

3.1.2 Improvements in the Growth of EFG Octagon Tubes

Improvements in graphite purity

Extensive testing of several grades of graphite from several vendors, and several graphite purification processes, were conducted during Phase I of this program. This testing consisted of both spectroscopic measurement of impurity levels in the various grades, and the fabrication of the purest of these grades into furnace components for correlation of cell efficiency with material type. As a result of these studies, several graphite grades and at least two purification methods have been qualified for production use.

Most importantly, the standard purification process for ASE materials has been improved. This has greatly reduced the variability of purification level from one lot of furnace parts to the next. As a result, although efficiency shortfalls due to contaminated graphite were frequent in the past, few such instances of contamination occurred during 1996. Quality improvements are monitored by a program of routine Deep Level Transient Spectroscopy (DLTS) impurity level measurements on wafers, which was established as part of this PVMaT program.

Growth rate experiments

The growth rate of EFG tubes affects wafer cost in a number of ways. Clearly, running the growth furnaces at their maximum rate will minimize capital and labor costs in the growth area. However, wafers that are cut from tubes which are grown too rapidly tend both to be buckled, leading to breakage during later processing, and to contain higher levels of electronic defects, reducing cell efficiency. In addition, these buckled tubes have reduced yield in the laser cutting operation.

During Phase I of this program, experiments were conducted to find a combination of the optimum growth rate and yields for EFG tubes to maximize throughput. As a result of those experiments and analysis of the results, growth speed was reduced. The result has been improved yield in both crystal growth and laser cutting operations, justifying the effort.

Furnace ambient experiments

Past experiments aimed at improving the electronic quality of EFG wafers have indicated that the introduction of oxygen in low concentrations into the ambient of the growing crystal provides such an improvement. In production at ASE, this has been accomplished by the addition of small amounts of carbon monoxide (CO) into the argon purge gas surrounding the growing tube. An unfortunate byproduct of this practice is the production of silicon monoxide (SiO), which condenses in feathery deposits which eventually interfere with various components in the furnace, resulting in the termination of the growth run. Since the rate of growth of these deposits depends on CO concentration, a study was conducted as part of Phase I of this program to locate the optimum CO concentration to trade off efficiency versus production cost.

Although tests were conducted at various times during the year, remarkably, the improvements seen earlier for CO additions were not observed to a degree that could be validated by statistical analysis. This result is puzzling, since tests in earlier years have shown consistent improvements on the order of 0.5% absolute from the use of CO additions. The result may be related to the improved graphite purity described in a previous paragraph. One of the explanations for the effectiveness of CO in raising cell efficiency is that it reacts with metallic impurities during crystal growth, resulting in the formation of a metal-containing oxide coating on the growing tube, which is later removed when wafers are etched. Since the graphite components in the furnace are the primary source of metallic impurities during crystal growth, the new graphite purification processes used during the preparation of EFG furnace parts may have obviated the need for the use of CO. Another possibility is that the grade of silicon currently in use contains more oxygen than grades used in the past, so that further additions provide no benefit.

As a result of these findings, the use of CO in normal crystal growth production at ASE Americas has been reduced, and this has resulted in nearly a doubling of the length of the average production growth run. This benefit has lowered costs and raised production throughput. Experiments are being continued to attempt to determine if some combination of CO additions and changes in cell processing conditions would result in improved cell quality. If successful, these experiments may lead to further improvements in EFG cell efficiency.

Engineering of an enclosure for EFG furnaces

Wafer quality is affected not only by the purity of materials intentionally placed inside the furnace, but also by impurities that infiltrate into the furnace in the form of contaminants from the ambient air. Analysis of affected cells has shown the offending impurity introduced in this manner most often to be titanium. Exposure of EFG tubes to the environment can cause other problems as well: tube buckling and contamination of the growth furnace atmosphere with air. Clearly, protection of the furnace and growing tube from the environment would improve the quality and consistency of EFG wafers.

During Phase I of this program, the design of an enclosure was completed. Fabrication of the component parts is now underway. Installation of a first enclosure for test purposes will occur in Phase II (1997).

Growth of thin (275 μm) EFG tubes

The current standard thickness of EFG wafers is 300 μm. A major goal of the current PVMaT effort is to reduce the average thickness of EFG tubes to 250 μm in order to reduce silicon cost. At the same time, this effort will improve EFG cell efficiency, because the back-surface field reflector used on ASE's cells is more effective on thin wafers for a given bulk quality. This was demonstrated by sampling EFG cells produced at various times during the year. In every case, an inverse relationship was observed between cell thickness and efficiency. A typical efficiency difference corresponding to a cell thickness difference of 50 μm was about 0.3-0.4% absolute. (See Figure 1.)

Experiments were conducted in the crystal growth area to determine the feasibility of growing tubes at these lower thicknesses. In the first experiment, thickness was reduced to 275 μm. No growth problems were experienced at this thickness level, and laser cutting yields were normal. In the next level of experiments, thickness was further reduced to 250 μm. Tube growth was more difficult in this case because of thickness nonuniformities. More problematic, however, was the difficulty of laser cutting the thin material. Cutting yields were unacceptably low for production purposes. The conclusion drawn from this work is that it will not be possible to introduce 250 μm EFG tubes into production until improvements are made in the laser cutting process.

3.1.3 Research into Improved Laser Cutting of Tubes into Wafers

The current process of cutting EFG octagon tubes into wafers using Nd:YAG lasers introduces microcracks into the edge of the wafers as a result of the rapid heating of the silicon by the laser beam. Through repeated flexing during cell production, those cracks propagate and can eventually lead to cell breakage. In addition, as described in the preceeding paragraph, this problem becomes particularly severe with thin silicon, which is needed to achieve the cell efficiencies targeted for this program.

Two new types of lasers were tested as replacements for the YAG lasers, one a carbon dioxide

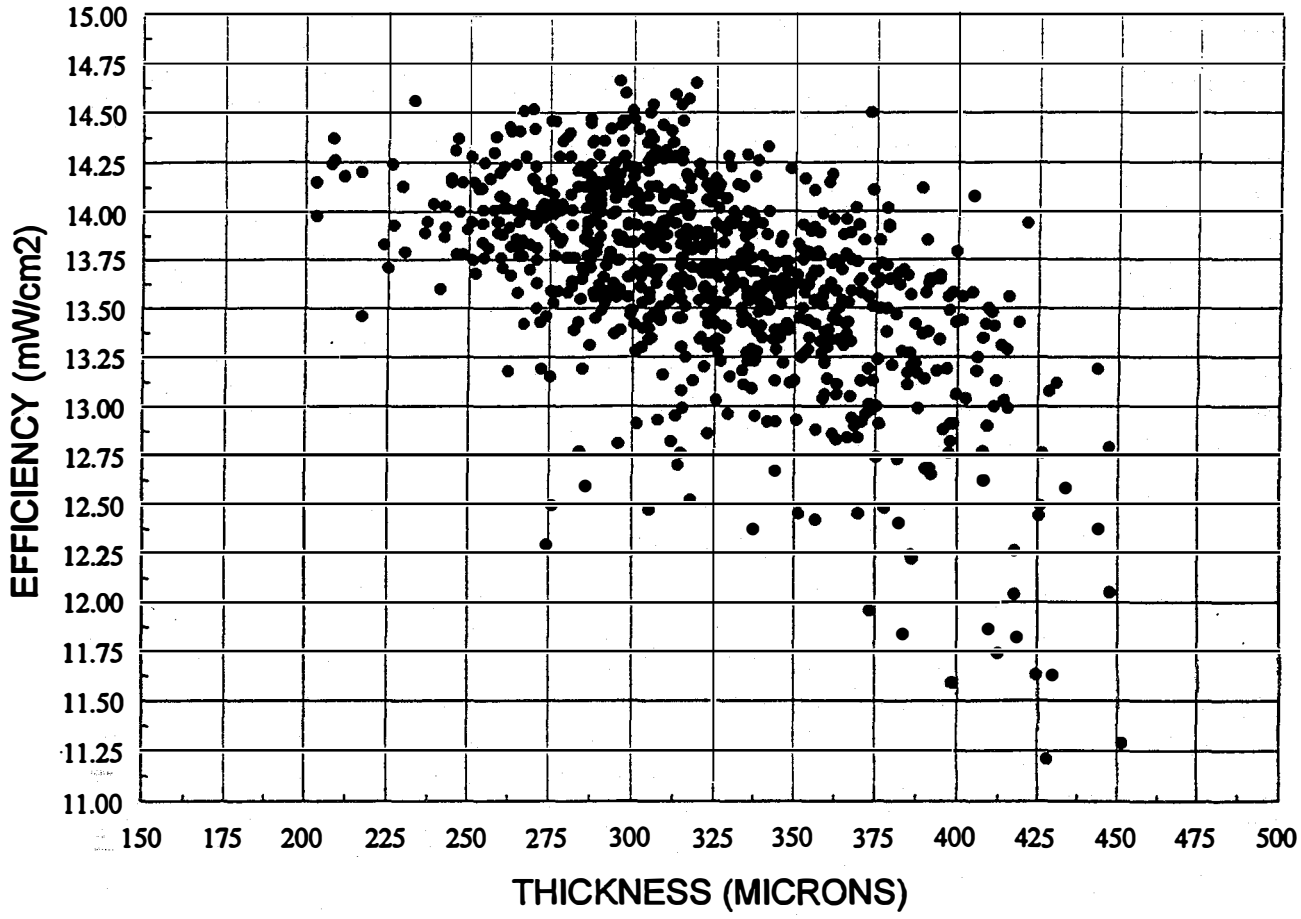

Figure 1. EFG cell efficiency as a function of wafer thickness. A decrease in thickness of 50 μm is predicted to raise efficiency by 0.3 - 0.4% absolute.

(CO_2) laser and the other a copper vapor laser. The CO_2 laser was chosen for evaluation based on the simplicity and robustness of its design and on the results of test cuts performed at the laser manufacturer's facility. The quality of those test cuts clearly exceeded normal cut quality achieved on the ASE production line. Accordingly, a laser was obtained for testing at the ASE facility, and used to cut EFG tubes. The result was that, although the cut quality was excellent on the side at which the beam entered the silicon, debris was present at the exit side of the cut. This debris both caused the cut edge to be rough and appeared to be the source of microcracks that were initiated where particles of molten material solidified. The conclusion drawn from these tests was that the laser holds promise, but cutting conditions are not optimal. An effort is continuing to study parameters which affect cut quality.

The second type of laser tested, of the copper vapor type, was of interest because it emits radiation at a wavelength which is strongly absorbed very near the surface of silicon. In this situation, ablation of the surface can occur with very little transfer of heat to the bulk, avoiding the formation of cracks. Unfortunately, this type of laser is expensive in models possessing the high power levels normally needed to cut silicon quickly. The key to the experiment was,

therefore, to try to achieve adequate cutting with a low power version of the laser, using a novel set of focussing optics. This work was carried out by consultants with extensive experience in laser optics. The result was unexpected. The new optics did permit the laser to cut through a silicon wafer, but because the cut was so narrow, it became partially filled in by silicon redeposited from the vapor phase . Thus the edges produced by circular test cuts on the wafer could not be separated, although the beam had clearly penetrated both sides. Although this was not a successful result, it indicates that further work is warranted to determine which factors affect silicon redeposition in the cut and how it may be eliminated. ASE will continue to work on improving the cutting process during Phase II of this project.

3.2 TASK 2 - IMPROVEMENTS IN EFG CELL PRODUCTION

3.2.1 Evaluation of Textured Anti-reflection Coatings

One of the disadvantages that multicrystalline silicon materials such as EFG face when compared with monocrystalline silicon as a substrate for photovoltaic cells is the inability to texture the surface by the same chemical means. Texturing on monocrystalline silicon is performed by means of an acid etch which attacks the various crystallographic planes at different rates, and it can be used to form a matte black finish. The very low reflectance of this surface improves light collection and improves solar cell performace very significantly. The same technique cannot be used successfully on multicrystalline wafers because the same process polishes some crystal grains while texturing others. This results in a nonuniform surface which provides very little gain, if any at all.

Recently, a method has been demonstrated which can provide multicrystalline cells with the advantage of a textured surface by adding transparent material to the cell surface, rather than subtracting silicon. This work, conducted at Sandia National Laboratories, was performed on cells coated with textured layers of zinc oxide (ZnO) in the laboratory of Professor Roy Gordon at Harvard University. In this study, the investigators demonstrated improvements of as much as 0.5% absolute resulting from the use of the textured ZnO coating.

The incorporation of such coatings into the design of EFG cells was therefore one of the major goals of ASE's PVMaT program. Completed cells were fabricated, tested, and shipped to Harvard University for coating, and then retested after the coated cells were returned. A few trials were conducted before optimal deposition conditions were obtained; the cells coated during this period were gray in appearance. The later cells processed after the coating process was optimized were matte black in appearance, as predicted. These cells were retested at ASE both in the open air and under a coating of a thin film of isopropanol, to simulate the refractive index match that would occur when the cell was encapsulated. Finally, a few of these cells were encapsulated, using ASE's standard encapsulation process and materials.

Unfortunately, none of the cells demonstrated an efficiency gain large enough to exceed the range of error associated with the cell tester. This was true despite the fact that both the black cells and many of the gray ones appeared to have very low reflectance levels when encapsulated or tested under isopropanol. The cause for the lack of improvement has not yet been identified.

Several possibilities exist. One is that some of the improvement seen in the work at Sandia was due to the coating of a high index material with a slightly lower one. If so, the improvement due to texturing alone on an EFG cell may not be very large, and may be difficult to measure. Another possibility is that the particular texture deposited on these cells was not optimized, and may reduce reflectance in one part of the spectrum, but not in another. Finally, it is possible that the improvement provided by reduction in reflection loss was negated by a loss due to optical absorption in the relatively thick layer. The latter possibility is a strong one, given the fact that the absorption of ZnO films tends to be high when deposited at the relatively low temperatures required to avoid damage to EFG cells after metallization.

Samples of the cells produced in this study have been sent to Harvard and Sandia for analysis of the cause of the lack of improvement. Planned tests include measurement of reflectance and transmittance of the ZnO films, examination of film texture by scanning electron microscopy, and modelling of the reflectance levels expected for the observed texture. It is expected that the results of these studies will provide a direction for further work on this task.

3.2.2 The Development of a New Process for Phosphorus Glass Removal

As is typical for any diffusion process on silicon wafers, the diffusion process at ASE Americas leaves the wafer surface coated with a silicate/phosphate glass, which must be removed prior to any further processing. At ASE, this is accomplished by wet chemical etching of the wafers, which are held in carriers in an acid bath. The need for the use of carriers presents a handling difficulty, since neither preceeding nor following process steps require the use of carriers. In addition, although little acid is consumed by chemical reaction during the process, the bath must be replaced periodically. The disposal of the spent acid is costly, since it requires treatment before it can be discharged, and removal of the fluoride that it contains is expensive.

ASE has been seeking an alternative to this process, which could be carried out on wafers as they are transported by belt from one processing area to another, eliminating the need for carriers and a great deal of manual handling. The task of studying the feasibility of designing such a process and developing equipment to carry it out was subcontracted to Bright Technology, Inc. During Phase I, that firm demonstrated the effectiveness of their method by processing a number of EFG wafers coated with phosphorus glass, and those wafers were then subjected to the remaining cell processing steps. Except for minor imperfections inherent in the manual handling methods used in the tests, the resulting cells were normal in appearance, with no evidence of residual glass.

The process developed by Bright Technology reduces chemical consumption at this step by 95-98%. The equipment required to carry out the process can also be highly automated, and may be less expensive than the equipment currently used for the standard process. Bright Technology completed the feasibility study slightly ahead of schedule, and is now in the process of designing a prototype unit to be used to demonstrate the process on ASE's manufacturing floor. If that demonstration is successful, construction of a production etch unit will be started before the end of Phase II.

3.2.3 Optimization of Metal Printing and Firing

Optimization of the Front Grid

The width of the silver fingers used in the front grid pattern on the cells currently manufactured at ASE Americas is approximately 100 μm; the narrowest fingers achieved in developmental engineering work at ASE is approximately 60 μm. If those narrower fingers could be produced consistently on the manufacturing line, the resultant reduction in shadowing would increase cell efficiency by about 0.2% absolute. If, in addition, the number of fingers in the grid pattern were increased from 32 to 40 or more, the reduced spacing between the fingers would reduce series resistance losses in the cell emitter, raising efficiency by an additional 0.1-0.2%. Achieving these efficiency increases is part of the PVMaT program.

The difficulty in achieving this objective lies mainly in the flow properties of commercially available thick film silver pastes designed for use on PV cells. The number of commercial pastes compatible with the printing technology at ASE Americas is limited, and all of those pastes were designed for rapid and trouble-free screen printing. These pastes have a tendency to spread after printing, increasing linewidth. In order to achieve narrower lines, modifications must be made in the formulation of the silver paste. The modifications provided to ASE by commercial vendors to date have not been consistent enough to use in manufacturing, although they have sometimes produced good results in developmental work.

Current work at ASE is now focussed on modifying the pastes. Test printing work was initially delayed by mechanical problems with the test printing equipment. Since that equipment was repaired, several test runs have been made using silver pastes containing various flow-modifying additives. Experience in blending of the pastes is being acquired, and some encouraging results have been obtained. However, the results obtained so far are not good enough to justify testing on expensive production-scale equipment. Testing is continuing, and is expected to produce useful results by the midpoint of Phase II of this program. Equipment changes will then be carried out to permit the use of the new material on the production line, near the end of Phase II.

Optimization of metal firing conditions

The firing of the thick-film metallization on ASE's cells affects both the emitter contact and the back surface field. If the emitter contact is either underfired or overfired contact resistance is high, and overfiring will in addition cause leakage currents to increase. Meanwhile, underfiring of the back aluminum contact does not permit the formation of an effective back surface field, and improper cooling after firing produces a defective layer that contributes little to cell efficiency.

An extensive series of experiments was carried out as part of Phase I of this program to adjust firing conditions to achieve the best possible firing conditions for both contacts. Process variables were varied over a wide range of conditions. The test results were used to make incremental changes of firing conditions on the manufacturing line, which resulted in improved cell efficiencies (see Figure 2). At the beginning of this task, cells exceeding 14% in efficiency

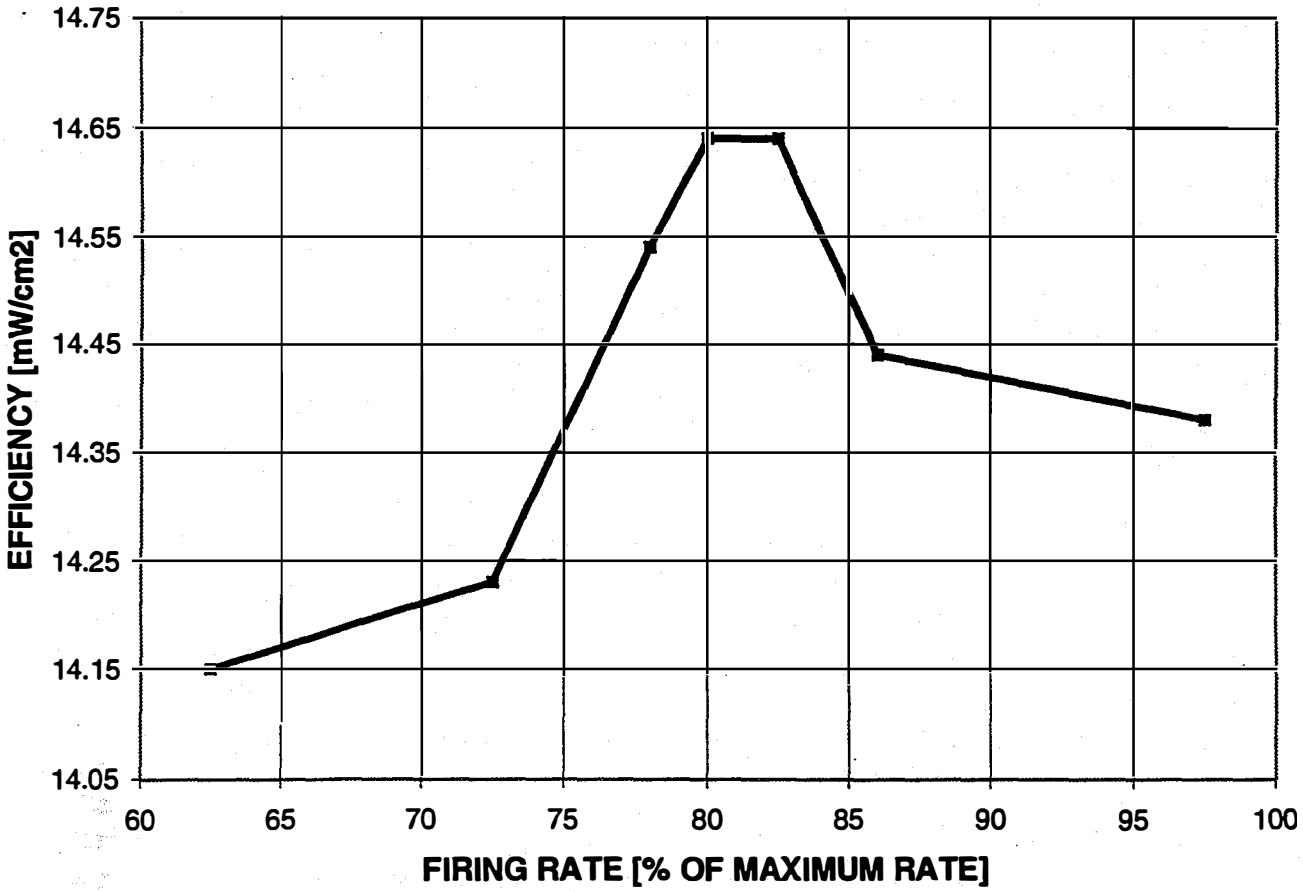

Figure 2. EFG cell efficiency as a function of the rate of firing of the cell metallization pattern. Optimization of this process has reduced contact resistance and improved the back surface field.

were relatively rare, but by its end they became a large fraction of the total number produced. Total efficiency improvements attributable to this optimization program are estimated to be approximately 0.3-0.4%.

Design of cells for single-side interconnection

One of the objectives of this PVMaT program is to reduce the cost and complexity of the cell interconnection process. One of the factors making this process difficult is the need to interconnect conventional cells by wiring the front of one cell to the rear of the next. If both the emitter and base contacts were accessible from one side, the interconnection process could be greatly simplified.

Several approaches for achieving this objective were tested during Phase I of this program. One involved the attachment of a metal strip to the edge of a cell. This strip was then bonded to the emitter grid of that cell, forming a unit which could be 'shingled' with the next cell in the string. The total concept for this design called for robotic placement of one cell on a layer of encapsulant and the dispensing of a conductive adhesive on the metal strip, followed by

repetition of this procedure with the next cell, and the next. Curing of the adhesive would occur during lamination, providing the necessary electrical connections. This approach was set aside when electrical resistance losses in test samples were found to be unacceptably high.

A second approach called for the use of a cylindical wire as a replacement for busbars on the emitter grid, which would reduce both resistance and shadowing losses. The wire would be bent into a "U" shape overlapping the cell edge. The interconnection process would consist of wrapping a conductive tape around the protruding wire, and fastening it to the rear of the following cell. Appropriate materials for this process were located, and mock-ups of strings created, which were attractive. Difficulties were encountered in attaching the wires to the front grid, however, and relatively high resistance losses were discovered at the connection between the tape and the wire. Work continued on this concept, however, until it was discovered that a European patent was issued on a very similar design (German Patent DE 4435219 C1, assigned to Siemens Solar). Its impact on future work will be studied before we proceed further.

Currently, work continues on a simpler approach of wrapping the cell busbar from the front of the cell to its rear, which would permit a rapid interconnection of cells using a soldering process. ASE has already developed the technology to wrap the contact around the cell edge. The present challenge is that the design requires changes in the busbar geometry in order not to incur fill factor losses due to increased series resistance. The new busbar will need to be shaped in a manner that will challenge ASE's current printing technology. A method for producing such busbars is under development, and test cells are expected to be produced soon. After that hurdle is overcome, further work will be required to develop a production method for the interconnection process itself.

3.3 TASK 3 - IMPROVEMENTS IN ASE MODULE PRODUCTION

3.3.1 The Development of New Methods for the Interconnection of Cells into Strings

The objective of this task is to develop a cell interconnection method that is inherently simpler than the conventional method of connecting the front of one cell to the rear of another by soldering to copper tabs. A number of methods were studied, with a goal of developing a process similar to that used industrially to surface mount components on printed circuit boards. The task is made challenging by the need to contact both sides of the cells, the fact that the cells are both large and fragile, and the inability of encapsulant material to withstand the temperatures required for soldering.

The most direct approach to this task is to develop a method for providing contact points connected to the emitter on the rear of the cell, and assembling the cell array on a layer of encapsulant on which connector strips have been placed, so that the assemblage is very similar to a printed circuit board. The cells would be attached to the connectors by means of either solder or electrically conductive adhesive. If an adhesive is used, the lamination procedure can be used to further strengthen the bond. However, since the encapsulant melts during lamination, a reasonably strong mechanical bond must be established prior to this melting, to ensure that the bond does not separate before good electrical contact is established.

This recipe contains room for a variety of approaches to this task. For example, the conductor strips may be pre-bonded to the encapsulant in the locations where cells are to be placed. The assembly process using this approach is very different from that required to apply copper tape to the rear side of the cells and to connect that tape to the emitter contacts on adjacent cells. A number of these approaches were tested, using a variety of specialized materials. The various approaches also required changes in cell design, as described in the previous section. Tests to date have not demonstrated a combination of cell design and interconnect method which would achieve the desired reduction in interconnection cost without reducing module efficiency. The next stage in testing requires modifications to the cell design, which are underway. Materials have been obtained for testing new approaches to interconnecting the new cells. Those tests will be underway during the first quarter of Phase II.

3.3.2 Simplification of Module Lay-up

This task is closely related to the previous one. It is presented separately here only because of the clear distinction in the present manufacturing line at ASE Americas between the interconnection and module lay-up production steps. The goal of the integrated interconnection part of the current PVMaT program is to reduce manufacturing steps and simplify assembly. If a method can be developed to interconnect cells by bonding them to a substrate, then their attachment to that substrate also will locate them in a module. This is in contrast to current technology, in which cells are connected into strings, and the lay-up of strings into their location in the module is a separate operation.

In the current manufacturing process, module lay-up includes not only locating the cells, but also the placement of layers of encapsulant, the module power busses, and the sheet of glass used as the rear of the ASE module. Those operations would still be necessary. However, total labor and time required for this process step would be reduced by 25-30%. The timetable for the achievement of these savings is obviously the same as for the interconnection task described in the previous section.

3.3.3 Increases in Lamination Throughput

One of the competitive features of the module manufactured by ASE Americas is the proprietary encapsulant used in its construction, which has been demonstrated to survive exposure to UV radiation with far less degradation than the standard EVA encapsulant used throughout the PV industry. A drawback exists in manufacturing modules using this material, however, in that it flows more slowly than EVA during the lamination process. One of the goals of this PVMaT program is to reduce lamination time by 25% or more, permitting an expansion in module manufacturing capacity at ASE Americas without the need to purchase additional lamination equipment.

One of the means under investigation to accomplish this objective is the replacement of at least part of the encapsulant with another material which has many properties, including UV resistance, that are similar to that of ASE's current encapsulant, but which also imparts properties not present in the base encapsulant. Samples of two different grades of such a material were obtained, and test coupons were laminated using each of these materials as encapsulants. It was found that it was possible to laminate one grade in a much shorter time than ASE's standard encapsulant, while the other grade could be laminated in a slightly shorter time. However, the former grade did not possess sufficient clarity to be useful as an encapsulant. This appeared to be due to the addition of a dusty anti-blocking agent to the sample by the manufacturer, to make the material easier to handle. There was no such additive obvious in the second sample, which was highly transparent.

Adhesion peel-strength tests were performed on both of the samples. The sample with the anti-block coating demonstrated very poor adhesion, even on primed glass. This was attributed to the additive, and because of the poor performance it was decided not to test that sample further. The other material formed a weak bond on unprimed glass, but bond strength was improved considerably by use of the primer. However, the bond was still more than 50% weaker than that obtained using the present encapsulant. Further testing will be required to determine if a better primer exists for use with this material. It was decided that environmental testing of the material would not be worthwhile at this stage of development because of probable further weakening of the bond by exposure to a high temperature, high humidity environment.

Concurrently with the work on new materials, experiments were carried out to determine whether changes in the heating and cooling cycles could be used to reduce lamination time using the current encapsulant. These experiments rather quickly resulted in successful laminations at process times more than 25% shorter than the standard process, achieving the goal of this effort.

The quality of the modules produced using this process appeared to be identical to that of modules made by the standard process. Modules produced by this method will be subjected to environmental testing to ensure that reliability is not compromised by the change in process. Further lamination tests are also scheduled, to provide a larger statistical base on which to evaluate lamination yield.

At present, the major effort on this task is being focussed on the lamination process change, because it does not introduce a new material which requires extensive testing. This will likely permit its relatively rapid introduction into manufacturing. Further testing on the new materials will continue also, but at a lower level of effort.

3.3.4 Reduction in Materials and Labor Costs of Module Framing

One of the major cost components of a PV module is its frame. These costs are related not only to the cost of materials, but also to labor costs involved in its attachment to the module. At ASE Americas, this assembly includes the attachment of gasketing material to the edge of the laminate, the locating of four sections of extruded aluminum over the gasket, the alignment of those sections, and their connection to one another using screws. This operation appeared to provide an opportunity for significant cost reduction.

The approach investigated during Phase I is a change in frame design from one made of extruded aluminum to one made of roll-formed aluminum. Roll forming is a process commonly used in the manufacture of commercial metal products, such as furniture, appliances, and window frames. It requires a relatively high investment in tooling, but, because it produces individual parts at a reduced cost compared to extrusion, that investment can be quickly recovered if part production volume is sufficiently high. In addition, roll-forming is commonly used for framing applications because of low assembly cost. Roll-formed frames are produced as a single piece, which is wrapped around the object being framed, and the two free ends attached at only one point. The question that needed to be answered was whether the savings produced by a change to this technology would be sufficient to pay for the costs of implementing it.

ASE Americas has been working with a consultant company experienced in roll-forming to answer this question. Several rounds of designs and modifications have been completed. The most promising design to emerge as of the end of Phase I provides a cross-section very similar to that of ASE's present frame, while total weight is reduced significantly. Because of the shape of the design, this is still expected to provide the required stiffness. However, if the frame's inherent stiffness proved to be insufficient, it could be redesigned to be stronger with only a slight increase in weight.

The consultant is now working on modifications to this design to answer concerns raised in the most recent design review at ASE Americas. Their engineers are also working on cost calculations to determine the economic advantage of a change to the new design. Expectations are that the new frame will cost 25% less than the current one, and will also provide at least a 50% reduction in assembly time. An evaluation will still need to be made at ASE, however, on

whether that level of cost savings will justify the costs of structural evaluation and testing.

3.3.5 Reduction in Cost of Diode Housing

The large 300 W module manufactured by ASE Americas is most commonly supplied with electrical quick connectors to provide connections between modules. Therefore, it does not require a junction box *per se*. However, it does require diode protection to minimize problems associated with hotspot heating due to uneven illumination. The protective diodes are mounted on a circuit board enclosed in a housing on the rear of the module. A large part of the housing cost arises because of the use of an extruded and machined aluminum cover on the housing, which provides a heat sink which dissipates the heat generated by the diodes during the rare instances when they are operating.

A reevaluation of this design was called for in response to new customer demands. This prompted a review of the diode circuit. An opportunity was discovered to change the circuitry so as to reduce the heat load. This circuitry was tested both indoors and outdoors and found to function as predicted, while meeting all requirements for certification. Due to the reduction in heat load, the requirements for heat dissipation using this circuit design were reduced as well. This permits the elimination of the aluminum radiator, to provide a substantial reduction in the cost of such a design.

As of the end of Phase I, a circuit card and preliminary housing design had been developed. A mockup of the housing is currently undergoing tests to evaluate its thermal performance. If it passes the tests, as expected, detailed samples will be produced by rapid prototyping for further evaluation tests. This will be followed by the generation of a mold for a production part. At this time, it is projected that the new housing design will be in use in ASE's production modules at the end of the second quarter of Phase II, at a savings of several U.S. dollars per module.

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This report summarizes the accomplishments during the reporting period. The "Task 1: Wafers" accomplishments include improvements in graphite purity in edge-defined film-fed growth (EFG) crystal-growth furnaces, improving wafer quality; optimization of EFG crystal growth rate; increased die run-length due to reductions in the use of carbon monoxide during EFG crystal growth; completion of engineering and design work for EFG growth-furnace enclosures; feasibility demonstrated for the reduction of EFG wafer thickness from 300 μm to 275 μm; design and testing of a system to reduce costs of silicon feedstock sorting prior to EFG crystal growth; and testing of new carbon dioxide and copper vapor lasers for improved cutting of EFG wafers from octagon tubes. The "Task 2: Cells" accomplishments include improvements in cell diffusion conditions resulting in increased cell efficiency; the completion of process design for a new approach to remove phosphorus glass from diffused wafers, reducing chemical consumption and hazardous waste by 95%; testing and evaluation of the use of textured coatings to improve cell efficiency; improvements in EFG cell efficiency by optimization of metallization firing conditions; initiation of work on an optimized cell grid design; production of test samples of cells designed for interconnection on the rear side only; and demonstration of average efficiencies over 14.0% in more than 5000 EFG cells during one 2-week period. The "Task 3: Modules" accomplishments include testing of new encapsulants promising reduced lamination time and improved yield; initial design work completed on new module frames that are both less expensive and faster to attach to modules; completion of initial testing and design work for lower-cost module diode housing; and concept developed for improved collection of light from area between cells in modules.

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