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Seventh Workshop on The Role of Impurities and Defects in Silicon Device Processing

Summary of the Panel Discussions

August 11–13, 1997
Vail, Colorado

Workshop Chairman:
Bhushan Sopori

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1. Overview

The Seventh Workshop on the Role of Impurities and Defects in Silicon Device Processing, held August 11-13, 1997, in Vail, Colorado, was a great success. The workshop theme, "R&D Issues for Crystalline Silicon to Support GW/yr Goal by the Year 2010," provided a focus that proved both timely and stimulating. The workshop attracted 76 attendees from six countries, who participated in lively discussions of the issues. This is an upbeat time for the photovoltaic industry as sales passed 100 megawatts per year. The workshop revealed that worldwide R&D in silicon PV is stronger than ever. The new thin-Si technologies are developing remarkably fast since the resurgence in their interest about 10 years ago. A number of groups around the world are reporting cell results with efficiencies above 9% from polycrystalline cells deposited on low-cost substrates. Conventional wafer and ribbon Si manufacturing costs continue to come down as new capacity is added. Detailed studies on manufacturing costs convincingly show, for the first time, that module manufacturing costs in the range of $0.70 to $1.90 per watt are achievable with manufacturing volumes per facility in the range of 100 to 500 megawatts per year. Such cost reduction will improve profitability and allow expansion into ever-larger markets. This encouraging prognosis for future technology, when coupled with the current climate of 20% market growth despite stable, or even increasing, module prices, signals the eminent emergence of PV as a vital, global industry. Exciting times indeed; one gigawatt per year is not so far away!

The workshop comprised 19 oral presentations, 22 poster presentations, and 5 panel discussion sessions. In addition to the presentation of the university results that were a part of the NREL Silicon Materials Research Program, the workshop included a number of talks presented by internationally recognized experts on Si growth, defects, and hydrogen in silicon. These talks indicated that the enormous research effort of the silicon integrated-circuit (IC) industry has important effects on the emerging Si PV industry.

2. University Program and Fundamental Research Results

This year, the traditional session on impurity gettering was replaced by a review of NREL's Crystalline Silicon Materials Research Program. This program was initiated 5 years ago and embarked on an ambitious plan to:

- Develop suitable techniques and perform detailed characterization of various PV substrates and cells. Develop a detailed data base of impurities and defects in commercial PV substrates and solar cells.
- Identify cell performance-limiting defects and the associated mechanisms.

- Perform modeling/analyses to determine how these limitations on the cell performance can be overcome by suitable processing schemes.
- Develop an in-depth knowledge base for impurity gettering and defect passivation as post-growth, quality-enhancement processes, including information "imported" from the microelectronics industry.
- Attempt to integrate quality-enhancement steps into cell processing to ensure maximum cell efficiency at a minimum cell-fabrication cost.

The subcontract program was supported by in-house research at both NREL and Sandia, along with strong interactions with the PV industry. This program has been very successful in developing and applying post-growth quality-enhancement techniques to improve the efficiencies of solar cells fabricated on commercial Si substrates. Many of these processes or process modifications have already been adopted by the PV manufacturers into their production lines. Detailed investigations and theoretical modeling have been very helpful in identifying the bottlenecks in the path of reaching 18%-efficient commercial solar cells.

Following are major results of the research under this program.

2.1 Defects/Impurities

Many commercially available materials were analyzed to identify impurities and the types of defects and their distributions using PVSCAN5000, the SPV technique, and the laser microwave photoconductive decay technique. In addition, solar cells were fabricated by optimized processes and were then analyzed. These data led to the following conclusions:

- The dominant defects are intragrain dislocations. Dislocations can be selectively present in certain grains, which leaves other grains with a low or zero dislocation density. The defective grains contain clusters of dislocation loops and networks, which may be decorated by impurity precipitates.
- The dominant impurities are C, O, Fe, and Cr.
- The dominant defects in grains containing no dislocations are the so-called micro-defects. The exact nature of the micro-defects is not known, but it is believed to be related to oxygen or carbon precipitates or frozen-in point-defect clusters.

2.2 Impurity Gettering

- Cl, P, and Al gettering techniques all work well in IC-grade or solar-grade multicrystalline Si with a low-defect density, leading to improvements in the average material quality of PV substrates.
- High-temperature gettering can degrade the material quality of PV substrates and cells. This is believed to arise from dissolution of impurities precipitated at the defect sites.
- Optical processing and RTA produce effective gettering of transition metals at significantly lower temperatures (<700°C).

- Defect clusters cannot be gettered (or passivated) well. Network modeling established that the localized regions of high dislocation density (defect clusters) can shunt the device. The defect clusters can act as current "sinks" that dissipate the power within the cell, and thus, can be very detrimental to the cell performance.
- A diffusion segregation model was developed to help understand the conditions needed for dissolving precipitates that appear to be the bottlenecks in improving cell performance by gettering.

2.3 Hydrogen Diffusion/Passivation

Investigations into hydrogen passivation included both theoretical and experimental studies.

- Calculations done at near the ab-initio, Hartree-Fock level in molecular clusters, and the molecular dynamic (MD) calculations, have yielded the following results: the "normal" diffusion of H^0 or H^+ occurs by hopping from bond center (BC) to BC sites with an activation energy of 0.5 eV. However, MD simulations show that a metastable state of H^0 results in much faster hopping among tetrahydral (T) sites, without involving BC sites. Further, a (V-H) pair appears to be mobile.

The main results from the experimental work are:

- Hydrogen diffusion at low temperatures occurs predominantly via a [V-H] complex.
- The diffusivity of H in Si can vary in materials grown by different vendors by several orders of magnitude.

2.4 Solar-Cell Fabrication

- Al gettering and Al-BSF formation reduces the back-surface recombination velocity (BSRV) to 200-400 cm/s and improves the bulk lifetime, τ_b, of lower-quality Si.
- The conditions for optimum gettering for different commercial PV materials were found to be different.
- PECVD nitridation, for depositing an AR coating, can produce passivation with a significant increase in τ_b.
- Forming-gas anneal produces passivation in some cells.

Solar cells, fabricated by these processes, yielded the record 18.6%-efficient cells on HEM material, 16% on EFG, 17.2% on dendritic web, and 15% on string ribbon.

2.5 Cleaning Chemistry

Although solar-cell processing is not done under a rigor comparable to microelectronic device processing, there is an increasing need to maintain cleanliness during processing. As the cell efficiencies increase, the need to minimize contamination is also growing. This is particularly important if the substrate already has a low concentration of metallic impurities.

Thus, further indiffusion of impurities must be prevented. Such contamination can occur not only from high-temperature processing, but also from steps such as cleaning. The latter issue was investigated. It was found that metals will dissolve from the Si surface into the cleaning solution in a certain pH range of the solution, whereas the reverse will happen in other pH ranges. Clearly, the former is the preferred condition for cleaning Si materials.

3. Discussion 1: Important Industrial Issues for the Year 2010 Goal

Discussion Leader: Chandra Khattak

Panelists: Jim McCormick, Dominique Sarti, Juris Kalejs, Hans Möller, Katsuhiko Shirasawa, Tim Tomlinson, Terry Jester

The results of a major cost study funded by the European Union, and the inferences from the Sunshine Project on Crystalline Silicon, concurred that module manufacturing costs well below $2.00/W can be realistically achieved when manufacturing volume is over 500 MW/yr. Ribbon Si is projected to yield module manufacturing costs of only 0.71 ECU/W. Aside from increased manufacturing volume and the capital commitment, the 1-GW/yr production requires that a number of other issues be resolved that pertain to the feedstock availability, production equipment and automation, wafer slicing, wafer-handling tools, processing tools, metrology and process control.

3.1 Feedstock Availability

Feedstock availability was extensively discussed because reliable sources of Si feedstock have been a perennial problem for PV manufacturers. Presently, the feedstock consists of scraps from the IC and poly-Si industries. Although, in the past the availability of Si feedstock has increased each year, such a growth rate is not expected in the near future. It is expected that a 1-GW/year PV production would require 5-8 kton of Si feedstock. This quantity of scrap may not be available from the IC industry, prompting investigations into a source dedicated to supply the PV industry. However, feedstock need may be significantly reduced by going to ribbon substrates and larger-diameter CZ wafers. Additional conservation can be attained as the wire-sawing technology matures to produce thinner wafers. Finally, thin film Si solar cells can provide a great reduction in the usage of Si. Hence, it is not clear how important is the need for a dedicated PV feedstock.

3.2 Production Equipment

1-GW/year production capability is likely to invoke a variety of production equipment and diagnostic/monitoring tools. Such facilities are essentially unavailable. Although some equipment and tools can be carried over from the IC industry, there is a need for developing

equipment specific to solar-cell technology needs. However, because of the diversity of substrate and cell types, it seems that for the same processing step a variety of equipment may be needed.

3.3 Wafer Slicing

The introduction of wire saws has been an important contribution to reducing module prices. Nevertheless, sawing remains the highest-cost step in cell manufacturing. Further improvements in wire sawing will have important cost implications.

3.4 Wafer-Handling Tools and Automation

Increased automation is a key to reduced cost. Wafer-handling is the most important area to automate. Unfortunately, the requirements of the PV industry are so different from the microelectronics industry that conventional Si wafer-handling equipment is not particularly useful. On the other hand, the PV industry is too small to have spawned the emergence of much of a PV-manufacturing-equipment industry. This needs to change before large, automated factories can be built. For each PV company to independently fund the development of its own equipment would be prohibitively expensive. Some standardization of wafer sizes and specifications is needed for the PV industry (similar to the SEMI standards for microelectronics). An important avenue for reducing cell material cost is to reduce cell thickness. Manufacturers have already done this to the extent that further reductions are counter-productive because of increased wafer breakage. The development of processing and wafer-handling procedures that work with thinner wafers will allow further improvements in this area.

3.5 Cell Processing Tools

Si PV manufacturing has its roots in the broader Si device industry, and the typical manufacturing equipment of diffusion tubes, etc., belies this heritage. At the high volumes contemplated in the year 2010 goals, higher-throughput tools are needed. Rapid thermal processing and continuous-belt furnaces are examples of approaches that need to be developed to see if they are suitable.

3.6 Metrology and Process Control

At high manufacturing volume, any delay in process monitoring can result in large amounts of scrap. Development of real-time, high-speed process-control measurement instruments that ensure product quality at high throughput is an important requirement for higher-volume production.

3.7 Marketing

It was recognized that a suitable marketing strategy is needed for the Third-World-specific issues, including items such as financing concepts and availability of systems. Environmental factors are also a concern, e.g, using CdTe type of materials.

4. Discussion 2:
Fundamentals of Crystal Defects and Impurities in Silicon

Discussion Leader: Teh Tan

Panelists: Ted Ciszek, Fritz Kirscht, Takao Abe, Subash Mahajan

This discussion addressed the basic aspects of impurities, grown-in defects, impurity defect interactions, and electrical activity of defects. The highlights of some of the issues are given below.

4.1 Metallic Impurities

Metallic impurities permeate all phases of PV Si solar cell production — low-grade feedstock and its handling, lower quality furnace parts, and location and operation of process equipment all add to this saga. There is a general awakening in the PV industry to "clean up" some process steps. Many manufacturers have recognized that a higher-quality feedstock results in higher yields that can offset the higher prices of the feedstock. The use of a higher-quality feedstock may raise the question whether a general cleaning-up effort in crystal-growth and cell-processing facilities is desirable – and cost effective – in the long-run (i.e., for 2010 at 1-GW/year production rate). No reasonable answer has been found.

4.2 Grown-in defects in Si

Grown-in defects in the IC Si are of the "swirl-defects" category. The A-type defects in FZ and CZ Si are interstitial (I) type dislocation loops that apparently form because of condensation of a net excess of I. The D-type defects in FZ Si are vacancy (V) clusters that form apparently because of condensation of a net excess of V. The D-type defect equivalent in CZ Si are voids coated by thin SiO_2. In large-diameter crystals, A-defects form at the crystal-rim region, while D-defects form in the crystal-center region separated by an apparent defect-free ring-region. In CZ Si, A and D-defects may coexist in the same region.

Theoretical studies of the grown-in defects do not provide accurate results because the values of the parameters are not accurately known. The following equations are fairly reliable:

$$D_I C_I^{eq} \approx 10^3 \exp(-5\ \text{eV/kT})\ \text{cm}^2\ \text{sec}^{-1}$$

$$D_V C_V^{eq} \approx 0.6 \exp(-4\ \text{eV/kT})\ \text{cm}^2\ \text{sec}^{-1}$$

The individual components D_I, C_I^{eq}, D_v and C_v^{eq} are not.

The most reliable estimate of formation and migration enthalpy are:

$h_i^f \approx 4$ to 4.5 eV,
$h_I^m \approx 1$ to 0.5 eV

and

$h_v^f \geq 3.4$ eV,
$h_v^m \leq 0.6$ eV.

Such uncertainties tremendously hamper the understanding of the grown-in defect formation process. Other factors hampering the interpretation include (1) whether v/g (growth-rate/thermal-gradient) or just g alone determines the types of defects formed, and (2) whether a model involving the presence of oxygen in addition to the radial I and V diffusion may work for CZ Si.

4.3 Large Diameter Ingots

To achieve the 1-GW/year goal in 2010, low-cost, 400-mm-diameter Si crystals must be grown with a high growth rate. Such crystals are likely to contain many D-defects, which can be treated by RTA to obtain a defect-free surface. Low-cost slicing is also needed. A 400-mm CZ crystal, 1.2 m in length, weighs ~ 800 kg, which cannot be supported by a 3-mm seed neck. The remedies are (1) double necking, and (2) a dislocation-free seed with a taped tip to dip into the Si melt before growth.

4.4 Swirl Defects in MC-Silicon

Characterization efforts on "swirl defects" in MC-Si is nonexistent. However, these defects could be responsible for nucleation of dislocations. For example, if A-type defects form, then thermal stress will generate large-sized intra-granular dislocations from A-defects by cross-slips. GB is also a source of dislocations in MC-Si.

4.5 Metal-contaminated (in growth) CZ Si

The results of single-crystal wafers grown with controlled concentrations of metals have provided interesting clues. The electrical activity is dominated by $M \geq 10^{13}$ cm^{-3} in p-type Si, but already at 10^{11} cm^{-3} in n-type Si. The severity of the electrical activity, in descending order, is Ti, Mn, Cr, Fe, Ni, Zn, and Cu. When oxidized at 900°C for 1 hour, p-type Si shows little electrical activity change; but in an n-type wafer, the wafer center recovers, while the wafer rim region deteriorates, implying the formation of extended defects in the wafer-rim regions that gettered M.

5. Discussion 3: Effects of Impurities and Defects

Discussion Leader: Kim Kimerling

Panelists: H. J. Möller, Lubek Jastrzebski, George Rozgonyi, Worth Henley, Yukio Takano, James Gee

The discussion was centered about using newly gained insight in addressing future works in the applications area, including the roles of:

- Dislocations
- Transition-metal precipitation
- Oxygen precipitation
- Nitrogen.

There is the general feeling that knowledge gained in the area of gettering in the NREL-sponsored PV community has surpassed, in many aspects, that of the IC community; as such, the knowledge will also be useful for the IC community. In this sense, the group seems to be in a position to help the PV industry in areas such as efficiency and throughput. However, it cannot yet be said that all issues associated with the solar-grade MC-Si are resolved. For example, the Fe precipitation-dissolution cycling behavior, well understood for single-crystal Si, does not apply to MC-Si. Also, it is not yet firmly understood why gettering cannot improve the MC-Si "bad" grain regions, although the existence of metal precipitates is a plausible reason. Concerning gettering that involves precipitated metals, modeling has shown the ineffectiveness of the process at lower temperatures for short times; however, gettering at high temperatures should be effective. There are some RTA data indicating that this may indeed be the case.

There is the need to characterize the kinds of metal impurities present in MC-Si and to develop monitoring and control schemes for solar-cell processing, at a cost. The alternative would be some blanket cleaning schemes for crystal growth, as well as processing facilities, also at a cost. The industry needs tools that can rapidly map desired parameters such as defects, minority carrier diffusion lengths, etc.

One last issue discussed concerns whether the NREL support to universities should be concentrating on fundamental or industry-support research. No conclusion was reached.

6. Discussion 4: Passivation

Discussion Leader: Stefan Estreicher

Panelists: Juris Kalejs, Ajeet Rohatgi, Michael Stavola

It is known that hydrogen in Si passivates grain boundaries, some "good" dislocations, point defects, and some transition metals. However, Si does not passivate the "bad" dislocation, some other transition metals, and materials rich in oxygen. The reason hydrogen is not effective in O-rich Si is that O atoms in Si attract H to form pairs. The reason that hydrogen will not passivate some transition metal atoms is that such H-M pairs can themselves be electrically active. We have no understanding of why "bad" dislocations cannot be passivated.

Other issues not understood include the role of Si surface damage, p-n junction, enhanced hydrogen diffusion, and the detailed manner of H interaction with different metal atoms and defects. The role of hydrogeneration processes, e.g., I/I, plasma, FGA, and PECVD of Si_3N_4, is also not understood.

The hydrogen passivation process will be less effective at T much higher than 450°C, because in general, an H-X (X:defect) or H-M will be unstable, and hence, will not form at the high temperatures.

7. Discussion 5: GW Solar-Cell Processing Requirements

Discussion Leader: Kim Mitchell

Panelists: Tohru Nunoi, Shreesh Narasimha, Tadashi Saitoh, Katsuhiko Shirasawa, Mehmet Ozturk, Andrew Blakers

At a GW/yr level of PV energy capability, the cell production rate can be very large. For example, if we assume the size of the cell to be 250 cm^2 and the cell efficiency as 20%, 1 GW/yr would require $2x10^8$ wafers/yr to be processed into cells. Such a production implies a processing time of 0.15 s/wafer, which is not feasible for one processing line. This time becomes 10 s/wafer for 100 lines. The needed feedstock should be ~5 kton/year, which may be obtained either from IC scraps or from a dedicated manufacturer; e.g., Kawasaki Steel (50% backed by the Japanese government) has plans to produce 300 tons/year by 2000, and 1.5 kton/year by 2010.

Obviously, a number of issues need to be addressed in cell and module manufacturing. (a) Throughput may be a problem, and it is not simply dependent on the cell fabrication rate. (b) Rapid- thermal processed cells showed efficiencies matching thermally processed cells, provided RTO passivation is used. (c) Screen-printing passivation loses 2%-3% in efficiency. (d) Laboratory cells save processing time up to 20 times by RTP/cell; however, this rate cannot be directly translated into throughput because RTP is not a batch-processing scheme. (e) Single-wafer processing may be rapid, but it does not have a throughput equivalent to furnace processing throughput. (f) Tools, involving UHV, may be extremely difficult to operate and extremely expensive.

Concentrator Si cells, and other competitive cells (e.g., thin-Si-film cells and non-Si-material cells) will have their niche share in the 1-GW/year market.

8. Recommendations for Future Research

There was consensus that to achieve the 1-GW/yr market size, the cost of photovoltaic modules must decrease. This can come from a combination of improved performance, improved processes, and increased manufacturing volume. The following areas for R&D were highlighted as especially important toward meeting the goals.

- **Bad grains in multi-crystalline silicon**

  The gettering work has greatly improved our understanding of the process of gettering. Researchers have found that some grains have poor performance because of dislocation tangles and associated precipitated (or agglomerated) phases of transition metals. To date, the success in repairing the worst grains has been limited, although directions for future research are suggested. Prior results in gettering and hydrogenation have already narrowed the performance gap between single crystal and multi-crystalline cells to 1 to 2 percentage points. Success in learning how to getter bad grains would essentially eliminate this gap.

- **Continued improvements in understanding the science of gettering**

  Although understanding of both the phenomenology and theoretical background of gettering mechanisms has increased greatly, there remain important issues needing resolution. Foremost among these issues is what is actually being gettered and what are the sources of these contaminants. A better understanding of transition metals in silicon is needed—their defect structure, diffusion, and complexes with dopants, carbon, and oxygen. The interaction of hydrogen with transition metal complexes is now recognized as an important, but unexplored area, especially because recent findings indicate that hydrogen does not passivate all types of defects.

- **A more practical source of hydrogen**

  Now that hydrogen passivation is established as an important tool for improving multi-crystalline and ribbon-cell performance, it is important to find lower-cost, higher-throughput methods of hydrogenation, i.e., methods that can be added to conventional production processes with little added cost.

- **Low-cost, high-efficiency processes**

  Complex laboratory cells have explored the upper bound in possible silicon-cell performance with efficiencies over 24%. These results point out the possibility of considerably improving commercial cells from their current range of 14% to 15%. To date, however, most of the high-efficiency processes are not cost-effective for commercial modules. What is needed is extensive searching for innovative new processes that capture much of what is possible in laboratory cells, but with costs comparable to current commercial practice.

- **Improved screen printing**

  Screen-printed contacts represent one of the largest constraints to improved performance because of their large line widths and poor metal-semiconductor contact properties. Research in improving the screen-printing process could pay considerable dividends.

- **What is solar-grade silicon, and where will it come from?**

  The early work on defining the silicon-quality needs of the PV industry is now 15 years old and needs to be revisited in the context of both our current understanding of the role of transition metals, as well as the higher performance now expected from silicon cells. The industry can probably continue for some time to use scrap silicon from the microelectronics industry, but a better understanding of what is acceptable scrap is needed.

- **Czochralski silicon**

  Most research has focused on multi-crystalline silicon; however, Czochralski silicon remains the largest source for production solar cells at this time. There is much room left for optimizing the Czochralski process for producing solar-grade wafers. In fact, if practical production processes are found that give over 20%-efficient cells, these processes will probably not give such high efficiency on multi-crystalline silicon. Therefore, a parallel program incorporating studies on the growth and manufacturing of Czochralski silicon cells is warranted.

- **Experimental facilities**

  There was a general concern that few laboratory facilities are capable of dealing with the large wafer sizes (125 to 200 mm) becoming common for solar-cell manufacturing. This makes it difficult to do research that is relevant to high-volume manufacturing.

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13. ABSTRACT *(Maximum 200 words)*

This report is a summary of the panel discussions included with the Seventh Workshop on the Role of Impurities and Defects in Silicon Device Processing. The theme of the workshop was **"R&D Issues for Crystalline Silicon to Support GW/Yr Goal by the Year 2010."** This workshop provided a forum for an informal exchange of information between researchers in the photovoltaic and nonphotovoltaic fields on various aspects of impurities and defects in silicon, their dynamics during device processing, and their application in defect engineering. This interaction helped establish a knowledge base that can be used for improving device-fabrication processes to enhance solar-cell performance and reduce cell costs. It also provided an excellent opportunity for researchers from industry and universities to recognize mutual needs for future joint research.

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