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High-Efficiency GaAs Solar Cells on Polycrystalline Ge Substrates

Final Report

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1.0 EXECUTIVE SUMMARY

High-efficiency single-junction GaAs solar cells with an efficiency of 25.7% [1] and tandem $GaInP_2$/GaAs solar cells with efficiencies of 29.5% and 30.2% under AM1.5G [2] and 140-180 suns [3], respectively, have been demonstrated on single-crystal GaAs substrates. The goal of this effort was to investigate and effect a transition of these high-efficiency cell results on to potentially low-cost substrates for flat-plate (1-sun and low-concentration) applications. Large-area polycrystalline Ge substrates offer reduced cell substrate-cost as well as cell processing-cost, both on a unit-area basis. Development of GaAs solar cells on large-grain poly-Ge substrates appears to be a good first step towards the transitioning of these cells on to other low-cost substrates through an understanding and amelioration of the various loss mechanisms.

Our initial attempt at developing GaAs solar cells on such poly-Ge substrates had been successful. Under AM1.5G simulation, a total-area efficiency of 15.8% [4] was obtained for a p^+-n GaAs solar cell on large-grain poly-Ge substrate and no degradation of efficiency was observed in going from cell areas of 0.25 cm^2 to 1 cm^2. The use of large-area poly-Ge substrates with well-established large-scale MOCVD growth is expected to allow cell-processing costs to be reduced significantly. Cast, large-area, poly-Ge substrates, with an average grain size of 1 cm, are commercially available and have been qualified as substrates for GaAs cell growth [4].

The objective of this program, therefore, was to further improve on the performance of GaAs solar cells on poly-Ge substrates. Material and device issues related to the development of GaAs solar cells on poly-Ge substrates were addressed. Key material physics issues include the use of Group-VI dopant, specifically Se, to passivate the grain-boundaries in the n-GaAs base to achieve large J_{sc} values. Device-structure optimization studies have led us to achieve an AM1.5 efficiency of ~20% for a 4-cm^2-area GaAs cell and an efficiency of ~21% for a 0.25-cm^2-area cell on sub-mm grain-size poly-Ge substrates. Key device physics issues include understanding of the dark-current reduction mechanism with an undoped spacer at the p^+-n depletion layer.

The successful demonstration of high-efficiency GaAs cells on sub-mm grain-size poly-Ge substrates motivated us to develop high-quality GaAs materials on lower-cost substrates such as glass and moly foils. We achieved a best minority-carrier lifetime of 0.41 nsec in an n-GaAs thin-film on moly. The role of Group-VI dopant in the possible passivation of grain-boundaries in has been studied in GaAs films on moly foils. We believe the development of PV-quality GaAs material with minority-carrier lifetimes in the range of 1 to 2 nsec are achievable on low-cost moly foils and, if so, can significantly impact the use of GaAs solar cells for terrestrial PV applications.

2.0 INTRODUCTION

GaAs solar cells grown on single-crystal GaAs substrates have achieved impressive high-efficiency results. Specifically, a single-junction GaAs cell has achieved an efficiency of 25.7 percent [1]. A variety of GaAs-based multijunction cell concepts have also been demonstrated with high efficiencies, under AM1.5 1-sun conditions. This list includes the monolithic, tunnel-interconnected, two-terminal, $GaInP_2$/GaAs cascade with an AM1.5 efficiency of 29.5 percent [2]. Monolithic, tunnel-interconnected, multi-junction cells offer the best scope for realizing high efficiencies at costs comparable to those for single-junction cells. The $GaInP_2$/GaAs cascade is such a device and has demonstrated the highest, 1-sun efficiency for a two-junction cascade solar cell.

Single-crystal Ge substrates became the first-demonstrated, effective, low-cost alternative to the more expensive single-crystal GaAs substrates for GaAs solar cells [6]. This clearly was a result of the fact that Ge is lattice-matched as well as thermally-matched to GaAs. Ge substrates also offer significantly improved mechanical strength than GaAs substrates, even when sliced into thin (~ 4 mil) substrates. The use of a thinner substrate offers considerable scope for reducing substrate cost as well. Ge being an elemental semiconductor, its bulk crystals are easier to pull with improved yield compared to GaAs, and this can lead to a lower-cost substrate for solar cell growth.

GaAs solar cells on single-crystal Ge substrates have demonstrated efficiencies comparable to those on single-crystal GaAs substrates [6]. More importantly, GaAs solar cells on the Ge substrates have moved into manufacturing with excellent yield, almost twice better than that on GaAs substrates. These GaAs solar cells as well as GaAs/$GaInP_2$ multi-junction solar cells are presently produced for the AM0 satellite PV applications.

Cost analysis [7] indicates that the GaAs/Ge cell technology can compete very effectively with Si solar cells for point-of-focus, AM1.5 concentrator (X500) applications. However, for terrestrial flat-plate and low-concentration systems, the material cost associated with the single-crystal Ge substrates for the fabrication of GaAs and related $GaInP_2$/GaAs multi-junction solar cells need to be reduced quiet significantly. The use of polycrystalline Ge substrates for the growth of GaAs solar cells [4] and related $GaInP_2$/GaAs multi-junction cascade cells [8], respectively, are attractive toward this objective for flat-plate and possibly for concentrator applications as well.

Polycrystalline Ge substrates offer several advantages compared to single-crystal Ge substrates. First, they can be cast by a simple modified Bridgemann technique [9] to produce significantly large size wafers. For example very large area (up to ~ 24 inch diameter) cast poly-Ge substrates are commercially produced for optical applications. The use of larger diameter wafers for MOCVD growth can significantly reduce costs associated with substrate polishing, substrate-preparation for epitaxy, and most importantly, the solar cell processing cost on a per-unit-area basis. This adds impetus to the development of high-performance GaAs solar cells on large-area poly-Ge substrates for both flat-plate and concentrator applications. In contrast, wafer sizes greater than about 4-inch-diameter can cause crystallographic lineage problems with present-day single crystal Ge substrate technology. This can cause both yield and cell efficiencies to fall, thus preventing the transition on to large-area substrates.

The typical grain size in these polycrystalline-Ge wafers is about 0.4 mm to 1 cm, about an order of magnitude higher than even some of the highest measured bulk diffusion lengths (40 μm) in high quality GaAs materials grown on single-crystal GaAs substrates. Such grain sizes are more than adequate for solar cell applications since GaAs and other direct band gap materials have sufficiently high absorption coefficients.

3.0 GaAs GROWTH ON POLYCRYSTALLINE Ge

3.1 Optimization of Surface Morphology

We have investigated and reported [10] on the growth of specular GaAs-AlGaAs layers by MOCVD on poly-Ge substrates. We have shown that the variations in growth morphology across various grain-structures and boundaries are related to the difficulty of GaAs growth on non-(100) or near-(111) orientations. We have minimized this problem by the use of low growth rates (typically 0.04 μm/min.), the use of higher V/III ratios during MOCVD growth (typically >60), the use of optimal Se-doping levels, and optimum nucleation procedures including extremely low growth rates during growth initiation.

In our initial work, poly-Ge substrates were chemically etched, similar to single-crystal Ge substrates, during the polishing step prior to MOCVD growth. It was observed that this chemical etching step resulted in a non-flat poly-Ge substrate as a result of the different etching-rates of the various orientations present in the poly-Ge substrate. This uneven surface especially on the backside of the substrate can cause portions of the wafer to be not in good thermal contact with the susceptor, thereby leading to a non-uniform temperature distribution across the poly-Ge wafer. This typically exacerbated the problems of poor surface morphology of GaAs-AlGaAs layers on certain orientations of the poly-Ge substrates. In contrast, a chemo-mechanical polishing of the poly-Ge substrate resulted in significant improvement in "across-the grains" morphology of GaAs-AlGaAs layers. We have typically obtained uniform specular growth across 85 to 90% of the area of a typical 2" poly-Ge wafer with tens of different crystalline orientations. This was evident in the surface-morphology of GaAs layers grown on chemo-mechanical polished poly-Ge substrates [10].

3.2 Minority-Carrier Lifetime Measurements in GaAs double-hetero Structures

With the morphology of GaAs-AlGaAs layers on poly-Ge substrates under control, we conducted an optimization study of the minority-carrier properties of GaAs layers. Several GaAs-$Al_{0.8}Ga_{0.2}As$ double-hetero (DH) structures were grown at a growth temperature of 670°C. Photoluminescence (PL) decay was used to obtain minority-carrier lifetimes. All the DH structures were grown with a 2-μm GaAs buffer to minimize the effects of Ge auto-doping in the active region although 5-μm-GaAs buffer has been typically found to effectively eliminate any auto-doping effects. The lifetime-spread across various grains was reduced through the use of lower Se-doping for the $Al_{0.8}Ga_{0.2}As$ confinement layers. The lifetimes were comparable to

typical values obtained in GaAs DH structures, for similar buffer layer thicknesses, grown on single-crystal Ge substrates.

The reduced lifetime-spread across various grains was also evident in the typical variation of dark currents in GaAs p^+-n junctions located on the various grains of a poly-Ge substrate. Electron-beam-induced-current (EBIC) scans on p^+-n GaAs junction grown on poly-Ge substrates have indicated hole diffusion lengths in excess of ~1 μm near the depletion layer in the base region of the solar cell. This diffusion lengths are consistent with the typical lifetimes measured on DH structures. A longer diffusion length was typically estimated away from the junction region of the cell.

4.0 GaAs SOLAR CELL DEVELOPMENT ON POLY Ge

4.1 Baseline GaAs Solar Cells on Single-Crystal Ge Substrates

We initially conducted some baseline GaAs solar cell development on single-crystal Ge and GaAs substrates to demonstrate that good cell efficiencies can be obtained on these substrates. The typical cell data on both substrates are shown in **Table 1**, where both RTI-measured and NREL-measured efficiencies are indicated. The V_{oc} of the cells, including those on Ge substrates, were around 1.02-1.03 Volts suggesting good material quality. The typical performance of GaAs cells on single-crystal Ge substrates were comparable to those on GaAs substrates.

The highest total-area AM1.5 efficiency, in this set, is 22% on a GaAs substrate and 21.8% on Ge substrate respectively. We believe that we can grow, reproducibly, good GaAs cells on Ge substrates without the formation of a buried-junction in the Ge substrate. We also note from **Table 1** that the cell efficiencies on Ge substrates are relatively independent of the thickness of the GaAs buffer that is used to control the Ge auto-doping.

Table 1. Comparison of Single junction GaAs Cell Grown on GaAs and Single-crystal Ge Substrates

Cell #	Area (cm^2)	Substrate	Buffer Thickness (μm)	RTI-Measured Efficiency (%)	NREL-Measured Efficiency (%)
1-2102-a-1	1.04	GaAs	--	21.2	20.7
1-2101-b-2	0.2488	Ge	0.92	22.4	21.8
1-2105-3	0.2499	GaAs	--	22.8	21.6
1-2105-1	1.038	GaAs	--	22.7	22.0
1-2106-1	1.038	Ge	2.3	22.0	21.1

4.2 GaAs Cell Development On Poly-Ge

Shown in **Figure 1**, is a schematic of the GaAs solar cell device structure that we have developed [4] for use on polycrystalline Ge substrates. Note the undoped spacer between the base and the emitter. The undoped spacer at the depletion layer of the p^+-n junction has been shown to reduce the dark-current and improve the V_{oc}, fill-factor, and the efficiency of the cell on poly-Ge [4]. While the spacer has no effect in dark-current reduction in GaAs cells on single-crystal Ge substrates, there is a 40-fold reduction in the saturation dark current in GaAs cells with the spacer on poly-Ge substrates, as shown in **Figure 2**. The dark current reduction mechanism is further discussed in Section 4.2.3.

4.2.1 Effect of Various Defects in Poly-Ge Substrates

We have observed in an earlier work [10] that substrate-polishing defects such as dents/ledges/steps are more detrimental than grain-boundaries on GaAs solar cell performance. The GaAs solar cell data in **Table 2** illustrate this point. Here, we observe that the cell V_{oc} values do improve with larger grain-sizes, for a given spacer thickness of 0.12 μm. However, macro-polishing defects such as dents, ledges and steps in the cell active-area tend to reduce the V_{oc} values much more strongly than grain-boundaries. We believe this is a result of presence of higher electric-fields (in the p^+n junction) at the vicinity of these steps and ledges, causing excessive leakage-currents. Once again, the J_{SC} values were found to be less sensitive to the density of grain boundaries or such macro-polishing defects.

TABLE 2. Effect of grain size and other substrate-polishing defects on device performance.

Cell # 1-2322

Cell #	Area (cm^2)	Average Grain Size	Substrate Polishing Dents	V_{OC}(V)	J_{SC}(mA/cm^2)
1	0.25	1-2 mm	None	0.975	26.3
2	0.25	1 mm	Yes	0.87	25.8
3	0.25	1 mm	None	0.91	25.7
4	0.25	0.5 mm-1 mm	None	0.902	24.9
5	0.25	2 mm	None	0.945	24.9

4.2.2 Optimization of Ohmic Contacts to Poly-Ge Substrates

The Ohmic-contacts to poly-Ge substrates were optimized to improve the cell fill-factors. It became clear that typical Sb/Sn/Au contacts that have been typically used in RTI for GaAs solar cells on single-crystal Ge substrates were not suitable for poly-Ge substrates (doped less with Sb). We evaluated the use of AuGe/Ni/Au (500Å/100Å/3000Å) contact to n-type poly-Ge substrates. The metallization was applied through e-beam evaporation. The contacts were sintered at 365°C for 30 seconds. The typical resistivity of these contacts were <1 ohm-cm^2, about a factor of five lower than that obtained with Sb/Sn/Au contacts to poly-Ge substrates. With these contact resistivities, the Ohmic-drop was reduced to about 30 mV for a GaAs solar cell operating under AM1.5 1-sun condition.

4.2.3 Dark current reduction mechanism

The use of spacer for dark-current reduction in solar cell structures grown on poly-Ge was not unique to those for GaAs junctions. We observed a similar behavior in p^+-n $GaInP_2$ junctions grown on poly-Ge, as shown in **Figure 3**.

The reduction in dark current and the improvement in cell V_{oc} with the spacer are believed to be associated with the reduction of tunneling currents near the depletion-layer of the p^+-n junction in polycrystalline materials. Towards understanding this behavior, we conducted an experimental study of dark currents in p^+-n GaAs junctions as a function of temperature (77K to 288K). The temperature dependence of saturation dark currents in p^+-n GaAs junctions, without and with the undoped spacer, are shown in **Figure 4** and **Figure 5**, respectively. The temperature dependence of the saturation dark current in these two GaAs solar cells are compared in **Figure 6.**

We note that the junction without the spacer shows a stronger reduction with temperature. The activation energy for the saturation dark current with temperature is ~0.07 eV. We also note the apparent convergence of the two curves near zero Kelvin.

The band diagram of a p-n junction near the vicinity of a grain boundary, due to possible n-type Se-dopant accumulation at grain-boundaries, is expected to resemble that of a p-n^+ junction as shown in **Figure 7**. This would lead to electron tunneling (dark) current from the p-emitter to the n^+-base, depending on the empty states below the Fermi-energy (E_f) (see **Figure 8**) in the n^+-region. Such a model fits the temperature dependence of the saturation dark currents and the apparent convergence at zero K.

We therefore suggest that the reduction of these tunneling dark-currents may be a key to V_{oc} enhancement in many of the III-V p-n junction cells on polycrystalline substrates.

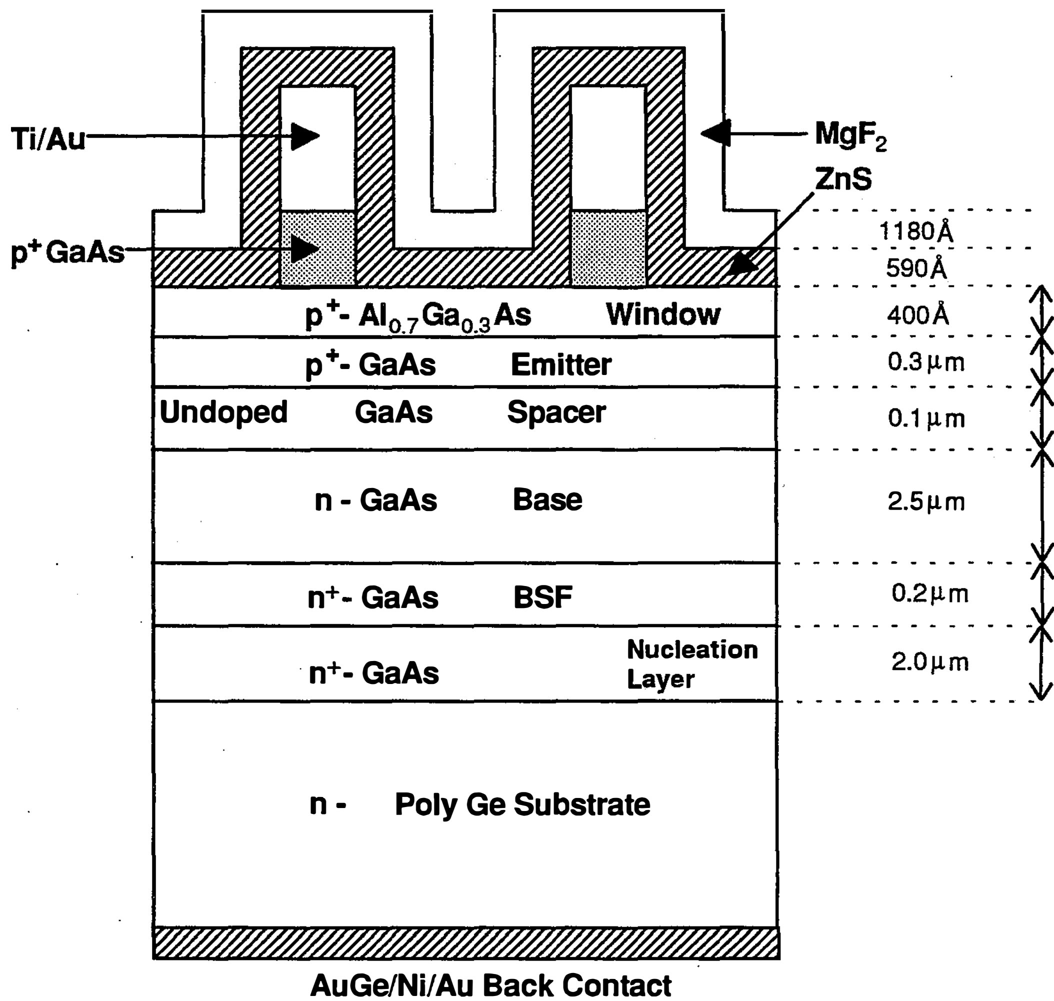


Figure 1. Schematic of a p^+n GaAs solar cell device structure on a poly-Ge substrate

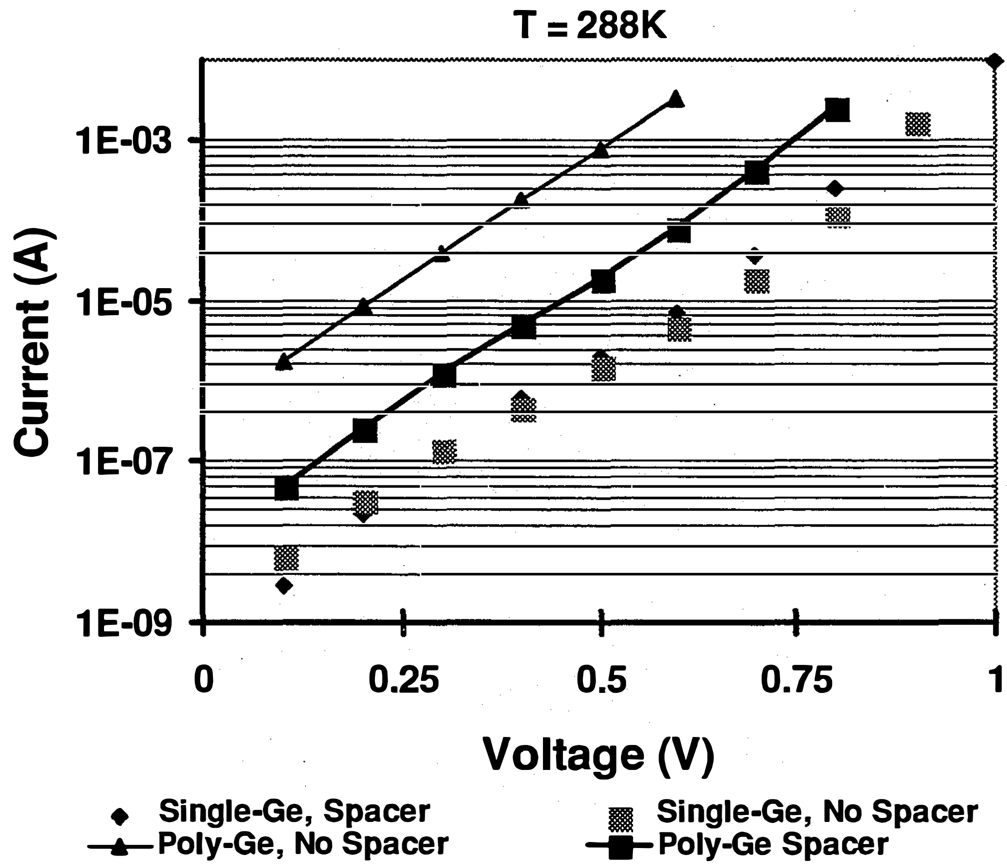


Figure 2. Effect of an undoped spacer on dark current reduction in GaAs cells; note the effect of spacer on single-crystal Ge versus poly-Ge substrates.

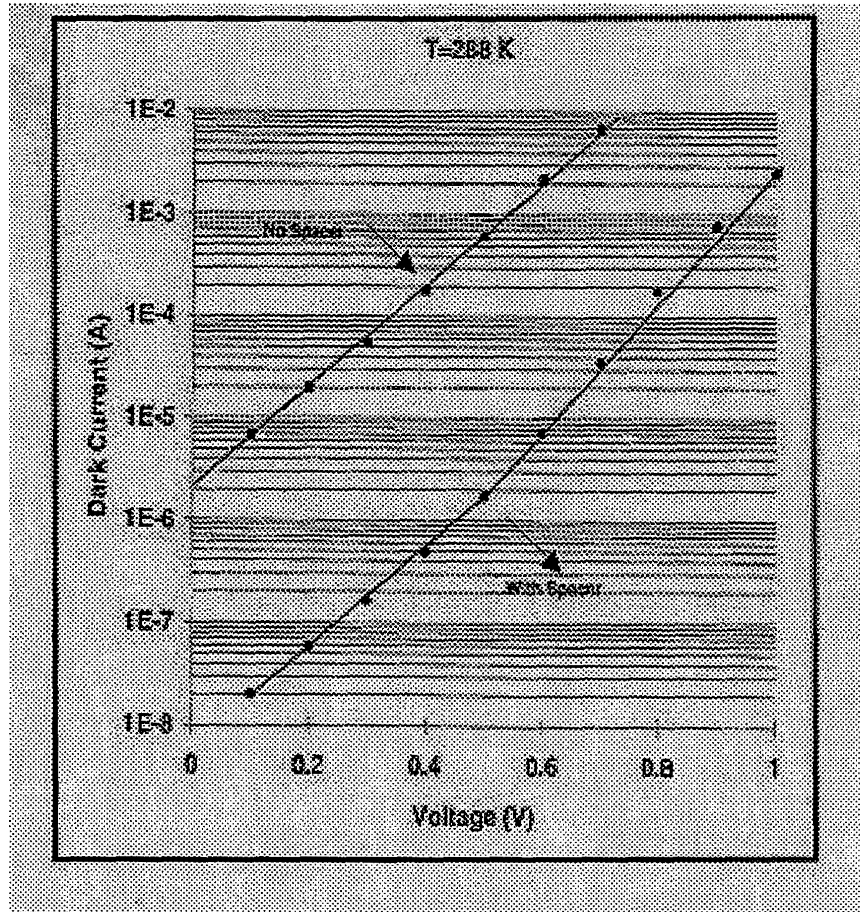


Figure 3 Dark I-V characteristics of p^+-n $GaInP_2$ junctions grown on poly-Ge with and without the spacer

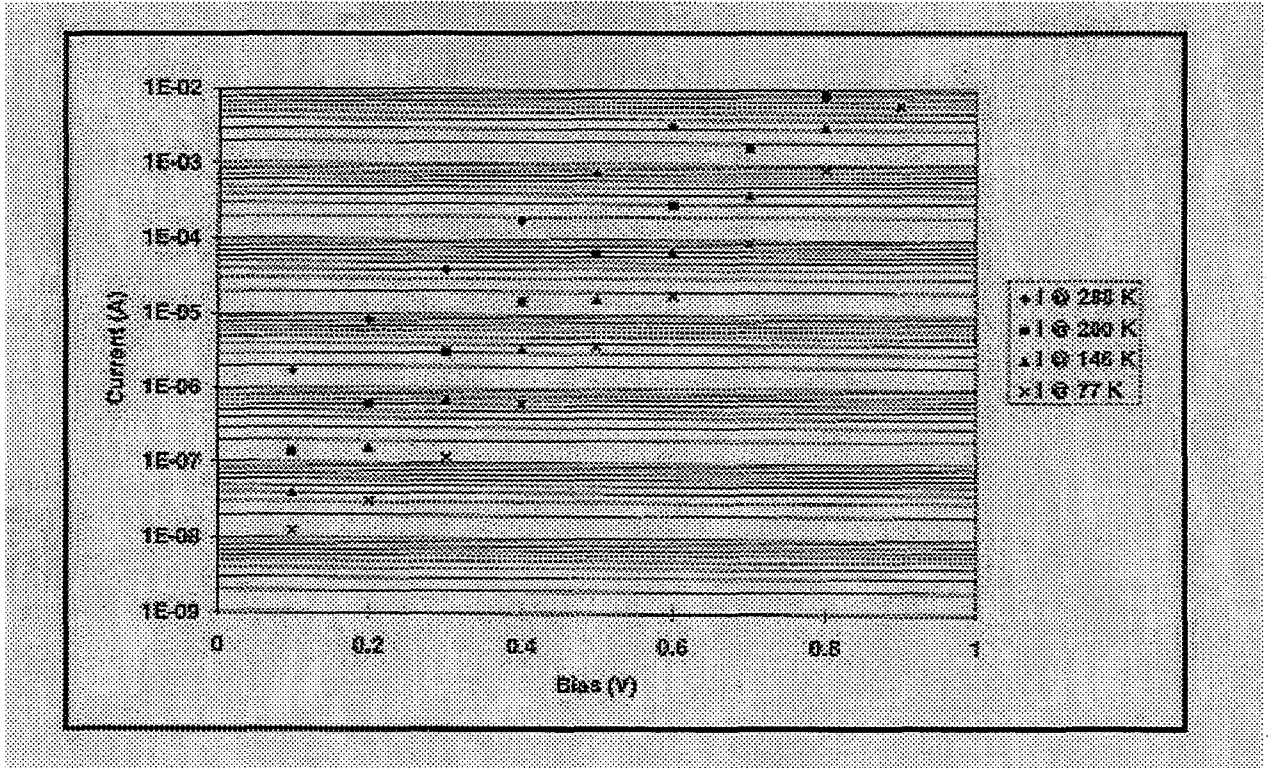


Figure 4 Temperature dependence of ark I-V characteristics of p^+-n GaAs junctions on poly-Ge (without the spacer)

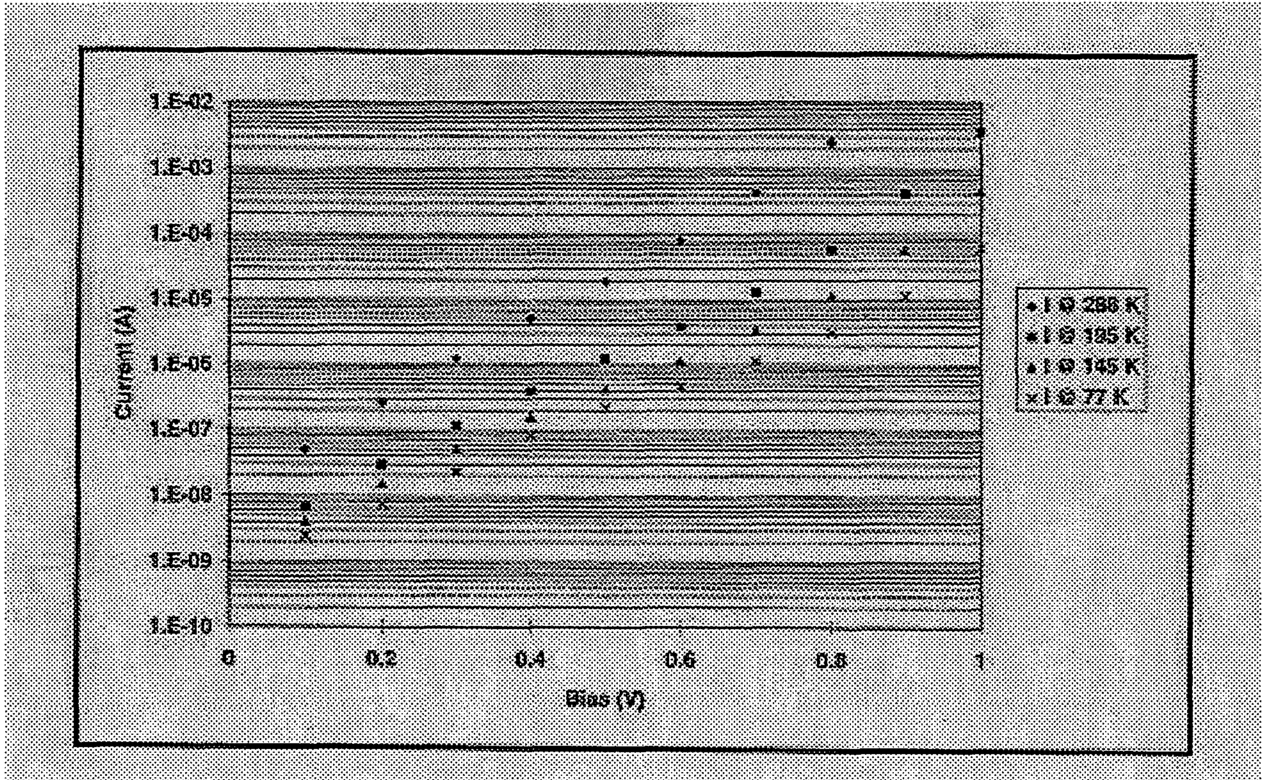


Figure 5 Temperature dependence of dark I-V characteristics of p^+-n GaAs junctions on poly-Ge (with the spacer)

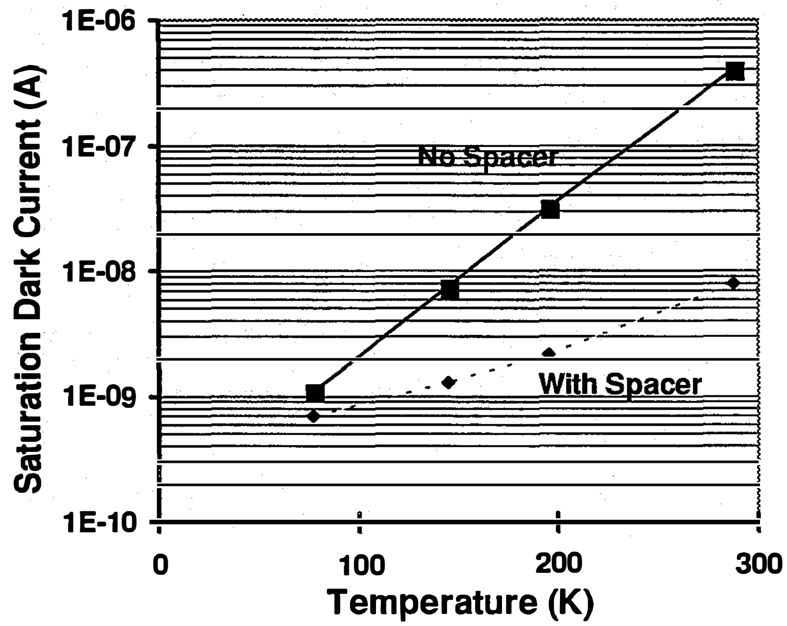


Figure 6 Temperature dependence of saturation dark current in GaAs cells on poly-Ge, with and without the undoped spacer.

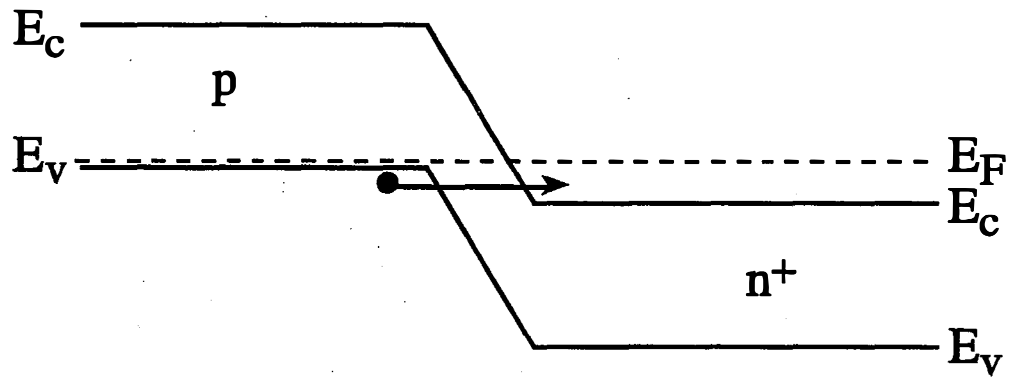


Figure 7 Schematic of electron tunneling from p-GaAs to the heavily-doped n^+-GaAs

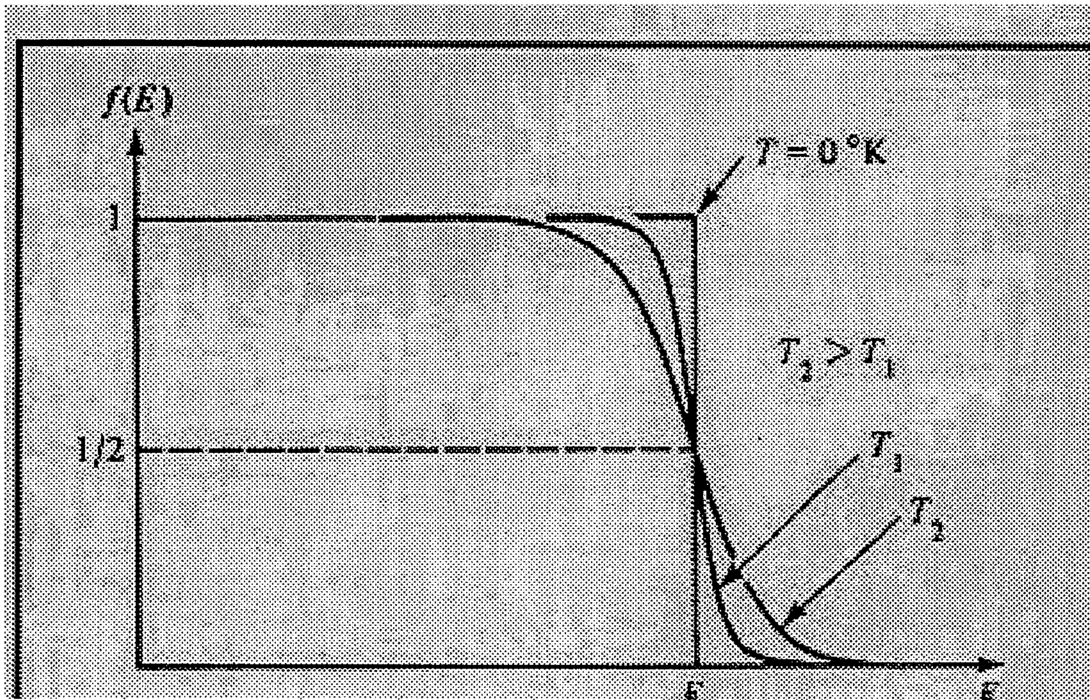


Figure 8. Fermi-Dirac Statistics for electron occupational probability near the Fermi-energy E_f.

4.2.4 J_{sc} and V_{oc} Optimization Procedures

In order to improve the efficiency of the p^+-n GaAs cells on poly-Ge, from our early result of ~18.2% with a J_{sc} of ~23 mA/cm^2 [5], we investigated several approaches to improve the blue-response of the cells. Reducing the thickness of the $Al_xGa_{1-x}As$ window, the use of an optimal emitter thickness, an optimized AR-coat, and a reduction of the emitter grid-metallization coverage, have all led to an AM1.5 J_{sc} of as much as ~27 mA/cm^2.

Towards the improvement of V_{oc} values, we considered a study of the optimum spacer thickness. We investigated the effect of varying the spacer thickness on cell V_{oc}, for approximately similar grain-size in the GaAs solar cells. A typical set of data is shown in **Table 3**. We conclude that as long as the spacer is thick enough to avoid tunneling of carriers between the heavily-doped p-GaAs emitter and the heavily-doped n-GaAs base regions, formed near the grain-boundaries and discussed in the previous section, a thinner spacer should be advantageous for lowering the dark current.

Under optimal spacer thickness, we have also considered the effect of the emitter thickness and the amount of emitter-grid metallization coverage on the V_{oc} of cells. The data shown in **Table 4**, suggest that a significant component to dark-current generation may be from the emitter-contact regions or from the $Al_xGa_{1-x}As$ window-GaAs cap hetero-interface in these poly-GaAs solar cells with an optimal spacer.

Table 3. Effect of Spacer Thickness on V_{OC} of GaAs Cells on mm-Grain-Size Poly-Ge; Cell Area ~4 cm^2.

Cell #	**Spacer Thickness (μm)**	**V_{oc} (V)**
1-2766	0.22	0.90
1-2763	0.14	0.96
1-2782	0.14	0.96
1-2786	0.10	1.00

Table 4. Effect of Emitter Thickness Plus Emitter Grid-Coverage on V_{oc} of GaAs Cells on mm-Grain-Size Poly-Ge Substrates; Cell Area ~4 cm^2

Cell #	**Emitter Thickness (μm)**	Grid Coverage (%)	V_{oc} (V)
1-2786	0.14	9	1.00
1-2804	0.22	9	1.01
1-2809	0.28	9	1.01
1-2840	0.28	5	1.03

4.2.5 Status of Efficiency of GaAs solar cells on Poly-Ge at the end of program

The material and device optimization studies have enabled us to achieve a significant improvement in large-area GaAs cell efficiencies on mm and also on *sub-mm* grain-size poly-Ge substrates. The typical grain structures and other crystalline features in the *sub-mm* grain-size substrates are as small as 400 μm as shown in **Figure 9(a, b)**. The RTI-measured data on 4-cm2 large-area GaAs solar cells on sub-mm grain-size poly-Ge substrates are shown in **Figure 10 (a,b)**. Also shown in **Figure 11** is the I-V characteristic and efficiency data of a small-area cell on sub-mm grain-size poly-Ge substrate.

The time-line of progress of cell efficiencies are summarized in **Table 5.** This indicates that the recent cell results are in spite of smaller, sub-mm grain-sizes in addition to higher resistivity of the starting poly-Ge substrates. The data in Table 5 clearly suggest that large-area GaAs cell efficiencies in excess of 20% are achievable on mm and sub-mm grain-size poly-Ge substrates. We observe that in the small-area, 21%-efficient cell, a V_{oc} of as much as 1.04 Volt and a J_{sc} ~ 27 mA/cm^2 have been observed, thereby approaching some of the best single-junction GaAs cell results on single-crystal GaAs substrates [1].

Table 5. Progress of GaAs Cell Efficiency on poly-Ge Substrates.

Ref.	Grain-Size (cm)	Cell Area (cm^2)	AM1.5 Eff. (%)
PVSC 1993 [4]	0.5	1	15.8
PVR&D 1995 [10]	0.5	4	16.6
PVSC 1996 [5]	0.5	4	18.2
Current state-of-art PVSC 1997	0.04-0.1	4	19.7
	0.04-0.1	0.25	21.2

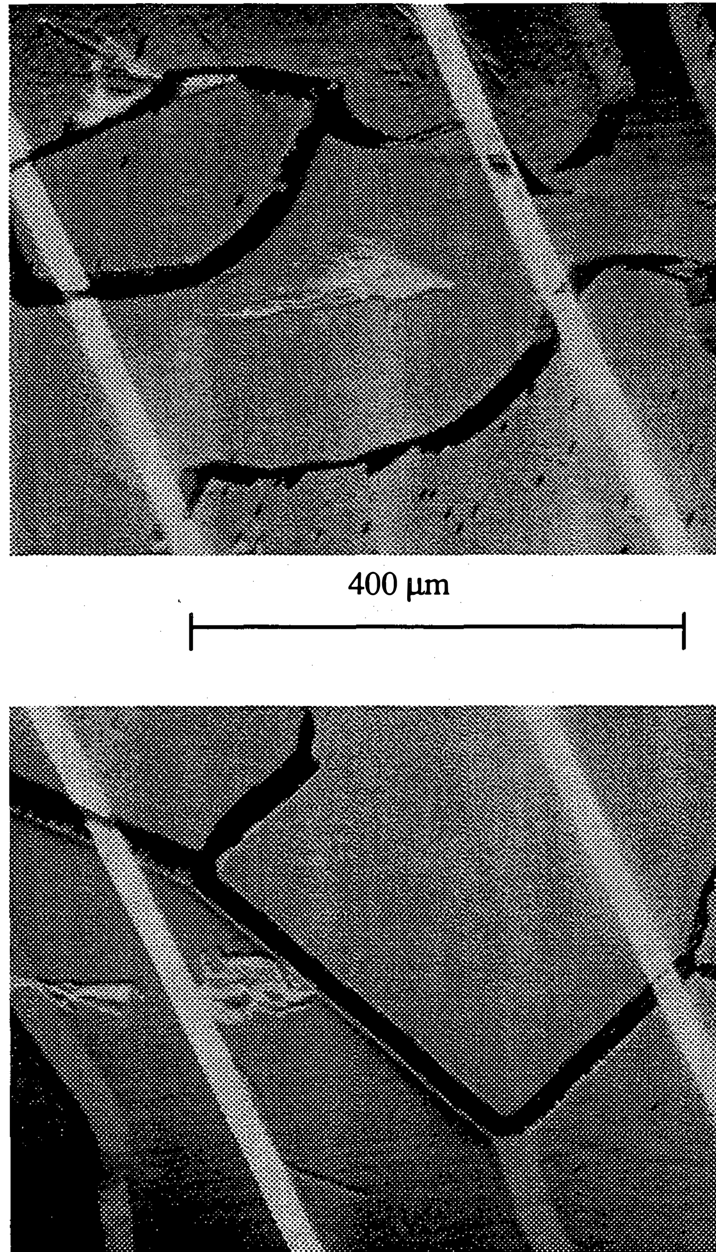
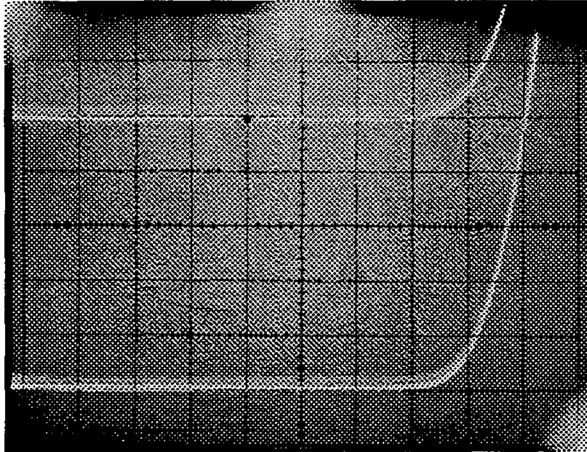
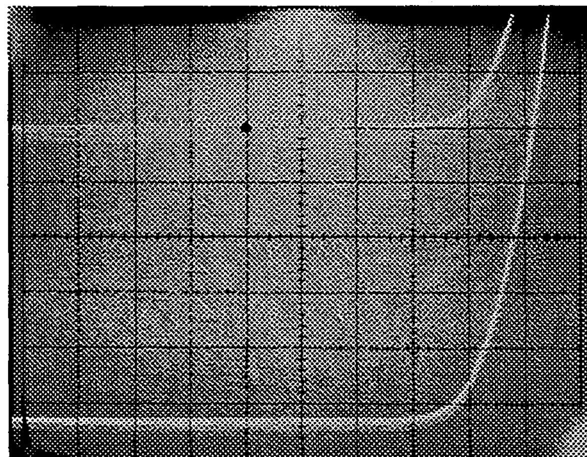


Fig. 9 (a, b) Typical microstructures in polycrystalline Ge substrate showing various crystalline orientations and grain boundaries.

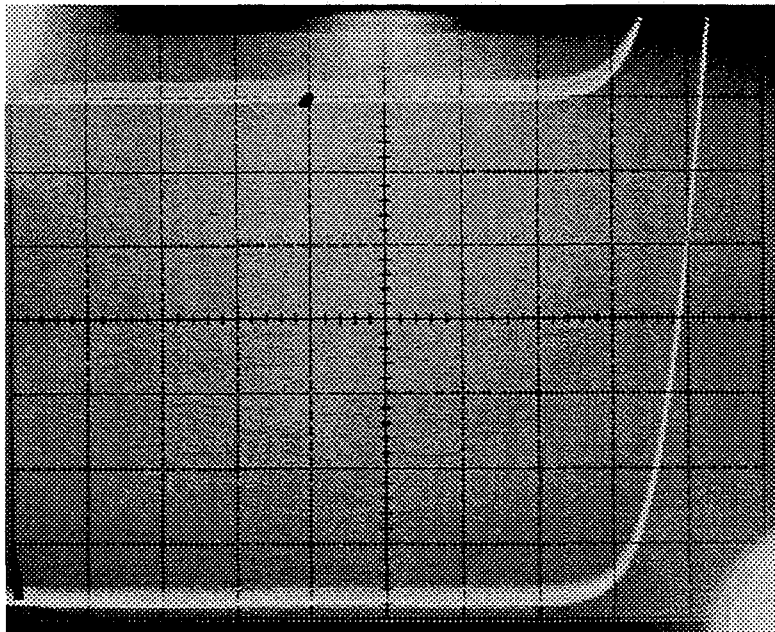


H:0.2 V/div. V:20 mA/div.
V_{oc} = 1.01 V, J_{sc} = 25.5 mA/cm^2, ff = 0.725
Total-area efficiency = 18.7%



H:0.2 V/div. V:20 mA/div.
V_{oc} = 1.03 V, J_{sc} = 26.3 mA/cm^2, ff = 0.725
Total-area efficiency = 19.7%

Fig. 10 (a, b) I-V characteristics of 4-cm^2 area GaAs solar cells on sub-mm grain-size poly-Ge



H:0.2 V/div. V:1.0 mA/div.
V_{oc} = 1.04 V, J_{sc} = 27.2 mA/cm^2, ff = 0.75
Total-area efficiency = 21.2%

Figure 11 I-V characteristic of a 0.25-cm^2-area cell on sub-mm grain-size polycrystalline Ge substrate

4.3 PV-Quality GaAs On Moly Foils

The successful transition of high-efficiency GaAs cells on to sub-mm grain-size poly-Ge substrates motivated us to consider the development of high-efficiency GaAs solar cells on significantly lower-cost substrates such as glass and moly foils. Thin moly-foils are attractive due to the thermal expansion match between moly and GaAs, the ease of cell fabrication with minimal or no backside contact processing, the mechanical strength of moly for manufacturing, and also for possible use in flexible, light-weight, solar arrays.

Minority-carrier lifetime is an important material parameter that directly affects the potential efficiency achievable in GaAs solar cells. **Figure 12** indicates the dependence of 1-sun AM1.5 solar cell efficiency as a function of the minority-carrier lifetime. This model is very similar to the work of Ref. 11. In this figure, we also indicate the GaAs solar cell efficiencies, as a function of lifetime, in two less-than perfect GaAs materials, GaAs-on-Si [12] and GaAs-on-poly Ge [8]. Given the significant dependence of cell efficiency on the minority-carrier lifetime, we focused our efforts on improving minority-carrier lifetimes in GaAs thin-films on moly.

4.3.1 Minority-carrier lifetimes in GaAs thin-films on moly

The baseline DH structures on GaAs substrates for lifetime measurements was first established, as evident in the >1 μsec lifetime (**Figure 13**) in DH structures grown on GaAs substrates with low Se doping levels for the active region. The minority carrier lifetime in GaAs DH structure on moly was optimized at a certain Se-doping level. This is further discussed below. However, we note that the best lifetime for a GaAs DH thin-film on moly was ~0.41 nsec as seen in **Figure 14.**

An important understanding resulting from our development of high-efficiency GaAs solar cells on poly-Ge was that, most likely, there is an accumulation of Se-dopants at the grain boundaries, similar to a proposal on an earlier work at the grain boundaries can lead to n/n^+ minority-carriers for holes in n-GaAs. Thus we anticipated improved minority-carrier lifetime with increased Se-doping in poly-GaAs on moly. The dependence of minority carrier lifetime as a function of Se-doping level in GaAs grown on single-crystal GaAs substrates (i.e., no grain boundaries) and that of GaAs grown on moly are compared in **Figure 15**. While the lifetime falls continuously with increased Se-doping level in the case of single-crystal GaAs films, primarily due to the reduction in the radiative lifetime, the poly-GaAs films on moly show a significant increase in lifetime with Se-doping up to a certain level. The moderate increase in lifetime in these GaAs

films, in spite of the anticipated decrease in radiative lifetime, gives clear evidence for the Se-passivation of grain-boundaries.

In addition to Se-passivation of the grain boundaries, higher growth temperatures lead to improved lifetimes in GaAs thin-films on moly. The improvement in lifetime with higher growth temperature is thought to be due to a reduction of intra-grain dislocation densities. The effect of improved lifetimes with higher growth temperature was also evident in the higher J_{sc} levels obtained in GaAs solar cells on moly (**Figure 16**).

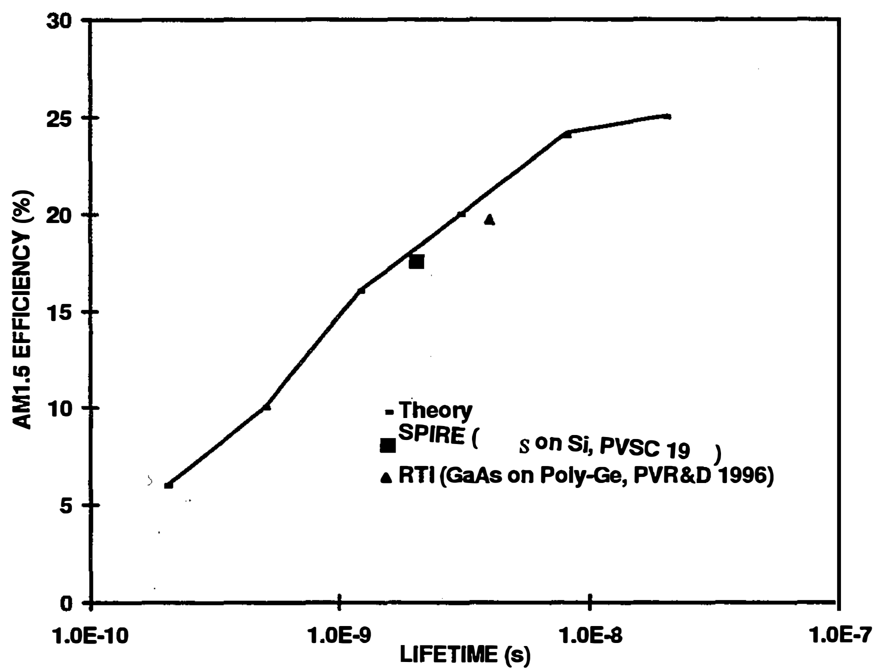


Figure 12. Dependence of GaAs solar cell efficiency on lifetime and some benchmark GaAs cell efficiencies on less-than-perfect substrates.

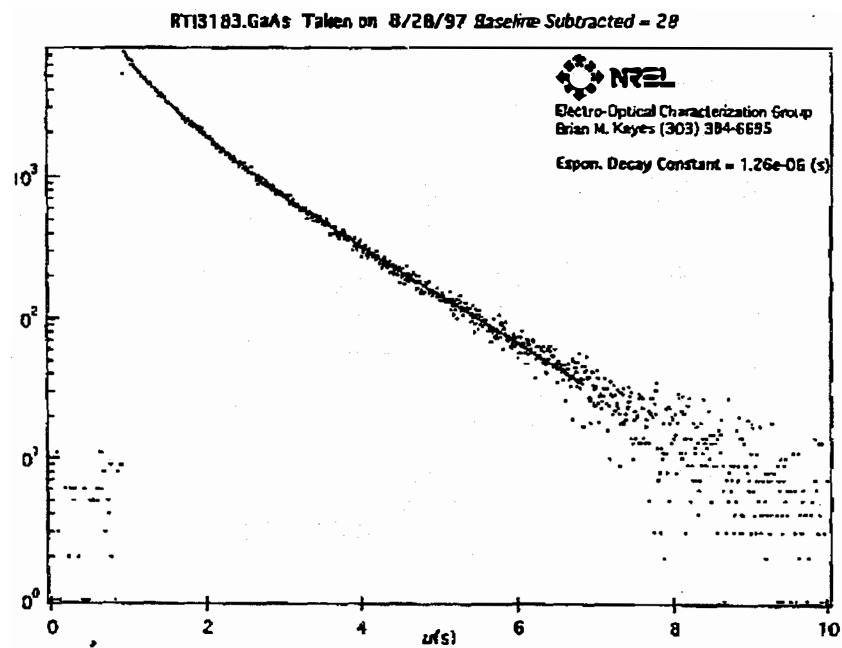


Figure 13. PL decay transient from a GaAs DH structure on GaAs substrate

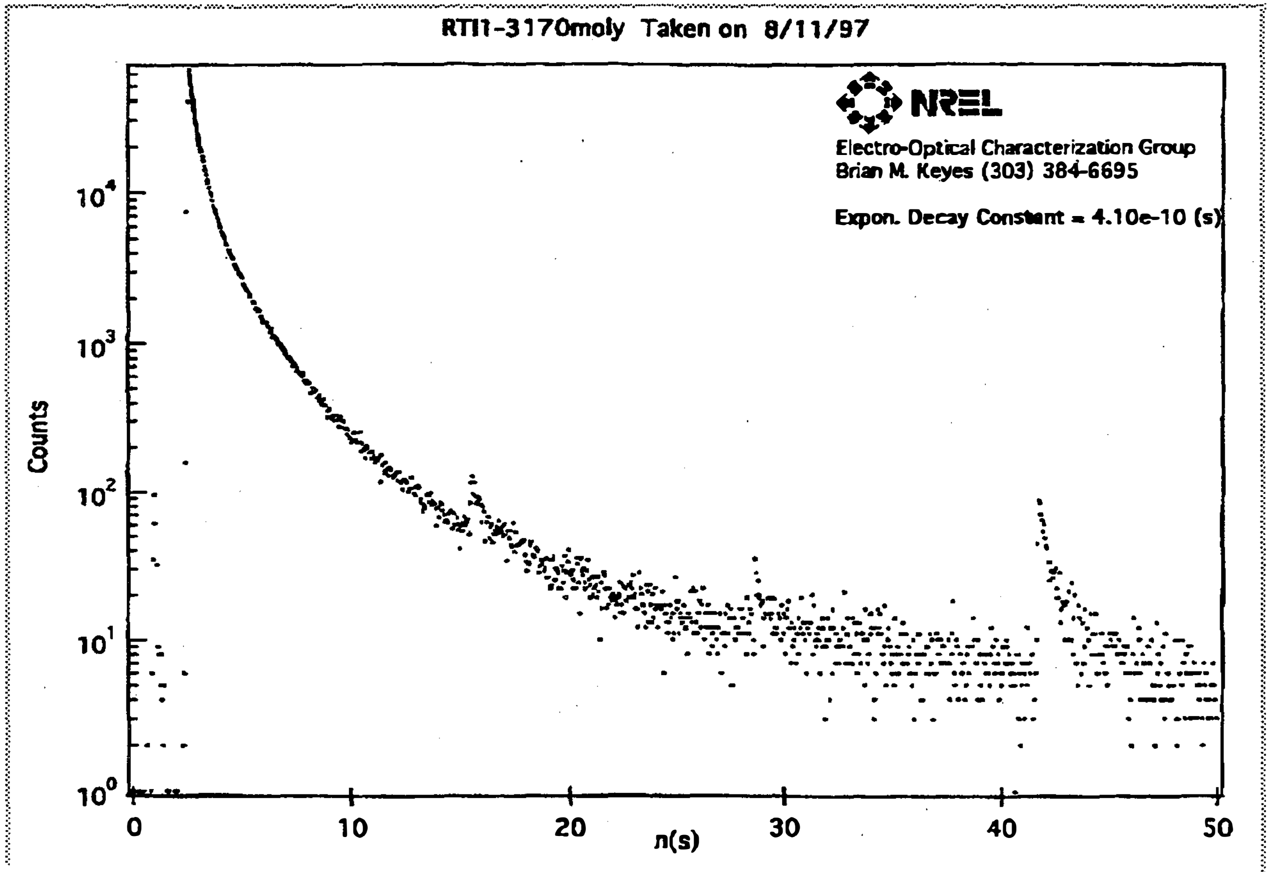
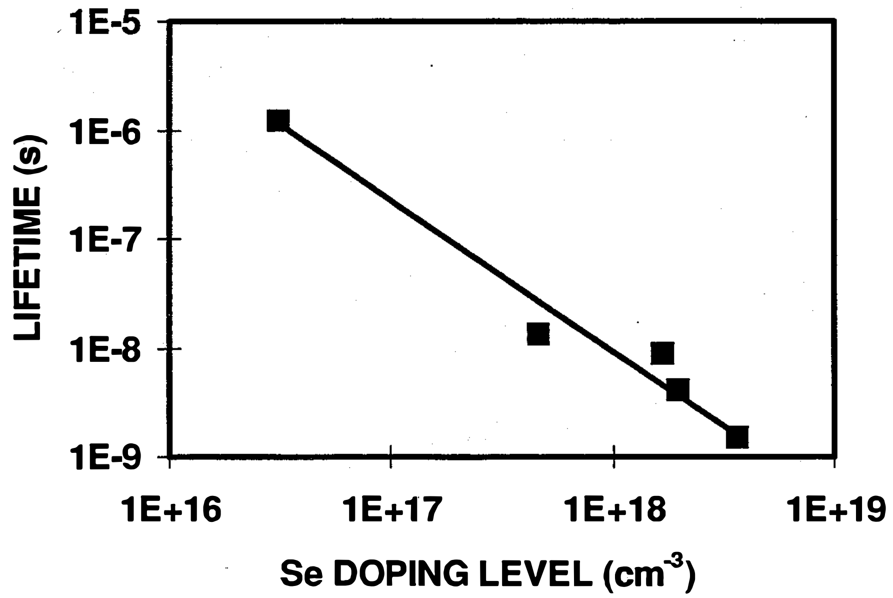


Figure 14 PL decay transient from a GaAs DH structure on moly



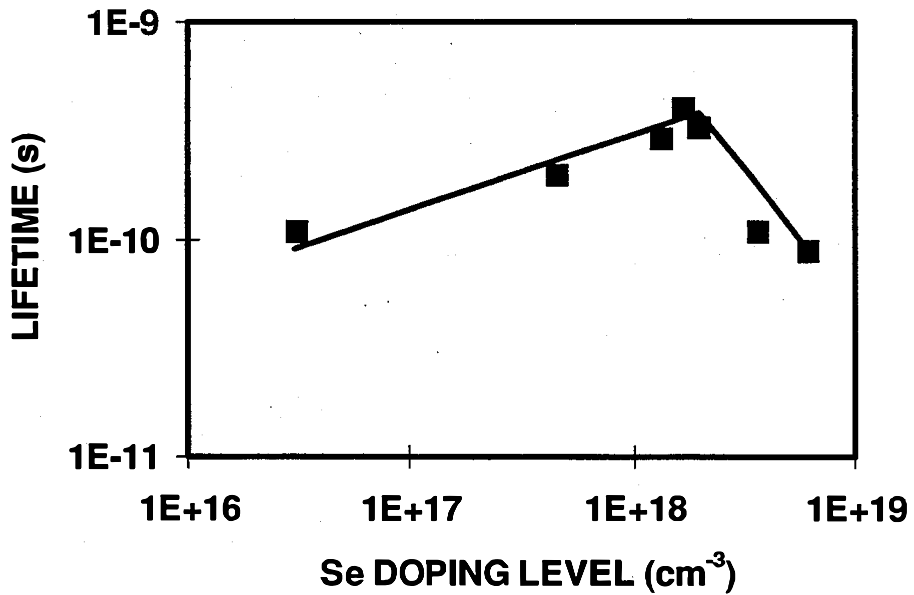


Figure 15. Dependence of lifetime on Se-doping level in GaAs films (a) on single-crystal GaAs substrates and (b) on moly foils.

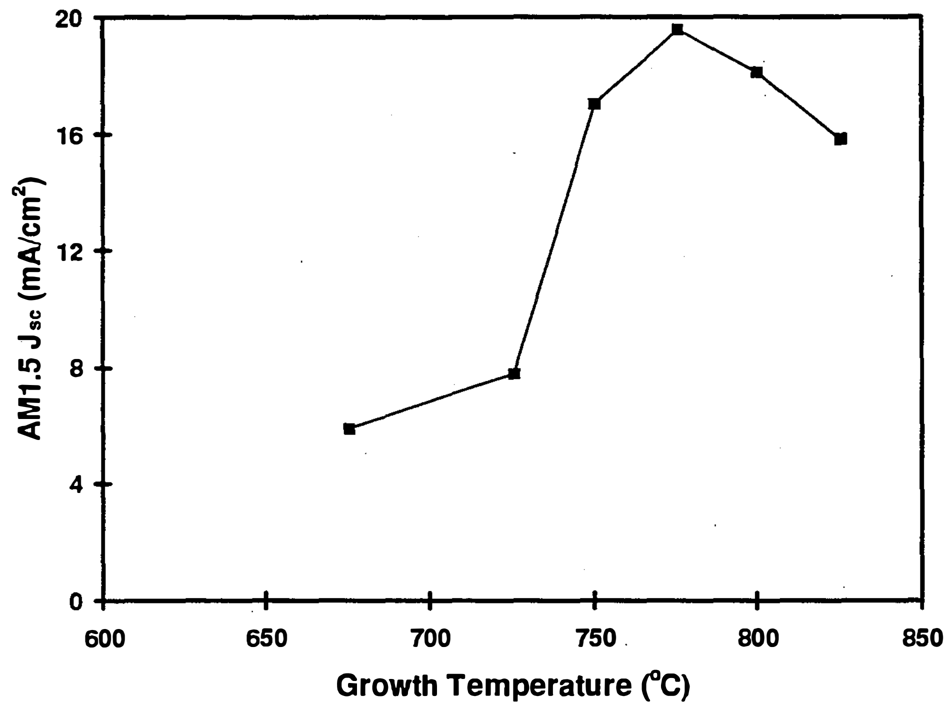


Figure 16. Dependence of J_{sc} on growth temperature in Se-passivated p^+-n GaAs solar cells on moly foils.

5.0 CONCLUSIONS

Development of GaAs solar cells on large-grain poly-Ge substrates appears to be a good first step towards the transitioning of these cells on to other low-cost substrates through an understanding and amelioration of the various loss mechanisms. Material and device issues related to the development of GaAs solar cells on poly-Ge substrates were addressed in this program. We have observed that substrate-polishing defects such as dents/ledges/steps are more detrimental than grain-boundaries on GaAs solar cell performance.

The undoped spacer at the depletion layer of the p^+-n junction has been shown to reduce the dark-current and improve the V_{oc}, fill-factor, and the efficiency of the cell on poly-Ge. The reduction in dark current and the improvement in cell V_{oc} with the spacer are believed to be associated with the reduction of tunneling currents near the depletion-layer of the p^+-n junction in polycrystalline materials. Device-structure optimization studies have led us to achieve an AM1.5 efficiency of ~20% for a 4-cm^2-area GaAs cell on sub-mm grain-size poly-Ge and an efficiency of ~21% for a 0.25-cm^2-area cell.

The successful demonstration of high-efficiency GaAs cells on sub-mm grain-size poly-Ge substrates motivated us to develop high-quality GaAs materials on lower-cost substrates such as glass and moly foils. To date, we have achieved a best minority-carrier lifetime of 0.41 nsec in an n-GaAs thin-film on moly. The role of Group-VI dopant in the possible passivation of grain-boundaries in poly-GaAs has been studied. Development of PV-quality GaAs material, with minority-carrier lifetime of 1 to 2 nsec, on low-cost moly foils can significantly impact both the terrestrial and space GaAs-based solar cells for PV applications.

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13. ABSTRACT *(Maximum 200 words)*
This report describes work performed by Research Triangle Institute (RTI) under this subcontract. The objective of this program was to further improve on the performance of GaAs solar cells on poly-Ge substrates. Material and device issues related to the development of GaAs solar cells on poly-Ge substrates were addressed. Key material physics issues include the use of Group-VI dopant, specifically Se, to passivate the grain boundaries in the n-GaAs base to achieve large J_{sc} values. Device-structure optimization studies led RTI researchers to achieve an AM1.5 efficiency of ~20% for a 4-cm^2 GaAs cell and an efficiency of ~21% for a 0.25-cm^2 cell on sub-mm grain-size poly-Ge substrates. Key device physics issues include understanding of the dark-current reduction mechanism with an undoped spacer at the p$^+$-n depletion layer. The successful demonstration of high-efficiency GaAs cells on sub-mm grain-size poly-Ge substrates motivated researchers to develop high-quality GaAs materials on lower-cost substrates such as glass and moly foils. They achieved a best minority-carrier lifetime of 0.41 ns in an n-GaAs thin-film on moly. The role of Group VI dopant in the possible passsivation of grain boundaries has been studied in GaAs films on moly foils.

14. SUBJECT TERMS
photovoltaics ; polycrystalline Ge ; high-efficiency GaAs solar cells ; poly-Ge substrates ; dark-current reduction mechanism ; low-cost substrates ; passivation

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