

SERI/STR-211-3190
DE87012270

July 1987

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Final Subcontract Report
16 February 1985 - 31 March 1987

R.H. Bube
A.L. Fahrenbruch
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Stanford University
Stanford, CA

Prepared under Subcontract No. XL-4-04022-1



SERI

Solar Energy Research Institute

A Division of Midwest Research Institute

1617 Cole Boulevard
Golden, Colorado 80401-3393

Operated for the
U.S. Department of Energy
under Contract No. DE-AC02-83CH10093

SERI/STR-211-3190
UC Category: 63
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Printed in the United States of America
Available from:
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Price: Microfiche A01
Printed Copy A04

Codes are used for pricing all publications. The code is determined by the number of pages in the publication. Information pertaining to the pricing codes can be found in the current issue of the following publications, which are generally available in most libraries: *Energy Research Abstracts (ERA)*; *Government Reports Announcements and Index (GRA and I)*; *Scientific and Technical Abstract Reports (STAR)*; and publication. NTIS-PR-360 available from NTIS at the above address.

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ABSTRACT

10/1/80 to 2/15/85

This research was begun in late 1980 to explore the method of hot wall vacuum evaporation [1] HWVE as a tool to grow CdTe films for photovoltaics, with particular emphasis on its promise to control doping and film structure and to enhance grain size. A versatile HWVE system was constructed, utilizing a four zone deposition chamber of quartz and high purity graphite, situated inside a bell jar vacuum system.

Films of CdTe were grown on BaF₂, 7059 glass, CdTe single crystal SX, and graphite substrates. Large grain epitaxy was obtained on SX substrates, whereas polycrystalline PX grain sizes of 1 to 10 μm were obtained on amorphous substrates. Co-evaporation doping of n-CdTe:In using elemental In was shown to be successful and well controlled [2]. Electronic measurements on these n-CdTe SX films yielded resistivities from 2 ohm-cm to $3 \times 10^4 \text{ ohm-cm}$ and carrier densities from 3×10^{15} to $1 \times 10^{17} \text{ cm}^{-3}$, depending on In source temperature from 375 to 510°C. A maximum in carrier density occurs at $\sim 510^\circ\text{C}$ and for higher In source temperatures the carrier density decreases slowly. At higher carrier densities and/or under illumination the mobilities for the epitaxial layers were essentially those of single crystal. PX films grown under similar conditions yielded minimum dark resistivities of $\sim 7 \times 10^4 \text{ ohm-cm}$ and maximum carrier densities of about $7 \times 10^{10} \text{ cm}^{-3}$, with the grains being totally depleted in the dark.

Attempts to dope CdTe p-type by co-evaporation were not as successful. Co-evaporation of As yielded essentially no change in electronic properties. Co-evaporation of Sb gave no change until Sb source temperature exceeded 419°C, at which point the resistivity plummeted from 10^7 to below 1 ohm-cm , probably because of the inclusion of metallic Sb.

The effect of diffusion doping, by coating the graphite with thin layers ($\sim 20 \text{ \AA}$) of Au or Cu before CdTe deposition was also investigated. Although high concentrations of Au or Cu in the film were determined by microprobe analysis, these CdTe films had lower hole densities than films grown on uncoated graphite. In addition the presense of Cu appeared to decrease the minority carrier diffusion length in the CdTe films.

It was found, however, that by increasing the substrate temperature, carrier densities in the 10^{15} to 10^{16} cm^{-3} range could be obtained without doping. (Similar substrate temperature effects on carrier density occur with p-CdTe films deposited by close-spaced vapor transport [3,4].)

A variety of solar cells have been fabricated using the CdTe layers deposited by HWVE. Epitaxial films of n-CdTe:In on p-CdTe single crystal produced homojunction cells with high V_{OC} , up to 0.8 V, but with modest efficiency because front surface recombination losses limited J_{SC} . All PX thin film cells in the n⁺-CdS:In/n-CdS/p-CdTe/graphite

configuration were fabricated using undoped CdTe and showed modest efficiencies ($n_s = 4-5\%$, $V_{oc} = 0.67$ V, and $J_{sc} = 16$ mA/cm² were typical maximum values). Heat treatment (HT) of these cells in air increases the cell series resistance and decreases the fill factor, whereas HT in H₂ produces the reverse effect. The hole density in the CdTe is not affected by such HT, suggesting that the observed effects are associated with the grain boundaries in the film [3,5].

The variation of photovoltaic properties of these cells was investigated as a function of CdS carrier density which was varied by changing the temperature for CdS deposition T_s . The V_{oc} , J_{sc} , and ff were found to depend on the relative carrier densities in the CdS ($n = N_D^+$) and in the CdTe ($p = N_A^-$) in a dramatic way. Values of V_{oc} , in particular, increased to 0.67 V for polycrystalline (PX) CdTe cells and to 0.8 V for cells based on single crystal (SX) CdTe when $N_D^+ = N_A^-$. This effect was shown not to be due to the annealing of the CdTe film during CdS deposition, nor to the diffusion of In from the outermost n⁺-CdS:In layer. An imperfection level lying 0.45 eV below the conduction band of the CdTe was identified by extrinsic spectral response measurements on the cells, and the junction transport of all cells could be modeled by recombination through this level in two parallel paths: (i) recombination/generation within the CdTe depletion region, and (ii) interface recombination with minority carriers at the CdS/CdTe metallurgical junction. A model based on these assumptions successfully describes the change in V_{oc} , as well as the J vs V characteristics in light and dark, as a function of the relative carrier densities of the CdS and CdTe [6,7].

Cells of the configuration contact/p-CdTe/n-CdS/n⁺-ITO/(7059 glass) ("inverted" structure) were also made; this stacking lends itself to testing of alternative contacts. Au, Cu:Au, and heat treated Cu contacts were tried, none of which gave any major decrease in series resistance R_s . Cu-colloidal graphite mixtures produced lower series resistance R_s but substantially lowered the photogenerated current and/or produced leaky junctions. The most promising candidate was a mixture of colloidal graphite and NaH₂PO₂ · H₂O (which decomposes to PH₃ and other compounds at about 250°C) in low concentrations. The entire cell is heat treated to diffuse the impurity, yielding R_s as low as 5 ohm-cm² and reasonably good solar cells ($n_s = 3-4\%$). Inverted cells, deposited at higher CdTe deposition and/or heat treated at higher temperatures, have homojunction-like behavior, but these can be converted to heterojunctions by application of the "Na-graphite" contact followed by heat treatment.

To gain insight into the complex electronic transport present in these polycrystalline cells, a significant amount of research was focused on grain boundary (GB) phenomena in bicrystals and in PX thin films and on the passivation of grain boundary activity [5]. Conductivity activation energy, GB diffusion potential, density of GB states, minority-carrier recombination velocity, the majority carrier capture coefficient, and the optical cross section of GB states were all evaluated. Passivation experiments indicate that HT in atomic H or Li provides an effective but temporary passivation in p-CdTe, and that similar effects are found for HT in air for n-CdTe.

A one dimensional computer model for grain boundary transport was formulated and successfully applied to n-CdTe epitaxial layers on CdTe SX and n-CdTe PX layers on graphite.

2/16/85 to 2/6/87

Since the previous work showed no clear path toward successful p-type doping of CdTe during deposition, post-deposition annealing of the films in various ambients was examined as a means of doping. Anneals were done in Te, Cd, P, and As vapors and in vacuum, air, and Ar, all of which showed large effects on R_s and the diode parameters. In the case of As, R_s values of In/p-CdTe/graphite structures were decreased strongly (e.g., from ~ 50 to ~ 5 ohm-cm²). This decrease was shown to be principally due to a decrease in grain boundary and/or back contact barrier height; thus the R_s decrease was due to large increases in mobility whereas the carrier density was not altered substantially. Although the R_s decreases were substantial, the diode characteristics became worse, and the R_s decreases were not observed when CdS/CdTe cells were fabricated on Te vapor annealed films.

A number of other research areas were explored in the later parts of the contract. Preparation of ZnO films by reactive evaporation yielded promising results: films of ZnO 0.4 μ m thick with a resistivity of 160 ohm-cm and high optical transmission were deposited on room temperature substrates using a ZnO source and an O₂ ambient. Deposition of p-ZnTe films by HWVE, using conventional techniques, yielded films of carrier density $2-3 \times 10^{15}$ cm⁻³ and resistivities of 200 to 5000 ohm-cm without intentional doping. Further analysis of PX grain boundary transport in p-CdTe films on alumina substrates, for both dark and illuminated cases, yielded good agreement with existing data.

INTRODUCTION

This Final Report is principally focused on research done after 2/16/85. Results of work done on this program before that time are summarized in the Abstract and discussed in detail in the previous Final Reports.*

General Description of the HWVE Method

By confining the evaporated species to an almost closed cell, the use of hot walls surrounding a region in which vacuum evaporation is taking place produces increases in the flux of species to the substrate to such a degree as to permit substantially higher substrate temperatures and growth much closer to thermal equilibrium [1]. The benefits are larger grain sizes, better crystalline structure, better epitaxy on single crystal substrates, and vastly increased utilization of material (in the 90 to 95% range) relative to conventional vacuum evaporation. In addition, it was hoped at the outset of this program that this procedure could lead to the feasibility of co-evaporation doping during vapor deposition and incorporation of p-type dopants into CdTe thin films.

Research Program

In the previous section of this research a HWVE system was constructed and tested. Various n-CdTe films, both epitaxial [on single crystal (SX) substrates] and polycrystalline (PX) [on amorphous substrates], were deposited, and control of co-evaporation doping with In up to carrier densities of 10^{17} cm^{-3} was established. Despite extensive work, we were not able to accomplish p-type doping using As, Na, Sb, Ag, Au, or Cu, however. In the case of As this was apparently because of lack of incorporation of As due to the high dissociation energy of As_4 and the relatively high vapor pressure of As at the substrate compared to that of CdTe. This led to the SERI sponsored research on ion-assisted doping in which we are currently engaged. (Incidentally, As ion doping is successful.) Despite the lack of success in extrinsic doping in HWVE, we found that moderately high carrier densities N_a could be obtained by simply increasing substrate temperature T_{sub} up to 560 to 600°C, giving $N_a = 10^{15}$ to 10^{18} cm^{-3} . Various types of CdS/CdTe solar cells of moderate efficiency were fabricated based on these p-CdTe films [3,7], although excessive series resistance R_s continued to be a problem.

Post-deposition annealing of p-CdTe/graphite samples in various ambients has been shown to produce large changes in the photovoltaic parameters. In particular Te vapor anneals produce a reduction of the through-the-film resistivity (including bulk and contact resistances) by factors of 10 to 200.

Several preliminary solar cells fabricated by putting CdS window layers on these Te-annealed CdTe films have been made but as yet a reduction in cell resistance has not been observed.

* Previous SERI Project and Final Reports and Letters (e.g., PR#8) are listed at the end of the reference page.

HWVE DEPOSITION PROCEDURE AND SAMPLE PREPARATION

The HWVE deposition system is shown in Fig. 1 and is described in detail in Progress Report #5.

Deposition parameters and measurements of film thickness and grain size are shown in Table I. The CdTe layers were grown on Poco DFP-3-2 high purity graphite sheets which had been previously cleaned using a sequence of DIH₂O, MeOH, acetone, and MeOH (all solvents are electronic grade) at room temperature using ultrasonic agitation. The source material was single crystal CdTe, grown at Stanford from 5 to 6 nines elements, and doped with P. Previous experience has shown that the P does not transport from the source crystal to actively dope the film.

All current growth runs were done at nominally the same source and substrate temperatures T_{sub} . It was desirable to use as high a T_{sub} as possible in order to minimize resistivity. Since there was some difficulty in nucleating the films on the substrates at these higher temperatures, the growth was split into two parts: (a) a four minute prerun at $T_{\text{sub}} = 518^{\circ}\text{C}$ to provide uniform nucleation and (b) a growth of 16 to 26 min at 580°C to increase the thickness and carrier density.

After the deposition was terminated by closing the shutter, the samples were withdrawn from the substrate furnace and allowed to cool by radiation in the vacuum. Most samples were halved or quartered as required experiments.

Similar times and temperatures used in the previous research yielded films with through-the-film resistivities of ~ 2000 ohm-cm and carrier densities of $2-5 \times 10^{15} \text{ cm}^{-3}$ (by $1/C^2$ vs V). The resistivities and carrier densities of the current series of films are generally a little higher and lower, respectively than those of the previous research but of comparable magnitude.

CdTe film thicknesses were measured using a Dektak.

ELECTRONIC CHARACTERIZATION METHODS

The electronic characterization of PX thin films is complicated by their columnar structure, with resultant anisotropic electronic properties, and by the presense of the substrate. Deposition on an insulating substrate with subsequent measurement of conductivity (using 4 point geometry) along the plane of the film (AtF) involves a transport path through many grain boundaries. In contrast, deposition on a conducting substrate and measurement of transport through the film plane (TtF) involves transport along the columnar grains which might pass through relatively few grain boundaries. The TtF method makes observations on the film in the same geometry as that for the final device, but involves some uncertainty of the ohmic quality of the contacts (since 4 point measurements can't be used).

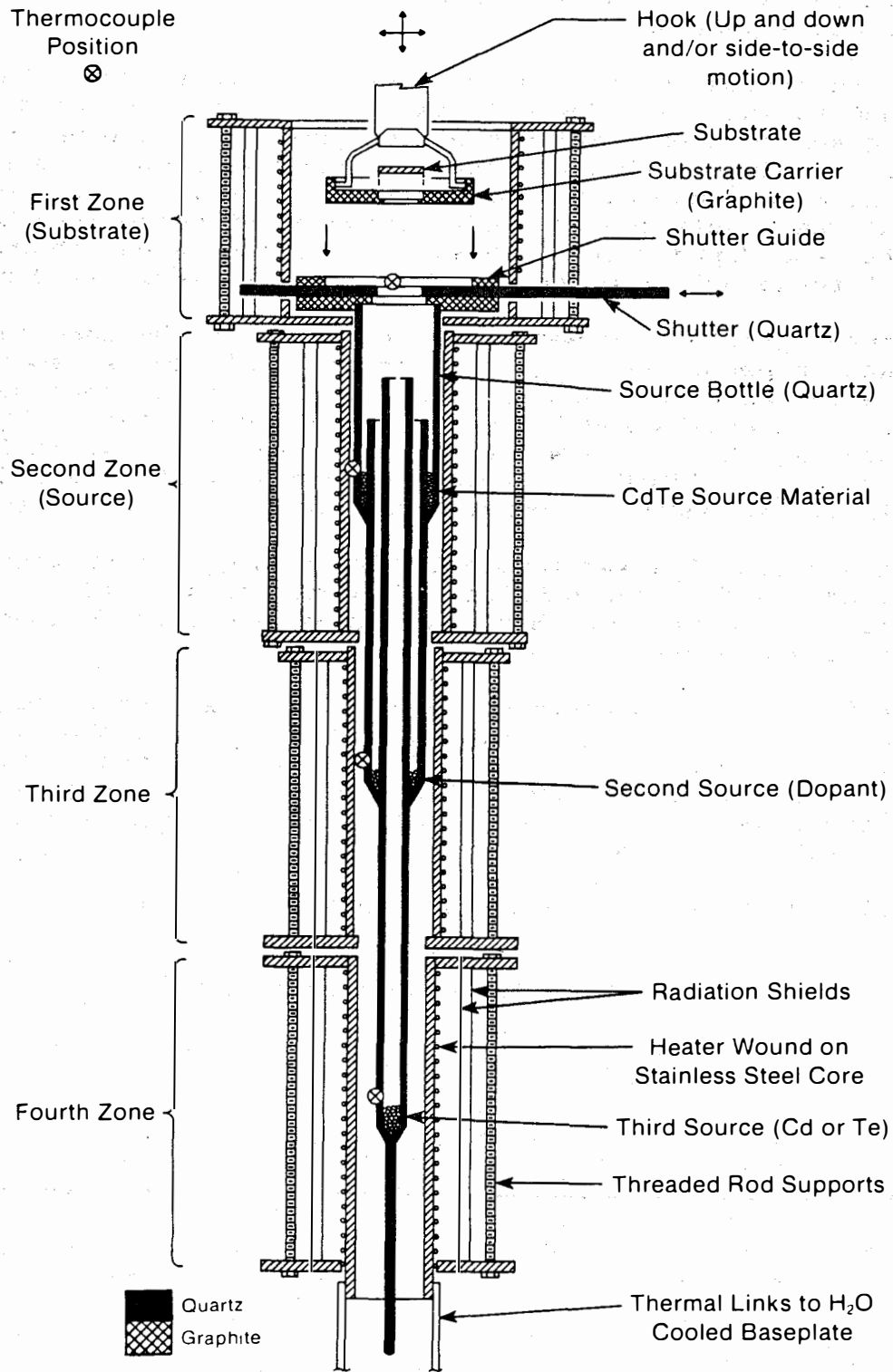


Fig. 1. Schematic diagram of hot-wall vacuum evaporation apparatus.

TABLE I. RECENT CdTe FILM DEPOSITIONS - GROWTH PARAMETERS

Sample No.	Growth Date	Source Boule	NUCLEATION			FINAL GROWTH		TOTAL Film Thickness (um)	Apparent Grain size (um)	Comments
			CdTe Temp (°C)	Substrate Temp. (°C)	Growth Time (min)	Substrate Temp. (°C)	Growth Time (min)			
UD-90 -90A*	10/15/84	T-59	646	528	4	583	16	20	6	12 Å Cu on graphite HT 5 1/2 hr at 510°C**
UD-91 -91L -91A	10/ 6/84	"	646	525	4	583	16	28 25	6	HT 7 1/2 hr at 510°C
KF-1-1 -1-1L -1A-1 -1A-1L -1A-2 -1A-2L	1/18/85	"	646	525	4	580	16	30	5	HT 6 hr at 500°C " "
KF-2	2/25/85	"	646	525	4	580	16	5	3	
KF-3 -3L -3A-2	2/ 1/85	"	646	525	4	580	16	11	2	HT 6 hr at 500°C
CK-1	2/13/85	"	646	518	4	580	16			
KF-4	3/ 6/85	"	646	518	4	580	12	30	10	
CK-2	3/ 5/85	"	646	518	4	580	16			
==== 3/11/85====System bake-out=====										
KF-5-1 -5-1L -5-3 -5-3L -5-4 -5-4L -5A	3/20/85	T-53	646	518	4	580	21	45	15	
	4/30/85							60	15	HT 7 hr at 510°C
KF-6-1 -1L -2 -2L -4 -4L -5 -5L	3/21/85	"	646	518	4	585	26	25	10	

* "A" indicates Te annealed sample.
"L" indicates measurement under illumination (~AM1.5).

** Heat treatments in Te vapor. Sample and Te at approximately the same temperature.

TABLE I. RECENT CdTe FILM DEPOSITIONS - GROWTH PARAMETERS (cont.)

Sample No.	Growth Date	Source Boule	NUCLEATION			FINAL GROWTH			Film Thickness (um)	Apparent Grain size (um)	Comments
			CdTe Temp (°C)	Substrate Temp. (°C)	Growth Time (min)	Substrate Temp. (°C)	Growth Time (min)				
CK-3	4/ 2/85	T-53	646	518	4	580	16	19.5	-	Post-dep. in situ anneal [Ⓐ]	
CK-4	4/10/85	"	646	518	4	580	16	59	-		
CK-5	4/16/85	"	646	518	4	580	16	46	-		
KF-7	4/ 4/85	"	646	518	4	580	16	85	20	Pre-dep. vac. bake-out [^]	
KF-8	4/ 8/85	"	646	518	4	580	16	35	20		
===== 4/20/85 ===== System bake-out =====											
KF-9	4/22/85	"	646	520	4	580	16	25	10		
-9L	(4/30/85) [#]									HT 7 hr at 510°C	
-9A											
-9AL											
KF-10	4/23/85	"	646	528	4	580	16	6	4		
CK-6a	4/23/85	"	646	518	4	580	16	40	-	Post-dep. in situ anneal	
-6b								62	-	Normal cooling	
CK/KF-7	4/30/85	"	646	518	4	580	16	63	-		
===== 5/17/85 ===== System bake-out =====											
KF-11	6/18/85	"	646	518	4	576	16	(30, estimated)			
KF-12	6/18/85	"	646	518	4	580	16	"			
KF-13	6/20/85	"	646	518	4	582	16	"			
KF-14	6/19/85	"	646	518	4	581	16	"			
KF-15	6/21/85	"	646	518	4	579	16	"			
===== 6/25/85 ===== System bake-out =====											
CK-8	6/25/85	"	646	518	1	none		~4 (non-uniform)			
===== 7/22/85 ===== System bake-out =====											
CK-9gr	7/23/85	"	646	518	2	none		10.5		Graphite substrate	
-9al								12.5		Alumina substrate	
===== 7/23/85 ===== System bake-out =====											
KF-16	7/26/85	"	646	518	4	?	16	(30, estimated)		New source bottle— single zone	
KF-17	7/27/85	"	646	518	4	580	16	"			
KF-18	7/27/85	"	646	518	4	584	16	"			
KF-19	7/31/85	"	646	518	4	582	16	"			
===== 8/2/85 ===== System bake-out =====											
CK-10gr	8/5/85	"	646	518	1/2	none		-		Graphite substrate	
-10al										Alumina substrate	
===== 8/5/85 ===== System bake-out =====											
KF-20	8/6/85	"	646	518	4	595 [§]	16	(30, estimated)		Substrate TC broken; temp. measured at substrate furnace (substrate at ~582°C)	
KF-21	8/7/85	"	646	518	4	595 [§]	16	"		"	
KF-22	8/7/85	"	646	518	4	595 [§]	16	"		"	
KF-23	8/8/85	"	646	518	4	595	16	"		"	
===== 8/14/85 ===== System bake-out =====											
KF-24	8/14/85	"	646	518	4	590	16	"		"	
KF-25	8/15/85	"	646	518	4	595	16	"		"	

* "A" indicates Te annealed sample.
 "L" indicates measurement under illumination (~AM1.5).
 # () Denotes measurement date.

** Heat treatments in Te vapor. Sample and Te at approximately the same temperature.
 Ⓐ Substrate pick-up was aborted and substrate could not be removed from substrate furnace until system was opened. Therefore it received an in situ bakeout in high vacuum while system was cooling from 580°C (~1-2 hr).
 ^ KF-7 graphite substrates were baked out in vacuum at 10⁻⁶ Torr for 6 min prior to growth.
 § Measured at substrate furnace liner.

Electronic measurements of the p-CdTe/graphite samples are complicated by the fact that the CdTe/graphite contact is only partially ohmic. We chose to use an In/p-CdTe Schottky barrier as one of the major diagnostic tools. J-V measurements gave the diode parameters and, at high forward bias, an upper bound on the through-the-film resistance for the complete device, and $1/C^2$ vs V measurements gave carrier density information.

Electronic measurement data on the samples are presented in Table II (an "A" following the sample number denotes an sample annealed in Te vapor).

The series resistance R_s of a diode structure is comprised of resistances of the bulk, the back contact (graphite), and the (small) spreading resistance in the In film. For PX CdTe the bulk resistivity is modified by (and in most cases dominated by) the presence of grain boundary potential barriers within the polycrystalline CdTe. In all cases the observed R_s was non-linear, showing the typical curvature associated with non-ohmic contacts and/or with current transport across grain boundaries. For this reason R_s was taken from the maximum slope of the forward I-V characteristic where it should be most dominated by the bulk resistivity. For the samples which had not been heat treated HT in Te vapor, R_s values ranged from 44 ohm-cm² to over 10⁴ ohm-cm².

The parallel resistance R_p of the diode structure, obtained from the reverse bias slope of the I-V characteristic, gives an indication of the existence of shorting paths through the CdTe film and thus is a measure of the presence of pinholes. Values of R_p were typically 0.3-8 x 10⁵ ohm-cm² for un-heat-treated samples and 0.8-3 x 10⁵ ohm-cm² for samples heat-treated in Te vapor. These values suggest reasonably pinhole free films and that Te HT does not produce pinholes. Optical examination at 500X also shows a dense film character.

The diode parameters J_0 and the diode quality factor A give an indication of the mode of current transport across the In/CdTe diode. In most cases the log J-V characteristics have two branches and can be modelled well using two values of J_0 (the zero-bias extrapolation of the log J-V plot), two values of the A factor, and the values of R_p and R_s obtained from the linear data plots. The J_0 and A values typically fall into two groups, one for un-heat-treated samples and one for heat-treated samples. The data groups for the latter samples are tighter, as shown in Fig. 2. Taken at face value these data indicate an increase in current transport for the In Schottky barriers on the HT samples. For the A=1 branch (Bethe transport) this represents a decrease in apparent barrier height (resulting from a change in interface state character) and/or an increase in tunneling through the barrier [8, p.162] (resulting perhaps from changes at the grain boundaries intersecting the junction). Less than extreme changes in the carrier density should have little or no effect on the magnitude of the forward-bias A = 1 current transport [8, p. 169]. For the A~2 branch the data represent an increase in recombination in the depletion layer. The magnitude of the A ~ 2 recombination current should vary approximately as $N_A^{-1/2}$.

TABLE II. RECENT CdTe FILM DEPOSITIONS: ELECTRONIC PARAMETERS

Sample No.	J-V CURVES				R_s^{\dagger} ohm-cm ²	ρ^{\dagger} ohm-cm	$N_A (1/C^2)^{\oplus}$ cm ⁻³	COMMENT
	$\frac{J_{01}z}{A/cm^2}$	A	$\frac{J_{02}z}{A/cm^2}$	A				
UD-90leaky diode.....				25	1×10^4	Not avail.	
-90A	...little rectification....				13	7×10^3	Not avail.	
UD-91	(2×10^{-7})	(2.5)	-	-	2×10^4	5×10^6	-	
-91L	-	-	-	-	5000	2×10^5	-	
-91A	9×10^{-8}	2.5	-	-	359	1×10^5	8×10^{14}	
KF-1-1	5×10^{-9}	1.5	-	-	1×10^4	5×10^6	-	
-1-1L	-	-	-	-	654	2×10^5	-	
-1A-1	(3×10^{-5})	(1.5)	-	-	118	4×10^4	-	Poor rectif.
-1A-1L	-	-	-	-	56	3×10^4	-	
-1A-2	(3×10^{-5})	(1.5)	-	-	135	5×10^4	-	Poor rectif.
-1A-2L	-	-	-	-	50	2×10^4	-	
KF-2bad sample, too thin.....							
KF-3	4×10^{-10}	1.6	-	-	6×10^4	5×10^7	Not avail.	
-3L	-	-	-	-	9000	8×10^6	-	
-3A-2little rectification....				308	3×10^5	-	
CK-1too resistive to measure ($< 10^9$ ohm-cm).....							
KF-4too resistive to measure.....							
CK-2too resistive to measure.....							
===== 3/11/85=====System bake-out=====								
KF-5-1	2×10^{-8}	2.2	4×10^{-12}	1.0	44	1×10^4	2×10^{14}	
-5-1L	-	-	-	-	28	6×10^3	-	
-5-3similar to 5-1.....				43	1×10^4	-	
-5-3L	-	-	-	-	26	6×10^3	-	
-5-4similar to 5-1.....				114	3×10^4	-	
-5-4L	-	-	-	-	50	1×10^4	-	
-5A	4×10^{-8}	2.0	4×10^{-10}	1.0	4	666	1.4×10^{14}	
KF-6-1	1×10^{-8}	2.0	(1×10^{-12})	(1)	654	3×10^5	4×10^{14}	
-1L	-	-	-	-	417	2×10^5	-	
-2similar to 6-1.....				654	3×10^5	-	
-2L	-	-	-	-	441	2×10^5	-	
-4similar to 6-1.....				736	3×10^5	-	
-4L	-	-	-	-	371	2×10^5	-	
-5similar to 6-1.....				314	1×10^5	-	
-5L	-	-	-	-	261	1×10^5	-	

[†] From maximum slope of J-V curve. [R_s (ohm-cm) = ρ (ohm-cm²)/thickness].
[⊕] Carrier density from high frequency capacitance (ca. 1 MHz).

TABLE I. RECENT CdTe FILM DEPOSITIONS: ELECTRONIC PARAMETERS (cont.)

Sample No.	J-V CURVES						N_A ($1/C^2$) [@] cm ⁻³	COMMENT
	J_{01} A/cm ²	A	J_{02} A/cm ²	A	R_s^+ ohm-cm ²	ρ^+ ohm-cm		
CK-3	6×10^{-9}	2.0	1×10^{-11}	1.0	68	3×10^4	7×10^{14} @ 2 MHz	
CK-4	-	-	(5×10^{-6})	(1)	2×10^4	3×10^6	NA	Poor rectif.
CK-5	-	-	(4×10^{-8})	(1)	~280	1×10^4	10×10^{14} @ 2 MHz	Poor rectif.
KF-7	2×10^{-10}	2.0	(1×10^{-14})	(1)	2200	3×10^5	0.3×10^{14}	Note 1
KF-8	9×10^{-9}	1.9	(8×10^{-12})	(1)	1240	4×10^5	$\sim 2 \times 10^{14}$	
===== 4/20/85 ===== System bake-out =====								
KF-9	3×10^{-9}	2.0	8×10^{-12}	1.0	57	2×10^4	8×10^{14}	
-9L	-	-	-	-	39	2×10^4	-	
-9A	4×10^{-8}	2.0	3×10^{-10}	1.0	6	2000	0.8×10^{14}	
-9AL	-	-	-	-	4.5	1500	-	
KF-10	8×10^{-9}	2.1	4×10^{-12}	1.0	200	3×10^5	10×10^{14}	
CK-6a	3×10^{-9}	1.7	-	-	1×10^4	3×10^6	1×10^{14} @ 2 MHz	
-6b	2×10^{-9}	1.7	-	-	1×10^4	2×10^6	2.5×10^{14}	"
CK/KF-7	5×10^{-9}	2.0	-	-	8000	1×10^6	3.6×10^{14}	"
===== 5/1/85 ===== System bake-out =====								
KF-11	3×10^{-9}	1.75	(1×10^{-12})	(1)	375	-	14×10^{14}	
KF-12leaky diodes.....				130	-	-	
KF-13	7×10^{-9}	1.75	(2×10^{-11})	(1)	300	-	-	
KF-14								
KF-15								
===== 6/26/85 ===== System bake-out =====								
CK-8leaky diode.....				280	7×10^5	-	
===== 7/22/85 ===== System bake-out =====								
CK-9gr								
-9al								
===== 7/23/85 ===== System bake-out =====								
KF-16								
KF-17								
KF-18								
KF-19								
===== 8/2/85 ===== System bake-out =====								
CK-10gr								
-10al								
===== 8/5/85 ===== System bake-out =====								
KF-20								
KF-21								
KF-22								
KF-23								
===== 8/14/85 ===== System bake-out =====								
KF-24leaky diodes.....				220	-	-	
KF-25".....				400	-	-	

⁺ From maximum slope of J-V curve. [R_s (ohm-cm) = ρ (ohm-cm²)/thickness].
[@] Carrier density from high frequency capacitance (ca. 1 MHz).

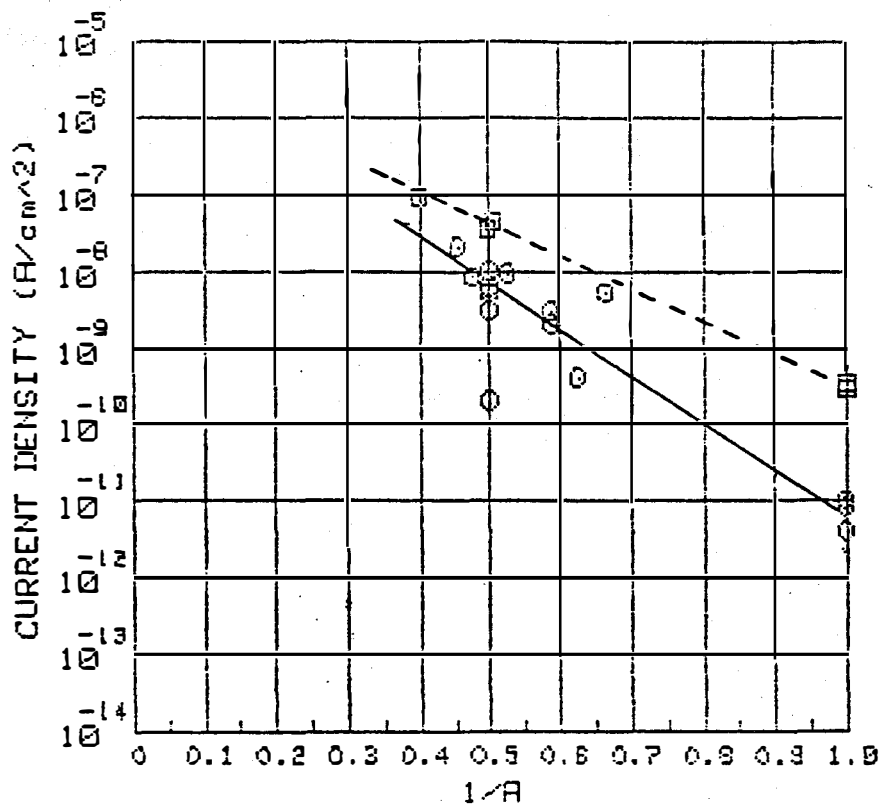


Fig. 2. Plot of $\log J$ versus $1/A$ for the In/p-CdTe diodes listed in Table II. A fit for the un-heat-treated (circles and solid line) and the heat-treated samples (boxes and dashed line) is shown. The plotting axes are primarily chosen here to display the data. [For possible further significance see ref. 8, p. 160].

One of the samples, deposited on a graphite substrate which had been annealed in vacuum at $\sim 700^{\circ}\text{C}$ before deposition of the CdTe, yielded a particularly low set of J_0 values. In this case the carrier density was very low and the depletion layer was wide enough to affect the current transport due to carrier mobility effects within the layer (the Schottky effect) [8, p. 169].

Capacitance-voltage measurements using In/CdTe were used to measure carrier density in the CdTe films and ac series resistance of the devices. In general, capacitance-voltage data taken at high frequencies (> 1 MHz) should yield an accurate value of the ionized shallow acceptor density at the edge of the depletion layer (equal to the free carrier density there) provided that the trap (deep acceptor) density within the depletion layer is small compared to the ionized shallow acceptor density at the depletion layer edge and that the series and parallel resistance of the device are within certain limits. As the probe frequency is decreased, the deeper centers can increasingly respond to the probe oscillation giving larger capacitance and a smaller depletion layer width. This gives a measure of the deep state density within the depletion layer where these levels intersect the Fermi level (but not at the depletion layer edge). In the current samples the deep state density is comparable to or larger than the shallow state density so care must be exercised in interpreting the C-V data. While precise carrier density information cannot be obtained without involved data analysis and additional measurements, the high frequency result is still a good approximation to the ionized shallow acceptor density and the low frequency result gives an estimate of the total acceptor density.

Detailed deep state evaluation in CdTe is beyond the scope of this project but is being investigated under a separate DOE program, and samples and information have been exchanged. Using this insight we are able to get reasonably accurate values of shallow acceptor density and broad estimates of deep trap density. Both quantities are important to device operation. Shallow acceptor density determines the bulk resistance in the quasineutral (QN) portions of the grains. The sum of the shallow acceptor density and the ionized portion of the deep acceptor density determine the barrier shape [e.g. ref. 9]. The barrier shape in turn determines the junction transport and the grain boundary barrier limited mobility which dominates the bulk resistance in most of these films [8, p. 369]. To obtain a rough estimate of these two quantities $1/C^2$ vs V data were taken at both high and low frequencies.

AMPOULE ANNEALING EXPERIMENTS

SUMMARY

Ampoule doping studies were undertaken to subject the films to much higher Te, Cd, and/or dopant pressures than is possible in the HWVE deposition chamber. In addition, diffusion doping during deposition was explored by evaporation of thin films of Cu on the substrate prior to CdTe deposition.

This work has shown that post-deposition annealing of p-CdTe/graphite samples in vacuum or Te vapor in quartz ampoules can reduce the through-the-film resistivity (including bulk and contact resistances) by factors of 10 to 200. This change is thought to be primarily due to an increase in carrier mobility due to a reduction in grain boundary and/or contact potential barrier height rather than an increase in carrier density. Unfortunately, this increase in conductivity is accompanied by a decrease in the V_{oc} of these cells. To explore these effects, the annealing process was studied in detail by including shorter annealing times, and both slow and rapid quenches following the anneals. In addition, the effects of other annealing ambients--vacuum, argon, air, and As vapor--were compared with the effects of Te vapor annealing.

Annealing times in vacuum as short as 30 min (with rapid quenching) appear to produce nearly the same resistivity and V_{oc} reductions as 7 hr anneals in Te vapor or vacuum. Annealing effects are strongly quenching rate dependent. When films annealed in vacuum are cooled slowly ($\sim 1^\circ\text{C}/\text{sec}$) rather than rapidly quenched ($\sim 50^\circ\text{C}/\text{sec}$), the through-the-film resistivity is unchanged or increased somewhat and the V_{oc} is decreased only slightly. Annealing in air increases the resistivity strongly. Annealing in Ar at roughly 100 Torr reduces the resistivity to an intermediate value but increases the V_{oc} .

Several solar cells were fabricated by putting CdS window layers on these annealed CdTe films.

ANNEALING STUDIES

Heat treatment (HT) in Te vapor was carried out as follows. The CdTe/graphite sample was sealed under vacuum in a quartz ampoule with a small piece of elemental Te. The ampoule was then heated to 510°C , typically, in a tube furnace which was carefully set up with a near-zero temperature gradient so that transport of Te and/or CdTe from one end of the tube to the other would be minimized. To end the HT, the Te end of the ampoule was withdrawn from the furnace first and spray quenched to eliminate the condensation of Te on the CdTe film. These samples were then compared to un-heat-treated companion samples from the same deposition run. HT in Cd vapor, Ar, and vacuum were done by similar techniques. Annealing in air was done without an ampoule.

The experimental results summarized in Table IV show that the un-heat-treated samples have carrier densities in the mid 10^{14} cm^{-3} range while the heat-treated samples have comparable or lower densities. Despite the lower carrier density of the heat-treated samples they have a substantially reduced series resistance. Apparently the major effect of the Te HT is to reduce the resistance of the grain boundaries and/or the semi-ohmic contact to the graphite. This hypothesis was explored briefly by altering the HT parameters.

At high frequencies the contacts, grain-boundary potential barriers, and semi-ohmic contacts are shunted by their capacitances, and the conductance approaches that of the QN regions of the device. The QNR resistance is calculated from the measured carrier density, an estimated single-crystal mobility ($50 \text{ cm}^2/\text{V}\text{-sec}$), and the layer thickness. This is compared with the high frequency resistance in Table III. Considering the complexity of the structure, the agreement is quite good and lends confidence to our measurement of carrier density.

In Fig. 3 are plotted the dc resistivity (from the J-V plot slopes) and high frequency ac resistivity data versus the carrier density. Using the theoretical constant mobility curves one can estimate an effective mobility for the CdTe layer. For the dc measurements this effective mobility includes the effects of the grain boundary potential barriers in impeding carrier flow. For the ac resistance measurements the effective mobility should be approximately the single crystal (or QNR) value. The following trends are evident:

- a) A number of the ac data and two of the dc data show effective mobilities near $40 \text{ cm}^2/\text{V}\text{-sec}$.
- b) All the ac data show effective mobilities above $5 \text{ cm}^2/\text{V}\text{-sec}$.
- c) HT of the films appears to increase the effective mobility strongly and, in all cases except one, the dc and ac after-heat-treatment mobility are quite close to each other.
- d) Some un-heat-treated layers show dc mobilities $< 0.04 \text{ cm}^2/\text{V}\text{-sec}$, indicating severe restriction of carrier transport by grain boundary potential barriers.

A major deposition factor influencing R_s appears to be the bake-out cleaning of the HWVE deposition chamber. The bake-out consists of heating the uncovered HWVE tube to 750°C and the substrate furnace to 650°C for 1 hr. This drives residual CdTe (which had condensed in the end of the source tube and on the graphite shutter holder parts) and impurities out of the tube. The CdTe condenses on an aluminum foil cap in the vacuum chamber and is removed from the system. For depositions done immediately after the bake-out the resistivity is lowest; with succeeding depositions the resistivity generally increases substantially. Bake-outs are now being done between every 2 to 3 depositions.

Heat treating samples in Te vapor at $500\text{--}510^\circ\text{C}$ decreases the resistivity by a factor of 10 to 200 in all cases studied. The decrease is larger for larger initial resistivities [e.g., control sample KF-5-1 ($44 \text{ ohm}\text{-cm}^2$) vs. HT sample KF-5A ($4 \text{ ohm}\text{-cm}^2$) compared with control sample KF-3 ($6 \times 10^4 \text{ ohm}\text{-cm}^2$) vs. HT sample KF-3A ($308 \text{ ohm}\text{-cm}^2$)].

TABLE IV. SUMMARY OF CAPACITANCE-VOLTAGE DATA

Sample	R _s [#] (ohm-cm ²)			Acceptor density (10 ¹⁴ cm ⁻³)		R _s from N _A [*] (ohm-cm ²)
	dc	Low f	High f	Low f	High f	
UD-91A	359	-	3	-	8	0.4
KF-5-1	44	20	5	3	2	2.8
-5A	4	23	7	1.5	1.4	6.2
KF-6-1	654	509	2.5	6	4	0.8
KF-7s [^] ..**	2200	1700	59 50	0.2	0.3 0.3	35 35
KF-8s [^] -8L [^]	1240 -	12 -	- 6	1 -	- 2	- 2
KF-9s	57	56	2.4	10	8	0.4
-9L		241	2.1	7	5	0.6
-9As	6	132	9.7	12	0.8	3.9
-9AL		406	132	2.6	0.4	8.4
KF-10s	200	-	0.9	-	10	0.1
CK-6a	1x10 ⁴	-	15	-	2	2.5
-6b	1x10 ⁴	-	8	-	3	2.6
CK/KF-7	8000	-	5	-	4	2.8
KF-11	375	-	13	-	14	0.3

These are resistance values measured (a) in dc from the maximum slope of the J-V curves, and by the capacitance bridge at (b) low frequency (ca. 200 KHz) and (c) high frequency (1-2 MHz).

* R_s calculated from the carrier density measured by high frequency 1/C² vs V, an assumed QNR mobility of 50 cm²/V-sec, and the sample thickness.

** Same sample 30 days later.

[^] "s" denotes small In area, "L" denotes In area about 4X larger.

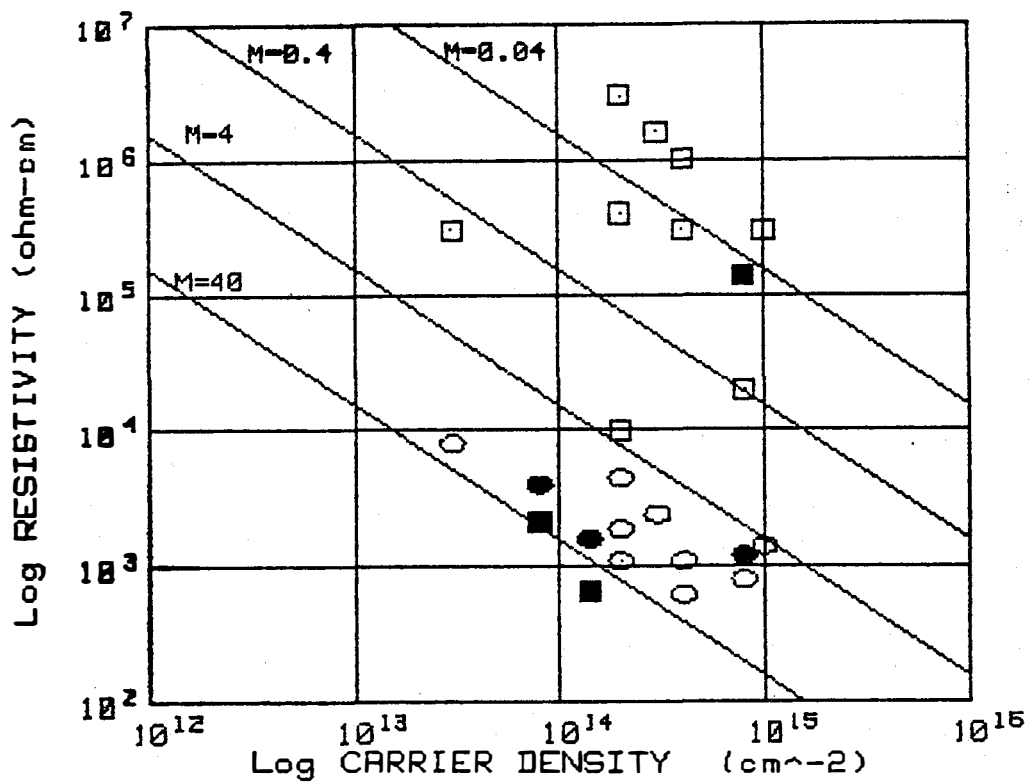


Fig. 3. Log resistivity versus log carrier density. Squares indicate dc data, ovals are ac data. Open symbols are un-heat-treated data and filled symbols show heat-treated data. Theoretical mobility lines for four mobilities from 0.04 to 40 cm²/V-sec are also shown.

FURTHER ANNEALING STUDIES

To gain further understanding of the electronic effects of ampoule annealing on the HWVE films the following questions were addressed:

1. the areal homogeneity of the CdTe films,
2. the effect of annealing time on the film properties,
3. the effect of cooling rate (after annealing) on film properties, and
4. the effects of various annealing ambients including vacuum, air, Ar, and As.

As much as possible, films from the same deposition were used for the comparisons. Experimental conditions and results for samples from the four deposition runs used (8, 26, 27, and 30) are shown in Table V.

The major diagnostic tool for these experiments has been the electronic characteristics of In Schottky diodes deposited by vacuum evaporation. In almost all cases two In dots (0.5 and 1 mm in diameter, large and small, denoted L and S) were put side-by-side on each sample to check for reproducibility. V_{OC} values were measured to give a rough estimate of the diode quality of the films. Note however that the photogenerated carrier collection is from outside the area of the In dot since the In is thick enough to be opaque. These V_{OC} values are expected to be roughly 50% of those for an n-CdS/p-CdTe device.

The log J vs V characteristics of several of the diodes are shown in Fig. 4 along with data for a similar In diode formed on a p-CdTe single crystal. The latter diode is a state-of-the-art device for our laboratory having: $J_{01} = 2.5 \times 10^{-9}$ A/cm² and $A_1 = 1.75$ for the recombination/generation transport mode and $J_{02} = 1 \times 10^{-11}$ A/cm², and $A_2 = 1.00$ for the thermionic mode with a calculated barrier height of 1.05 eV. Except for R_S , the characteristics of the best of the thin films diodes are very similar to the single crystal device.

Film homogeneity and reproducibility

Evaluation of the homogeneity of the films, made by comparison of adjacent In diodes, showed the variation to be reasonably small and considerably less than the variation from sample to sample. Samples 26-1 and 26-2, and 27-1 and 27-2 were chosen from two depositions (each with 6 films). The I-V characteristics of In dots deposited on the films without annealing were measured and found to be reasonably similar: the thicker films (~50 μ m), samples 26-1 and 26-2, had dc resistances of 600 to 1800 ohm-cm², ac resistances of 1.6 to 21 ohm-cm², and carrier densities of 3 to 6 $\times 10^{14}$ cm⁻³. For the thinner films, 27-1 and 27-2, the dc resistances were 97 to 325 ohm-cm², the ac resistances were 2 to 11.5 ohm-cm², and carrier densities were 5.7 to 10.1 $\times 10^{14}$ cm⁻³. Variations between dots on the same films (e.g., 26-1S and 26-1L) were considerably smaller than the variations between samples. These results are consistent with those for the majority of the un-annealed films previously reported.

TABLE 5. CdTe FILM AMPOULE ANNEALING STUDIES

Sample No.	Anneal min	Ambient	Quench*	J-V CURVES				V _{oc} V	R _{dc} - Ω-cm ²	R _{ac} - Ω-cm ²	N _A 10 ¹⁵ cm ⁻³	W _d μm	V _d V
				J _{o1} - A/cm ²	A ₁	J _{o2} - A/cm ²	A ₂						
8-1S	30	Air	Rapid	5x10 ⁻¹⁰	1.4	-	-	0.2	63000	3.5	0.45	3.0	3.9
8-1L	"	"	"	"	"	-	-	0.21	113000	5.8	0.27	4.1	4.2
8-2S	30	Air	Slow	8x10 ⁻¹¹	2.7	2x10 ⁻⁹	5.6	0.2	476000	7.3	0.32	4.2	5.5
8-2L	"	"	"	1x10 ⁻¹⁰	1.8	-	-	0.2	103000	4.3	0.51	3.0	4.5
26-1S	None	-	-	-	-	-	-	0.34	610	1.6	0.63	1.6	1.5
26-1L	"	"	"	-	-	-	-	0.27	670	21	0.41	1.9	1.4
26-2S	None	-	-	-	-	-	-	0.35	1900	4.0	0.34	2.6	2.3
26-2L	"	"	"	-	-	-	-	0.34	1200	8.9	0.49	1.9	1.8
26-3S	420	Te	Rapid	-	-	-	-	0.07	4700	99	0.007	28	5.2
26-3L	"	"	"	-	-	-	-	0.07	9000	121	0.024	35	28
26-4S	420	As+Te	Rapid	-	-	-	-	0.03	390	4.4	1.1	1.3	1.7
26-4L	"	"	"	-	-	-	-	0.04	450	5.4	1.3	1.3	2.1
27-1S	None	-	-	-	-	-	-	0.3	160	2.0	1.0	1.1	1.2
27-1L	"	"	"	-	-	-	-	0.3	96	11.5	0.74	1.3	1.3
27-2S	None	-	-	-	-	-	-	0.3	235	2.6	0.83	1.3	1.2
27-2L	"	"	"	-	-	-	-	0.3	325	7.2	0.57	1.6	1.3
27-3S	390	Vac*	Rapid	-	-	-	-	0.02	34	2.9	1.6	0.9	1.1
27-3L	"	"*	"	-	-	-	-	0.03	45	4.4	1.3	1.0	1.2
27-4S	390	Vac^	Rapid	-	-	-	-	0.09	33	3.5	1.5	1.0	1.4
27-4L	"	"^	"	2x10 ⁻⁸	2.3	-	-	0.03	36	3.8	1.2	1.1	1.4
27-5L	"	"	"	7x10 ⁻⁷	2.4	-	-	0.16	30	5.3	2.1	0.8	1.2
30-1B	None	-	-	2x10 ⁻⁹	1.9	-	-	0.38 0.35 ⁺	390 1960 ⁺	3	0.34	2.4	1.9
30-1L	"	-	-	2x10 ⁻⁹	1.9	-	-	0.38 0.34 ⁺	1200 3800 ⁺	4.6	0.2	3.5	2.4
30-2S	15	Vac	Rapid	9x10 ⁻⁸	1.8	8x10 ⁻⁷	3.7	0.2 0.2 ⁺	196 560 ⁺	0.86	1.9	1.1	2.2
30-2L	"	"	"	1x10 ⁻⁷	1.4	1x10	3.6	0.13 0.11 ⁺	174 500 ⁺	1.05	1.7	1.2	2.1
30-3S	30	Vac	Rapid	4x10 ⁻⁷	-	6x10 ⁻⁶	3.6	0.14 0.06 ⁺	32 280 ⁺	1.35	2	0.78	1.2
30-3L	"	"	"	7x10 ⁻⁸	1.8	6x10 ⁻⁷	3.0	0.17 0.11 ⁺	20 160 ⁺	1.9	1.65	0.87	1.2
30-4S	30	Vac	Slow	2x10 ⁻⁹	1.9	-	-	0.38 0.35 ⁺	2400 1727 ⁺	0.54	0.57	1.76	1.7
30-4L	"	"	"	1x10 ⁻⁸	2.3	-	-	0.325 0.3 ⁺	2400 1800 ⁺	1.05	0.58	1.77	1.8
30-5S	30	Argon	Rapid	2x10 ⁻⁹	1.9	-	-	0.43 0.4 ⁺	260 940 ⁺	2.3	0.25	2.5	1.5
30-5L	"	"	"	1x10 ⁻⁹	1.9	-	-	0.4 0.37 ⁺	300 1140 ⁺	2.8	0.17	3.4	1.9
30-6S	30	Argon	Slow	6x10 ⁻¹⁰	1.7	-	-	0.41 0.36 ⁺	225 950 ⁺	1.6 2.1	0.39 0.23	2.3	1.9
30-6L	"	"	"	1x10 ⁻⁹	1.8	-	-	0.4	578	4.0	0.16	3.4	1.7

* Quench rates:

slow = ~ 1 °C/sec, rapid = ~ 50-100 °C/sec.

* Without CdTe flakes in ampoule.

^ With CdTe flakes.

+ Measured after approximately 1 week of storage.

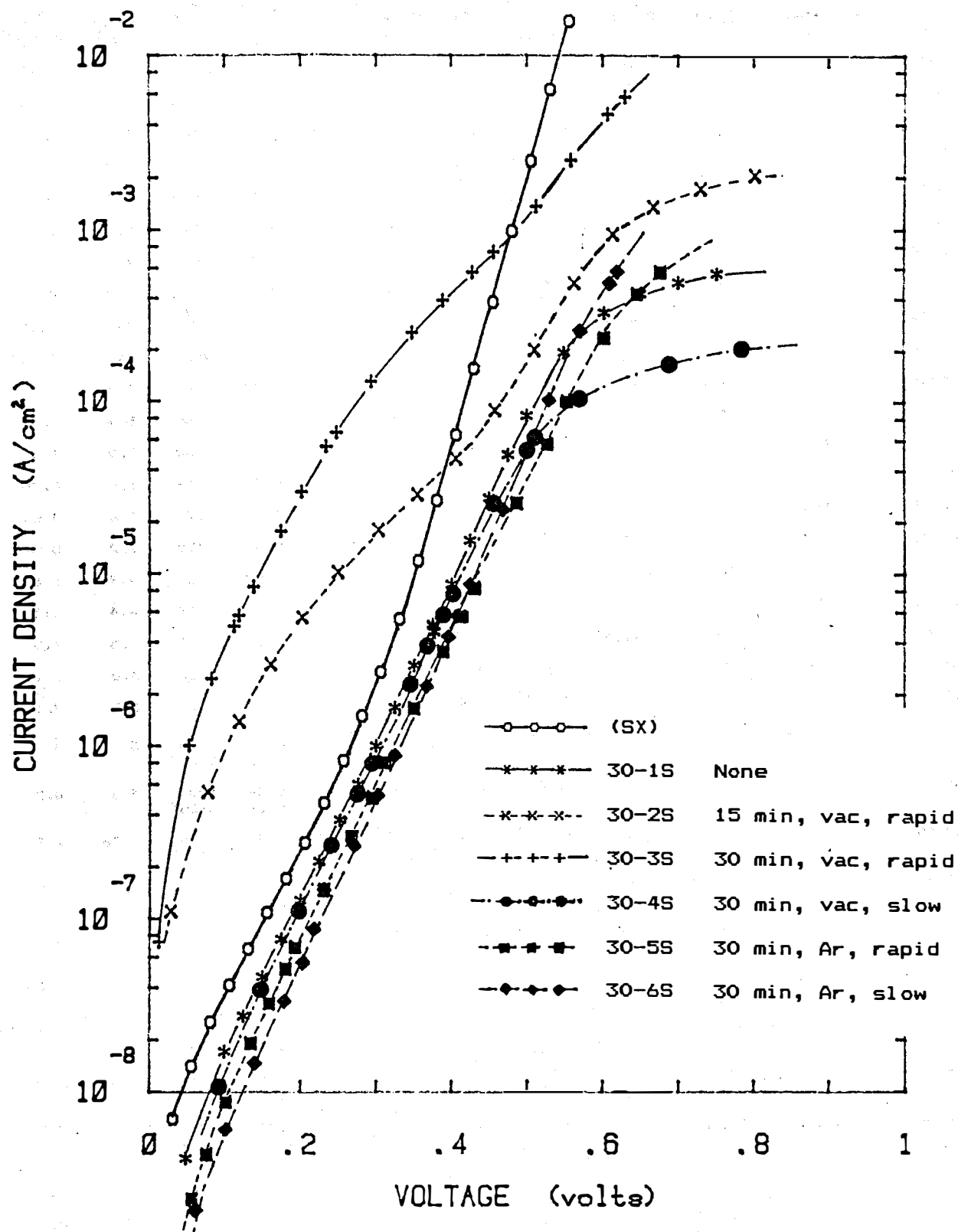


Figure 4. Dark, log J vs V characteristics of selected In/CdTe diodes. All are polycrystalline except for (SX) for which the CdTe is single crystal.

Annealing time

To better describe the effect of annealing time on properties, several samples were annealed in vacuum for considerably shorter times. Comparison of the properties of 30-1 (un-annealed), 30-2 (15 min) and 30-3 (30 min) with 27-4 (6.5 hr) shows that the largest part of the effect of annealing has been accomplished in 15 min and after 30 min the properties are quite similar to those existing after 7 hrs.

Quenching rate

For the earlier annealing experiments the ampoules have been withdrawn rather quickly from the hot zone of the furnace, CdTe film end last. As the ampoule was pulled out of the furnace it was rapidly quenched by spraying methanol on it. An estimated cooling rate for this process is about 20 to 50°C/sec at high temperatures. This may be compared with the cooling rate for film deposition which is about 1°C/sec, estimated from the radiation law with an emissivity of 0.9 in a vacuum. In order to find what if any influence quenching rate had on the annealing process, several samples were slow cooled by withdrawing them slowly from the furnace, giving a cooling rate of about 1°C/sec. For the vacuum ambient the slow cooling essentially eliminated the effect of the annealing and the resulting film properties were almost the same as those for un-annealed samples (compare samples 30-3 and 30-4). For air and Ar anneals (see below) there is little difference between the results obtained by rapid and by slow quenching.

Ambient

Early experiments were with films that had been annealed in either Te vapor or vacuum ($\sim 10^{-6}$ Torr) and there was some concern about possible loss of CdTe from the film to other positions in the ampoule during annealing. This was evidenced in some cases by a decrease in film thickness of, for example, a loss of ~ 2 μm from a film initially 26 μm thick (#6). This loss was controlled by a) maintaining a level temperature profile during annealing, b) monitoring deposits inside the ampoule, and c) putting a small amount of CdTe flakes near the film in the ampoule. The latter means was tested using 27-3 and 27-4, for which there was little difference in resistance or carrier density between "with-flakes" and "without-flakes" samples.

Perhaps more important were differences for annealings in various ambients. From these data there appears to be little consistent qualitative difference between annealing in vacuum and in Te vapor (e.g., compare 91A, 1A, 5A, and 9A from the previous report with 30-3) provided that quenching is rapid. The resistivity values are quite comparable and the carrier density obtained by vacuum anneal appears to be 2-3 times higher than for the Te anneal.*

Four additional ambients: air, Ar, As, and P, were also evaluated. Annealing in air (samples 8-1 and 8-2) produced moderate decreases in V_{oc} but increased R_s almost two orders of magnitude, independent of quenching rate. This result can be compared with the findings of T. Thorpe who found small increases of along-the-film resistance for polycrystalline CdTe on insulating substrates [Progress Reports #11, p. 18, and #13, p. 10, and ref. 5] on annealing in air. Thorpe's films had

considerably higher before-annealing resistivity (before anneal: 2×10^6 ohm-cm, after anneal: 3.5×10^6 ohm-cm) but a somewhat larger carrier density (before anneal: 10^{15} cm⁻³, after anneal 2×10^{16} cm⁻³).

Annealing in an inert atmosphere, Ar (samples 30-5 and 30-6), produced a more satisfying result. The ampoules were first evacuated to $\sim 10^{-6}$ Torr and then back-filled with about 0.1 atm of Ar bled in through a "Oxiclear"TM purifier which removed O₂ and H₂O to ppm levels. Annealing in Ar had the effect of producing small increases in V_{OC} while reducing R_S considerably. These effects were independent of quenching rate. To complete our picture of the effects of Ar annealing, anneals of 60 min were done with both rapid and slow quenching. The values of dc resistance R_{DC} and carrier density p were essentially the same as for the 30 min anneals, but the V_{OC} values for the In diodes were decreased by 30 to 60 mV. This suggests that the effects of the Ar anneal arise from a complex interplay of at least two different mechanisms--one fast, responsible for decreasing R_S, and the other slow, decreasing V_{OC}.

Annealing in As vapor (with Te also present) reduced the V_{OC} strongly to 0.025-0.04 V and only moderately reduced the R_S.

Annealing in an ampoule with a small amount of Cd₃P₂ present (sample 26-5) causes the CdTe film to flake off of the graphite substrate. This result was confirmed with a second sample.

Initial experiments on anneals in P vapor were done in the usual way by encapsulating a PX film sample and a small amount of elemental red P in a quartz ampoule, sealing it off under $\sim 10^{-6}$ Torr vacuum, and then annealing. About 2 mg of P was used, (0.74 times the weight of the CdTe film), enough to produce a P₄ pressure of about 4 atm. After annealing, clear, amorphous deposits appeared on the P end of the tube which turned yellow after some time. On opening the tube and exposure to air these produced smoke; the deposits were yellow P. The central portion of the tube had no deposits. Before opening the tube several shiny, colored deposits were visible on the CdTe film, much like the glaze on pottery. These deposits remained after the tube was opened, were not soluble in H₂O or methanol, and were not removed by a short anneal at 500°C in H₂. The deposits were partially dissolved in NH₄OH, but evidence of a reaction of the deposit with the CdTe film was still visible. The deposits might be (a) Cd₃P₂ or P₂Te₃, (b) phosphates or phosphites of Cd, or (c) unlisted ternary compounds of Cd, Te, and P. The first two compounds are possible candidates (they decompose on contact with moist air but P₂Te₃, at least, is reported to be insoluble in H₂O or alcohol). The phosphates and phosphites seem unlikely because the presence of yellow P in the tube during and after the annealing would preclude the presence of oxygen.

* Samples 26-3S and -3L are atypical.

To evaluate the effect of diffusion doping during deposition, a 10 Å film of Cu was deposited on the graphite substrate by vacuum evaporation prior to CdTe growth. Microprobe analysis confirmed the presence of Cu in the film. Comparison of samples with and without Cu suggests that Cu gives a considerably smaller through-the-film resistivity but that the presence of Cu is detrimental to the diode characteristics. Indium diodes made on the Cu containing material were leaky, showing large reverse bias current and little rectification. Annealing in Te vapor reduces the resistivity somewhat but the In diodes then show even smaller rectification ratios.

DISCUSSION

Because of the rapid nature of the changes occurring on annealing in various ambients, it appears most likely that the changes in resistivity of the films are due to changes occurring at the grain boundaries, rather than in the bulk of the grains. Diffusion of impurities into the bulk of the grains at these low temperatures and times as short as 15 min would appear to be unlikely.* Probably the most compelling evidence for the grain boundary hypothesis is the low ac resistivity of all the films and the relatively high carrier density despite the high resistivity of the air-annealed films. It does appear that anneals which might remove oxygen from the grain boundaries (vacuum, Te vapor, As vapor, and, to a lesser extent, Ar) cause decreases in resistance whereas the air anneal causes increases in resistance.

Most of the data indicate that V_{oc} decreases strongly as R_s is decreased by the various annealings. The Ar anneal is an exception to this with V_{oc} increasing a few tens of millivolts and R_s decreasing by an order of magnitude relative to the un-annealed sample. The Ar pressure may inhibit the release of oxygen by the grain boundaries because the Ar is at much higher pressure (0.1 atm) when gas transport is by diffusion. However, the partial pressure of oxygen in the Ar is low, comparable to that in vacuum. The question remains: why then does V_{oc} increase during the Ar anneal?

SOLAR CELLS MADE ON Te-ANNEALED CdTe

It is of course crucial to find out whether the decreases in film resistance obtained by Te annealing can be used to advantage in solar cells made from these materials. Test structures for evaluation of CdS/CdTe solar cells utilizing Te-annealed p-CdTe are shown in Fig. 3. To satisfy SERI requirements for deliverables full size $1.2 \times 1.2 \text{ cm}^2$ graphite substrates were coated with 1 cm^2 of p-CdTe by the standard technique. Samples were then either annealed or not, without cleaning. Then CdS was evaporated on about 3/4 of the p-CdTe area by conventional techniques in two layers, again without cleaning the CdTe. Usually about 24 hours of air exposure occurred between processing steps. After

* However chemical diffusion of vacancies in CdTe has been reported to be very rapid [$1.3 \times 10^{-7} \text{ cm}^2/\text{sec}$ at 500°C , extrapolated from the data in K. Zanio, Semiconductors and Semimetals (R.K. Willardson and A.C. Beer, eds.), Vol. 13, "Cadmium Telluride." Academic Press, NY (1978), p. 124].

-CdS deposition, an In grid covering about 4% of the CdS area was applied. Next, four In dots, with area ratios spanning a factor of ten, were applied directly to the remaining 1/4 area of p-CdTe to evaluate its carrier density. Unfortunately the use of full size substrates precluded the use of direct comparison control samples. The samples are KF-11, 12A, 13, 24A, and 25A. Through-the-film resistivity measured for the CdS/CdTe diode and for all the In/CdTe diodes for each substrate were almost the same. This shows that the In diode is a reliable indicator of the through-the-film resistivity for the CdS/CdTe case as well. This resistivity was approximately the same for all the films, whether annealed or not, and was somewhat higher than the best un-annealed samples (such as KF-5). Since the series resistance of these cells would severely reduce the solar efficiency (probably to less than 3%), no efficiency measurements were done.

These particular Te heat treatments did not succeed in reducing the resistivities of the fabricated CdS/CdTe devices. It is likely that the vacuum anneal at 160°C for about 30 minutes during CdS deposition and subsequent slow cooling in vacuum reversed the effect of the Te anneal. On the other hand, the poor diode performance of the annealed samples suggests that these samples are atypical and that there may be an uncontrolled variable in the annealing procedure (e.g., KF-1A showed poor diode characteristics for some unknown reason, while the diode characteristics of KF-5A and KF-9A were excellent)

Cells KF-11, 12A, 13, and 24A were sent to SERI as deliverables.

CONCLUSIONS

1. Annealing effects observed for $T = 500^{\circ}\text{C}$ are quite rapid with the greater part of the changes occurring in 15 to 30 min. This, and the low ac conductivity of the films suggest that most of the changes are occurring at the grain boundaries rather than in the bulk of the crystallites. Thus mobility increases dramatically for vacuum and Te anneals while the carrier density remains constant or decreases.
2. Vacuum and Te vapor anneals decrease the resistivity but also decrease the V_{oc} of In/p-CdTe diodes. The presence of Te vapor appears not to have a large effect on the film properties.
3. Air annealing substantially increases R_s and decreases V_{oc} .
4. Annealing in elemental As vapor sharply reduces the V_{oc} while reducing the R_s only moderately.
5. Annealing in Ar increases the V_{oc} while decreasing R_s .
6. Quenching rate has a strong effect on the properties of the vacuum annealed films but little or no effect on films annealed in Ar or air.
7. The decreases in series resistance after annealing, observed to be stable with the In/CdTe devices, are apparently lost during the fabrication of CdS/CdTe devices and the latter devices do not show a decreased series resistance when prepared on Te-annealed CdTe substrates.

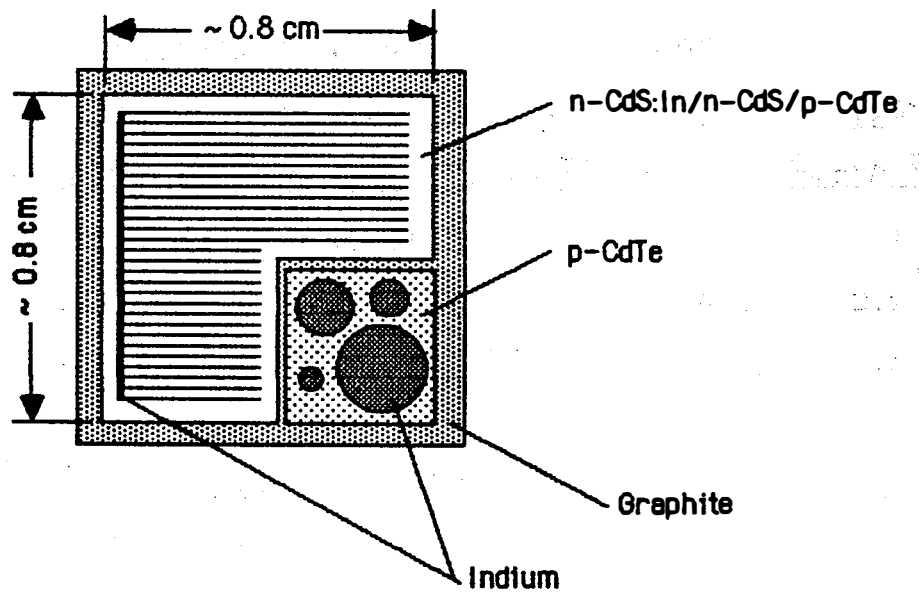


Fig. 5. Solar cell test structure. The area of the n^+ -CdS:In/n-CdS/p-CdTe cell portion is defined by scribing its edges. In/p-CdTe test diodes are deposited on a portion of the p-CdTe masked off during the CdS deposition.

PHOTOVOLTAIC DEVICES

Four photovoltaic cells, of the type $n^+-CdS:In/n-CdS:undoped/graphite$ were made using CdTe films KF-31 through 34. All the CdTe films were prepared in the same way and were about 40 μm thick.

The cell properties are listed in Table VI. All four cells had large series resistance R_s , at least partially because of the thick CdTe layer. Plots of $\log J_{sc}$ vs \log photon flux revealed that R_s was large enough to reduce the J_{sc} and that the true light generated current was approximately 15 mA/cm^2 . Cell PS-4 had a rather small shunt resistance R_p initially. Several potential shorts were found with optical microscopy (200x) which appeared to be voids in the CdTe layer. One of the potential shorts lay on a center line of PS-4 and so the cell was divided into two halves (PS-4-1 and PS-4-2). This caused the R_p to increase by a factor of 3.

For PS-3 and PS-4 the V_{oc} values were respectable, 0.668 and 0.681 V, the dark and light J vs V curves were similar, and superposition held approximately.

TABLE VI. PHOTOVOLTAIC DEVICES

Sample	J_{o1} $10^{-9} A/cm^2$	A_1	J_{o2} $10^{-13} A/cm^2$	A_2	R_s $\Omega-cm^2$	R_p $10^6 \Omega-cm^2$	J_{sc} mA/cm^2	V_{oc} V
PS-3	1	1.8	(2)	(1.0)	940	1.5	--	--
	2.5	1.8			--	--	7.84	0.67
PS-4A	(3)	(1.8)			3800	0.09	--	--
					--	--	9.74	0.68
PS-4-1					1240			
					--	--	5.62	0.65
PS-4-2	0.8	1.8	(2)	(1.0)	500	0.4	--	--
	2.5	1.8	(0.4)	(1.0)	--	--	9.4	0.67

() Indicates values are sufficient (but not necessary) to satisfy curve fitting of data.

PS-4-1 and PS-4-2 are two halves cut from PS-4.

ZnO DEPOSITIONS

In the literature four methods of deposition of ZnO are discussed: reactive sputtering of Zn in O₂, chemical vapor transport using H₂ mixtures as transport gases, spray pyrolysis of H₂O solutions of zinc acetate or nitrate, and in situ oxidation of a previously deposited Zn film. The latter three of these methods have the disadvantage that high substrate temperatures are required, ca. 400–500°C. The first method, sputtering, can alter the interface properties by ion impact damage. A fifth method, little discussed in the literature, is reactive evaporation, which has the advantage of low substrate temperatures and immediate control of carrier density by O₂ pressure.

For our initial trials the compound ZnO was evaporated from an alumina coated W boat source. The region between the source and the substrate was enclosed by a cylindrical quartz shield to help contain the unused flux. The substrate heater was not used but both the substrate and the quartz cylinder were heated by radiation during the deposition; the maximum substrate temperature is estimated at not over 150°C. The first run, without O₂ input to the bell jar, was a relatively brief deposition which yielded no visible film on the substrate but a black layer on the quartz cylinder. The second run, with 2×10^{-5} Torr of O₂ maintained at the ion gauge position, was of about 20 min duration and yielded a transparent ZnO film with a thickness of about 0.5 μm (measured by a quartz crystal thickness monitor) and a 4 point resistivity of 1700 ohm-cm. During this run the portion of the black film on the inside of the quartz cylinder adjacent to the source became transparent. This film was visibly much thicker than that on the substrate. Resistivity measurements using two point contacts were taken at various positions along the axis of the cylinder giving resistances varying from 50K ohms to 13 ohms that suggest a transition along the tube from ZnO to almost metallic Zn. A third run using two increments of 20 min each, but with no external O₂ supply yielded a transparent film about 0.4 μm thick and with a resistivity of 160 ohm-cm. (The size of the ZnO source limited the duration of the deposition).

By controlling the relative magnitudes of the fluxes of Zn and O₂ we should be able to control the stoichiometry of the ZnO and hence the resistivity. ZnO is a defect semiconductor with the carrier density determined by O vacancies. The geometry of the deposition setup is one of the factors that influences the fluxes at the substrate position. In the experiment above, the direct, line-of-sight fluxes of Zn and $\frac{1}{2}\text{O}_2$ from the source to the substrate are probably about equal. Fluxes of Zn to the cylinder are mostly condensed (except in positions where it is hot), while the O₂ flux is mostly reflected. The reflected O₂ flux adds to the direct flux at the substrate giving an excess of O₂ at the substrate and producing a rather high resistivity film. The absolute magnitudes of the fluxes are also important; at higher fluxes and/or lower substrate temperatures the formation of ZnO is controlled by the reaction rate at the substrate surface and, if the substrate is cool, O₂ escapes from the surface preferentially because of its higher vapor pressure and the resulting film is Zn rich. At lower fluxes and/or

higher substrate temperatures the formation is controlled to a greater degree by the arrival rates and the film can be more stoichiometric. This is why the film on the cylinder tends to be black (Zn rich) in its cool regions, while a transparent film (more stoichiometric) is formed on the substrate which is farther away and on the closer portions of the cylinder where it is heated more strongly by the source heater.

Our experience suggests that nucleation is tenuous for this system, and the situation abruptly switches from no film at all to a relatively thick film.

The means of control that we have with the existing system are several: (a) the O_2 partial pressure in the bell jar, by means of a leak valve, (b) the height of the cylinder, which should regulate the excess O_2 flux, (c) the magnitude of the Zn and O_2 fluxes (using a ZnO source) by the source temperature, and/or (d) the Zn pressure by using an elemental source of Zn rather than or in conjunction with a ZnO source.

CONCLUSIONS

Direct vacuum evaporation of ZnO in a controlled pressure O_2 environment appears promising. By optimizing the ZnO source size and configuration and the conditions for activating the surface reaction at the substrate, thicker films with controllable electronic properties should be able to be deposited.

ZnTe FILMS AND DEVICES

SUMMARY

Because of its possible application as a component in multi-band gap solar cells based on II-VI compounds and as an interlayer in ohmic contact to p-CdTe, the photoelectronic character of polycrystalline p-ZnTe films deposited on graphite substrates by HWVE was explored.

SAMPLE PREPARATION

ZnTe films were deposited on graphite substrates using the same techniques as used for the CdTe previously reported [e.g., PR #22]. The source material was un-doped single crystal ZnTe grown by the Crystal Synthesis Laboratory at the Center for Materials Research here at Stanford. The vapor pressure of ZnTe is considerably lower than that of CdTe, and we decided to increase growth time rather than altering the temperature profile in the hot-wall deposition cell. The difference in growth rate is about a factor of 50 at a source temperature of 646°C and a substrate temperature of $\sim 600^\circ\text{C}$. The growth time was increased by a factor of 10 to give films about 10 μm thick. The standard nucleation and film growth temperatures were used and no dopants were introduced during the deposition.

The following films and devices were among those deposited and constituted the final set of deliverables.

TABLE I. ZnTe DEVICES

<u>Number</u>	<u>Deposition</u>	<u>Window and/or device</u>
KF-48	CdTe/ZnTe/graphite	CdS (double layer) plus In dots
KF-49	ZnTe/graphite	CdS (double layer) plus In dots
KF-50	ZnTe/graphite	None
KF-51	ZnTe/graphite	None

MEASUREMENTS

Devices were made using the ZnTe films for preliminary evaluation as a solar cell component material. Schottky diodes were formed by deposition of In to evaluate diode formation, to measure carrier density by C-V analysis, and to measure through-the-film resistivity. The In diodes had somewhat soft forward J-V characteristics with high series resistance R_S . Typical values are $J_0 = 8 \times 10^{-6} \text{ A/cm}^2$ with an A factor of 2.2 and $R_S = 90 \text{ ohm-cm}^2$ at 0.5 V forward bias. The series resistance typically decreased with increasing forward bias, e.g., to about 9 ohm-cm^2 at 5 V. Capacitance-voltage measurement of one of the diodes at 1 MHz yielded a carrier density value of $N_A = 2-3 \times 10^{15} \text{ cm}^{-3}$ and an ac through-the-film resistivity value of $R_{ac} = 3.4 \text{ ohm-cm}^2$. The latter measurement gives an estimate of the bulk resistance of the grain interiors by removing the effects of the grain boundaries and contacts. Using N_A and R_{ac} , we obtain a mobility value of $\sim 1 \text{ cm}^2/\text{V-sec}$, probably grain boundary limited.

A solar cell [configuration (In grid)/ n^+ -CdS:In/ n -CdS/ p -ZnTe/graphite] was made by vacuum deposition of CdS with a total thickness of about 2 μm . Under 96 mW/cm^2 simulated AM1.5, this gave $V_{oc} = 0.191 \text{ V}$ and $J_{sc} = 0.04 \text{ mA/cm}^2$.

Contacts of Au applied to the ZnTe films on graphite yield completely ohmic behavior for through-the-film transport in both directions and give resistivities of $\sim 0.2 \text{ ohm-cm}^2$ (bulk resistivity = 200 ohm-cm).

A solar cell with the configuration (In grid)/ n^+ -CdS:In/ n -CdS/ p -CdTe/ p -ZnTe/graphite] was made by vacuum deposition of CdS with a total thickness of about 2 μm . Under 96 mW/cm^2 simulated AM1.5, this gave $V_{oc} = 0.512 \text{ V}$ and $J_{sc} = \sim 0.1 \text{ mA/cm}^2$. In this case the light-generated current was severely limited by the extremely high series resistance, $R_S = 3 \times 10^5 \text{ ohm-cm}^2$. Measurement at low light intensities showed that the excessive series resistance was at fault and, by extrapolation, that the intrinsic light-current generating capacity of the cell was near normal. Indium Schottky barriers formed on the same film (In/ p -CdTe/ p -ZnTe) show similar high series resistance values.

DISCUSSION - DEVICES ON ZnTe

Using the handbook value of the work function of In (4.1 eV) and the electron affinity value for ZnTe of 3.7 eV, the Schottky barrier height for the In/p-ZnTe junction is ~ 1.8 eV. Thus one expects the thermionic emission component of junction current to be very small. However the barrier to minority carrier injection into the depletion layer is small, 0.4 eV, and, given the polycrystalline nature of the ZnTe, the minority recombination-generation current in the depletion layer is likely to be quite large. From the results above this appears to be the case.

For the CdS/ZnTe heterojunction the predicted J_{sc} for AM1.5 is 1.5 mA/cm^2 , a factor of about 40 larger than that observed. The light-generated current was not limited by series resistance in this case, so it must be concluded that the diffusion length in the ZnTe is very short and/or that there is considerable loss of photogenerated carriers at the interface. The latter conclusion is likely because of large lattice mismatch and the relatively low electric field at the interface. The small V_{oc} is understandable, given that the junction diffusion voltage is limited to about 0.8 V by the predicted conduction band discontinuity. From extrapolation of the illuminated J-V characteristics, $V_{oc} = 0.42 \text{ V}$ is predicted for $J_{sc} = 20 \text{ mA/cm}^2$.

The ohmic, low resistance behavior of the Au contact on ZnTe/graphite suggests that both Au and graphite make excellent ohmic contacts to p-ZnTe even at these moderately low carrier densities. This is in agreement with the barrier height of ~ 0.3 eV, predicted by the electron affinity and work function.

For the CdS/CdTe/ZnTe/graphite cell, the high series resistance which limits the light-generated current is certainly due in part to the large CdTe thickness, 50 μm , but the large magnitude of R_s suggests that a blocking barrier may be formed between the p-CdTe and the p-ZnTe. Never-the-less, we feel that the introduction of a thin interlayer of more highly doped p-ZnTe at a metal or graphite junction with p-CdTe is a good possibility for making a low resistance contact.

CONCLUSIONS

1. The diode characteristics of the In/ZnTe device are not good because of excessive minority carrier transport, since the high Schottky barrier provides ready access for the minority carriers to the grain boundary states.
2. The potential of p-ZnTe as an ohmic contact forming interlayer at p-CdTe contacts is promising, since even at the relatively low carrier density of 10^{15} cm^{-3} , it makes good ohmic contact to both Au and graphite.

POLYCRYSTALLINE FILM CHARACTERIZATION

As a corollary to the earlier grain boundary GB work which concentrated mainly on bicrystals, a small effort was directed toward electronic characterization of polycrystalline p-CdTe films deposited on alumina substrates. These films were deposited by HWVE using the same techniques as described in previous reports. Measurements of across-the-film resistivity versus temperature and illumination were made and these data were analysed using a general GB electronic transport model.

SAMPLE PREPARATION AND MEASUREMENT

The sample preparation is as described previously (also see PR#22) and the physical and electronic characteristics reported here are a typical subset for these growth parameters. Typical values from earlier measurements are:

Thickness	30	μm
Grain size	4 - 10	μm
Resistivity (dc, through-the-film)	3×10^5	ohm-cm
Resistivity (ac, 1 MHz, TtF)	1300	ohm-cm
Carrier density ($1/\text{C}^2$)	0.5×10^{15}	cm^{-3}
Depletion layer width (In/p-CdTe)	1.8	μm

These films were deposited concurrently on alumina and high purity graphite substrates and the results reported here are for the alumina group. Deposition conditions are shown in Table VI.

Semi-ohmic contacts of Au were applied in a four stripe pattern by VE. Across-the-film (AtF) resistance was measured using the four point method with a differential voltmeter with $> 10^{13}$ ohms input resistance. Measurements were made versus temperature in the dark and with ir filtered tungsten illumination of ~ 2 suns. The I-V characteristics of the films show the typical $I \propto \sinh(V)$ shape associated with GB transport, Fig. 6. The zero bias resistance of two of the films, plotted in Fig. 7 versus $10^3/T$, show well defined activation energies of 0.72 eV for #20 and 0.66 eV for #21 in the dark. Near room temperature, illumination reduced these activation energies to ~ 0.2 eV. At higher temperatures the illuminated activation energies increased toward the dark values. At the highest temperatures used ($\sim 440^\circ\text{K}$) there was little difference between the light and dark resistivities. The electrical characteristics are summarized below.

ELECTRONIC PROPERTIES OF PX SAMPLES

SAMPLE	DARK		LIGHT		D/L	E (eV)	
	$R(10^6 \Omega)$	$\rho(10^6 \Omega\text{-cm})$	$R(10^6 \Omega)$	$\rho(10^6 \Omega\text{-cm})$		DARK	LIGHT
#20a	240	12	0.46	0.022	516	0.72	0.18
#21	80	4	0.4	0.02	176	0.66	0.15

D/L is dark/light resistance ratio.

TABLE VI. CdTe FILM DEPOSITIONS - GROWTH PARAMETERS

Sample No.	Growth Date	Source Boule	NUCLEATION			FINAL GROWTH		Film Thickness (μm)	Apparent Grain size (μm)
			CdTe Temp ($^{\circ}\text{C}$)	Substrate Temp. ($^{\circ}\text{C}$)	Growth Time (min)	Substrate Temp. ($^{\circ}\text{C}$)	Growth Time (min)		
===== 8/5/85 ===== System bake-out =====									
KF-20al	8/6/85	"	646	518	4	595 ^s	16	50-60	
KF-20gr	8/6/85	"	646	518	4	595 ^s	16	60-70	
KF-21al	8/7/85	"	646	518	4	595 ^s	16	50-60	20
KF-21gr	8/7/85	"	646	518	4	595 ^s	16	60	
KF-22al	8/7/85	"	646	518	4	595 ^s	16		
KF-22gr	8/7/85	"	646	518	4	595 ^s	16		
KF-23al	8/8/85	"	646	518	4	595	16		
KF-23gr	8/8/85	"	646	518	4	595	16		

^s Estimated temperature. Substrate TC broken; temperature measured at substrate furnace liner.

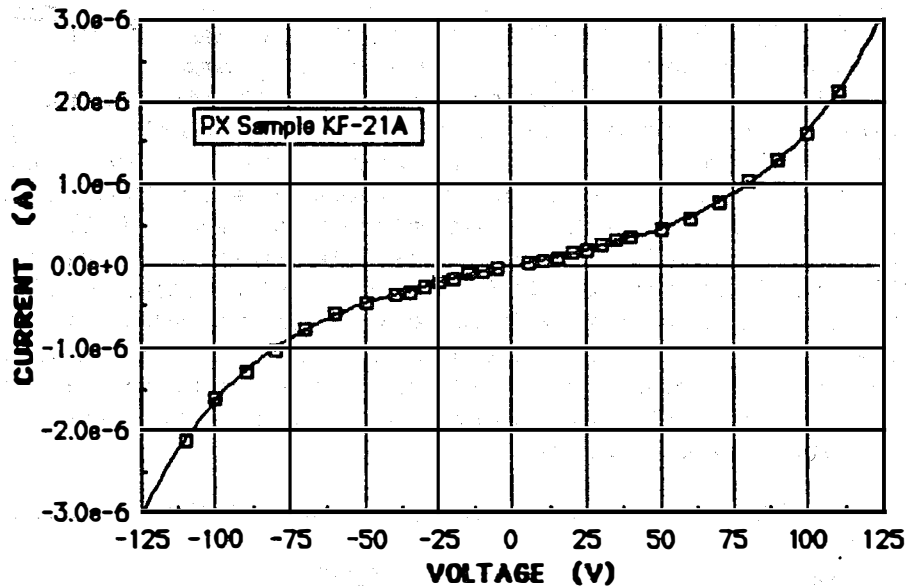


Fig. 6. Current-voltage characteristic for sample #21al at 25 $^{\circ}\text{C}$ in dark.

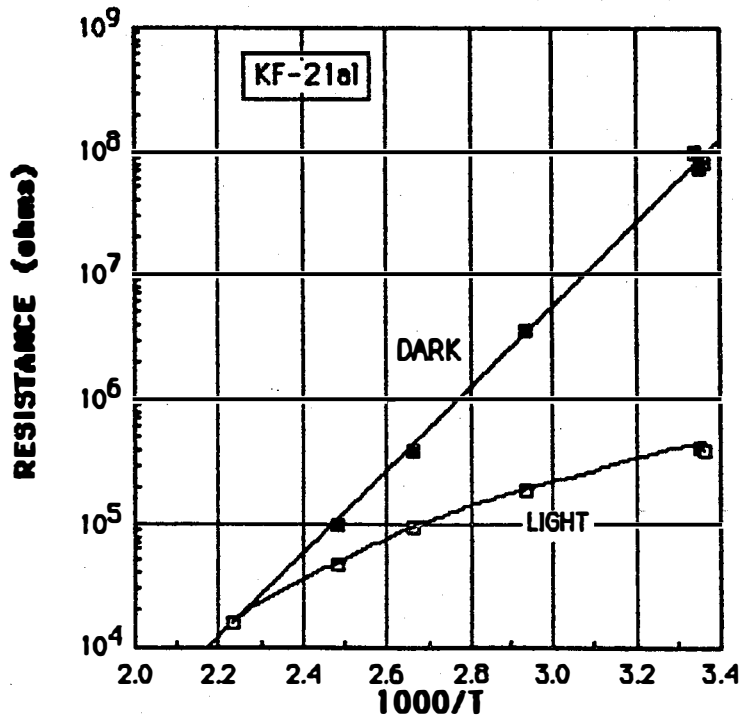
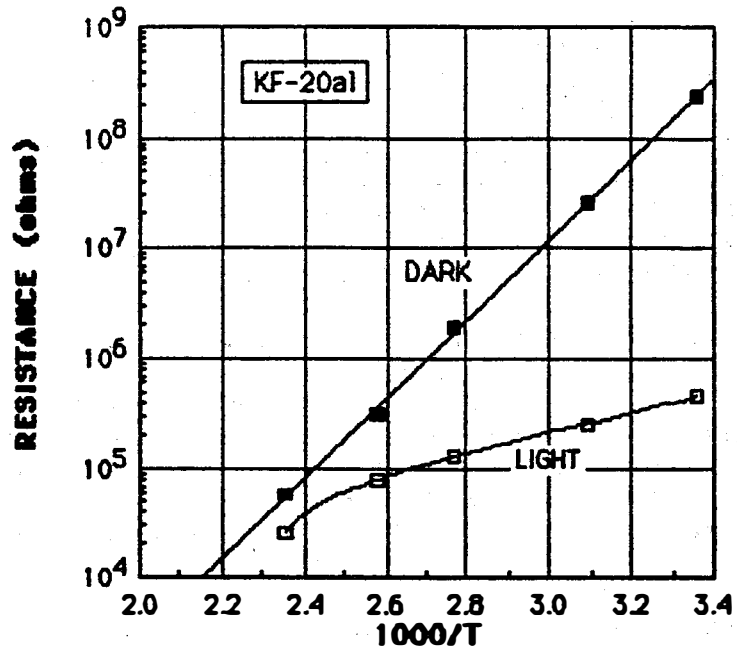


Fig. 7. Dark and illuminated resistance vs. $10^3/T$ for samples #20 and #21.

DISCUSSION

The activation energies measured here are consistent with those measured by other workers for similar films and bicrystals (5) and films (10). For the range of carrier densities N_A from 10^{15} to 10^{17} cm^{-3} , the range of measured activation energies for p-CdTe is 0.4 to 0.6 eV, from the above publications. Given the typical N_A values $\sim 10^{15}$ cm^{-3} for the present series of films, the GB depletion width should be on the order of 1 μm , or about 0.1 of the grain size. Thus the grains are only partially depleted by the GB potential barriers and the resistance of the films is controlled almost totally by the GB barriers rather than the bulk resistivity inside each grain. (A single crystal of this carrier density would have a resistivity of ~ 100 ohm-cm.)

In the dark, the along-the-film AtF resistivities of these films are 4 and 12×10^6 ohm-cm, about an order of magnitude higher than the typical through-the-film TtF values measured for previous devices from the high forward-bias slopes of the I-V data for In/p-CdTe/graphite diodes. This difference arises from the columnar character of the grains, with their long axis perpendicular to the substrate. For the AtF measurement more grain boundaries must be traversed by the current than for the TtF measurement.

The IV plot of Fig. 6 shows that significant breakdown of the linear characteristic does not occur until bias voltage across the V probes reaches ~ 100 V. Given the grain size of this film (~ 20 μm) and the probe spacing, this means that each grain boundary has ~ 3 V across it at 100 V total bias, almost all of this being across the reverse biased half of each GB potential barrier. Thus the density of GB states is large enough to substantially pin the Fermi level in the forward biased half of each barrier. The density of charge at the GB increases strongly with applied bias and prevents the effective barrier from being reduced very much by the applied bias (see for e.g., 8, p. 373). In this case the conductivity activation energy is given approximately by

$$E_{\sigma} = q\phi_{gb} + kT - qT(d\phi_{gb}/dT),$$

where the $d\phi_{gb}/dT$ term can be taken to be of the order of the variation of the band gap with temperature (about -0.0003 eV/ $^{\circ}\text{K}$ for CdTe).

A one-dimensional computer model for GB electronic transport was formulated as an extension of the model presented earlier [2] to the illuminated case. In essence, for the dark case the program finds the GB barrier height (measured from the Fermi level) for which the charge on the GB states (those above the Fermi level for p-type) exactly balances the depletion layer charge between the barriers. For the illuminated case, a "shell" around the dark case program finds the energy difference between the electron and hole quasi-Fermi levels such that the Shockley-Read-Hall recombination through the grain boundary and bulk recombination centers exactly balances the photogeneration in the layer. While such a program is somewhat inexact, because of its one

dimensional nature and for other reasons, it can give significant insight into the processes involved in transport. Whereas the carrier density, grain size, dark and light resistivity, and their variation with temperature are quite exact experimental inputs, the GB state distribution and its recombination behavior are derived circumstantially and are thus possibly inexact. In Fig. 8 is plotted a computer modeled resistivity versus $10^3/T$ curve using the properties of sample #21 along with its measured resistivity data. The best fit for the dark case resistivity magnitude and activation energy was obtained using a triangular GB state distribution with N_{gb} tapering from 2.6×10^{11} to $0 \text{ cm}^{-2}\text{-eV}^{-1}$ between 0.66 and 1.10 eV from the valence band. For this temperature range the Fermi level lies just above the lower edge of the GB state distribution. The derived values of the grain boundary barrier height ϕ_{gb} , diffusion voltage V_{gb} , conductivity activation energy E_o , and the resistivity are quite insensitive to the exact shape of the distribution. All that matters is the total number of charged states above the Fermi level. While this doesn't help us much in determining the N_{gb} distribution given this small range of experimental data, it does allow us to test distributions obtained by other means (such as deconvolution of the large bias I-V curves, or bicrystal capacitance measurements).

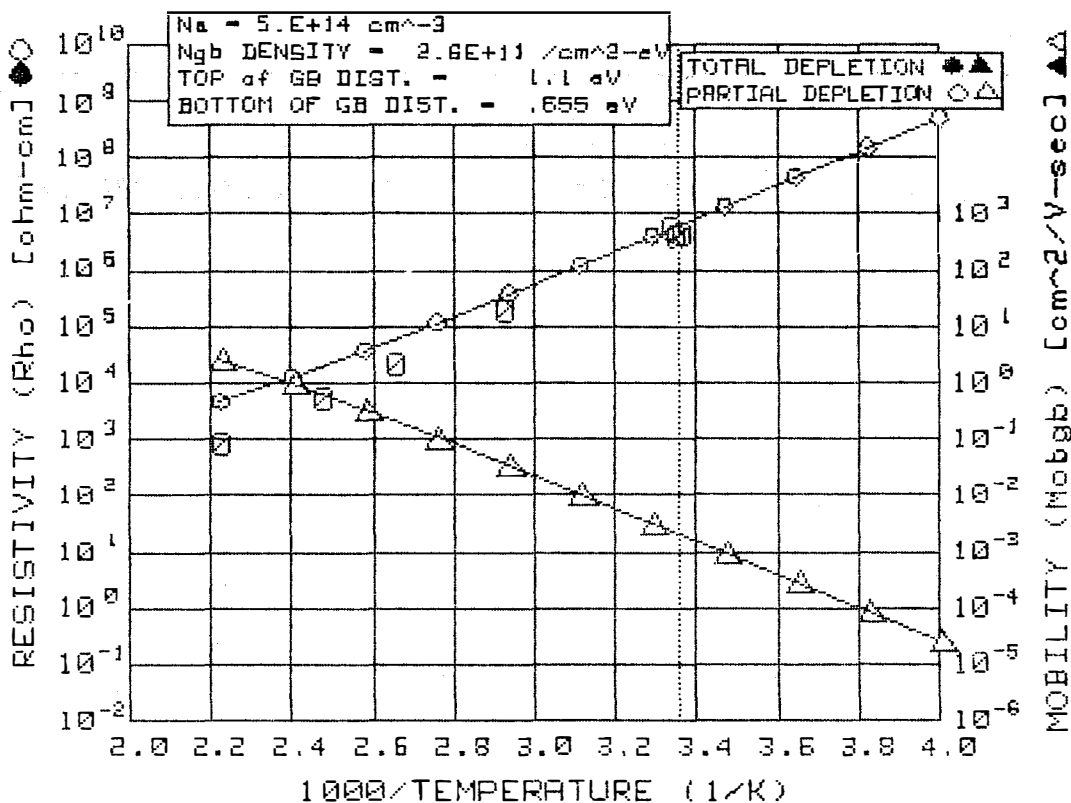
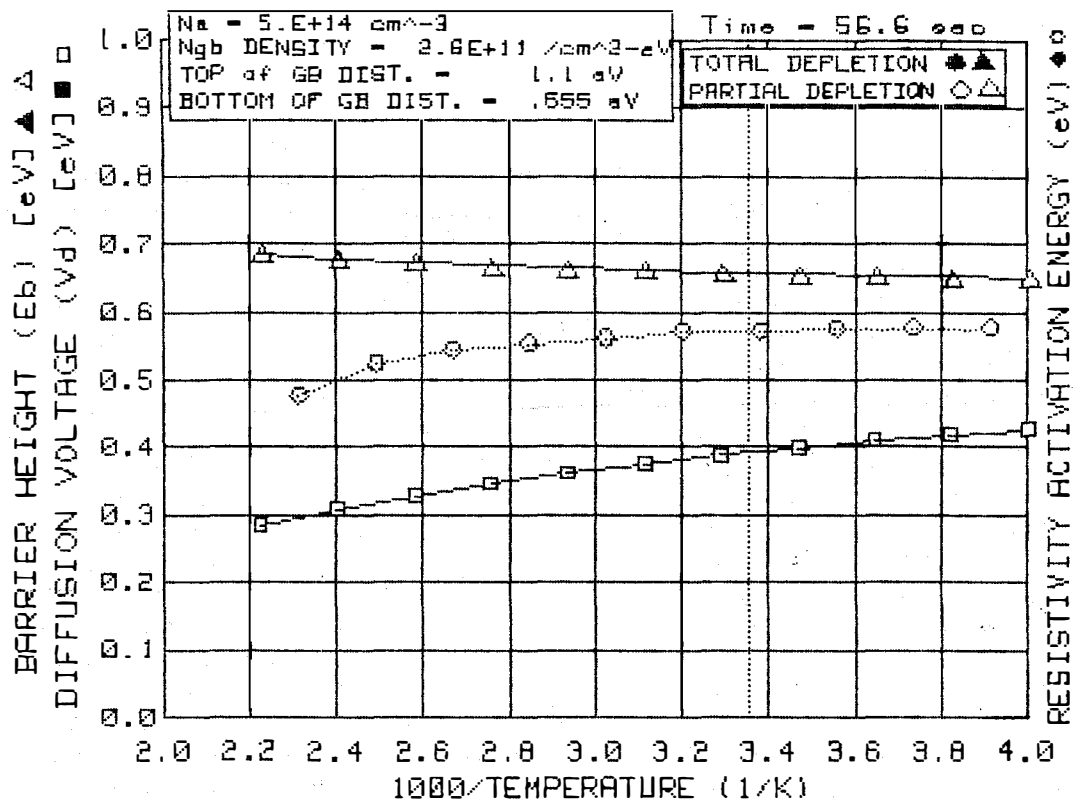


Fig. 8. (Top) Computer modeled barrier height, diffusion voltage, and resistivity activation energy vs $10^3/T$. (Bottom) Modeled resistivity and mobility vs $10^3/T$. Experimental data for sample #21 is shown by "O".

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SERI TECHNICAL REPORTS

- Progress Reports #1 - 8, 10/1/80-10/31/82, SERI subcontract XW-1-9330.
- Annual Report #9, 2/1/82-1/31/83, SERI subcontract XW-1-9330.
- Progress Reports #10 - 12, 1/1/83-10/31/83, SERI subcontract XW-1-9330.
- Annual Report #13, 2/1/83-1/31/84, SERI subcontract XE-2-02081-01.
- Progress Letters #14 - 15, 2/1/84-6/15/84, SERI subcontract XL-4-04022-1.
- Semi-Annual Progress Report #16, 2/16/84-8/15/84, SERI subcontract XL-4-04022-1.
- Progress Letters #17 - 18, 8/16/84-12/15/84, SERI subcontract XL-4-04022-1.
- Annual Technical Progress Report #19, 2/16/84-2/15/85 SERI subcontract XL-4-04022-1.
- Progress Letters #20 - 21, 2/16/85-6/15/85, SERI subcontract XL-4-04022-1.
- Semi-Annual Progress Report #22, 2/16/85-8/15/85 SERI subcontract XL-4-04022-1.
- Progress Letters #23 - 26, 8/16/85-6/15/86, SERI subcontract XL-4-04022-1.
- Final Report #27, 2/16/85-3/31/87 SERI subcontract XL-4-04022-1.

APPENDIX

A computer program listing "GBvsT" for computing grain boundary transport parameters vs temperature is attached. The program is written in BASIC 2.1 for the Hewlett-Packard 9816S computer. Semiconductor properties and grain boundary parameters are inserted directly into the program in lines 170 through 710. Special attention must be paid to the accuracy test parameter on lines 200 (which should be set to 0.0001 or less) and the prefactor on line 3270 which determines the step size in the Simpson's rule integration of the GB states. It should be set to 2 for rough surveys and 5 or greater for final runs. Increasing the latter parameter involves the most extra computing time.

The program is available on 3.5" disc upon request.

```

10 ! *** "GBvst2 " *** 2/5/87 ,1/30/87, 1/25/87, 1/22/87, 10/2/86
20 !
30 ! Grain boundary transport model: transport parameters vs temperature
40 ! for the dark case.
50 ! >>>>>>>> NOTE!!!! GRAPH2_1 MUST BE PRESENT <<<<<<<<<<<<<<<<
60 !
70 ! =====CONSTANTS=====
80 Print=0 ! '0' deletes most running comments
90 Print1=0 ! '0' deletes all the rest except Na
100 SET TIME 0
110 Timeo=TIMEDATE MOD 86400
120 !
130 ! -----Experimental conditions-----
140 ! T=300 ! Temperature (K)
150 ! -----Dimensions and graphics setup-----
160 !
170 To1=250 ! Range of temperature for graph, initial
180 To2=450 ! Range of temperature for graph, final
190 Dpts=10 ! Number of data points in range
200 Acc=.0001 ! Accuracy of Eb determination
210 ! Also note prefactor at "Integ" (determines partition)
220 ! -----Semiconductor variables-----
230 Sc#="p-CdTe" ! Name of semicond.
240 Gzo=7 ! Grain size (um)
250 Na=5.E+14 ! Hole density
260 Ln=1.E-4 ! Diffusion length for e' (cm)
270 Lp=5.E-5 ! Diffusion length for h'
280 Sn=1.E+10 ! GB recomb. velocity for e'
290 Sp=1.E+10 ! GB recomb. velocity for holes at RT (cm/sec)
300 Mobn=300 ! SX carrier mobility for e' (cm^2/V-sec)
310 Mobp=40 ! SX carrier mobility for h'
320 ! -----Grain boundary state distribution, rectangular approx.-----
330 Egb1=.7 ! Bottom of distrib., measured from Ev (eV)
340 Egb2=.95 ! Top of distrib., measured from Ev (eV)
350 Ngbden=5.E+11 ! GB state density, rect. (#/cm^3-eV)
360 Ngbtot=(Egb2-Egb1)*Ngbden ! Total # of GB states in distrib. (#/cm^3)
370 Deg=2 ! Degeneracy of GB states
380 ! .....integration to obtain Ngbtot.....
390 ! Fermi=0 ! Replaces fermi fn in 'Integ' with 1.00
400 ! GOSUB Integ ! To integrate total for strange distrib.
410 ! Ngbtot=Ngbo ! Integrated value of Ngbtot
420 ! .....
430 !
440 ! Other distributions at "Gb_dist:"
450 ! [Ngbden = FNGb(E,Egb1,Egb2,Ngbtot,...etc.)]
460 !
470 ! -----Semiconductor constants-----
480 Eg=1.5 ! Band gap (eV)
490 Eps=8.85E-14 ! Permittivity (F-cm)
500 Kapp=9.4 ! Relative dielectric constant (dc)
510 Eps=Kapp*Eps ! Semicond. permittivity
520 Nv=1.E+19 ! Density of states (val. band) at 300 K
530 Nc=2.E+18 ! Density of states (cond. band)
540 Meffh=1.1 ! Effective mass of holes for 'Arich' (m*/mo)
550 Arich=120 ! Richardson constant (A/K^2)
560 Astar=Arich*Meffh ! Effective Rich. const.
570 ! -----Physical constants-----
580 KO=8.48E-5 ! Boltzman const. (eV/K)
590 Q=1.6E-19 ! Electron charge
600 ! -----Derived quantities-----

```

```

610 ! Npo=Ni^2/Na ! Minority carr. dens. @ depl. layer edge for V=0
620 Gz=Gzo*1.E-4 ! um to cm
630 !
640 FOR Runvar=1 TO 1 ! To plot more curves on one graph
650 SELECT Runvar
660 CASE 1
670 Ngbden=5.E+11
680 CASE 2
690 Ngbden=7.5E+11
700 CASE 3
710 Ngbden=1.E+12
720 END SELECT
730 Ngbtot=(Egb2-Egb1)*Ngbden ! Total # of GB states in distrib. (#/cm^3)
740 !=====DECLARE VARIABLES=====
750 Declare: !
760 OPTION BASE 0
770 DIM T(50) ! Temperature (K)
780 ! DIM Na(50) ! Carrier density in bulk
790 DIM Ndl(50) ! Charge (number) density in depl. layers
800 DIM Ngbl(50) ! Charged states at GB (number density)
810 DIM Eb(50,1) ! Barrier height & total vs. partial depletion
820 DIM Vd(50,1) ! Diffusion voltage & total vs. partial depletion
830 ! DIM Ef(50) ! Fermi level at .....????????
840 DIM Rho(50,1) ! Resistivity
850 DIM Eact(50) ! Activation energy for resistivity
860 DIM Mobgb(50,1) ! GB limited mobility
870 DIM Naeff(50) ! Effective carrier density
880 INTEGER Grapheb(1:7500) ! storage for graph of Eb, etc.
890 INTEGER Graphrho(1:7500) ! storage for graph of Rho, etc.
900 !=====PROGRAM MECHANICS=====
910 !
920 Ebstepo=.3 ! Starting increment size for energy stepping
930 !
940 !=====DISPLAY CHOICES CONTROL=====
950 Graphdisp: !
960 OUTPUT 2;"K"; ! Clear screen
970 GOTO Main ! This section disabled
980 PRINT
990 PRINT TABXY(1,10),"GRAPHICS DISPLAY CHOICES:"
1000 PRINT
1010 PRINT TAB(3),"Eb, Vd vs Na",TAB(30),"E";
1020 PRINT TAB(3),"Rho, Mu vs Na",TAB(30),"R"
1030 PRINT TAB(3),"Both",TAB(30),"B or 'ENTER' "
1040 PRINT TAB(3),"Neither",TAB(30),"N";
1050 PRINT TABXY(0,0)
1060 !
1070 LINPUT "WHICH ?",Graf#
1080 IF Graf#<>"E" AND Graf#<>"R" AND Graf#<>"B" AND Graf#<>"N" AND Graf#<>" "
THEN
1090 ! GOTO Graphdisp
1100 END IF
1110 LINPUT "Print out data? (Y/N or ENTER)",Dataprint#
1120 OUTPUT 2;"K"; ! (clear screen)
1130 !
1140 !
1150 !=====PROGRAM BODY=====
1160 Main: !
1170 !-----Independent variable control-----
1180 Span=1000*((1/To1)-(1/To2))
1190 Int=Span/Dpts

```



```

2390 PRINT
2400 !.....
2410 !
2420 NEXT M
2430 !
2440 !-----Calculate activation energy for Rho-----
2450 FOR M=0 TO Dpts-1
2460 Eact(M)=K0*LOG(Rho(M+1,0)/Rho(M,0))/((1/T(M+1))-(1/T(M)))
2470 NEXT M
2480 !
2490 Time=TIMEDATE MOD 86400-Time0
2500 !
2510 Endcalc: !
2520 !=====END OF CALCULATIONS=====
2530 !
2540 !-----Display directives-----
2550 Displaydir: !
2560 GOSUB Graph_eb
2570 IF Graf#="R" THEN 2620
2580 IF Graf#="N" THEN Choice
2590 DISP "To see the Rho, Mu vs Na graph press CONT"
2600 PAUSE
2610 GSTORE Grapheb(*)
2620 GOSUB Graph_rho
2630 DISP "Press CONT for more choices"
2640 PAUSE
2650 GSTORE Graphrho(*)
2660 !
2670 NEXT Runvar
2680 !
2690 Choice: !
2700 OUTPUT 2;"k";
2710 GRAPHICS OFF
2720 PRINT TABXY(1,8)
2730 PRINT "WHAT'S NEXT DUDE???"
2740 PRINT
2750 PRINT "1. Display graph Eb, Vd vs Na"
2760 PRINT "2. Display graph rho, mu vs Na"
2770 PRINT "3. Print graph Eb, Vd vs Na"
2780 PRINT "4. Print graph rho, mu vs Na"
2790 PRINT "5. Print both graphs"
2800 PRINT "6. Print data"
2810 PRINT "7. EXIT"
2820 LINFUT "?????",Disp$
2830 IF Disp#="7" THEN Stop
2840 ALPHA OFF
2850 GRAPHICS ON
2860 GCLEAR
2870 IF Disp#="1" THEN
2880 GLOAD Grapheb(*)
2890 PAUSE
2900 END IF
2910 IF Disp#="2" THEN
2920 GLOAD Graphrho(*)
2930 PAUSE
2940 END IF
2950 IF Disp#="3" THEN
2960 GLOAD Grapheb(*)
2970 DUMP GRAPHICS #701
2980 END IF

```

```

2990 IF Disp#="4" THEN
3000 GLOAD Graphrho(*)
3010 DUMP GRAPHICS #701
3020 END IF
3030 IF Disp#="5" THEN
3040 GLOAD Grapheb(*)
3050 DUMP GRAPHICS #701
3060 PRINTER IS 701
3070 PRINT USING "2/"
3080 GLOAD Graphrho(*)
3090 DUMP GRAPHICS #701
3100 ! form feed
3110 PRINTER IS 1
3120 END IF
3130 IF Disp#="6" THEN
3140 ! print data
3150 END IF
3160 GOTO Choice
3170 !
3180 Stop: !
3190 !=====END OF PROGRAM=====
3200 !
3210 STOP
3220 !
3230 !=====SUBROUTINES=====
3240 !
3250 !=====INTEGRATION OF GB STATES=====
3260 Integ: !.....Integrates Ngb distrib. either with Fermi function or 1
3270 Iinc=2*INT(2.5*(1000/T(M))/2)+2 ! # of increments depends on temp.
3280 ! (2 = Prefactor good for most calc)
3290 Einc=(Egb2-Egb1)/Iinc
3300 Ngbo=0
3310 FOR I=0 TO Iinc
3320 IF I=0 OR I=Iinc THEN
3330 C=1
3340 ELSE
3350 IF I MOD 2>0 THEN
3360 C=4
3370 ELSE
3380 C=2
3390 END IF
3400 END IF
3410 !
3420 E=Egb1+I*Einc
3430 IF Fermi=0 THEN ! This is used to integrate Ngbden to get Ngbtot
3440 Ffermi=1
3450 ELSE
3460 Ffermi=1-(1/(1+(1/Deg)*EXP((E-Ebo)/(K0*T(M))))))
3470 END IF
3480 Ninc=(Einc/3)*C*FNGb(E,Egb1,Egb2,Ngbden)*Ffermi ! Rect. distrib.
3490 ! Ninc=(Einc/3)*C*FNGbtt(E)*Ffermi ! Thorpe's dist.
3500 ! PRINT "E=";E,"FNGbtt=";FNGbtt(E)
3510 Ngbo=Ngbo+Ninc
3520 NEXT I
3530 RETURN
3540 !
3550 !=====Eb and Vd vs Na GRAPHICS SET UP=====
3560 !
3570 Graph_eb: ! Subroutine for graphing barrier height and diff. voltage
3580 IF Runvar>1 THEN ! Skips setup for more than one curve

```

```

3590 GLOAD Grapheb(*)
3600 GOTO Ploteb
3610 END IF
3620 !
3630 OUTPUT 2;"K";
3640 GINIT
3650 GRAPHICS ON
3660 DEG
3670 GOSUB Symbols ' Load symbol defining arrays
3680 !----- Label axes -----
3690 VIEWPORT 0,100*RATIO,0,100
3700 LORG 5
3710 LDIR 90
3720 CSIZE 4,.7
3730 MOVE 7,50
3740 LABEL "DIFFUSION VOLTAGE (Vd) [eV]";
3750 CSIZE 3
3760 IMOVE -2,2
3770 SYMBOL F4(*)
3780 IMOVE -.6,5
3790 SYMBOL O4(*)
3800 MOVE 2,50
3810 CSIZE 4,.7
3820 LABEL "BARRIER HEIGHT (Eb) [eV]";
3830 CSIZE 3
3840 IMOVE -2,2
3850 SYMBOL F3(*)
3860 IMOVE -1.3,6
3870 SYMBOL O3(*)
3880 MOVE 98*RATIO,51
3890 CSIZE 4,.6
3900 LABEL "RESISTIVITY ACTIVATION ENERGY (eV)";
3910 IMOVE -2,2
3920 CSIZE 3
3930 SYMBOL F8(*)
3940 IMOVE 0,3.5
3950 SYMBOL O8(*)
3960 LDIR 0
3970 CSIZE 4
3980 MOVE 55*RATIO,2
3990 LABEL "1000/TEMPERATURE (1/K)"
4000 CSIZE 4
4010 MOVE 78*RATIO,98
4020 LABEL "Time =";DROUND(Time,3);"sec"
4030 MOVE 20,86
4040 !
4050 !----- Setup and number axes -----
4060 VIEWPORT 19,95*RATIO,11,96 ! this viewport does not include numbers
4070 ! (graph frame only)
4080 !..... Y axis description.....
4090 Maxe=1.0 ! Maximum value of energy axis
4100 Intervale=.1
4110 Mine=0
4120 Spame=Maxe-Mine
4130 !..... X axis description .....
4140 Mina=INT(1000/To2)
4150 Maxa=INT(1000/To1)+(FRACT(1000/To1)>.01)
4160 Spana=Maxa-Mina
4170 IF Spana>8 THEN Size=1
4180 IF Spana>2 AND Spana<=8 THEN Size=.5

```

```

4190 IF Spana>1 AND Spana<=2 THEN Size=.2
4200 IF Spana<=1 THEN Size=.1
4210 !.....
4220 WINDOW Mina,Maxa,0,Maxe
4230 GRID Size,Intervale,Mina,0,1,1,2
4240 VIEWPORT 0,100*RATIO,0,100 ! open it all up
4250 !-----Y axis numbers-----
4260 CSIZE 4
4270 FOR M=0 TO 1 STEP .2
4280 MOVE Mina-.04*Spana,M
4290 LABEL USING "Z.D";M
4300 NEXT M
4310 !-----X axis numbers-----
4320 FOR M=Mina TO Maxa+.0001 STEP Size
4330 MOVE M-.0.*Spana,-.05*Spame
4340 CSIZE 4
4350 IF Size>=1 THEN LABEL USING "DD";M
4360 IF Size<1 THEN LABEL USING "D.D";M
4370 NEXT M
4380 !----- Add RT axis-----
4390 MOVE 1000/298,0
4400 LINE TYPE 4
4410 DRAW 1000/298,Maxe
4420 !
4430 !-----graph Eb data-----
4440 Ploteb: !
4450 VIEWPORT 19,95*RATIO,11,96 ! this window does not include numbers
4460 WINDOW Mina,Maxa,0,Maxe
4470 VIEWPORT 0,100*RATIO,0,100 ! open it all up
4480 PENUP
4490 LINE TYPE 1
4500 CSIZE 3
4510 MOVE 1000/T(0),Eb(0,0)
4520 FOR M=0 TO Dpts
4530 PLOT 1000/T(M),Eb(M,0),-1 ! down before move
4540 PENUP
4550 IF Eb(M,1)=1 THEN
4560 SYMBOL F3(*)
4570 ELSE
4580 SYMBOL O3(*)
4590 END IF
4600 PENUP
4610 MOVE 1000/T(M),Eb(M,0)
4620 NEXT M
4630 !
4640 !-----graph Vd data-----
4650 PENUP
4660 LINE TYPE 1
4670 MOVE 1000/T(0),Vd(0,0)
4680 FOR M=0 TO Dpts
4690 PLOT 1000/T(M),Vd(M,0),-1 ! down before move
4700 PENUP
4710 IF Vd(M,1)=1 THEN
4720 SYMBOL F4(*)
4730 ELSE
4740 SYMBOL O4(*)
4750 END IF
4760 PENUP
4770 MOVE 1000/T(M),Vd(M,0)
4780 NEXT M

```

```

4790 !-----Graph activation energy data-----
4800 PENUP
4810 CSIZE 4
4820 MOVE ((1000/T(0))+(1000/T(1)))/2,Eact(0)
4830 FOR M=0 TO Dpts-1
4840 LINE TYPE 4
4850 PLOT ((1000/T(M))+(1000/T(M+1)))/2,Eact(M),-1
4860 PENUP
4870 LINE TYPE 1
4880 IF Eb(M,1)=1 THEN
4890     SYMBOL F8(*)
4900 ELSE
4910     SYMBOL O8(*)
4920 END IF
4930 PENUP
4940 MOVE ((1000/T(M))+(1000/T(M+1)))/2,Eact(M)
4950 NEXT M
4960 !
4970 !-----label parameters-----
4980 GOSUB Labelparam
4990 LORG 5
5000 !
5010 RETURN
5020 !
5030 !===== Graph resistivity, mobility =====
5040 Graph_rho: !
5050 !
5060 IF Runvar>1 THEN
5070     GLOAD Graphrho(*)
5080     GOTO Plotrho
5090 END IF
5100 !
5110 !===== Set up graphics =====
5120 OUTPUT 2;"K";
5130 GINIT
5140 GRAPHICS ON
5150 DEG
5160 VIEWPORT 0,100*RATIO,0,100
5170 !-----label axes-----
5180 LORG 5
5190 LDIR 90
5200 CSIZE 4,.7
5210 MOVE 2,54
5220 LABEL "RESISTIVITY (Rho) [ohm-cm]"
5230 CSIZE 5
5240 MOVE 2,92
5250 SYMBOL F8(*)
5260 MOVE 2,95
5270 SYMBOL O8(*)
5280 CSIZE 4,.7
5290 MOVE 98*RATIO,50
5300 LABEL "MOBILITY (Mobgb) [cm^2/V-sec]"
5310 CSIZE 3
5320 MOVE 98*RATIO,93
5330 SYMBOL F3(*)
5340 MOVE 98*RATIO,96
5350 SYMBOL O3(*)
5360 CSIZE 4,.7
5370 LDIR 0
5380 MOVE 50*RATIO,2

```

```

5390 LABEL "1000/TEMPERATURE (1/K)"
5400 !-----setup and number axes-----
5410 VIEWPORT 15,87*RATIO,11,96 ! This viewport does not include number
5420 ! labels (graph frame only)
5430 !..... X axis description .....
5440 Mina=INT(1000/To2)
5450 Maxa=INT(1000/To1)+(FRACT(1000/To1)>.01)
5460 Spana=Maxa-Mina
5470 IF Spana>8 THEN Size=1
5480 IF Spana>2 AND Spana<=8 THEN Size=.5
5490 IF Spana>1 AND Spana<=2 THEN Size=.2
5500 IF Spana<=1 THEN Size=.1
5510 !.....y1 axis description....
5520 Rhoo1=1.E-2
5530 Rhoo2=1.E+10
5540 Miny1=INT(LGT(Rhoo1))
5550 Maxy1=INT(LGT(Rhoo2))+(FRACT(LGT(Rhoo2))>.01)
5560 Spany1=Maxy1-Miny1
5570 !
5580 !.....y2 axis description....
5590 Mobo1=1.E-6
5600 Mobo2=1.E+6
5610 Miny2=INT(LGT(Mobo1))
5620 Maxy2=INT(LGT(Mobo2))+(FRACT(LGT(Mobo2))>.01)
5630 Spany2=Maxy2-Miny2
5640 Shift=Miny1-Miny2 ! registers data on y1,y2 axes
5650 !-----now plot graph and number labels-----
5660 WINDOW Mina,Maxa,Miny1,Maxy1
5670 GRID Size,1,Mina,Miny1,1,1,2
5680 VIEWPORT 0,100*RATIO,0,100 ! open it all up
5690 !-----Y1 axis numbers-----
5700 FOR M=0 TO Spany1
5710     MOVE Mina-.065*Spana,M+Miny1
5720     CSIZE 4
5730     LABEL "10";
5740     CSIZE 3
5750     IMOVE .02*Spana,.04*Spany1
5760     LABEL VAL$(M+Miny1)
5770 NEXT M
5780 !-----Y2 axis numbers-----
5790 FOR M=0 TO Spany1-3
5800     MOVE Maxa+.04*Spana,M+Miny1
5810     CSIZE 4
5820     LABEL "10";
5830     CSIZE 3
5840     IMOVE .02*Spana,.04*Spany1
5850     LABEL VAL$(M+Miny1-Shift) ! The Shift changes numbering of y2 axis
5860 NEXT M
5870 !-----X axis numbers-----
5880 FOR M=Mina TO Maxa+.0001 STEP Size
5890     MOVE M-.0*Spana,Miny1-.04*Spany1
5900     CSIZE 4
5910     LABEL USING "DD.D";M
5920 NEXT M
5930 ! -----add RT line-----
5940 MOVE 1000/298,Miny1
5950 LINE TYPE 4
5960 IDRAW 0,Spany1
5970 !
5980 !

```



```

5990 !----graph Rho data-----
6000 Plotrho: !
6010 VIEWPORT 15,87*RATIO,11,96 ! This viewport does not include numbers
6020 WINDOW Mina,Maxa,Miny1,Maxy1
6030 VIEWPORT 0,100*RATIO,0,100
6040 PENUP
6050 IF Runvar=1 THEN Lt=1
6060 IF Runvar=2 THEN Lt=7
6070 IF Runvar=3 THEN Lt=8
6080 CSIZE 4
6090 MOVE 1000/T(0),LGT(Rho(0,0))
6100 FOR M=0 TO Dpts
6110 LINE TYPE Lt
6120 PLOT 1000/T(M),LGT(Rho(M,0)),-1 ! down before move
6130 PENUP
6140 LINE TYPE 1
6150 IF Rho(M,1)=1 THEN
6160 SYMBOL F8(*)
6170 ELSE
6180 SYMBOL O8(*)
6190 END IF
6200 PENUP
6210 MOVE 1000/T(M),LGT(Rho(M,0))
6220 NEXT M
6230 !
6240 !----graph Mob data-----
6250 PENUP
6260 MOVE 1000/T(0),LGT(Mobgb(0,0))+Shift
6270 FOR M=0 TO Dpts
6280 LINE TYPE Lt
6290 PLOT 1000/T(M),LGT(Mobgb(M,0))+Shift,-1 ! down before move
6300 PENUP
6310 LINE TYPE 1
6320 IF Mobgb(M,1)=1 THEN
6330 SYMBOL F3(*)
6340 ELSE
6350 SYMBOL O3(*)
6360 END IF
6370 PENUP
6380 MOVE 1000/T(M),LGT(Mobgb(M,0))+Shift
6390 NEXT M
6400 !-----label parameters-----
6410 GOSUB Labelparam
6420 LORG 5
6430 !-----
6440 RETURN
6450 !
6460 !
6470 !-----Subroutine to label parameters on graphs-----
6480 Labelparam: !
6490 VIEWPORT 15*RATIO,62*RATIO,86,100
6500 WINDOW 0,1,0,1
6510 PEN -1
6520 LINE TYPE 1
6530 GRID .004
6540 PEN 1
6550 FRAME
6560 MOVE .02,.76
6570 CSIZE 3.3
6580 LORG 1

```

```

6590 LABEL "Na =" ;Na; "cm^-3"
6600 LABEL "Ngb DENSITY = " ;Ngbden; "/cm^2-eV"
6610 LABEL "TOP of GB DIST. = " ;Egb2; "eV"
6620 LABEL "BOTTOM OF GB DIST. = " ;Egb1; "eV"
6630 ! .....add legend for point symbols.....
6640 VIEWPORT 63*RATIO,93*RATIO,88,95
6650 WINDOW 0,1,0,1
6660 PEN -1
6670 GRID .004
6680 PEN 1
6690 FRAME
6700 MOVE .02,.50
6710 CSIZE 3.3
6720 LORG 1
6730 LABEL "TOTAL DEPLETION ";
6740 IMOVE 0,-.05
6750 CSIZE 4
6760 SYMBOL F8(*)
6770 IMOVE .08,-.16
6780 CSIZE 3
6790 SYMBOL F3(*)
6800 MOVE .02,.02
6810 LABEL "PARTIAL DEPLETION ";
6820 IMOVE 0,-.05
6830 CSIZE 4
6840 SYMBOL O8(*)
6850 CSIZE 3.3
6860 IMOVE .08,-.16
6870 SYMBOL O3(*)
6880 RETURN
6890 !
6900 Symbols: !
6910 !-----Define symbol arrays-----
6920 !....."F3", a filled triangle.....
6930 REAL F3(5,2)
6940 READ F3(*)
6950 DATA 0,0,11, 1,0,13, 0,2,-1, 13,2,-1, 6,12,-1, 0,2,0
6960 !
6970 !....."O3", an open triangle.....
6980 REAL O3(5,2)
6990 READ O3(*)
7000 DATA 0,0,11, -1,0,13, 0,2,-2, 13,2,-1, 6,12,-1, 0,2,0
7010 !
7020 !....."F4", a filled box.....
7030 REAL F4(6,2)
7040 READ F4(*)
7050 DATA 0,0,11, 1,0,13, 1,4,-2, 9,4,-1, 9,12,-1, 1,12,-1, 1,4,0
7060 !....."O4", an open box.....
7070 REAL O4(6,2)
7080 READ O4(*)
7090 DATA 0,0,11, -1,0,13, 1,4,-2, 9,4,-1, 9,12,-1, 1,12,-1, 1,4,0
7100 !....."F8", a filled circle.....
7110 REAL F8(14,2)
7120 READ F8(*)
7130 DATA 0,0,11, 1,0,13, 1,8,-2, 2,6,-1, 3,5,-1, 5,4,-1, 7,5,-1
7140 DATA 8,6,-1, 9,8,-1, 8,10,-1, 7,11,-1, 5,12,-1, 3,11,-1
7150 DATA 2,10,-1, 1,8,0
7160 !....."O8", an open circle.....
7170 REAL O8(14,2)
7180 READ O8(*)

```

```

7190 DATA 0,0,11, -1,0,13, 1,8,-2, 2,6,-1, 3,5,-1, 5,4,-1, 7,5,-1
7200 DATA 8,6,-1, 9,8,-1, 8,10,-1, 7,11,-1, 5,12,-1, 3,11,-1
7210 DATA 2,10,-1, 1,8,0
7220
7230 RESTORE
7240 RETURN
7250 !=====
7260
7270 END
7280
7290 !=====FUNCTIONS=====
7300 DEF FNGb(E,Egb1,Egb2,Ngbden)
7310 IF E>=Egb1 AND E<=Egb2 THEN
7320 Z=Ngbden
7330 ELSE
7340 Z=0
7350 END IF
7360 RETURN Z Returns Ngbden(E)
7370 FNEND
7380 !-----T. THORPE'S Distribution-----
7390 '... (BE SURE TO SET Egb1=0 and Egb2=1.5 BEFORE USING)....
7400 DEF FNGbt(E)
7410 IF 0<=E AND E<.45 THEN
7420 Z=(+1)*((1.E+12)-(8.E+11)*(E/.45))
7430 END IF
7440 IF .45<=E AND E<=1.05 THEN
7450 Z=0
7460 END IF
7470 IF 1.05<E AND E<=1.5 THEN
7480 Z=(+1)*((2.E+11)+(2.E+13)*((E-1.05)^4)/(.45^4))
7490 END IF
7500 IF E<0 OR E>1.5 THEN
7510 Z=0
7520 END IF
7530 RETURN Z Returns Ngbden(E)
7540 FNEND

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Document Control Page	1. SERI Report No. SERI/STR-211-3190	2. NTIS Accession No.	3. Recipient's Accession No.
4. Title and Subtitle Preparation and Properties of Evaporated CdTe Films, Final Subcontract Report, 16 February 1985 - 31 March 1987		5. Publication Date July 1987	6.
7. Author(s) R.H. Bube, A.L. Fahrenbruch, K.F. Chien		8. Performing Organization Rept. No.	
9. Performing Organization Name and Address Department of Materials Science and Engineering Stanford University Stanford, California 94305		10. Project/Task/Work Unit No. 3494.10	11. Contract (C) or Grant (G) No. (C) XL-4-04022-1 (G)
		12. Sponsoring Organization Name and Address Solar Energy Research Institute 1617 Cole Boulevard Golden, Colorado 80401	
13. Type of Report & Period Covered Technical Report		14.	
15. Supplementary Notes SERI Technical Monitor: Richard Mitchell			
16. Abstract (Limit: 200 words) Previous work on evaporated CdTe films for photovoltaics showed no clear path to successful p-type doping of CdTe during deposition. Post-deposition annealing of the films in various ambients thus was examined as a means of doping. Anneals were done in Te, Cd, P, and As vapors and in vacuum, air, and Ar, all of which showed large effects on series resistance and diode parameters. With As, series resistance values of In/p-CdTe/graphite structures decreased markedly. This decrease was due to a decrease in grain boundary and/or back contact barrier height, and thus was due to large increases in mobility; the carrier density was not altered substantially. Although the series-resistance decreases were substantial, the diode characteristics became worse. The decreases were not observed when CdS/CdTe cells were fabricated on Te vapor-annealed films. Preparation of ZnO films by reactive evaporation yielded promising results. Deposition of p-ZnTe films by hot-wall vapor evaporation, using conventional techniques, yielded acceptable films without intentional doping.			
17. Document Analysis a. Descriptors Photovoltaic cells ; thin films ; cadmium telluride solar cells ; deposition b. Identifiers/Open-Ended Terms c. UC Categories 63			
18. Availability Statement National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, Virginia 22161		19. No. of Pages 52	20. Price A04