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Polycrystalline Thin Film Materials and Devices

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SUMMARY

Objectives:

The objectives of this research are to obtain the understanding of the materials processing, properties and performance of polycrystalline thin-film $CuInSe_2$ and CdTe solar cells that are needed to achieve the goals for efficiency, reliability and cost for flat plate thin-film photovoltaic systems set by DOE for the National Photovoltaics Program. A further objective of this program is to support the development of a competitive U.S. photovoltaic industry through collaboration with other research groups and the training of photovoltaic engineers and scientists.

Discussion:

A three-year phased research program of integrated investigations of processing, properties and performance of thin-film $CuInSe_2$ and CdTe solar cells was undertaken by the Institute of Energy Conversion (IEC). Phase I, which was completed at the end of the first year, comprised of two tasks: $CuInSe_2$-Based Materials and Devices; and CdTe-Based Materials and Devices.

Research on $CuInSe_2$-based materials and devices during Phase I concentrated on formation of $CuInSe_2$ thin-films by selenization of copper and indium layers, mechanisms limiting open circuit voltage in $CuInSe_2$ solar cells and an examination of the influence of $CuInSe_2$ thickness on performance.

Formation of $CuInSe_2$ by selenization of copper and indium metal layers promises to be readily translated from laboratory scale solar cells to commercial scale module manufacturing. The research conducted during Phase I of this program has found that the initial reaction of copper/indium bi-layers at 400°C with 2.5 mole per cent hydrogen selenide in argon at atmospheric pressure proceeds rapidly via a copper rich solid phase and indium rich liquid phase. Two micron thick $CuInSe_2$ films meeting the stoichiometry and morphology requirements for use in solar cells were formed using initial copper and indium bi-layers that were 0.23 and 0.56 microns thick, respectively. A small (active area~0.08 cm^2) $CuInSe_2$/CdS device with efficiency near 10% was made.

An alternative approach to selenization which replaces flowing hydrogen selenide with reaction of deposited layers of selenium indium and copper was also investigated. Single phase $CuInSe_2$ films were prepared in a bell-jar vacuum system at 400°C with continuous impingement of thermally evaporated selenium during growth. A cell efficiency of 7% was attained.

The investigation of band gap modified $CuInSe_2$ using compositionally graded $Cu(InGa)Se_2$ to improve open circuit voltage was complicated by the presence of photoconductive behavior in the

ZnCdS window layer. Experiments have shown that the photoconductive behavior is associated with introduction of a Ga gradient during growth of the band gap modified layer using elemental evaporation techniques. In a related study, incorporation of gallium into the back of a cell by depositing a thin, 0.02 micron, layer of Ga onto the substrate prior to formation of the $CuInSe_2$ was found to have negligible effect on open circuit voltage.

Examining a large number (>100) of standard $CuInSe_2$ cells has shown that the devices with the highest V_{oc} are not those with the highest efficiency. Moreover, further analysis showed that the limitations to open circuit voltage cannot be described by simple Shockley-Read-Hall recombination mechanism. An admixture of SRH and interface recombination or SRH with a voltage-dependent diode "A" factor were found to be consistent with observations to date.

One result of reducing the $CuInSe_2$ thickness is that the metal-$CuInSe_2$ back contact plays a larger role in the performance of the device. Three types of behavior -ohmic, blocking and accumulation- were considered. For $CuInSe_2$ less than one micron thick, either ohmic or blocking contacts contribute to significant degradation in cell performance. Achievement of thin high efficiency $CuInSe_2$ cells is likely to require development of an accumulation type contact which may be expected from placing a higher band gap layer of $Cu(InGa)Se_2$ between the $CuInSe_2$ and Mo.

Research on CdTe-based solar cells during Phase I concentrated on improving the repeatability of post-deposition processing. It was found that the 400°C heat treatment of $CdCl_2$-coated CdTe works best if done in an Ar-O_2 atmosphere. CdTe cells with open circuit voltage greater than 750 mV, fill factor exceeding 72% and efficiencies approaching 10% under Global AM 1.5 test conditions were achieved.

Efforts to improve short circuit current focussed on increasing light transmission through the CdS window layer. Thinner and restructured CdS layers were investigated and short circuit currents of 22-24 mA/cm^2 were observed. Reduction in CdS thickness below 0.1 micron resulted in poor diode behavior. Reduction in thickness of evaporated CdS below 0.1 micron resulted in poor diode behavior.

Evaporated CdTe/CdS cells with Cu/Au contacts stored in ambient dark conditions for up to 18 months were found to degrade. Examination of these cells confirms reports by others attributing the degradation to the influence of gold in the contact to CdTe. CdTe/CdS cells with ZnTe:Cu contacts appear to be more stable than cells with gold contacts.

Studies of CdTe/CdS junction behavior from measurements of current-voltage behavior and spectral response indicated that the cell

operates as p-n heterojunction with current dominated by SRH recombination in the junction region of the CdTe.

Highlights:

- A small area (0.08 cm^2) $CuInSe_2$/CdS solar cell with 10% efficiency was fabricated with $CuInSe_2$ formed by selenization with hydrogen selenide.

- Single phase $CuInSe_2$ films were prepared by reaction of deposited copper-indium-selenium layers and a cell efficiency of 7% was attained.

- The open circuit voltage of $CuInSe_2$ solar cells cannot be solely described by a Shockley-Read-Hall recombination mechanism.

- For $CuInSe_2$ less than one micron thick, the back contact significantly influences cell performance.

- Restructuring of CdTe by heat treating $CdCl_2$-coated CdTe must be carried out without exposure to moisture.

- By reducing the thickness of CdS in CdTe/CdS solar cells, short circuit currents of 22-24 mA/cm^2 were observed. Further reduction in CdS thickness below 0.1 micron was limited by interdiffusion between CdS and CdTe.

- CdTe/CdS cells with gold contacts stored without protection from the atmosphere were found to degrade. The degradation was attributed to the gold contact to CdTe. CdTe/CdS cells with ZnTe:Cu contacts appeared to be more stable.

- The CdTe/CdS cell operates as p-n heterojunction with current dominated by SRH recombination in the junction region of the CdTe.

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SECTION 1.0
INTRODUCTION

1.1 BACKGROUND

Modules utilizing copper-indium-selenide ($CuInSe_2$) and cadmium telluride (CdTe) have emerged as promising candidates for meeting the DOE long range efficiency, reliability and cost targets for flat plate photovoltaic energy systems (1).

Under the SERI Polycrystalline Thin-Film Task, the Institute of Energy Conversion (IEC) has been conducting an integrated program of investigation of $CuInSe_2$-solar cells (2). IEC has established a two-step physical vapor deposition (PVD) process and characterization capabilities for fabricating and analyzing state-of-art $CuInSe_2$ materials and devices. This enabled IEC to: achieve open circuit voltage of 0.55 Volts by alloying $CuInSe_2$ with Ga to increase the band gap; show that band gap modified $Cu(InGa)Se_2/CuInSe_2$ has promise for achieving increased open circuit voltage without loss in short circuit current; fabricate a $CuInSe_2/CdS$ solar cell with short circuit current of 40 mA/cm^2 using a thin CdS window layer deposited from aqueous solution and sputtered ZnO transparent conductor; fabricate a $CuInSe_2/CdS$ solar cell in a superstrate configuration - glass/ITO/CdS/$CuInSe_2$/Pt - with >5% efficiency; develop a bi-facial spectral response technique for determining the diffusion length and optical absorption coefficient of $CuInSe_2$ in an operational $CuInSe_2$ solar cell; and quantitatively model the effects on current-voltage behavior of heating $CuInSe_2$ solar cells in air and in hydrogen on the basis of reversible changes in Fermi level position in $CuInSe_2$.

IEC also initiated a chemical reaction engineering analysis of the formation of device quality $CuInSe_2$ by selenization of copper and indium metal layers, a process which promises to be more readily translated from the laboratory scale solar cells to large area module manufacturing.

These results, along with those obtained by others under the SERI Polycrystalline Thin-Film Task indicate that further improvements in performance and cost potential of $CuInSe_2$ modules can be expected from continued investigations of processing, material properties and device behavior.

Research conducted by IEC on CdTe has also shown that PVD is capable of producing near state-of-art CdTe materials and devices and that sequential post-deposition treatments are critical for achieving efficiencies above 10% regardless of CdTe deposition technique (2). Recent results obtained by IEC and others under the SERI Polycrystalline Thin-Film Task indicate that further research is likely to lead to achievement of practical efficiencies greater than 15% and long term stability for thin-film CdTe modules.

Accordingly, a continued research effort with the objective of obtaining the understanding of materials processing, properties and performance of polycrystalline thin-film solar cells needed to achieve the goals for performance, cost and reliability set by DOE for the National Photovoltaics Program is needed. A further objective of such a program should be to support the development of competitive U.S. photovoltaic industry through collaboration with other research groups and the training of engineers and scientists in photovoltaic technology.

1.2 TECHNICAL APPROACH

In order to achieve these objectives IEC has undertaken a phased three year program to carry out the following integrated research tasks:

Task 1 - $CuInSe_2$ Based Materials and Devices

A. Characterize and optimize selenization of Cu/In films with a primary goal of establishing capability to fabricate state-of-art $CuInSe_2$ materials and devices by selenization and explore use of alternatives to H_2Se.

B. Increase open circuit voltage in $CuInSe_2$-based solar cells, through investigations of reducing space charge recombination by alloying with gallium and/or sulfur and reducing the space charge width in the $CuInSe_2$ by optimizing doping levels in the $CuInSe_2$ and window layers.

C. Examine interface recombination as a limiting mechanism for open circuit voltage by fabricating and characterizing $CuInSe_2$ heterojunctions with ZnSe, ZnO, or other thin, n-type materials.

D. Identify the controlling mechanisms and demonstrate approaches for improving open circuit voltage in superstrate $CuInSe_2$ devices.

E. Quantify losses due to multidimensional junction effects and relate them to material processing and properties.

Task 2 - CdTe Based Materials and Device

A. Characterize and optimize fabrication of state-of-art CdTe material and devices using physical vapor deposition to deposit CdTe.

B. Develop and characterize thermally stable, transparent contacts to CdTe.

C. Develop a quantitative model of the effects of sequential post-deposition processing, from systematic studies of the following relationships: $CdCl_2$/high temperature heat treatment step and restructuring of CdTe; contacting/low temperature heat treatment and type conversion of CdTe; chemical treatments with bromine-methanol (or hydrazine).

D. Develop and optimize high transparency n-type window layer/heterojunction partners for increased short circuit current. Tin oxide and thin (<50 nm) CdS will be investigated for realizing short circuit currents in excess of 25 mA/cm^2. Other window layers, including ZnCdS, will be used to study heterojunction interface mechanisms limiting open circuit voltage.

Task 3 - $CuInSe_2$ and CdTe Cells with Thin Absorber Layers

A. Fabricate and characterize $CuInSe_2$ solar cells with $CuInSe_2$ absorber layers 1 micron or less in thickness and CdTe solar cells with CdTe absorber layers 0.3 micron or less in thickness. The effects of thin absorber layers on cell efficiency will be investigated. Losses in short circuit current, open circuit voltage and fill factor will be investigated. Losses in short circuit current, open circuit voltage and fill factor due to reduced thickness will be quantified with particular emphasis on recombination losses at ohmic contacts, optical losses due to decreased optical path length and shunts.

B. Develop and assess approaches for minimizing thickness-related losses, with particular emphasis on use of back surface reflection and texture to enhance optical absorption in thin $CuInSe_2$ and CdTe cells.

C. Fabricate and optimize the efficiency of thin absorber layer $CuInSe_2$ and CdTe solar cells.

1.3 OUTLINE OF REPORT

In this report we describe the significant results and conclusions reached at the end of the first year of the program.

Section 2.0 is devoted to $CuInSe_2$ material and device research. Results of studies of the kinetics of $CuInSe_2$ formation by reaction of Cu and In layers with H_2Se and the achievement of a 10% small area cell are described in Section 2.1. $CuInSe_2$ formation, materials characterization and solar cell results obtained by reaction of Cu/In layers with elemental Se are also presented. In Section 2.2 efforts to understand and develop effective ways of improving open circuit voltage in $CuInSe_2$ devices are reported in connection with photoconductive window layer effects on band gap modified $CuInSe_2$ devices. The relationship between open circuit voltage and diode ideality factor obtained from analysis of current-voltage data is also discussed in Section 2.2. The characteristics of superstrate devices, influence of grain structure and implications for future developments are presented in Section 2.3. The report of progress with $CuInSe_2$ materials and devices concludes in Section 2.4 with a consideration of the effect of thin $CuInSe_2$ on device performance.

CdTe solar cell device research is covered in Section 3.0. The effects of humidity and heat treatment atmosphere on the effectiveness and repeatability of post-deposition processing of are described in Section 3.1. Section 3.2 reports the results of an investigation of window layer processing and properties in connection with improving the short circuit current in CdTe solar cells. The effect of contacts on CdTe cell behavior and stability found in Section 3.3 includes results obtained with ZnTe:Cu contacts that were developed at IEC under the SERI "New Ideas" Program, as well as conventional metal contacts. Finally, efforts to characterize and understand CdTe device behavior are reported in Section 3.4. The discussion of device analysis results includes a comparison of methods for determining short circuit current, sub-band gap spectral response, and mechanisms of junction recombination.

SECTION 2.0
$CuInSe_2$ MATERIALS AND DEVICES

2.1 $CuInSe_2$ THIN GROWTH

$CuInSe_2$ films were grown by two techniques: 1) elemental evaporation which provided $CuInSe_2$ and $Cu(InGa)Se_2$ films to support the efforts to improve the open circuit voltage and developed improved window layers; and 2) selenization of Cu/In layers which included forming $CuInSe_2$ films from Cu/In layers in either H_2Se or Se.

2.1.1 Two-Step Elemental Evaporation

$CuInSe_2$ films were deposited by elemental vacuum evaporation from Cu, In and Se effusion sources where the incident fluxes are controlled by precisely controlling source temperature. The films are grown by a two step process where both substrate temperature and the incident flux ratio of Cu/In is increased during the deposition as described previously (3). Eight 2.5 x 2.5 cm substrates are coated with $CuInSe_2$ during each deposition. The substrates are typically a combination of 7059 or soda lime glass coated with from 400 nm to 1.0 microns of Mo. One sample from each deposition is processed into devices to verify the quality of the $CuInSe_2$ films. A fourth Ga source in the system was to deposit $Cu(InGa)Se_2$ films with a thin wider bandgap layer.

2.1.2 Selenization of Cu/In Layers in H_2Se/Ar Gas

The emphasis of the research was two-fold: 1) to develop a process to form $CuInSe_2$ films for high efficiency solar cells in a flowing H_2Se/Ar system and characterize the films properties particularly with respect to films grown by elemental evaporation; and 2) characterize the selenization process to develop the fundamental information need for development of large scale systems.

Selenizations of Cu/In layers were carried out in a 2 cm diameter quartz reaction tube shown schematically in Figure 2-1. The 60 cm long tube was heated with a jacket and substrate temperature was controlled to +/- 2°C by a digital programmable controller. A 5.1% hydrogen selenide in argon gas mixture from Matheson Gas Products with a hydrogen selenide purity of no less than 98% was used.

Hydrogen selenide gas mixture and pure (99.999%) argon gas flows were controlled by means of a mass flow controller and rotameter, respectively. The gases passed through a mixing tee prior to introduction into the reaction tube.

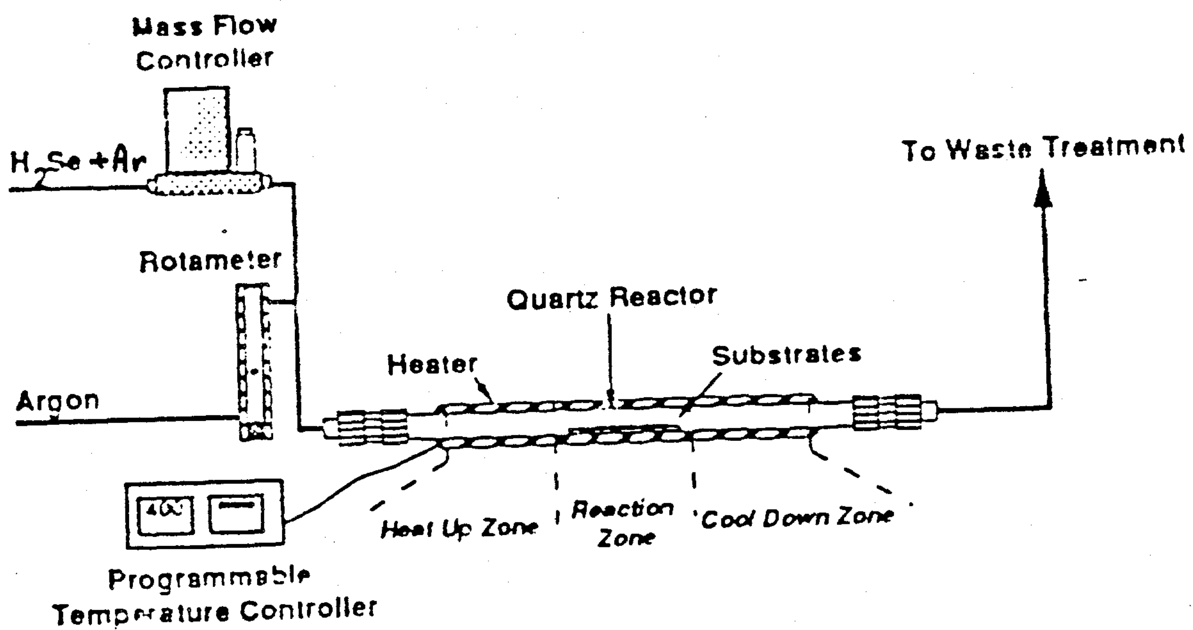


Figure 2-1 Quartz Tube Reaction Apparatus for Selenization

Figure 2-2 depicts the selenization process steps:

- deposition of the Cu/In layers on Mo/glass substrates deposited by e-beam;
- purge or evacuation of the heated tube reactor;
- introduction of a flowing inert gas (usually argon);
- heat up to reaction temperature, often with a hold at an intermediate temperature;
- reaction at 380-450°C in the presence of 3-12% by weight hydrogen selenide in argon;
- purge with argon with an anneal at an elevated temperature for 0-2 hours;
- cool down to room temperature.

The quartz tube reactor has three zones: 1) an entrance region 20 cm long in which gases are heated to reaction temperature and pyrolysis of H_2Se begins; 2) a constant temperature reaction zone 20 cm long in which the substrates are located; and 3) a cool down zone.

Cu/In layers were deposited by e-beam evaporation on both Corning 7059 and soda lime glass substrates coated with Mo and were examined by optical microscopy, SEM/EDS to characterize their morphology and also dissolved in aqua regia to determine absolute amounts of the two metals by AA analysis. XRD was used to investigate the phases present in the as-deposited layers. Cu/In layers were also heat treated and examined by optical microscopy and SEM to evaluate the effect of the heat up process on morphology. XRD was used to identify and follow the progress of the intermixing of the copper and indium.

Selenized copper, indium and Cu/In films were examined by SEM, EDS, optical microscopy, and XRD. Films were also dissolved in aqua regia for AA analysis to determine the uptake of selenium into the films and to evaluate the possible loss of indium selenide species during selenization. Optical reflectance measurements were made to compare the surface texture of the selenized films to evaporated material.

Cu/In layers with molar ratios from 0.8 to 1.1 were selenized under different H_2Se gas concentrations and flows rates at a reaction temperature of 400°C. The composition and structure of the $CuInSe_2$ films were characterized and $(CdZn)S/CuInSe_2$ devices fabricated to determine the best growth parameters for devices $(CdZn)S/CuInSe_2$.

Experiments to investigate the individual steps in the selenization process shown in Figure 2-2 are described below:

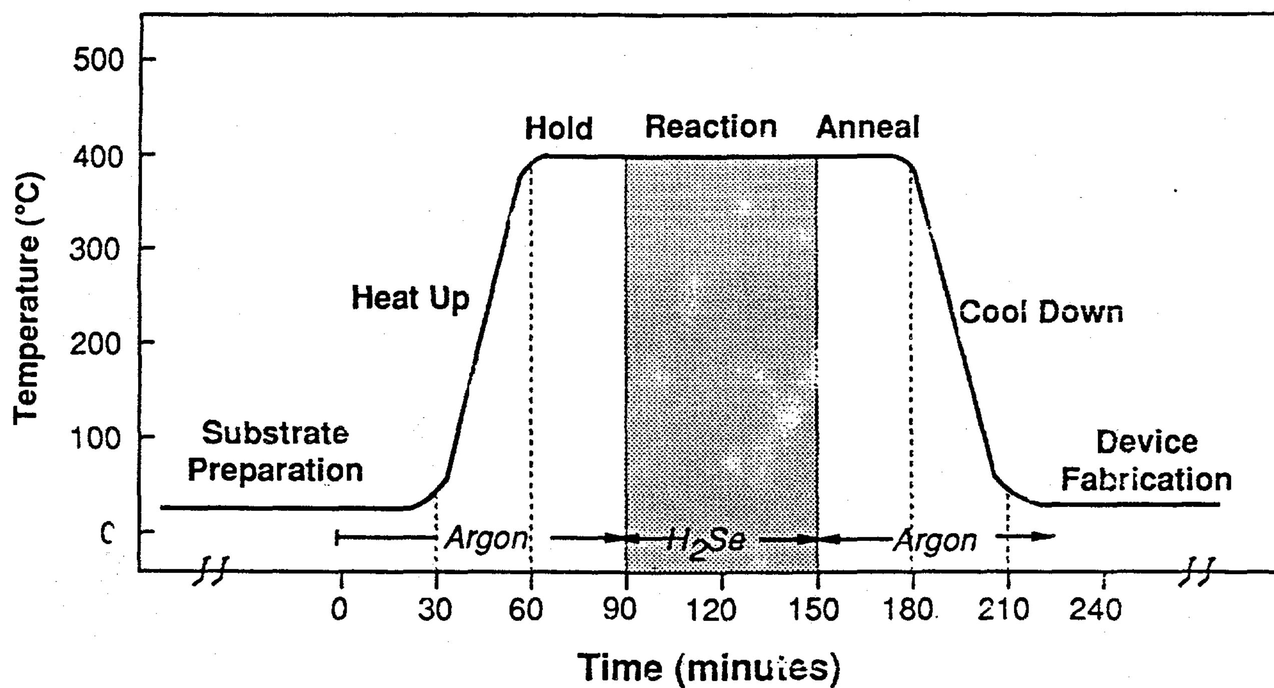


Figure 2-2. Selenization Process Steps

Metal Layer Depositions

Cu/In bilayer films were deposited by electron gun evaporation from 99.999% pure copper and indium sources. Nine one square inch 2 μm Mo-coated glass substrates in a three by three square array, or eighteen 1/2" by 1" substrates were placed into the deposition system at one time. Copper was deposited first, followed by a top layer of indium. Films selenized from Cu on In layers did not adhere to the Mo-coated 7059 or soda lime substrates. The copper to indium atomic ratio was chosen to be between 0.85 and 0.90, since selenized films from this starting material were found to produce high efficiency devices. To achieve a final $CuInSe_2$ film thickness of about 2 μm, copper and indium thicknesses of 2300Å and 5600Å respectively were chosen.

Based on AA analysis, the copper deposition process was found to be controllable to within +/- 4.7% for the 2300Å films. The indium deposition process for 5600Å films was found to be controllable to within +/-2.5%. For a target copper to indium ratio of 0.90, the actual ratio was found to be in the range of 0.85 to 0.95, corresponding to a control over the ratio of +/-5.5%. Thicknesses of the films were verified using optical interferometry and surface profilometry.

For single layer films, the copper layer was observed by SEM and optical microscopy to be smooth and specular. On the other hand, the indium layers usually appeared rough, with droplets or connected pools of indium approximately 10 μm across. Figure 2-3 is an SEM micrograph of a Cu/In bilayer. XRD of as-deposited Cu/In bilayers showed the presence of some intermetallic Cu/In phases in addition to the pure metals.

Cu/In Heat Treatments

The copper-indium phase diagram shows that at 400°C, a solid consisting of approximately 40% indium and 60% copper co-exists with a liquid phase consisting of approximately 90% indium. During hot stage optical microscopy, we observed the formation of liquid and solid phases at temperatures between 150°C and 450°C. Heat treatments of the Cu/In bilayers on glass and Mo-coated glass substrates were performed in 200 sccm of flowing argon at temperatures between 300°C and 450°C for times as short as 1.5 minutes and as long as 8 hours. The irregular, connected structure of the indium layer was preserved for heat treatments of up to two hours at 400°C. XRD patterns of films heat treated for 15 minutes at 400°C showed no pure copper but a pure indium metal phase. For most of the heat treated films, the XRD patterns could be related to one or more of the established Cu/In intermetallic phases (e.g. Cu_9In_4, Cu_4In). After about one hour at 400°C, the XRD patterns of the films stabilized indicating that an equilibrium was reached between copper and indium as one expects from the phase diagram.

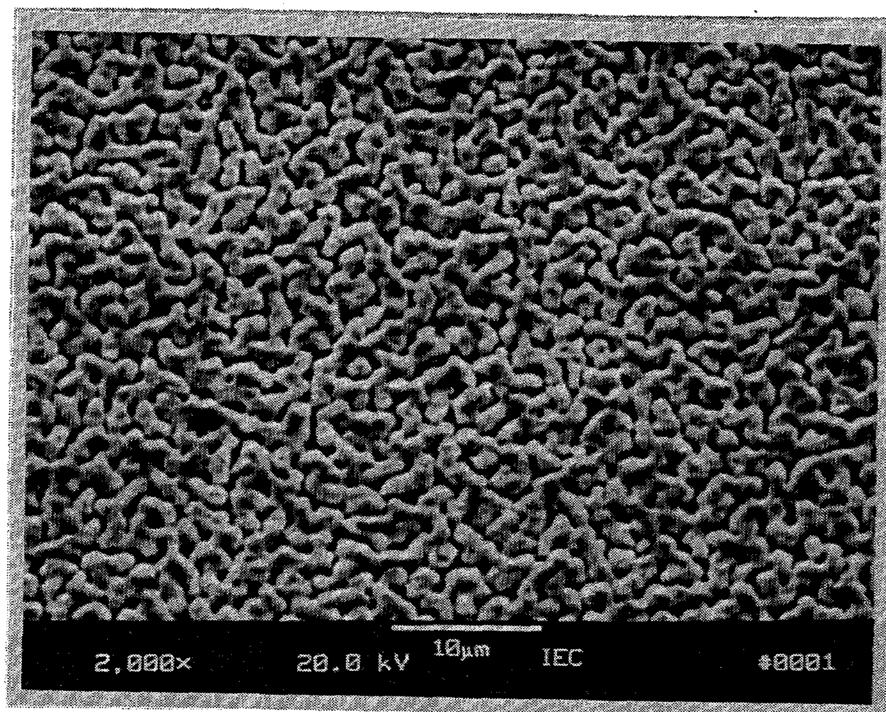


Figure 2-3. SEM micrograph of an as deposited Cu/In bilayer.

The results of heat treatments at lower (300°C) and higher (450°C) temperatures were qualitatively similar to those at 400°C. At 300°C, XRD results after 120 minutes showed little change, while the same was true after 15 minutes at 450°C. Atomic absorption analyses of heat treated copper/indium bilayers showed no measurable loss of indium due to the heating process.

Selenizations of Copper and Indium Single Layers

Copper and indium layers on Mo-coated glass substrates were selenized by placing four 1/2"x 1 substrates in the quartz tube reaction system (Figure 2-2). Reaction temperature was 380°C, 400°C or 420°C. Reaction time was varied from 1.5 minutes to 2 hours. Heat up to reaction temperature was accomplished in about 30 minutes. After holding for 2 to 3 minutes at the reaction temperature, a hydrogen selenide/argon gas mixture was introduced into the reactor at a flow rate of 35 to 75 sccm. Since the substrates were placed halfway along the axis of the 60 cm long reaction tube (at the midpoint), the hydrogen selenide gas would be expected to reach the substrates in about one minute.

Residence time distribution experiments on the reaction system with injections of trace amounts of He in a flowing argon stream indicate that axial dispersion will reduce this time by about 50%. For an estimated hydrogen selenide diffusivity of 0.4 cm^2/second, the Peclet number based on the length of the reactor is about 30. This supports the observation that axial dispersion will play a role in determining the actual concentration of hydrogen selenide at the substrates as a function of time. A best estimate of the time it took for the gas to reach the substrates is thirty seconds. We further expect that the gas concentration would be generally uniform across the tube cross-section as the characteristic time for radial diffusion process is on the order of a few seconds, while the characteristic time for axial convection is about 30 seconds.

Once the desired reaction time was reached, the hydrogen selenide gas flow was stopped and the reactor was quickly purged with 2000 sccm of flowing argon. The films were allowed to cool to room temperature in 30 minutes. Faster cooling of the films often resulted in peeling from the substrates.

Figure 2-4a shows the results of selenizations of 2000Å copper layers on Mo-coated glass for increasing reaction time. (This figure is a corrected version of that used as Figure 2-4a in reference (4). Re-evaluation of the data indicated that the Cu thickness was incorrect due to the calibration of the AA spectrometer. The data was corrected based on XRD results of the film selenized for 20 min. which indicated that it was entirely converted to $Cu_{2-x}Se$. Thus, the actual Cu thickness could be estimated.) These experiments were performed in 2.6 mole% by weight hydrogen selenide in argon at 400°C.

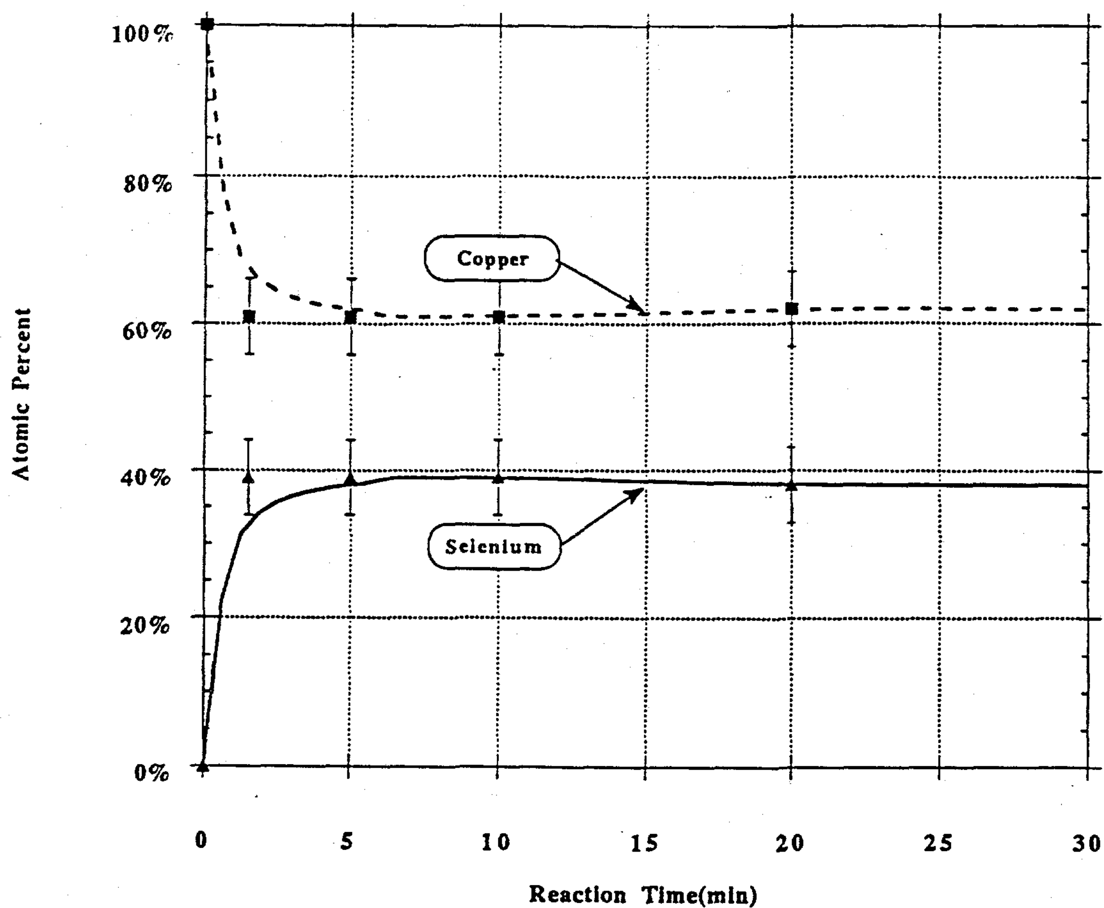


Figure 2-4(a) Atomic Composition during Copper Selenization

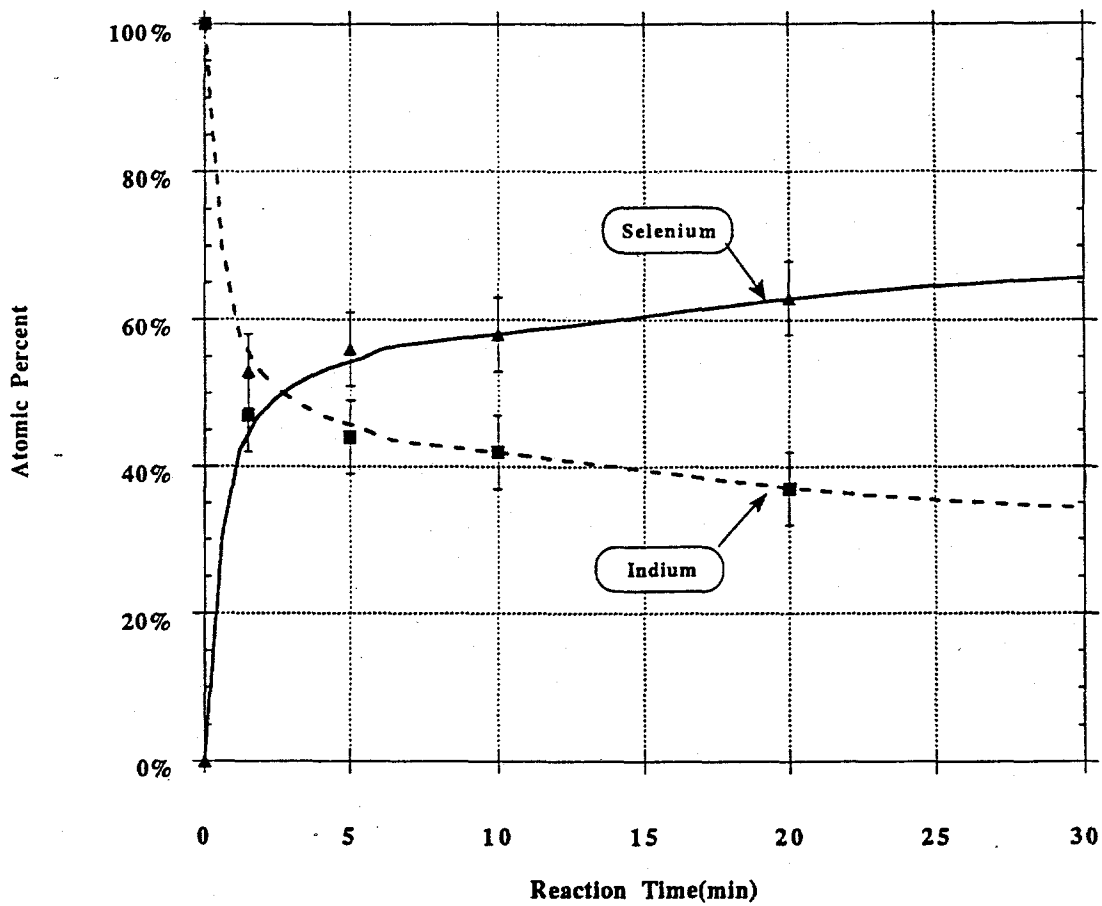


Figure 2-4(b) Atomic Composition during Selenization

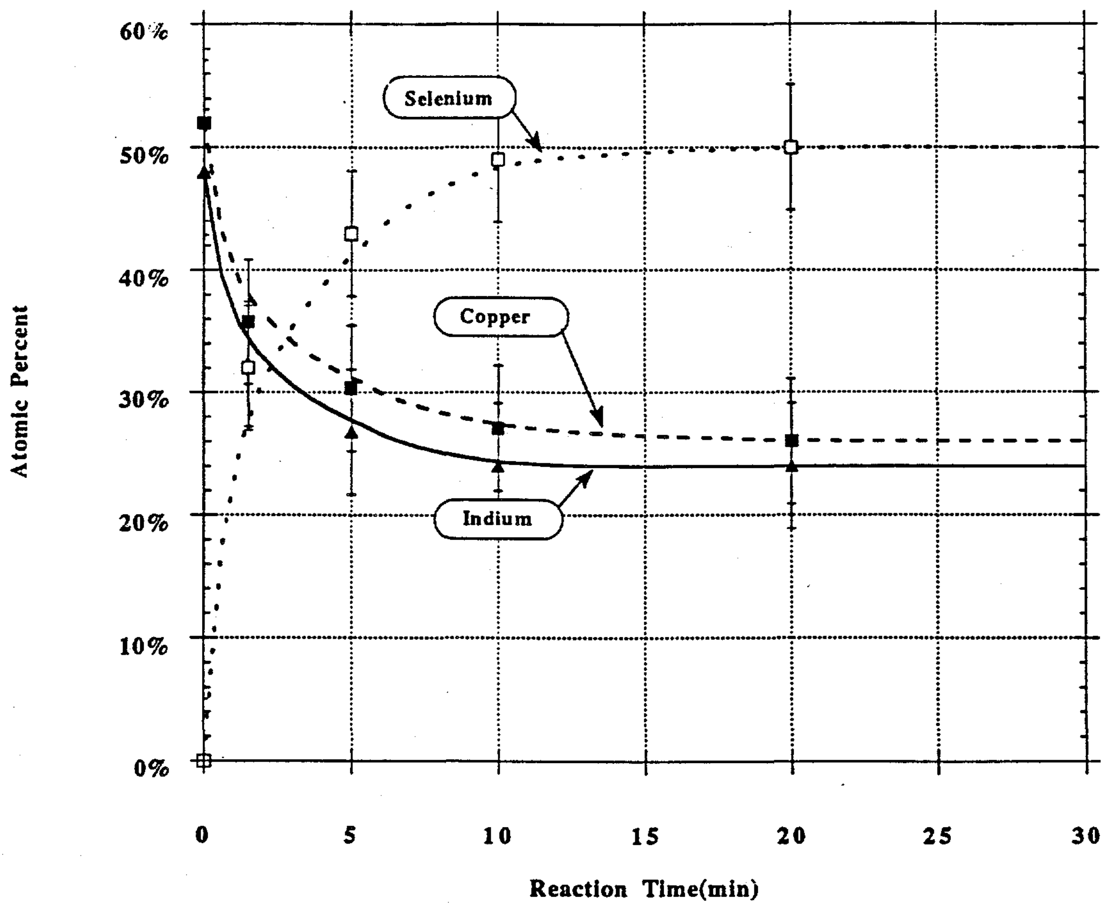


Figure 2-4(c) Atomic Composition during Bilayer Selenization

XRD evaluations of the selenized copper films indicated the presence of a $Cu_{2-x}Se$ (JCPDS Card 6-680) compound for reaction times greater than 5 minutes. Figure 2-5a is an SEM micrograph of a selenized copper layer. The grain size of the selenized copper films is about 1-2 μm. The films were generally uniform over the substrates.

Figure 2-4b shows the results of selenizations of 5000Å of indium layers for increasing reaction times. These experiments were also performed in 2.6 mole % by weight hydrogen selenide at 400°C. As indicated in the figure, the rate of incorporation of selenium into the film slows after 15 minutes. XRD evaluations of the selenized indium reveal the presence of In and In_2Se_3 phases in the earlier stages, with eventual conversion to hexagonal β-In_2Se_3 (JCPDS Card 20-494) after 20 minutes. The final composition of the selenized indium layers is in close agreement with that expected for In_2Se_3. Figure 2-5b depicts an SEM micrograph of a typical selenized indium layer. In general, the selenized indium films appeared irregular, with no discernable grain structure or size.

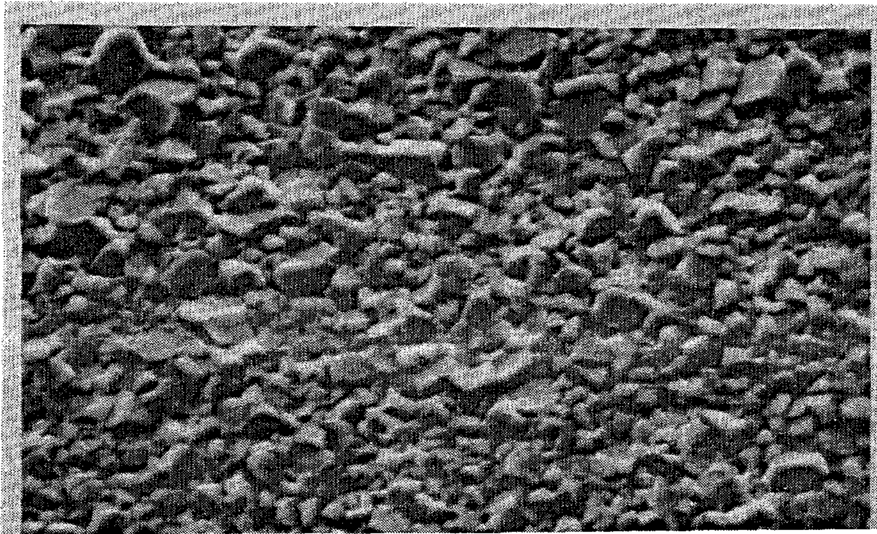
Selenizations of Cu/In Bilayers

At the reaction temperatures of interest, H_2Se can dissociate by pyrolysis to form H_2 and selenium species, primarily Se_2 according to: $2\ H_2Se \longrightarrow 2H2 + Se_2$

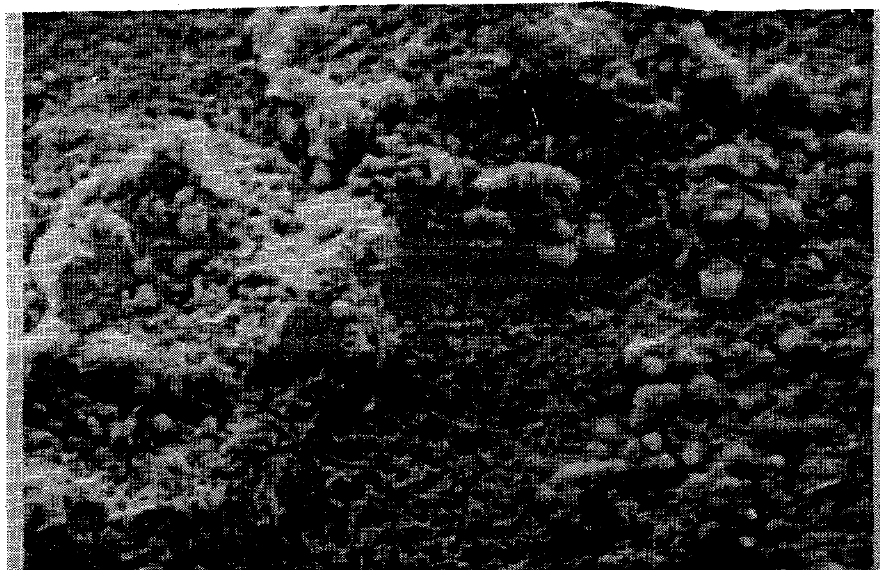
Figure 2-4c shows the results of selenization of a Cu/In bilayer consisting of 2300Å of copper and 5600Å# of indium for increasing reaction times. (This figure is a corrected version of that used as Figure 2-4c in reference ?. Re-evaluation of the data indicated that the Cu thickness was incorrect due to the calibration of the AA spectrometer. The data was corrected based on the $CuInSe_2$ film composition of the Cu/In film composition of the Cu/In layer selenized for 20 min.) The progress of the selenization reaction as measured by increasing incorporation of selenium into the film appears to be essentially complete within 15 to 20 minutes.

XRD evaluations of these films after cooling revealed the presence of In_2Se_3 almost from the onset of the process. Some matches to copper selenides patterns (CuSe, Cu_2Se, and $Cu_{2-x}Se$) were present from the onset as well. $CuInSe_2$ peaks were detected as early as three minutes into the selenization, with the entire XRD pattern coinciding with single phase $CuInSe_2$ by 30 minutes. Although the final selenium content of the film is shown to be about 52%, EDS analyses indicated a selenium content of about 50%. The excess selenium measured by atomic absorption is believed to be associated with selenization of the exposed molybdenum edges of the film. This observation is also applicable to the selenization of single layers.

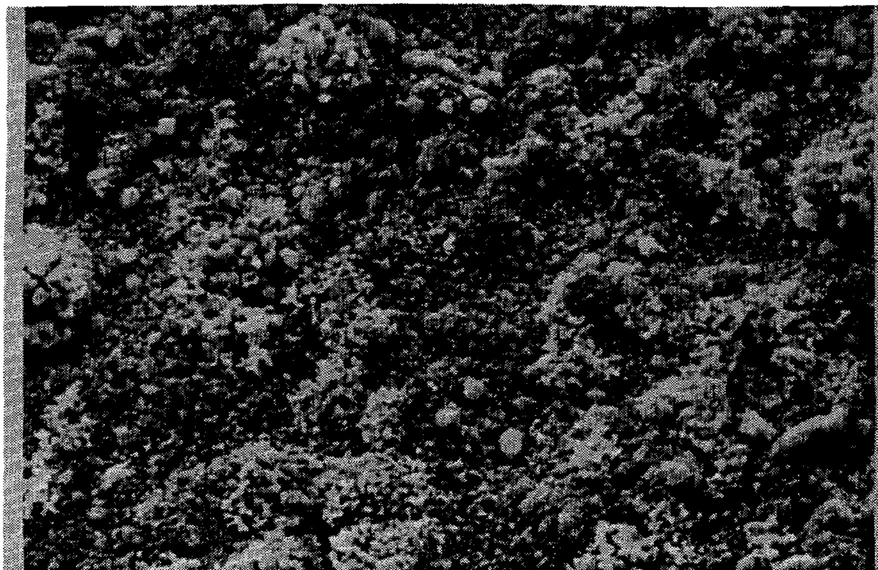
Figure 2-5c shows an SEM micrograph of a selenized Cu/In layer on 2 μm Mo-coated soda lime glass. As with the selenized copper



(a)



(b)



(c)

Figure 2-5. SEM micrographs of selenized layers (a) copper, (b) indium, and (c) Cu/In bilayer (10 μm marker shown).

layer, the grain size appears to be about 1-2 μm. The films were uniform over the entire 2 square centimeter substrate.

Cu/In layers were selenized in the flowing H_2Se reactor to evaluate $CuInSe_2$ films for devices. The best cells were made on $CuInSe_2$ films grown from Cu/In layers with molar ratios from 0.85 to 0.95 that were selenized in flowing H_2Se (3.43% by weight)/Ar at 400°C for 30 to 70 minutes. Table 2-1 summarizes the I-V results for these cell from each piece with efficiencies over 6%. It should be noted that the device with the highest V_{oc} was made using thin solution grown CdS. With the exception of two samples, the starting Cu/In layers were from the same e-beam deposition. The control of the Cu/In layer deposition appears to be critical for achieving high efficiency $CuInSe_2$ devices. Currently our procedure for selecting substrates is to evaluate the Cu/In ratio by AA and examine surface structure by both optical and SEM microscopy. These results are then correlated with EDS and SEM analysis after selenization.

Table 2-1
Best Cell Results Using Selenized $CuInSe_2$ Films

Cell #	V_{oc}	J_{sc}	FF
81111.1	.392	33.4	66.7
81124.0*	.423	30.9	66.4
81076.1	.375	32.7	64.3
82210.2	.365	32.7	59.3
81076.1	.350	32.8	60.1
81110.2	.394	32.5	52.1
81115.1	.383	30.4	46.7

* solution grown CdS

Twenty-seven Cu/In samples, 8 of which were from the same Cu/In e-beam deposition, were selenized under identical growth conditions in the reactor and were then made into $CuInSe_2$/CdS devices to evaluate the reproducibility of the process. From 1 to 6 cells were fabricated on each sample. Out of these samples only 7 samples had an <u>average</u> fill factor greater than 40%. The rest were categorized as shorted or open depending on the slope of the I-V characteristic. The samples with "live cell" had J_{sc} ~ 30 mA/cm^2 and V_{oc} ~ 0.37V. The lack of reproducibility is associated with; 1) the integrity of the glass to metal seal to the reactor tube, which can allow air to enter the system during film growth and 2) variability in the Cu/In ratio of the starting substrate and 3) defect structures in the Cu-In layers formed during the e-beam deposition.

2.1.3 Selenization of Cu/In layers using elemental Se

An alternative way of selenizing Cu-In layers using Se vapor in a vacuum system is being developed. The selenization process consists of the following: 1) 1 micron of Se is deposited by thermal evaporation with no intentional heating of the substrates 2) the samples are then heated to an intermediate reaction temperature in the presence of Se vapor for nominally 15 min 3) the samples are heated to 400°C in the presence of Se and reacted for 1 hr. and 4) the samples are cooled to room temperature (~3 hr.). Substrates with Cu:In ratios from 0.9 to 1.2 were selenized using this approach and an intermediate temperature of 250 C. Single phase CIS films were confirmed with XRD and in Table 2-2 the composition of the $CuInSe_2$ films are summarized.

Table 2-2
Composition of Selenized Cu/In Layers

Cu/In	Cu	In	Se	
0.9	25.3	25.2	49.5	
0.91	24.6	25.6	49.8	
1.05	25.2	25.0	49.8	
1.06	25.1	24.8	49.7	(soda lime)
1.22	28.2	24.5	47.4	

Devices were made on all samples, but the cells had poor performance or were shorted with the exception of the sample on soda lime glass (all others were on 7059 glass) and the best device had an efficiency of over 7% with V_{oc}= 0.378V, J_{sc}=29.9 mA/cm^2, and FF=55.2%. Based on these encouraging results work will continue on the method during the coming year.

2.2 $CuInSe_2$ CELL ANALYSIS AND V_{oc} IMPROVEMENT

2.2.1 Introduction

Analysis of $CuInSe_2$/(CdZn)S cells has shown that they are dominated by Shockley-Read-Hall (SRH) recombination in the space charge region, where p~n, and the barrier height is equal to the bandgap of the absorber, 1.0eV (3). Therefore, the recombination can be reduced and V_{oc} increased by increasing the bandgap of the absorber in the space charge region or by reducing the depletion width. To increase the bandgap, thin $Cu(InGa)Se_2$ layers were deposited on $CuInSe_2$ films and cells were fabricated. If the higher bandgap layer is thin enough compared to the space charge width, a barrier to photogenerated carriers should have a very small effect on the fill factor and J_{sc} (5). Preliminary results showed that V_{oc} can be increased this way while generating carriers out to the $CuInSe_2$ band edge (7). However, the cells had low J_{sc} and FF, and spectral

response measurements indicated that the (CdZn)S became very photoconductive in these cells.

During the current reporting period, several modifications to the deposition of the $CuInSe_2$, $Cu(InGa)Se_2$, and (CdZn)S layers have been made in an attempt to improve the cell performance. However, the problems mentioned above remain. In addition, results will be reported for cells with Ga deposited at the Mo/$CuInSe_2$ interface. Finally, analysis of the current mechanisms limiting V_{oc} in $CuInSe_2$ cells has continued. Results show that the cells have a range of diode A-factors, from 1.2 to >2, which cannot be described by a simple SRH model. Alternatives which also take into account observed variations in I-V data with intensity or current are being evaluated.

2.2.2 Bandgap Modified Cells

$CuInSe_2$/$Cu(InGa)Se_2$ films have been deposited by thermal evaporation using four elemental effusion sources. $CuInSe_2$/$Cu(InGa)Se_2$/(CdZn)S cells with the bandgap modified in the space charge region were fabricated as described previously [3]. Two deposition sequences were used in the present work: 1) a thin $Cu(InGa)Se_2$ layer was deposited in a second evaporation on completed $CuInSe_2$ films which were re-inserted in the evaporator; and 2) a surface layer was produced with a single three step evaporation which included standard Cu-rich and Cu-poor $CuInSe_2$ layers deposited at a substrate temperature T_{ss}=300 and 450°C immediately followed by a thin $Cu(InGa)Se_2$ layer deposited at T_{ss}=350 or 450°C.

Using the first sequence in which the $Cu(InGa)Se_2$ films are deposited on completed $CuInSe_2$ films, a range of film parameters and deposition conditions were evaluated. These included varying the $Cu(InGa)Se_2$ thickness from 0-0.4μm, the composition from ~20-25 %Cu, and T_{ss} during the $Cu(InGa)Se_2$ deposition from 300-500°C. The $Cu(InGa)Se_2$ layer thicknesses were determined with a Dektak profilometer on witness pieces deposited on glass. Since the composition of the $Cu(InGa)Se_2$ layers was difficult to determine due to their thinness, a thicker layer (1.5μm) was deposited at 450°C using the same source temperatures. The composition of the 1.5μm thick film was measured by atomic absorption spectroscopy and found to be: 24% Cu, 19% In, 7.5% Ga, and 49% Se. Lower Cu compositions were achieved by reducing the Cu source temperature while holding all other parameters fixed during the $Cu(InGa)Se_2$ deposition. The Ga content was determined from cells made on witness pieces with just the thin $Cu(InGa)Se_2$ layers deposited on Mo. While these cells generally had poor diode characteristics the long wavelength edge of the spectral response was used to determine the bandgap and, using the data of Dimmler et al. (7), the ratio Ga/(In+Ga).

The Cu, In, Ga, and Se composition profiles for three $CuInSe_2$/$Cu(InGa)Se_2$ layers were determined by SIMS measurements

done by Sally Asher at SERI. The data shows that films deposited by the two evaporation sequence, in which the $CuInSe_2$ film is re-inserted into the evaporator for the $Cu(InGa)Se_2$ deposition, with the $Cu(InGa)Se_2$ layers ~1200Å and ~400Å thick, respectively, have a well defined Ga rich region at the surface. After this surface layer the Ga count falls off rapidly and is reduced by more than 2 orders of magnitude after 0.5μm sputtering depth. The profile for a sample with the $CuInSe_2/Cu(InGa)Se_2$ layers deposited in the single 3 step evaporation sequence still shows a clearly defined Ga rich layer, but a much higher Ga content in the bulk $CuInSe_2$ due to Ga diffusion during the deposition process.

For devices, $CuInSe_2/Cu(InGa)Se_2$ layers were deposited on glass/Mo substrates. Evaporated In-doped (CdZn)S films with thickness ~1.5 μm, 0-15% Zn, and sheet resistance ≈ 50Ω/■ were deposited on $CuInSe_2/Cu(InGa)Se_2$. Devices in a substrate configuration were completed with sputtered ITO and Ni contacts. Previously, I-V results were given for cells with three thicknesses of 1.15 eV bandgap $Cu(InGa)Se_2$ layers (6). With the $Cu(InGa)Se_2$ layer 0.4μm thick, V_{oc} was close to that of a cell with uniform $Cu(InGa)Se_2$ but J_{sc} was much smaller. As the $Cu(InGa)Se_2$ layer thickness was reduced, V_{oc} decreased and J_{sc} increased. Since V_{oc} is limited by recombination in the space charge region, the reduction in V_{oc} indicates that the layer thickness was less than the space charge width. In all cases, the cells had low fill factors.

Figure 2-6 shows the J-V characteristics for a cell with the $CuInSe_2/Cu(InGa)Se_2$ layers deposited in two evaporations with a ~400Å thick $Cu(InGa)Se_2$ layer and Ga/(In+Ga)≈25%. The curves are shown after 8 and 24 hours total heat treatment in air at 200°C. After 24 hours, with the voltage maximized, the cell had V_{oc}=0.44V, J_{sc}=27mA/cm^2, and FF=27%. The inflection point in the power quadrant of the J-V curve suggests that there is a barrier in the conduction band at the $CuInSe_2/Cu(InGa)Se_2$ interface. As the forward bias voltage is increased minority carriers generated deeper in the bulk $CuInSe_2$ will be blocked by this barrier and only carriers generated in the $Cu(InGa)Se_2$ layer will be collected. After only 8 hours heat treatment V_{oc} was not maximized which indicates that the $CuInSe_2$ is more resistive and, therefore, the space charge width is greater (8). As a result, a barrier to minority carrier collection will have less effect on the collection so J_{sc} and FF are increased, particularly in the long wavelength response. In addition, the low FF may be due to a smaller diffusion length when Ga is present. Similar behavior was reported by Klenk et al. (9) for $Cu(InGa)Se_2$ cells in which the resistivity was increased by hydrazine treatment and by Tuttle et al. (10) for $CuInSe_2/Cu(InGa)Se_2$ cells.

The spectral response for the same $CuInSe_2/Cu(InGa)Se_2$ cell is shown in Figure 2-7 at 0V and -1V bias voltage and under ELH bias illumination. The long wavelength response is strongly voltage dependent, as expected for the low J_{sc} and FF. The spectral response and J-V measurements also show that the (CdZn)S layer has become highly resistive and photoconductive after processing.

The high resistance layer of (CdZn)S has been identified by spectral response and light and dark J-V measurements. The light-dark crossover of the J-V characteristics indicate light dependent changes in electric field and current collection mechanisms. The photoconductive peak near the (CdZn)S band edge in the spectral response with 0V bias identifies the (CdZn)S layer as the cause of the light induced changes (11). The high resistance (CdZn)S alters the electric field distributions in the active $CuInSe_2/Cu(InGa)Se_2$ layers, so the effects of the addition of the $Cu(InGa)Se_2$ cannot be separated from that of the (CdZn)S. Hence, it has not been determined which parts of the changes in J_{sc}, FF and spectral response are caused by the high resistance (CdZn)S layer and what parts are caused by the $Cu(InGa)Se_2$ layer.

The described behavior of these $CuInSe_2/Cu(InGa)Se_2$ cells has been observed despite any variations in deposition conditions.
Cell results for cells with ~1200Å thick $Cu(InGa)Se_2$ layers deposited at T_{ss}=300-500°C and with ~20 and ~24% Cu are shown in Table 2-3. In each case, the cells had low fill factors due to highly resistive (CdZn)S. The same effects were seen for different thickness $Cu(InGa)Se_2$ layers. However, a cell fabricated with the same two evaporation sequence but with no Ga in the second evaporation did not have the highly photoconductive (CdZn)S. Also, increasing the indium doping level or eliminating the Zn in the (CdZn)S to increase the as-deposited conductivity had little or no effect. Finally, it was determined that the resistive (CdZn)S layer is not present when a cell is made with a homogeneous $Cu(InGa)Se_2$ layer.

Cells were also fabricated from $CuInSe_2/Cu(InGa)Se_2$ layers deposited in a single three step deposition. The best cell from this deposition sequence had V_{oc}=0.428mV, J_{sc}=29.1mA/cm^2, FF=46% and 6.6% efficiency. A control piece was made, using a shutter in the evaporator, with just the $CuInSe_2$ layer on one half and just the thin $Cu(InGa)Se_2$ layer on the other. The best standard $CuInSe_2$/CdS cell made on this piece had only V_{oc}=0.38V, J_{sc}=29.4mA/cm^2, FF=64% and 8.2% efficiency. Cells were also made with just the thin $Cu(InGa)Se_2$ as the absorber and again used to determine the Ga/(Ga+In) content which was 31%. This single evaporation process for depositing $CuInSe_2/Cu(InGa)Se_2$ layers has not given a significant increase in V_{oc} compared to typical $CuInSe_2$ cells regardless of changes in T_{ss} or composition of the $Cu(InGa)Se_2$ layer. In addition, the spectral response shows a small shift in the long wavelength edge indicating that some Ga had diffused throughout the absorber layer consistent with the SIMS results.

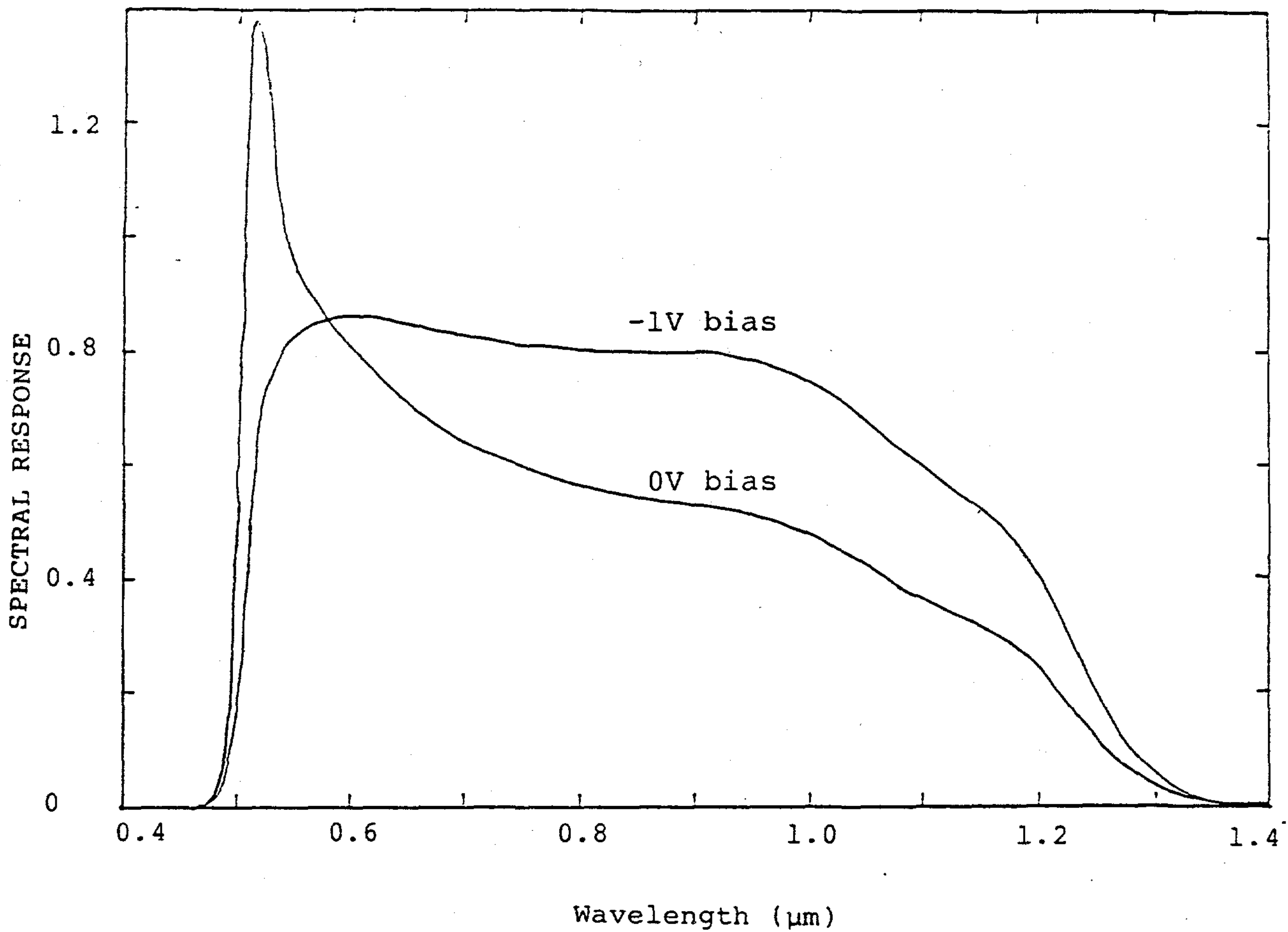


Figure 2-7. Spectral response measured under ELH bias illumination of the same $CuInSe_2/Cu(InGa)Se_2$ cell. The peak in the response at 0V indicates that the (CdZn)S is highly photoconductive.

Table 2-3
Cu(InGa)Se2/CuInSe2 Cell Results

$CuInSe_2$	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	eff (%)	T_{ss} (°C)	Comp.	%Ga	Window
32139.22 (CdZn)S:In	0.461	16.4		29.8	2.57	300	low Cu	25
32139.23 (CdZn)S:In	0.463	13.8		35.4	2.59	300	high Cu	25
32141.12 (CdZn)S:In	0.441	25.3		28.4	3.61	400	low Cu	27
32141.22 CdS:In	0.456	21.9		29.5	3.37	400	high Cu	31
32171.23 CdS:In	0.368	15.2		41.0	2.62	500	low Cu	32
32171.22 CdS:In	0.382	21.1		43.3	3.98	500	high Cu	31

This results in an additional loss in J_{sc} compared to a standard $CuInSe_2$ cell. The fill factor was again low indicating a barrier in the conduction band and/or a poor diffusion length due to the addition of $Cu(InGa)Se_2$. Finally, these cells also had a highly resistive and photoconductive (CdZn)S layer. Therefore, the photoconductive (CdZn)S only occurs when there is a Ga gradient in the absorber layer but is not caused by removing the $CuInSe_2$ layer from the evaporator before the $Cu(InGa)Se_2$ deposition. A more detailed analysis of the junction is underway to see if this effect might be inherent in the specific device design.

2.2.3 Ga/$CuInSe_2$ Cells

A thin ~200Å equivalent layer of Ga incorporated into the back of the Cu layer in Cu/In layers used for selenization has been reported to increase V_{oc} by as much as 40 mV (12). It was reported that Auger analysis of these devices showed that the Ga did not diffuse all the way through the $CuInSe_2$ layer during the selenization process. Initial experiments were done to evaluate the effect of a thin Ga layer deposited at the back of $CuInSe_2$ layers deposited by three source evaporation. Ga layers ~200Å thick were deposited by open boat evaporation onto glass/Mo substrates which were subsequently used as substrates for standard two layer $CuInSe_2$ depositions. Cells were then fabricated on these layers with evaporated CdS:In/ITO window layers. I-V results are compared to control pieces from the same $CuInSe_2$ deposition in Table 2-4 for cells with soda lime and 7059 glass substrates. In each case no improvement in V_{oc} or cell performance was achieved with the Ga layers. Ga/$CuInSe_2$ have also been fabricated with the Ga deposited in the $CuInSe_2$ evaporator at the beginning of a standard $CuInSe_2$ deposition. In this case the best cell had V_{oc}=0.38V, J_{sc}=28mA/cm^2, FF=62%, and efficiency=7.4%. The effect of incorporating a thin Ga layer at the back of the $CuInSe_2$ for a selenization process, in which improved adhesion may also be beneficial, will be evaluated in the future.

2.2.4 I-V Device Analysis

2.2.4.1 Introduction

Detailed analysis of the current-voltage behavior of high efficiency $CuInSe_2$/(CdZn)S cells can determine the mechanisms limiting V_{oc} and efficiency and suggest improvements. Previous analysis and modeling has indicated that the primary mechanism controlling these devices is Shockley-Read-Hall (SRH) recombination in the space charge region of the $CuInSe_2$ (3,13). The current-voltage (J-V) relation was described by a standard diode model with a barrier height equal to the $CuInSe_2$ bandgap, 1.0eV, and a diode A-factor ~2.

Table 2-4. Glass/Mo/Ga/$CuInSe_2$ Cell Results

$CuInSe_2$	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)	Ga (μm)	Substrate
32186.23	0.363	29.7	50.9	6.26	200	7059
32186.21	0.360	28.0	48.7	5.61	none	7059
32188.22	0.402	31.0	63.0	8.97	200	soda lime
32188.21	0.408	30.0	61.8	8.64	none	soda lime

In the present work, J-V measurements of high efficiency evaporated $CuInSe_2$/(CdZn)S solar cells as a function of light intensity and temperature are presented, as well as analysis of the illuminated J-V characteristics for many cells. The results show that the A-factor varies from 1.2 to 2 depending on the device and also varies as a function of light intensity. This indicates that a more comprehensive model of the diode mechanisms is necessary. The results will be discussed in terms of two models: 1) an admixture of currents controlled by Shockley-Read-Hall (SRH) recombination in the space charge region of the $CuInSe_2$ and recombination through states at the (CdZn)S-$CuInSe_2$ interface, and 2) SRH recombination with a voltage dependent A-factor that depends on the distribution in energy of states within the gap involved in the recombination process.

Standard I-V Analysis

In order to better analyze the standard I-V tests done on solar cells, IEC has begun recording two additional measurements besides the standard V_{oc}, J_{sc}, V_{MP}, and J_{MP}. These are $(dJ/dV)=G_{sc}$ at $J=J_{sc}$ and $(dV/dJ)=-R_{oc}$ at $V=V_{oc}$. Using these additional measurements allow us to 'curve fit' the I-V characteristic in the active quadrant. The 'curve fitting' equation is:

$$J+GV=J_L-J_o[\exp(\alpha(V+RJ))-1]$$

with G, J_L, J_o, α, and R as fitting parameters. The fitting parameters make it much easier to check various models of solar cell behavior against the measurements as well as to allow adjustment of the I-V characteristics to different conditions of illumination and temperature (if the dependency of the parameters are known).

If an A-factor is defined from the above equation as $A\equiv q/\alpha kT$, then the standard I-V testing allows the determination of diode A-factor on all cells tested. Table 2-5 shows this with 97 of the highest

Table 2-5
Averaged device results from high efficiency $CuInSe_2$ cells

# of Cells in sample	Avg. V_{oc} (V)	Avg. Eff.	Avg. FF	Avg. A-factor	Avg. FF_o (R=6=0)
17	0.47	8.8	60	>2	63
20	0.46	9.6	65	1.9	68
20	0.45	9.8	64	1.8	68
20	0.44	10.6	67	1.6	71
20	0.43	10.5	68	1.4	72

efficiency cells whose V_{oc} (normalized to a J_{sc} of $40mA/cm^2$) is grouped between 0.425 and 0.475V. Alongside are the average of the measured efficiencies, measured fill factors, derived diode A-factors, and derived ideal fill factors. As seen, maximum V_{oc} does not lead to either maximum efficiency or maximum fill factor.

J_{sc}-V_{oc} Analysis

Another one of the methods used for this investigation has been to measure J_{sc} and V_{oc} at different temperatures and light intensity. Figures 2-8 and 2-9 show this for 7 temperatures from 242K to 332K. The intensity was varied over 2 orders of magnitude with neutral density filters.

The lines are a fit to the equation:

$$V_{oc}=\phi - (AkT/q)\,Ln(J_{oo}/J_{sc})$$

with A=1.26

$$J_{oo}=1.8x10^{10} \text{ mA/cm}^2$$
$$\phi=1.07 \text{ eV}$$

A closer look at Figure 2-8 shows a definite deviation from linearity in the measured data points. If this is taken into account by allowing the A-factor to vary as a function of I-V bias or light intensity then:

$$A\equiv slope=d(qV_{oc}/kT)/d(LnJ_{sc})$$

This variation is shown in Table 2-6.

J-V curves are shown in Figure 2-10 for the same cell at T=290K in the dark and under ~87.5 mW/cm^2 illumination. This data cannot be represented in terms of simple superposition of the dark current and photocurrent even after corrections for voltage dependent collection and series and shunt losses.

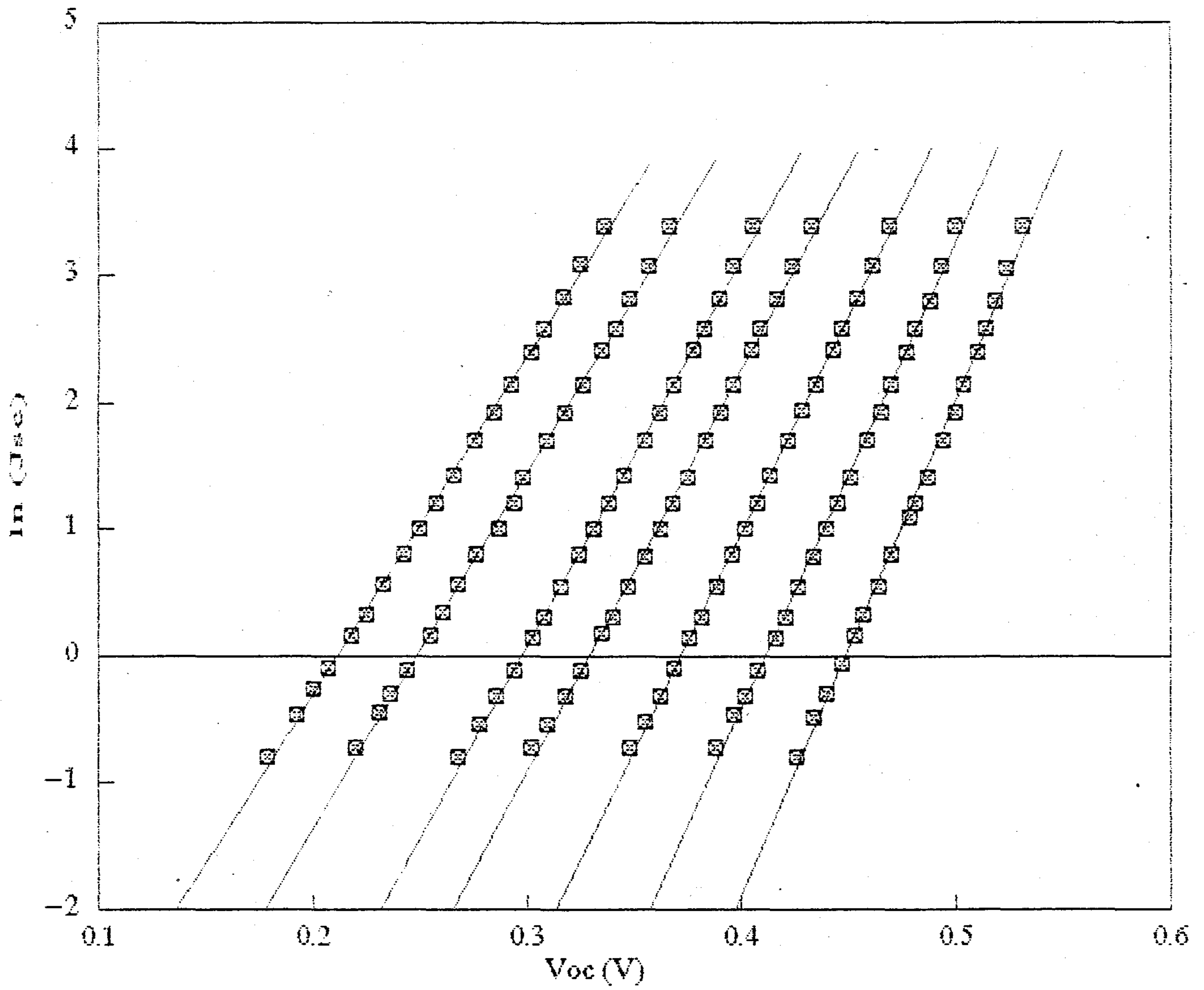


Figure 2-8. $CuInSe_2$/(CdZn)S Cell #32187-22-7 at temperatures 242, 255, 273.5, 290, 302, 318.5, and 332°K.

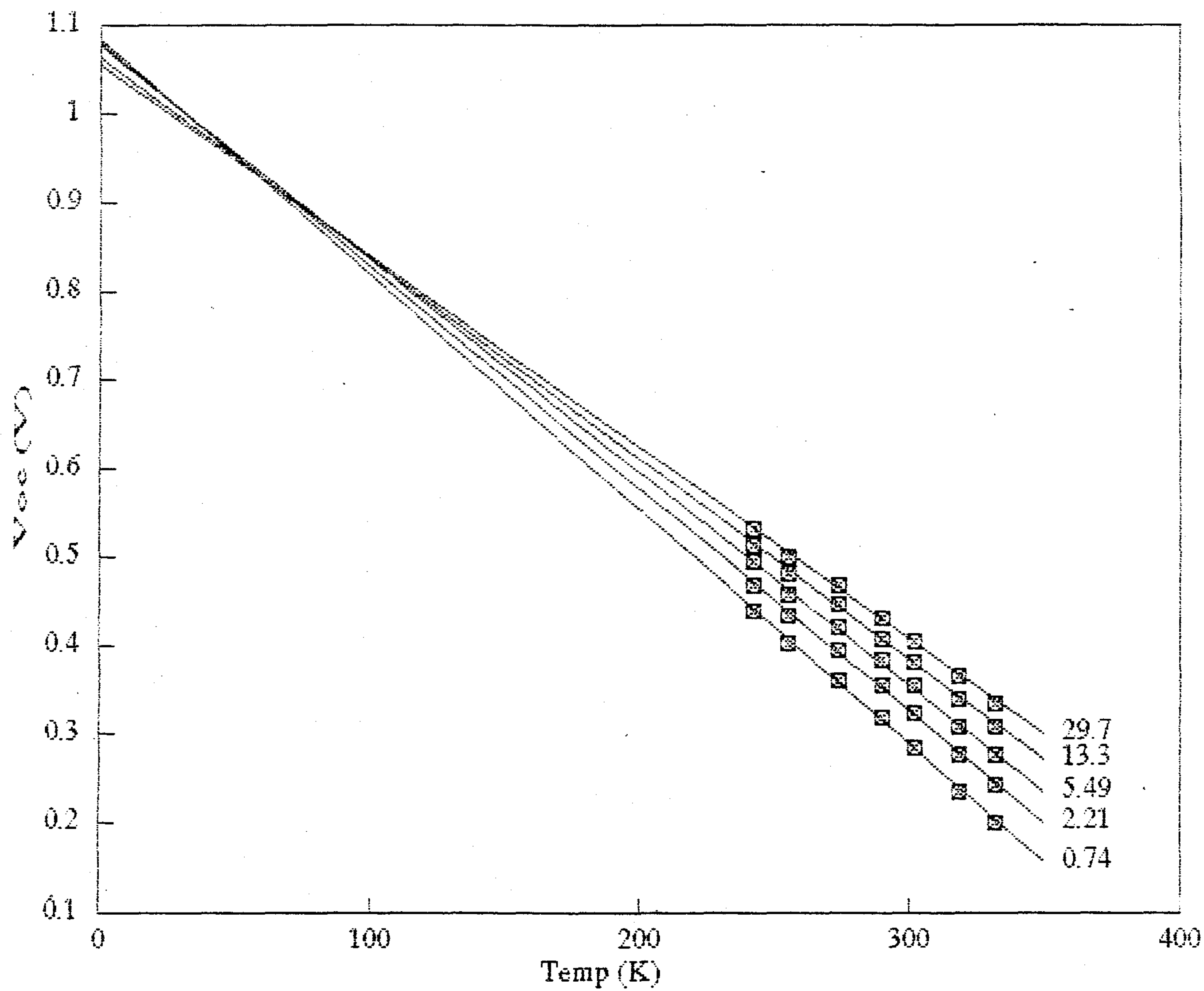


Figure 2-9. $CuInSe_2$ #32287-22-7 V_{oc} vs T at J_{sc}=29.7, 13.3, 5.5, 2.2, and 0.7 mA/cm^2

Table 2-6

J_{sc} vs. V_{oc} Results
$CuInSe_2$ #31287-22-7
T=242.0°K

J_{sc} (mA/cm^2)	V_{oc} (V)	Log(J_{sc})	qV_{oc}/kT	A-factor Slope
29.50	0.532	1.47	25.51	0.98
21.50	0.524	1.33	25.13	1.02
16.63	0.519	1.22	24.89	1.05
13.18	0.514	1.12	24.65	1.07
11.10	0.510	1.05	24.46	1.09
8.46	0.504	0.93	24.17	1.12
6.85	0.500	0.84	23.98	1.15
5.46	0.494	0.74	23.69	1.17
4.10	0.487	0.61	23.35	1.21
3.35	0.481	0.53	23.07	1.23
2.99	0.478	0.48	22.92	1.24
2.21	0.470	0.34	22.54	1.28
1.73	0.464	0.24	22.25	1.30
1.38	0.457	0.14	21.91	1.33
1.17	0.453	0.07	21.72	1.35
0.95	0.447	-0.02	21.43	1.37
0.74	0.440	-0.13	21.10	1.40
0.61	0.434	-0.21	20.81	1.42
0.46	0.426	-0.34	20.43	1.46

T=255.0°K

J_{sc} (mA/cm^2)	V_{oc} (V)	Log(J_{sc})	qV_{oc}/kT	A-factor Slope
29.50	0.500	1.47	22.75	1.03
21.63	0.493	1.34	22.44	1.06
16.63	0.488	1.22	22.21	1.09
13.16	0.481	1.12	21.89	1.11
11.08	0.477	1.04	21.71	1.13
8.48	0.470	0.93	21.39	1.15
6.84	0.465	0.84	21.16	1.18
5.46	0.459	0.74	20.89	1.20
4.11	0.451	0.61	20.52	1.23
3.34	0.445	0.52	20.25	1.25
2.73	0.440	0.44	20.02	1.27
2.20	0.434	0.34	19.75	1.29
1.73	0.427	0.24	19.43	1.32
1.37	0.421	0.14	19.16	1.34
1.16	0.416	0.06	18.93	1.36
0.90	0.408	-0.05	18.57	1.38
0.73	0.402	-0.14	18.29	1.40
0.63	0.397	-0.20	18.07	1.42
0.49	0.388	-0.31	17.66	1.44

$CuInSe_2$ #31267-22-7

T=273.5

J_{sc}	V_{oc}	Log J	qV/kT	Slope
29.75	0.469	1.47	19.90	1.11
21.88	0.461	1.34	19.56	1.13
16.88	0.454	1.23	19.26	1.15
13.30	0.447	1.12	18.97	1.16
11.19	0.443	1.05	18.80	1.17
8.54	0.435	0.93	18.46	1.19
6.91	0.429	0.84	18.20	1.20
5.51	0.422	0.74	17.91	1.22
4.15	0.414	0.62	17.57	1.23
3.35	0.408	0.53	17.31	1.25
2.74	0.402	0.44	17.06	1.26
2.21	0.396	0.34	16.80	1.27
1.74	0.389	0.24	16.51	1.29
1.37	0.382	0.14	16.21	1.30
1.15	0.376	0.06	15.95	1.31
0.91	0.369	-0.04	15.66	1.33
0.73	0.362	-0.14	15.36	1.34
0.59	0.355	-0.23	15.06	1.35
0.49	0.348	-0.31	14.77	1.37

T=290.0

J_{sc}	V_{oc}	Log J	qV/kT	Slope
29.63	0.433	1.47	17.33	1.07
21.63	0.424	1.34	16.97	1.10
16.88	0.417	1.23	16.69	1.12
13.25	0.409	1.12	16.37	1.14
11.16	0.405	1.05	16.21	1.16
8.52	0.397	0.93	15.89	1.18
6.89	0.391	0.84	15.65	1.20
5.49	0.384	0.74	15.37	1.22
4.10	0.375	0.61	15.01	1.25
3.33	0.368	0.52	14.73	1.27
2.71	0.362	0.43	14.49	1.29
2.20	0.355	0.34	14.21	1.31
1.73	0.347	0.24	13.89	1.33
1.35	0.340	0.13	13.61	1.36
1.19	0.335	0.08	13.41	1.37
0.89	0.325	-0.05	13.01	1.39
0.73	0.318	-0.14	12.72	1.41
0.59	0.309	-0.23	12.36	1.43
0.48	0.302	-0.32	12.08	1.45

$CuInSe_2$ #31287-22-7

T=302.0

J_{sc}	V_{oc}	Log J	qV/kT	Slope
29.75	0.406	1.47	15.60	1.13
21.75	0.397	1.34	15.25	1.15
16.88	0.390	1.23	14.99	1.16
13.24	0.383	1.12	14.72	1.18
11.15	0.378	1.05	14.52	1.19
8.52	0.369	0.93	14.18	1.21
6.89	0.362	0.84	13.91	1.22
5.50	0.355	0.74	13.64	1.24
4.14	0.345	0.62	13.26	1.26
3.36	0.338	0.53	12.99	1.27
2.74	0.331	0.44	12.72	1.28
2.22	0.324	0.35	12.45	1.30
1.74	0.316	0.24	12.14	1.31
1.35	0.308	0.13	11.84	1.33
1.14	0.303	0.06	11.64	1.34
0.89	0.294	-0.05	11.30	1.36
0.72	0.286	-0.14	10.99	1.37
0.58	0.278	-0.24	10.68	1.39
0.45	0.268	-0.35	10.30	1.40

T=318.5

J_{sc}	V_{oc}	Log J	qV/kT	Slope
29.88	0.367	1.48	13.37	1.17
21.88	0.357	1.34	13.01	1.19
16.88	0.348	1.23	12.68	1.21
13.25	0.341	1.12	12.42	1.22
11.14	0.335	1.05	12.21	1.23
8.59	0.326	0.93	11.88	1.25
6.90	0.318	0.84	11.59	1.26
5.50	0.309	0.74	11.26	1.28
4.13	0.298	0.62	10.86	1.29
3.36	0.294	0.53	10.71	1.31
2.75	0.287	0.44	10.46	1.32
2.22	0.277	0.35	10.09	1.33
1.75	0.268	0.24	9.76	1.35
1.40	0.261	0.15	9.51	1.36
1.17	0.255	0.07	9.29	1.37
0.89	0.244	-0.05	8.89	1.39
0.74	0.236	-0.13	8.60	1.40
0.64	0.231	-0.19	8.42	1.41
0.49	0.220	-0.31	8.02	1.43

$CuInSe_2$ #31287-22-7

T=332.0

J_{sc}	V_{oc}	Log J	qV/kT	Slope
29.88	0.336	1.48	11.74	1.16
22.00	0.325	1.34	11.36	1.18
17.00	0.317	1.23	11.08	1.20
13.38	0.308	1.13	10.77	1.22
11.06	0.302	1.04	10.56	1.23
8.48	0.293	0.93	10.24	1.25
6.89	0.285	0.84	9.96	1.26
5.48	0.276	0.74	9.65	1.28
4.14	0.266	0.62	9.30	1.30
3.35	0.258	0.53	9.02	1.32
2.74	0.250	0.44	8.74	1.33
2.22	0.243	0.35	8.49	1.35
1.75	0.233	0.24	8.14	1.37
1.39	0.225	0.14	7.86	1.38
1.17	0.218	0.07	7.62	1.40
0.91	0.207	−0.04	7.24	1.42
0.76	0.200	−0.12	6.99	1.43
0.63	0.192	−0.20	6.71	1.44
0.45	0.178	−0.35	6.22	1.47

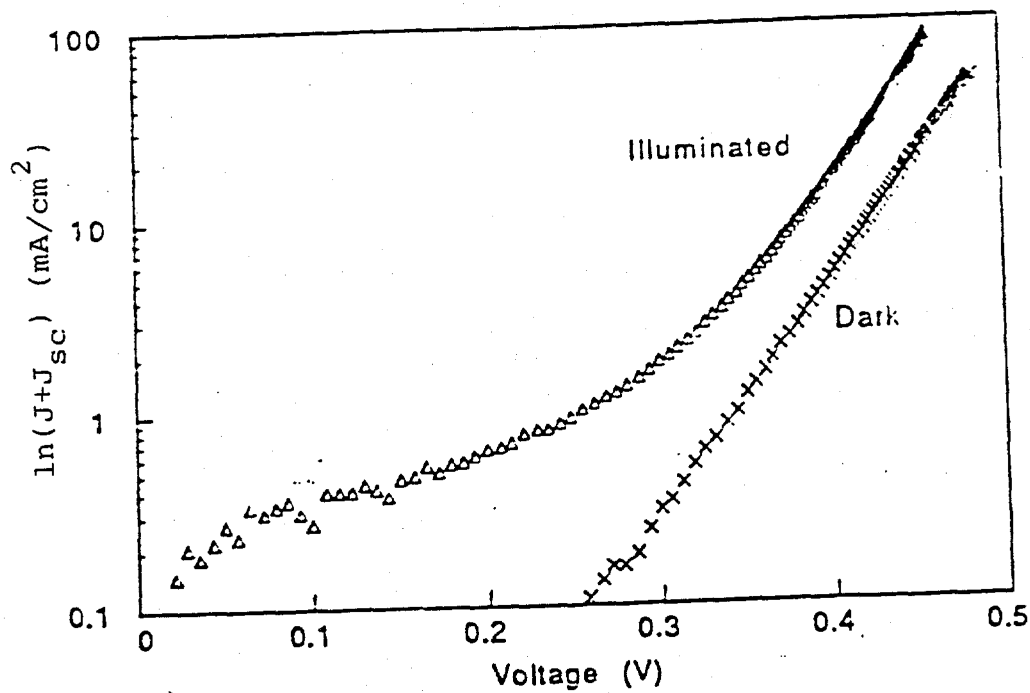


Figure 2-10. Forward bias J-V curves for the same cell in the dark and under illumination at T=290K.

Discussion

The results presented can be modelled with both SRH recombination and interface recombination playing a role in the diode characteristic. Thus, the diode can be represented by:

$$J+J_L = J_{oo1}\exp(-q\phi_1/A_1kT)\{\exp[qV/A_1kT]-1\} + J_{oo2}\exp(-q\phi_2/kT)\{\exp[qV/kT]-1\}.$$

The first term is due to the SRH recombination with A_1=1.5-2 and ϕ_1=1.0eV. The second term, due to interface recombination, has ϕ_2=0.9-1.0eV. Fitting the J_{sc}-V_{oc} data discussed above gives $J_{oo2}\sim10^{10}$mA/cm^2 which is comparable to the Richardson constant. This indicates that the interface recombination is limited only by the supply of holes from the $CuInSe_2$ because of a high density of interface states, which may result from the lack of lattice matching between the $CuInSe_2$ and the (CdZn)S. This will limit V_{oc} to slightly more than 0.5V unless the density of interface recombination states is reduced significantly or the bandgap of the $CuInSe_2$ is increased near the interface.

Alternatively, the diode characteristics can be described by a single current mechanism controlled by SRH recombination but with a voltage dependent A factor. Such a dependence has been predicted by numerical models for SRH recombination in homojunctions dependent on the energy distribution of states involved in the recombination process (14,15). However, the low A factors observed for cells with high fill factors would not be likely.

Conclusions

The variation in the diode A factor indicates that the diode cannot be described by a simple SRH recombination model with A=2. Instead, the results suggest two models: an admixture of SRH recombination in the space charge region of the $CuInSe_2$ and recombination through states at the (CdZn)S-$CuInSe_2$ interface, or SRH recombination with a voltage dependent A-factor. In any polycrystalline heterojunction both recombination mechanisms will be present. To improve V_{oc}, determination of the limiting current mechanisms may be essential.

2.2.5 Discussion - Further Work

$CuInSe_2$/Cu(InGa)Se_2 cells have been fabricated with modifications in the compositions, substrate temperatures, and thicknesses of the $CuInSe_2$, Cu(InGa)Se_2, and (CdZn)S layers. While the cell results again show that V_{oc} can be increased with such a bandgap modified device structure, problems remain with low J_{sc} and FF and with photoconductive and resistive (CdZn)S. We have concluded that these problems do not result from simple deposition conditions but may be inherent in the specific device design. As a result, we have concluded that the most fruitful approach to improving V_{oc} for

$CuInSe_2$ cells will be to re-examine in greater depth the recombination mechanisms that control high efficiency devices. I-V analysis has shown that a simple SRH recombination model is not sufficient and alternatives are being examined. Work will also continue on modeling of bandgap modified cells and fabrication and analysis of $CuInSe_2$/$Cu(InGa)Se_2$ and Ga/$CuInSe_2$ cells, including use of selenization processes which may form more continuous layers.

2.3 EFFECT OF $CuInSe_2$ THICKNESS ON DEVICE PERFORMANCE

Predicting the output of a $CuInSe_2$ solar cell as the thickness of the absorbing $CuInSe_2$ material is reduced requires that the electrical behavior of the metallic Mo contact be taken into consideration. Depending on the type of contact that is produced when $CuInSe_2$ is put on the Mo can make a large difference in the collection of current as the $CuInSe_2$ thickness is reduced. Figure 2-11 shows the possible types of contacts that can be produced.

In order to predict the behavior of these types of contacts with respect to $CuInSe_2$ thickness, a model of current collection based on diffusion and space charge electric field collection was chosen (16). The collection equations for the various contacts are shown below, (see page 37) where:

α = absorption coefficient of $CuInSe_2$
L = diffusion length
t= thickness of $CuInSe_2$
w = width of space charge region at the $CuInSe_2$/CdS junction
w_1 = width of space charge region at the $CuInSe_2$/Mo junction
d=t-w
d_1 = t-w-w_1

The diffusion length of 1.5 μm and the space charge collection width of 0.1 μm was chosen as representative based on reference 17. A 0.1 μm width of CdS was picked as typical for IEC devices. The optical absorption characteristics of CdS and $CuInSe_2$ were obtained from references 18 and 19 respectively. Optical losses due to reflection or contact shading were ignored. J_{sc}'s were calculated from the standard AM1.5 global spectra normalized to 100 mW/cm^2. The calculated results are shown in Table 2-7.

From Table 2-7 it can be seen that the "accumulation" contact gives the highest J_{sc} as the $CuInSe_2$ thickness is reduced. This is because the band bending as shown in Figure 2-11 shields the minority carriers from the high recombination metal surface. The "ohmic" contact is worse due to the lack of shielding.

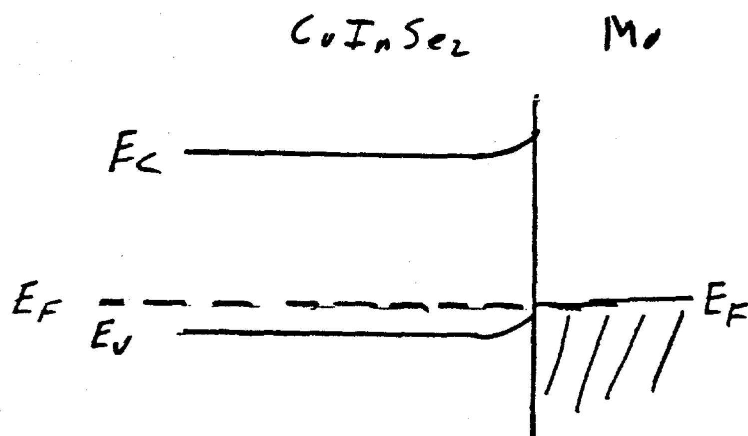
$$\text{Internal Q.E. "Accumulation" contact} = 1-e^{-\alpha w} + \frac{\alpha L e^{-\alpha w}}{\alpha^2 L^2 - 1}\left[\alpha L - \frac{\sinh\left(\frac{d}{L}\right) + \alpha L e^{-\alpha d}}{\cosh\left(\frac{d}{L}\right)}\right]$$

$$\text{Internal Q.E. "Ohmic" contact} = 1-e^{-\alpha w} + \frac{\alpha L e^{-\alpha w}}{\alpha^2 L^2 - 1}\left[\alpha L - \frac{\cosh\frac{d}{L} - e^{-\alpha d}}{\sinh\frac{d}{L}}\right]$$

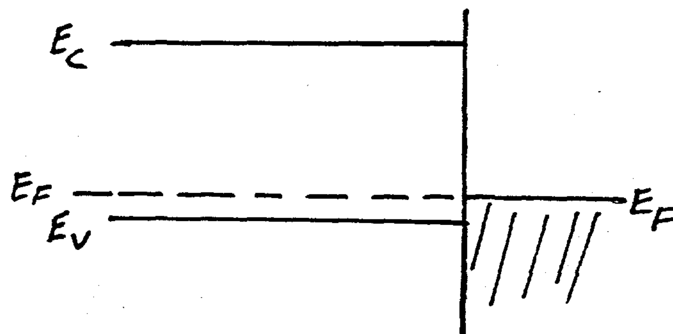
$$\text{Internal Q.E. "Depletion" contact} = 1-e^{-\alpha w} + \frac{\alpha L e^{-\alpha w}}{\alpha^2 L^2 - 1}\left[\alpha L - \frac{\cosh\frac{d_1}{L} - e^{-\alpha d}}{\frac{d_1}{L}}\right]$$

$$\text{Reverse Internal Q.E. "Depletion" contact} = \frac{\alpha L e^{-\alpha w}}{\alpha^2 L^2 - 1}\left[\frac{1-e^{-\alpha d_1}\cosh\frac{d_1}{L}}{\sinh\frac{d_1}{L}} - \alpha L e^{-\alpha d_1}\right.$$

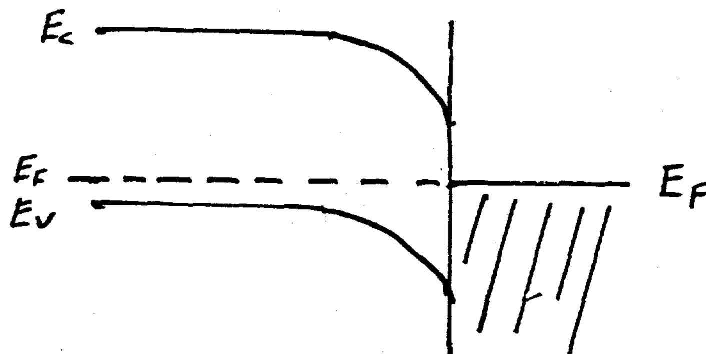
$$\left. + e^{-\alpha d_1} \quad 1-e^{-\alpha d_1}\right.$$



"Accumulation" Contact



"Ohmic" Contact



"Depletion" Contact

Figure 2-11. Band configuration of possible types of metal contacts

Table 2-7
Integrated J_{sc} for Types of Back Contact with a CdS Window Layer of 0.1 μm (Jsc_{max}=42.9 mA/cm^2) and L_n= 1.5 μm and a space charge collection width of 0.1 μm.

$CuInSe_2$ Thickness (μm)	J_{sc} (mA/cm^2) "Accumulation" contact	"Ohmic" contact	"Depletion" contact x_o=0.07 μm
10	35.3	35.3	35.3
5	35.4	35.3	35.3
2	36.3	33.6	33.5
1	35.8	29.2	27.3
0.5	30.2	23.0	21.6
0.2	18.8	15.3	12.7

Finally, the effects of a "depletion" contact are included because it may be close to the actual behavior of the $CuInSe_2$/Mo contact (references 3 and 20). Table 2-7 shows that this contact will reduce J_{sc} the most due to its reverse collection depletion region. In addition, this type of contact can also reduce V_{oc} by acting as a reverse solar cell. The effects of this are summarized in Table 2-8 for a "depletion" contact with a barrier of 0.52 eV.

Table 2-8
Reverse Photovoltaic Effect of the "Depletion" Contact with a Barrier Height of 0.5 eV so that J_o~20 mA/cm^2.

$CuInSe_2$ Thickness	J_{sc} (mA/cm^2)	ΔV_{oc} (mV)
10	0.1	0
5	1.1	-2
2	5.5	-7
1	8.5	-10
0.5	9.0	-10
0.2	6.1	-7

In conclusion, it can be seen that the type of electrical contact made to the back of the $CuInSe_2$ device will be very important when the $CuInSe_2$ thickness is reduced. The "accumulation" contact would be best. Perhaps it can be achieved with a Cu(In,Ga)Se_2 layer between the $CuInSe_2$ and Mo.

SECTION 3.0
CdTe BASED MATERIALS AND DEVICES

3.1 INTRODUCTION

During the reporting period, we investigated the effect of post-deposition processing described previously (1) on improving cell performance of PVD CdTe devices. This included studies of contact preparation, contact materials, and heat treatments. We studied the influence of window layer preparation and properties on V_{oc} and J_{sc}. Significant effort was focussed on improving the stability by using different contact materials and processing.

3.2 DEVICE FABRICATION

Basic device fabrication steps are given below, and have been described in detail elsewhere (21,22). The CdTe/CdS/ITO/7059 devices were prepared in a superstrate configuration by first sputter depositing 400 nm of ITO onto cleaned 1"x1" Corning 7059 glass substrates, resulting in a transparent conductive coating having 95% transmission at 900 nm and a sheet resistance of 10 ohm/■. Undoped CdS films 1 to 2 microns thick were then deposited by PVD from an effusion source bottle using high purity CdS powder onto the ITO/7059 superstrate. The undoped CdS films typically had a resistivity of 10 ohm-cm.

The CdTe films were also deposited by PVD, using high purity (5N) CdTe powder. Nominally two micron thick films were deposited at a substrate temperature of 250°C and growth rate of 0.02 microns per minute, which correspond to the single phase region of growth for CdTe. Thus, all CdTe films were deposited under nominally identical conditions for the results presented here.

Following CdTe deposition, a 1% (wt.) solution of $CdCl_2$ in CH_3OH was prepared by dissolving anhydrous $CdCl_2$ in electronic grade CH_3OH at room temperature. Five to seven drops of the solution were dispensed onto the CdTe using an eyedropper. The samples were dried in an oven at 50 to 90°C for several minutes. The solubility of the $CdCl_2$ in CH_3OH is only 1.7% at room temperature, and as the CH_3OH evaporates, the solution becomes supersaturated, leading to uniform precipitation of $CdCl_2$ onto the CdTe surface. Based on the volume of solution, concentration, substrate area and density, the thickness of the $CdCl_2$ layer is estimated to be 0.5 μm. Immediately following the $CdCl_2$ application, the glass/ITO/CdS/CdTe was placed in a pyrex tube, purged in an 80:20 $Ar:O_2$ mixture flowing at ~.3ℓ/minute at 25°C for 30 minutes, then heat treated in air in a tube furnace at a temperature of 400°C for 30 minutes. After heat treatment, the surface of the samples was rinsed in de-ionized water for 30 seconds.

Semi-transparent contacts consisting of typically 100Å Cu and 500Å Au were deposited onto the CdTe surface by electron beam

evaporation. To minimize oxidation of the thin Cu film, the bell jar was backfilled with 4% H_2-Ar and pumped to $5x10^{-6}$ Torr, and a Ti flash evaporation was performed just prior to the Cu deposition. Other metal contacts were investigated as well.

The first step of device optimization following deposition of the Cu/Au contact was a heat treatment in a drying oven at 150°C for 30 min. to 2 hrs. Next, the samples were chemically treated by immersion in 0.02 M Br_2-CH_3OH for 5 seconds. The CdTe/CdS structures have been characterized at each stage of the post-deposition process to correlate processing steps, structural changes and device behavior. This information has been previously reported (21,22).

3.3 CELL TESTING CONDITIONS

Cell performance at IEC is measured with ELH lamps calibrated to yield 87.5 mW/cm^2 with Si standard cells. The cell temperature is typically 28 to 30°C. To allow a better comparison of these results to those obtained under standard testing (AM 1.5 global simulation) and to predict the performance of these devices under SERI measurement conditions, we investigated the dependence of J_{sc} on the illumination source. J_{sc} was measured on 12 cells from different CdTe pieces under ELH (calibrated as above) and under Oriel (Xe lamp) AM 1.5 global illumination, calibrated to 100 mW/cm^2 using a filtered Si reference obtained from SERI. Additionally, J_{sc} was calculated by integrating the cells' quantum efficiency (QE) with the AM 1.5 global spectrum. We found that J_{sc} (Oriel) was 12 ± 2% lower than J_{sc} (ELH) and J_{sc} (Oriel) was 3 ± 2% larger than J_{sc} (QE). These results are in good agreement with a direct comparison of IEC versus SERI testing in 1989 and repeated again this year which found that J_{sc} (IEC) was 12 ± 3% larger than J_{sc} (SERI).

Table 3-1 shows cell performance measured on two devices at IEC and at SERI. Note that V_{oc} and FF are in good agreement and remain stable over ~1 month. The value of J_{sc} (SERI) is 0.88 ± 0.02 of J_{sc} (IEC). The IEC efficiency is determined by normalizing with 87.5 mW/cm^2, while the SERI value is normalized with 100 mW/cm^2. The integrated QE gave J_{sc} = 17.9 mA/cm^2 from cell #2 and 18.5 mA/cm^2 from cell #3, in reasonable agreement with the SERI value.

Therefore, we scale all CdS/CdTe cell test values measured at IEC for the remainder of this report as follows: J_{sc} (ELH) is multiplied by 0.88 and η (ELH) is multiplied by 0.88x0.875 = 0.77. This procedure will yield values expected if the cells had been tested at SERI with 100 mW/cm^2 global AM1.5 illumination.

Table 3-1
Illuminated Cell Test Values from CdS/CdTe Piece 40699-31 Measured at IEC (87.5 mW/cm^2, uncorrected ELH) and SERI. (100 mW/cm^2, global AM 1.5 mismatch corrected) Area of cell is 0.071 cm^2.

Cell	Tested/Date	V_{oc}	J_{sc}	FF	η
#2	IEC 11/21 (init)	.762	19.52	70.6	12.0
	IEC 12/5	.757	19.11	68.7	11.4
	SERI 12/10	.761	16.9	69.3	8.9
	IEC 12/22	.750	18.85	69.3	11.2
#3	IEC	.753	20.80	66.2	11.9
	IEC	.749	20.87	67.6	12.1
	SERI	.751	17.93	68.1	9.2
	IEC	.733	20.73	70.4	12.2

3.4 POST-DEPOSITION PROCESSING - EFFECT OF $CdCl_2$ AND HEAT TREATMENTS

Experiments were performed to identify the critical but often hidden variables in the post-deposition processing. Controlling these parameters resulted in improved spatial uniformity, reproducibility and overall device performance.

We incorporated the previously reported $CdCl_2$ application and slow thermal drying procedures (21,22) to evaluate the influence of the atmosphere used during the 400°C heat treatment. We frequently observed that the $CdCl_2$ surface did not rinse off as expected in deionized water following 400°C heat treatment in room air. In cases where the surface was not removed by the rinse, the J_{sc} optimization step took 1.5 to 2 times longer and the V_{oc} optimization step (Br_2-MeOH dip) did not produce the expected increase, resulting in V_{oc} of less than 600 mV. These effects were more pronounced and frequent on samples heat treated on humid days. We examined the visual and structural properties of CdTe/CdS samples heat treated at 47% and 85% relative humidity (Table 3-2) and found, at high humidity: 1) the surface became very textured and milky; 2) the CdTe (111) peak was not sharpened; 3) the CdTe lattice parameter was not shifted; and 4) many new peaks appeared, indexed to CdO, $Cd(ClO_4)_2$, and $TeO_2(OH)_2$. Rinsing the sample which was heat treated at high humidity did not change the surface or the x-ray pattern. Thus heat treatment in humid (85% RH) ambient resulted in reaction of the $CdCl_2$ layer with the atmosphere forming various oxides (Table 3-2) but the CdTe layer was not restructured. In contrast, the samples heat treated at less than 50% RH were easily rinsed, exhibited the CdTe restructuring associated with the high efficiency process, and showed an increase in V_{oc} and FF after the Br_2CH_3OH dip.

These observations may be explained within the framework of our understanding of the function of the heat treatment and optimization steps on the devices. The $CdCl_2$ recrystallizes the CdTe film during the 400°C heat treatment, resulting in enhanced grain size. The rinse ideally removes excess $CdCl_2$ from the CdTe surface so that direct electrical contact may be made. After depositing the metals, a mild heat treatment is needed to drive Cu into the CdTe. We feel that the role of the Cu at this stage is two-fold: 1) Cu dopes CdTe p-type and 2) Cu is available in near surface region for reaction with Te to form a p^+ Cu_xTe contact layer. The chemical immersion ensures formation of ohmic contact by removing Cd from the near surface region. Additionally, some passivation of CdTe grain boundaries occurs, which reduces leakage paths and decreases the effective J_o.

From a chemical point of view, it would appear that humid air reacts with the $CdCl_2$ and CdTe layers in such a way that $CdCl_2$ does not recrystallize the CdTe (Table 3-2). Compounds are formed which do not rinse away in ordinary DI water. These surface compounds are a barrier layer to Cu and to the chemical immersion reactants (Br_2-CH_3OH) manifested by longer 150°C heat treatment times and little or no V_{oc} enhancement by the chemical immersion. Thus, we concluded that the moisture content of the ambient air present during the 400°C heat treatment influences the action of the $CdCl_2$ and can have serious detrimental effects which prevent full optimization of the CdTe/CdS structure.

Experiments were then performed in dry atmospheres consisting of mixtures of high purity argon and oxygen. We observed that heat treatment in dry 80% argon:20% oxygen atmospheres resulted in CdTe surfaces which visually resembled those seen on the low humidity sample from Table 3-2 despite the high room humidity (75%). Also, the DI water rinse noticeably removed excess $CdCl_2$ following the heat treatment, as desired. The time needed to heat treat devices at 150°C was only 1 hour on the samples treated in the dry $Ar:O_2$ mixture. Samples heat treated at 400°C in pure argon showed no visible $CdCl_2$ coating after the heat treatment. This was also observed for heat treatment in a vacuum or H_2-Ar atmosphere. We speculate that the $CdCl_2$ sublimes from the surface in inert, reducing, and evacuated environments. Consistent with this conclusion, devices made on samples heat treated in such atmospheres exhibit poor J_{sc} as do those using no $CdCl_2$. For heat treatments in oxygen containing atmospheres, a small amount of CdO or Cd chlorate may form on the surface of the $CdCl_2$, reducing its vapor pressure and preventing it from subliming.

Table 3-2

Composition of Physical Changes on CdS/CdTe Under

Different Ambient Humidity Conditions

During 400°C Treatment

Aspect ↓	Humidity Condition in Lab 47% R.H. 40639	 85% R.H. 40656
$CdCl_2$ coat		
Visual →	clear coating	milky coating
XRD →	$CdCl_2$ peaks	$CdCl_2$ peaks
400C H.T.		
Visual →	textured, milky	very milky
XRD →	CdTe FWHM sharper CdTe (111) increased CdTe ao decreased $CdCl_2$ peaks unchanged No extra peaks	CdTe FWHM unchanged CdTe (111) unchanged CdTe ao unchanged $CdCl_2$ peaks decreased Many extra peaks: CdO, $Cd(ClO_4)_2$, $TeO_2(OH)_2$
DI Rinse		
Visual →	milky removed	no change
XRD →	$CdCl_2$ peaks decreased	All peaks unchanged
Device Optimization		
Jsc	2 hours at 150C	3 hours at 150C
Voc	Dip: +100 mV	Dip: +0 to 20 mV

The effect of purging time of the samples prior to insertion in the furnace was investigated. The quartz tube and samples were purged at 25°C with flowing (.3ℓ/min) 80% Ar/20% O_2 for 15 or 30 minutes, then inserted into the 400°C furnace. Device results for this experiment, with all pieces coming from CdTe run #40689, are shown in Table 3-3. One piece was given the 400°C heat treatment in ambient air for comparison. From these uniform device results obtained on samples purged for 30 minutes, we conclude that purging for 30 minutes or more is needed to remove residual moisture from the tube and samples. This has become standard operating procedure. Data in Table 3-3 for the 30 minute purge represents a significant improvement in uniformity and performance. Note that most cells from the 12 and 13 piece had V_{oc}>.7V and several had FF exceeding 73%.

3.5 WINDOW LAYERS

Results in previous sections (i.e. Tables 3-1 and 3-3) have indicated that we can routinely obtain V_{oc} > .7V and FF > 65% with our processing. Our best values of V_{oc} and FF (~.77V and ~73%) are state-of-the-art. However, to meet the goal of 12% efficiency requires significant improvement in J_{sc}. Present devices have AM 1.5 corrected values less than 19 mA/cm^2. During this contract we have begun to analyze optical losses and to fabricate devices with improved window layer transmission.

Reflectance and transmission spectra were measured on glass/ITO/CdS, and then reflectance was measured on the piece following cell fabrication. The CdS was "standard" material (~1.5 μm, evaporated, undoped). Analysis of this data by integration with the AM 1.5 global spectrum indicated losses in J_{sc} of approximately 2-3 mA/cm^2 due to CdS/ITO absorption and 1.4 mA/cm^2 due to front surface reflection, calculated over the range of 550 to 900 nm (the range of typical CdS/CdTe generation). However, another 6 mA/cm^2 is lost due to absorption of the ITO/CdS window below 550 nm. We have previously reported that current gains of ~5 mA/cm^2 are possible on SnO_x/CdTe structures; compared to SnO_x/CdS/CdTe structures (21), consistent with results of others (23,24). While the V_{oc} and FF of the SnO_x/CdTe structures were very poor, this demonstrates that a significant gain in J_{sc} is achievable by optimizing window layers. The challenge is to simultaneously maintain high V_{oc} and FF.

We have taken two approaches. One is to increase the window transmission by reducing the CdS thickness, including the use of CdS deposited by techniques other than evaporation in order to achieve continuous thin (<1000Å) layers. The second approach is to modify the CdS prior to CdTe evaporation to improve its transmission (hence J_{sc}) and grain size (hence V_{oc}). Preliminary results are presented here.

Table 3-3. CdTe/CdS J-V parameters for devices heat treated at 400°C in room air compared to in a flowing mixture of 80:20 $Ar:O_2$. Jsc are normalized to AM 1.5 100 mW/cm^2.

Device #		Atmosphere	Purge Time (min)	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff (%)
40689.31	1	Room Air	None	568	15.2	59.3	5.1
	2	Room Air	None	573	13.3	51.6	3.9
	3	Room Air	None	573	11.5	47.6	3.1
	4	Room Air	None	618	16.1	64.7	6.4
	5	Room Air	None	595	16.1	63.3	6.1
	6	Room Air	None	617	16.5	64.6	6.6
40689.11	1	$Ar:O_2$	15	654	18.2	60.0	7.1
	2	$Ar:O_2$	15	714	19.5	66.9	9.3
	3	$Ar:O_2$	15	649	18.3	62.1	7.4
	4	$Ar:O_2$	15	717	20.0	68.0	9.7
	5	$Ar:O_2$	15	655	18.7	62.8	7.7
	6	$Ar:O_2$	15	720	19.7	66.6	9.5
	7	$Ar:O_2$	15	651	18.8	61.6	7.6
	8	$Ar:O_2$	15	715	19.9	64.7	9.2
40689.23	1	$Ar:O_2$	15	625	16.5	65.0	6.7
	2	$Ar:O_2$	15	625	16.9	66.3	7.0
	3	$Ar:O_2$	15	699	17.2	72.0	8.6
	4	$Ar:O_2$	15	597	15.9	57.6	5.5
	5	$Ar:O_2$	15	596	16.6	57.8	5.7
	6	$Ar:O_2$	15	717	17.5	71.5	9.0
40689.12	1	$Ar:O_2$	30	739	18.2	73.0	9.8
	2	$Ar:O_2$	30	764	18.0	73.4	10.1
	3	$Ar:O_2$	30	735	18.0	67.7	9.0
	4	$Ar:O_2$	30	746	17.4	73.0	9.5
	5	$Ar:O_2$	30	782	17.2	73.5	9.9
	6	$Ar:O_2$	30	735	17.0	64.7	8.1
40689.13	1	$Ar:O_2$	30	703	18.5	59.4	7.7a
	2	$Ar:O_2$	30	696	16.9	65.6	7.7
	3	$Ar:O_2$	30	749	17.3	71.8	9.3
	4	$Ar:O_2$	30	753	16.3	67.5	8.3
	5	$Ar:O_2$	30	689	17.2	65.7	7.8
	6	$Ar:O_2$	30	719	17.1	68.5	8.4
	7	$Ar:O_2$	30	756	16.7	73.9	9.3b

a = 0.57 cm^2 cell area

b = highest in-house ≠EC CdTe cell FF

Table 3-4 lists the measured V_{oc}, J_{sc}, and FF obtained for cells with CdS thickness varying from 0.03 to 1.5 μm. Accurate J_{sc} values were obtained from integration of the QE with the AM 1.5 global spectrum. As expected, improvement in J_{sc} is seen for cells having CdS less than 0.3 μm due to increased short wavelength QE as shown in Figure 3-1. The device performance for 0.03 and 0.12 μm CdS devices is very similar to CdS-free TCO/CdTe junctions (Table 3-4). The QE shows a high, flat response below 500 nm which also indicates the absence of a CdS layer. Thus the 400°C processing step has resulted in the complete interdiffusion of CdS and CdTe, and elimination of a distinct CdS layer. In the case of thicker CdS, partial interdiffusion results in up to 30 meV shift in the CdTe absorption edge (Figure 3-2) which is consistent with formation of CdS_xTe_{1-x} (25) where 20% S lowers the bandgap to 1.3 eV. Interdiffusion of CdS and CdTe in the presence of $CdCl_2$ is widely reported (26-29) for CdS/CdTe devices prepared by screen-printing and sintering processes. Integration with the global AM 1.5 spectrum suggests that potential gains of ~6mA/cm^2 in the blue are slightly offset by a loss of <1 mA/cm^2 in the red. The effective CdS thickness in a completed device depends on processing conditions, and optimization of blue response involves a small tradeoff with red response.

The loss in V_{oc} with thin CdS shown in Table 3-4 will be investigated using analysis of J_{sc}-V_{oc} and J-V characteristics as a function of temperature and intensity. Controlling the losses with new thin CdS processing will be the subject of future effort.

Beside causing interdiffusion, the $CdCl_2$ heat treatment used for restructuring the CdTe layer also restructures CdS. Preliminary recrystallization experiments have been performed on evaporated CdS films for three thicknesses: 0.12 μm, 1.5 μm, and 9 μm. The 9 μm thick films were employed to provide a large-grain (1 μm) substrate for CdTe film growth, in the hope of reducing J_o via grain boundaries, to increase V_{oc}. For the recrystallization, the CdS films were coated with ~0.5 μm $CdCl_2$ by the same method used for CdTe/CdS and were heat treated at 400°C for 30 minutes in a dry Ar-O_2 mixture. XRD analysis of the 9 μm film (the only film measured so far) showed sharpening of the basal plane diffraction peaks, suggesting either strain reduction and/or grain size enhancement. SEM examination of CdS grain boundaries in the 9 μm thick films (revealed by Cu_xS formation and etching) did not show measurable increase in grain size, which was ~1 μm.

Restructuring the CdS films with the $CdCl_2$ heat treatment has a pronounced effect on the optical properties. Before heat treatment, the CdS films are yellow-orange in appearance, while after heat treatment they are pale-yellow. In all cases, the CdS absorption edge sharpens considerably after the heat treatment. The change is most significant for the 1.5 μm thick films. Figure 3-3 shows that after the $CdCl_2$ heat treatment, the sub bandgap absorption of the 1.5 μm film is decreased and approaches that of

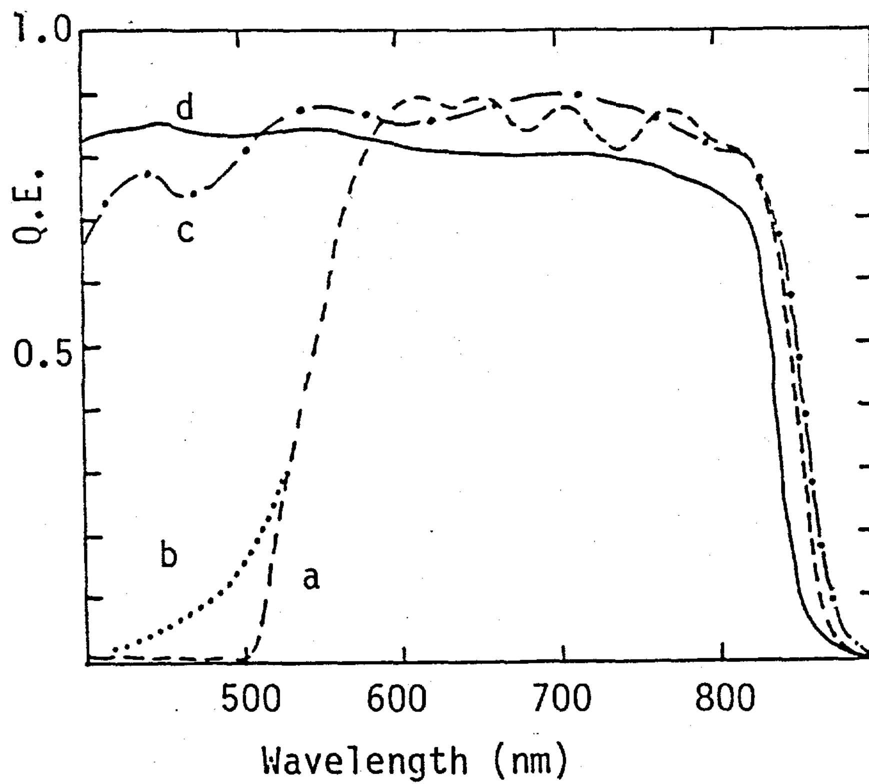


Figure 3-1. Comparison of CdS/CdTe QE for varying CdS thickness: a) 1.5 μm; b) 0.3 μm; c) 0.12 μm; d) 0.03 μm.

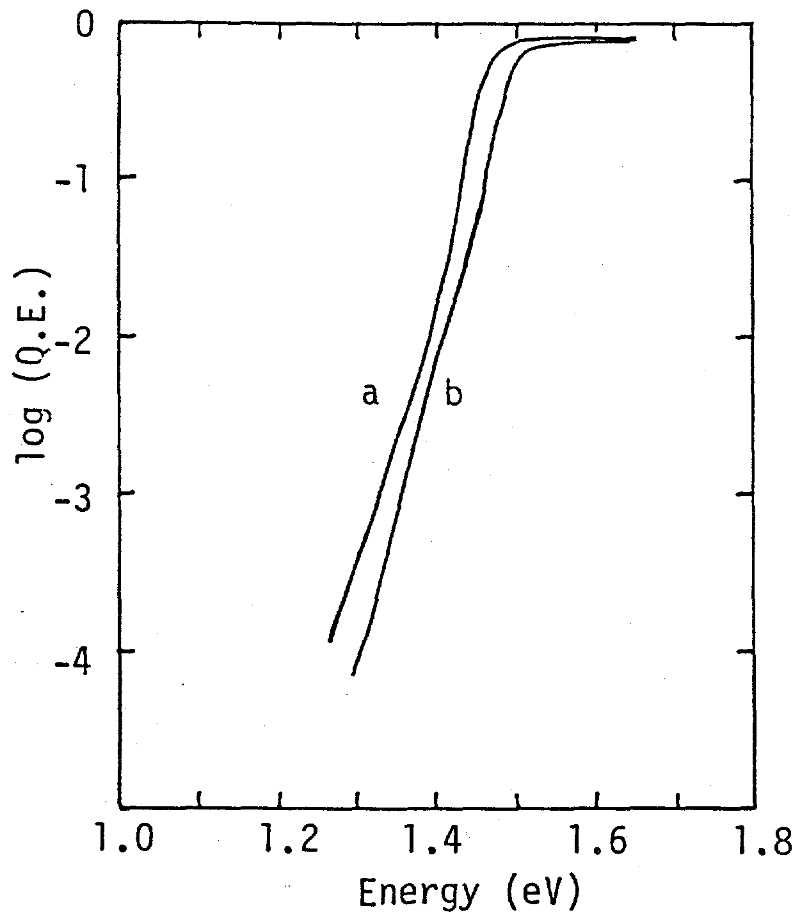


Figure 3-2. Log(QE) versus E for a) 1.5 μm CdS and b) 0.03 μm CdS.

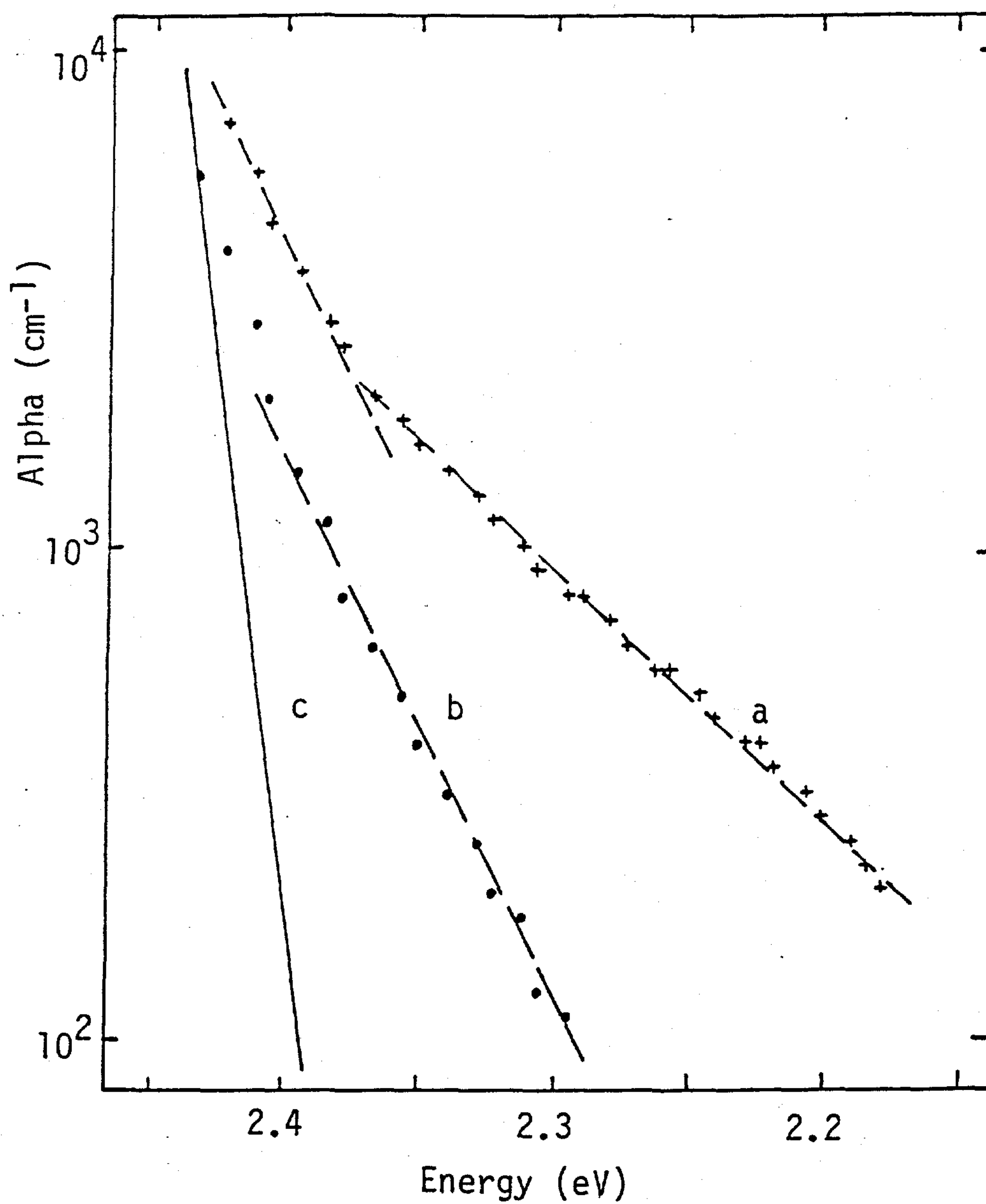


Figure 3-3. Absorption coefficient versus E for CdS film a) before and b) after $CdCl_2$ heat treatment compared to c) single crystal.

Table 3-4. CdTe device performance with varying CdS thickness.

Cell	CdS Method	CdS Thk (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
40699-31	Evaporated	1.5	750	18.5	67.6
40685-11-1	Evaporated	0.3	739	17.9	68.0
40699-23-3	Evaporated	0.12	345	24.5	59.1
40701-31-2	Sol. Grown	0.03(est.)	424	23.4	53.0
40651.321	none	0	440	24.0	53.0

single crystal CdS (30). Figure 3-4 shows that the above bandgap transmission is also increased. These changes are expected to increase J_{sc} (by increasing short wavelength transmission) and to increase V_{oc} (by reducing tail state density). The short wavelength QE of a cell with $CdCl_2$ treated CdS (Figure 3-5) exhibits the same sharpening of the short wavelength edge as in Figure 3-4 leading to a J_{sc} gain of 1 mA/cm^2. However, both devices had comparable V_{oc} (> 750 mV) and FF (~65%).

To conclude, devices with thin (<0.3 μm) CdS layers have improved J_{sc}. Short and long wavelength QE measurements show that CdS layers less than 0.1 μm effectively disappear after processing due to interdiffusion with CdTe. Formation of a TCO/CdTe junction is responsible for low V_{oc} and FF. The $CdCl_2$ heat treatment used to restructure the CdTe film can also be used to restructure the CdS layer and improve its properties. Future work will investigate the potential of obtaining high J_{sc} while maintaining V_{oc}>.70V using ZnO and SnO_2 TCO layers, CdS doping with In, ZnS alloying, and various CdS deposition methods and treatments.

3.6 CONTACTS AND STABILITY

Under our previous subcontract (21), we began to study the stability of CdTe devices stored in air. We found preliminary evidence of device instability in V_{oc} and FF over periods of months. CdTe/CdS samples prepared at IEC and Ametek were evaluated using either a Cu/Au contact or ZnTe:Cu contact.

The data suggested that the ZnTe:Cu contact, which has Cu but no Au, produced more stable devices than Cu/Au. A substantial body of literature exists which links Au contacts with instability in CdTe cells (26,31-33). In particular, a recent article (34) identifies an increase in contact resistance over a period of three months as due to CdTe-Au interdiffusion. Thus, alternative contacts such as Cu/Mo, Cu/Pt, Cu_2Te, or ZnTe:Cu were examined under the current contract.

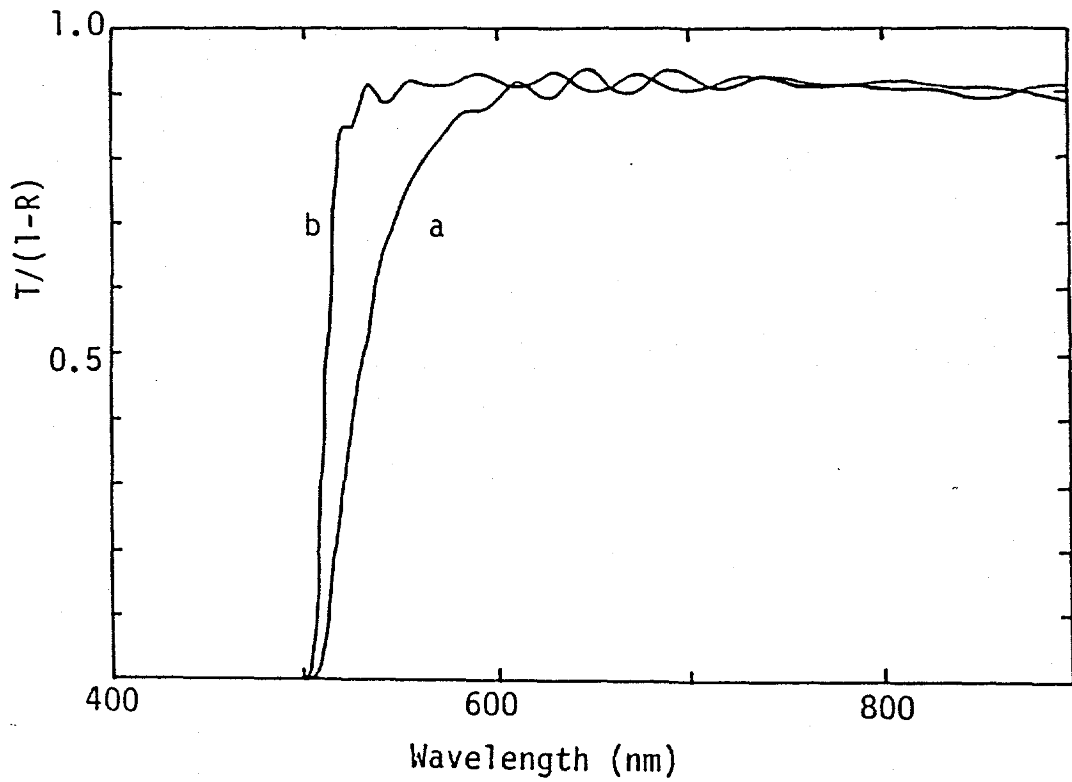


Figure 3-4. T/(1-R) versus wavelength for CdS/ITO in a) as-deposited condition and b) after $CdCl_2$ coating and 400°C heat treatment.

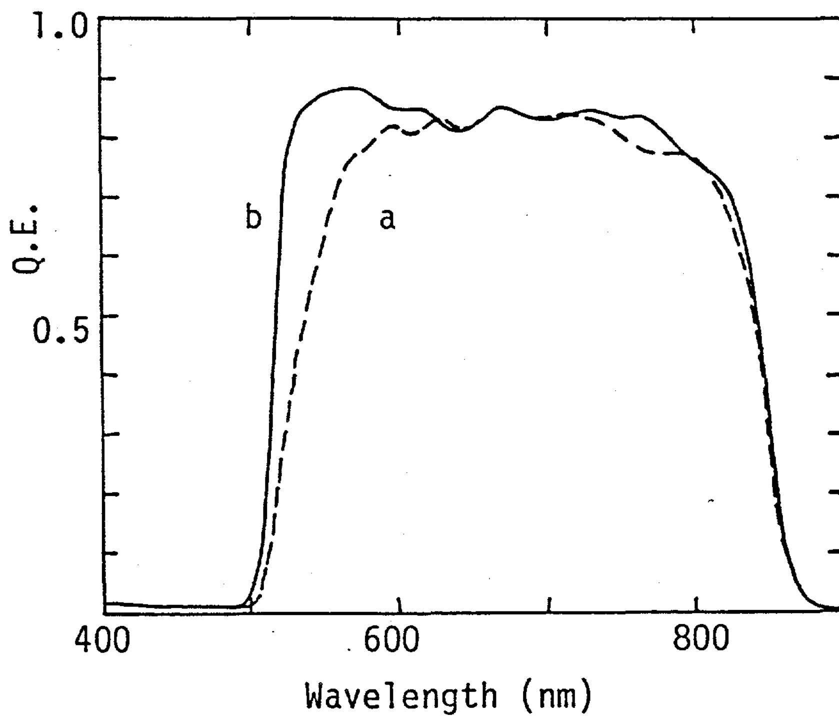


Figure 3-5. Comparison of CdS/CdTe cell QE using a) as-deposited CdS (a) and b) recrystallized CdS.

Several general trends became apparent from our stability study on IEC evaporated CdS/CdTe cells with Cu/Au contacts when stored in room air in the dark.

1. Degradation can be in V_{oc} or FF or both, but typically J_{sc} is unaffected.
2. Good cells (η>8%) degrade while poor cells (η<6%) are stable, even for cells on the same piece.
3. Very high initial parameters (V_{oc}>.75V, FF>70%) degrade within a few weeks to more typical values.
4. Degradation is not due to repeated probing or damage of the contact.

The influence of heat treatments on completed, optimized cells was also investigated, either as a "cure" for stability problems by restoring degraded V_{oc} and FF values, or to indicate further contact optimization is needed by influencing the Cu/Au reaction with the CdTe. Devices were heated in H_2 for 0.5 or 1 hour at 150, 200, or 250°C, and in air at 150°C for 1 hour.

There was a considerable range in response to the heat treatments, even across a given piece. The following trends were generally observed. Heat treatment in air (1 hour/150°C) <u>reduced</u> V_{oc} by 20-150 mV, J_{sc} by .5 to 3 mA/cm^2 and FF by 2-12% (absolute). Subsequent heat treatment of the same sample in H_2 (1 hr/200°C) <u>increased</u> V_{oc} to its initial value but not J_{sc} or FF. Heat treatment at 150°C in H_2 (150°/.5 or 1 hour) increased V_{oc} by up to 50 mV, had no effect on J_{sc}, and caused random changes in FF of a few percent. At 200°C, V_{oc} increased 20 to 90 mV, while J_{sc} and FF either increased or decreased by a few percent. At 250°C (for .5 hour), V_{oc} increased by less than 30 mV, while J_{sc} and FF decreased uniformly on all cells, with many developing high series resistance or double-diode-like curvature. We noted that cells having very high initial performance but which had degraded (mostly V_{oc} and FF) over several months storage, were not restored to their initial levels. While V_{oc} after H_2 heat treatment at 150 or 200°C in some cases greatly exceeded the initial value, FF was never completely restored. Thus, H_2 heat treatments are not a cure for device (FF) instability.

Our stability effort has focussed on the contact process. This is justified by results from piece 40579-21, which is IEC evaporated CdS/CdTe material which received a ZnTe:Cu contact at Ametek. Cells on this piece have remained at 8±.5% efficiency for over 18 months. (Based on results of 40579-21, we feel that IEC evaporated CdS/CdTe material is essentially stable.) Cells on another piece of 40579, which received the standard Cu/Au contact at IEC, degraded from 9% to less than 7.5% in two months. Thus, the contact material and process is critical to the stability of the device.

Alternatives to Au as the secondary metal contact were investigated. An experiment was carried out using 100Å Cu layers with 500Å Pt and Mo contacts. Device results are shown in Table 3-5 for the stability of the best cell from pieces with Cu/Au, Cu/Mo and Cu/Pt contacts.

Table 3-5

Stability of CdS/CdTe Cells with Cu/Au, Cu/Mo and Cu/Pt Contacts (Cu=100Å, Au, Mo, Pt = 500Å)

Piece Cell	Contact	Time	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
40688-13-4	Cu/Au	init	.700	17.2	68.6	8.2
		2 wk.	.692	17.2	67.8	8.1
		6 wk.	.676	17.1	64.8	7.5
40682-112-2	Cu/Au	init.	.678	18.8	68.6	8.8
		2 wk.	.675	18.5	66.0	8.2
40688-11	Cu/Au	init.	.710	18.5	68.3	8.9
		3 mo.	.718	17.5	66.4	8.3
40682-122-2	Cu/Pt	init.	.660	17.9	63.2	7.5
		1 wk.	.600	17.6	56.6	6.0
		2 mo.	.623	17.8	58.0	6.5
		5 mo.	.617	14.3	53.8	4.7
40682-312-3	Cu/Pt	init.	.625	17.7	65.5	7.2
		1 wk.	.588	17.3	57.4	5.8
40688-212-4	Cu/Mo	init.	.707	17.2	60.8	7.4
		1 wk.	.695	17.1	63.5	7.5
		2 mo.	.712	16.4	59.7	6.9
40683-132-4	Cu/Mo	init.	.693	15.6	62.3	6.8
		1 wk.	.675	16.3	61.5	6.7
		3 mo.	.618	15.8	59.0	5.8

Typically, cells with Cu/Pt or Cu/Mo contacts have slightly lower FF than those with Cu/Au contacts due to curvature beyond V_{oc}. The best cells, listed in Table 3-5, show signs of degradation as well. Thus, we have abandoned alternative metal contacts as the sole cure for producing stable, high-efficiency CdS/CdTe devices, and have focussed on using a semiconductor contact such as Cu_2Te or ZnTe:Cu grown on the CdTe. Note that both of the above materials have Cu, which is critical in achieving a low resistance contact on CdTe.

The Cu_2Te was formed by an exchange reaction in a CuCl bath. Thirteen depositions on CdS/CdTe explored bath temperature (40-60°C) and CuCl concentration ($4.0x10^{-3}$ to $4.0x10^{-4}$ M or between 10% of saturation to saturation). The CdTe was given the 400°C $CdCl_2$ treatment and etched briefly in 0.01% Br_2CH_3OH prior to the Cu_2Te formation step. Sample immersion time for Cu_2Te formation ranged from 7 sec to 1 min. Cells were completed with Au contacts. Most cells were shorted or strongly shunted even when deposited on 4 μm of CdTe. It was suspected that preferential formation of Cu_2Te along grain boundaries was responsible. Cell results yielded V_{oc} < .55V and $J_{sc} \leq 15$ mA/cm^2.

Solution grown ZnTe:Cu as a CdTe contact is being investigated under New Ideas Subcontract #XM-0-18110-1 and the method for growth of ZnTe is described elsewhere (35). Over 25 CdS/CdTe pieces have been fabricated with live devices having ZnTe:Cu contacts to the CdTe. It has been found that a pH of 3 and a Cu concentration of 10^{-4} (M/ℓ) gave reasonable results. Deposition times of 15 to 60 minutes have been used, leading to estimated ZnTe:Cu film thicknesses of about 0.1 μm. Devices have been completed with Cu/Au, ITO/Ni and Ni contacts.

The highest initial efficiency cell to date with ZnTe:Cu and Cu/Au metallization was #40691-231-1. Cell performance is given in Table 3-6 along with another piece having similar efficiency which <u>increases</u> over three months. Individual parameters of V_{oc} = .76V and FF = 74% have been achieved using ZnTe:Cu with ITO/Ni or Ni contacts. Optimization of the ZnTe:Cu process and subsequent post-contact processing will be further investigated in the following year. The goal will be to establish a standard, reproducible contact fabrication yielding stable, high-efficiency CdS/CdTe/ZnTe devices.

Table 3-6
Stability of CdS/CdTe Cells with ZnTe:Cu Metal Contacts

Cell	Metal Contact	Time	V_{oc}	J_{sc}	FF	η
40691-231-1	Cu/Au	init	.703	16.8	69.0	8.2
		2 mo.	.711	17.9	66.4	8.5
		3 mo.	.700	17.9	66.5	8.3
40690-232-2	Cu/Au	init	.753	16.7	62.1	7.9
		3 mo.	.733	18.7	64.3	8.8
406941-22	ITO/Ni	init	.693	18.3	65.9	8.3
		6 wks	.695	16.2	65.6	7.5

3.7 CHARACTERIZATION OF CdTe/CdS SOLAR CELL JUNCTION BEHAVIOR

Frontwall spectral response measured through the 7059 glass/ITO/CdS and backwall spectral response through the semi-transparent Cu/Au contact is shown in Figure 3-6. The strongly peaked backwall response at longer wavelengths and the high collection efficiency exhibited by the frontwall response at short wavelengths indicates that the electrical junction is located very close to the metallurgical interface between the CdTe and CdS. Frontwall spectral responses normalized with respect to the short circuit spectral response for various voltage biases [$SR(-V,\lambda)/SR(OV,\lambda)$] are shown in Figure 3-7. The change at long wavelengths with voltage bias is probably due to variation in the width of the space charge region and hence the current collection width of this region. Cell spectral response can be integrated at each voltage bias to determine the change in $J_L(V)$.

Current voltage measurements in the dark and under AM1 illumination over a temperature range of ~100°K corrected for series resistance and shunt conductance can be described very well by the following equations:

$$J=J_L(V)-J_o[\exp(qV/AkT)-1]$$

$$\text{with } J_o=J_{oo}\exp(-q\phi/AkT) \quad .$$

When the current-voltage measurements under illumination are corrected for this $J_L(V)$, both dark and illuminated current -voltage measurements yield barrier heights of about the CdTe bandgap with diode quality factors ~1.7-1.8.

The values determined for barrier height (ϕ) diode quality factor (A) and J_{oo} from these measurements are shown in Table 3-7.

The barrier height of 1.35 eV which is near the band gap of the CdTe as well as the high A-factors (~1.8) are strong indication that the current transport is controlled by Shockley-Read-Hall recombination in the junction region of the CdTe. The spectral response locates the junction region at or very near the CdTe/CdS interface. These results then indicate that the CdTe/CdS solar cell operates as a p-n heterojunction with current transport dominated by Shockley-Read-Hall recombination in the CdTe.

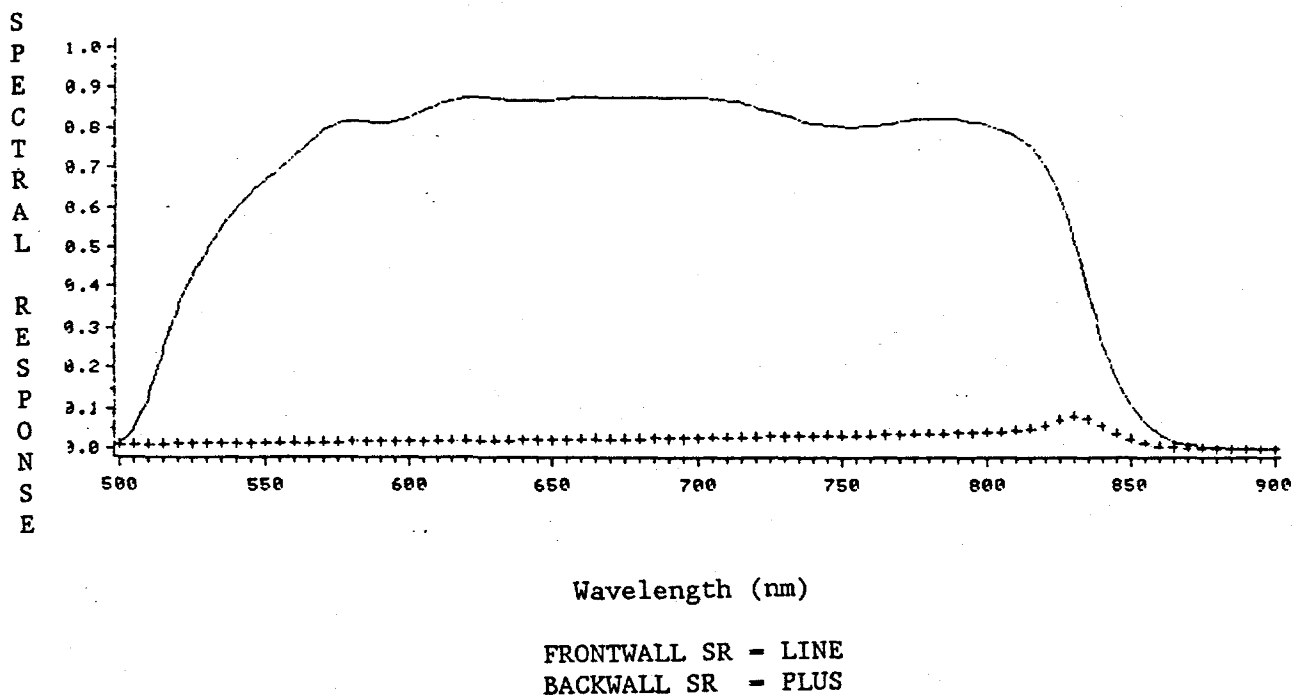


Figure 3-6. Frontwall, backwall spectral response vs. wavelength

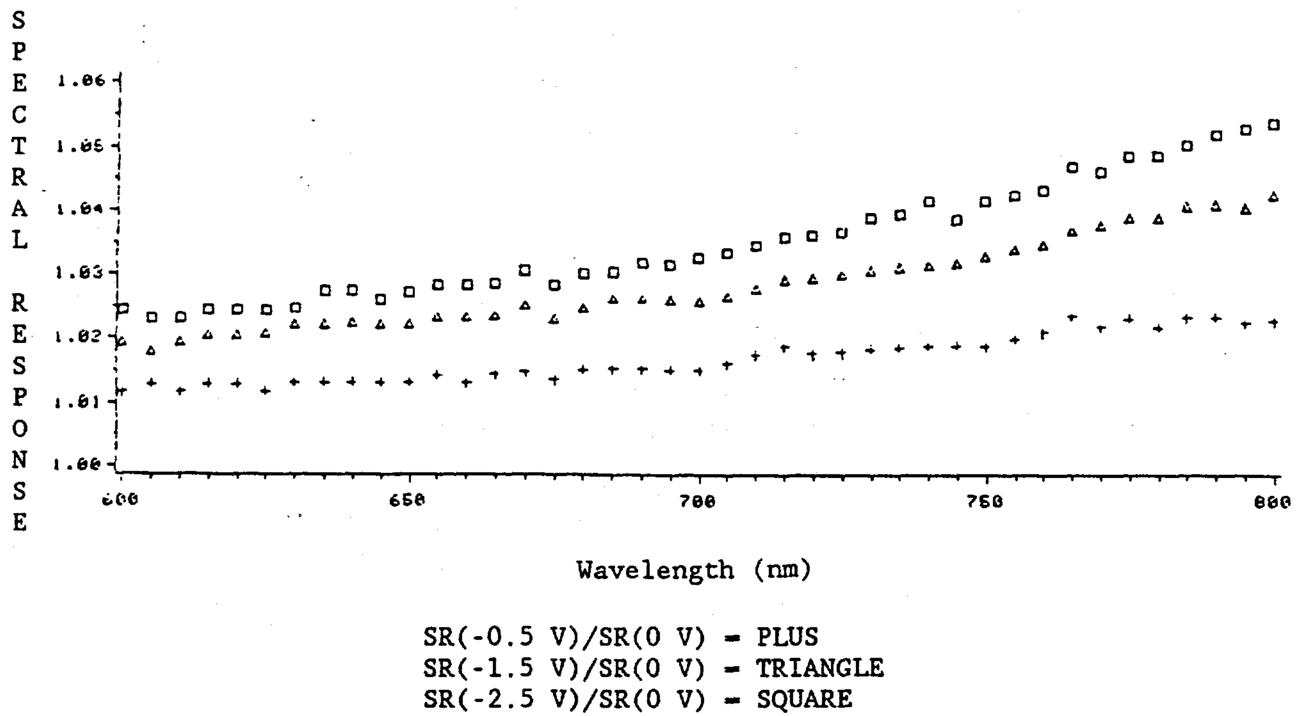


Figure 3-7. Normalized spectral response vs. wavelength

Table 3-7
Basic Device Parameters Derived from Measurements

Measurement	ϕ (eV)	A	J_{oo} (mA/cm^2)
V_{oc} vs. T	1.35	-	-
Light J-V vs T	1.35	1.8	1x10^7
Dark J-V vs T	1.3	1.7	5x10^6

3.8 CONCLUSIONS AND FUTURE WORK

We have investigated the effect of post-deposition processing in detail to improve the reliability and reproducibility of cell performance. Experiments were performed to identify hidden variables in the processing which affected the reproducibility. It was found that uniformly higher FF and V_{oc} were obtained when the 400°C heat treatment of the $CdCl_2$ coated CdS/CdTe sample was performed in dry $Ar:O_2$ as opposed to humid ambient air. Purging the samples and the tube for 30 minutes at 25°C in dry $Ar:O_2$ prior to the 400°C heat treatment was also important to improve uniformity as well as the average values of V_{oc} and FF across a given piece. The effect of the ambient on the CdTe structure and surface properties were studied in detail. Humid ambient promotes the growth of surface oxides and retards the restructuring of the CdTe by the $CdCl_2$. Using the methods discussed in this section, we can routinely achieve V_{oc}>700 mV, J_{sc}>17 mA/cm^2, FF>68%, and η>8%, with all evaporated CdS/CdTe junctions. Several pieces having cells with V_{oc}>750 mV and F>72% and efficiencies approaching 10% have been processed during this reporting period. Having achieved satisfactory values of V_{oc} and FF, it was clear that relatively low J_{sc} was limiting the performance of the present cells.

We focus on improving J_{sc} by significantly increasing the response of the cell at wavelengths below 500 nm. We investigated this using thinner and restructured CdS layers to improve the CdS transmission. Currents of 22-24 mA/cm^2 were obtained. Short and long wavelength QE measurements show that CdS layers less than 0.1 μm effectively disappear after processing due to interdiffusion with CdTe. Formation of a TCO/CdTe junction is responsible for low V_{oc} and FF. The $CdCl_2$ heat treatment used to restructure the CdTe film can also be used to restructure the CdS layer and improve its properties. Future work will investigate the potential of obtaining high J_{sc} while maintaining V_{oc}>.70V using ZnO and SnO_2 TCO layers, CdS doping with In, ZnS alloying, and various CdS deposition methods and treatments.

Stability studies of cells stored in ambient dark conditions over periods of up to 18 months have indicated that degradation occurs, especially in cells with high V_{oc} and FF. Considerable evidence in the literature and our own studies indicate that this may be due to reaction between CdTe and Au. Evaporated IEC CdS/CdTe devices with ZnTe:Cu contacts appear to be more stable than those with any metal contact (Cu/Pt, Cu/Mo or Cu/Au). Future work will improve the uniformity of the ZnTe deposition and monitor the stability of CdS/CdTe/ZnTe devices.

SECTION 4.0
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SECTION 5.0
ABSTRACT

Results and conclusion of Phase I of a multi-year research program on polycrystalline thin film solar cells are presented. The research comprised investigation of the relationships among processing, materials properties and device performance of both $CuInSe_2$ and CdTe solar cells. The kinetics of the formation of $CuInSe_2$ by selenization with hydrogen selenide was investigated and a $CuInSe_2$/CdS solar cell was fabricated. An alternative process involving the reaction of deposited copper-indium-selenium layers was used to obtain single phase $CuInSe_2$ films and a cell efficiency of 7%. Detailed investigations of the open circuit voltage of $CuInSe_2$ solar cells showed that a simple Shockley-Read-Hall recombination mechanism can not account for the limitations in open circuit voltage. Examination of the influence of $CuInSe_2$ thickness on cell performance indicated that the back contact behavior has a significant effect when the $CuInSe_2$ is less than 1 micron thick. CdTe/CdS solar cells with efficiencies approaching 10% can be repeatedly fabricated using physical vapor deposition and serial post deposition processing. The absence of moisture during post deposition processing was found to be critical. Improvements in short circuit current of CdTe solar cells to levels approaching 25 mA/cm^2 are achievable by making the CdS window layer thinner. Further reductions in the CdS window layer thickness are presently limited by interdiffusion between the CdS and the CdTe. CdTe/CdS cells stored without protection from the atmosphere were found to degrade. The degradation was attributed to the metal contact. CdTe cells with ZnTe:Cu contacts to the CdTe were found to be more stable than cells with metal contacts. Analysis of current-voltage and spectral response of CdTe/CdS cells indicates the cell operates as a p-n heterojunction with the diode current dominated by SRH recombination in the junction region of the CdTe.

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16. Abstract (Limit: 200 words)
This report covers Phase I of a multiyear research program on polycrystalline thin-film solar cells. IEC investigated the relationships between processing, material properties, and device performance of $CuInSe_2$ and CdTe solar cells. IEC studied the formation of $CuInSe_2$ by selenization with hydrogen selenide and fabricated a $CuInSe_2$/CdS solar cell. IEC also reacted the deposited copper-indium-selenium layers to obtain single-phase $CuInSe_2$ films and a cell efficiency of 7%. Studies of the open-circuit voltage (V_{oc}) of $CuInSe_2$ solar cells showed that a simple Shockley-Read-Hall recombination mechanism cannot accout for the limitations in V_{oc}. Examining the influence of $CuInSe_2$ thickness on cell performance showed that the back contact is significant when the $CuInSe_2$ is less than 1 micron thick. CdTe/CdS solar cells with efficiencies approaching 10% can be fabricated repeatedly. Improvements in short-circuit current of CdTe solar cells to levels approaching 25 mA/cm^2 are achievable by making the CdS window layer thinner. CdTe/CdS cells stored without protection from the atmosphere degraded because of the metal contact. CdTe cells with ZnTe:Cu contacts to the CdTe were more stable.

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