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High-Efficiency Cadmium and Zinc-Telluride-Based Thin-Film Solar Cells

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1. INTRODUCTION

Recent advances in polycrystalline CdTe solar cells have generated considerable interest in this area. CdTe cell efficiencies in excess of 12% have been verified with the potential of approaching 20%. However, in order to attain this potential, considerable amount of basic research needs to be done. More specifically, there is a need to understand the loss mechanisms including optical losses, bulk and interface recombination, grain boundary effects and resistive losses. Several different technologies have produced CdTe cell efficiencies in excess of 10%. However, different loss mechanisms are not understood well enough to make a precise comparison between the technologies and provide guidelines for improvements. It is necessary to develop new tools and models, and apply existing tools more prudently, in order to reveal and quantify loss mechanisms in CdTe solar cells.

The motivation for developing a wide bandgap photovoltaic material stems from the fact that the optimum two cell tandem design consists of 1.7 eV bandgap cell on top of a 1.0 eV bandgap cell. Considerable progress has been made on the bottom cell, particularly $CuInSe_2$ cells have given a small area efficiency of ~ 14%. However, the 1.7 eV bandgap material on II-VI elements for the top cell has not yet been discovered.

There are two ways of realizing ~20% efficient polycrystalline tandem solar cells. The first approach involves improving the CdTe cell efficiencies in excess of 15% and utilizing only a small amount of power from the bottom cell because of 1.5 eV bandgap of CdTe. The second approach is to develop a high efficiency (>10%) 1.7 eV bandgap cell with significant subgap transmission and take greater advantage of the high efficiency (~15%) bottom cell. This research addresses both approaches by fabricating CdTe as

well as 1.7 eV bandgap CdZnTe solar cells.

The overall goal of this program is to improve basic understanding of CdTe and CdZnTe cells, by growing and characterizing these films along with cell fabrication. One of the objectives is to develop wide bandgap (1.6-1.8 eV) material for the top cell, along with compatible window material and transparent ohmic contact, so that cascade cell design can be optimized. In addition to the CdZnTe cells, CdTe cells are fabricated and analyzed to determine efficiency limiting mechanisms and to provide guidelines for achieving higher efficiency cells.

In this program, front-wall solar cells were fabricated with glass/SnO_2/CdS window layer to maximize transmission and current. Absorber films were grown by MBE and MOCVD techniques, which provide excellent control for tailoring the film composition and properties. CdZnTe films were grown by MBE and CdTe films were grown by both MBE and MOCVD techniques. All the as-grown films were characterized by several techniques such as surface photovoltage spectroscopy (SPV), Auger electron spectroscopy (AES), and X-ray photoelectron spectroscopy (XPS) for composition, bulk uniformity, thickness, film and interface quality. Front-wall type solar cells were fabricated in collaboration with AMETEK materials research laboratory using CdTe and CdZnTe polycrystalline absorber films. The effects of processing on ternary films were studied by AES and XPS measurements coupled with C-V and I-V-T measurements. Bias dependent spectral response and electrical measurements were used to test some models in order to identify and quantify dominant loss mechanisms.

Research was conducted to understand the need for hydrogen anneal of the

glass/SnO_2/CdS substrate to achieve ~10% efficient MOCVD CdTe cells. Detailed analysis was performed to reveal the beneficial as well as detrimental effects of the heat treatment based on the measured cell parameters and defect analysis. Model calculations were performed to provide guidelines for achieving 18% CdTe cells.

It is well known that $CdCl_2$ dip followed by 400°C heat treatment results in grain growth and helps in achieving high efficiency CdTe cells. A detailed investigation was carried out to reveal the change in defect states, optical and electrical properties, and carrier transport mechanism due to $CdCl_2$ treatment. Another motivation for this investigation was to see if the $CdCl_2$ treatment introduces defects which tend to limit the present day CdTe cell performance in the range of 10-13%. This was accomplished by correlating the defects with cell parameters before and after the $CdCl_2$ treatment.

Finally, 1.7 eV bandgap CdZnTe films were grown by MBE for tandem cell applications. Front wall cells were fabricated using the CdTe process. Detailed analysis was performed to characterize, quantify, and understand the bandgap shift and high series resistance problems associated with the widegap material. Attempts were made to solve these problems through basic understanding of the source of degradation.

2. TECHNICAL PROGRESS

The technical progress has been divided into three sections. The pre-heat treatment of CdS and its effects on CdTe cell performance are described in section 2.1. Section 2.2 describes the effects of $CdCl_2$ treatment on the electronic properties of CdTe/CdS heterojunction. Section 2.3 deals with the process optimization of CdZnTe polycrystalline films for high efficiency solar cells.

2.1 Effects of Pre-heat Treatment of CdS on MOCVD CdTe/CdS Solar Cell Performance

This paper was presented and published in the Proc. 21st IEEE Photovoltaic Specialists Conference 1990.

2.1.1 Introduction

Polycrystalline CdTe solar cells are one of the leading candidates for terrestrial solar cell applications. Theoretical calculations predict an efficiency of 27%, while the practically achievable efficiency is 22% (1,2). Recently, an efficiency of 12.3% was reported on CdTe films grown by spray pyrolysis technique (3). In order to approach the practically achievable limit, many design modifications have been suggested including replacement of CdS window layer by CdZnS and use of ZnO instead of the transparent conducting SnO_2 layer to improve J_{sc} (1,2). However, a fundamental understanding of carrier loss and transport mechanisms at the CdTe/CdS heterojunction is necessary to improve V_{oc} and fill factor values intelligently rather than empirically. In CdTe/CdS solar cells, interface states play a major role in limiting the V_{oc} (4,5). Several factors such as

surface condition of CdS prior to CdTe growth, CdTe growth conditions, lattice mismatch, and the difference in thermal expansion coefficient between CdS and CdTe dictate the interface state density. A surface treatment on CdS/SnO_2/glass substrates prior to CdTe growth is one of the methods to reduce interface states. Every successful growth technique for fabricating CdTe/CdS solar cells today uses either a chemical or thermal treatment to clean the Cds surface prior to CdTe deposition.

Several investigators have shown that thermal treatment of CdS in H_2 atmosphere, modifies the electrical properties of CdS (6-8). It was observed earlier that annealing of CdS films in H_2 atmosphere at 400° C prior to deposition of CdTe modifies the defects and transport mechanism at the CdTe/CdS heterojunction (9). However, the surface modifications of CdS due to thermal treatment and its effects on cell performance have not yet been studied in detail. A systematic study of pre-heat treatment of CdS prior to deposition of CdTe by MOCVD was conducted in this section of the report. Both beneficial and undesirable effects of such heat treatment on device performance are characterized and discussed.

2.1.2. Experimental

CdS film were deposited on commercially available SnO_2/glass substrates by spray pyrolysis at a substrate temperature of 450° C. Prior to CdTe deposition by MOCVD, CdS/SnO_2/glass substrates were annealed in hydrogen atmosphere inside the reactor, in the temperature range of 300 to 450° C for five minutes. The surface modifications of CdS after each treatment were studied by Auger electron spectroscopy (AES) technique.

A 3 KeV electron beam with a current of 1.0 uA was used for AES measurements. Sputter profiling was performed using a normally incident 2 KeV Ar ion beam at a current density of 28 uA/cm^2. Electrochemical I-V and C-V measurements were performed to determine carrier concentration and electrical characteristics of annealed CdS films using an automated electrochemical etching profiler. An electrolyte, composed of 0.2M NaOH and 0.1M EDTA, was used to form a Schottky barrier contact on the CdS surface for I-V and C-V measurements.

CdTe films were deposited on annealed CdS/SnO_2/glass substrates under the same conditions, at a substrate temperature of 300° C. Dimethylcadmium and diallyltellurium were used as Cd and Te sources, respectively. Front-wall n-i-p solar cells were fabricated with glass/SnO_2/CdS/CdTe/ZnTe/Ni structures. Dark and light I-V and capacitance-frequency (C-F) measurements were performed to monitor the device performance.

2.1.3. Results and Discussion

C-V measurements indicated that annealing of CdS films in hydrogen atmosphere at 450° C increased the doping concentration of CdS from ~2 × 10^{17} cm^{-3} to ~10^{18} cm^{-3}. This is consistent with the claim of several investigators that adsorption of oxygen in CdS films increases the grain boundary barrier height (6-8) and reduces the mobility and carrier concentration. Oxygen in grain boundaries gives rise to electron traps which reduce the doping concentration by trapping electrons. Hydrogen annealing in our study causes desorption of oxygen from the grain boundaries which should reduce the

intergrain barrier height, resulting in the observed increase in carrier concentration. Annealing induced reduction of grain boundary states and their effects on device performance were studied by fabricating n-i-p cells on these substrates. Figure 2.1.1 shows the C-F data for cells fabricated on annealed substrates.

CdTe/CdS devices fabricated on unannealed substrates showed high capacitance at all frequencies along with maximum dispersion in capacitance at lower frequencies compared to devices fabricated on hydrogen annealed substrates. Hydrogen annealing not only reduce the absolute capacitance but also causes the capacitance to become frequency dependent. In general, at low frequencies interface states or extraneous states in the bandgap interact with voltage modulation, giving rise to increased capacitance (10). Thus, decrease in absolute capacitance and its frequency dependence after annealing suggests reduction of interface states. Similar behavior has been reported for $CuInSe_2$/CdS and closed space sublimation (CSS)-grown CdTe/CdS polycrystalline solar cells (9,10). The effects of reduction in interface states due to annealing are also seen clearly in the dark I-V measurements (figure 2.1.2), which show that CdTe/CdS diode behavior improves with increasing annealing temperature. In order to determine the variation in diode parameters quantitatively, a multivariable regression analysis was performed. The measured dark I-V data were fitted to a single exponential diode given by $I = I_o[\exp\{(q/AKT)(V-IR_s)\}-1] + (V-IR_s)/R_{sh}$ where A is the diode ideality factor, R_s is the series resistance, I_o is the saturation current density, and R_{sh} is the shunt resistance of the diode. The results of the analysis are given in table 2.1.1, which clearly show a decrease in I_o and series resistance with increasing annealing temperature. The reduction

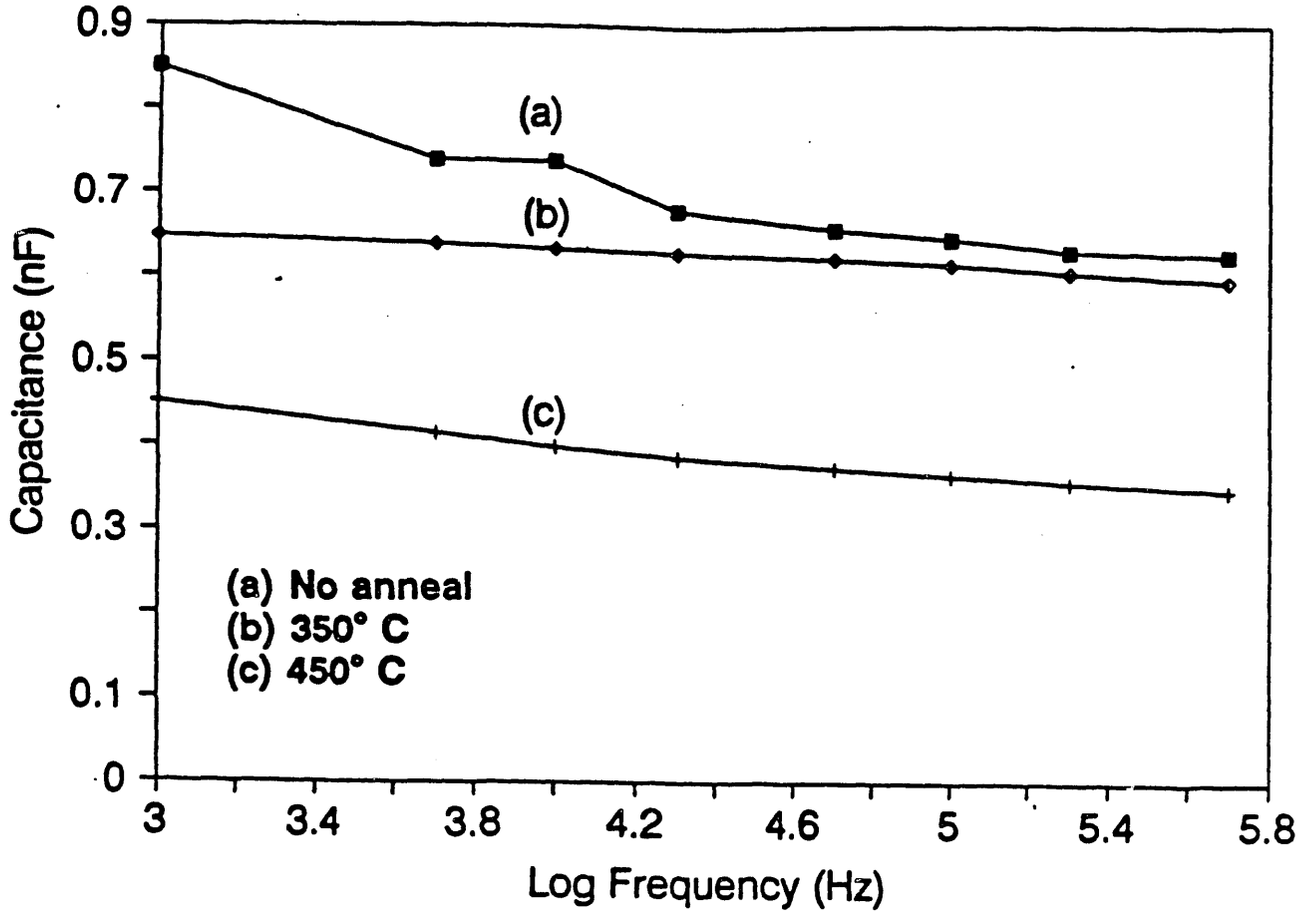


Figure 2.1.1 **Capacitance versus frequency measurements of CdTe/CdS devices fabricated on CdS/SnO_2/glass substrates for different annealing conditions a) unannealed, b) 350 C anneal, and c) 450 C anneal**

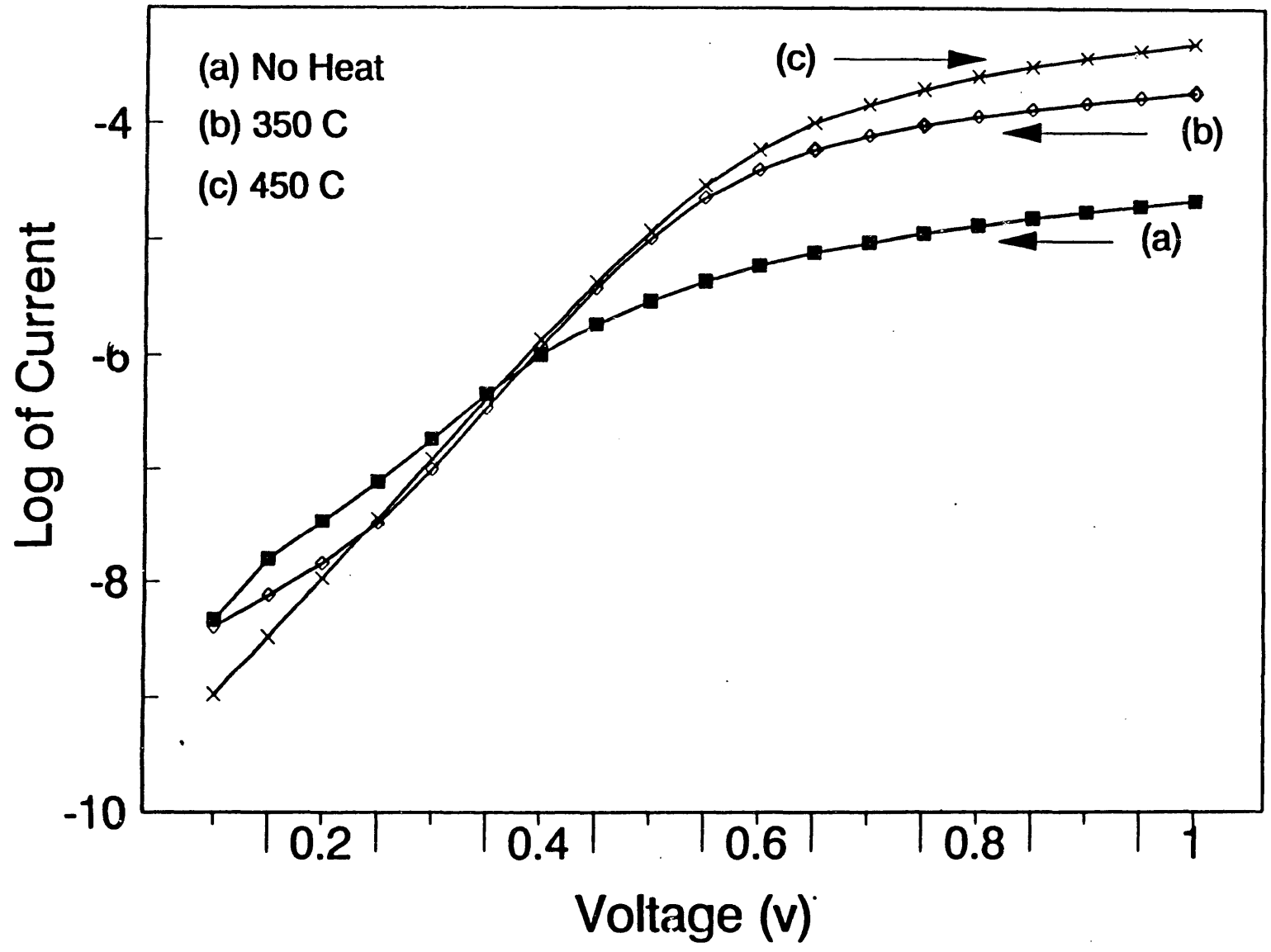


Figure 2.1.2 **Dark I-V data of CdTe/CdS solar cells fabricated on CdS/SnO_2/glass substrates annealed at different temperatures.**

Table 2.1.1 **Single diode parameter values of dark I-V data of CdTe/CdS devices fabricated on substrates annealed at different temperatures.**

Temperature C	A	I_o $X10^{-8}$ (A)	R_s Ohms	R_{sh} $X10^8$ Ohms
No anneal	2.14	8.9	20795	2.86
300	1.50	.35	1815	2.76
400	1.36	.063	1496	846
450	1.61	.008	748	2.44

in series resistance can be attributed to the increased doping of CdS observed by the C-V measurements. The improvement in I_o may be due to the reduction in interface state density. Furthermore, the diode ideality factor decreased from 2.1 to 1.5, suggesting a possible change in the transport mechanism across the CdTe/CdS interface. It has been shown earlier that in CdTe/CdS devices grown by CSS technique, H_2 annealing modifies the carrier transport from tunneling to interface recombination (9).

The improvement in CdTe/CdS cell performance upon heat treatment is also depicted in light I-V measurements shown in figure 2.1.3. Both open-circuit voltage and fill factor increased with heat treatment, increasing the efficiency of CdTe/CdS device from 5.8 to 8.1% (table 2.1.2). However, the J_{sc} did not change appreciably after annealing which indicates that the increase in open circuit voltage is primarily due to the decrease in I_o. In this study, the CdTe film thickness (1.5 um) and growth conditions were not optimized, therefore, only 8% efficiency was achieved. Nevertheless, the above results show a direct correlation between pre-heat treatments and cell performance. Using the guidelines of the above study for best pre-heat treatment and optimized CdTe thickness of 2.5 um, we were able to fabricate 9.7% efficient cell (11). In order to understand the source of these defects, XPS and AES measurements were performed on various CdS films before and after the preheat treatment. XPS data (figure 2.1.4) verified that the preheat treatment was able to remove significant amount of oxygen from the CdS surface. Since it is known that oxygen adsorbed on the surface of CdS gives rise to recombination centers (7), it is reasonable to speculate that oxygen induced defects on the CdS surface could be responsible for large number of interface states and poor performance of the

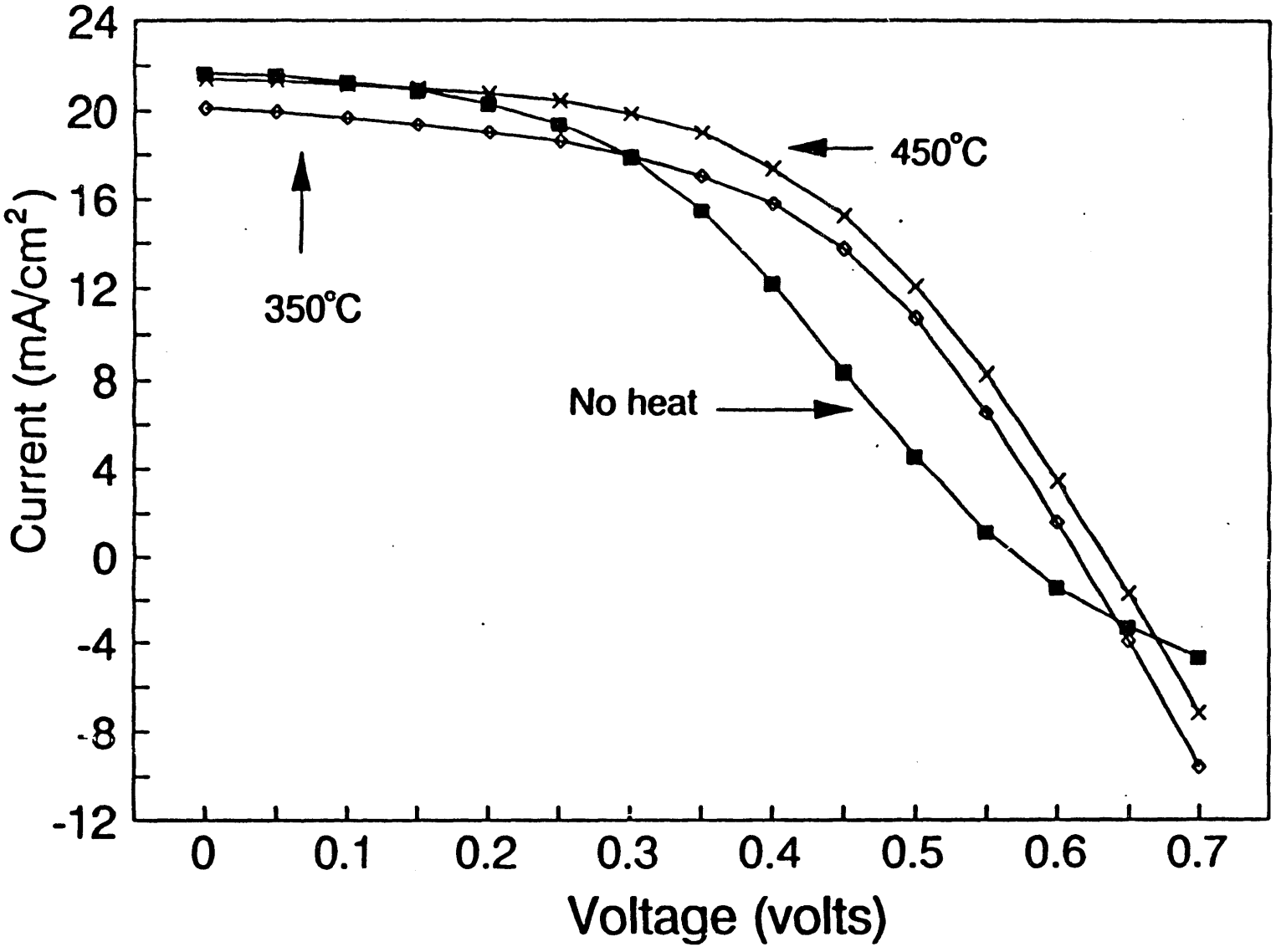


Figure 2.1.3 **Lighted I-V data of CdTe/CdS solar cells fabricated on CdS/SnO_2/glass substrates annealed at different temperatures.**

Table 2.1.2 **Light I-V data on CdTe/CdS cells prepared on CdS/SnO_2/glass substrates annealed at different temperatures.**

Anneal Temperature C	V_{oc} (mV)	J_{sc} (mA)cm^2	FF	Efficiency %
No anneal	600	20.9	.47	5.9
300	620	20.2	.53	6.6
350	630	20.2	.55	7.0
450	680	20.5	.56	7.9

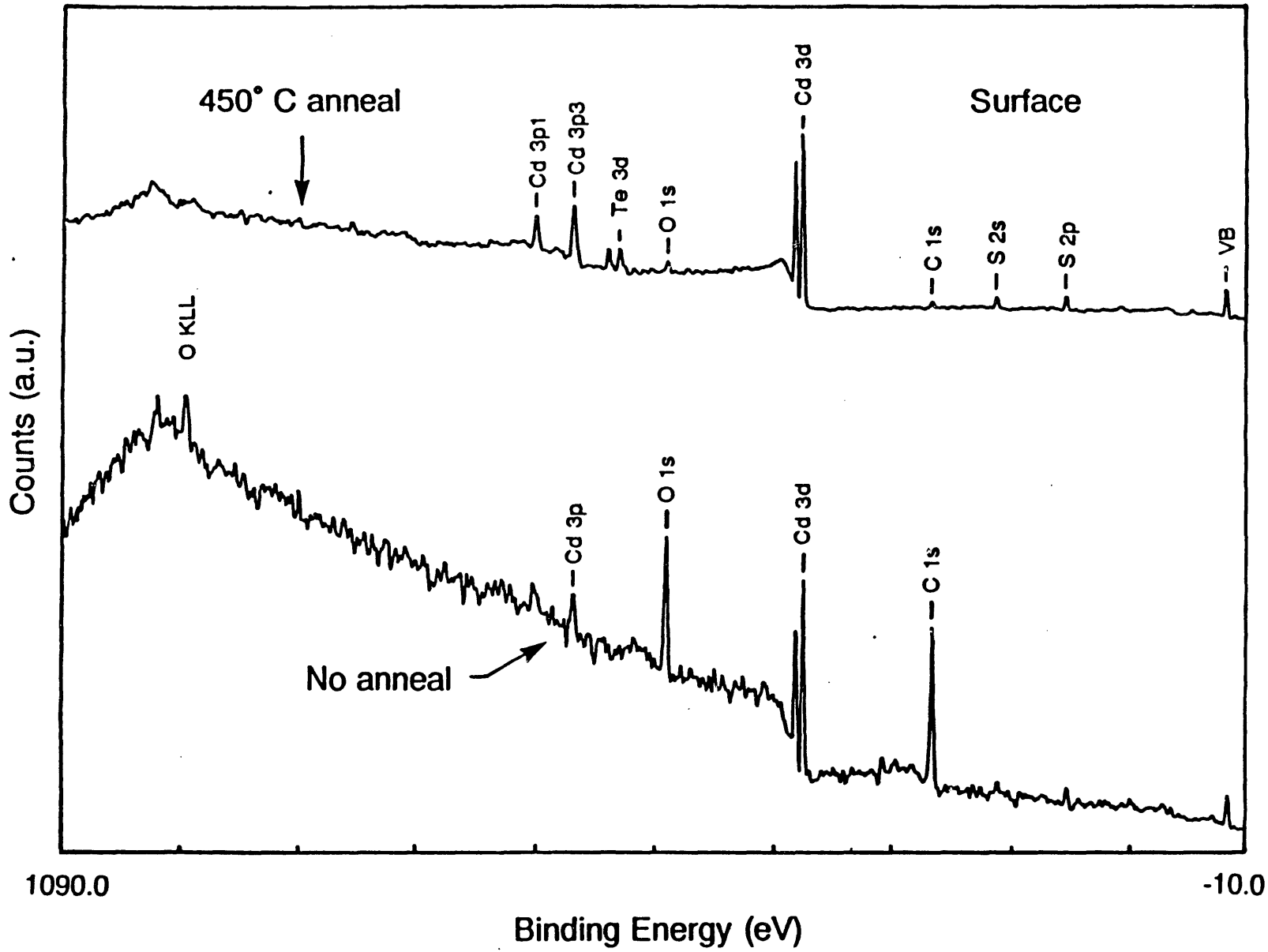


Figure 2.1.4 **XPS data on the surfaces of CdS substrates before and after annealing at 450° C in hydrogen atmosphere inside the MOCVD reactor.**

untreated cells.

Although, the thermal cleaning of CdS/SnO_2/glass substrates improves the final device performance, it also introduces some undesirable effects on CdTe/CdS devices. Figure 2.1.5 shows a comparison of AES spectra of CdS/SnO_2/glass substrates before and after 450°C anneal.

The Cd/S ratio was found to be uniform and higher on the surface of the unannealed films compared to the bulk CdS. It is known that due to high vapor pressure and growth temperature (450° C) of CdS films, sulfur evaporates from CdS surface during deposition thus causing a higher Cd/S ratio on the surface (8). Also, the Cd/S ratio was found to be higher on the surface of CdS films annealed up to 400° C. However, in the case of substrates annealed at 450° C AES spectrum on CdS surface showed Cd depletion. Since CdS films were grown at a temperature of 450° C, it is possible to have evaporation of Cd from CdS. Also, for a particular annealing temperature, the surface of CdS had varying Cd/S ratios indicating a non-uniform composition (figure 2.1.6). This may have adverse effect on large area devices, where uniformity is important.

The undesirable heat treatment effects, described above, significantly alter the I-V characteristics of electrochemical Schottky barrier formed on CdS film, as shown in figure 2.1.7. The forward bias I-V curve of the substrate without any heat treatment has a single slope indicating one dominant transport mechanism whereas CdS films annealed at 450° C show two different slopes. This suggests that the annealing-induced Cd depleted layer (figure 2.1.6) may have defects which provide an alternative current path at lower voltages which may degrade CdTe/CdS device performance by increasing diode current. In

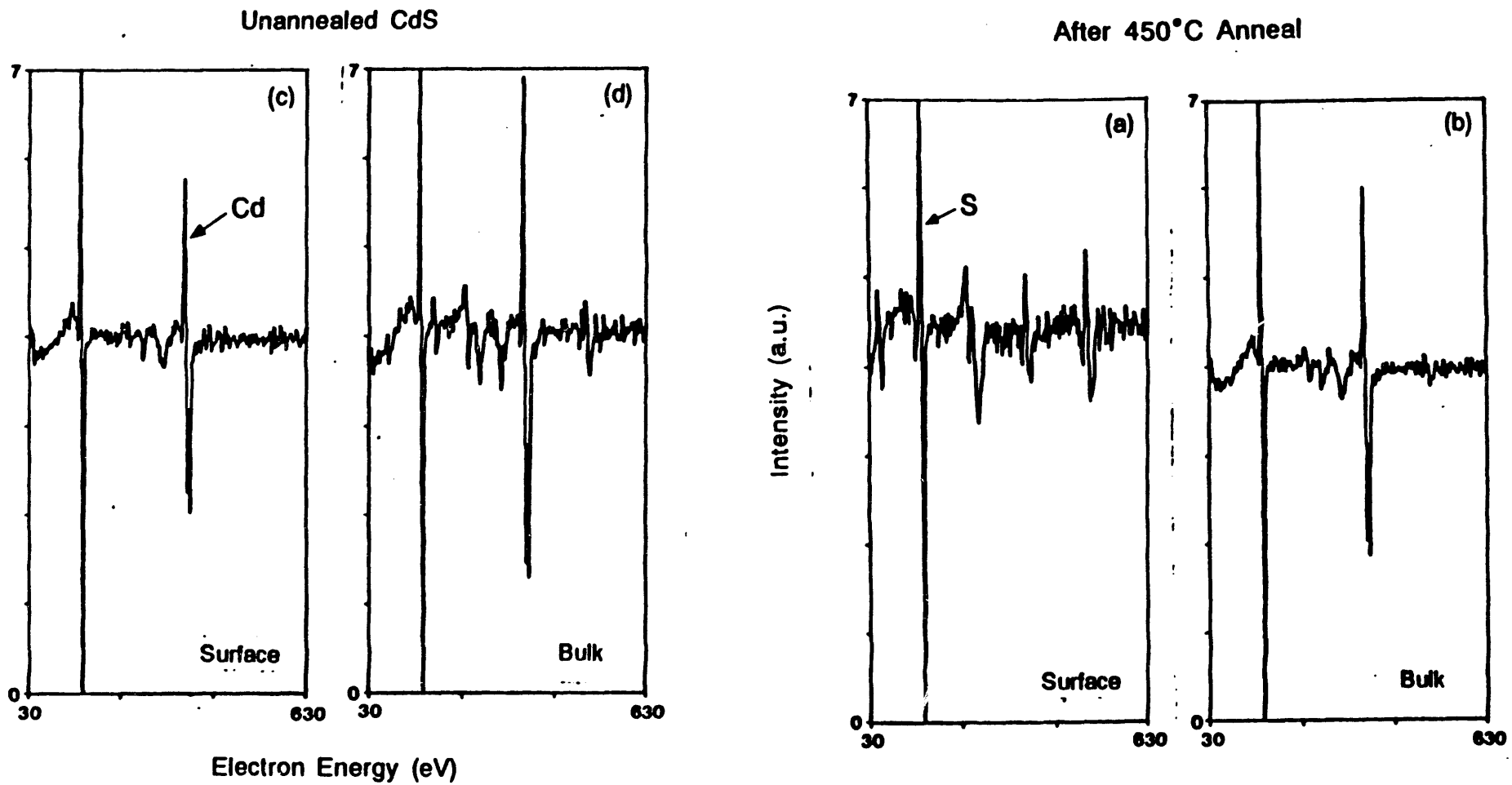


Figure 2.1.5 **Comparison of AES spectra of CdS/SnO_2/glass substrates before and after 450 C anneal taken at the surface and after 2 *min* sputtering.**

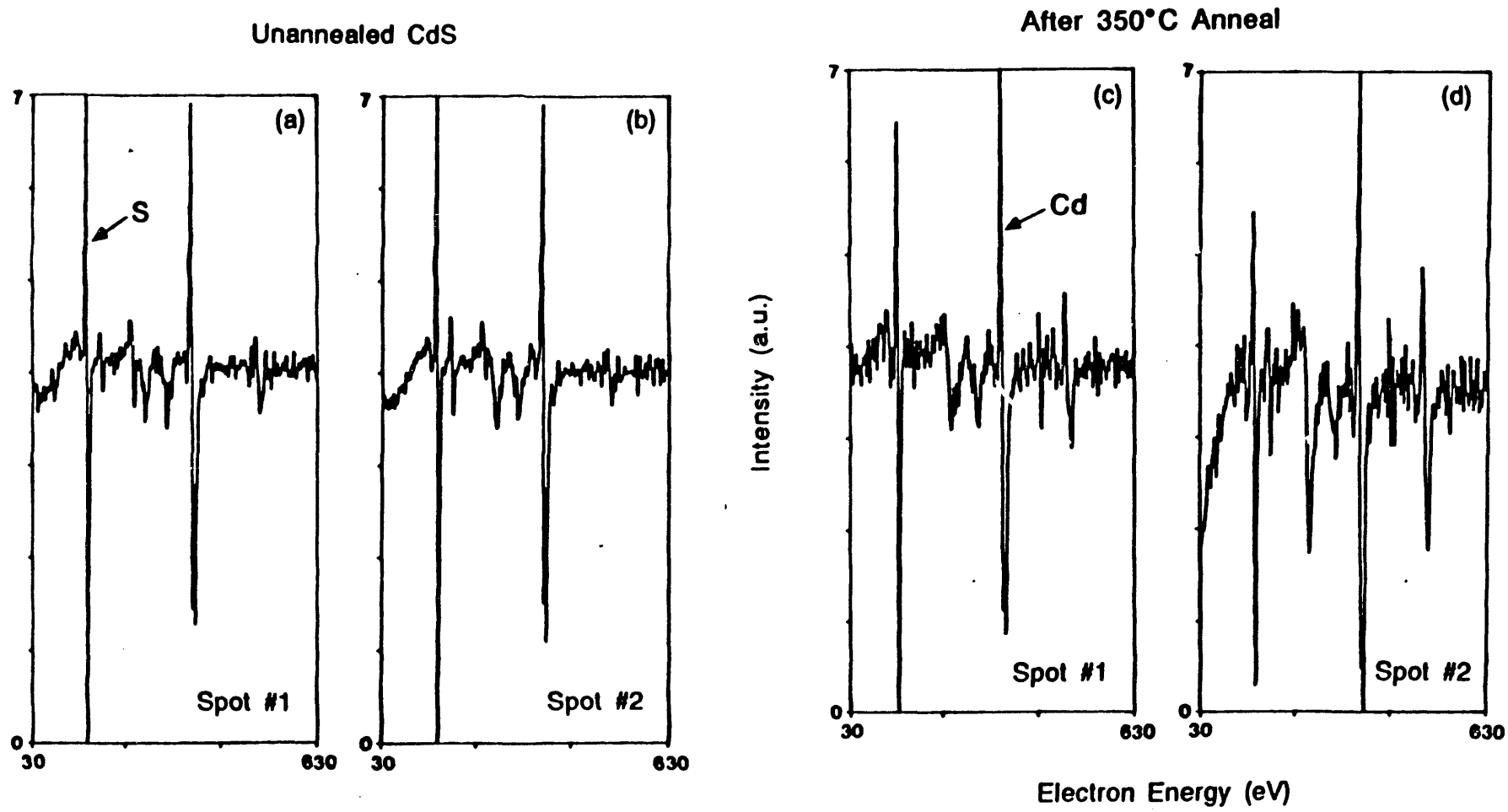


Figure 2.1.6 **The AES spectra taken at two different spots on CdS surface of unannealed and annealed substrates.**

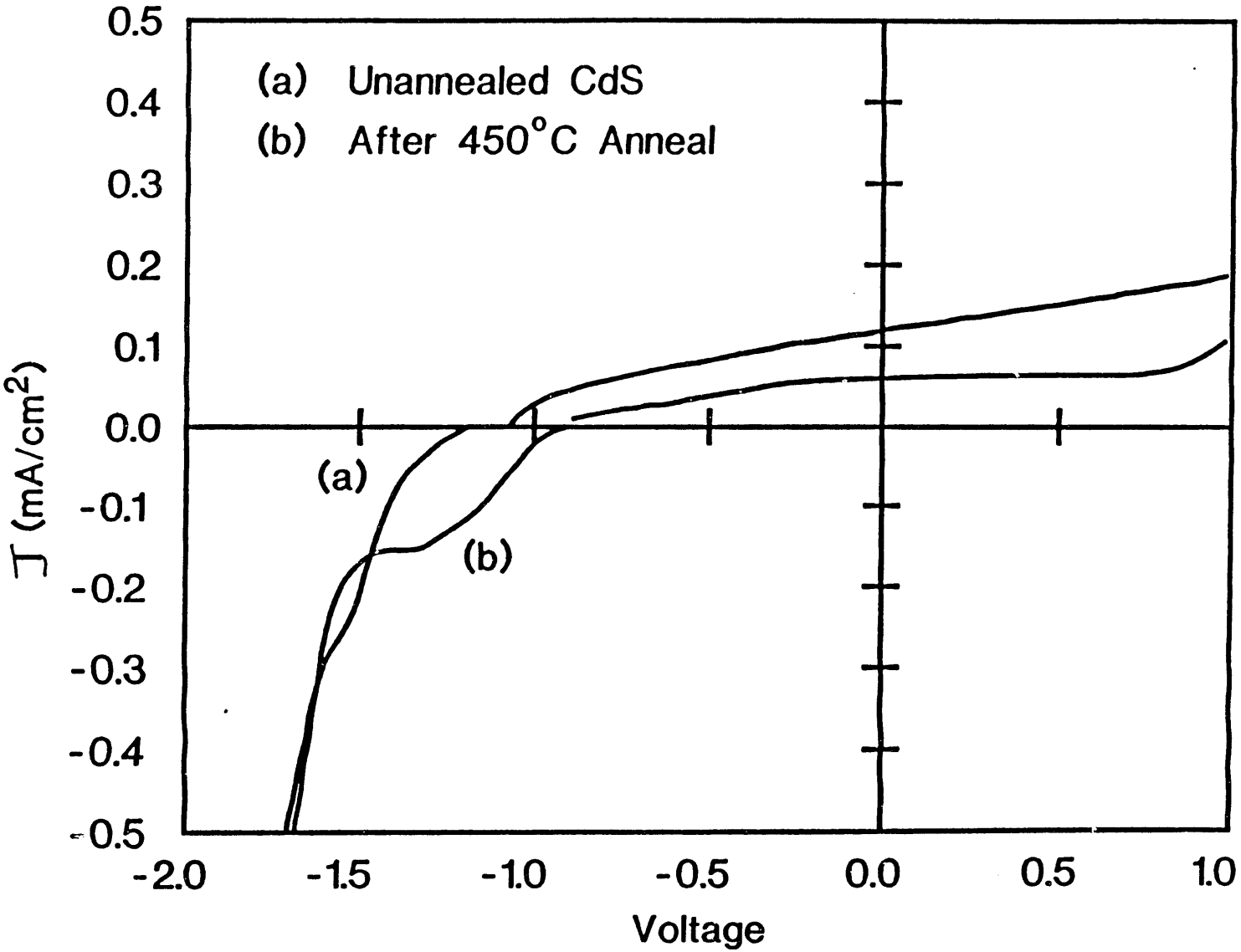


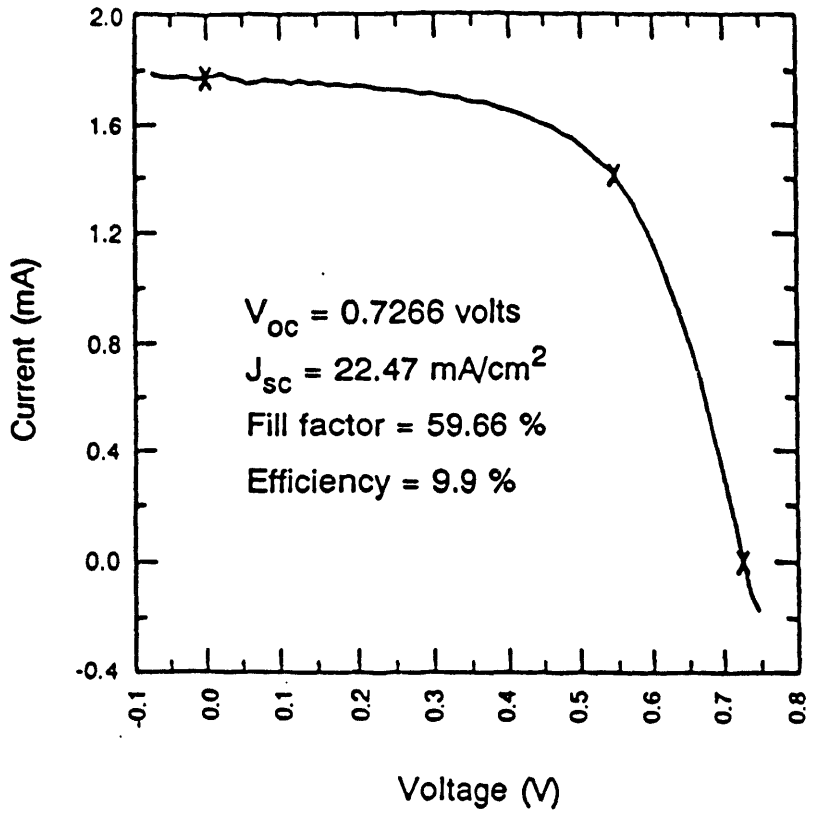
Figure 2.1.7 **Electrochemical I-V data of CdS/SnO_2/glass substrates before and after 450 C anneal.**

addition, some investigators have reported (12,13) that presence of a CdS layer with lower carrier concentration near the CdTe/CdS junction will reduce the open circuit voltage. This has been experimentally verified in $CuInSe_2$/CdS solar cells by growing an insulating layer of CdS near the heterojunction. Hence, even though devices made on the annealed substrates gave better efficiency, annealing-induced undesirable effects may limit further improvement in efficiency for a given cell design unless fabrication process and design are optimized.

Figures 2.1.8-2.1.9 show the comparison of light I-V and bias dependent spectral response of 9.7% p-i-n and 9.9% p-n CdTe cells. The cell parameters are similar, and in both cases the spectral response is fairly uniform with sharp cut-off indicating that bulk recombination does not play a major role in the collection efficiency in either cell. However, the spectral response of both cells show a strong wavelength independent bias dependence, suggesting that defects at the CdS/CdTe interface are limiting the performance of these cells by making the interface recombination velocity sensitive to applied bias (11).

Attempts were made to improve the interface quality by (a) controlling CdTe film deposition conditions, (b) adjusting CdTe stoichiometry and (c)varying the in-situ preheat treatment of CdS in hydrogen atmosphere prior to CdTe deposition.

The fact that the 10% efficient cells, subjected to this 450° C/15 min. preheat treatment, showed a strong bias dependence in the spectral response, suggests that preheat treatment is necessary but not sufficient to eliminate the detrimental effects of interface recombination. However, depth resolved AES measurements made on the



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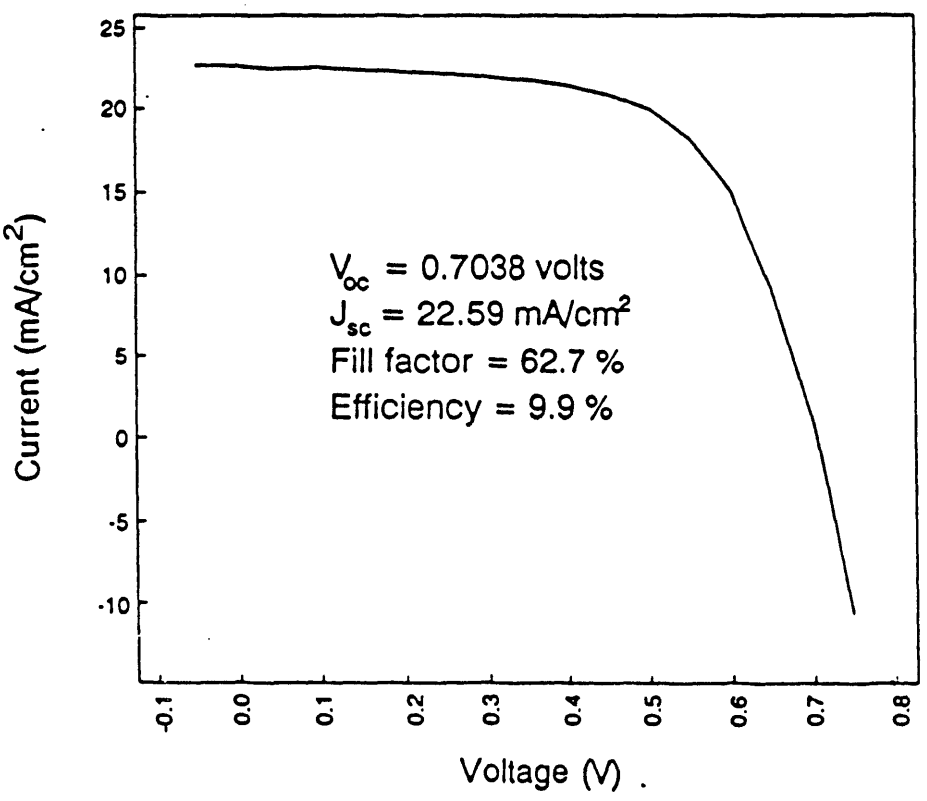

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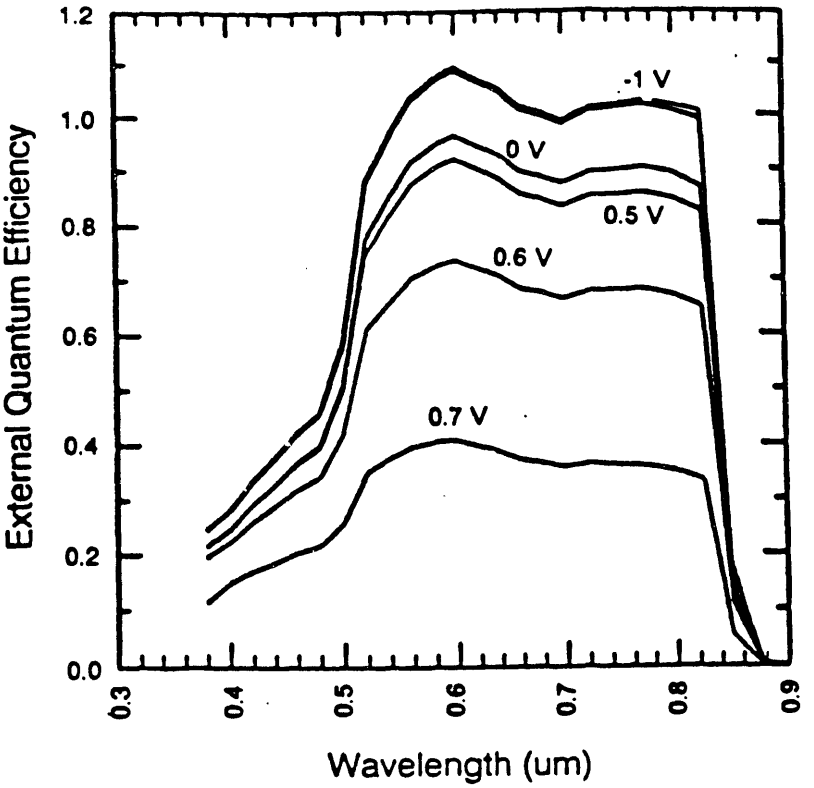
Figure 2.1.8 **Comparison of light I-V data of 9.7% efficient p-i-n and 9.9% p-n MOCVD-grown CdTe cells.**



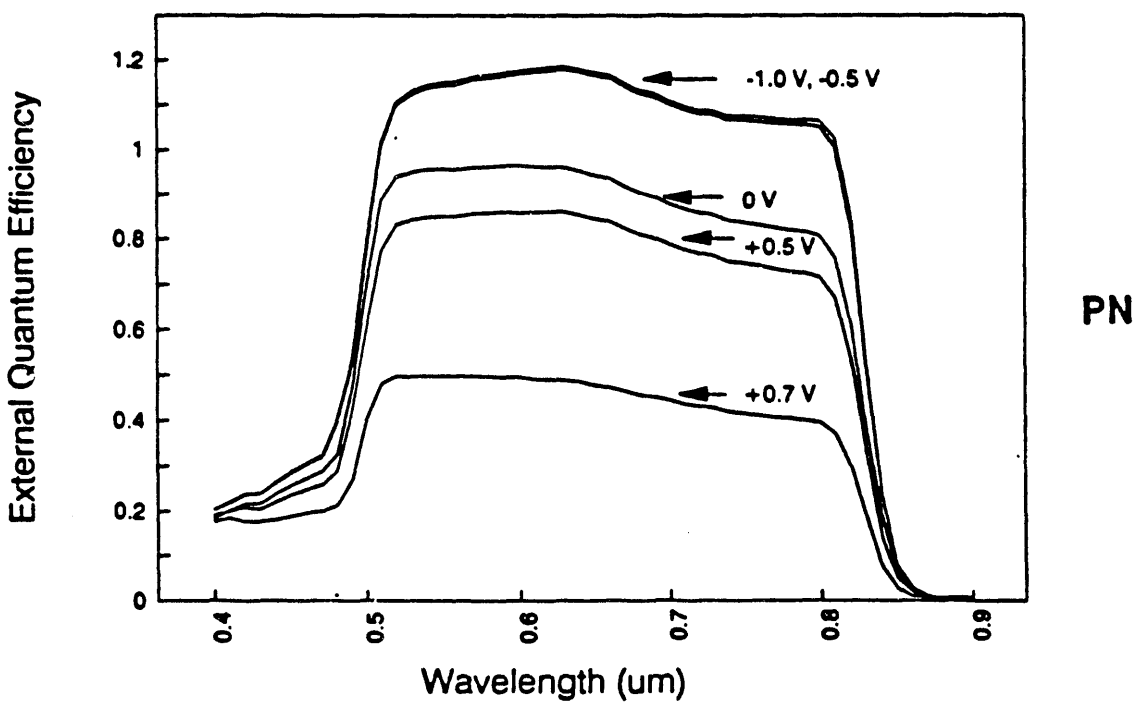


Figure 2.1.9 **Comparison of bias dependent spectral response data of 9.7% p-i-n and 9.9% p-n CdTe cells.**

annealed CdS film showed that 450° C heat treatment in hydrogen causes the CdS surface to become Cd-deficient (Cd/S < 1) in addition to removing oxygen. It is well known that Cd deficiency in CdS gives rise to an acceptor type defect level which is situated at 0.26 eV above valence band (14). This can produce a high resistive CdS surface layer, which is known to reduce V_{oc} and fill factor in $CuInSe_2$/CdS solar cells (12). A similar mechanism is possible in CdTe/CdS cells which may in part be responsible for limiting the efficiency to 10%.

Since Cd deficiency in CdS is a potential source of interface defects, one way of reducing such defects is to grow CdTe in Cd-rich conditions. This was attempted by gradually increasing the Cd/Te ratio in the vapor from 0.4 to 4.0. It should be noted that the 10% cells were grown with Cd/Te ratio of 0.4, in a Cd deficient ambient. The SPV responses of these films were measured with light incident on the CdTe side. Figure 2.1.10 shows electrochemical SPV spectra of CdTe films grown on CdS with various Cd/Te ratios. In order to separate the electrolyte-CdTe junction contribution from CdTe/CdS interface contribution, SPV response only in the long wavelength region is shown in the figure. It is interesting to note that the Cd-rich films show a significant increase in the surface photovoltage suggesting that the excess Cd in the CdTe film is eliminating the Cd deficiency at the CdS/CdTe interface. Since SPV response is an indicator of V_{oc}, it is possible to expect higher V_{oc} on films grown under Cd-rich condition compared to 9.7% efficient CdTe cells grown in Te-rich ambient. The films are now being subjected to the standard post deposition 400° C/30 min. air anneal for cell fabrication. If the higher SPV response is maintained throughout the cell processing, then we should

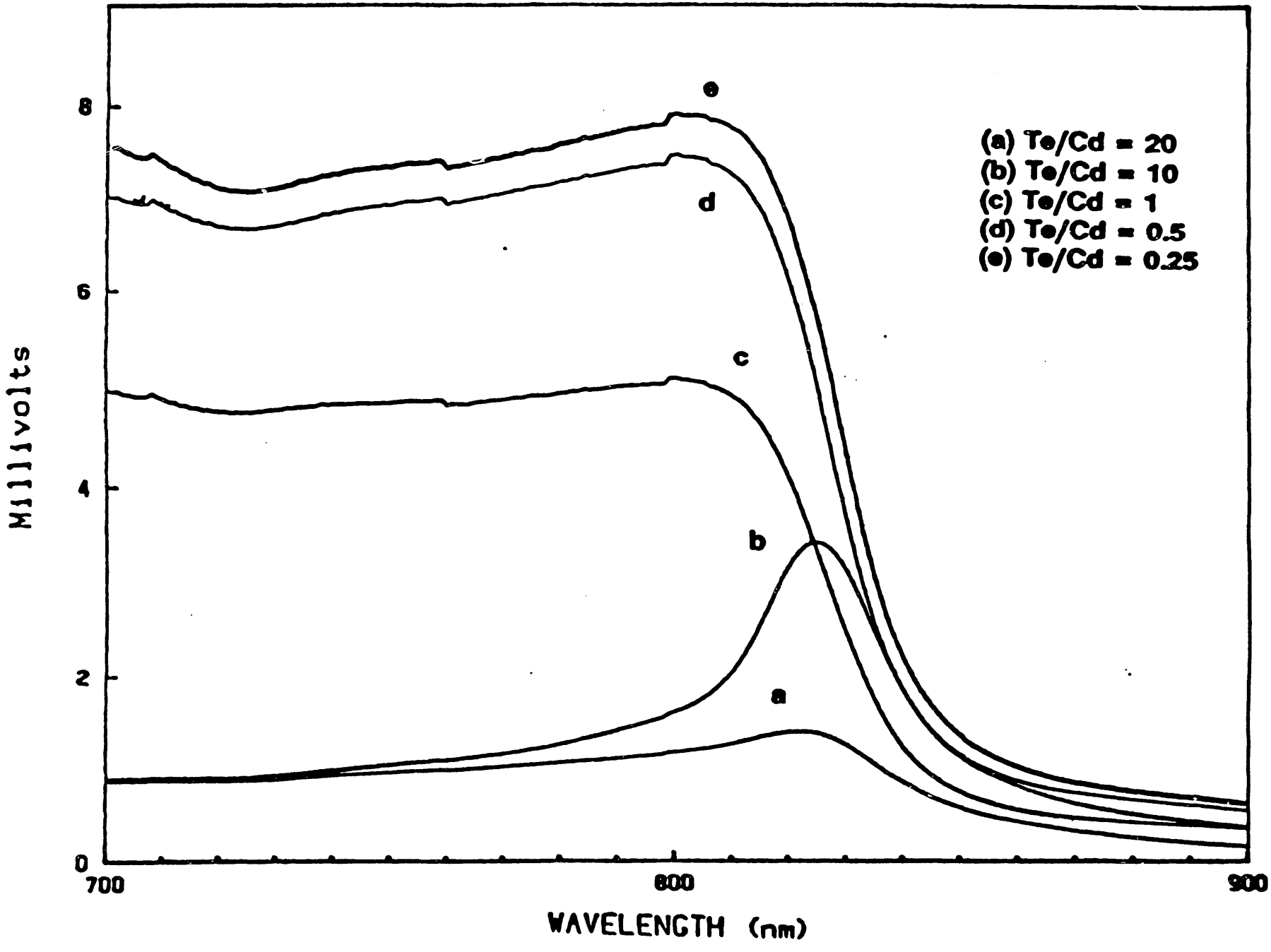


Figure 2.1.10 SPV spectra of CdTe films grown by MOCVD on CdS/SnO_2/glass substrates with different Cd/Te ratios.

be able to attain a higher V_{oc} and efficiency compared to the 10% efficient cells.

In order to estimate the maximum attainable efficiency due to the improved quality of the CdTe/CdS interface, model calculations were performed by using a collection function approach. This was done by first calculating the collection function (ratio of zero bias quantum efficiency to quantum efficiency at different bias voltages) as a function of applied bias using bias dependent spectral response data (figure 2.1.9). The loss in V_{oc} and fill factor due to the collection function were calculated according to (11,12):

$$\Delta V_{oc} = (AKT/q)\ (\ln\eta(V_{oc})$$

$$\Delta FF = (V_{mp}/V_{oc})(1-\eta(V_{mp})$$

For 9.7% efficient MOCVD CdTe cell, the calculated loss in V_{oc} and fill factor were 0.05 V and 0.12, respectively. In addition, reverse bias spectral response measurements indicate (figure 2.1.9) an additional loss of at least 10% (1.5 mA/cm^2) in J_{sc} due to interface recombination. If these losses can be eliminated by improving the interface quality then we project that cell efficiencies of 13.5% can be achieved from the MOCVD CdTe cells.

Further improvement in efficiency can be achieved by eliminating the loss due to absorption of high energy photons in the thick (1500 Å) CdS window layer. The 10% cells had ~1500 Å of CdS on SnO_2, and the estimated loss in J_{sc} due to absorption is 4 mA/cm^2 (2). This results in an additional loss of 0.02 volts and 0.08 in V_{oc} and fill factor, respectively. Thus, by eliminating this loss mechanism along with the interface

recombination, it is possible to achieve 18% efficient CdTe cells. Attempts are being made to deposit thin CdS films by the chemical immersion method (15). We have successfully grown CdS films in the thickness range of 400 to 1400 Å by controlling the immersion time and have found an appreciable improvement in the transmission of 400 Å CdS film in the short wavelength range. Thus a combination of optimum preheat treatment, proper Cd/Te ratio, and thin CdS films should yield a significant improvement in the MOCVD CdTe cell efficiency.

2.1.4. Conclusions

Thermal cleaning of CdS/SnO_2/glass substrates prior to CdTe deposition by MOCVD has both beneficial and detrimental effects on the CdTe/CdS device performance. The beneficial effects include a) removal of contaminants and impurities from the surface and reduction in the surface states, b) increase in the series resistance of the device, and d) higher open circuit voltage, fill factor, and cell efficiency.

Annealing induced deleterious effects include the formation of a non-stoichiometric CdS surface and a thin layer of Cd depleted CdS underneath the surface. Even though thermal treatment produces a net improvement in cell efficiency these undesirable effects will eventually limit further improvement in CdTe/CdS cell efficiency, unless fabrication process and design are optimized.

MOCVD grown polycrystalline CdTe solar cells with efficiencies of ~ 10% were demonstrated using both p-i-n and p-n structures. In-situ pre-heat treatment of glass/SnO_2/CdS substrates at 450° C for 15 minutes prior to CdTe deposition was found

to be essential for high performance devices because it removes oxygen and related defect states. The heat treatment also simultaneously makes the CdS surface Cd-deficient resulting in Cd vacancy-related interface states because of which even the 10% efficient cells show a strong bias dependent spectral response and lower V_{oc} and fill factor compared to the best reported (2) cells. Preliminary model calculations suggest that the removal of these states can increase the cell efficiency from 10% to 13.5 %. Photon absorption in the CdS film also limits the cell performance and elimination of this loss mechanism can result in efficiencies in excess of 18%.

2.2 The Effects Of $CdCl_2$ On The Electronic Properties of Beam Epitaxially Grown CdTe/CdS Heterojunction Solar Cells

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2.2.1 Introduction

High efficiency (~ > 10%) polycrystalline CdTe/CdS solar cells have been fabricated by electrodeposition (1), physical vapor deposition (2), close-spaced vapor transport (CSVT) (3), sintering (4), metalorganic chemical vapor deposition (MOCVD) (5), and molecular beam epitaxy (MBE) (5). To obtain high efficiency in all of these approaches, it is necessary to have CdTe grain sizes of ~ 1 um or greater to avoid significant bulk recombination, large interface state density, and high sheet resistance. A commonly used procedure to enhance the grain size and density the CdTe film is the introduction of an annealing (or sintering) aid such as $CdCl_2$ either during or after CdTe film growth (6-8). The influence of the $CdCl_2$ treatment on CdTe microstructure and solar cell performance has been previously investigated for CdTe films prepared by a high temperature (T > 600 C) sintering process (6-8) which requires incorporation of $CdCl_2$ in the CdTe slurry prior to CdTe film formation. This method has resulted in CdTe cell efficiencies in excess of 10%. However, polycrystalline CdTe films prepared by techniques such as electrodepostion, physical vapor deposition, MBE and MOCVD require a post-deposition heat treatment in the presence of $CdCl_2$ to obtain high efficiency (9). To date, the observed beneficial effects of the $CdCl_2$ treatment on device characteristics and performance are at best qualitatively understood. In order to improve present-day CdTe/CdS cell efficiency beyond 12-13%, it is necessary to quantify and

improve the fundamental understanding of process-induced effects on the bulk and interface properties of these cells.

In this paper, MBE-grown polycrystalline CdTe/CdS solar cells are investigated to quantify the mechanisms responsible for improved cell performance due to the $CdCl_2$ treatment and reveal process-induced defects which may dictate the device characteristics after the $CdCl_2$ treatment. First, microstructural changes in the CdTe films due to post-deposition annealing with and without the $CdCl_2$ dip are investigated by scanning electron microscopy (SEM). Second, electrochemical surface photovoltage (SPV) and bias-dependent spectral response measurements are used to estimate the improvement in bulk and interface quality of the CdTe/CdS cells due to the $CdCl_2$ treatment. Third, the dominant current transport mechanisms in CdTe/CdS cells processed with and without the $CdCl_2$ treatment are studied by current density-voltage-temperature (J-V-T) analysis. Finally, Deep Level Transient Spectroscopy (DLTS) measurements are performed to identify traps which may dominate the current transport and limit the $CdCl_2$-treated CdTe/CdS cell performance. Attempts are made to correlate transport mechanisms and traps within the CdTe cells to film microstructure, SPV and spectral response, and solar cell performance in order to provide guidelines for achieving higher efficiencies.

2.2.2. Experimental Techniques

A. CdTe Growth and Cell Processing

Polycrystalline CdTe films were grown to a thickness of 2 um by MBE on n-type

CdS/SnO_2/glass substrates suitable for solar cell applications. (10) Prior to CdTe deposition, the surface doping density of the CdS was found to be $5x10^{16}$ cm^{-3} by electrochemical C-V measurements. After the CdTe film deposition, CdTe/CdS structures were dipped in a saturated $CdCl_2$:CH_3OH solution and then annealed in air at 400 C for 35 minutes. (5,9) Selected samples from the same growth run were annealed in air at 400 C for 35 minutes without the $CdCl_2$ solution to distinguish the effects of $CdCl_2$ on CdTe material and device properties. Cell fabrication was completed by etching the annealed CdTe surface in ~ 0.1% Br_2:CH_3OH, to remove residual surface oxides, followed by a DI water rinse and blow dry in N_2. Ohmic back contacts were formed on the etched CdTe surface by evaporating 150 nm of Cu-doped ZnTe capped with 200 nm of Ni. (5)

B. Microstructural Studies

The grain size of the as-grown and processed CdTe/CdS structures was determined by SEM. A beam voltage of 15 KV was used. To prevent sample charging effects, the CdTe surfaces were coated with 10 nm of gold.

C. Electrochemical Surface Photovoltage and Spectral Response Measurements

Process-induced effects on bulk and junction quality were monitored by electrochemical SPV measurements, using the Polaron PN4200 electrochemical profiler with the PN4250 photovoltage spectroscopy accessory. The CdTe/CdS/SnO_2/glass structures in the as-grown state, after air anneal, and after the $CdCl_2$ dip followed by air anneal were analyzed in detail. A 0.2M NaOH + EDTA (ethylenediaminetetraacetic acid)

solution was used to form an electrochemical Schottky barrier to the CdTe surface and ohmic contact was made to the underlying SnO_2 with Indium. The samples were illuminated from the CdTe side, through the electrolyte, by chopped light in the wavelength range of 700 -900 nm and the resulting photovoltage was measured under open-circuit conditions to avoid etching of the CdTe film by the electrolyte. The net open-circuit SPV signal at each wavelength is the difference between the internal photovoltages generated at the surface barrier and CdTe/CdS heterojunction (11). To accurately compare material and junction quality of different CdTe/CdS samples, it is necessary for the CdTe film thicknesses and doping to be identical to insure that the same carrier generation profile is seen by the collecting junctions in all of the samples. Our SPV setup uses low illumination intensity such that the SPV magnitude is much less than kT. In this case, it has been shown that the photovoltage generated at the CdTe/CdS heterojunction, ignoring the presence of the electrolyte/CdTe surface barrier for now, can be approximated as (11,12)

$$SPV(\lambda) = V_{oc}(\lambda) = [nkT/q]ln(J_{PH}/J_0 + 1) \approx [nkT/q][J_{PH}/J_o] = [nkT/J_o]F(\lambda)R(\lambda) \quad (1)$$

where n is the heterojunction ideality factor, J_o is the "effective" junction leakage current density, $F(\lambda)$ is the photon flux absorbed in the quasi-neutral CdTe bulk, and $R(\lambda)$ is the spectral response function which is comprised of contributions from the quasi-neutral and depletion regions of both the CdTe and CdS and reflects bulk material quality (12). Note that the contributions from the CdS layer to $R(\lambda)$ can be ignored since the minimum

wavelength (maximum energy) of the photons incident on the CdTe surface was chosen to be 700 nm (1.77 eV) which will not be absorbed by the 2.42 eV bandgap CdS layer. Hence the magnitude of the SPV signal is proportional to both the CdTe/CdS junction quality, through J_o and n, and CdTe material quality through $R(\lambda)$. The final SPV spectrum is normalized to a calibrated photodiode to eliminate flux variations and the spectrometer response.

To support the results from the above SPV analysis, bias-dependent spectral response measurements were performed on completed CdTe/CdS cells processed with and without $CdCl_2$. A.c. photocurrent measurements were made with O volts d.c. and -0.5 volts d.c. reverse bias applied across the device.

D. Dark J-V-T and Light J-V Measurements

Dark J-V-T measurements were performed to determine the current transport mechanisms in CdTe/CdS devices fabricated with and without the $CdCl_2$ treatment. J-V data were measured in the temperature range of 180 - 320 K in 10 K increments using an automated J-V-T setup. The J-V characteristic at each temperature was fitted to a parallel double diode equivalent circuit model with shunt resistance, R_s, described by

$$J = J_1 + J_2 + (V - JR_s)/R_{sh} \qquad (2)$$

where

$$J_1 = J_{01}[exp[(q/A_1kT)(V - JR_s)] - 1] \qquad (3)$$

and

$$J_2 = J_{02}[exp[(q/A_2kT)(V - JR_s)] - 1] \quad (4)$$

A multivariable regression analysis was used to fit the data and obtain J_{01}, J_{02}, A_1, A_2, R_s, and R_{sh} with less than 5% error in the fit over the entire voltage range. The temperature dependence of these parameters was used to determine current transport mechanisms in each device. Solar cell data were determined by lighted J-V measurements taken at 300 K under 100 mW/cm^2 AM1.5 conditions.

E. Deep Level Transient Spectroscopy (DLTS) Measurements

DLTS measurements were performed on Ni/ZnTe/CdTe/CdS/SnO_2/glass structures annealed with and without $CdCl_2$ to identify traps within the CdTe depletion. DLTS data were taken using an automated DLTS spectrometer in a lock-in amplifier type arrangement. The output signal was integrated and analyzed using five different weighting functions from 4 msec. to 64 msec. A pulse width of 8 ms. was necessary to saturate the detectable traps. Since the CdTe doping concentration ($5x10^{15}$ cm^{-3}, as determined by C-V measurements) is much less than that of the CdS, only the CdTe depletion region is probed. A steady reverse bias of -400 mV was used and a pulse of + 300 mV was applied to scan the CdTe depletion region. Spatial trap distributions were measured by varying the reverse steady bias from -400 mV to -100 mV, but keeping the sum of the reverse steady bias and the pulse height constant at - 100 mV. In this way, the edge of the depletion region is stepped toward the CdTe/CdS interface as the steady

reverse bias is decreased to provide a spatial trap profile in the CdTe depletion. The temperature of each device is monitored by a thermocouple mounted directly on a glass slide of identical thickness to the glass substrate of the CdTe/CdS device which was situated adjacent to the device under test. Trap activation energies and cross-sections were determined from the $\log(T^2/e_m)$ vs. 1000/T Arrhenius plot. The trap emission rate, e_{mp}, for majority carrier holes in the CdTe is given by

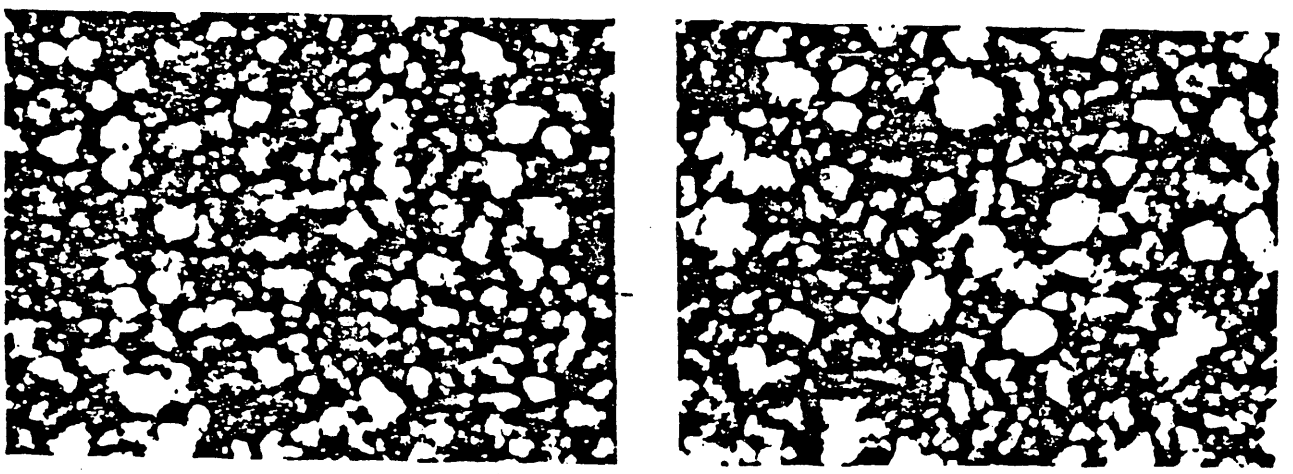
$$e_{mp} = N_v \sigma_p v_{th} exp[(E_v - E_T)/kT] \qquad (5)$$

where the terms in eq. (5) have their usual meanings. (13)

2.2.3. Results and Discussion

A. Effects of $CdCl_2$ Treatment on MBE-grown Polycrystalline CdTe Films and Solar Cells

The $CdCl_2$ dip prior to post-deposition annealing of small grain CdTe films grown by electrodeposition and physical vapor deposition has been previously shown to be necessary for grain growth and cell efficiencies in excess of 10%. (2,6-9) We have found the same to be true for MBE-grown polycrystalline CdTe. The SEM photomicrographs shown in Figure 2.2.1 indicate an estimated increase in average grain size from ~ 0.25 um for the as-grown and air annealed films without a $CdCl_2$ dip to ~ 1 um for the $CdCl_2$ treated and annealed films. Note that little or no grain growth is evident for the air annealed CdTe film without the $CdCl_2$ treatment. It is likely that the presence of $CdCl_2$ during the anneal induces a sintering mechanism within the CdTe film that acts to



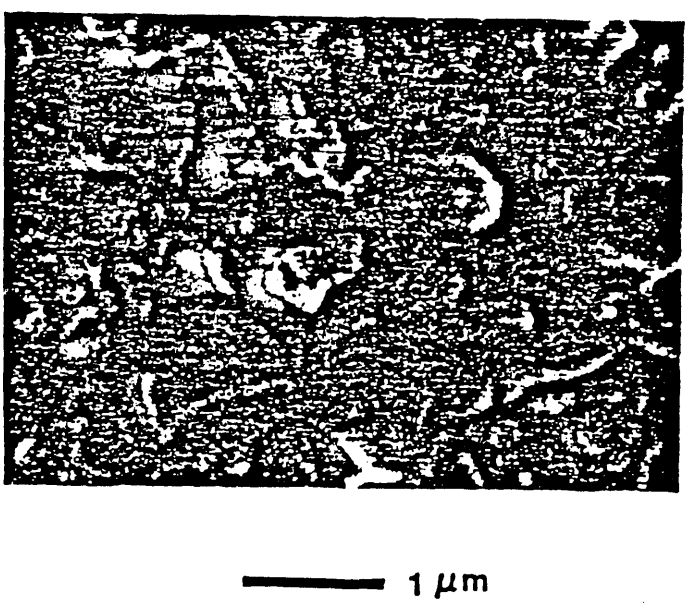


Figure 2.2.1 SEM photomicrographs of (a) as-grown CdTe, and CdTe annealed in air at 400 C for 35 minutes (b) without $CdCl_2$ and (c) with $CdCl_2$.

decrease inter-grain pore size and increase average grain size. (7) The effect of this grain growth on solar cell performance is shown in Table 2.2.1 which indicates a dramatic improvement in all solar cell parameters, with the efficiency increasing from 1.3% to 8.6%.

B. Effect of $CdCl_2$ Treatment on the Photoresponse of CdTe/CdS Structures

CdTe grain growth is expected to reduce the bulk and interface state density which tend to influence the spectral response and leakage current of the fabricated device. In order to directly assess the effects of $CdCl_2$ treatment on recombination at the CdTe/CdS junction and in the CdTe bulk, SPV measurements were performed on CdTe/CdS structures with and without the $CdCl_2$ treatment, prior to back contact (ZnTe + Ni) deposition. Samples of identical thickness from the same growth run, deposited on identical substrates, were used for the SPV analysis. Figure 2.2.2 shows the measured SPV spectra for (a) an as-grown sample, (b) a sample after air anneal and (c) a sample dipped in $CdCl_2$ followed by an air anneal. The as-grown CdTe/CdS structure (curve a) yields a small and flat SPV response prior to the CdTe bandedge ($\lambda \sim 850$ nm), while the air annealed structure without the $CdCl_2$ treatment exhibits a peak near the bandedge. This peak can be attributed to the p-type conversion of CdTe (14) and subsequent formation of a p-CdTe/n-CdS heterojunction after air annealing which aids in the collection of carriers generated close to and within the CdTe depletion layer (recall that light is incident on the CdTe side and not the CdS). However, even though annealing in air without $CdCl_2$ aids in the formation of the CdTe/CdS junction, little or no improvement in CdTe bulk diffusion length is evident based on the similar SPV response for shorter

Table 2.2.1 **AM1.5 solar cell data for MBE-grown ZnTe/CdTe/CdS devices processed with and without $CdCl_2$ fluxing agent.**

treatment	Voc (mV)	Jsc ($mA\text{-}cm^{-2}$)	FF	EFF (%)	Rs $\Omega\text{-}cm^2$)
no $CdCl_2$	385	10.5	0.32	1.3	3.6
with $CdCl_2$	720	23.1	0.51	8.6	.90

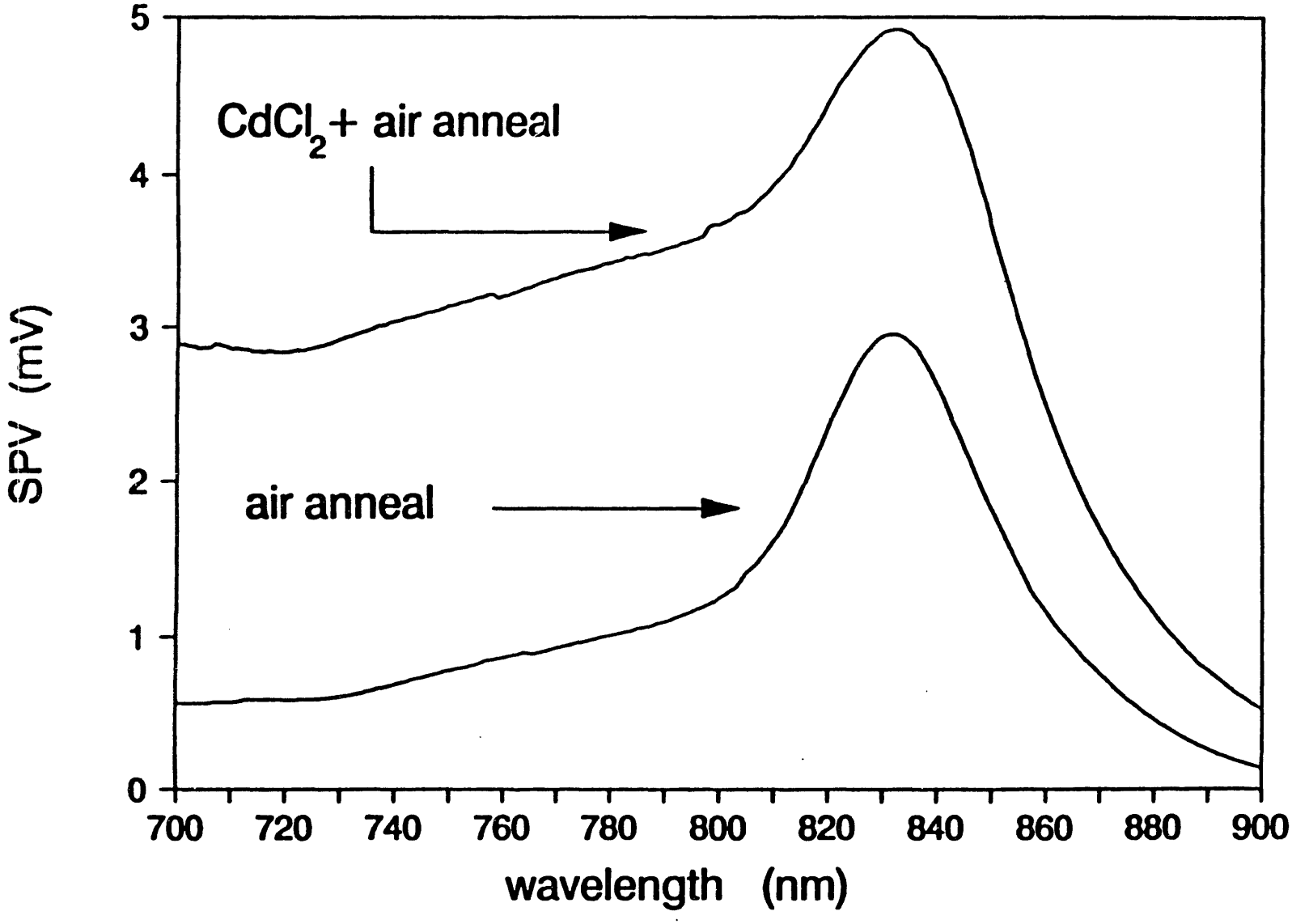


Figure 2.2.2 SPV spectra of as-grown, air annealed, and $CdCl_2$ + air annealed CdTe/CdS structures with light incidence on the CdTe surface.

wavelengths below the peak for both the as-grown and air annealed samples. In contrast, the SPV response of the CdTe/CdS structure annealed after the $CdCl_2$ treatment (curve c of Figure 2.2.2) is significantly larger at all wavelengths compared to the structure annealed without $CdCl_2$, suggesting an increase in effective carrier collection length and an improvement in CdTe bulk quality. Furthermore, the peak near the bandedge is even more pronounced after the $CdCl_2$ treatment suggesting additional improvement in the junction quality compared to CdTe/CdS annealed without the $CdCl_2$ dip. The trends in the SPV spectra are consistent with $CdCl_2$-induced grain growth shown in Figure 2.2.1 suggesting that the SPV improvement results from a decrease in the density of grain boundary states throughout the CdTe bulk and depletion region.

To investigate the role of the $CdCl_2$ treatment on interface quality, bias-dependent spectral response measurements were performed on solar cells fabricated from films annealed with and without $CdCl_2$. Figure 2.2.3 shows the spectral responses for each sample with and without an applied reverse bias, revealing three important results. First, a significant increase in absolute spectral response with the $CdCl_2$ treatment demonstrates reduced interface recombination and increased carrier collection length. Second, while the spectral response of both samples show a wavelength-independent increase with applied reverse bias, the spectral response of the $CdCl_2$ treated samples show a smaller bias dependence, suggesting an improved interface collection function (15) due to reduced number of defect states at or near the CdTe/CdS interface after $CdCl_2$ treatment. Both of these results are consistent with the SPV data. Finally, even after the $CdCl_2$ treatment, appreciable bias dependence in the spectral response is

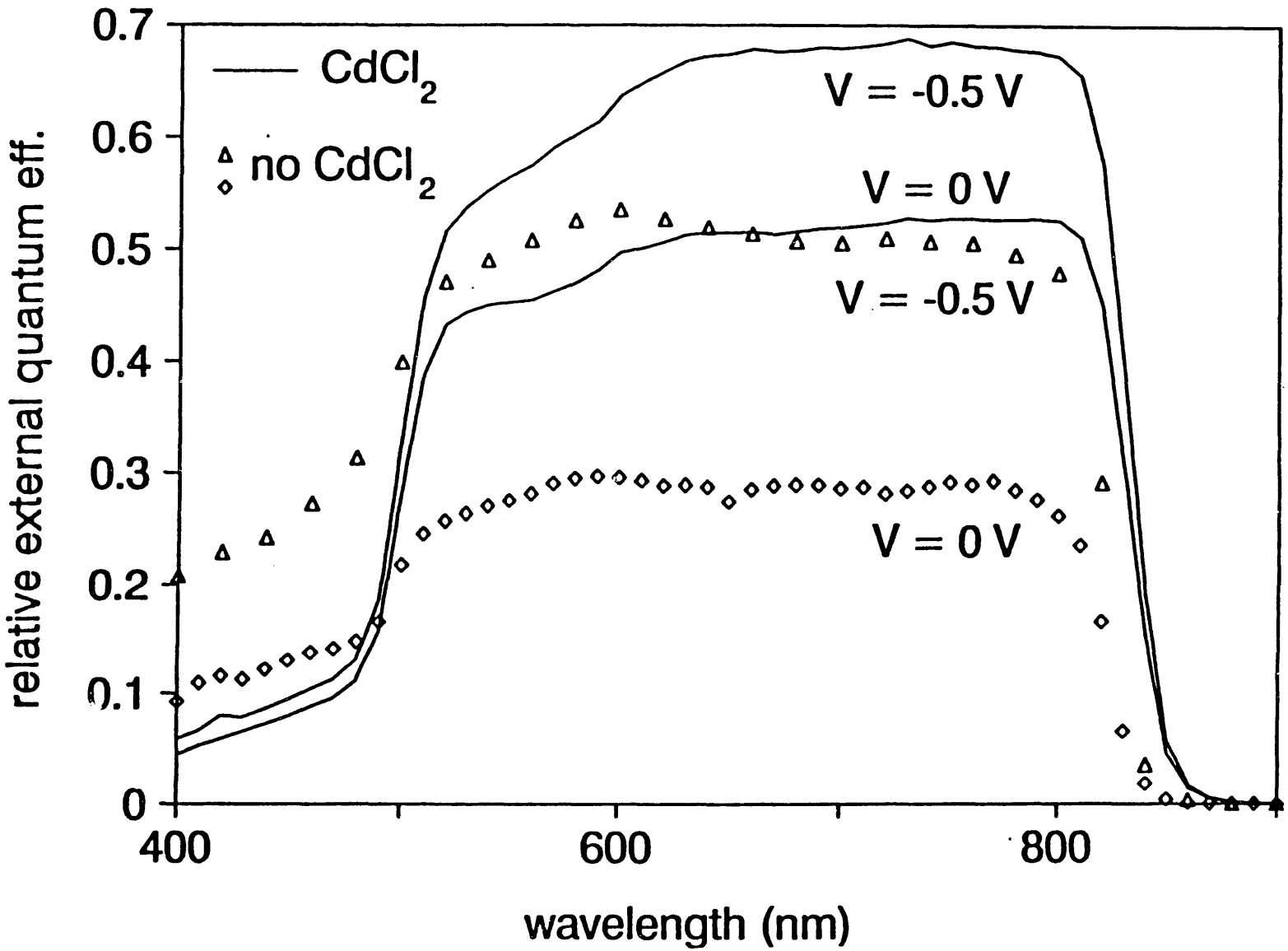


Figure 2.2.3 **Bias-dependent spectral response data of completed Ni/ZnTe/CdTe/CdS/SnO_2/glass solar cells with $CdCl_2$ (solid lines) and without $CdCl_2$ (symbols). The values of the applied reverse bias are noted.**

evident suggesting that there is still considerable interface recombination in this 8.6% efficient cell. The identification and elimination of the states responsible for this recombination is necessary to increase device performance further.

C. Effect of $CdCl_2$ Treatment on CdTe/CdS Junction Transport Properties

The dark J-V-T behavior of devices processed with and without the $CdCl_2$ process were analyzed to investigate the effect of the $CdCl_2$ treatment on the diode transport mechanisms in the CdTe/CdS cell. The measured and modeled dark lnJ-V characteristics of both samples are shown in Figure 2.2.4 as a function of temperature. Each lnJ-V curve was fit to the double diode equivalent circuit model described by eqs. (2) -(4), and the fitting parameters for each cell as a function of temperature are summarized in Tables 2.2.2 and 2.2.3. The lnJ-V characteristics are plotted with respect to the junction voltage (= $V-JR_s$) to reveal the junction transport. The deviation from linearity at higher bias voltages is due to the non-ohmic behavior of the back Ni/ZnTe/CdTe contact at larger bias voltages. (16) Figure 2.2.4 shows significant differences in the voltage dependence and magnitude of the diode current for devices processed with and without $CdCl_2$, suggesting a change in the dominant mode of current transport. To understand and quantify this difference, the dominant transport mechanisms in each cell are described in the remainder of this section. The dark current transport in the $CdCl_2$-treated cells above 220 K was best described by a single diode model, viz.,

Table 2.2.2 Dark J-V-T parameters extracted from fit to eqs. (2) - (4) for MBE-grown CdTe/CdS solar cell treated with $CdCl_2$ fluxing agent. Diode 1 (subscript 1) represent the higher voltage region of the J-V-T data and diode 2 (subscript 2) represent the lower voltage region of the J-V-T curves. α_1 and α_2 represent the slopes of the lnJ-V characteristics and $\alpha_2 = 1/A_2kT$ in the table.

T (K)	J_{o1} (Acm^{-2})	A_1	α_1	J_{o2} (Acm^{-2})	α_2	R_s (Ω-cm^2)
180	9.5×10^{-18}	2.16	29.8	4.3×10^{-13}	9.51	4.0×10^{6}
190	2.6×10^{-17}	2.05	29.8	7.9×10^{-13}	9.71	5.1×10^{5}
200	3.4×10^{-17}	1.90	30.5	2.5×10^{-12}	9.57	1.3×10^{5}
210	1.5×10^{-16}	1.75	31.6	6.5×10^{-12}	9.49	4.0×10^{4}
220	3.2×10^{-15}	1.78	29.6	-----	-----	9.8×10^{3}
230	3.2×10^{-14}	1.78	28.3	-----	-----	2.4×10^{3}
240	2.2×10^{-13}	1.77	27.3	-----	-----	9.5×10^{2}
250	2.1×10^{-12}	1.77	26.2	-----	-----	3.2×10^{2}
260	9.5×10^{-12}	1.77	25.2	-----	-----	1.8×10^{2}
270	4.4×10^{-11}	1.77	24.3	-----	-----	9.8×10^{1}
280	2.0×10^{-10}	1.77	23.4	-----	-----	6.0×10^{1}
290	8.5×10^{-10}	1.77	22.6	-----	-----	3.4×10^{1}
300	2.6×10^{-9}	1.75	22.1	-----	-----	2.4×10^{1}
310	8.1×10^{-9}	1.74	21.4	-----	-----	1.7×10^{1}
320	2.1×10^{-8}	1.73	21.0	-----	-----	1.5×10^{1}

Table 2.2.3 Dark J-V-T parameters extracted from fit to eqs. (2) - (4) for MBE-grown CdTe/CdS solar cell not treated with $CdCl_2$ fluxing agent. J-V data below 240 K was dominated by resistance terms and are not listed.

T (K)	J_{01} (Acm^{-2})	A_1	R_s (Ω-cm^2)
240	2.2×10^{-9}	3.02	3.5×10^{6}
250	4.0×10^{-9}	2.96	8.1×10^{5}
260	9.0×10^{-9}	2.92	2.4×10^{5}
270	2.4×10^{-8}	2.80	8.2×10^{4}
280	8.2×10^{-8}	2.76	2.8×10^{4}
290	2.3×10^{-7}	2.70	1.2×10^{4}
300	4.7×10^{-7}	2.63	6.6×10^{3}
310	9.8×10^{-7}	2.53	4.0×10^{3}
320	2.3×10^{-6}	2.50	1.9×10^{3}

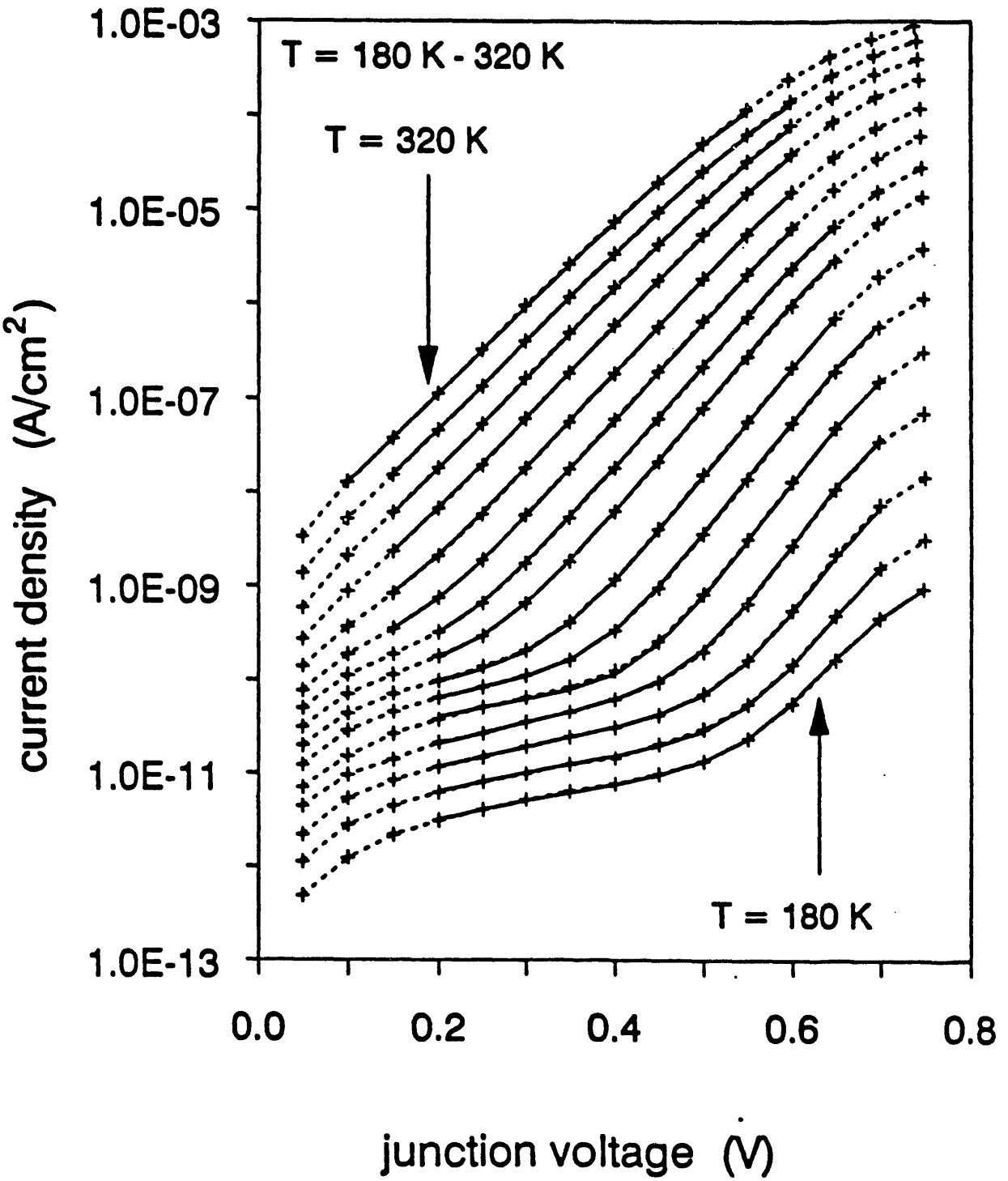


Figure 2.2.4 (a) Measured (symbols) and modeled (lines J-V-T data for (a) $CdCl_2$ + air annealed and (b) air annealed without $CdCl_2$Ni/SnTe/CdTe/CdS/SnO_2/glass solar cells. Shown is the current behavior as a function of junction voltage (V-JR). The average error of each fit is less than 5%.

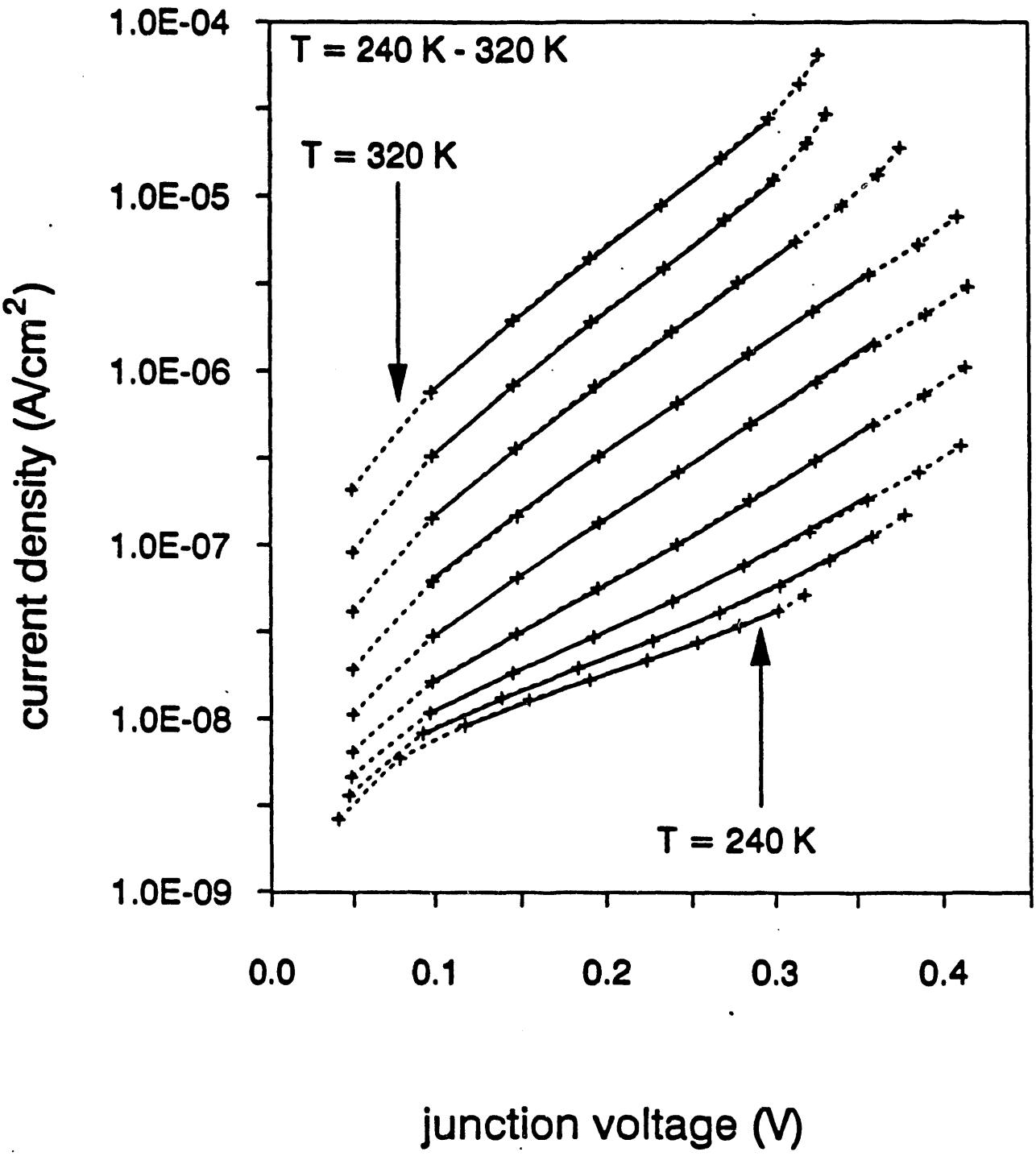


Figure 2.2.4 (b) Measured (symbols) and modeled (lines J-V-T data for (a) $CdCl_2$ + air annealed and (b) air annealed without $CdCl_2$Ni/SnTe/CdTe/CdS/SnO_2/glass solar cells. Shown is the current behavior as a function of junction voltage (V-JR). The average error of each fit is less than 5%.

$$J = J_{01}\{exp[(q/A_1kT)(V - JR_s)] - 1\} + (V - JR_s)/R_{sh} \quad (6)$$

where

$$J_{01} = J_{001}exp(-\Delta E/kT) \quad (7)$$

which is the general form for recombination-controlled current transport. (17) For interface recombination-dominated current transport, the value of A_1 should be ~ 1 for this device structure ($A_1 = 1 + (N_A\epsilon_{CdTe})/(N_D\epsilon_{CdS})$ for interface recombination) and the activation energy, ΔE, of the lnJ_{01} vs. 1000/T plot should be ~ 1.2 eV (built-in voltage of the CdS/CdTe junction). (18) Neither of these conditions were met for the $CdCl_2$-treated devices because $A_1 = 1.75$ and $\Delta E = 0.85$ eV, Figure 2.2.5 and Table 2.2.2. Hence, it is concluded that interface recombination is not the dominant transport mechanism for $CdCl_2$-treated CdTe/CdS devices. If recombination through localized states within the CdTe depletion region is dominant, then a plot of $ln(J_{01}T^{-2.5})$ vs. 1000/T should yield an activation energy approximately equal to half of the CdTe bandgap. (17,19) Such a plot is shown in Figure 2.2.6, yielding a ΔE value of 0.79 eV, close to half of the CdTe bandgap. Hence it is likely that depletion region recombination dominates current transport in the $CdCl_2$-treated cells. Furthermore, the A_1 value of 1.75 suggests that the dominant path of recombination occurs through states displaced either above or below midgap ($A_1 = 2$ for a midgap recombination center). The presence and importance of these states will be discussed later. Note that below 220 K the J-V-T behavior exhibits temperature-independent lnJ-V slopes (given by α_1 and α_2 in Table 2.2.2 after correction for series resistance) and weakly temperature dependent diode prefactors (J_{01} and J_{02}),

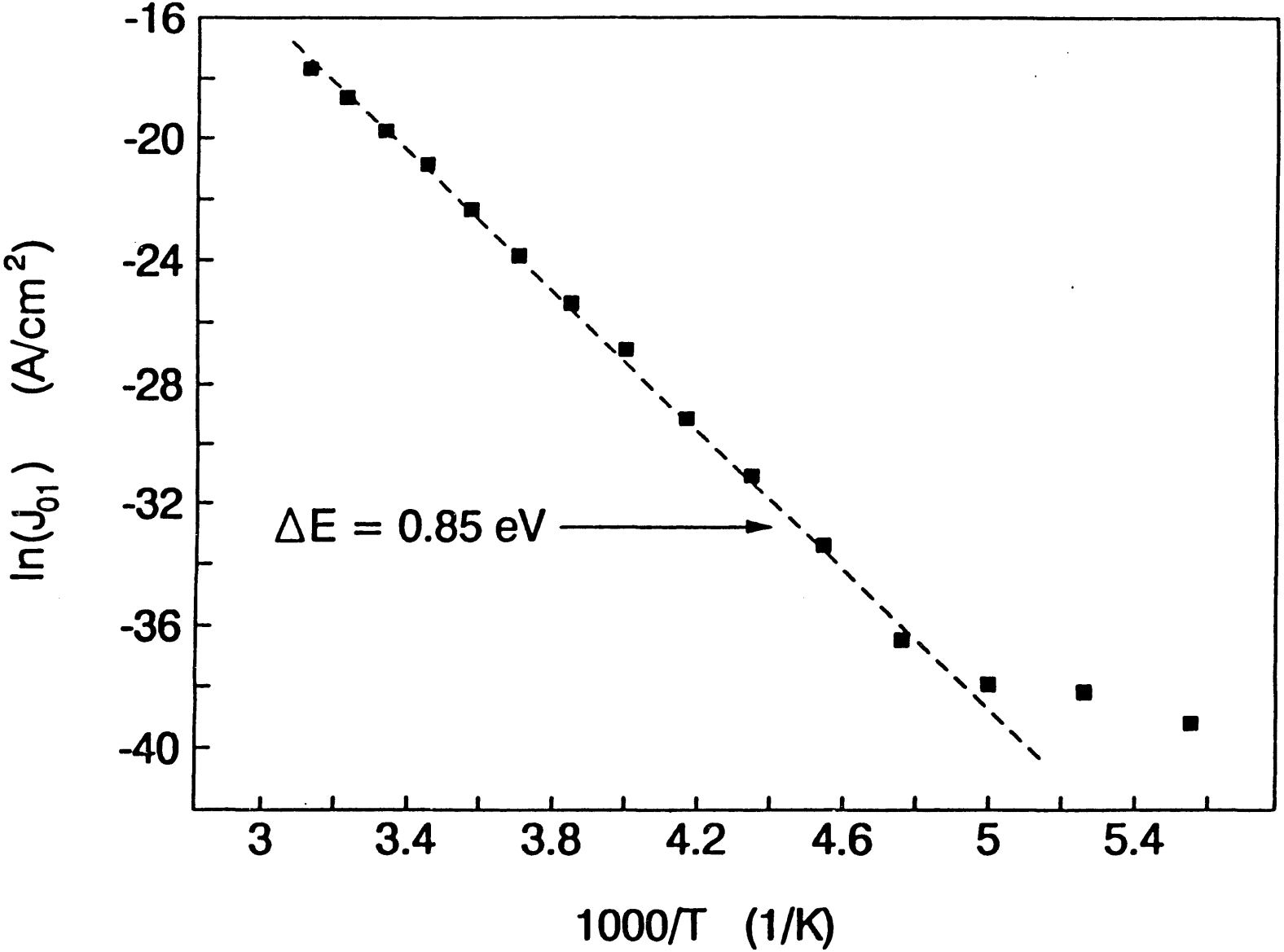


Figure 2.2.5 Plot of lnJ_{01} vs. 1000/T for CdTe/CdS cells have undergone $CdCl_2$ + air anneal.

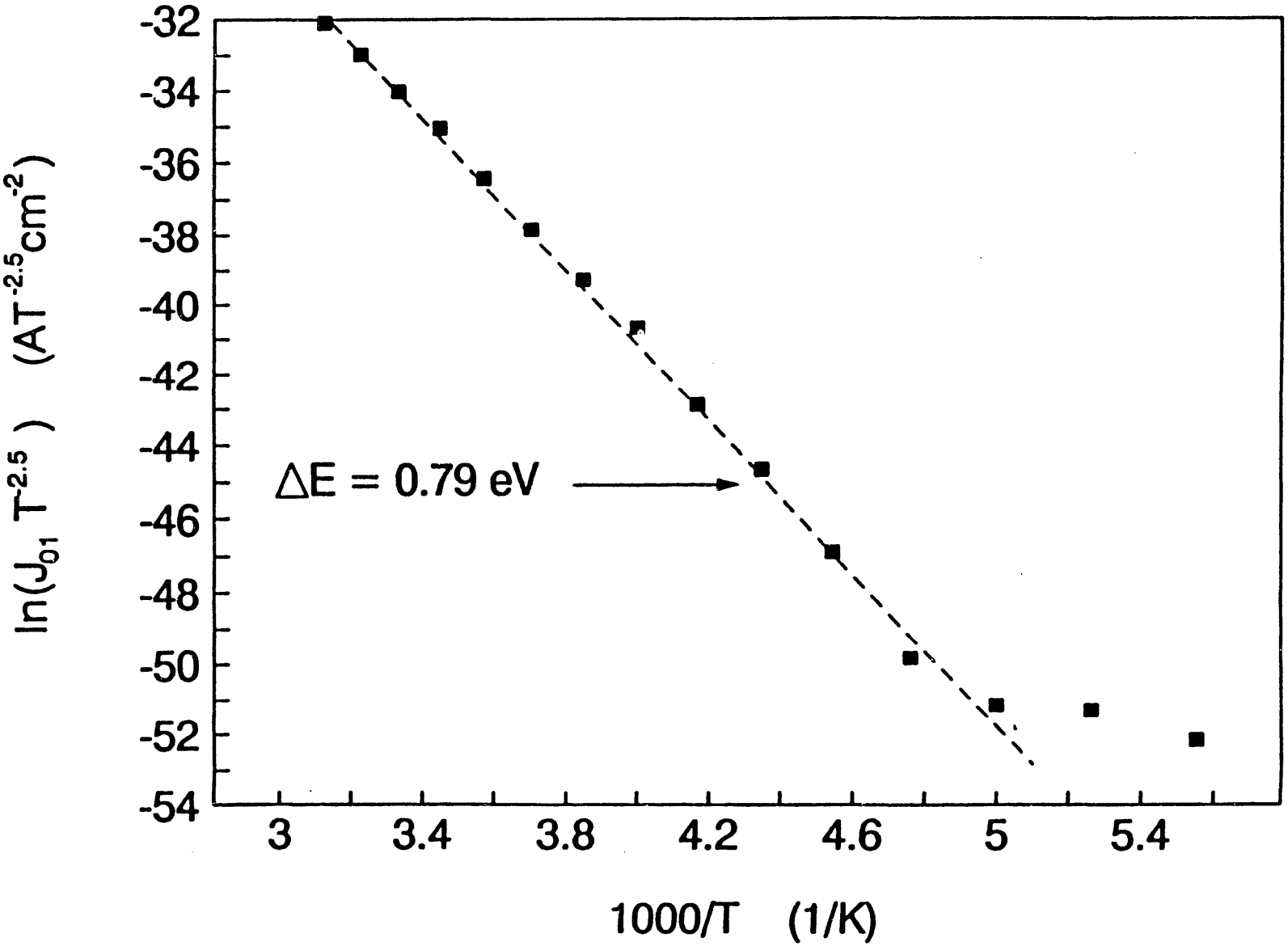


Figure 2.2.6 Plot of $\ln(J_{01}T^{25})$ vs. 1000/T for CdTe/CdS cells that have undergone $CdCl_2$ + air anneal.

as determined by further computer fitting. These transport characteristics suggest that a tunneling-type behavior is dominant at lower temperatures. Further analysis showed that the observed characteristics at low temperatures were well described by a multi-step tunneling model (20) which required ~ 40-50 tunneling steps through the CdTe depletion region to fit the experimental J-V-T behavior, similar to previously reported results for. (15) Note that two parallel diodes dictate the low temperature transport, as indicated in Table 2.2.2.

The dominant mode of dark current transport in cells processed without $CdCl_2$ was found to be significantly different than the $CdCl_2$-treated cells. Analysis of the J-V-T behavior (above 240 K) of the cells processed without the $CdCl_2$ treatment indicates thermally activated current transport, but with a much lower activation energy of 0.56 eV (Figure 2.2.7) compared to 0.85 eV for the $CdCl_2$-treated cell. This low value of ΔE (slope of $\ln J_{01}$ vs 1000/T) is responsible for the large diode current and J_{01} values observed for the cells processed without $CdCl_2$. Furthermore, the current transport behavior cannot be explained by depletion region recombination (in contrast to the $CdCl_2$-treated cell), interface recombination, or direct tunneling. This is evident from Table 2.2.3 which shows that the diode quality factor (A_1) is > 2 and is temperature-dependent (recall that A_1 = 1.75 and was independent of temperature for the $CdCl_2$-treated cell), eliminating the possibility of simple depletion region and interface recombination. In addition, the lnJ-V slope (α_1) is temperature-dependent and J_{01} is thermally-activated (Figure 2.2.6), which eliminates the possibility of direct tunneling as the dominant transport mechanism. Instead, current transport by thermally-assisted tunneling of holes from CdTe into interface

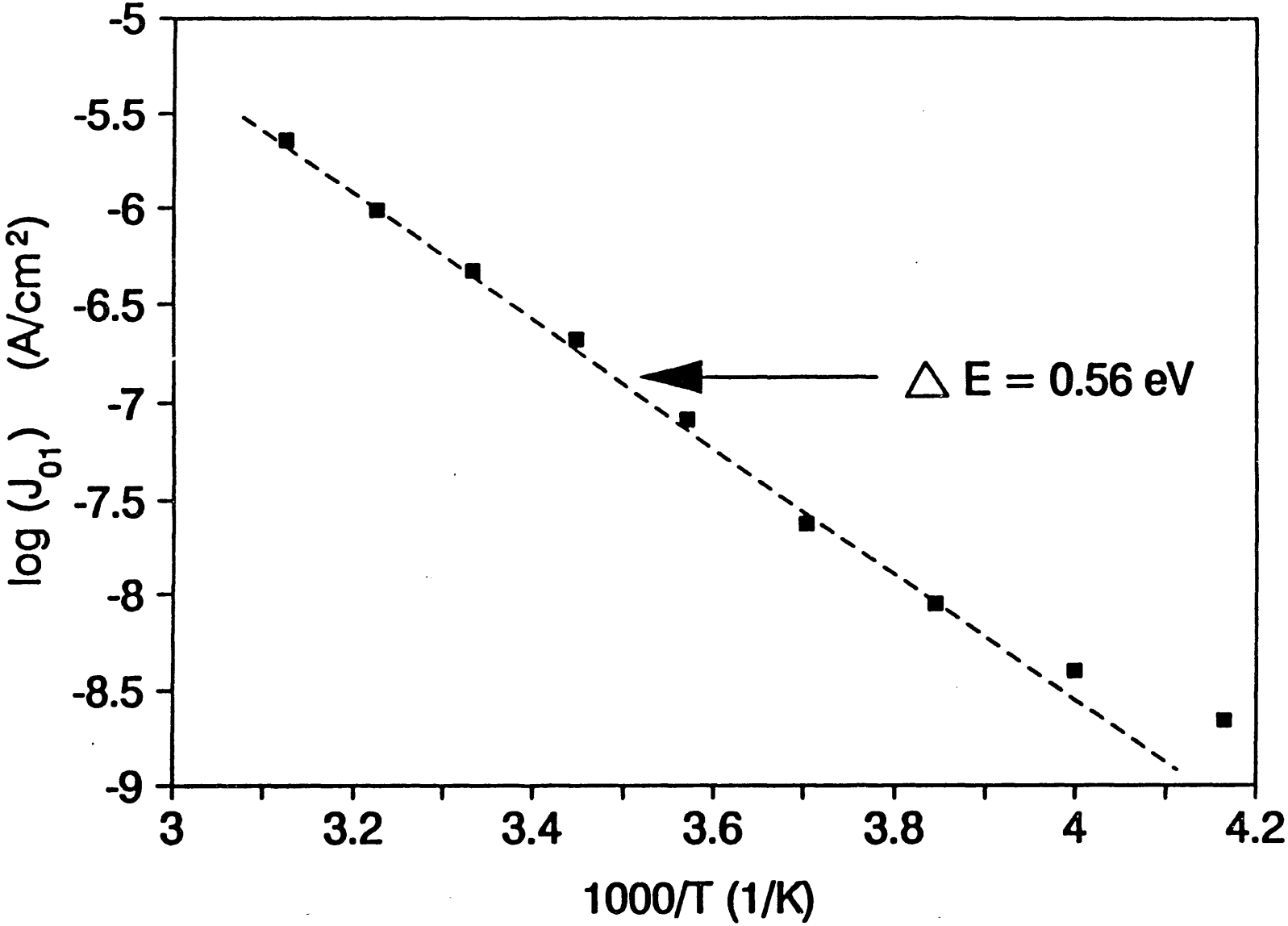


Figure 2.2.7 Plot of $\ln J_{01}$ vs. 1000/T for a CdTe/CdS cell annealed without $CdCl_2$.

states followed by interface recombination was found to adequately explain the observed J-V-T behavior of the CdTe/CdS heterojunctions processed without $CdCl_2$. The J-V-T behavior is well described by the tunneling/interface recombination (T/IR) model of Miller and Olsen (21) which approximates the thermally-assisted tunneling process by a series combination of direct tunneling and pure interface recombination. According to the T/IR model, (21)

$$J = J_{01}[exp[C(V - JR_s)] - 1] + (V - JR_s)/R_{sh} \quad (8)$$

$$J_{01} = J_{001}exp(-\Delta E/kT) \quad (9)$$

$$C = (1 - f)B + f/(\xi kT) \quad (10)$$

where ΔE is the thermal activation energy shown in Figure 2.2.7, B is a temperature-independent tunneling parameter, C is the slope of the lnJ-V curves, and ξ represents the voltage division between the CdTe and CdS. The value of the f parameter quantifies the degree of tunneling in the observed J-V behavior with f = 1 representing pure interface recombination and f = 0 representing direct tunneling. By plotting the experimentally determined values of C ($=q/A_1kT$ in Table 2.2.3) vs. 1000/T in Figure 2.2.8, the values of (1-f)B and f/ξ in eq. (10) were determined to be 10.3 V^{-1} and 0.266, respectively, indicating that the current transport in the cells processed without $CdCl_2$ is limited by both interface recombination and tunneling, consistent with the lower barrier height observed for these devices.

Clearly, current transport via thermally-assisted tunneling, as described by the T/IR

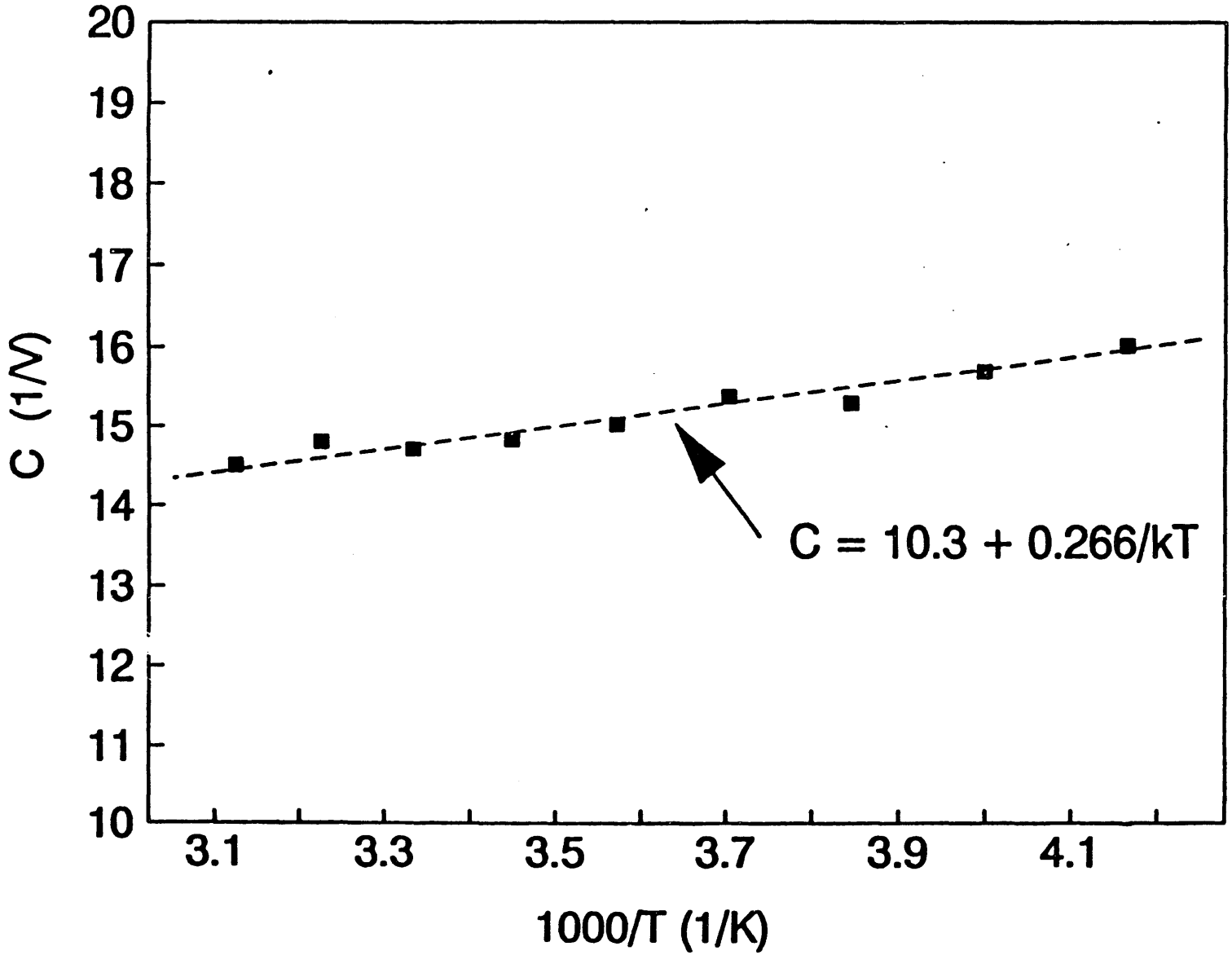


Figure 2.2.8 Plot of the T/IR model C-factor vs. 1000/T indicating both interface recombination and tunneling limited behavior.

model, significantly worsens cell performance of the CdTe/CdS devices in the absence of the $CdCl_2$ treatment. It is apparent that the $CdCl_2$-induced grain growth is necessary to decrease leakage current and increase V_{oc} via reduction of interface state density near the interface. However, even though the CdTe/CdS interface no longer controls the dark diode current transport after the $CdCl_2$ treatment, the bias dependence of the spectral response after $CdCl_2$ treatment (Figure 2.2.3) indicates that interface recombination may still limit the collection of photogenerated carriers. This suggests that the $CdCl_2$ treatment removes enough interface states to alter the diode transport mechanism and reduce the diode leakage current, but is less effective in removing interface states that limit the photocurrent collection across the CdTe/CdS (recall the bias dependent spectral response, Figure 2.2.3). To identify the origin and better understand the role of process-related defects, DLTS measurements were performed on CdTe/CdS cells processed with and without the $CdCl_2$ treatment and are discussed in the following section.

D. Effect of $CdCl_2$ and Heat Treatment on Defect Generation in CdTe/CdS Heterojunctions

Figure 2.2.9 shows a typical DLTS spectrum obtained for a CdTe/CdS device having undergone an air annealing step with $CdCl_2$ which revealed a hole trap peak at ~ 330 K. DLTS measurements were also performed on CdTe/CdS devices processed without $CdCl_2$, but it was not possible to obtain useful data because of the large series resistance in these samples which dominated the DLTS response. From the Arrhenius plot of $\log(T^2/e_{mp})$ vs. 1000/T, constructed using weighting functions from 4 msec. to 64 msec., the hole trap in the $CdCl_2$-treated device was found to be located at E_v + 0.64 eV

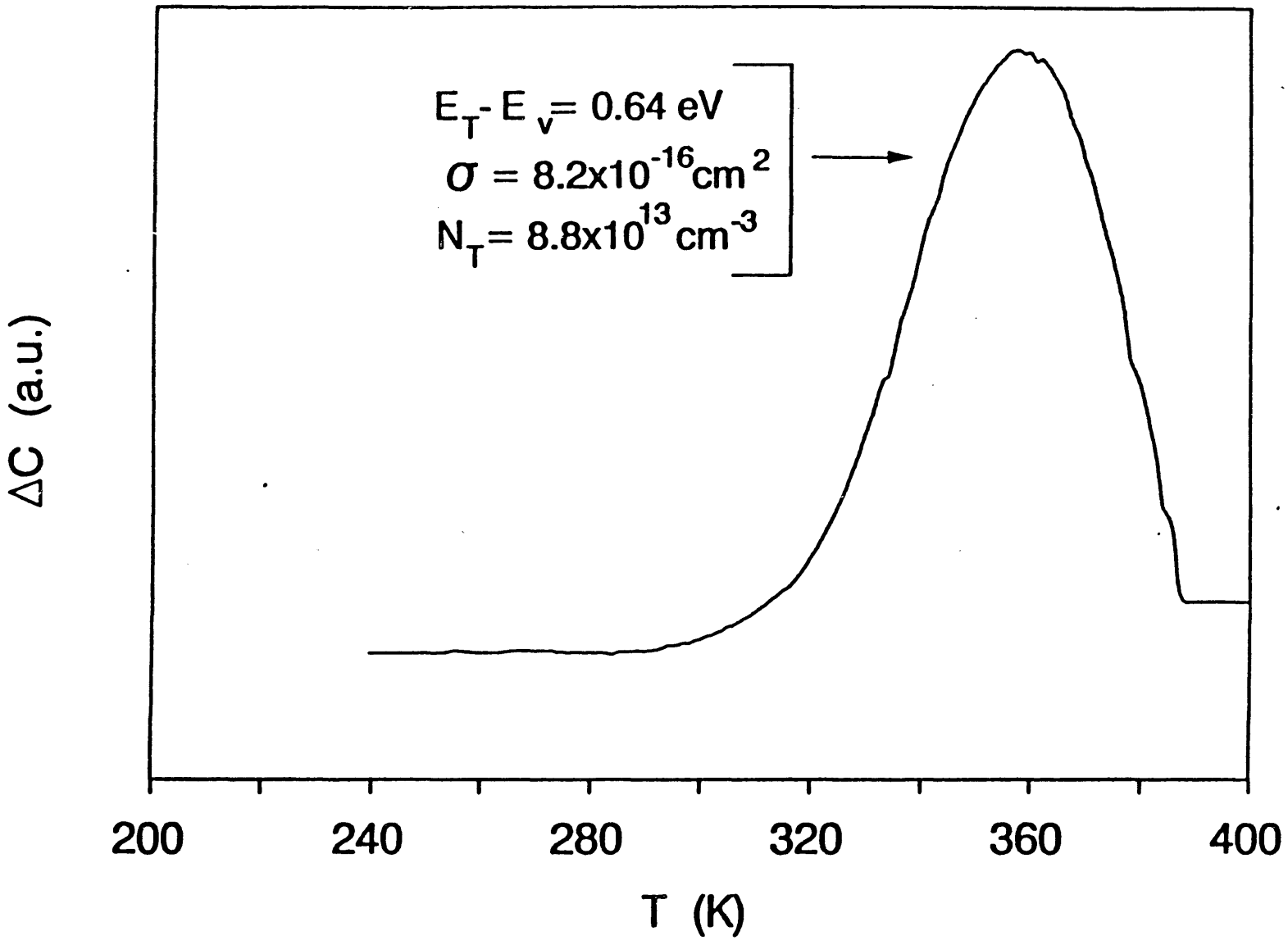


Figure 2.2.9 Typical DLTS spectrum of a CdTe/CdS cell having undergone an air anneal with $CdCl_2$ using a steady reverse bias of -400 mV and a pulse height of 300 mV, a pulse width of 8 msec. and a rectangular weighing function with a period of 4 msec.

(± 0.04 eV) with a cross-section of 8.2×10^{-16} cm^2 and a trap density of 8×10^{13} cm^{-3} (for the trap shown in Figure 2.2.9). This energy level agrees well with Cd vacancy-related defects such as doubly-ionized cadmium vacancies, $V_{Cd}^{=}$, or singly-ionized cadmium vacancy-halogen complexes such as $(V_{Cd}Cl)^{-}$, both of which have been reported to contribute acceptor-like traps in the range 0.54 to 0.9 eV above the valence band edge in CdTe after heat treatments. (22-28) Since halogen ions are known to readily form complexes with cadmium vacancies to give deep and shallow levels, it is likely that the E_v + 0.64 eV trap results from $(V_{Cd}Cl)^{-}$ defects. (27,28) However, further measurements are necessary to determine the exact configuration of the defect responsible for this trap. The presence of acceptor-like traps within the CdTe depletion region was found to adversely affect the CdTe/CdS solar cell characteristics. Figure 2.2.10 shows the direct consequences of the density of this defect on the measured V_{oc} and J_{sc} of different CdTe/CdS cells that have undergone the $CdCl_2$ dip followed by heat treatment. It is clear from this figure that the V_{oc} is inversely proportional to the detected trap density while there is no apparent correlation between J_{sc} and the trap density. Presently, it is not clear why the trap density shows a random spatial variation on a given sample with different cells and also from sample to sample since no intentional attempt was made to introduce a variation. It has recently been suggested that such variations can result from non-uniform drying of the $CdCl_2$-methanol solution on the CdTe surface prior to heat treatment. (29) To determine the variation in trap density as a function of depth, DLTS was performed in a multi-bias mode. A decrease in trap concentration from ~ 8×10^{13} cm^{-3} to ~ 3×10^{13} cm^{-3} was found as the CdTe/CdS interface is approached by decreasing

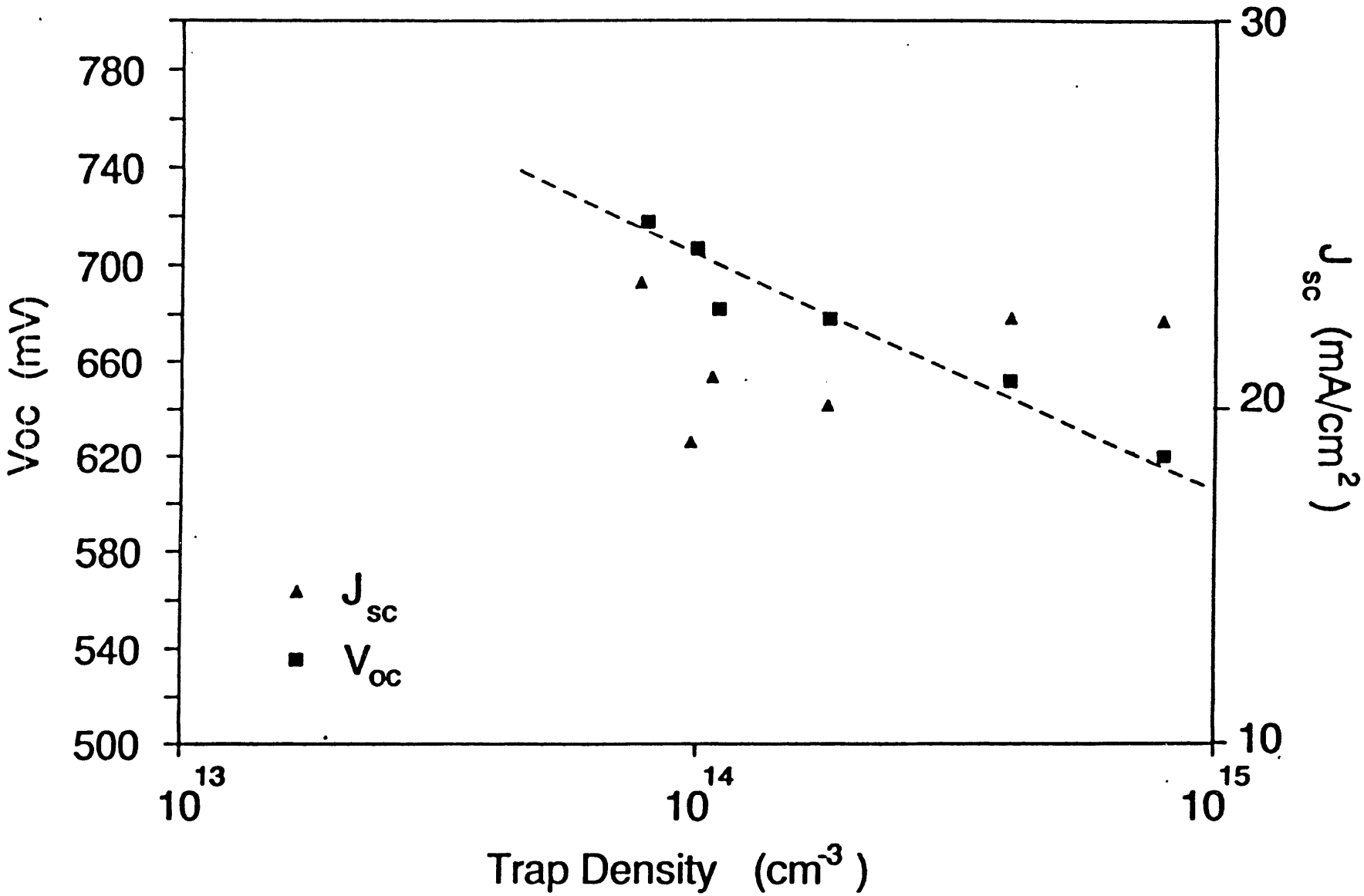


Figure 2.2.10 Measured cell V_{oc} and J_{sc} as a function of ($V_{Cd}Cl$) defect concentration for different CdTe/CdS solar cells that have undergone a 400 C air anneal with $CdCl_2$ as determined by DLTS measurements.

the depletion width. This is consistent with V_{Cd} and/or Cl diffusion from the CdTe surface into the bulk as a result of the 400 C anneal. From Figure 2.2.10, it is evident that the variations in V_{oc} must result from the diode leakage current, which was found to increase with increasing trap density, since J_{sc} showed no such dependence. Recalling that diode current transport in the devices processed with $CdCl_2$ is dictated by recombination via deep states within the CdTe depletion region which is characterized by an A-factor of 1.75, the off-center position of the trap at E_v + 0.64 eV suggests that this level may be responsible for the diode transport mechanism (note that an A-factor of 2 represents a midgap or E_v + 0.75 eV trap in CdTe (17)) which in turn dictates V_{oc}. Hence, the $CdCl_2$ dip and heat treatment greatly improves the cell performance via grain growth, interface state density reduction, and transport mechanism modification, but this process also appears to limit V_{oc} by cadmium vacancy-related defect formation. Further increases in V_{oc} and efficiency can be expected if the generation of this defect can be reduced or eliminated. This may require further modification or optimization of the current cell processing schemes.

2.2.4. Conclusions

In this section, the beneficial and adverse effects of the standard $CdCl_2$ dip followed by a post-deposition heat treatment on the material and device properties of MBE-grown polycrystalline CdTe/CdS solar cell structures were investigated and quantified. As expected, the $CdCl_2$ treatment induced CdTe grain growth and significantly improved cell efficiency from 1.3% to 8.6%. SPV and spectral response measurements

showed that the improvement in J_{sc} after $CdCl_2$ treatment was partly due to enhanced carrier collection resulting from increased carrier collection length and improved CdTe/CdS interface quality. However, even after the $CdCl_2$ treatment, the photocurrent demonstrated significant bias dependence, suggesting that J_{sc} was still limited by interface recombination, although to a lesser extent compared to cells processed without $CdCl_2$. Analysis of the dark J-V-T characteristics showed that in contrast to the photocurrent, the dark diode I-V characteristics showed a clear change in dominant transport mechanism, changing from an interface recombination/tunneling process to depletion region recombination after $CdCl_2$ treatment. The change in transport mechanism resulted in an increase in barrier height and reduced leakage current. DLTS measurements showed that depletion region recombination probably occurs through a large density of deep states at E_v + 0.64 eV which result from the formation of Cd-vacancy related defects during the $CdCl_2$ dip and heat treatment process that are tentatively attributed to a $(V_{Cd}Cl)^-$ defect complex resulting from the interaction between cadmium vacancies introduced by the heat treatment and chlorine from the $CdCl_2$. The cell V_{oc} was found to be inversely related to the density of this trap. Hence, even though the $CdCl_2$ treatment is very important for improving CdTe/CdS cell performance, it appears to introduce a V_{oc} and efficiency-limiting defect whose role must be studied in more detail or whose presence must be removed to achieve CdTe/CdS cell efficiencies beyond 12-13%.

2.3 Growth and Process Optimization of CdZnTe Polycrystalline Films for High Efficiency Solar Cells

2.3.1 Introduction

Thin film polycrystalline cell efficiencies higher than 20% can be achieved using a two cell tandem design. The optimum bandgaps for the top and bottom cells are 1.7 eV and 1 eV, respectively (1). Considerable progress has been made in the area of the bottom cell, with small area $CuInSe_2$ cell efficiencies in excess of 14% recently been reported recently (2). However, a compatible wide bandgap (1.7 eV) material for the top cell has not yet been developed. CdTe and CdZnTe alloys are considered for top cell applications. CdTe is a promising polycrystalline wide bandgap material that has given small area single cell efficiencies in excess of 12% (3). However, the CdTe bandgap is 1.45 eV instead of 1.7 eV which is optimum for the top cell. Thus, there are two approaches for realizing the goal of 20% efficient polycrystalline cells with a tandem structure. The first approach involves improving CdTe cell efficiencies in excess of 15% and augmenting that with a small amount of power from the bottom cell. The second approach involves developing a 1.7 eV bandgap CdZnTe top cell with efficiency of ~10% so that to take greater advantage of the bottom cell efficiency due to higher subgap transmission. This section describes the investigation of growth and process optimization of CdZnTe cells in order to understand the efficiency limiting defects and mechanisms. Future directions are suggested to improve their efficiencies to a point where they can be a potential candidate for ~ 20% tandem cells.

2.3.2 Experimental

A. Film growth

MBE $Cd_{1-x}Zn_xTe$ (x = 0.35, will be referred as CdZnTe) films were grown using a Varian Gen II MBE system and elemental sources were used for all constituents having a purity of at least 5N. The substrates were baked out at 250° C for 3-4 hours before film growth. The substrate temperature was kept at 275° C for 30 minutes to initiate film growth and increased to 300° C for the remainder of the run (4).

B. Cell Fabrication

P-i-n front-wall solar cells were fabricated at AMETEK applied materials laboratory. After a dip in a saturated $CdCl_2$:CH_3OH solution, the CdTe/CdS structures were annealed at 400° C for 30 minutes in air. Annealed films were etched in bromine-methanol solution for 5 sec followed by an evaporation of 1000 Å of Cu-doped p^+ZnTe film. Small area (8 mm^2) Ni contacts were evaporated to form an ohmic contact (5).

C. Material and device characterization

Electrochemical surface photovoltage (SPV) measurement, Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), and transmission measurements were used for optical, physical and chemical characterization of the films. J-V-T, frequency dependent C-V, and bias dependent spectral response measurements were used to characterize device properties.

2.3.3 Results and Discussion

Polycrystalline CdZnTe films with a 1.7 eV bandgap were successfully deposited by MBE on CdS/SnO_2/glass substrates (4). However, CdZnTe solar cells fabricated by the identical process sequence used successfully for high efficiency CdTe cells gave efficiencies of only ~ 4.4%. In addition, the CdZnTe bandgap shifted from 1.7 eV to 1.55 eV and the series resistance (~ 2-6 ohm-cm^2) was 3-5 times higher than in the counterpart CdTe solar cells. Detailed investigations were conducted to understand and remove the source of these problems.

In order to find and eliminate the source of high resistance, depth-resolved AES and ESCA measurements were performed near the CdZnTe surface after annealing (400° C, 30 min. in air without the $CdCl_2$ treatment) and subsequent chemical etching to investigate process-induced changes in the CdZnTe surface which can prevent the formation of good ohmic contacts (6). ESCA analysis and AES profiles in Figure 2.3.1 show that without any post-anneal chemical etch, a significant amount of Cd-O, Te-O and Zn-O are present at and below the CdZnTe surface. After an etch in Br_2:CH_3OH, which was used in the standard cell fabrication prior to ZnTe/Ni back contact deposition, both Cd and Te oxides were removed from the surface but the Zn-O remained at and below the surface, responsible in part for the high series resistance. In addition, the CdZnTe surface is not as Te-rich (Te/(Cd+Zn)~ 1.2) compared to the counterpart CdTe surface where Te/Cd ratio is ~ 1.5-2. It has been suggested that a Te-rich surface can facilitate the ohmic contact formation on p-type CdTe (7).

In an attempt to remove the Zn-O and make the CdZnTe surface Te rich, various

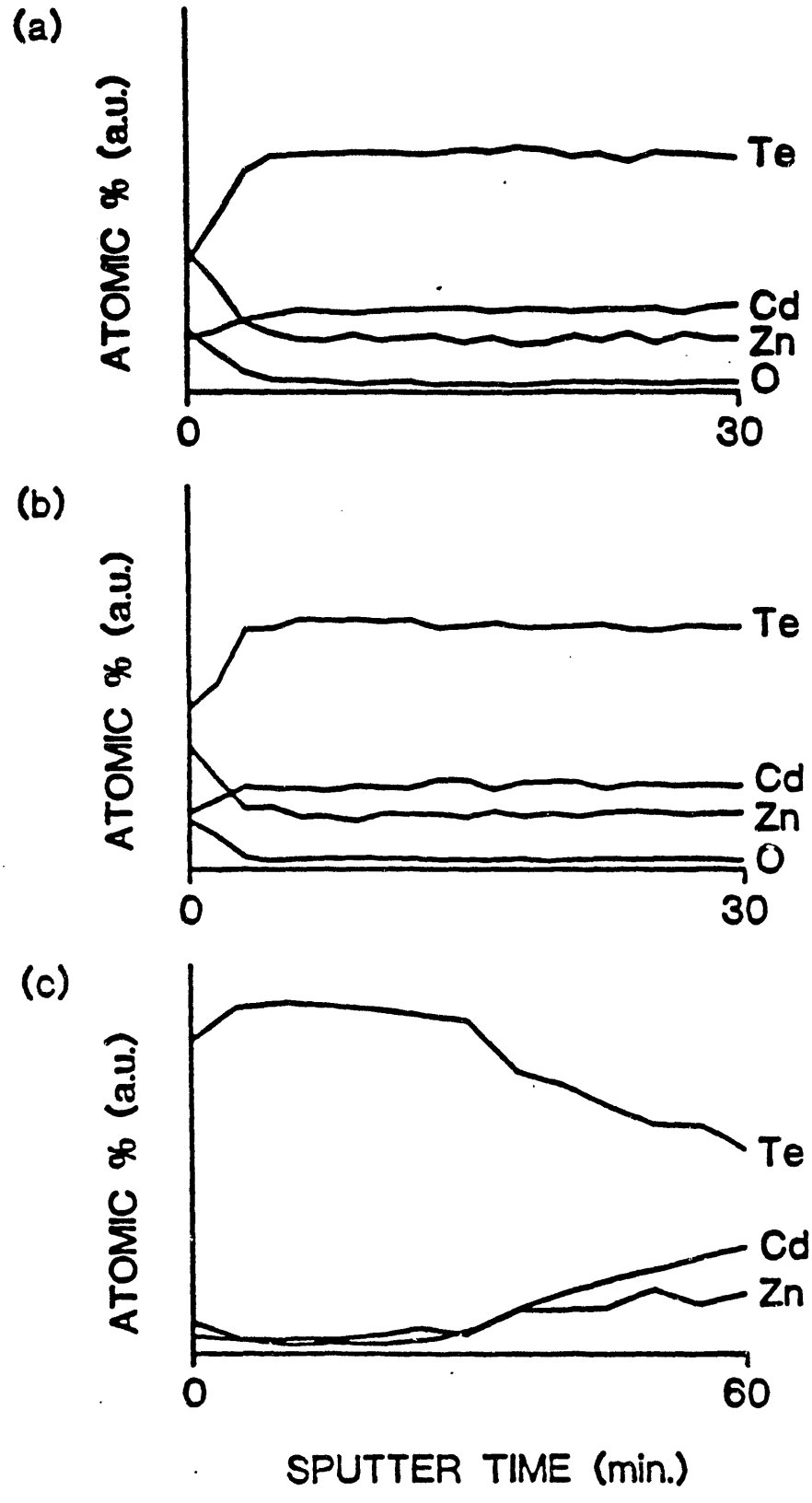


Figure 2.3.1 Auger depth profiles of air annealed CdZnTe films after (a) no post-anneal etch, (b) Br_2CH_3OH etch, and (c) saturated dichromate etch.

chemical enchants were investigated. Figure 2.3.1 shows that a post-anneal saturated dichromate ($K_2Cr_2O_7$:H_2SO_4) etch removed the near surface region that contained Zn-O and yielded a ~ 0.15 um Te-rich surface layer with little or no detectable trace of Cd, Zn, or oxygen. C-V measurements made on the dichromate-etched surface confirmed a much higher carrier concentration of ~ $2x10^{17}$ cm^{-3} in the Te-rich surface layer which gradually dropped down to the bulk doping concentration of ~ $5x10^{15}$ cm^{-3} over a distance of 0.15 um (6). This should eliminate the contribution from high contact resistance to the measured high series resistance.

The next step was to investigate the process-induced bandgap shift observed in processed CdZnTe films. AES depth profiles shown in Figure 2.3.2 and the SPV spectra in Figure 2.3.3 after the standard air anneal, with and without the $CdCl_2$ treatment, clearly demonstrate that it is not the air anneal itself, but the $CdCl_2$ treatment coupled with the air anneal that is responsible for the bandgap shift. Note that the cells were fabricated with the $CdCl_2$ treatment. The Auger profiles show that after the $CdCl_2$ treatment, out-diffusion of Zn from the bulk toward the surface occurs which reduces the bulk Zn content and decreases the bandgap, as demonstrated by the shift in the cut-off edge toward the longer wavelength in the SPV spectra of Figure 2.3.3. A proposed model for the phenomenon stems from the fact that thermodynamically, the formation of $ZnCl_2$ is preferred over $CdCl_2$. (8) Therefore, introducing $CdCl_2$ onto the surface and into the CdZnTe bulk triggers the formation of $ZnCl_2$ which has a much higher vapor pressure and lower melting point (318 C (8)) than $CdCl_2$, resulting in the outdiffusion of Zn. This process, where Cd from the $CdCl_2$ substitutes for lattice Zn, resulting in $ZnCl_2$ formation

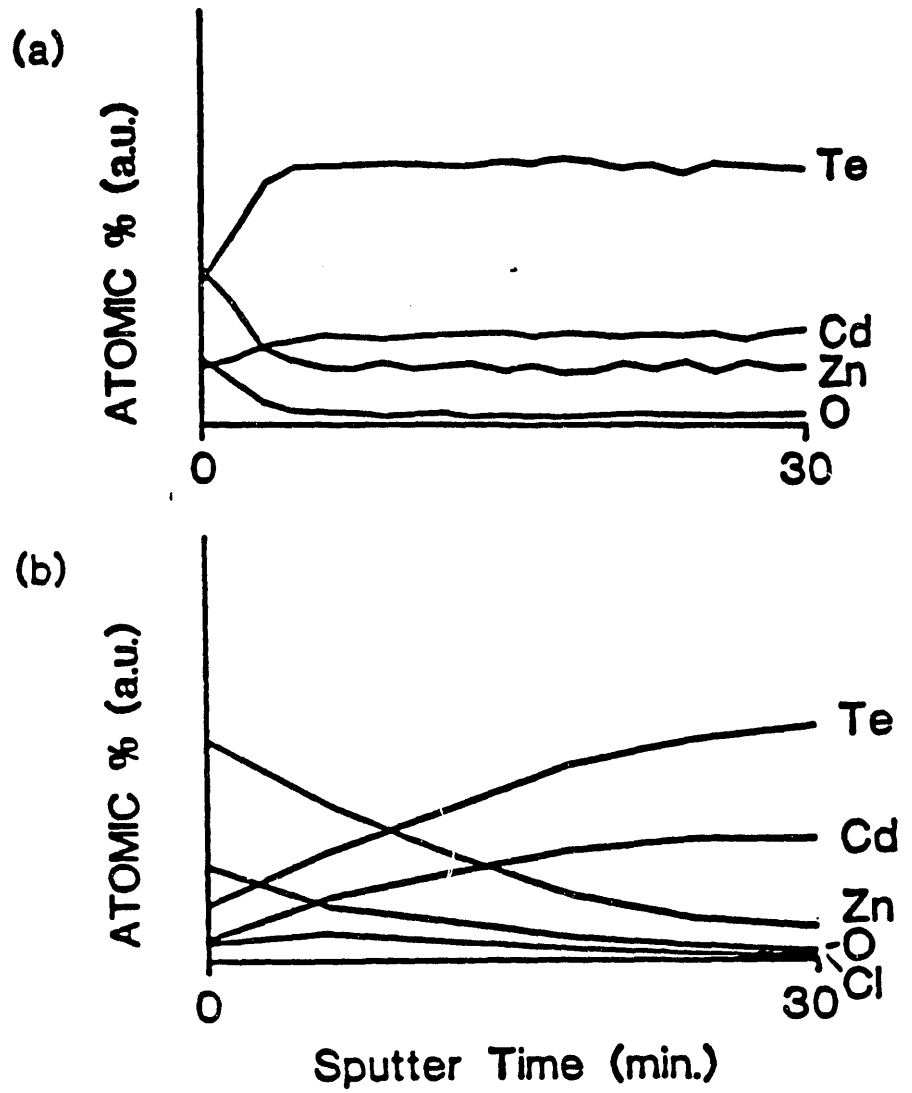


Figure 2.3.2 Auger depth profiles of air annealed CdZnTe films (a) without $CdCl_2$ treatment and (b) with $CdCl_2$ treatment.

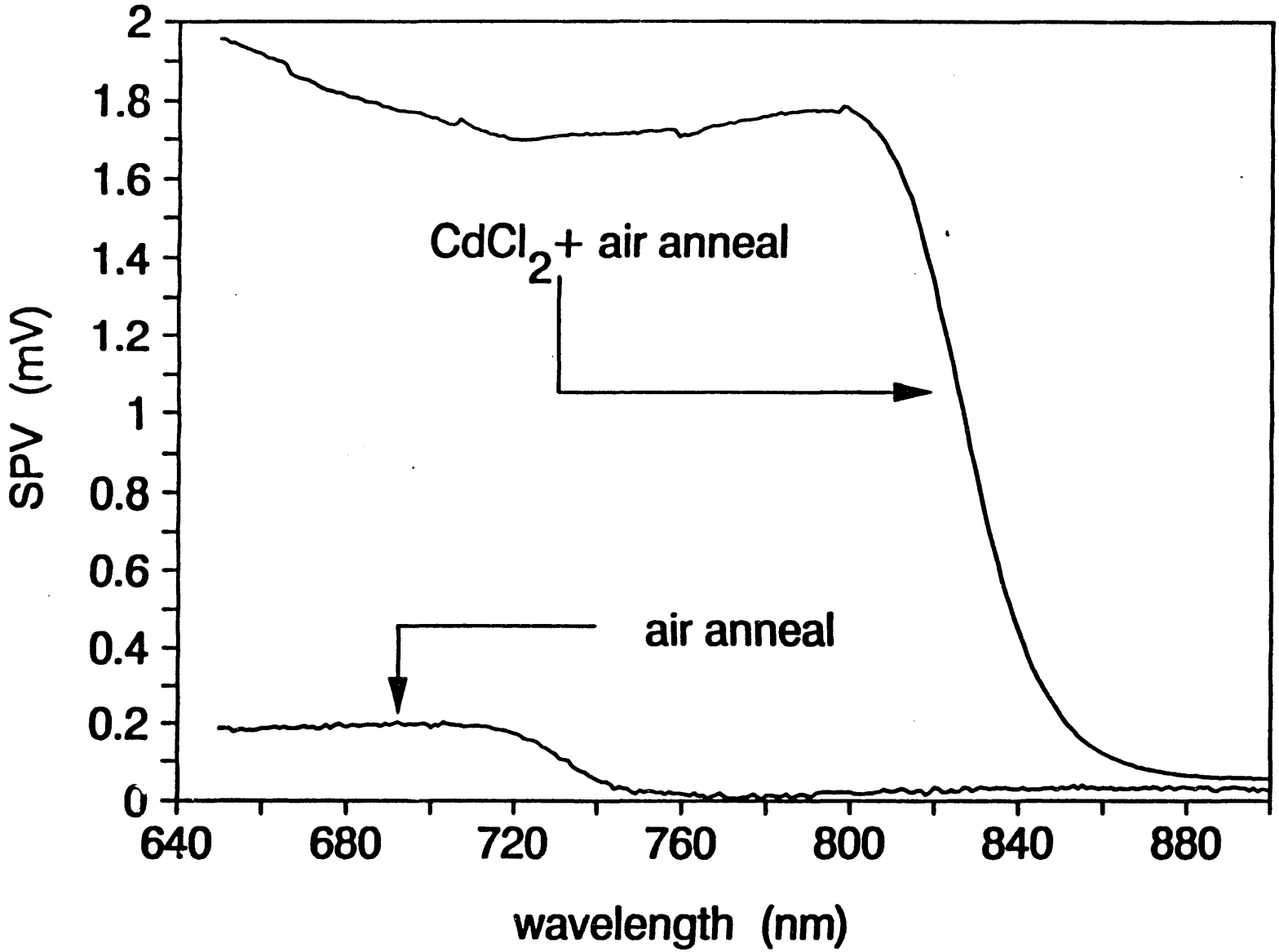


Figure 2.3.3 Electrochemical surface photovoltage spectra of air-annealed CdZnTe/CdS structures with and without the $CdCl_2$ treatment.

can be described by the following equation:

$$Cd_{1-x}Zn_xTe + yCdCl_2 \rightarrow Cd_{1-x+y}Zn_{x-y}Te + yZnCl_2$$

Note that if y > x, all of the Zn will be consumed and CdZnTe will reduce to CdTe.

Surface photovoltage data (Figure 2.3.3) taken on the CdZnTe/CdS structures show that if the $CdCl_2$ treatment is bypassed to preserve the bandgap, a very weak photoresponse is observed, resulting in only 1-2% efficient cells. However, the SPV data clearly show that incorporation of $CdCl_2$ during the processing of CdZnTe cells resulted in much higher photovoltages but the cutoff edge (or bandgap) shifted from 1.7 eV to 1.55 eV. The $CdCl_2$ treatment was also found to reduce the series resistance of the CdZnTe/CdS cells by a factor of ~ 10.

In order to investigate both the need and beneficial effects of the $CdCl_2$ treatment on CdTe-based polycrystalline solar cells, experiments were first conducted on p-i-n CdTe solar cells fabricated with and without the $CdCl_2$ treatment to eliminate the complication due to the presence of Zn. We have shown elsewhere (9) that the $CdCl_2$ treatment is essential for high efficiency MBE-grown CdTe cells because it promotes CdTe grain growth from ~ 0.1 um to ~ 1 um, resulting in an increase in V_{oc} from 385 to 720 mV, J_{sc} from 10.5 to 23.1 mA/cm^2, fill factor from 0.32 to 0.51 and cell efficiency from 1.3% to 8.6%. Other investigators have observed similar improvements due to the $CdCl_2$ treatment (10). In addition to quantifying the improvements in cell parameters, attempts were made to understand the effects of the $CdCl_2$ treatment on bulk properties, interface

quality and carrier transport mechanisms. The CdTe/CdS SPV response in Figure 2.3.4 showed a significant increase over the entire long wavelength range of 700-880 nm for cells annealed with $CdCl_2$ compared to cells annealed without $CdCl_2$. Since in our SPV measurements light is incident on the back side (not the sun side) of the CdTe cell structure, the long wavelength photons near the CdTe cutoff (~ 840 nm) are absorbed in the CdTe region near the CdTe/CdS interface. Hence, the significant increase in SPV response clearly supports an improved interface quality due to $CdCl_2$-induced grain growth. This is not surprising since grain growth reduces the number of grain boundaries intersecting the interface which should result in reduced interface state density. Spectral response measurements shown in Figure 2.3.5 also revealed a significant increase in bulk and interface quality due to the $CdCl_2$ treatment. The spectral response of a p-i-n device is generally dominated by interface recombination since the bulk is essentially depleted. Figure 2.3.5 shows that even after the $CdCl_2$ treatment, the spectral response showed an appreciable bias dependence with much higher response at 0.5 volts applied reverse bias. This is indicative of the fact that even though the $CdCl_2$ treatment significantly improves the interface quality, it does not completely eliminate those interface states which can increase the interface recombination velocity and reduce V_{oc} and fill factor.

Temperature dependent dark J-V measurements were performed to identify and quantify changes in the fundamental current transport properties due to the improved interface quality. CdTe/CdS cells, with and without $CdCl_2$ treatment, were analyzed by fitting the J-V-T data to equations governing various transport mechanisms such as direct and multi-step tunneling (11), thermally-assisted tunneling (12,13), depletion region

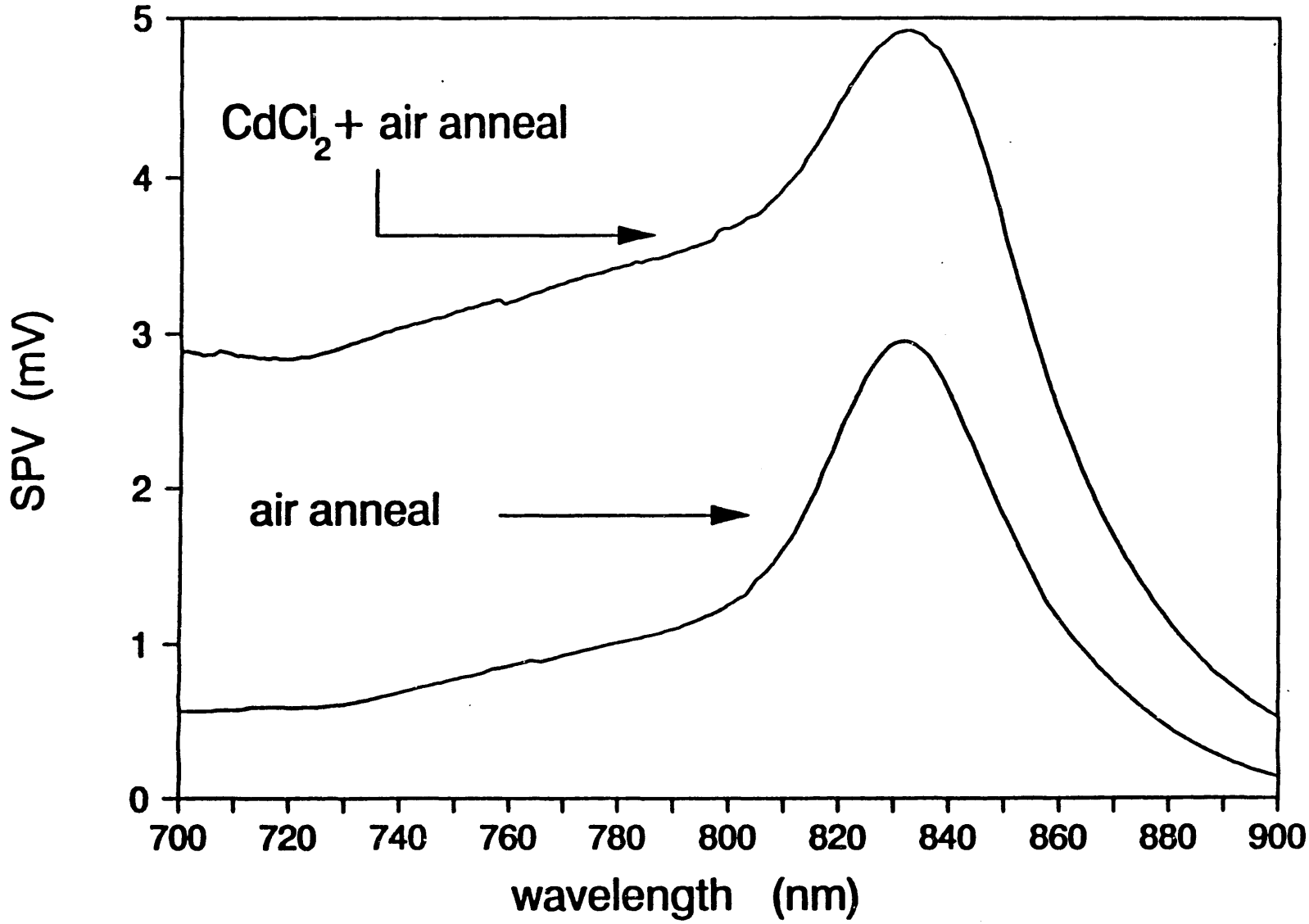


Figure 2.3.4 **Electrochemical surface photovoltage spectra of air-annealed CdTe/CdS structures with and without the $CdCl_2$ treatment.**

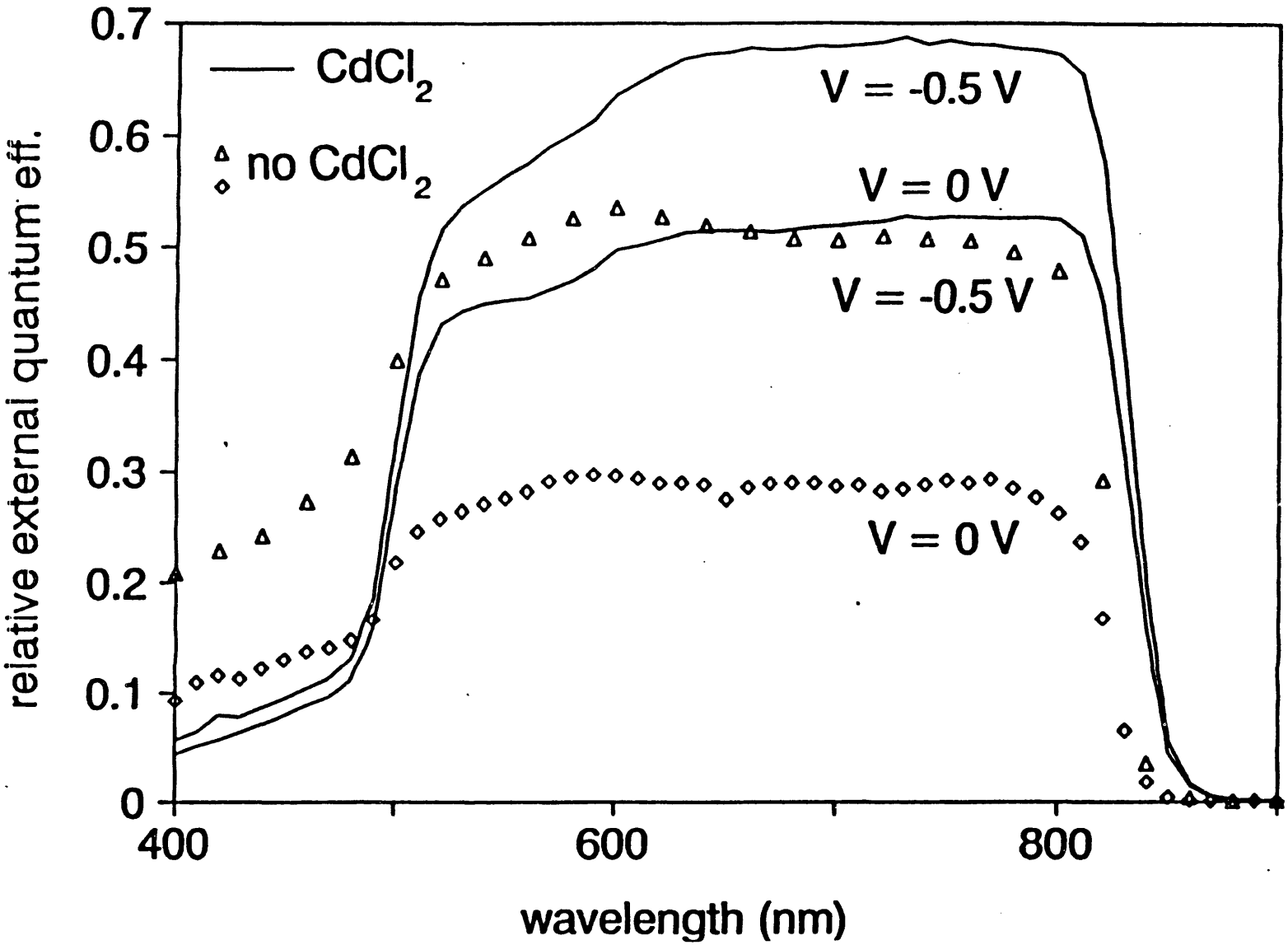


Figure 2.3.5 **Bias-dependent spectral response of completed Ni/ZnTe/CdTe/CdS/SnO_2/glass solar cells with $CdCl_2$ (solid lines) and without $CdCl_2$ (symbols). The applied reverse bias values are noted.**

recombination (14), interface recombination (15), etc.. It was determined that without the $CdCl_2$ treatment, current transport is dominated by thermally-assisted tunneling of holes from the CdTe into interface states followed by interface recombination, characterized by an activation energy of 0.56 eV and $J_o = 4.7x10^{-7}$ A/cm^2. For cells treated with $CdCl_2$, the dominant mode of current transport was found to shift from a tunneling/interface recombination mechanism to recombination via traps within the CdTe depletion region, indicating substantial reduction in interface state density. This change is manifested in an increase in the activation energy for current transport from 0.56 eV to 0.85 eV which results a significantly lower J_o value of $2.6x10^{-9}$ A/cm^2, accounting for the observed increase in V_{oc} from 385 mV to 720 mV.

Having established quantitatively the beneficial effects of the $CdCl_2$ treatment on CdTe material and device properties, in addition to the detrimental (bandgap shift) effects on CdZnTe, it became evident that a sintering aid other than straight $CdCl_2$ is essential for obtaining efficient CdZnTe solar cells. However, some combination involving $CdCl_2$ may be a good choice since the $CdCl_2$ treatment results in partial grain growth (determined from SEM measurements) and significantly lower series resistance (due to lower CdZnTe sheet resistance) yielding a much higher photoresponse (Figure 2.3.3). Since the bandgap shift appears to result from the substitution of Cd for Zn, attempts were made to control the bandgap shift and induce grain growth by dipping the CdZnTe films in various solutions of $CdCl_2$+$ZnCl_2$ in methanol prior to air annealing at different temperatures. Only limited success was obtained using this method since the $ZnCl_2$ readily evaporates into the anneal ambient at temperatures greater than 320° C, leaving

$CdCl_2$ alone which results in partial bandgap shift. For lower anneal temperatures (< 320° C), negligible bandgap shift occurs but this is accompanied by little or no grain growth and poor photoresponse. Attempts are underway to anneal $CdCl_2$ treated CdZnTe surfaces in a $ZnCl_2$ overpressure ambient using a closed system to prevent the outdiffusion of Zn and induce grain growth. In this system, $ZnCl_2$ is heated in a separate boat next to the CdZnTe sample. Thus, development of a sintering aid that can promote CdZnTe grain growth without the bandgap shift remains the major obstacle for the success of wide bandgap CdZnTe cells for tandem cell applications.

2.3.4 Conclusions

The CdTe process sequence cannot be used to fabricate efficient CdZnTe cells because it results in high resistance and a bandgap shift from the desired value of 1.7 eV to 1.55 eV. The contribution to the high series resistance from non-ohmic back contact was solved by using a saturated dichromate instead of the $Br:CH_3OH$ post-anneal etch, which resulted in a p-type surface doping concentration of $2x10^{17}$ cm^{-3}. It is shown that $CdCl_2$ is essential for high efficiency CdTe solar cells because it promotes grain growth which improves bulk collection, reduces interface state density, and eliminates the tunneling of carriers through the interface to improve V_{oc}, J_{sc} and efficiency. However, the use of a $CdCl_2$ dip prior to air anneal was established to be the main source of the observed bandgap shift in CdZnTe due to $ZnCl_2$ formation by substitution of Cd for lattice Zn. This also resulted in incomplete grain growth in CdZnTe since much of the $CdCl_2$ was consumed by this process. Development of an alternative sintering aid, which

induces grain growth but prevents the bandgap shift, is the key to the success of widegap polycrystalline CdZnTe solar cells for tandem cell applications.

3. SUMMARY

MOCVD grown polycrystalline CdTe solar cells with efficiencies of ~10% were achieved using both p-i-n and p-n structures. Pre-heat treatment of CdS/SnO_2/glass substrates at 450° C in Hydrogen atmosphere prior to CdTe growth by MOCVD was found to be essential for high performance since this heat treatment reduces the oxygen related defects from the CdS surface. However, this heat treatment also resulted in a Cd-deficient CdS surface which may, in part, limit the CdTe cell efficiency to 10% due to Cd vacancy related interface defects. Preliminary model calculations suggest that the removal of these states can increase the cell efficiency from 10% to 13.5%. Photon absorption in the CdS film also limits the cell performance and elimination of this loss mechanism can result in CdTe efficiencies in excess of 18%.

Significant improvements in CdTe/CdS solar cell efficiency are commonly observed as a result of a post-deposition $CdCl_2$ dip followed by a 400° C heat treatment during cell processing which increases CdTe grain size. I-V-T analysis in this research revealed that $CdCl_2$ treatment changes the dominant current transport mechanism from interface recombination/tunneling to depletion region recombination, suggesting a decrease in the density and dominance of interface states due to the $CdCl_2$ treatment. It is shown that the change in transport mechanism is associated with (a) an increase in heterojunction barrier height from 0.56 eV to 0.85 eV, (b) a decrease in dark leakage current from 4.7×10^{-7} A/cm^2 to 2.6×10^{-9} A/cm^2, and (c) an increase in cell V_{oc} from 385 mV to 720 mV. The $CdCl_2$ treatment also improved the optical response of the cell. Substantial increase in the surface photovoltage and quantum efficiency accompanied by a decrease in the bias

dependence of the spectral response in the $CdCl_2$-treated structures indicate that the $CdCl_2$-treated structures indicate that the $CdCl_2$ treatment improves carrier collection from the bulk as well as across the heterointerface. However, DLTS measurements detected a hole trap within the CdTe depletion region of the $CdCl_2$-treated devices at E_v + 0.64 eV which is attributed to the formation of V_{Cd}-related defects as a result of the $CdCl_2$ + anneal process. I-V-T analysis demonstrated that this trap is the probable source of dominant recombination in the $CdCl_2$-treated cells. An inverse correlation was found between the density of the E_v + 0.64 eV trap and cell V_{oc} suggesting that the $CdCl_2$ treatment may eventually limit the CdTe/CdS cell performance unless the formation of this defect complex is controlled or eliminated.

In addition to the CdTe cells, polycrystalline 1.7 eV CdZnTe films were grown by MBE for tandem cell application. CdZnTe/CdS cells processed using the standard CdTe cell fabrication procedure resulted in 4.4% efficiency, high series resistance, and a bandgap shift to 1.55 eV. Formation of Zn-O at and near the CdZnTe surface is found to be the source of high contact resistance. A saturated dichromate etch instead of Br_2:CH_3OH etch prior to contact deposition has been found to solve the contact resistance problem. The $CdCl_2$ treatment has been identified to be the cause of the observed bandgap shift due to the preferred formation of $ZnCl_2$. A model for the bandgap shift along with a possible solution using an overpressure of $ZnCl_2$ in the annealing ambient has been proposed. Development of a sintering aid which promotes grain growth and preserves the optimum 1.7 eV bandgap is shown to be the key to successful wide bandgap CdZnTe cells.

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6. LIST OF PUBLICATIONS AND PRESENTATIONS

The following is a list of publications and technical presentations since the beginning of this project in 1987.

Journal Papers

1. A. Rohatgi, S.A. Ringel, J. Welch, E. Meeks, K.T. Pollard, A. Erbil, C.J. Summers, P.V. Meyers, and C.H. Liu, "Growth and Characterization of CdMnTe and CdZnTe Polycrystalline Thin Films for Solar Cells," **Solar Cells**, 185-194, 1988.

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16. Abstract (Limit: 200 words)

This report describes research into polycrystalline CdTe solar cells grown by metal-organic chemical vapor deposition. Efficiencies of ~10% were achieved using both p-i-n and p-n structures. A pre-heat treatment of CdS/SnO_2/glass substrates at 450°C in hydrogen atmosphere prior to the CdTe growth was found to be essential for high performance because this heat treatment reduces oxygen-related defects from the CdS surface. However, this treatment also resulted in a Cd-deficient CdS surface, which may in part limit the CdTe cell efficiency to 10% due to Cd vacancy-related interface defects. Preliminary model calculations suggest that removing these states can increase the cell efficiency from 10% to 13.5%. Photon absorption in the CdS film also limits the cell performance, and eliminating this loss mechanism can result in CdTe efficiencies in excess of 18%. Polycrystalline, 1.7-e, CdZnTe films were also grown for tandem-cell applications. CdZnTe/CdS cells processed using the standard CdTe cell fabrication procedure resulted in 4.4% efficiency, high series resistance, and a band-gap shift to 1.55 eV. The formation of Zn-O at and near the CdZnTe surface is the source of high contact resistance. A saturated dichromate etch prior to contact deposition was found to solve the contact resistance problem. The $CdCl_2$ treatment was identified as the cause of the observed band-gap shift due to the preferred formation of $ZnCl_2$.

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