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Advanced High Efficiency Concentrator Cells

Final Subcontract Report
1 October 1988 - 31 March 1990

R. Gale
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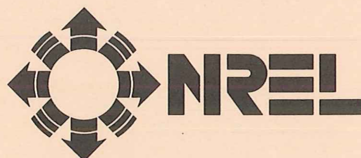
Palo Alto, California



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R. Gale
Varian Research Center
Palo Alto, California

NREL technical monitor: J. Benner

National Renewable Energy Laboratory
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Golden, Colorado 80401-3393
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1. INTRODUCTION

The overall objective of this program is to continue development of the technology needed to demonstrate a monolithic, multijunction, two-terminal, concentrator solar cell with a terrestrial power conversion efficiency greater than 35%.

Under three previous subcontracts, Varian has developed many of the aspects of a technology needed for the fabrication of very high efficiency concentrator solar cells. The development of metalorganic chemical vapor deposition (MOCVD) during the past several years now permits flexible and versatile control of the growth of complex semiconductor crystal structures. Two different designs of cascade cell structures have been developed, which present varying degrees of difficulty for crystal growth, but which also have different potentials for actual use. First, the metal-interconnected two-terminal cascade (MICC) cell is complex and expensive to process, but avoids development of grown-in tunnel junction interconnects and enables separate testing of component cells in a multijunction cascade. During the past two years, advances in MOCVD technology have provided capabilities for higher doping concentrations, which should enable improvements in grown-in tunnel junctions. Thus the second cell design, a two-terminal cascade with grown-in interconnects, is now considered feasible for concentrator cells.

In view of Varian's recent achievements which include demonstration of a 28%-efficient single-junction GaAs concentrator cell and a 24%-efficient AlGaAs-on-GaAs MICC, research on cell structures in the current project will be directed to exploit the new understanding of high efficiency solar cells. The recently improved efficiency in single-junction cells strengthens confidence that 30% efficiencies can be achieved at concentration with single junctions. Such a result is both significant in itself and provides guidance for optimizing individual cells of a cascade structure. The improved performance of the AlGaAs/GaAs cascade cell forces the reconsideration of the assumption that a three-junction cell would be too complex for use in terrestrial systems. This lattice-matched two-junction

cell does not have the greatest potential efficiency for operation under the terrestrial spectrum, but could achieve efficiencies of 35% under high concentration. A two-junction structure with optimum bandgaps might exceed 38% under concentration; however, the crystallographic complexity due to lattice constant mismatch of these two-junction structures makes such a result highly unlikely. The addition of a third low-bandgap InGaAs cell on the back of the GaAs substrates used for the AlGaAs/GaAs structure is a potentially simpler approach than the lattice-mismatched, two-junction, optimum-bandgap structure for achievement of the DOE concentrator cell efficiency goals of greater than 35%.

During this program, Varian has concentrated on developing components and beginning to integrate them into multijunction cascades. The efforts have been devoted to the following areas of development:

(1) growth and fabrication of high-efficiency materials and component cells, 1.93-eV AlGaAs, GaAs, and 1.0-eV InGaAs;

(2) growth and fabrication of 1.93-eV AlGaAs/GaAs metal-interconnected cascade cells (MICC);

(3) growth and fabrication of GaAs concentrator cells with a baseline pilot manufacturing process;

(4) growth of stable, high-conductance, grown-in tunnel junction interconnects;

(5) process development for a low-obscuration, thick metallization and a two-layer antireflection coating for high-efficiency single and multijunction cells;

(6) computer modeling of the AlGaAs/GaAs/InGaAs three-junction concentrator cell and the metal interconnect for concentrator applications.

Progress is highlighted in Section 3 and in greater detail in Section 4.

Portions of this work were partially supported by the Air Force Wright Aeronautical Laboratories.

2. SCOPE OF WORK

This final technical report describes results obtained during the SERI Subcontract XL-9-18103-1 for the period of performance October 1, 1988 to March 31, 1990.

The overall objective of this program has been to continue the development of the technology needed for eventual demonstration of monolithic, multijunction concentrator cells having efficiencies in excess of 35%. During the subcontract, Varian has worked on four specific research tasks: (1) continued development and understanding of MOCVD growth of III-V compounds, especially GaAs, InGaAs and AlGaAs; (2) investigation and development of procedures for MOCVD growth on each side of GaAs substrates sequentially and for processing of cells on both sides of the substrate; (3) improvement of the maximum usable current density for both the high-conductance interconnects, grown-in and metallized; and (4) continued improvement of single-junction GaAs concentrator cells and multijunction cells. These four tasks, as set out in the Statement of Work of the subcontract, are included here for reference.

Task 1: Mechanisms of MOCVD Growth

Work shall be carried out to enhance uniformity and reproducibility of doping, composition and deposition rates in III-V epitaxial semiconductors growth by MOCVD. Initial efforts in this area will focus on the binary GaAs, which is the best characterized of the III-V materials to be grown by MOCVD. Research will continue in the more complex AlGaAs and GaInAs ternary systems. Research shall be performed to improve the quality of these semiconductors and to increase the range of growth conditions under which high-quality material can be deposited.

The efforts on GaAs, AlGaAs and GaInAs will require characterization of doping levels, materials and junction quality, as well as research on and optimization of the quaternary AlGaInAs grading layers necessary to grow subcells. In addition, research under this task shall continue to improve the control of dopant incorporation in GaAs, AlGaAs and GaInAs. The

semiconductors shall be characterized routinely using photoluminescence, optical and electron microscopy, electron microprobe, secondary ion mass spectrometry, and standard measurements of electronic properties (such as capacitance-voltage measurements, Hall and mobility measurements, and sheet resistance).

Task 2: Bifacial Growth Experiments

The ultimate performance of cascade solar cells relies most heavily on the quality of the top cell. In traditional two-cell designs, the bottom cell (and graded layers if needed) serves as the substrate for growth of the top cell. In lattice-mismatched structures, this configuration will likely degrade the performance of the top cell. Recently the concept of bifacial growth on a GaAs substrate has been introduced to eliminate this problem as well as to provide greater latitude in design of the growth sequence, i.e., high-temperature growth can now precede low-temperature growth steps. Research in this task will focus on identification and solution of technical issues associated with bifacial growth. In particular, GaInAs (1.15 to 1.0-eV) cells configured for backside growth will be grown and fabricated on GaAs substrates and on the back of GaAs substrates on which GaAs and/or AlGaAs junctions have been grown. As appropriate, the reverse sequence will also be investigated. The performance of cells on both sides of the substrate will be evaluated to identify any degradation in performance caused by bifacial growth. Potential solutions to any degradation mechanisms will be identified and tested.

Task 3: High-Conductance Intercell Contacts

The development of grown-in intercell contacts capable of high current densities is desired in order to simplify post-growth processing and reduce final concentrator cell costs. The high-conductance junction developed previously works well for one-sun operation. Research in this task will improve the reproducibility and current-carrying capability and minimize adverse effects on crystal morphology of high-conductance interconnects prepared during MOCVD growth. In parallel with these efforts on grown-in contacts which are applicable for current-matched series-connected

cells, work will also be done to improve intercell metal interconnects which can be used for current-mismatched parallel-connected (three-terminal) cells. Recent developments in optically-shaped ("prismatic") cover glass which can effectively eliminate the obscuration of front grids enables the metal-interconnect designs to be used under concentration if adequate interconnect conductances can be achieved. This work will focus on achieving improved and optimized interconnect conductances and patterns appropriate for available prismatic cover glasses.

Task 4: High-Efficiency Single and Multijunction Cells

This task includes the research needed to develop the components of solar cells, including high aspect ratio grid metallizations, isolated contact pads, antireflection coatings, and processing steps such as cleaning, etching or plating. Using the existing computer code, an iterative effort in device modeling will be conducted in which data from the other tasks will be incorporated to optimize cell design. Fabrication of single junction and multijunction cells shall be performed in order to evaluate the quality of semiconductor materials, control of doping, quality of metallizations, and validity of modeling predictions. The characterization of these cells shall include measurement of the current-voltage properties without illumination as well as under 1-sun and multi-sun illumination. Cells shall be fabricated, which are designed for concentrator operation, and tested under very high illumination levels (up to 1000 suns concentration). The increased focus upon reproducibility and uniformity of cell components will require that substantial attention will be given to the component AlGaAs, GaInAs and GaAs single-junction cells, and especially to the GaAs cells.

3. MAJOR ACCOMPLISHMENTS

1. A 1.93-eV AlGaAs/1.42-eV GaAs metal-interconnected cascade cell (MICC) has been manufactured with a 1-sun efficiency of 27.6% AM1.5G measured at SERI in two-terminal operation [1,2]. This is the highest AM1.5G efficiency achieved for a monolithic cascade. This efficiency performance has improved from 23.9% at the end of the previous SERI subcontract. An Entech prismatic cover slide has been added to reduce the obscuration of gridline and cell interconnect metallizations.

2. A 1.0-eV InGaAs cell has been fabricated on the "reverse" side of a low-doped GaAs substrate with a one-sun efficiency of 2.5% AM1.5D and short-circuit current of 14.4 mA/cm^2. Testing has not been done under concentrated sunlight, but open-circuit voltage and fill factor are expected to increase significantly with larger photoinjection. The cell structure is designed to be the third junction of an AlGaAs/GaAs/InGaAs three-junction monolithic cascade cell. The most significant aspect of the latest results is that the spectral response has been increased sufficiently that the lower cell is able to current match the upper 1.93-eV AlGaAs and middle GaAs cells for the first time. The highest photocurrent achieved thus far in a cascade of the upper two junctions is 13.8 mA/cm^2 [1]. The improved spectral response has been accomplished using a n-i-p structure in the InGaAs cell wherein photogenerated carrier drift in the intrinsic region overcomes the reduced diffusion lengths caused by high defect densities in lattice-mismatched material [3].

3. Small-scale manufacturing of GaAs p/n concentrator cells has been attempted with excellent yield of high-efficiency cells. Cell structures were grown on two different OMVPE reactors and processed with an all-evaporated thick metallization to reduce front gridline obscuration below 5% [4]. Yield for the pilot manufacturing process was excellent, with 80% of all 517 cells fabricated having efficiencies of 24 to 26% under concentrated sunlight, AM1.5D [5].

Minor improvements in the antireflection coating process, plagued with problems during this effort, should raise the efficiencies to the 26 to 28% range.

4. Grown-in tunnel junction cell interconnects have been developed which are transparent and thermally stable using C [6] and Si [7] dopants. At the present state of development, the interconnects are stable enough i.e., have sufficiently low resistance-area product after cell growth, to enable operation of the AlGaAs/GaAs cascade at 20X and the GaAs/InGaAs cascade at 100X [8]. Further development is required to incorporate these interconnects into cascade cells and to enable their operation at even higher concentrations.

4. DETAILED SUMMARY OF RESULTS

A detailed summary of results is presented for the work performed during this subcontract. The results are organized according to the tasks described in Sec. 2, Scope of Work.

Task 1: Mechanisms of MOCVD Growth

Minority Carrier Lifetimes in n-GaAs

For p-type GaAs, the minority carrier lifetime is controlled by radiative recombination for the range of doping densities employed for devices. To analyze and design devices such as solar cells and heterojunction bipolar transistors, it is important to develop a corresponding understanding of recombination in n-type GaAs. A collaborative investigation has been undertaken by Varian, SERI and Purdue [9] to determine hole lifetimes in n-GaAs:Se by photoluminescence decay.

The films used for these studies were grown by MOCVD at Varian in a reactor that has produced record quality GaAs solar cells. Films were grown with six different electron densities ranging from $1x10^{17}$ to $5x10^{18}$ cm^{-3}. At each doping density, double heterostructures with five different active layer thicknesses ranging from 0.25 μm to 10 μm were grown. The active layers are bounded by $Al_{0.3}Ga_{0.7}As$ barrier layers doped at $2x10^{18}$ cm^{-3}. Active layer doping densities have been deduced from van der Pauw resistivity measurements. Photoluminescence decay measurements are being made at SERI using time-correlated photon counting techniques of a 10-psec FWHM mode-lock laser. The PL decay data are being analyzed at Purdue by G. B. Lush, a student of Prof. M. Lundstrom, for his doctoral research.

In all, approximately 50 samples were grown for evaluation with partial support by this subcontract. The PL measurements and data analysis are supported by other SERI subcontracts.

Development of 1.0-eV InGaAs on GaAs

The configuration being developed for a three-junction, two-terminal, 35-45%-efficient cell under concentrated sunlight has a 1.0-eV InGaAs lower cell grown on the farside (or back) of a low-doped GaAs substrate, i.e., the opposite side from the upper AlGaAs and GaAs cells. The primary challenge in developing this lower cell is to grow a high-performance 1.0-eV InGaAs cell lattice mismatched to the GaAs substrate that has a high enough J_{sc} to currently match the upper AlGaAs and GaAs cells.

Much of the work in the development of this lower InGaAs cell focused on comparing InGaAs cells grown in two related structures. In the AlGaAs/GaAs/InGaAs monolithic 3-junction structure, the InGaAs bottom cell is grown on the back of a low-doped GaAs substrate. This configuration is termed the "farside" configuration since it is designed such that light first enters the substrate and then the InGaAs cell (as shown in Fig. 1. A lattice-grading layer accommodates the lattice mismatch between the GaAs substrate and the InGaAs cell. A spacer layer of constant-composition AlInGaAs is intended to separate the InGaAs cell from the misfit dislocations generated in the lattice-grading layer. Both the lattice-grading and spacer layers are made transparent to light below the GaAs bandgap by the addition of aluminum. These together are referred to as the lattice-grading structure. Since cross-sectional TEM analysis done by Dr. Al-Jassim at the Solar Energy Research Institute (SERI) of simulated farside growths indicate that planes of misfit dislocations can form at abrupt AlInGaAs/InGaAs interfaces, this interface has been graded in recent growths. The other InGaAs component cell structure pursued is also shown in Fig. 1, termed the "sunnyside" configuration. It is designed such that the light enters the cell without first passing through the substrate. The lattice-grading layer that accommodates the lattice mismatch between the GaAs substrate and the InGaAs cell does not contain aluminum because it does not need to be transparent. Typical layer thicknesses for the farside and sunnyside n/p cells are shown in Fig. 1. The n-type emitter is doped at a level of 1×10^{18} cm^{-3}, and the p-type base is linearly graded from 5×10^{17} cm^{-3} at the junction to 3×10^{18} cm^{-3}.

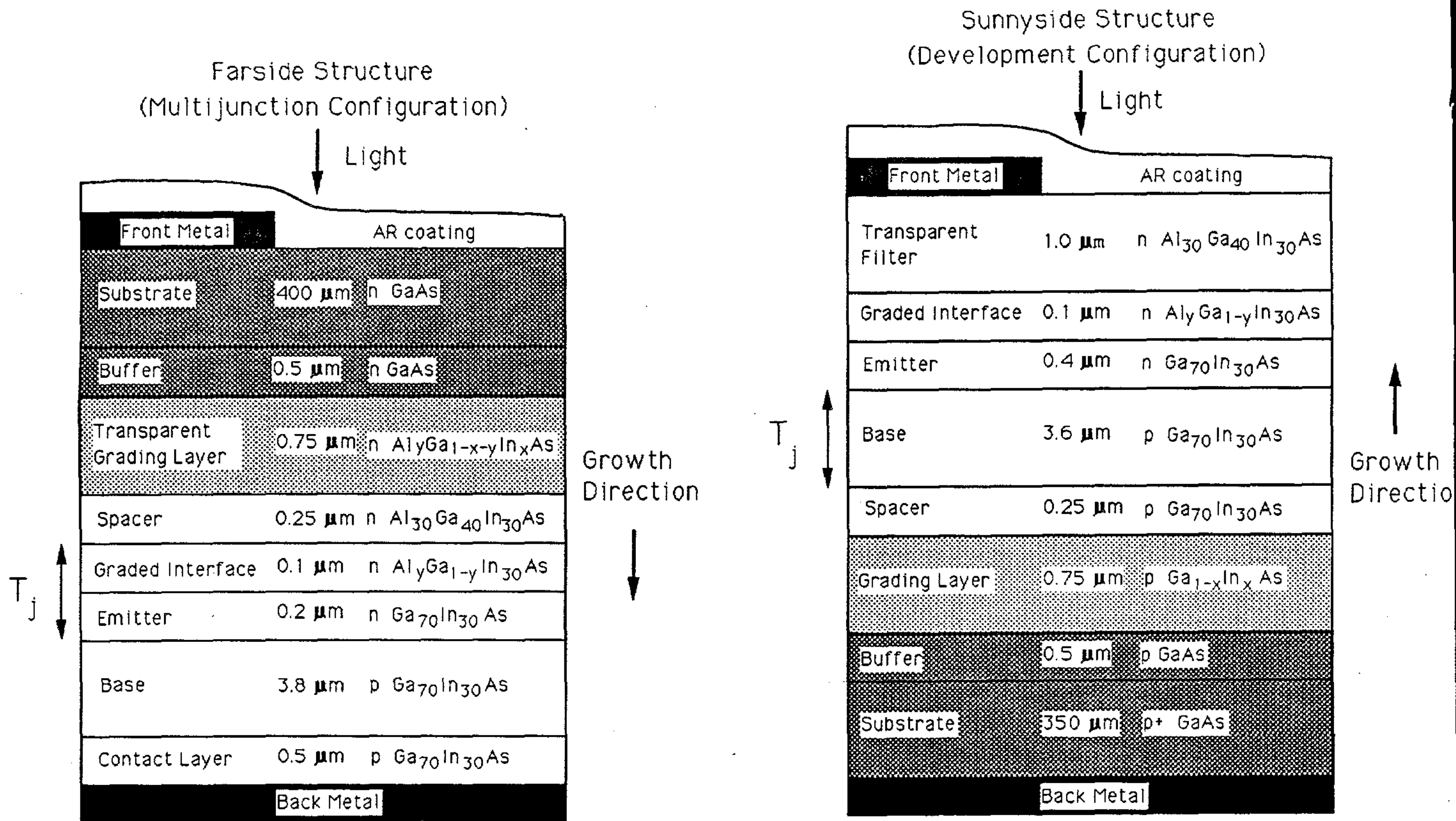


Fig. 1 Farside (multijunction configuration) and sunnyside (development configuration) n/p InGaAs growth structures.

Because of the similarity between these two structures, the sunnyside growth would be expected to approximate the performance of the farside growth. However, n/p farside cells have shown a significantly decreased quantum efficiency, i.e., $\leq$ 80% of that of the sunnyside n/p cells. This decrease is greater than the ~5% decrease due to the optical absorption in the overlying GaAs substrate. Previous work suggested that the degraded performance of the farside configuration is due to the close proximity of the AlInGaAs grading layer and spacer that accommodate the lattice mismatch. This apparently results in shorter minority carrier diffusion lengths in the upper part of the farside cell and/or a higher front interface recombination velocity.

Analysis by transmission electron microscopy (TEM) of a series of 1-μm 1.0-eV InGaAs epilayers grown on AlInGaAs linear grading layers of different thicknesses (from 0.25 to 1.75 μm) gave us some insight into the complicated defect structure that can be expected in the farside growths. Using both cross-sectional and plane-view TEM, clusters of threading dislocations were observed to originate at the AlInGaAs spacer layer/InGaAs cell emitter interface and propagate through the InGaAs epilayer. A plane of misfit dislocations was also observed at this interface. The threading dislocation density in the regions surrounding the "cluster" defects did depend on the grading layer thickness, and was lowest ($5x10^7$ cm^{-2}) for an intermediate thickness of 0.75 μm. However, the farside cell performance is presumably affected by the complex mix of different defects present. In subsequent farside and sunnyside growths, the AlInGaAs/InGaAs interface has been compositionally graded over 0.1 μm. The intent is to minimize the defect formation that can occur at the abrupt interface. Accompanying the compositional grade is a graded bandgap which can provide an electric field to aid in the collection of photogenerated carriers.

The performance of the farside n/p 1.0-eV InGaAs configuration has continued to be significantly below that of the sunnyside n/p 1.0-eV InGaAs configuration and below the 14 mA/cm^2 (1-sun, AM1.5D) J_{sc} needed to current match the upper cells. Midway in this subcontract, we decided to begin work on a n-i-p structure to maximize the current collection in the lower InGaAs cell [3]. The farside and sunnyside n-i-p structures have the same active cell design. The n-i-p structures have an n-type emitter, an undoped intrinsic region, and a p-type base that have thicknesses of 300 Å, 1-2 μm and 4 μm, respectively (shown in Fig. 2). The purpose of the intrinsic region is to produce a broad region where the built-in junction field coincides with the region of optical absorption. This results in field-assisted sweep-out of photogenerated carriers, and therefore a high collection efficiency despite the short diffusion lengths induced by the defects that result from the lattice mismatch to the GaAs substrate.

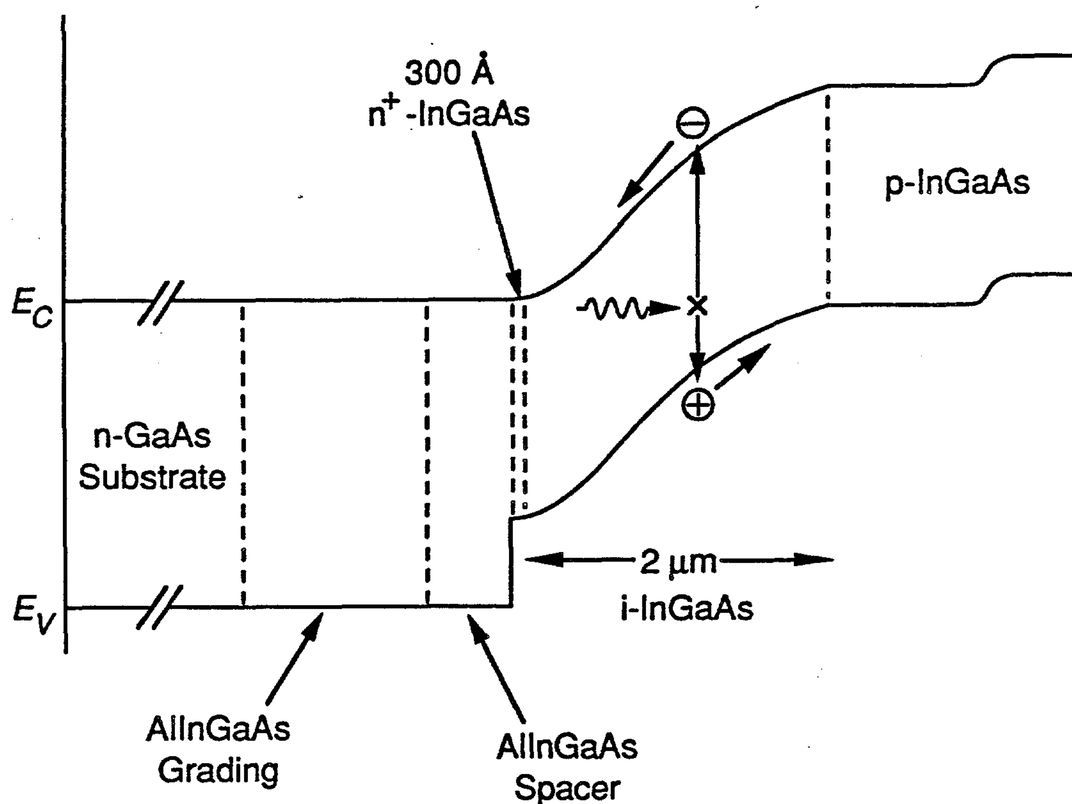


Fig. 2 Schematic cross section and band diagram for farside n-i-p cell.

Using the same diffusion lengths which reproduce the spectral response of the farside n/p cell with the highest 1-sun current achieved thus far (J_{sc} = 10.4 mA/cm^2 AM1.5D), computer simulation of the spectral response of the n-i-p structure shows that this configuration can provide 16 mA/cm^2 (as shown in Fig. 3). It is expected that this gain in J_{sc} will be accompanied by a minimal loss in efficiency due to somewhat lower V_{oc} and FF (as a consequence of higher dark currents in the extended i-region). For growth of the n-i-p structure, the same MOCVD growth conditions as those developed for n/p structures have been used. Atmospheric pressure MOCVD growth is done at 640°C at a V/III ratio of 20, a growth rate of 4-µm/hr and a H_2 carrier gas flow of 13 slpm. The one change is that in order to grow an intrinsic region after growing the n-region, disilane was used for donor doping rather than hydrogen selenide because of the well-known "memory effect" of the latter gas.

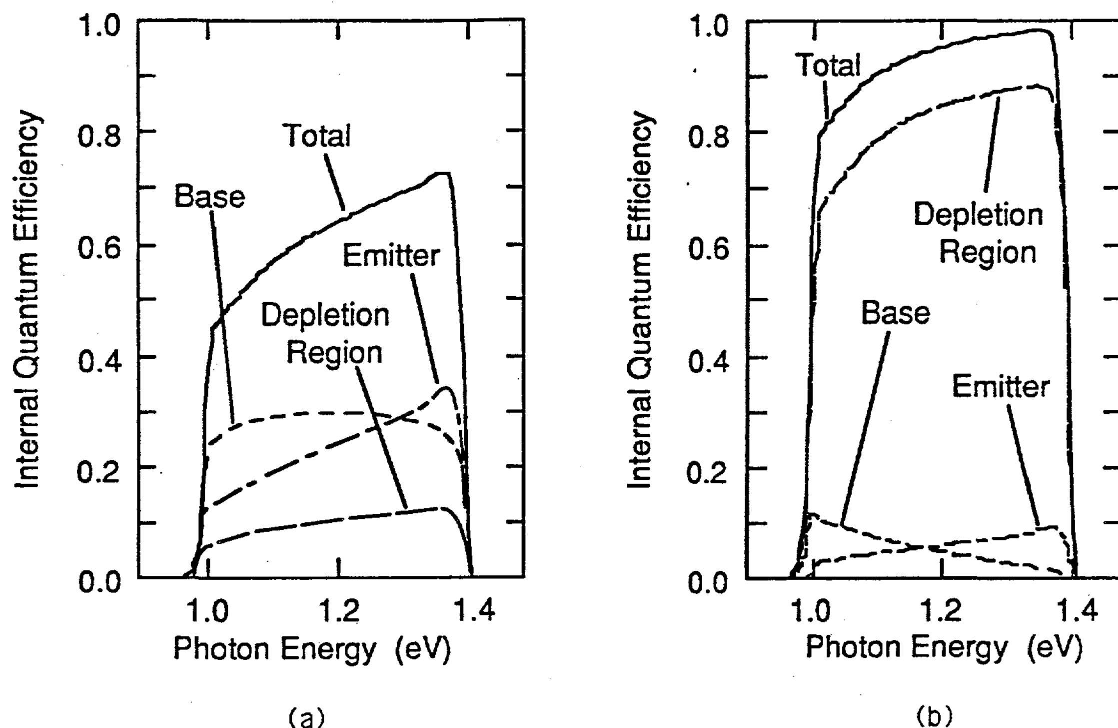


Fig. 3 Calculated spectral responses of: (a) n/p and (b) n-i-p structures using minority carrier diffusion lengths which reproduce for n/p structures the best n/p farside spectral response achieved to date.

During the development of the n-i-p structure, we reviewed optimization of MOCVD growth parameters by comparing spectral responses of InGaAs structures grown under a range of conditions. Over the temperature range 620 to 700°C, the V/III ratio range 10 to 40, and growth rate range 2 to 5 μm/hr, no significant differences were observed.

The advantage of the n-i-p structure for achieving increased photoresponse became immediately evident. In a few months, the short-circuit current density has been increased to 14.4 mA/cm^2, AM1.5D, for a farside cell (shown in Fig. 4). This current is now, for the first time, sufficient to current-match the upper two cells (see Sec. 4) and permit two-terminal operation of a three-junction cascade. Table I compares the cell parameters of the best sunnyside and farside cells to date under AM1.5D illumination.

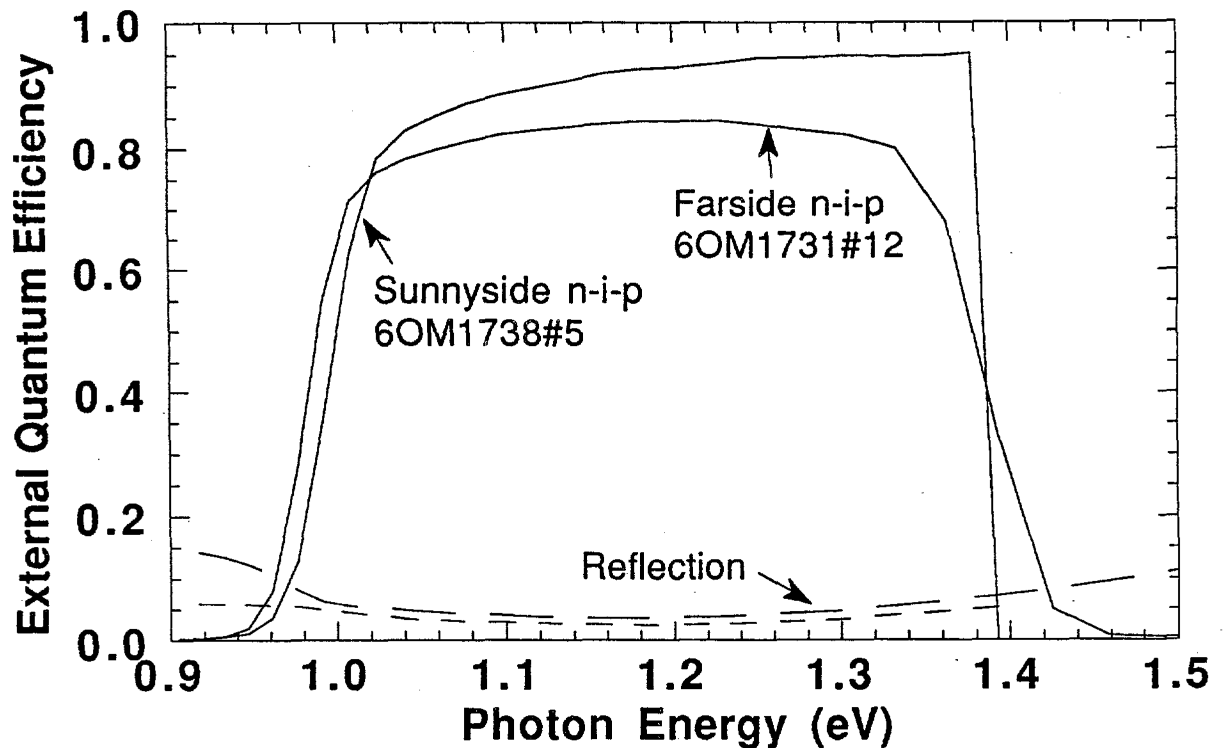


Fig. 4 Spectral responses of highest quantum efficiency sunnyside and farside n-i-p 1.0-eV InGaAs cells.

Table I

Efficiency measurements of sunnyside and farside n-i-p 1.0-eV InGaAs cells that achieved the highest quantum efficiency under 1-sun, AM1.5D, 25°C conditions. (Spectral responses shown in Fig. 4.)

	Sunnyside	Farside
Efficiency (%)	4.9	2.5
V_{oc} (volts)	0.446	0.290
Fill Factor (FF)	0.709	0.610
J_{sc} (mA/cm^2)	15.5	14.4

Note that V_{oc} and FF are significantly higher for the sunnyside cell that for the farside cell. This is likely due to the greater distance of the sunnyside i-region from the grading layer compared to the farside i-region which results in longer carrier lifetimes and lower dark current. These differences in V_{oc} and FF will diminish under concentrated sunlight because of the higher photoinjection. Earlier in this subcontract, a less efficient n-i-p farside cell was tested under concentration. At 130X, FF increased from 0.62 to 0.67 and V_{oc} increased from 0.302 to 0.489V. These results imply that the farside cell recently fabricated with J_{sc} = 14.4 mA/cm^2 would have an efficiency approaching 4.7% AM1.5D if its grid pattern would permit testing at concentration.

Task 2: Bifacial Growth Experiments

During this subcontract, no effort was made to grow cell structures sequentially on both sides of low-doped GaAs substrates. In the preceding section, progress is reported on increasing the farside InGaAs cell spectral response by the end of this subcontract period so that current matching in the multijunction can be achieved for the first time. In the next section, significant progress on the lower intercell contact, a grown-in tunnel junction, is reported. In the previous subcontract, we reported the successful demonstration of sequential growth of high-quality GaAs and InGaAs cells on both sides of transparent GaAs substrates [10]. Now all elements are sufficiently developed to integrate the three-junction cascade cell. Now is the proper time for bifacial growth experiments to be resumed.

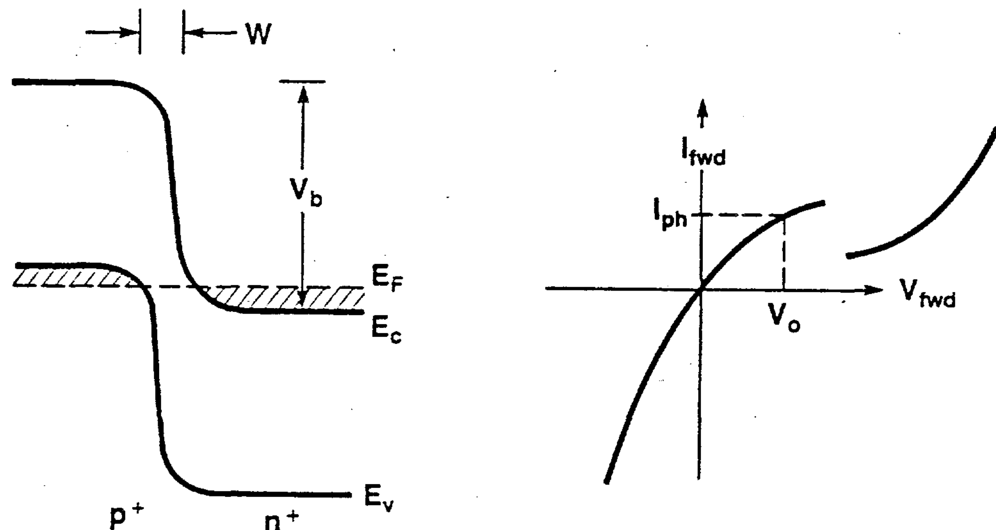
Task 3: High-Conductance Intercell Contacts

<u>Tunnel Junctions with C and Si Dopants</u>

The n-on-p three-junction structure requires two electrical intercell contacts to short out the p-n reverse junctions between the top and middle cells and between the middle and bottom cells. A monolithically grown-in tunnel junction is highly desirable for each interconnect. However, feasible methods to achieve this goal have not been completely implemented.

Development of tunnel junctions, which is described herein, is still underway.

Tunnel junctions are formed by doping the p- and n-type regions of the junction so heavily (10^{19} cm^{-3} and above) that the conduction and valence bands overlap in energy (shown on the left of Fig. 5). If the depletion width W is below about 100Å wide, sufficient amounts of charged carriers can tunnel directly across the junction at low voltage. A discontinuous I-V characteristic results (shown on the right of Fig. 5). The voltage drop V_o at the photocurrent value I_{ph} can be small enough that the ratio V_oA/I_{ph}, i.e., the tunnel junction resistance-area product, is in the range of 1 to 10^{-3} Ω-cm^2.



$$W \ \alpha \left(\frac{V_{b.n}}{N_D}\right)^{1/2} + \left(\frac{V_{b.p}}{N_A}\right) \ ; \ \frac{I}{V} \ \alpha \,(\exp - kW)$$

- SUFFICIENT TUNNELING IF W ≈ 100Å
  N_D, N_A ~ 10^{19} cm^{-3} REQUIRED

Fig. 5 Energy band diagram and I-V characteristics of typical tunnel junctions.

Major obstacles faced in developing tunnel junctions include: (1) achieving high doping levels (above 10^{19} cm^{-3}) in both p and n regions of the junction, and (2) maintaining high conductance tunnel junctions during

MOCVD growth of the overlying cell(s). During this subcontract, dramatic improvement has been achieved in the development of tunnel junctions using: (1) a planar doping technique for n-type Si doping, and (2) atomic layer epitaxy (ALE) for p-type C doping to replace Zn doping.

Figure 6 shows the Si doping of GaAs and AlGaAs using planar doping techniques. Volume donor doping concentrations of $4x10^{19}$ and $2x10^{19}$ cm^{-3} are obtained for GaAs and $Al_{0.28}Ga_{0.72}As$, respectively, grown at 730°C with Si doping planes sandwiched between 30Å thick undoped layers. These doping levels are about an order of magnitude higher than those of n-type GaAs and AlGaAs layers grown by conventional MOCVD techniques. The GaAs tunnel junction in Fig. 7 was grown using Zn doping and planar Si n-doping with the typical resistances for six growths shown at the bottom of the figure. Before annealing, these tunnel junction resistances are variable, but consistently at or below 1 Ω-cm^2. The subsequent growth of the bottom InGaAs cell and its transparent grading layer was simulated by annealing the samples for 2 hours at 700°C. Only two of the samples then retained resistances below 1 Ω-cm^2.

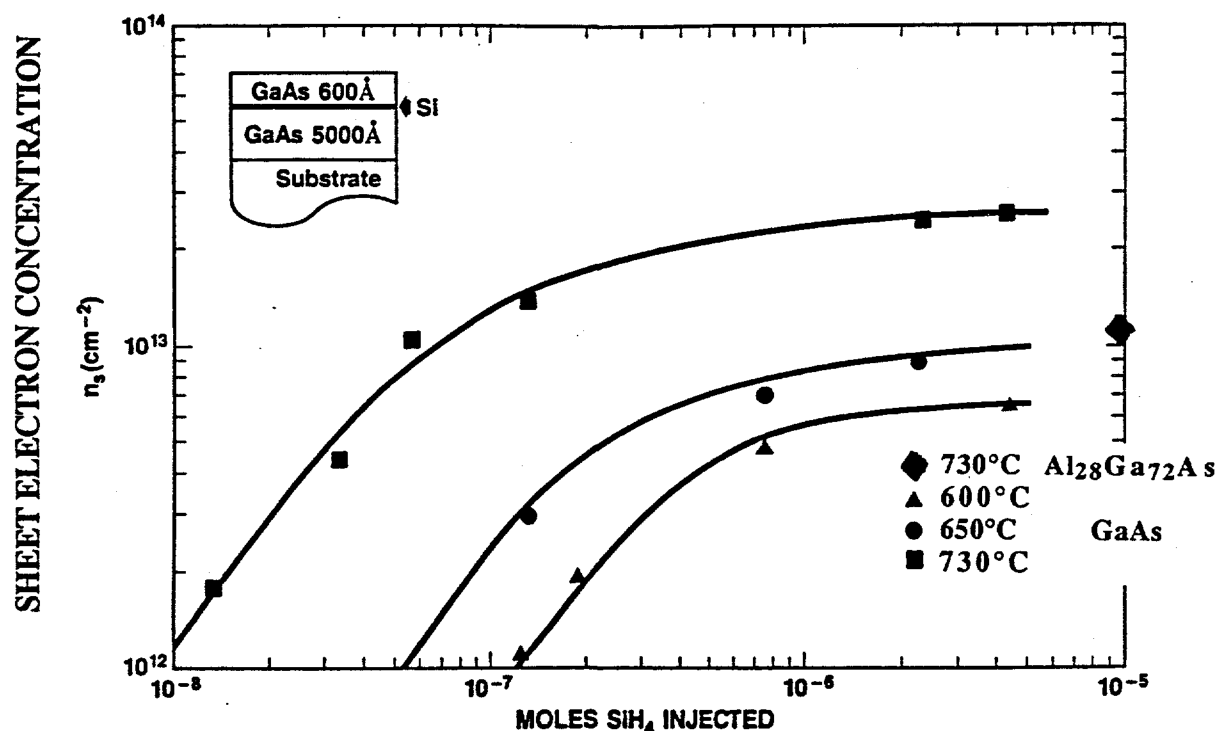
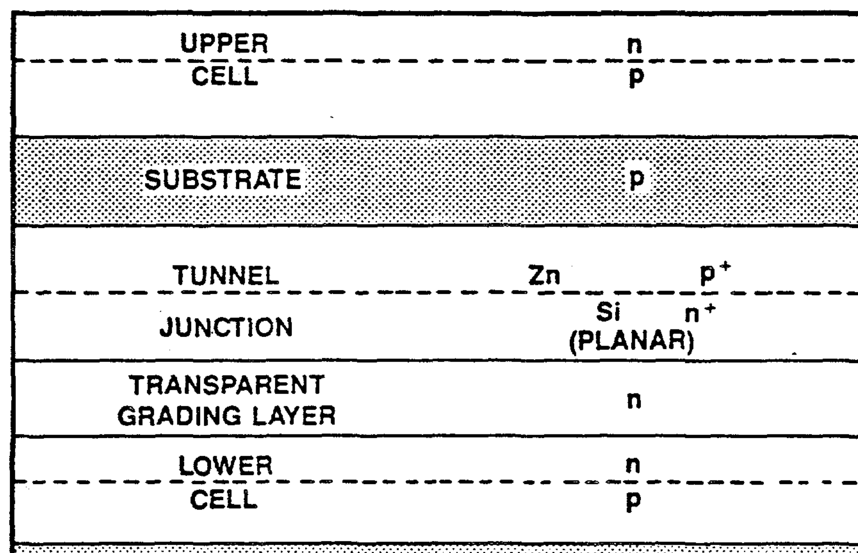


Fig. 6 Planar Si doping of GaAs and AlGaAs



SELECTED RESULTS FOR Si AND Zn DOPING

TUNNEL JUNCTION GROWTH NUMBER	RA ($ohm\text{-}cm^2$) BEFORE ANNEAL*	AFTER ANNEAL**
3519	0.15	0.84
3532	0.37	1.65
3533	0.33	8.0
3621	1.0	500
3630	0.38	0.60
3641	0.56	200

*AS GROWN; 700°C FOR 1 HOUR
**ANNEALLED; 700°C FOR 2 HOURS MORE

Fig. 7 Schematic of Si/Zn tunnel junction interconnect and representative resistance values obtained with it.

Si and Zn dopant profiles were measured on one of these samples (#3621) before and after anneal using SIMS. Initially, the peak Zn and Si levels were well above 10^{19} cm^{-3}, with concentrations that dropped abruptly at their interface (shown in Fig. 8). After the anneal, the peak and interface of the Si dopant were unchanged, but the Zn dopant appears to have diffused several hundred angstroms across the interface. The latter observation is the probable cause for the resistance increases after anneal shown in Fig. 7.

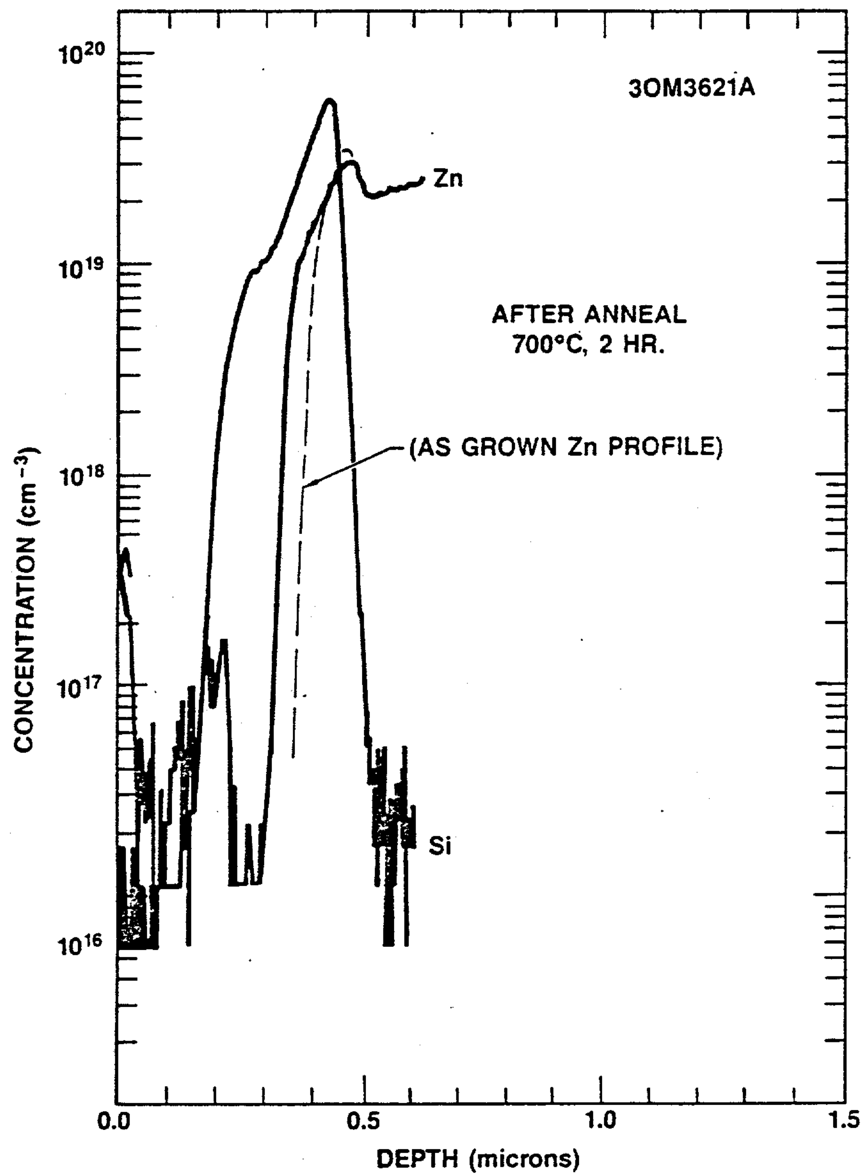


Fig. 8 Dopant concentrations determined by SIMS for the Si/Zn tunnel junction of Fig. 7 after anneal at 700°C for 2 hours.

To alleviate the Zn diffusion problem in the GaAs tunnel junction structure, C is a potential replacement for Zn due to its much lower diffusion coefficient (~10^{-16} cm^2/s at 900°C) compared to that of Zn (~10^{-14} cm^2/s at 800°C). During this subcontract, the ALE process (which takes advantage of plenty of hydrocarbon (C-H) species present in the growth environment) has been used to implement this concept. ALE is essentially a four-step process [6], as depicted in Fig. 9. In the case of GaAs, a monolayer of Ga is deposited from the TMGa source gas, followed by purging the growth chamber with H_2. A monolayer of As is next deposited from the AsH_3 source, which is then also flushed out from the reactor vessel by H_2. Repeating this sequence gives the GaAs epilayer as controlled monolayers generated one after another. For the case of ALE of AlGaAs, TMAl is injected in lieu of TMGa for some of the alkyl inject pulses.

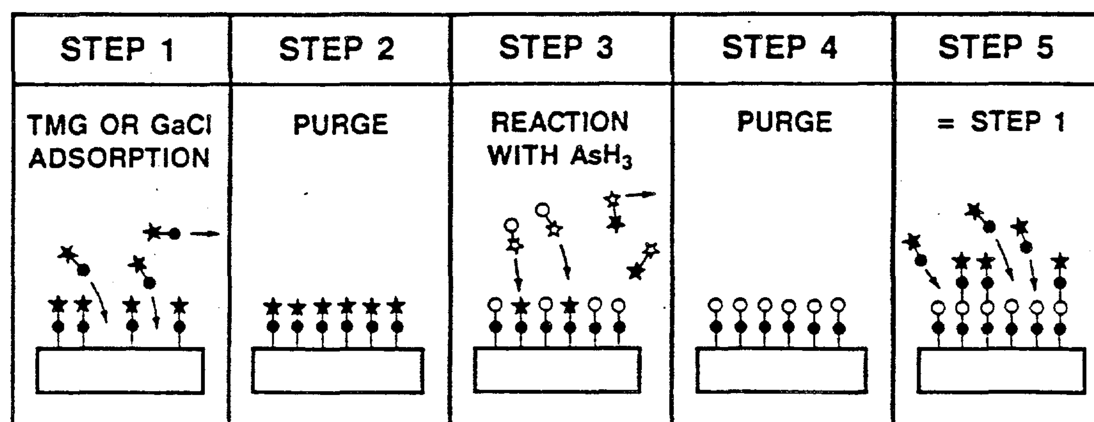


Fig. 9 Schematic diagram for atomic layer epitaxy (ALE).

Successful work in achieving C-doping above 10^{19} cm^{-3} in GaAs prompted the attempt to apply ALE techniques to the development of high C-doping in AlGaAs layers. The organometallic precursors (TMGa and TMAl) present in the growth ambient are the sources of carbon. Carbon and hole carrier concentrations have been studied in the whole Al composition range of $Al_xGa_{1-x}As$ ($0 \le x \le 1$). Figure 10 shows the dependence of carbon and hole carrier concentration on Al content in ALE-grown AlGaAs layers [6].

Hole concentrations as high as $2x10^{20}$ cm^{-3} have been obtained in $Al_{0.5}Ga_{0.5}As$ layers. This is the highest carbon doping level achieved in AlGaAs or GaAs layers grown by MOCVD.

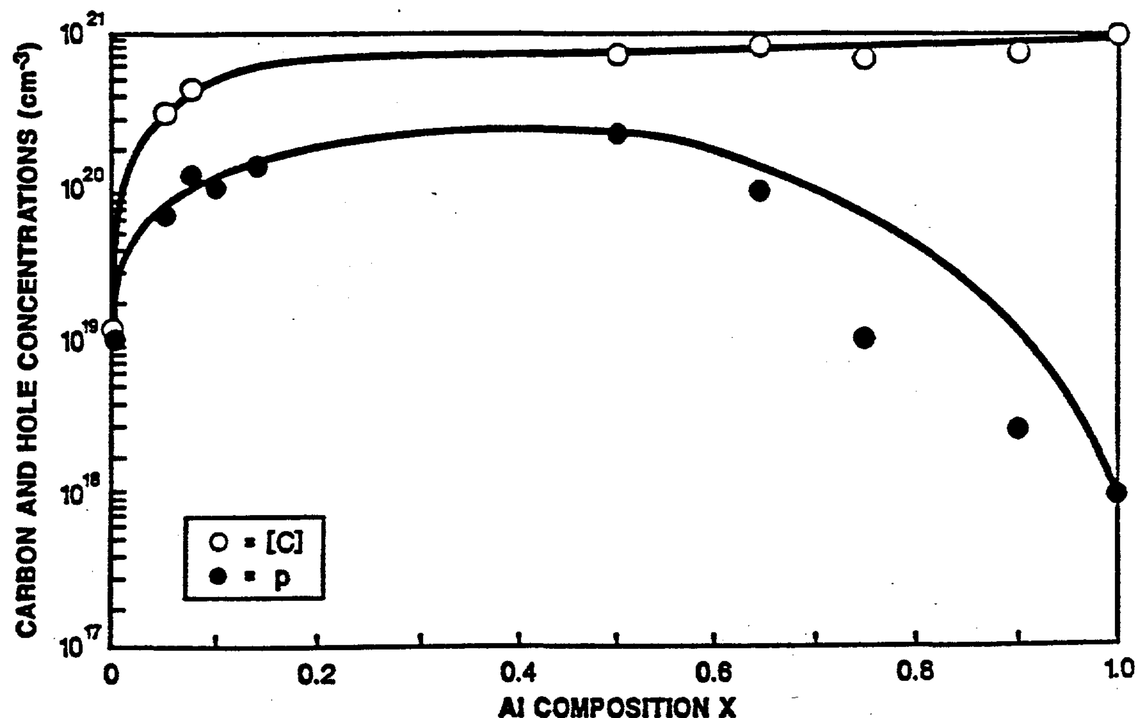


Fig. 10 Dependence of carbon and hole carrier concentration on Al content in ALE-grown $Al_xGa_{1-x}As$ layers.

Figure 11 shows the $Al_{0.5}Ga_{0.5}As$:C/GaAs:Si tunnel junction doping profile grown by these processes (sample OM3-3747) when annealed for 1.5 hours at 700°C. Both the Si n-dopant and C p-dopant profiles are unchanged from their pre-anneal values to within the resolution of this SIMS measurement. The peak C concentration is almost at 10^{21} cm^{-3}, and it falls abruptly at the Si-doped interface. The corresponding tunnel junction resistances for this and four other tunnel junctions with C and planar Si doping are shown in Table II. Four of the five samples have resistance-area values below 1 Ω-cm^2, both before and after anneal. These four are tunnel junctions of $Al_{0.5}Ga_{0.5}As$:C and GaAs:Si. The one tunnel

junction with higher resistance (i.e., OM3-3747) is $Al_{0.5}Ga_{0.5}As$:C and $Al_{0.25}Ga_{0.75}As$:Si. The higher resistance is likely due to the lower Si doping density achieved to date in AlGaAs (shown in Fig. 6). The transparency of such tunnel junctions to photons transmitted by the top AlGaAs cell has not yet been measured, but they are transparent to photons transmitted by the GaAs middle cell.

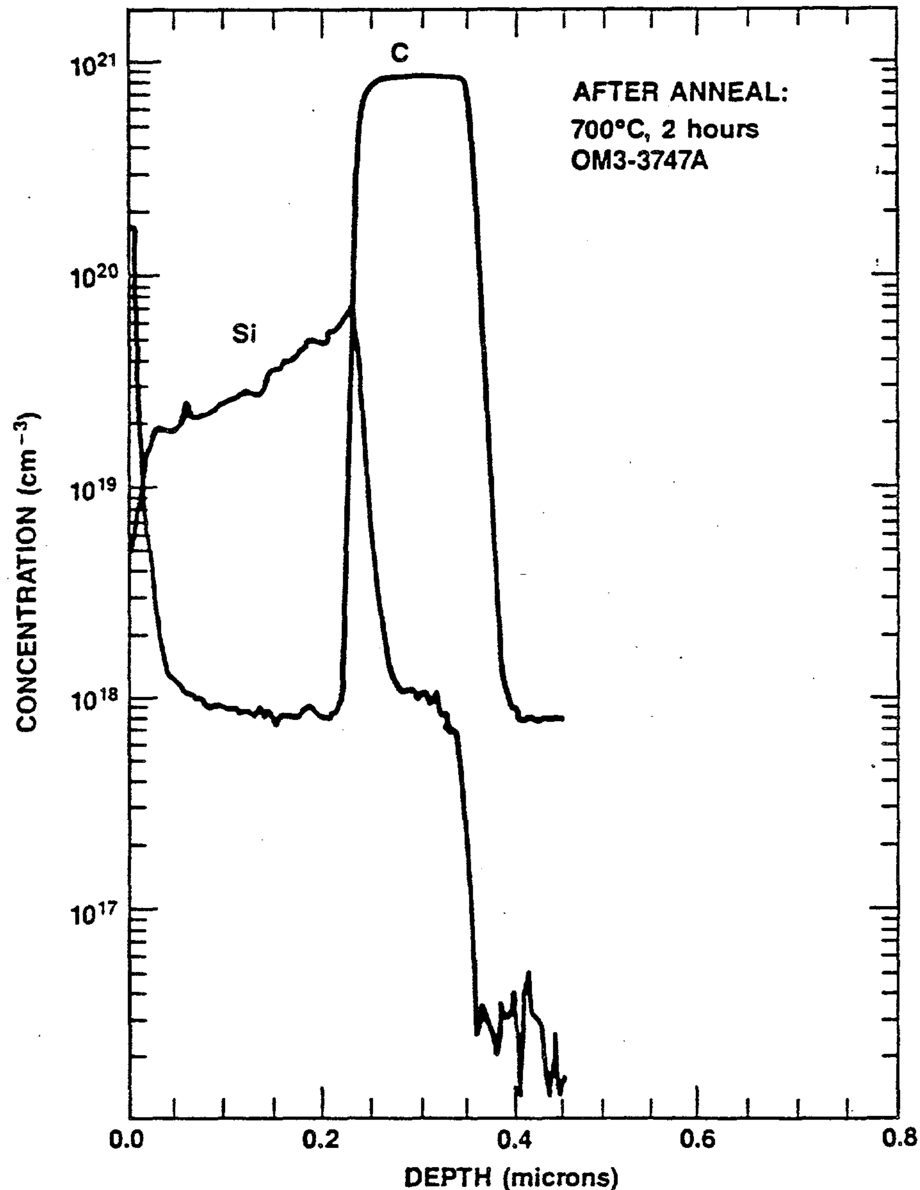


Fig. 11 Dopant concentration determined by SIMS for Si/C tunnel junction.

The tunnel junction resistance-area products shown in Table II indicate that a lower intercell contact between GaAs and InGaAs cells can now be grown in and be used up to solar concentrations of 100X. For the upper intercell contact, the tunnel junction resistance-area product limits its present application to 1X if n-AlGaAs:Si is used for the n^+ layer and to 10X if n-GaAs:Si is used. Since the n-GaAs:Si layer is very thin ($<$350 Å), it will cause less than 5% obscuration of the underlying GaAs cell. These results show substantial progress toward demonstrating grown-in high-conductance intercell contacts for multijunction concentrator cells. The approach looks promising. Significant development is still required to increase tunnel junction conductance and thermal stability, especially for the upper intercell contact.

Table II

Tunnel junction resistances achieved using C p-doping and Si n-doping.

Tunnel Junction Growth Number	Tunnel Junction Resistance (Ω-cm^2)		Anneal Temp. (°C)	Anneal Temp. (°C)
	Before Anneal*	After Anneal*		
OM3-3744	0.02	0.10	700	1.5
OM3-3747	0.03	0.05	700	1.5
		0.30	780	1.5
OM3-3766	0.06	0.12	780	1.5
OM3-3767	3.0	7.0	780	1.5
OM3-3807	0.2	0.02	700	2.0
		0.08	780	1.5

* As grown at 700°C for 1 hour.

MICC Design for 100X Operation

At the present time, the upper two cells of the AlGaAs/GaAs/InGaAs multijunction are interconnected with a metal intercell contact, as shown in Fig. 12. Eventually, it will be desirable to replace the metal interconnect with a grown-in tunnel junction, but as discussed in the preceding section, the upper tunnel junction is not sufficiently developed, especially for concentrator cells. Consequently, during this subcontract we have worked on a design of the metal interconnect for use in multijunction concentrator cells.

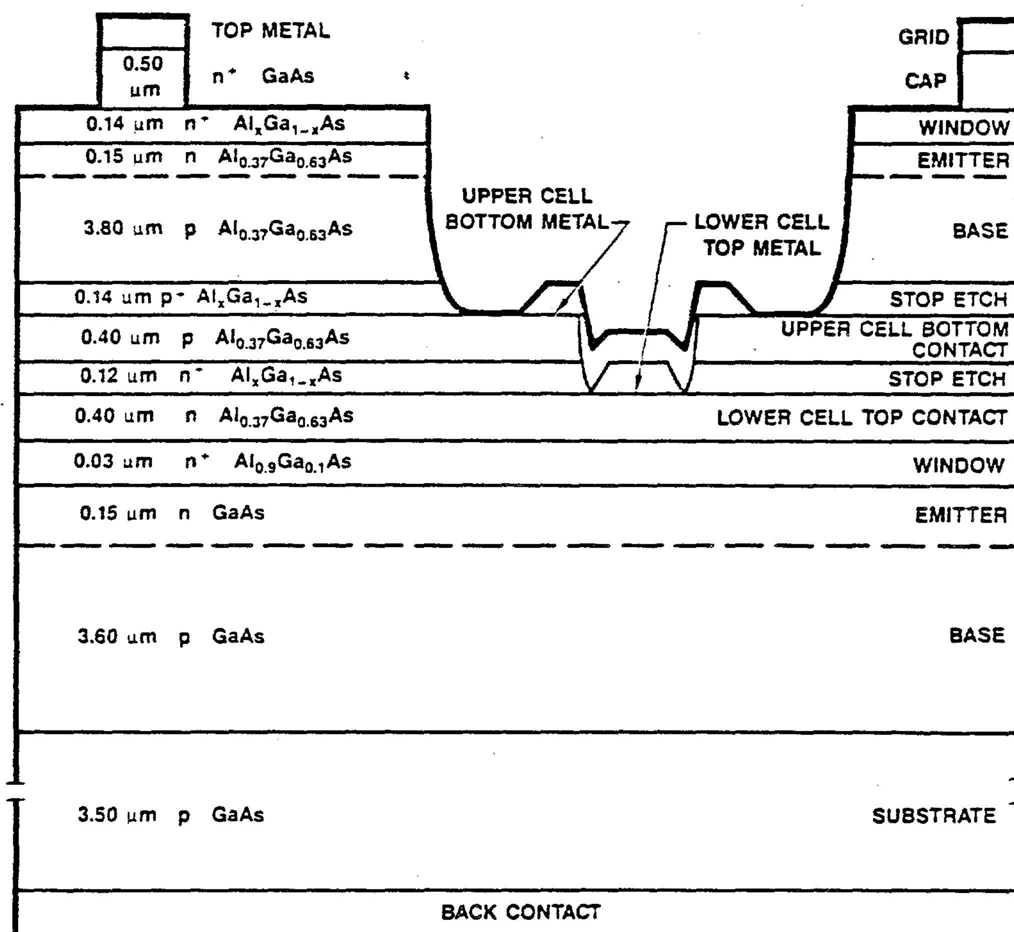


Fig. 12 Metal interconnect cascade cell (MICC).

Table III lists the electrical resistances of the contributing elements in the MICC. The upper part of the table presents resistance values for the interconnect designed for 1-sun operation. The lower half of the table presents resistance values for the interconnect redesigned for 100X operation. The total interconnect resistance is calculated to be 0.015 Ω-cm^2, close to the target of 0.01 Ω-cm^2 and entirely satisfactory for 100X concentrated sunlight. Examination of the key contributions to interconnect resistance suggest that the metal interconnect can be utilized up to approximately 300X. Note that the single largest contributor to cascade cell series resistance is the sheet resistance of the 1.93-eV AlGaAs emitter, which is about three times larger than that of the metal interconnect for the 100X design. Recent results have shown that we can reduce the AlGaAs emitter resistance to approximately 800 Ω-cm^2.

Table III

Resistance-area products for metal interconnect.

Standard 1-sun MICC Growth and Mask				Series R (Ω)	
				R(Ω)	R(Ω-cm2)
Groove Spacing (µm) (GS)	254	BCTM Rc(Ω-cm2)	1.00E-05	0.0010	0.0005
Groove Width (µm) (GW)	40	BCTC Rsh(Ω/sq)	250	0.1620	0.0794
BCTM width (µm)(BCTM)	5	TCBM Rc(Ω-cm2)	5.00E-05	0.0046	0.0023
TCBM width (µm)(TCBM)	5.5	TCBC Rsh(Ω/sq)	1000	0.0612	0.0300
MICC Metal Width (µm)(GMW)	16	TCBC//p Base(Ω/sq)	500	0.2730	0.1338
Groove Length (cm) (GL)	0.7				
Cell Width (cm) (CW)	0.7	Emitter Redundancy	1		
Number of Gridlines	28	Emitter Rsh (Ω/sq)	2000	1.0918	0.5350
		Total interconnect Series R (Ω)		0.502	0.2459
		Target Resistance			1.0
Proposed MICC concentrator Cell					
				Series R	R(Ω-cm2)
Groove Spacing (µm) (GS)	127	BCTM Rc(Ω-cm2)	1.00E-05	0.0005	0.0003
Groove Width (µm) (GW)	40	BCTC Rsh(Ω/sq)	50	0.0081	0.0040
BCTM width (µm)(BCTM)	5	TCBM Rc(Ω-cm2)	5.00E-05	0.0023	0.0011
TCBM width (µm)(TCBM)	5.5	TCBC Rsh(Ω/sq)	250	0.0077	0.0038
MICC Metal Width (µm)(GMW)	16	TCBC//p Base(Ω/sq)	100	0.0111	0.0054
Groove Length (cm) (GL)	0.7				
Cell Width (cm) (CW)	0.7	Emitter Redundancy	2		
Number of Gridlines	56	Emitter Rsh (Ω/sq)	1500	0.0832	0.0408
		Total interconnect Series R (Ω)		0.030	0.0145
		Target Resistance			0.01

Task 4: High-Efficiency Single and Multijunction Cells

All-Evaporated Thick Metallization Process

GaAs concentrator cells require front metal gridlines to carry large photogenerated currents. To accommodate this current while minimizing the number and width of obscuring grid lines, low-resistivity metal of 2-μm thick or more is often used. The best single-junction devices made by Varian thus far have been fabricated with a two-step grid formation process [10]. Requiring two separate process steps, the ohmic contacts are first evaporated and the excess metal lifted off, and then the contacts are thickened with plated gold. The introduction of a photolithographic plating mask has helped to lower obscuration by decreasing ballooning of the grid metal; however, process complexity is increased. A more manufacturable process is desirable for production of large numbers of cells. Our goal has been to develop a process where the ohmic contact and thick conducting metal can be deposited in a single evaporation or sputtering step.

Conducting metals considered for thick evaporation were gold and silver; however, neither satisfied our needs. While evaporated gold was used occasionally, routine deposition of 2-3 μm of gold would be prohibitively expensive. Silver, commonly used in the solar cell industry, was found to be incompatible with our subsequent reactive ion etching (RIE) step for selective removal of the GaAs cap layer. Measures to protect the silver, such as electroplating a protective layer of gold over the grid lines, would introduce process complexity we sought to avoid. Borrowing technology from the silicon IC industry, we opted for aluminum as the conducting metal. Initial concerns over the choice of aluminum centered around two issues: the deleterious reactions with gold (used in our contacts to p-GaAs), and the difficulty associated with soldering to aluminum. These issues have been addressed and resolved [4].

The full metallization, consisting of 1000Å Pt/2500Å Ti/30,000-40,000Å Al/2500Å Ti/2000Å Pt, is deposited by a CHA e-beam evaporator. After liftoff of the excess metal and resist, a sintering step at 420°C for 20 seconds is carried out to ensure uniform ohmic contacts across the wafer.

The initial platinum layer makes an ohmic contact to the p-GaAs cap with a specific contact resistance (R_c) of 5E-06 $\Omega-cm^2$, as measured by TLM pattern diagnostics. It was determined that gold is not necessary for these ohmic contacts. The top layer of platinum permits soldering or welding to the busbars, preventing any interaction between gold-bearing solders and the aluminum. The titanium layers block formation of platinum-aluminum intermetallics which can decrease the conductivity of the aluminum and also make the metallization unsolderable. It should be noted that the thicknesses of the platinum and titanium layers are critical [11]; attempts to reduce them undermined the dependability of the barrier effect. While this metallization is highly vulnerable to many wet chemical processes, it is completely compatible with the RIE steps in our pilot line. A modified version of this metallization has been developed for n-GaAs contacts and is used for the backside of the p-n GaAs cells.

Key to the implementation of the thick evaporated metallization was the development of a suitable feature patterning process. Control of the grid line geometry is the result of successful optimization of a single-layer photolithography reversal process described elsewhere [12-14]. As illustrated in Fig. 13, the photoresist profile obtained has a negative slope,

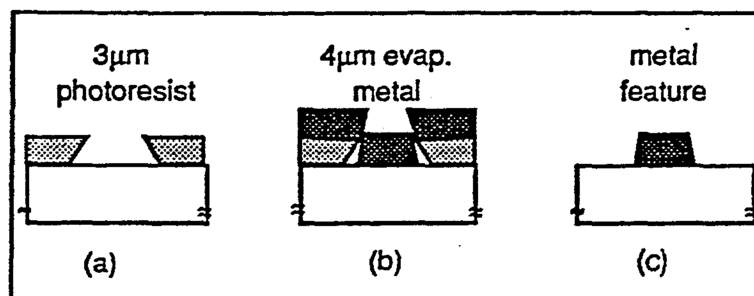


Fig. 13 Schematic of process steps for deposition of thick metallization. Formation of negatively-sloped photoresist profile (a) ensures discontinuity as metal is evaporated onto wafer surface and photoresist (b). Removal of photoresist and excess metal with solvents results in desired metallization pattern on wafer (c).

permitting clean liftoff of the excess metal. This profile works with the highly directional nature of evaporated metallizations, resulting in good separation between the excess metal and the deposited grid lines. The final metal features are approximately 4-μm thick with nearly vertical sidewalls, and height-to-width aspect ratios greater than one can be achieved. This cross-sectional geometry provides sufficient current-carrying capacity with minimal obscuration (<5%) for 1000X concentrator cells.

Two-Layer Antireflection Coatings

During this contract period, considerable progress was made on the development of a two-layer AR coating deposited by reactive rf sputtering. Several combinations have been tried, for both use in air (TiO_2/SiO_2 and NbO_x/SiO_2) and with a bonded cover slide (TiO_2/MgO and NbO_x/MgO). All combinations have shown both good adhesion and toughness. Unlike the single-layer SiO_xN_y previously used, for which the contact pad could be uncovered using chemical etches, the two-layer AR coatings must be lifted off or shadowed. Liftoff is feasible, since the low-temperature sputtering technique is compatible with photolithographic processes.

Figure 14 illustrates the advantages of the two-layer AR coating versus the single-layer coating. The reflections of the two different AR coatings as a function of photon energy has been calculated using a computer model. The model incorporates the measured index of refraction of relevant materials, including the dielectric coatings and III-V cell layers, and has shown excellent agreement with experiment. The two-layer AR coating maintains low reflection over a much wider range of photon energy. While this is advantageous for the single-junction cell, it becomes critical for the performance of multijunction cells. Similar improvements are observed when the AR coatings are optimized for use with a Entech prismatic cover slide or plane cover glass.

During this contract, we have fabricated our first single-junction GaAs cells and multijunction AlGaAs/GaAs cells with two-layer AR coatings. The GaAs cells have two-layer AR coatings for use without a bonded cover

glass. The AlGaAs/GaAs cells have two-layer AR coatings for use with a bonded Entech prismatic cover slide.

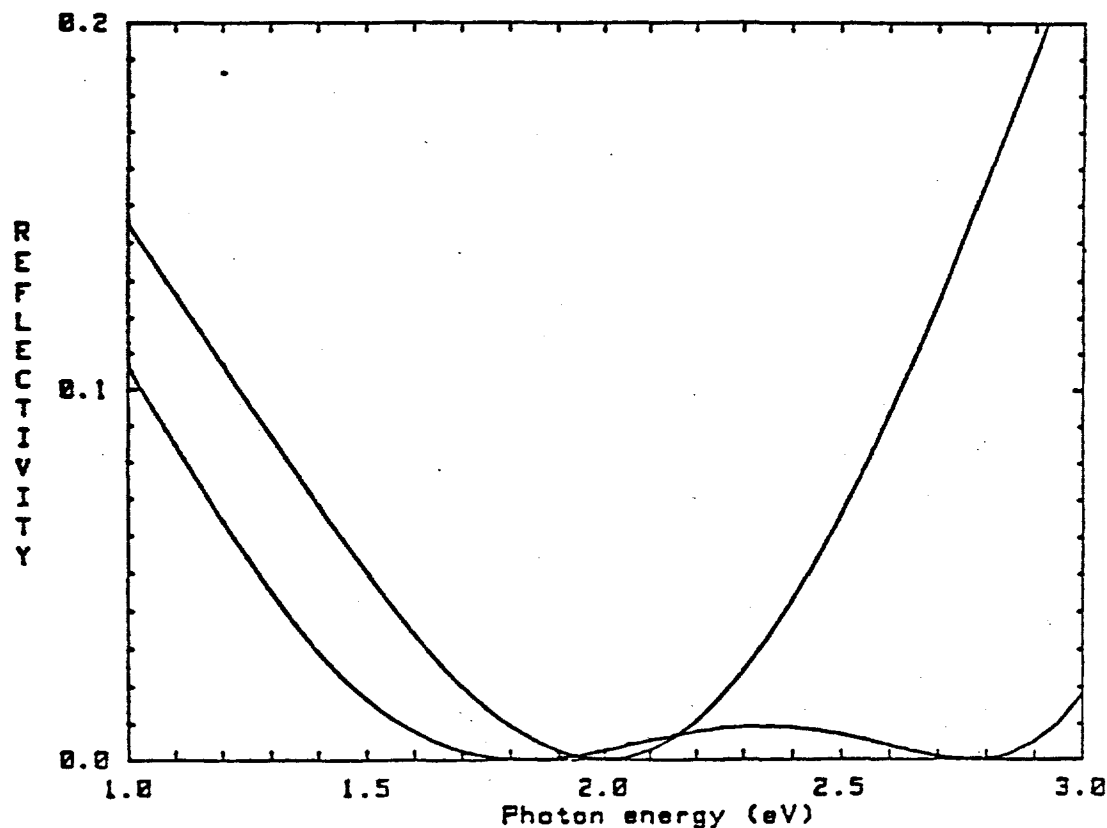


Fig. 14 Calculated reflection versus photon energy for an optimized single-layer SiO_xN_y (upper curve) and a two-layer anti-reflection coating. The incident medium is assumed to have a refractive index equal to 1.

Computer Modeling of Three-Junction Concentrator Cell

The computer code continues to be modified and upgraded to include all relevant electrical and optical interactions required for the optimization of a series- or parallel-connected multijunction monolithic cascade cell. It continues to run on the VAX 11-750 system. Input parameters include minority carrier diffusion lengths and mobilities, cell bandgaps, layer

thicknesses, optical absorption coefficients, layer resistivities, doping levels, contact resistances, surface recombination velocities and the desired cell geometry. The substitution of experimental data for literature values of materials parameters (in particular, minority carrier properties and optical absorption coefficients) is ongoing. Such data has been obtained from growths of high-quality individual layers of the materials of interest. The model can incorporate the effects of interconnect resistance and of grid obscuration and geometry for each cascade structure. The model is regularly updated to reflect new information obtained for actual cell processing and performance.

Output parameters include open-circuit voltage, short-circuit current and fill factor. These results are used in the design of optimized mask set geometries and for the prediction of ideal layer compositions for an optimized cascade structure. The model serves as a useful starting point for the empirical optimization of real solar cell structures.

Modeling predictions of multijunction performance parameters for a three-junction AlGaAs/GaAs/InGaAs cascade shown in Fig. 15 are shown in Fig. 16 for 1-sun, AM1.5D (direct) illumination. The predicted efficiency of the same cascade under concentrated AM1.5D illumination is shown in Fig. 17. The increase in efficiency under concentration results primarily from the increased output voltage of each component cell. These calculations did not include losses due to intercell contact resistances or to obscuration due to an intercell metal contact. Consequently, these predictions are realistic upper limits on three-junction performance.

The bandgaps of the three junctions are those determined by a computer optimization program to provide maximum AM1.5D efficiency for a two-terminal, three-junction cascade cell. The maximum efficiency occurs when there is equal photocurrent generation in all three junctions, as continuity dictates that the current will be limited to the smallest photocurrent.

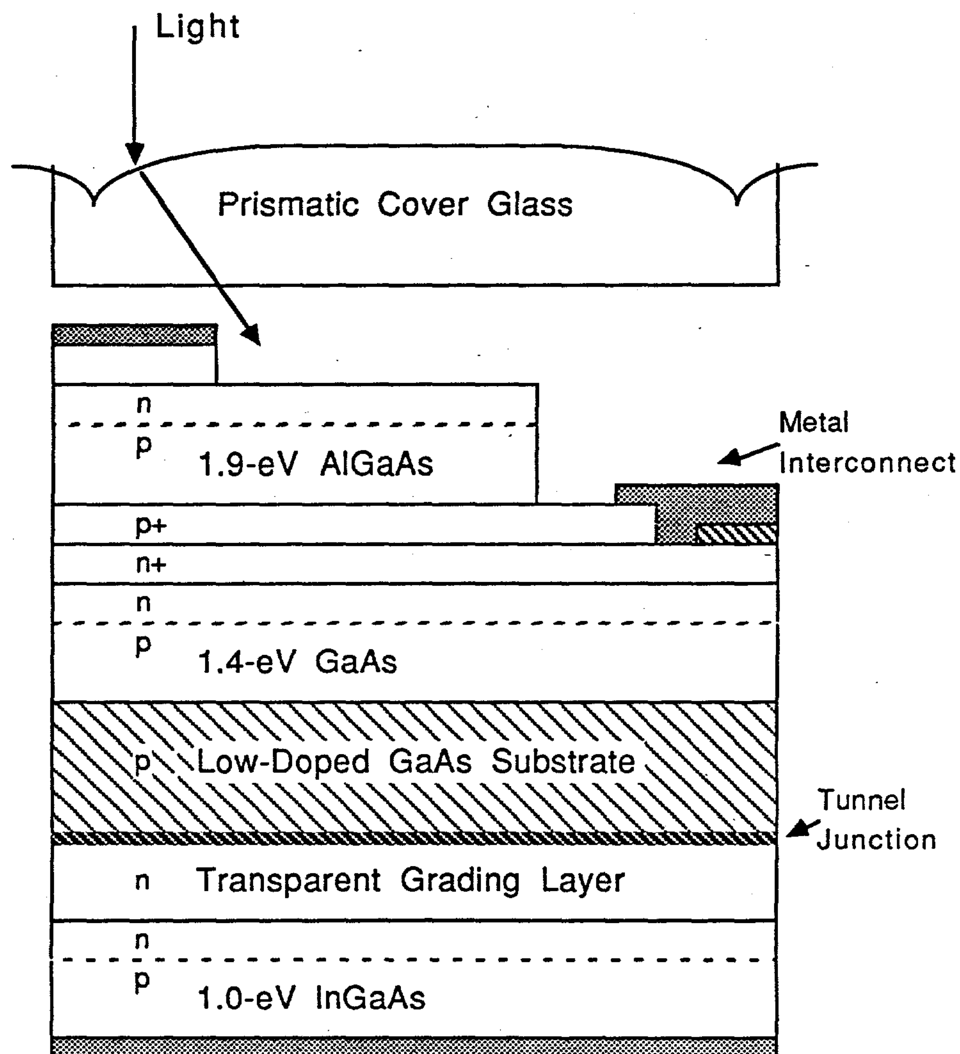
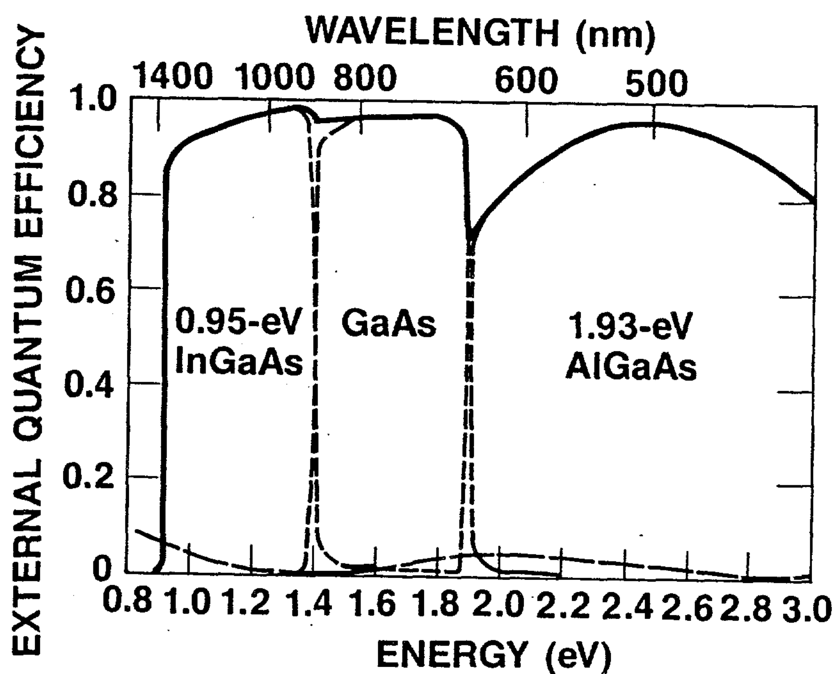


Fig. 15 Schematic cross section of three-junction AlGaAs/GaAs/InGaAs cascade cell.



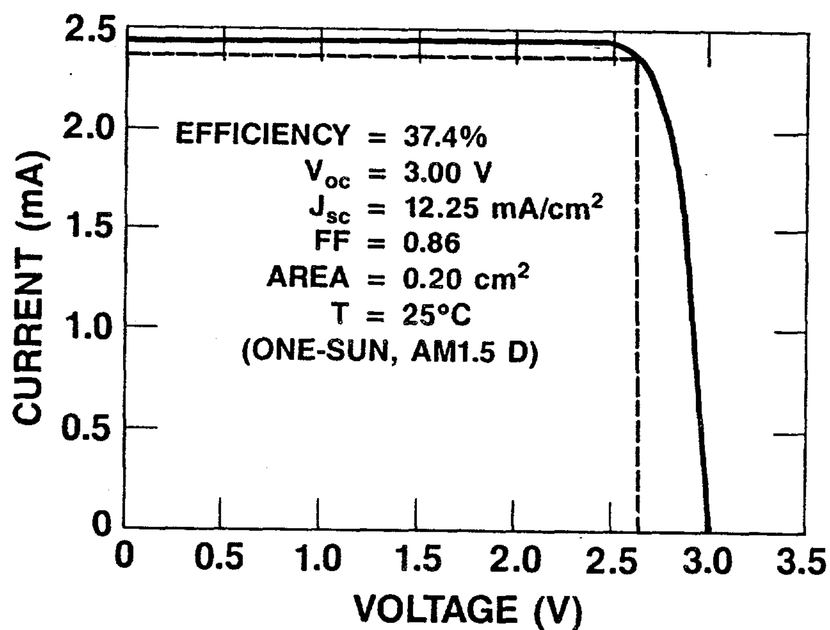


Fig. 16 Predicted spectral response (a) and current-voltage characteristics at 1-sun AM1.5D (b) for AlGaAs/GaAs/InGaAs monolithic, two-terminal cascade cell.

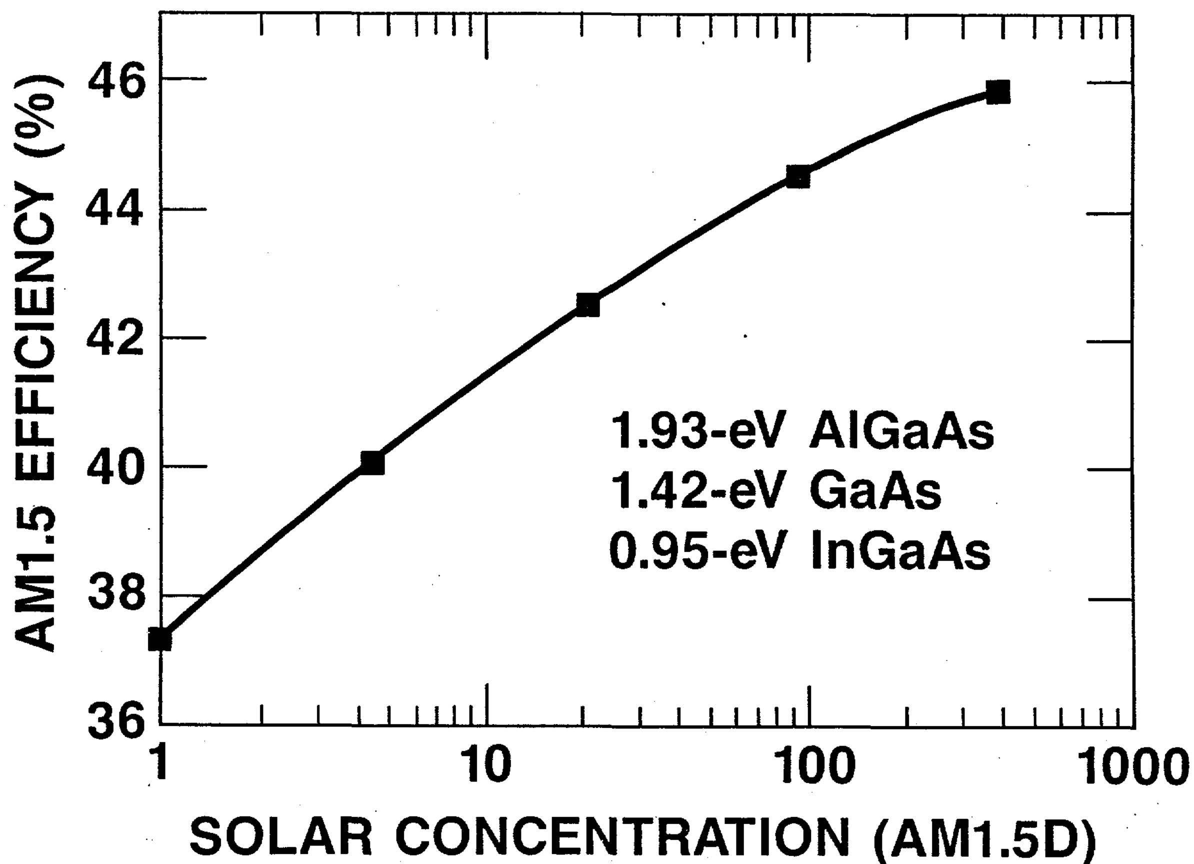


Fig. 17 Predicted efficiency of AlGaAs/GaAs/InGaAs cascade under concentrated AM1.5D illumination, 25°C.

The predicted 1-sun efficiency of the three-junction cascade is shown in Fig. 18 for a range of lower cell bandgaps. The maximum efficiency is at 0.95 eV. The gradual decline in efficiency for lower bandgaps is due to decreasing voltage which results from decreasing bandgap. The sharp decline in efficiency for larger InGaAs bandgaps is because the reduced photocurrent in the lower cell limits the current and hence the efficiency of the entire cascade. At the optimum InGaAs bandgap, the calculated contributions of the three junctions to the total cascade efficiency are: AlGaAs 18.6%, GaAs 12.2%, InGaAs 6.6% at 1-sun AM1.5D; and AlGaAs 21.6%, GaAs 15.1%, and InGaAs 9.1% at 400-sun AM1.5D. The predicted total cascade efficiency is 37.4% at 1 sun and 45.8% at 400 suns.

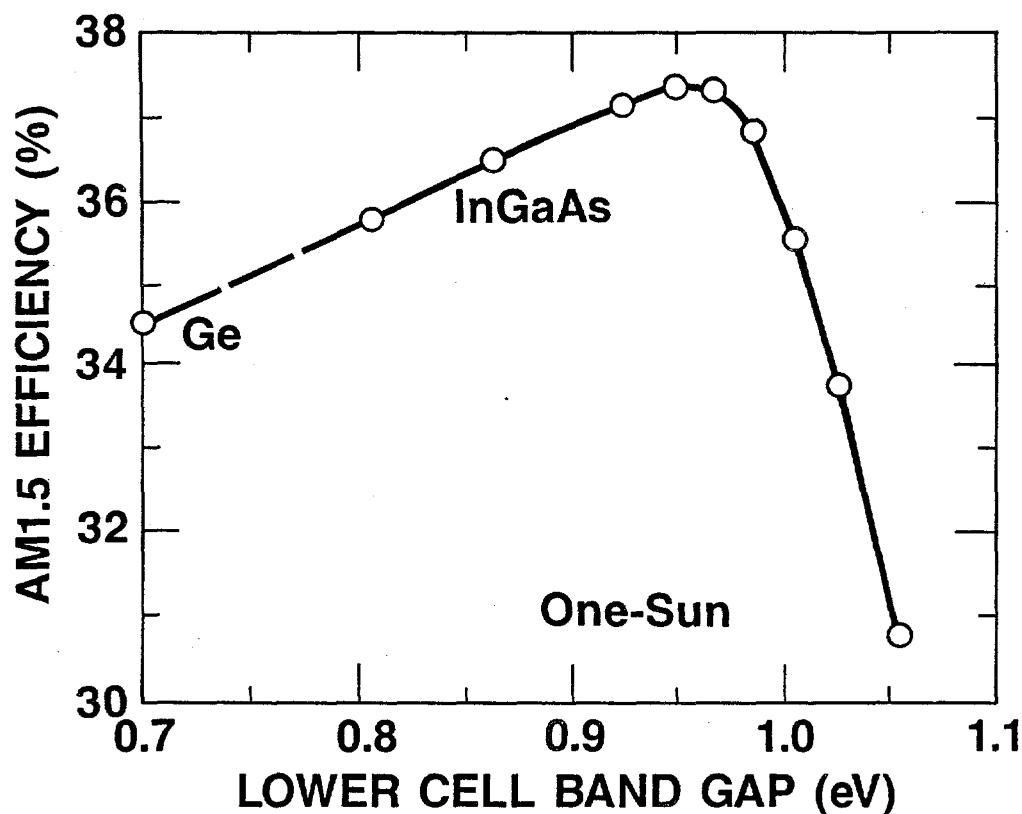


Fig. 18 Predicted efficiency of three-junction cascade at 1-sun AM1.5D for range of lower cell bandgaps.

<u>AlGaAs/GaAs MICC</u>

High efficiency 1.93-eV AlGaAs upper cells and GaAs middle cells under 1.93-eV AlGaAs are a prerequisite for a high-efficiency monolithic AlGaAs (E_g = 1.93-eV)/GaAs (E_g = 1.42-eV) two-junction cascade solar cell [10]. Due to the difficulties in developing a tunnel junction at the present time, the top and middle cells are electrically connected with metal interconnects formed during post-growth processing. This eliminates the unwanted p-n junction between the top and middle cells.

The schematic cross section of the metal-interconnected cascade cell (MICC) is shown in Fig. 12. The growth conditions for the component cells in the MICC are the same as those described previously [10]. The processing procedure for the MICC consists of seven major steps: (1) top

metallization (Au/Ge/Ni/Au) to upper cell, (2) wide groove etch, (3) deep groove etch plus top metallization (Au/Ge/Ni/Au) to lower cell, (4) bottom metallization (Au/Zn/Au) to upper cell, (5) isolation trench, (6) back contact (Au/Zn/Au) evaporation, and (7) MgO/TiO_2 two-layer AR coating.

The n-type contact deposited on top of the contact layer of each component cell consists of Au/Ge/Ni/Au, with thickness of 500/150/300/150 Å, respectively. The sheet resistance in the emitter of the 1.93-eV AlGaAs upper cell is typically 1600 Ω/sq. After evaporation of the Au/Ge/Ni/Au to the n-type AlGaAs conducting contact layer of the lower cell, Au/Zn/Au with thickness of 100/300/200 Å, is deposited on the p-type AlGaAs conducting contact layer of the upper cell. The p-type metallization only makes ohmic contact to the Zn-doped AlGaAs conducting layer, and also shorts the unwanted junction between the component cells by making electrical contact to the Au/Ge/Ni/Au of the Se-doped AlGaAs conducting layer. The sheet resistance of the Se- and Zn-doped conducting layers are typically 280 and 2000 Ω/sq, respectively. Both conducting layers are of the same bandgap as the active layers of the upper cell; therefore, these layers are transparent to photons passing through the upper cell to be absorbed by the GaAs lower cell. Evaporation of Pt/Au/Pt/Au (500/500/1000/2000 Å) to the back of the substrate is done after the isolation trench of the cells on the wafer is completed.

The cell active area including gridlines is 0.5 cm^2, and it is isolated at its perimeter by a deep groove trench. Two-layer plasma-deposited TiO_2/MgO (528/850 Å) is applied as the AR coating. With the help of computer simulation, the thickness of the two-layer AR coating is carefully chosen to minimize the reflection of photons in the AM1.5 solar spectrum from the front surface when the prismatic cover slide is bonded to the cell (see earlier section).

In order to minimize the optical obscuration of the grid lines and metal interconnects, a prismatic cover slide (Entech, Inc., Dallas, TX) has been used to deflect the incident photons toward the active area of the cell. Figure 19 shows the external quantum efficiency obtained from spectral response measurements of the MICC before (a) and after (b) bonding of the

prismatic cover slide to the front cell surface. The difference is due to the obscuration of the grid lines and metal interconnect. Due to the improper match of the refractive indices between the two-layer AR coating and the air, the reflection shown as the broken curve was detected from the cascade cell. Nevertheless, after the prismatic cover slide is bonded to the cell, not only the reflection is minimized, but also a dramatic increase of the external quantum efficiency is observed. The utilization of the prismatic cover slide has resulted in a 21% and 9% increase of the external quantum efficiency in the upper and lower cells, respectively. To date, the highest efficiency achieved by a MICC operating as a two-terminal device is 27.6% AM1.5 Global. The current-voltage characteristic of this cell under 1-sun, AM1.5G is shown in Fig.20.

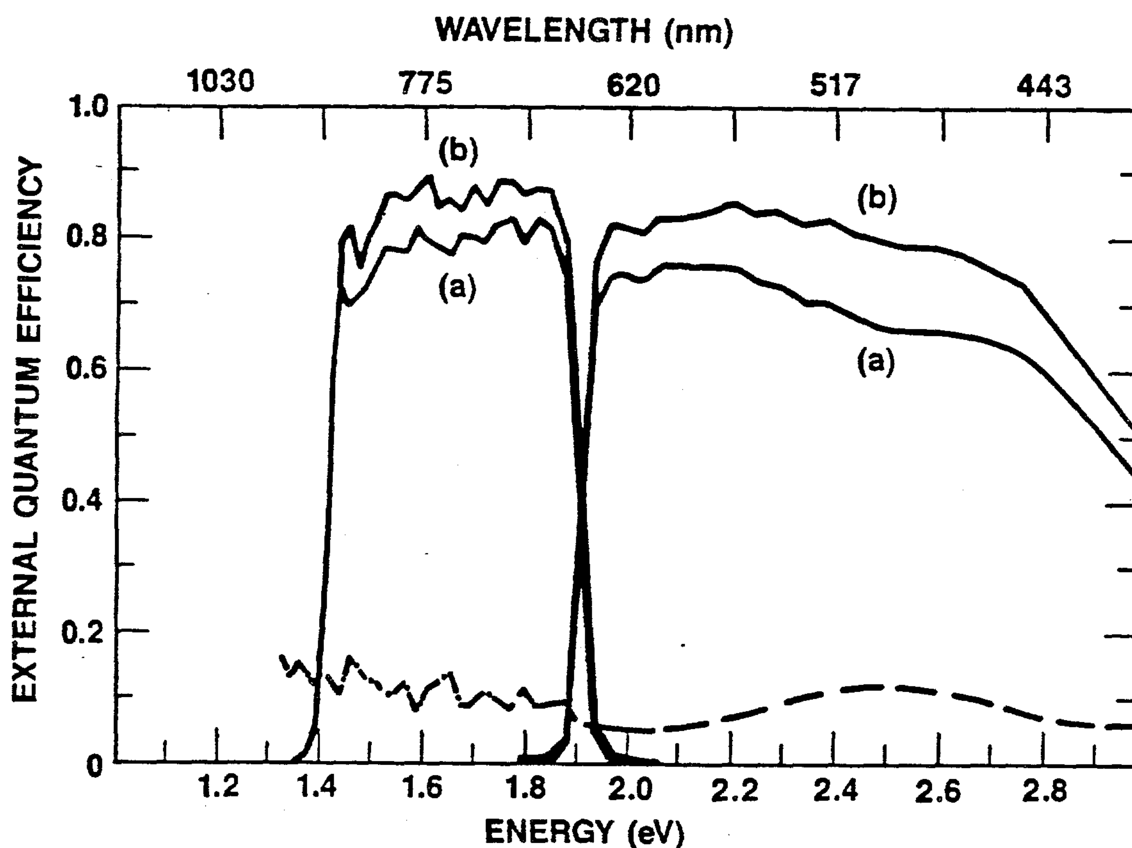


Fig. 19 Quantum efficiency spectra of MICC: (a) without the prismatic cover glass and (b) with prismatic cover slide.

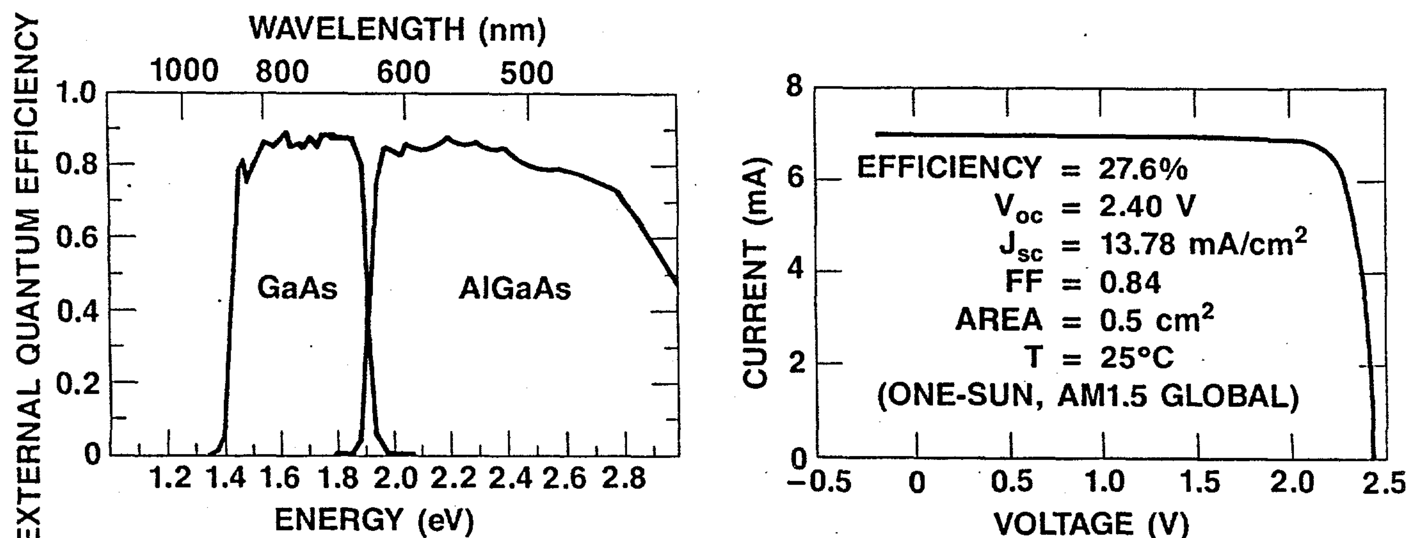


Fig. 20 Current voltage characteristic of 27.6%-efficient, two-terminal MICC under 1-sun, AM1.5G illumination.

In our preceding subcontract, we reported a three-terminal MICC with efficiency of 23.9% AM1.5G [10]. The improvement since that result, represented by the latest MICC efficiency of 27.6% AM1.5G, is dramatic. For the first time, a III-V cascade cell has surpassed the performance limit believed possible for any single-junction cell at 1-sun. The principal reasons for the latest advance in performance are incorporation of the Entech prismatic cover slide, the two-layer AR coating, and the improved AlGaAs materials quality, i.e., spectral response.

Pilot Manufacturing of GaAs Concentrator Cells

Pilot line production of 2x2-cm^2 GaAs space cells has been demonstrated [4] using multiwafer OMVPE reactors and batch processing techniques. During this contract, these high-throughput techniques have been applied to the manufacture of high-efficiency GaAs concentrator cells. A total of fourteen wafers were grown and processed into 516 p/n GaAs

concentrator solar cells designed for terrestrial operation at 1000 suns. The cells have a 5-mm diameter active area and 6x6-mm die size.

The wafers for these cells were grown in two atmospheric OMVPE reactors. Four of the wafers came from a home-built research reactor, while the other ten wafers were produced in a commercial multiwafer reactor from CVD Equipment. Equally good results were obtained from both reactors. The growth structure, depicted in Fig. 21, was designed to minimize both the sheet resistance in the emitter layer and the contact resistance in the cap and window layers. These parameters are important for cell performance at high concentration, and control of such parameters allows use of a grid pattern with minimal obscuration, as shown in Fig. 22 [15].

Thickness	Material	Layer
		FRONT CONTACT
0.6 μm	GaAs (p^+)	(cap) / AR COATING
400Å	$Al_{0.9}Ga_{0.1}As$	WINDOW
0.7 μm	GaAs	EMITTER 2.5×10^{18} p
3.8 μm	GaAs (n) 5×10^{17}	BASE
0.2 μm	$Al_{0.2}Ga_{0.8}As$	MIRROR
0.6 μm	GaAs	BUFFER
350 μm	GaAs	SUBSTRATE
		BACK CONTACT

Fig. 21 GaAs p.n concentrator cell structure.

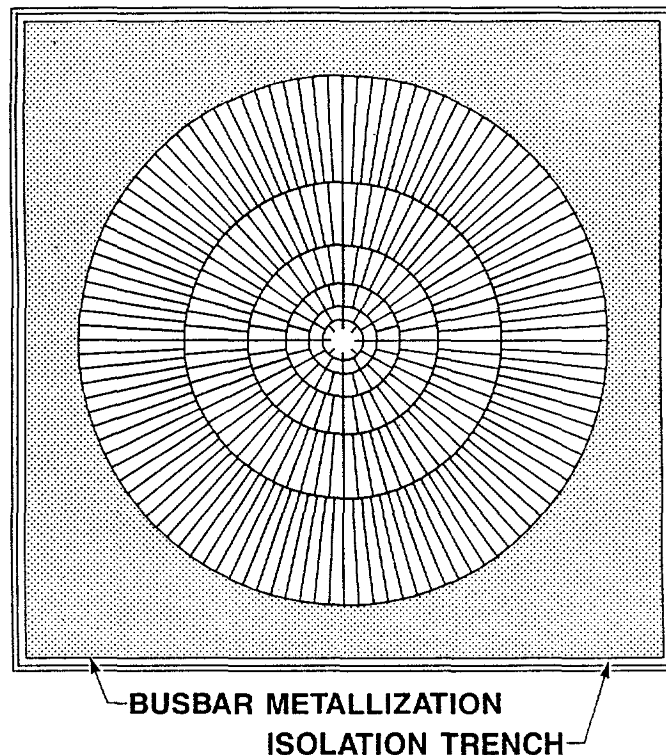


Fig. 22 Top view of GaAs concentrator cell showing active area, grid pattern, busbar metallization (interconnect pad) and isolation trench.

The process centers around the use of an evaporated thick aluminum front grid line metallization and dry etching techniques. The metallization is of particular importance because concentrator solar cell designs require front metal grids to carry large amounts of photogenerated current. To accommodate this current density while minimizing the number and width of obscuring grid lines, the metallization must be approximately 4-μm tall with nearly vertical sidewalls. This cross-sectional geometry provides sufficient current-carrying capacity with grid line obscuration below 5%.

After backside metallization, the front grid features are formed using photolithographic image reversal, evaporation and liftoff as described earlier. The front and back contacts are then sintered in a rapid thermal annealing system. Both the isolation etching of the devices and the selective removal of the GaAs cap layer between grid lines are carried out

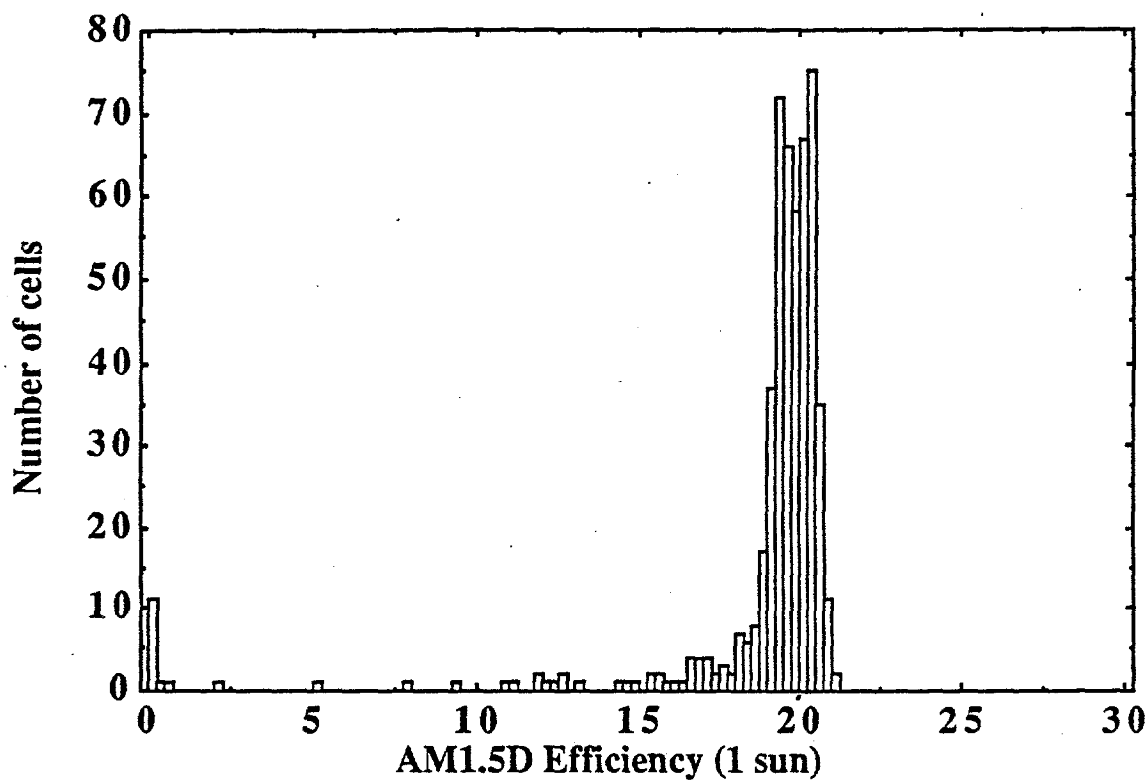
by RIE in the Varian Zylin-30 loadlocked system. A single-layer SiO_xN_y AR coating is deposited by plasma-enhanced chemical vapor deposition (PECVD) and then removed from the contact pads by RIE.

The completed cells had front and back metallizations that were both solderable and weldable. All cells were screened while still in wafer form on an automated tester to determine one-sun AM1.5D efficiencies. The results of this one-sun test are shown in the top histogram of Fig. 23. Measurements of sheet resistance and contact resistance were also conducted at this point, and these numbers were correlated to cell performance at concentration. The bottom histogram shows the results of flash tests at 750 suns for 59 cells randomly selected from those cells with one-sun efficiency in the range 19 to 21% AM1.5D.

Overall, we have demonstrated 81% yield for 516 GaAs cells with efficiencies of 24.5 to 26.5% AM1.5 at 750X, 25°C. These efficiencies are one to two percentage points lower than achieved earlier [15]. The open-circuit voltages and fill factors are excellent, but the short-circuit currents of the cells are unexpectedly low. The cause is believed to be associated with the RIE cap etch step and AR coating step sequence which were not well controlled during the period these cells were processed. The net result is a 5% reflection/absorption loss in cell spectral response. The present cost of these GaAs cells is approximately $2.50/Wp at 800X using pilot line manufacturing batch processing. Cells from this group have been incorporated into a twelve-cell, 1000X concentrator module which has demonstrated 22.3% overall power conversion efficiency in a tracker at Varian [16].

Task 5: Cell Deliverables

In response to SERI subcontract requirements and to a request by Dr. John Benner, ten (10) GaAs cells have been delivered to SERI. The ten cells are 6x6-mm GaAs p/n concentrator cells selected from cells described earlier, which were tested at one sun to have efficiencies in the range 19-21% AM1.5D. The cells were not flash tested at 750X. They have been sent to Dr. Keith Emery at SERI for his use.



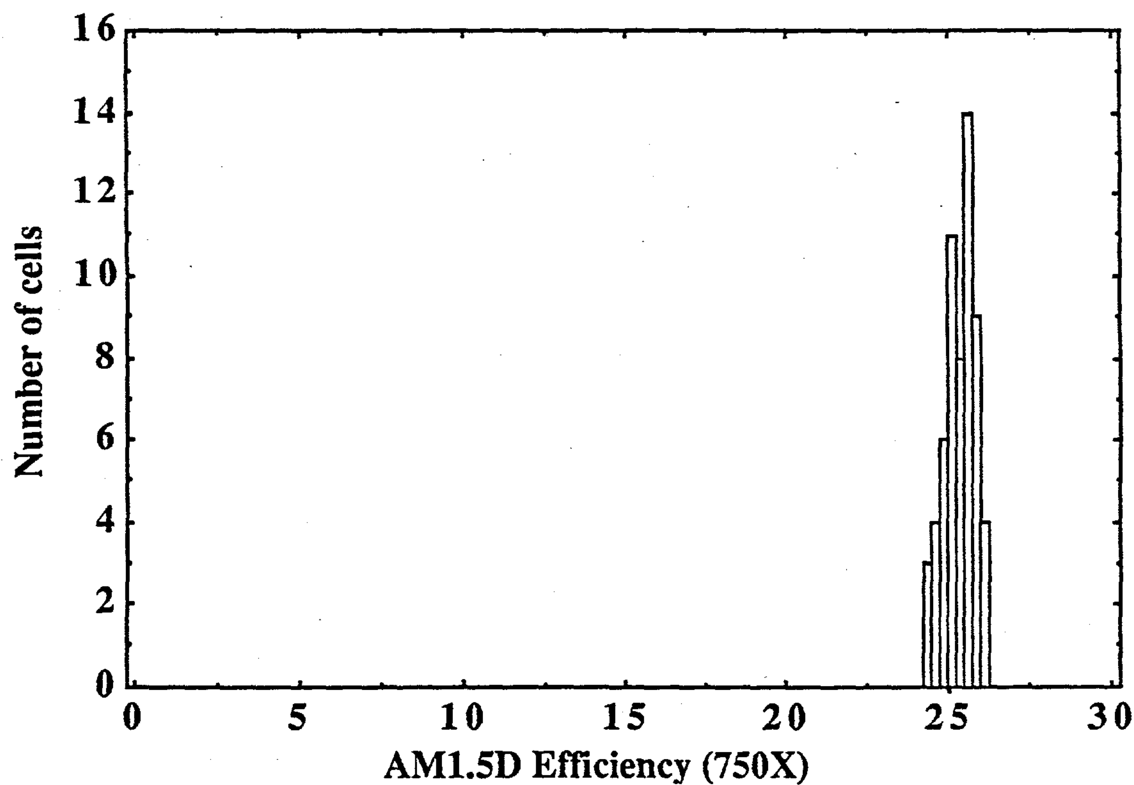


Fig. 23 Efficiency histograms of GaAs p/n concentrator cells. Upper 1-sun histogram is for all 516 cells fabricated from 14 wafers. Lower histogram is for 59 cells chosen randomly from the 19-21% range of 1-sun results and flash tested at 750X, 25°C.

5. SUMMARY AND CONCLUSIONS

During this subcontract period, a number of key results have been obtained; the most important are reiterated here:

1. A 1.93-eV AlGaAs/1.42-eV GaAs metal-interconnected cascade cell (MICC) has been manufactured with a 1-sun efficiency of 27.6% AM1.5G measured at SERI in two-terminal operation [1,2]. This is the highest AM1.5G efficiency achieved for a monolithic cascade. This efficiency performance has improved from 23.9% at the end of the previous SERI subcontract. An Entech prismatic cover slide has been added to reduce the obscuration of gridline and cell interconnect metallizations.

2. A 1.0-eV InGaAs cell has been fabricated on the "reverse" side of a low-doped GaAs substrate with a one-sun efficiency of 2.5% AM1.5D and short-circuit current of 14.4 mA/cm^2. Testing has not been done under concentrated sunlight, but open-circuit voltage and fill factor are expected to increase significantly with larger photoinjection. The cell structure is designed to be the third junction of an AlGaAs/GaAs/InGaAs three-junction monolithic cascade cell. The most significant aspect of the latest results is that the spectral response has been increased sufficiently that the lower cell is able to current match the upper 1.93-eV AlGaAs and middle GaAs cells for the first time. The highest photocurrent achieved thus far in a cascade of the upper two junctions is 13.8 mA/cm^2 [1]. The improved spectral response has been accomplished using a n-i-p structure in the InGaAs cell wherein photogenerated carrier drift in the intrinsic region overcomes the reduced diffusion lengths caused by high defect densities in lattice-mismatched material [3].

3. Small-scale manufacturing of GaAs p/n concentrator cells has been attempted with excellent yield of high-efficiency cells. Cell structures were grown on two different OMVPE reactors and processed with an all-evaporated thick metallization to reduce front

gridline obscuration below 5% [4]. Yield for the pilot manufacturing process was excellent, with 80% of all 517 cells fabricated having efficiencies of 24 to 26% under concentrated sunlight, AM1.5D [5]. Minor improvements in the antireflection coating process, plagued with problems during this effort, should raise the efficiencies to the 26 to 28% range.

4. Grown-in tunnel junction cell interconnects have been developed which are transparent and thermally stable using C [6] and Si [7] dopants. At the present state of development, the interconnects are stable enough i.e., have sufficiently low resistance-area product after cell growth, to enable operation of the AlGaAs/GaAs cascade at 20X and the GaAs/InGaAs cascade at 100X [8]. Further development is required to incorporate these interconnects into cascade cells and to enable their operation at even higher concentrations.

After several subcontracts and a decade of steady support from SERI, technical development has reached the point where integration of the three-junction cascade can begin in earnest. All of the necessary components have reached a stage where operation at concentrations up to 100X is possible; i.e., the 1.93-eV AlGaAs/GaAs MICC, the lower 1.0-eV InGaAs n-i-p cell and the lower intercell tunnel junction as well as the thick gridline metallization and two-layer AR coating.

In parallel with these component developments, we have demonstrated high yield pilot manufacturing of GaAs concentrator cells. In another program, we are presently performing a pilot manufacturing demonstration of the two-junction AlGaAs/GaAs MICC. These initial manufacturing efforts are providing invaluable experience necessary to successfully manufacture multijunction concentrator cells with terrestrial efficiencies above 35%.

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16. Abstract (Limit: 200 words)

This report describes research to develop the technology needed to demonstrate a monolithic, multijunction, two-terminal, concentrator solar cell with a terrestrial power conversion efficiency greater than 35%. Under three previous subcontracts, Varian developed many of the aspects of a technology needed to fabricate very high efficiency concentrator cells. The current project was aimed at exploiting the new understanding of high efficiency solar cells. Key results covered in this report are as follows. (1) A 1.93-eV AlGaAs/1.42-eV GaAs metal-interconnected cascade cell was manufactured with a one-sun efficiency of 27.6% at air mass 1.5 (AM1.5) global. (2) A 1.0-eV InGaAs cell was fabricated on the "reverse" side of a low-doped GaAs substrate with a one-sun efficiency of 2.5% AM1.5 diffuse and a short-circuit current of 14.4 mA/cm^2. (3) Small-scale manufacturing of GaAs p/n concentrator cells was attempted and obtained an excellent yield of high-efficiency cells. (4) Grown-in tunnel junction cell interconnects that are transparent and thermally stable using C and Si dopants were developed.

17. Document Analysis

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