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High-Efficiency Cadmium Telluride and Zinc Telluride Based Thin-Film Solar Cells

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1. INTRODUCTION

Recent advances in polycrystalline thin film CdTe solar cells have generated a lot of interest in this area. Thin film CdTe cell efficiencies in excess of 14% have been verified with the potential of approaching 20%. However, in order to attain this potential, considerable amount of basic research needs to be done. More specifically, there is a need to understand the loss mechanisms including optical losses, bulk and interface recombination, grain boundary effects and resistance losses. Several different technologies have produced thin film CdTe cell efficiencies in excess of 10%. However, different loss mechanisms are not understood well enough to make a precise comparison between the technologies and provide guidelines for improvements. It may be necessary to develop new tools and models, and apply existing tools more prudently, in order to reveal and quantify loss mechanisms in CdTe solar cells.

The motivation for developing a wide bandgap photovoltaic material stems from the fact that the optimum two cell tandem design consists of 1.7 eV bandgap cell on top of a 1 eV bandgap cell. A high efficiency wide bandgap cell on top of a 15% efficient low bandgap cell can give tandem cell efficiency on the order of 20%. Considerable progress has been made on the bottom cell, particularly $CuInSe_2$ which has reportedly given a small active-area efficiency > 14%. But the 1.7 eV bandgap material on II-VI elements for the top cell has not yet been discovered.

There are two ways of realizing ~20% efficient polycrystalline tandem solar cells. The first approach involves improving the CdTe cell efficiencies in excess of 15% and utilizing only a small amount of power from the bottom cell because of 1.5 eV bandgap

of CdTe. The second approach is to develop a high efficiency (>10%) 1.7 eV bandgap cell with significant subgap transmission and take greater advantage of the high efficiency (~15%) bottom cell. This research addresses both approaches by fabricating CdTe as well as 1.7 eV bandgap CdZnTe solar cells.

The overall goal of this program is to improve basic understanding of CdTe and ZnTe alloys, by growing and characterizing these films along with cell fabrication. The major objective is to develop wide bandgap (1.6-1.8 eV) material for the top cell, along with compatible window material and transparent ohmic contacts, so that cascade cell design can be optimized.

In this program, front-wall solar cells were fabricated with glass/SnO_2/CdS window, where the CdS film is thin in order to maximize transmission and current. Wide bandgap absorber films (E_g = 1.75 eV) were grown by MBE and MOCVD techniques, which provide excellent control for tailoring the film composition and properties. CdZnTe films were grown by MBE and CdTe films were grown by both MBE and MOCVD techniques. All the as-grown films were characterized by several techniques such as surface photovoltage spectroscopy (SPV), Auger electron spectroscopy (AES), and X-ray photoelectron spectroscopy (XPS) for composition, bulk uniformity, thickness, film and interface quality. Front-wall type solar cells were fabricated in collaboration with AMETEK materials research laboratory using CdTe and CdZnTe polycrystalline absorber films. The effects of processing on ternary films were studied by AES and XPS measurements coupled with C-V and I-V-T measurements. Bias dependent spectral response and electrical measurements were used to test some models in order to identify and quantify

dominant loss mechanisms.

2. TECHNICAL PROGRESS

The technical progress has been divided into five sections. The efficiency limiting mechanisms in CdTe/CdS solar cells associated with CdS films are described in section 2.1. Section 2.2 describes the effects of $CdCl_2$ treatment on the electronic properties of CdTe/CdS heterojunction and CdTe/CdS cell performance. Section 2.3 deals with the contact induced instability in CdTe/CdS cell performance. Section 3.1 and 3.2 describe the growth and process optimization of CdZnTe polycrystalline films for high efficiency solar cells.

2.0 PROGRESS IN CdTe/CdS SOLAR CELLS

2.1 Efficiency Limiting Mechanisms Associated With CdS Films

2.1.1 Introduction

Polycrystalline thin film CdTe solar cells are one of the leading candidates for terrestrial solar cell applications. Theoretical calculations predict an efficiency of 27%, while the practically achievable efficiency is 22% (1,2). Recently, an efficiency of 14.3% has been reported on CdTe films grown by closed space sublimation technique (3). In order to obtain the practically achievable limit, many design modifications have been suggested like replacing the CdS window layer by CdZnS with a bandgap of 2.8 eV and the transparent conducting SnO_2 layer by ZnO to improve J_{sc} (1,2). However, a fundamental understanding of carrier loss and transport mechanisms at the CdTe/CdS

heterojunction is necessary to improve V_{oc} and fill factor values to the theoretical limit. In CdTe/CdS solar cells, interface states play a major role in limiting the V_{oc} (4,5). Several factors such as surface condition of CdS prior to CdTe growth, CdTe growth conditions, lattice mismatch, and the difference in thermal expansion coefficient between CdS and CdTe dictate the interface state density. A surface treatment on CdS/SnO_2/glass substrates prior to CdTe growth is one of the methods to reduce interface states. Every successful growth technique for fabricating CdTe/CdS solar cells today uses either a chemical or thermal treatment to clean the Cds surface prior to CdTe deposition.

Several investigators have shown that thermal treatment of CdS in H_2 atmosphere, modifies the electrical properties of CdS (6-8). It was observed earlier that annealing CdS films in H_2 atmosphere at 400° C prior to deposition of CdTe modifies the defects and transport mechanism of the CdTe/CdS heterojunction (9). However, the surface modifications of CdS due to thermal treatment and its effects on cell performance have not been studied in detail so far. A systematic study of pre-heat treatment of CdS prior to deposition of CdTe by MOCVD has been conducted. Both beneficial and undesirable effects of heat treatment on device performance are characterized and discussed.

2.1.2. Experimental

CdS film were deposited on commercially available SnO_2/glass substrates by spray pyrolysis at a substrate temperature of 450° C. Prior to CdTe deposition by MOCVD, CdS/SnO_2/glass substrates were annealed inside the reactor, in hydrogen atmosphere in the temperature range of 300 to 450° C for five minutes. The surface modifications of

CdS after each treatment were studied by Auger electron spectroscopy (AES) technique. A 3 KeV electron beam with a current of 1.0 uA was used for AES measurements. Sputter profiling was performed using a normally incident 2 KeV Ar ion beam at a current density of 28 uA/cm^2. Electrochemical I-V and C-V measurements were performed to determine carrier concentration and electrical characteristics of annealed CdS films using an automated electrochemical etching profiler. An electrolyte, composed of 0.2M NaOH and 0.1M EDTA, was used to form a Schottky barrier contact on the CdS surface for I-V and C-V measurements.

CdTe films were deposited on annealed CdS/SnO_2/glass substrates under the same conditions, at a substrate temperature of 300° C. Dimethylcadmium and diallyltellurium were used as Cd and Te sources, respectively. Front-wall n-i-p solar cells were fabricated with glass/SnO_2/CdS/CdTe/ZnTe/Ni structures. Dark and light I-V and capacitance-frequency (c-F) measurements were performed to monitor the device performance.

2.1.3. Results and Discussion

2.1.3.a. Effects of Preheat Treatment of CdS on MOCVD-grown CdTe/CdS Solar Cell Performance

C-V measurements indicated that annealing CdS films in hydrogen atmosphere at 450° C increased the doping concentration of CdS from ~2 × 10^{17} cm^{-3} to ~10^{18} cm^{-3}. Several investigators have shown that adsorption of oxygen in CdS films increases the grain boundary barrier height (6-8). The increase in grain boundary height reduces the mobility and carrier concentration. Oxygen in grain boundaries gives rise to electron traps

which reduce the carrier concentration by trapping electrons. Hydrogen annealing causes desorption of oxygen from grain boundaries which reduces the intergrain barrier height resulting an increase in carrier concentration and mobility. Annealing induced reduction of grain boundary states and their effects on device performance were studied by fabricating n-i-p cells on these substrates. Figure 2.1.1 shows the C-F data for cells fabricated on annealed substrates.

CdTe/CdS devices fabricated on unannealed substrates showed highest capacitance at all frequencies along with maximum dispersion in capacitance at lower frequencies compared to devices fabricated on annealed substrates. Hydrogen annealing not only reduced the absolute capacitance but also caused the capacitance to become frequency dependent. In general, at low frequencies interface states or extraneous states in the bandgap interact with voltage modulation, giving rise to increased capacitance (10). Thus, decrease in absolute capacitance and its frequency dependence after annealing suggests reduction of interface states. Similar behavior has been reported for $CuInSe_2$/CdS and closed space sublimation (CSS)-grown CdTe/CdS polycrystalline thin film solar cells (9,10). The effects of reduction in interface states due to annealing are also seen clearly in dark I-V measurements (figure 2.1.2), which show that CdTe/CdS diode behavior improves with increasing annealing temperature. In order to determine the variation in diode parameters quantitatively, a multivariable regression analysis was performed. The measured dark I-V data were fitted to a single exponential diode given by

$$I = I_o[\exp\{(q/AKT)(V-IR_s)\}-1] + (V-IR_s)/R_{sh}$$

where A is the diode ideality factor, R_s is the series resistance, I_o is the saturation current

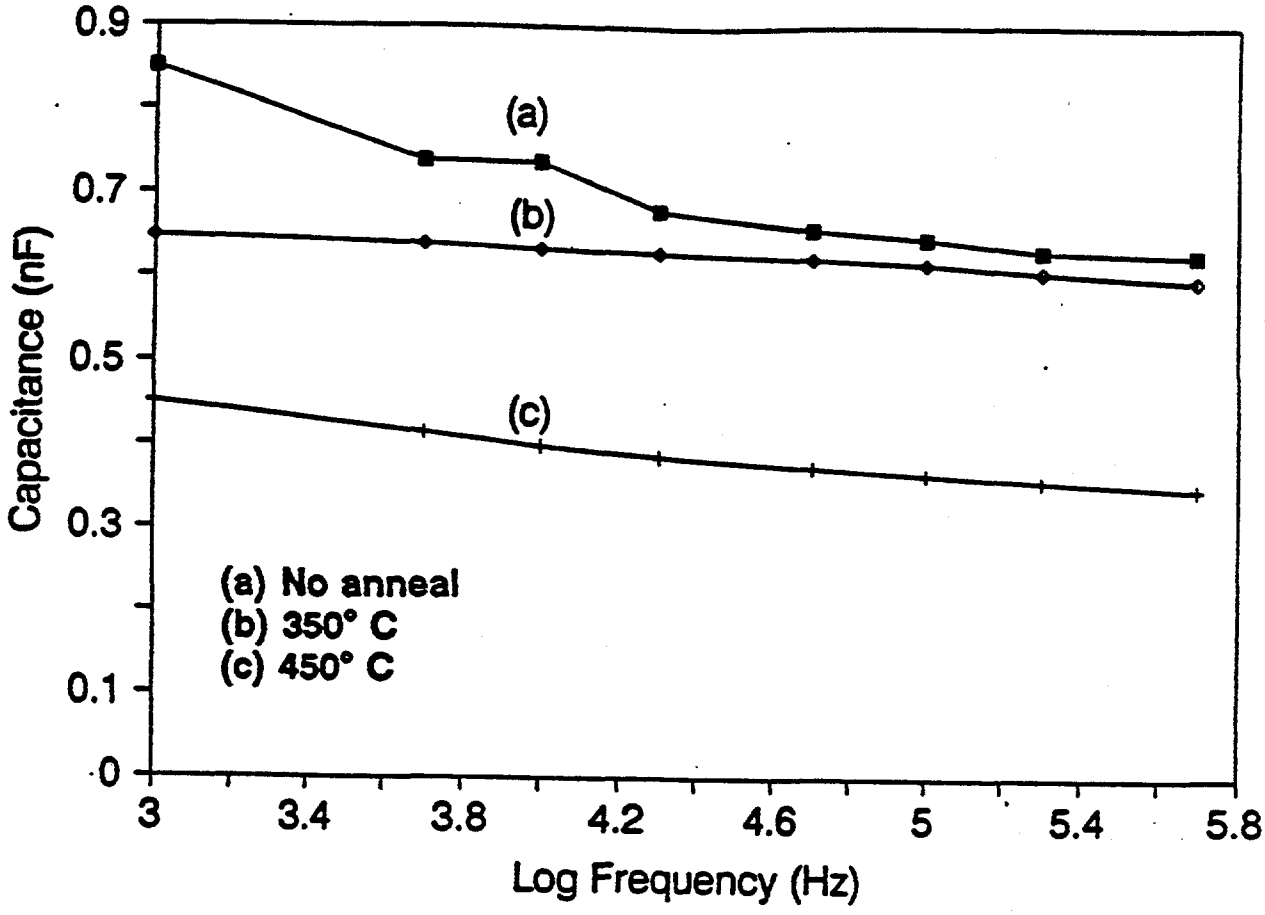


Figure 2.1.1 **Capacitance versus frequency measurements of CdTe/CdS devices fabricated on CdS/SnO_2/glass substrates for different annealing conditions a) unannealed, b) 350 C anneal, and c) 450 C anneal**

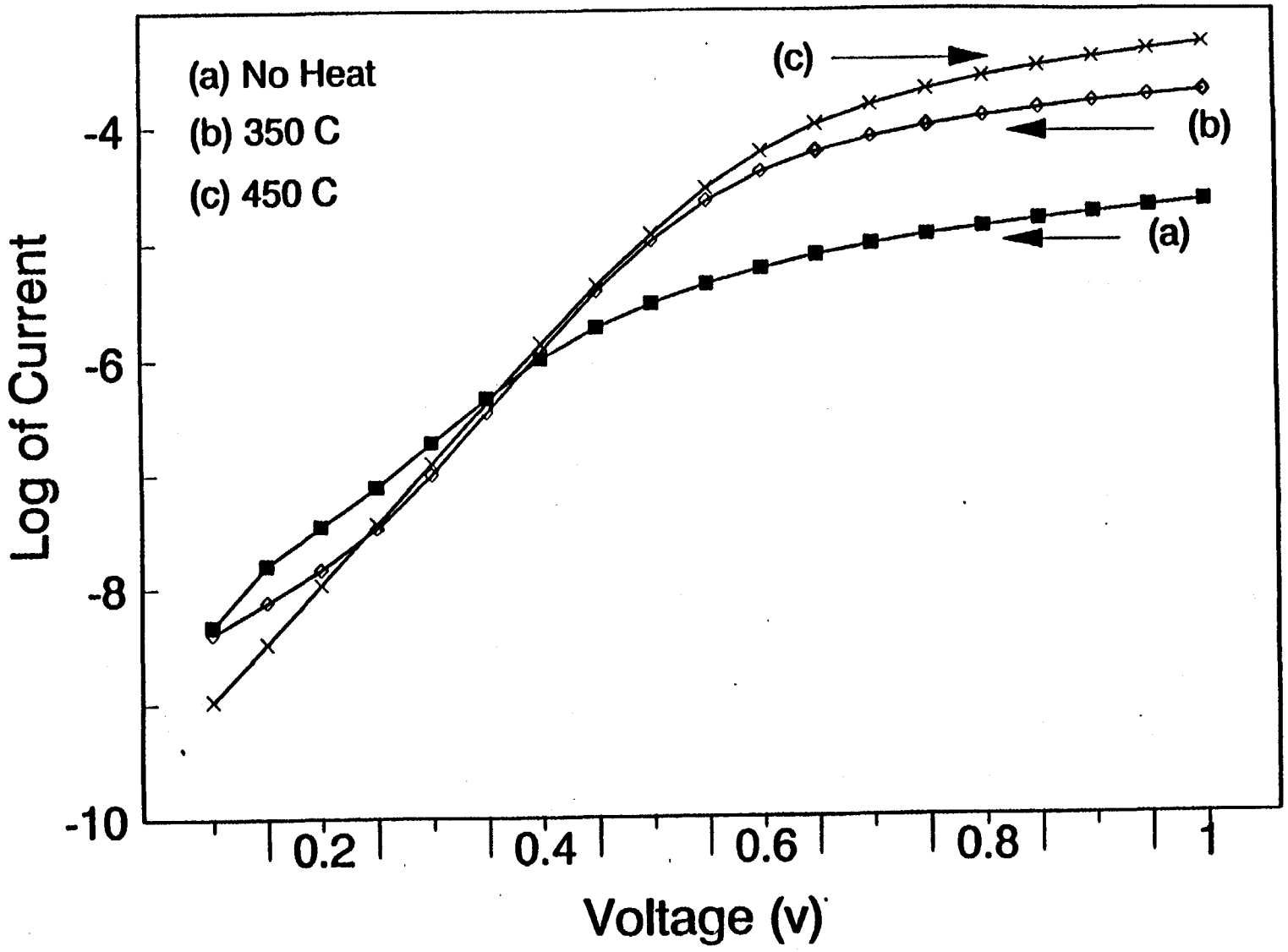


Figure 2.1.2 **Dark I-V data of CdTe/CdS solar cells fabricated on CdS/SnO_2/glass substrates annealed at different temperatures.**

density, and R_{sh} is the shunt resistance of the diode. The results of the analysis are given in table 2.1.1, which clearly show a decrease in I_o and series resistance with increasing annealing temperature. The reduction in series resistance can be attributed to the increased doping of CdS observed in C-V measurements. The improvement in I_o may be due to the reduction in interface states density. Furthermore, the diode ideality factor decreased from 2.1 to 1.5, suggesting a possible change in the transport mechanism across the CdTe/CdS interface. It has been shown earlier that in CdTe/CdS devices grown by CSS technique, H_2 annealing modifies the carrier transport from tunneling to interface recombination (9).

The improvement in CdTe/CdS cell performance upon heat treatment is also depicted in light I-V measurements shown in figure 2.1.3. Both open-circuit voltage and fill factor increased with heat treatment, increasing the efficiency of CdTe/CdS device from 5.8 to 8.1% (table 2.1.2).

However, the J_{sc} did not change appreciably after annealing which indicates that the increase in open circuit voltage is due to the decrease in I_o. In this study, the CdTe film thickness (1.5 um) and growth conditions were not optimized, therefore, only 8% efficiency was achieved. Nevertheless, the above results show a direct correlation between pre-heat treatments and cell performance. Using the guidelines of the above study for best pre-heat treatment and optimized CdTe thickness of 2.5 um, we were able to fabricate 9.7% efficient cell (11). In order to understand the source of these defects, XPS and AES measurements were performed on various CdS films before and after the preheat treatment. XPS data (figure 2.1.4) showed that the preheat treatment was able

Table 2.1.1 **Single diode parameter values of dark I-V data of CdTe/CdS devices fabricated on substrates annealed at different temperatures.**

Temperature C	A	I_o $X10^{-8}$ (A)	R_s Ohms	R_{sh} $X10^8$ Ohms
No anneal	2.14	8.9	20795	2.86
300	1.50	.35	1815	2.76
400	1.36	.063	1496	846
450	1.61	.008	748	2.44

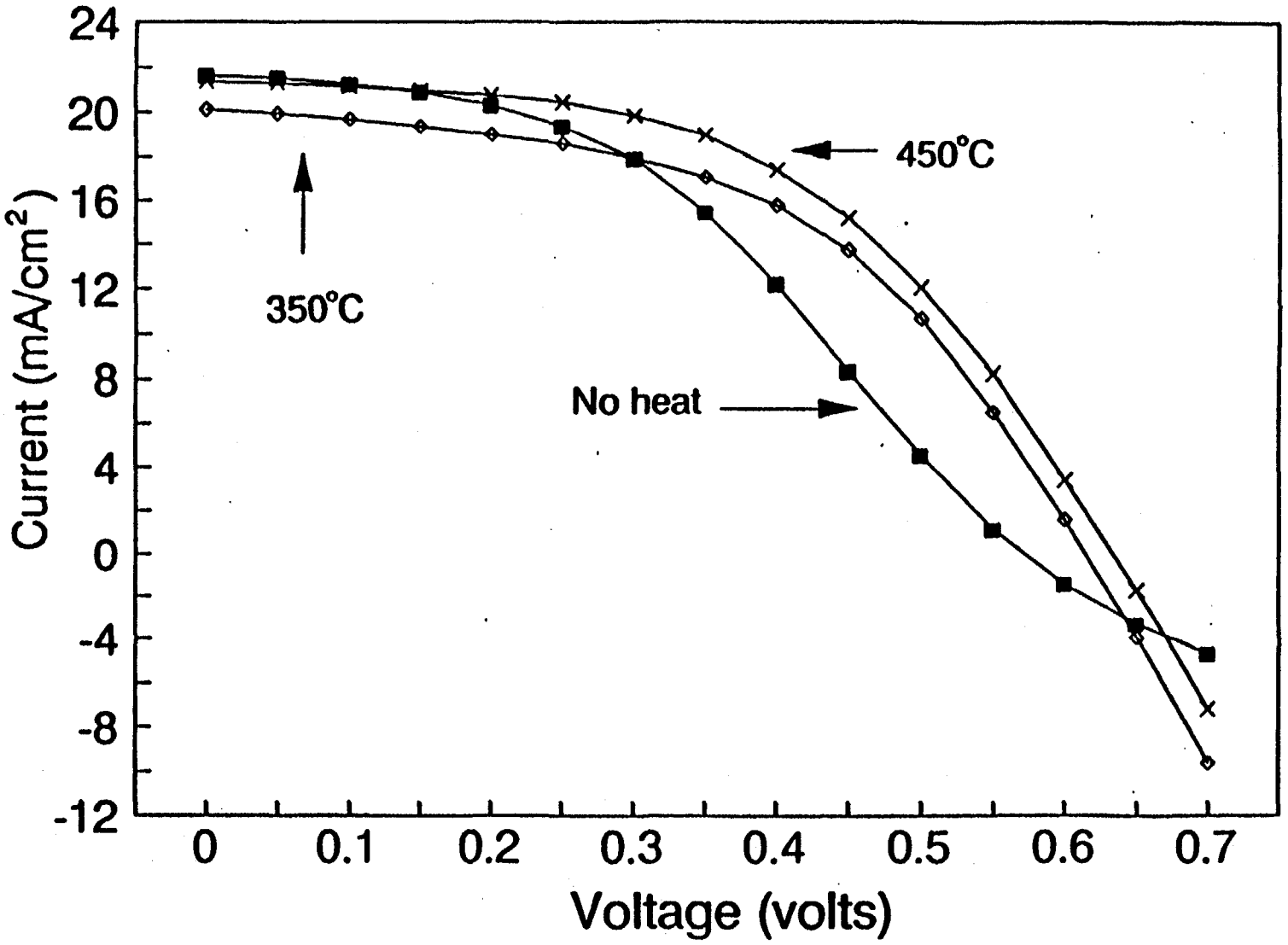


Figure 2.1.3 **Lighted I-V data of CdTe/CdS solar cells fabricated on CdS/SnO_2/glass substrates annealed at different temperatures.**

Table 2.1.2 **Light I-V data on CdTe/CdS cells prepared on CdS/SnO_2/glass substrates annealed at different temperatures.**

Anneal Temperature C	V_{oc} (mV)	J_{sc} (mA)cm^2	FF	Efficiency %
No anneal	600	20.9	.47	5.9
300	620	20.2	.53	6.6
350	630	20.2	.55	7.0
450	680	20.5	.56	7.9

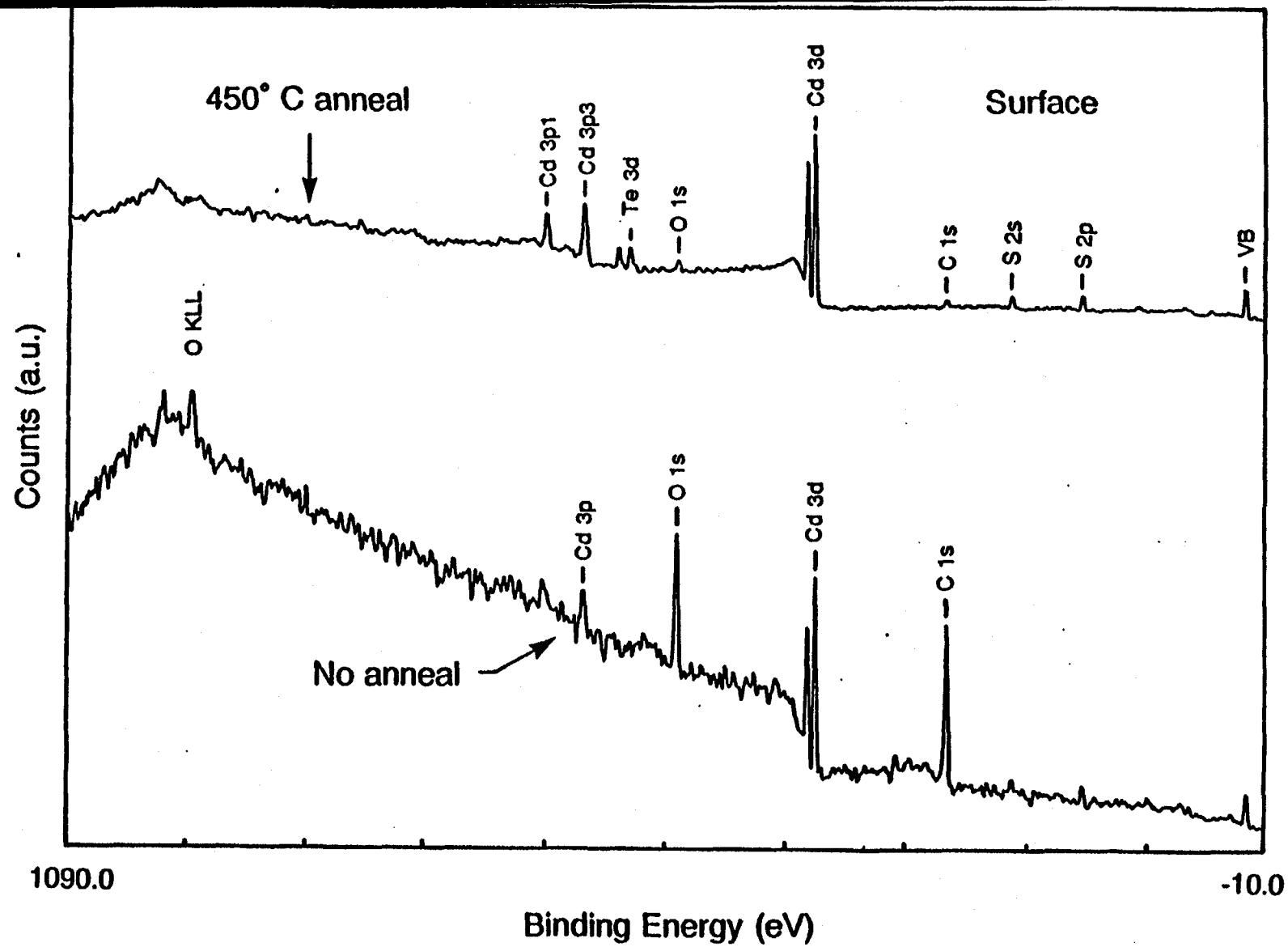


Figure 2.1.4 **XPS data on the surfaces of CdS substrates before and after annealing at 450° C in hydrogen atmosphere inside the MOCVD reactor.**

to remove significant amount of oxygen from the CdS surface. Since it is known that oxygen adsorbed on the surface of CdS gives rise to recombination centers (7), it is reasonable to state that oxygen induced defects on the CdS surface could be responsible for large number of interface states and poor performance of the untreated cells.

Although, the thermal cleaning of CdS/SnO_2/glass substrates improves the final device performance, it also introduces some undesirable effects on CdTe/CdS devices. Figure 2.1.5 shows a comparison of AES spectra of CdS/SnO_2/glass substrates before and after 450° C anneal.

The Cd/S ratio was found to be uniform and higher on the surface of the unannealed films compared to the bulk CdS. It is known that due to high vapor pressure and growth temperature (450° C) of CdS films, sulfur evaporates from CdS surface during deposition thus causing a higher Cd/S ratio on the surface (8). Also, the Cd/S ratio was found to be higher on the surface of CdS films annealed up to 400° C. However, in the case of substrates annealed at 450° C AES spectrum on CdS surface showed Cd depletion. Since CdS films were grown at a temperature of 450° C, it is possible to have evaporation of Cd from CdS. Also, for a particular annealing temperature, the surface of CdS had varying Cd/S ratios indicating a non-uniform composition (figure 2.1.6). This may have an adverse effect on large area devices, where uniformity is important.

The undesirable heat treatment effects described above significantly alter the I-V characteristics of electrochemical Schottky barrier formed on CdS film, as shown in figure 2.1.7. The forward bias I-V curve of the substrate without any heat treatment has a single slope indicating one dominant transport mechanism whereas, CdS films annealed at 450°

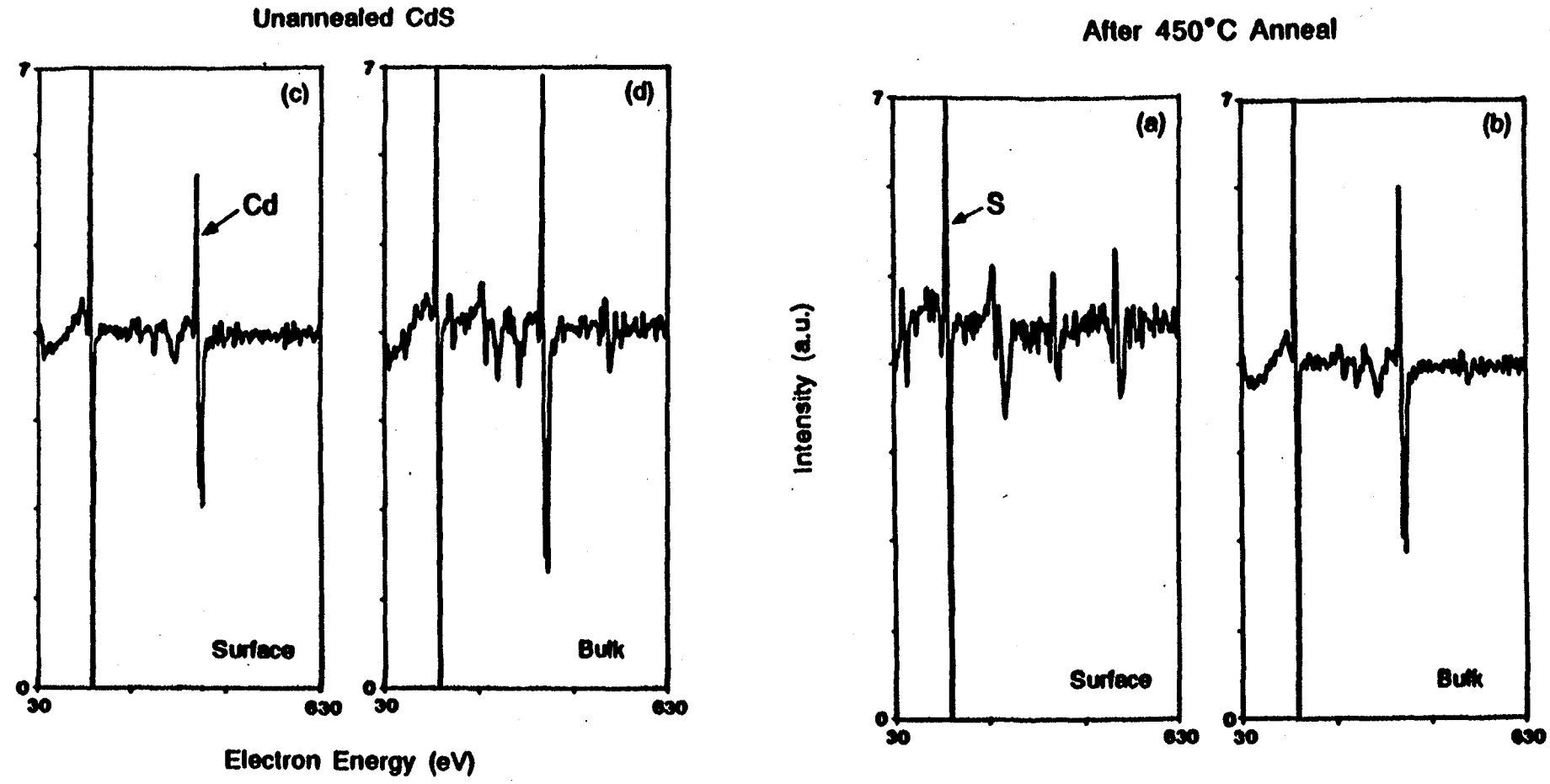


Figure 2.1.5 **Comparison of AES spectra of CdS/SnO_2/glass substrates before and after 450 C anneal taken at the surface and after 2 min sputtering.**

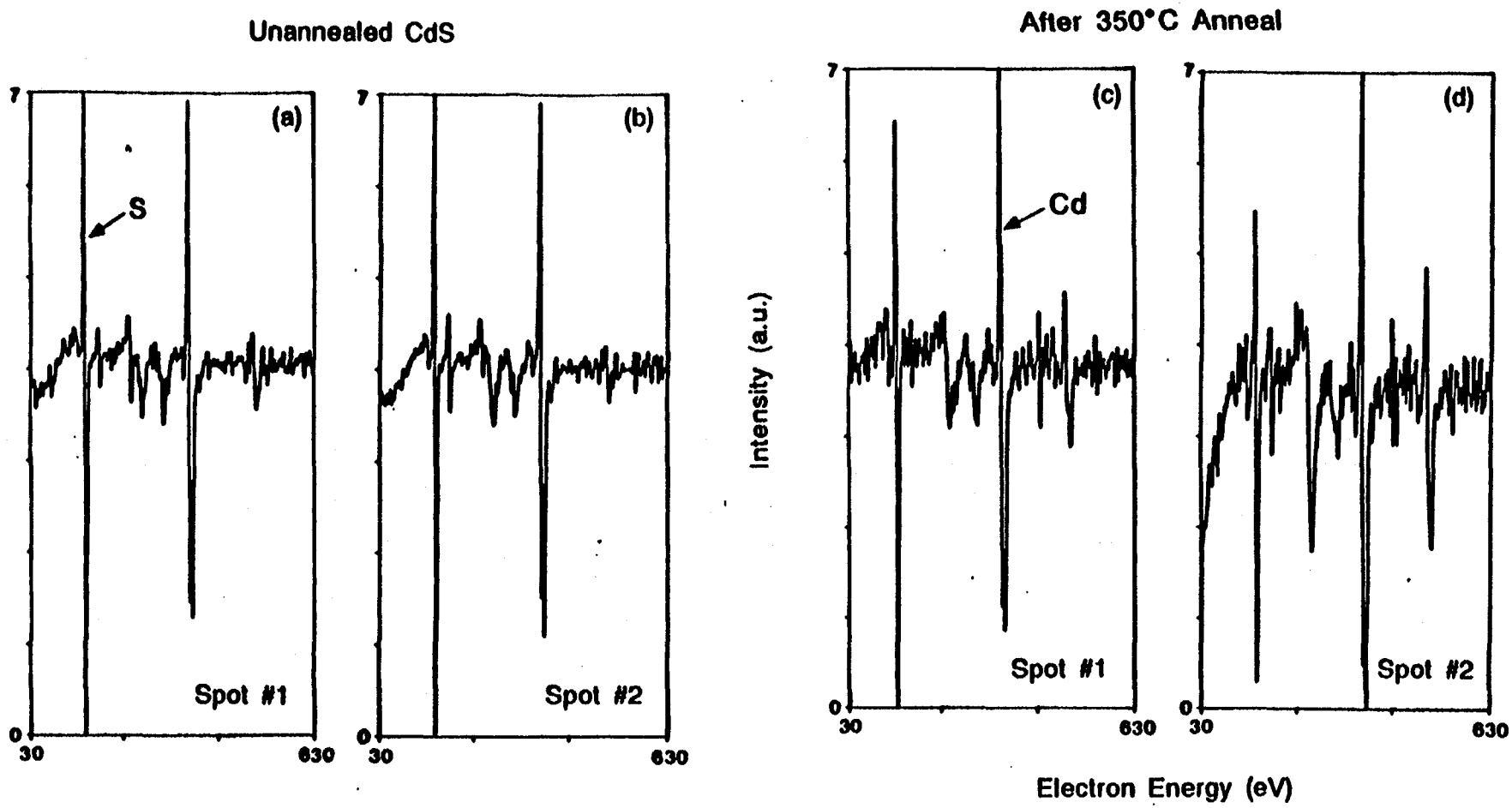


Figure 2.1.6 **The AES spectra taken at two different spots on CdS surface of unannealed and annealed substrates.**

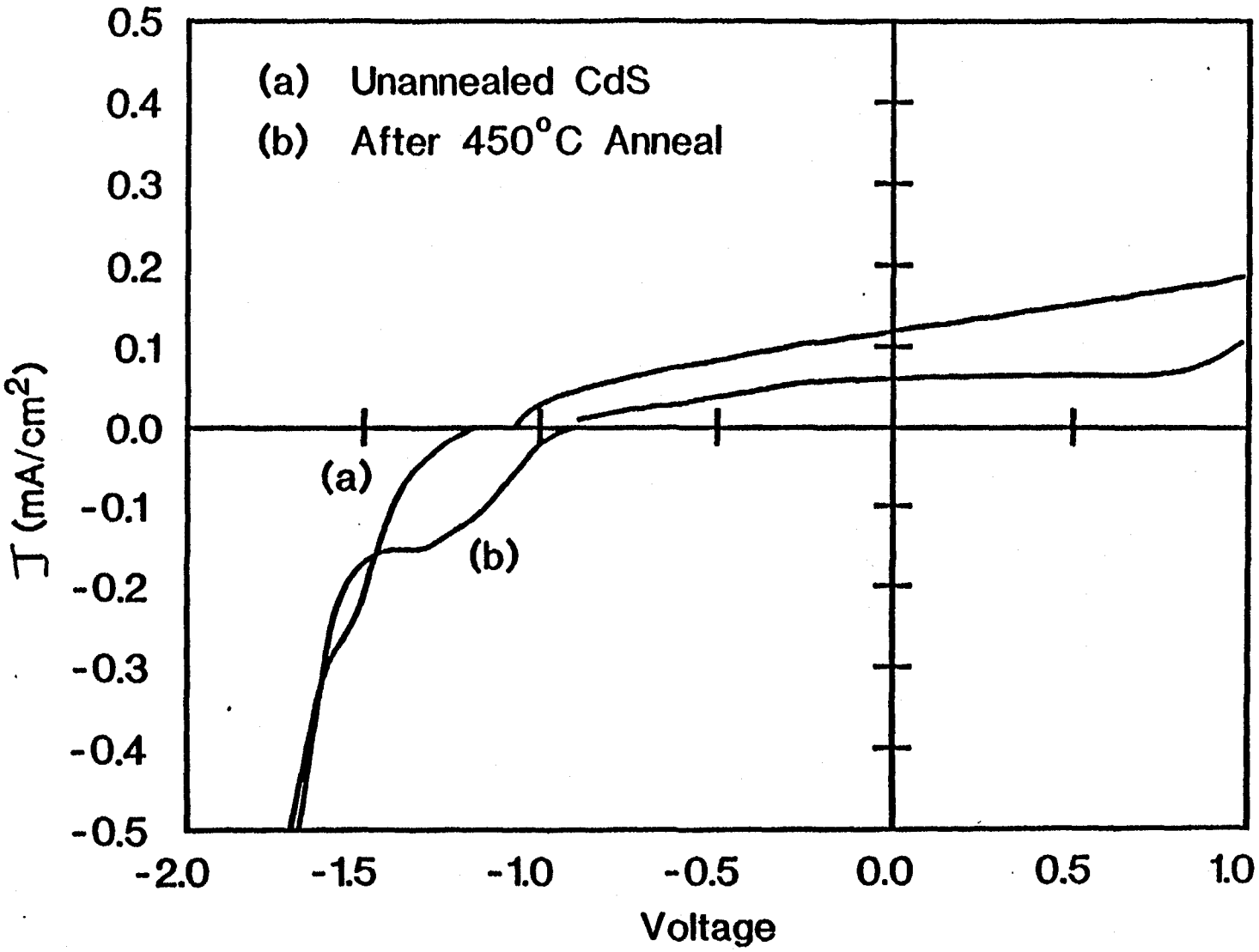
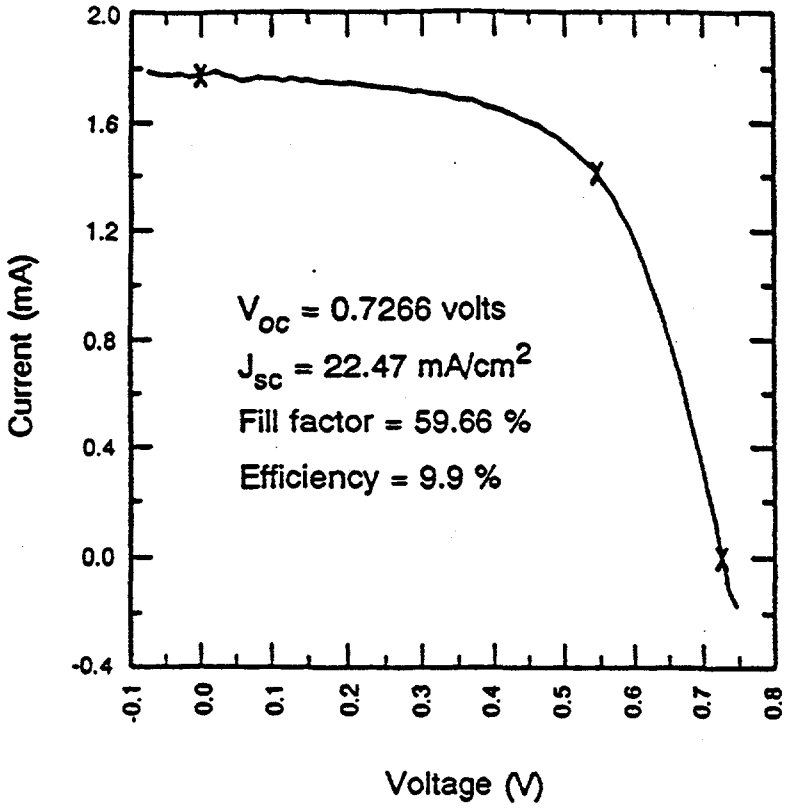


Figure 2.1.7 **Electrochemical I-V data of CdS/SnO_2/glass substrates before and after 450 C anneal.**

C show two different slopes. This suggests that the annealing-induced Cd depleted layer (figure 2.1.6) may have defects which provide an alternative current path at lower voltages which may degrade CdTe/CdS device performance by increasing diode current. In addition, some investigators have reported (12,13) that presence of a CdS layer with lower carrier concentration near the CdTe/CdS junction will reduce the open circuit voltage. This has been experimentally verified in $CuInSe_2$/CdS solar cells by growing an insulating layer of CdS near the heterojunction. Hence, even though devices made on the annealed substrates gave better efficiency, annealing-induced undesirable effects may limit further improvement in efficiency for a given cell design unless fabrication process and design are optimized.

In order to understand the efficiency limiting mechanisms in CdTe cells light I-V and bias dependent spectral response measurements were done on both p-n and p-i-n device structures. Figures 2.1.8-2.1.9 show the comparison of light I-V and bias dependent spectral response of 9.7% p-i-n and 9.9% p-n CdTe cells. The cell parameters are similar, and in both cases the spectral response is fairly uniform with sharp cut-off indicating that bulk recombination does not play a major role in the collection efficiency in either cell. However, the spectral response of both cells show a strong wavelength independent bias dependence, suggesting that defects at the CdS/CdTe interface are limiting the performance of these cells by making the interface recombination velocity sensitive to applied bias (11).

The fact that the 10% efficient cells, subjected to this 450° C/15 min. preheat treatment, showed a strong bias dependence in the spectral response, suggests that



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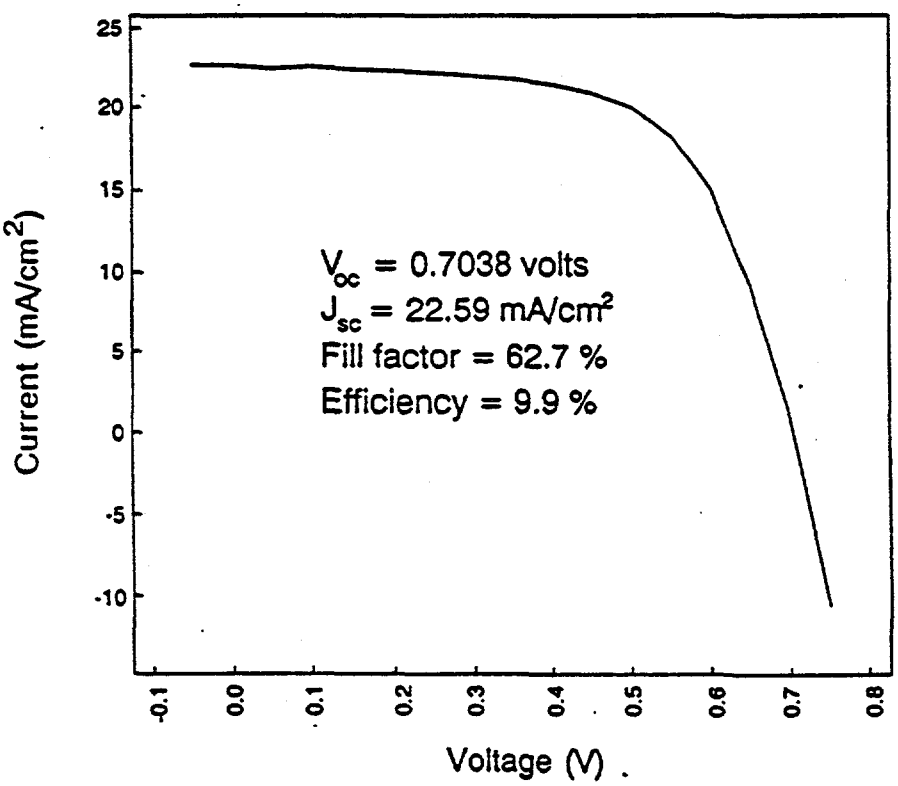

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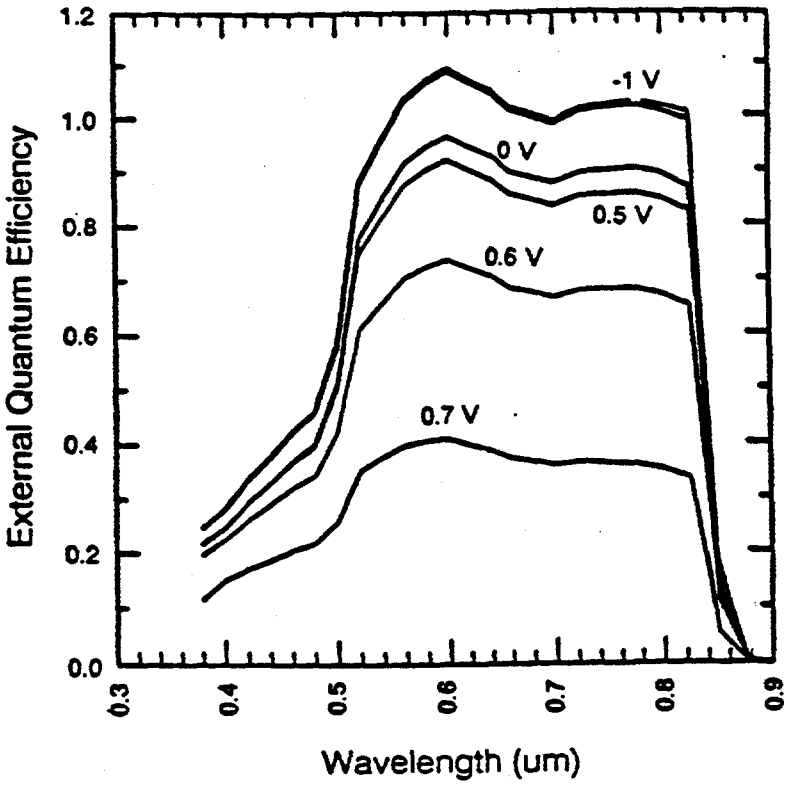
Figure 2.1.8 **Comparison of light I-V data of 9.7% efficient p-i-n and 9.9% p-n MOCVD-grown CdTe cells.**



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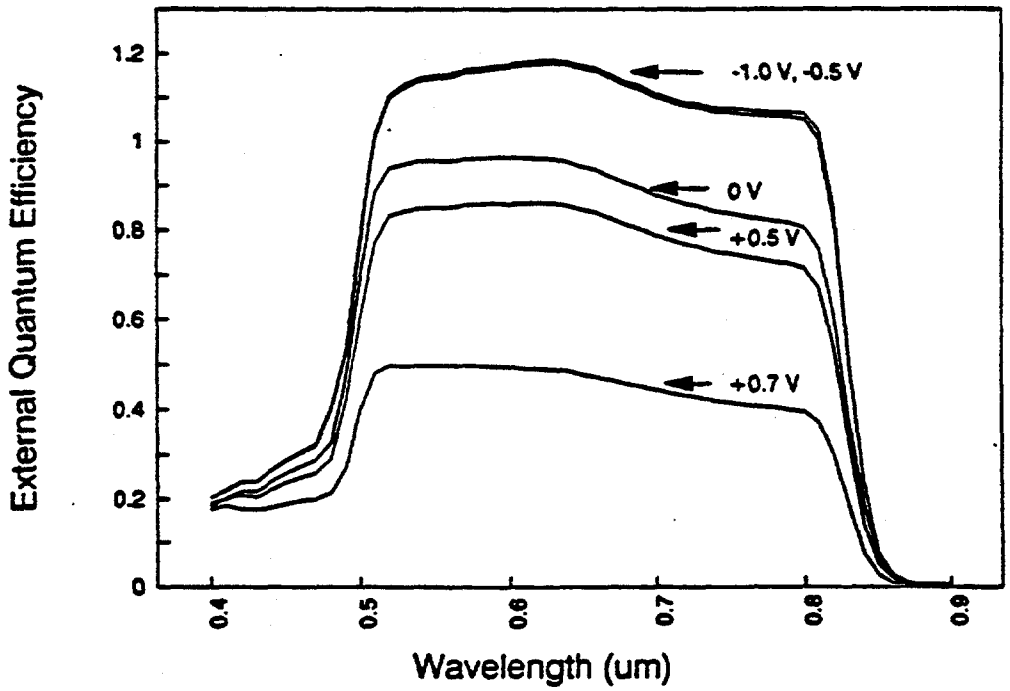

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Figure 2.1.9 **Comparison of bias dependent spectral response data of 9.7% p-i-n and 9.9% p-n CdTe cells.**

preheat treatment is necessary but not sufficient to eliminate the detrimental effects of interface recombination. However, depth resolved AES measurements made on the annealed CdS film showed that 450° C heat treatment in hydrogen causes the CdS surface to become Cd-deficient (Cd/S < 1) in addition to removing oxygen. It is well known that Cd deficiency in CdS gives rise to an acceptor type defect level which is situated at 0.26 eV above valence band (14). This can produce a high resistive CdS surface layer, which is known to reduce V_{oc} and fill factor in $CuInSe_2$/CdS solar cells (12). A similar mechanism is possible in CdTe/CdS cells which may in part be responsible for limiting the efficiency to 10%.

In order to estimate the maximum attainable efficiency due to the improved quality of the CdTe/CdS interface, model calculations were performed by using a collection function approach. This was done by first calculating the collection function (ratio of zero bias quantum efficiency to quantum efficiency at different bias voltages) as a function of applied bias using bias dependent spectral response data (figure 2.1.9). The loss in V_{oc} and fill factor due to the collection function were calculated according to (11,12):

$$\Delta V_{oc} = (AKT/q)\ (\ln^{n}(V_{oc})$$

$$\Delta FF = (V_{mp}/V_{oc})(1-^{n}(V_{mp})$$

For 9.7 % efficient MOCVD CdTe cell, the calculated loss in V_{oc} and fill factor were 0.05 V and 0.12, respectively. In addition, reverse bias spectral response measurements indicate (figure 2.1.9) an additional loss of at least 10% (1.5 mA/cm^2) in J_{sc} due to interface recombination. If these losses can be eliminated by improving the interface quality then we project that cell efficiencies of 13.5% can be achieved from the MOCVD

CdTe cells.

Further improvement in efficiency can be achieved by eliminating the loss due to absorption of high energy photons in the thick (1500 Å) CdS window layer. The 10% cells had ~1500 Å of CdS on SnO_2, and the estimated loss in J_{sc} due to absorption is 4 mA/cm^2 (2). This results in an additional loss of 0.02 volts and 0.08 in V_{oc} and fill factor, respectively. Thus, by eliminating this loss mechanism along with the interface recombination, it is possible to achieve 18% efficient CdTe cells. Attempts are being made to deposit thin CdS films by the chemical immersion method (15). We have successfully grown CdS films in the thickness range of 400 to 1400 Å by controlling the immersion time and have found an appreciable improvement in the transmission of 400 Å CdS film in the short wavelength range. Thus a combination of optimum preheat treatment, proper Cd/Te ratio, and thin CdS films should yield a significant improvement in the MOCVD CdTe cell efficiency.

Attempts were made to improve the interface quality by (a) controlling CdTe film deposition conditions, (b) adjusting CdTe stoichiometry and (c) varying the CdS thickness.

Since Cd deficiency in CdS is a potential source of interface defects, one way of reducing such defects is to grow CdTe in Cd-rich conditions. This was attempted by gradually increasing the Cd/Te ratio in the vapor from 0.4 to 4.0. The 10% cells were grown with Cd/Te ratio of 0.4, in a Cd deficient ambient. The SPV responses of these films were measured with light incident on the CdTe film side. Figure 2.2.10 shows electrochemical SPV spectra of CdTe films grown on CdS with various Cd/Te ratios. In

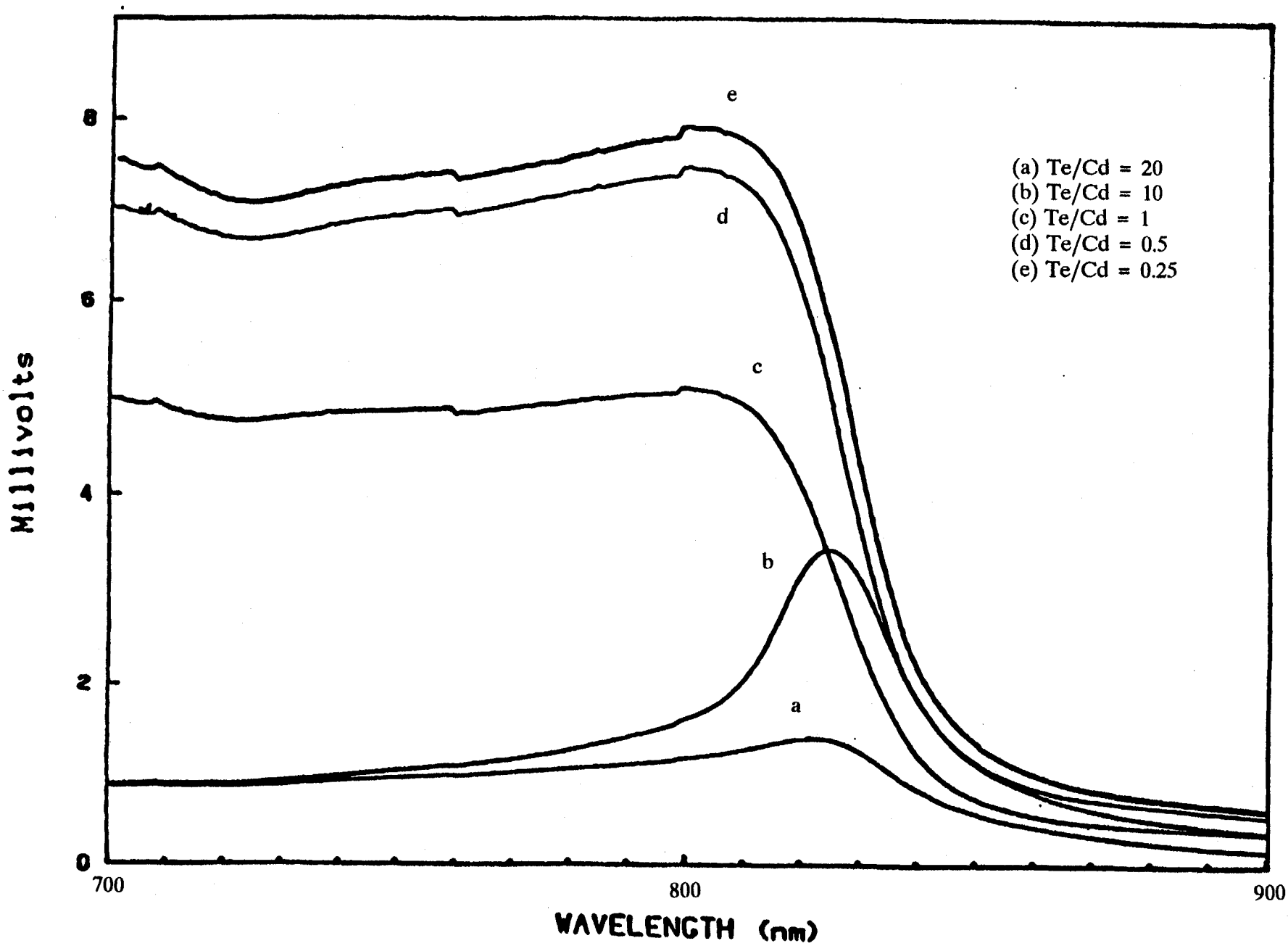


Figure 2.1.10 **SPV spectra of CdTe films grown by MOCVD on CdS/SnO_2/glass substrates with different Cd/Te ratios.**

order to separate the electrolyte-CdTe junction contribution from CdTe/CdS interface contribution only the SPV response in the long wavelength region is shown in the figure. It is interesting to note that the Cd-rich films show a significant increase in the surface photovoltage suggesting that the excess Cd in the CdTe film is eliminating the Cd deficiency at the CdS/CdTe interface. Since SPV response is an indicator of V_{oc}, it is possible to expect higher V_{oc} on films grown under Cd-rich condition compared to 10.9% efficient CdTe cells grown in Te-rich ambient. The films are now being subjected to the standard post deposition 400° C/30 min. air anneal for cell fabrication. If the higher SPV response is maintained throughout the cell processing, then we should be able to attain a higher V_{oc} and efficiency compared to the 10% efficient cells.

Also, the SPV spectra indicate, figure 2.1.11, that the films grown under Te-rich conditions have slightly lower bandgap compared to the films grown under Cd-rich conditions. The reduction of CdTe bandgap in CdTe/CdS structures was observed by several investigators (16,17) after the post growth heat treatment and attributed to interdiffusion between CdS and CdTe films. However, our data clearly show that the bandgap reduction in Te-rich films takes place during the MOCVD growth of the CdTe film, prior to the post-growth $CdCl_2$ heat treatment. We propose a model for the bandgap reduction based on sulfur diffusion. The sulfur diffusion gives rise to defect states near the bandedge and decrease the bandgap. Growth of CdTe films under Cd-rich conditions reduces the Cd vacancies and retards the sulfur diffusion into the CdTe films. This reduces the defect states near the bandedge and restores the bandgap of CdTe. Even though we were able to reduce the interdiffusion by growing the CdTe under Cd-rich

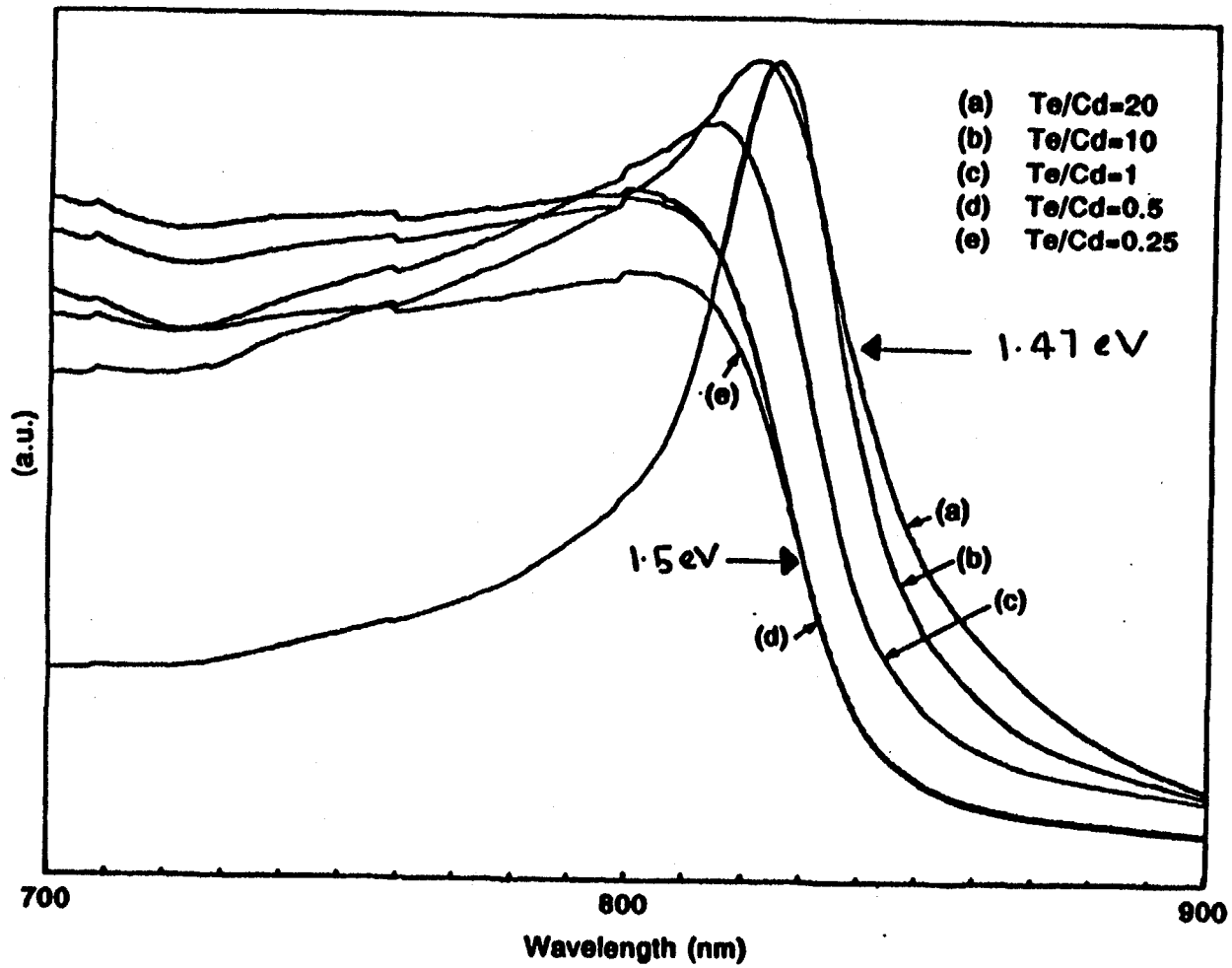


Figure 2.1.11 SPV spectra of CdTe/CdS structures grown under different DIPTe/DMCd input gas ratios. East spectrum is normalized to its maximum peak value to determine the bandgap.

conditions, the 400° C heat treatment used during the cell fabrication triggered the interdiffusion and caused a bandgap reduction similar to what was found in films grown under Te-rich conditions. Since 400° C heat treatment after the $CdCl_2$ dip is a necessary step for efficient cell fabrication, it may not be possible to avoid the interdiffusion in the current devices unless the cell fabrication procedure is altered. Modified heat treatment such as rapid thermal annealing and/or addition of an interlayer may prevent the interdiffusion to reduce the defects at the interface and restore the bandgap. It is important to recognize that the magnitude of the bandgap shift does not limit the efficiency but the interdiffusion induced defects responsible for the bandgap shift may degrade the cell performance.

Another efficiency limiting mechanism is related to the CdS thickness. Figure 2.1.12 shows a comparison of the light I-V data for the two CdTe/CdS cells fabricated with thick (3000 Å) and thin (1000 Å) CdS films. As expected, the thinner CdS film (1000 Å) increased the efficiency to 10.3% from 9.7% by increasing the J_{sc} to 24.19 mA/cm^2. Further reduction in the thickness of the CdS films to 600 Å resulted in a net decrease in the efficiency (8.9%) primarily due to the reduction in V_{oc} (680 mV) and fill factor (0.55) along with some decrease in J_{sc} (23.47 mA/cm^2). Pin-holes in the CdS films can cause low shunt resistance which will reduce V_{oc} and fill factor. In addition, CdS films were deposited on the textured SnO_2 films which can aggravate the pin hole problem in the CdS films. On the other hand, increasing the CdS thickness to 3000 Å increased the V_{oc} to 740 mV and, as expected, reduced the J_{sc} to 22.10 mA/cm^2. However, the cell efficiency increased to 10.9% which happens to be the highest efficiency for MOCVD-

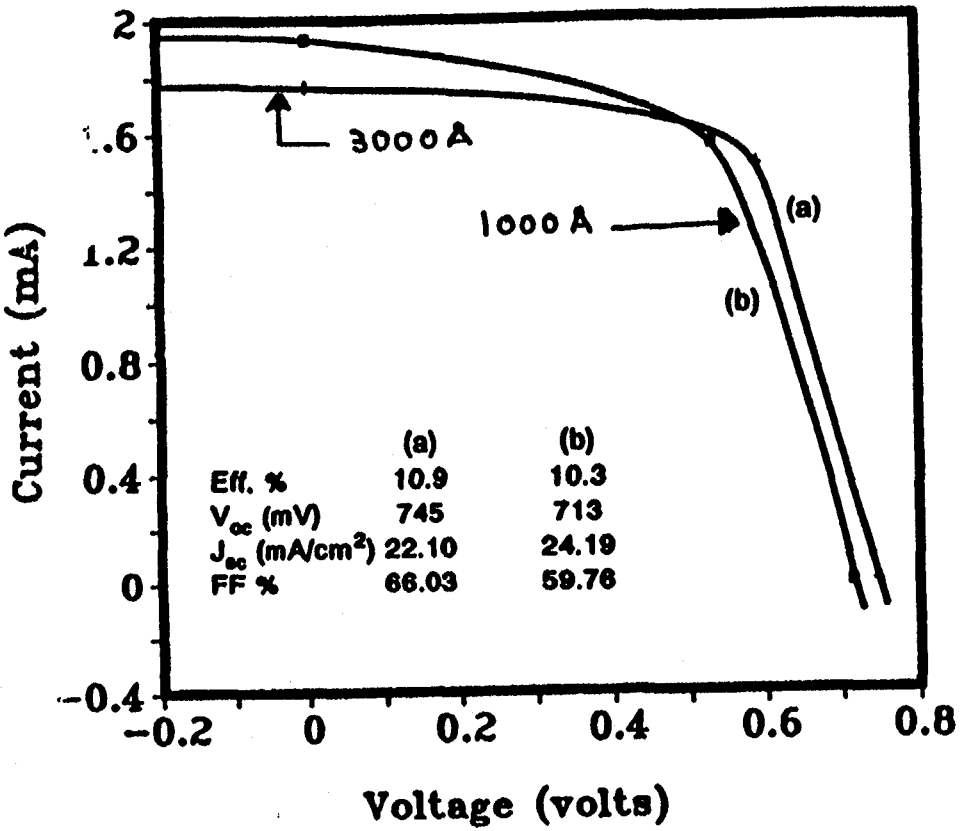


Figure 2.1.12 Comparison of light I-V data of CdTe/CdS cells fabricated on, (a) 3000 A and (b) 1000 Athick CdS films.

grown CdTe/CdS solar cell to date. The advantage of thinner CdS film is clear from the spectral response data in figure 2.1.13. The short wavelength response is higher for the cell with thinner CdS films because more high energy photons are able to reach the CdTe film. These results suggest that to improve the CdTe cell efficiency further, the CdS layer thickness should be optimized or replaced by a combination of thin CdS and wider bandgap material such as ZnO.

2.2 The Effects of $CdCl_2$ on the Electronic Properties of Molecular Beam Epitaxially Grown CdTe/CdS Heterojunction Solar Cells

2.2.1. Introduction

Solar cells based on CdTe are one of the leading candidates for low-cost conversion of solar energy due to their near optimum bandgap (1.45 eV), high absorption coefficient, and manufacturability. High efficiency (~ > 10%) thin film polycrystalline CdTe/CdS solar cells have been fabricated by electrodeposition (1), physical vapor deposition (2), close-spaced vapor transport (CSVT) (3), sintering (4), metal organic chemical vapor deposition (MOCVD) (5), and molecular beam epitaxy (MBE) (5). To obtain high efficiency in all of these approaches, it is necessary to have CdTe grain sizes of ~ 1 um or greater to avoid significant bulk recombination, large interface state density, and high sheet resistance. A commonly used procedure to enhance the grain size and densify the CdTe film is the introduction of an annealing (or sintering) aid such as $CdCl_2$ either during or after CdTe film growth (6-8). The influence of the $CdCl_2$ treatment on CdTe microstructure and solar cell performance has been previously investigated for

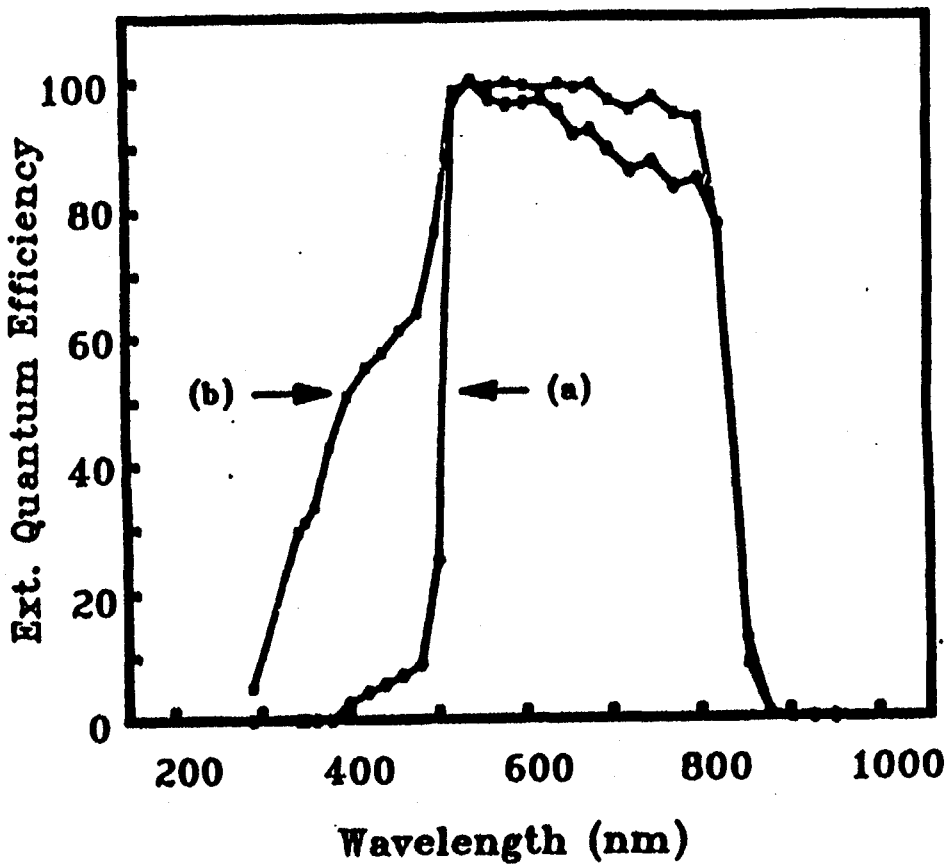


Figure 2.1.13 Comparison of spectral response data of, (a) 10.9% and (b) 10.3% efficient CdTe/CdS cells.

CdTe films prepared by a high temperature (T > 600 C) sintering process (6-8) which requires incorporation of $CdCl_2$ in the CdTe slurry prior to CdTe film formation. This method has resulted in CdTe cell efficiencies in excess of 10%. However, polycrystalline CdTe films prepared by techniques such as electrodeposition, physical vapor deposition, MBE and MOCVD require a post-deposition heat treatment in the presence of $CdCl_2$ to obtain high efficiency (9). To date, the observed beneficial effects of the $CdCl_2$ treatment on device characteristics and performance are at best qualitatively understood. In order to improve present-day CdTe/CdS cell efficiency beyond 13-14%, it is necessary to quantify and improve the fundamental understanding of process-induced effects on the bulk and interface properties of these cells.

In this section, MBE-grown polycrystalline CdTe/CdS solar cells are investigated to quantify the mechanisms responsible for improved cell performance due to the $CdCl_2$ treatment and reveal process-induced defects which may dictate the device characteristics after the $CdCl_2$ treatment. First, microstructural changes in the CdTe films due to post-deposition annealing with and without the $CdCl_2$ dip are investigated by scanning electron microscopy (SEM). Second, electrochemical surface photovoltage (SPV) and bias-dependent spectral response measurements are used to estimate the improvement in bulk and interface quality of the CdTe/CdS cells due to the $CdCl_2$ treatment. Third, the dominant current transport mechanisms in CdTe/CdS cells processed with and without the $CdCl_2$ treatment are studied by current density-voltage-temperature (J-V-T) analysis. Finally, Deep Level Transient Spectroscopy (DLTS) measurements are performed to identify traps which may dominate the current transport and limit the $CdCl_2$-treated

CdTe/CdS cell performance. Attempts are made to correlate transport mechanisms and traps within the CdTe cells to film microstructure, SPV and spectral response, and solar cell performance in order to provide guidelines for achieving higher efficiencies.

2.2.2. Experimental Techniques

A. CdTe Growth and Cell Processing

Polycrystalline CdTe films were grown to a thickness of 2 um by MBE on n-type CdS/SnO_2/glass substrates suitable for solar cell applications. (10) Prior to CdTe deposition, the surface doping density of the CdS was found to be $5x10^{16}$ cm^{-3} by electrochemical C-V measurements. After the CdTe film deposition, CdTe/CdS structures were dipped in a saturated $CdCl_2$:CH_3OH solution and then annealed in air at 400 C for 35 minutes. (5,9) Selected samples from the same growth run were annealed in air at 400 C for 35 minutes without the $CdCl_2$ solution to distinguish the effects of $CdCl_2$ on CdTe material and device properties. Cell fabrication was completed by etching the annealed CdTe surface in ~ 0.1% Br_2:CH_3OH, to remove residual surface oxides, followed by a DI water rinse and blow dry in N_2. Ohmic back contacts were formed on the etched CdTe surface by evaporating 150 nm of Cu-doped ZnTe capped with 200 nm of Ni. (5)

B. Microstructural Studies

The grain size of the as-grown and processed CdTe/CdS structures was determined by SEM. A beam voltage of 15 KV was used. To prevent sample charging effects, the CdTe

surfaces were coated with 10 nm of gold.

C. Electrochemical Surface Photovoltage and Spectral Response Measurements

Process-induced effects on bulk and junction quality were monitored by electrochemical SPV measurements, using the Polaron PN4200 electrochemical profiler with the PN4250 photovoltage spectroscopy accessory. The CdTe/CdS/SnO_2/glass structures in the as-grown state, after air anneal, and after the $CdCl_2$ dip followed by air anneal were analyzed in detail. A 0.2M NaOH + EDTA (ethylenediaminetetraacetic acid) solution was used to form an electrochemical Schottky barrier to the CdTe surface and ohmic contact was made to the underlying SnO_2 with Indium. The samples were illuminated from the CdTe side, through the electrolyte, by chopped light in the wavelength range of 700 -900 nm and the resulting photovoltage was measured under open-circuit conditions to avoid etching of the CdTe film by the electrolyte. The net open-circuit SPV signal at each wavelength is the difference between the internal photovoltages generated at the surface barrier and CdTe/CdS heterojunction. (11) To accurately compare material and junction quality of different CdTe/CdS samples, it is necessary for the CdTe film thicknesses and doping to be identical to insure that the same carrier generation profile is seen by the collecting junctions in all of the samples. Our SPV setup uses low illumination intensity such that the SPV magnitude is much less than kT. In this case, it has been shown that the photovoltage generated at the CdTe/CdS heterojunction, ignoring the presence of the electrolyte/CdTe surface barrier for now, can be approximated as (11,12)

$$SPV(\lambda) = V_{oc}(\lambda) = [nkT/q]ln(J_{PH}/J_0 + 1) \approx [nkT/q][J_{PH}/J_o] = [nkT/J_o]F(\lambda)R(\lambda) \quad (1)$$

where n is the heterojunction ideality factor, J_o is the "effective" junction leakage current

density, $F(\lambda)$ is the photon flux absorbed in the quasi-neutral CdTe bulk, and $R(\lambda)$ is the spectral response function which is comprised of contributions from the quasi-neutral and depletion regions of both the CdTe and CdS and reflects bulk material quality. (12) Note that the contributions from the CdS layer to $R(\lambda)$ can be ignored since the minimum wavelength (maximum energy) of the photons incident on the CdTe surface was chosen to be 700 nm (1.77 eV) which will not be absorbed by the 2.42 eV bandgap CdS layer. Hence the magnitude of the SPV signal is proportional to both the CdTe/CdS junction quality, through J_o and n, and CdTe material quality through $R(\lambda)$. The final SPV spectrum is normalized to a calibrated photodiode to eliminate flux variations and the spectrometer response. To support the results from the above SPV analysis, bias-dependent spectral response measurements were performed on completed CdTe/CdS cells processed with and without $CdCl_2$. A.C. photocurrent measurements were made with O V d.c. and -0.5 V d.c. reverse bias applied across the device.

D. Dark J-V-T and Light J-V Measurements

Dark J-V-T measurements were performed to determine the current transport mechanisms in CdTe/CdS devices fabricated with and without the $CdCl_2$ treatment. J-V data were measured in the temperature range of 180 - 320 K in 10 K increments using an automated J-V-T setup. The J-V characteristic at each temperature was fitted to a parallel double diode equivalent circuit model with shunt resistance, R_s, described by

$$J = J_1 + J_2 + (V - JR_s)/R_{sh} \quad (2)$$

where

$$J_1 = J_{01}[exp[(q/A_1kT)(V - JR_s)] - 1] \quad (3)$$

and

$$J_2 = J_{02}[exp[(q/A_2kT)(V - JR_s)] - 1] \quad (4)$$

A multivariable regression analysis was used to fit the data and obtain J_{01}, J_{02}, A_1, A_2, R_s, and R_{sh} with less than 5% error in the fit over the entire voltage range. The temperature dependence of these parameters was used to determine current transport mechanisms in each device. Solar cell data were determined by lighted J-V measurements taken at 300 K under 100 mW/cm^2 AM1.5 conditions.

E. Deep Level Transient Spectroscopy (DLTS) Measurements

DLTS measurements were performed on Ni/ZnTe/CdTe/CdS/SnO_2/glass structures annealed with and without $CdCl_2$ to identify traps within the CdTe depletion. DLTS data were taken using an automated DLTS spectrometer in a lock-in amplifier type arrangement. The output signal was integrated and analyzed using five different weighing functions from 4 msec. to 64 msec. A pulse width of 8 ms. was necessary to saturate the detectable traps. Since the CdTe doping concentration ($5x10^{15}$ cm^{-3}, as determined by C-V measurements) is much less than that of the CdS, only the CdTe depletion region is probed. A steady reverse bias of -400 mV was used and a pulse of + 300 mV was applied to scan the CdTe depletion region. Spatial trap distributions were measured by varying the reverse steady bias from -400 mV to -100 mV, but keeping the sum of the

reverse steady bias and the pulse height constant at - 100 mV. In this way, the edge of the depletion region is stepped toward the CdTe/CdS interface as the steady reverse bias is decreased to provide a spatial trap profile in the CdTe depletion. The temperature of each device is monitored by a thermocouple mounted directly on a glass slide of identical thickness to the glass substrate of the CdTe/CdS device which was situated adjacent to the device under test. Trap activation energies and cross-sections were determined from the $\log(T^2/e_m)$ vs. 1000/T Arrhenius plot. The trap emission rate for majority carrier holes in the CdTe, e_{mp}, is given by

$$e_{mp} = N_v \sigma_p v_{th} exp[(E_v - E_T)/kT] \quad (5)$$

where the terms in eq. (5) have their usual meanings. (13)

F. Photoluminescence (PL) Measurements

PL measurements were done on the finished devices which were treated with different concentrations of $CdCl_2$ solution. PL measurements were done at a temperature of 15K using 514 nm line of argon laser as an excitation source and GaAs photomultiplier tube as a detector. A SPEX 1404 double spectrometer was used to collect the luminescence spectrum.

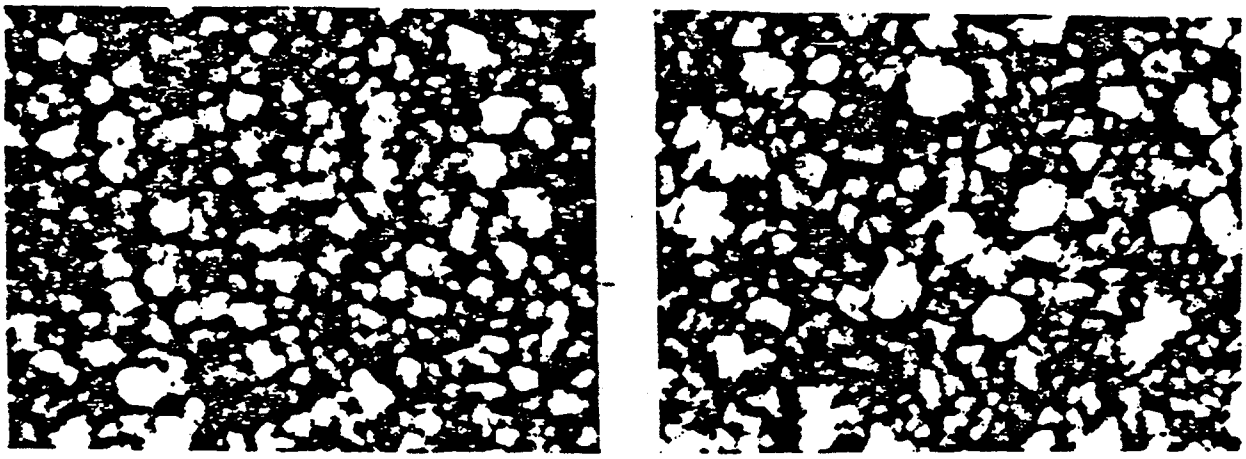
2.2.3. Results and Discussion

A. Effects of $CdCl_2$ Treatment on MBE-grown Polycrystalline CdTe Films and Solar Cells

The $CdCl_2$ dip prior to post-deposition annealing of small grain CdTe films grown by electrodeposition and physical vapor deposition has been previously shown to be necessary for grain growth and cell efficiencies in excess of 10%. (2,6-9) We have found the same to be true for MBE-grown polycrystalline CdTe. The SEM photomicrographs shown in Figure 2.2.1 indicate an estimated increase in average grain size from ~ 0.25 um for the as-grown and air annealed films without a $CdCl_2$ dip to ~ 1 um for the $CdCl_2$ treated and annealed films. Note that little or no grain growth is evident for the air annealed CdTe film without the $CdCl_2$ treatment. It is likely that the presence of $CdCl_2$ during the anneal induces a sintering mechanism within the CdTe film that acts to decrease inter-grain pore size and increase average grain size. (7) The effect of this grain growth on solar cell performance is shown in Table 2.2.1 which indicates a dramatic improvement in all solar cell parameters, with the efficiency increasing from 1.3% to 8.6%.

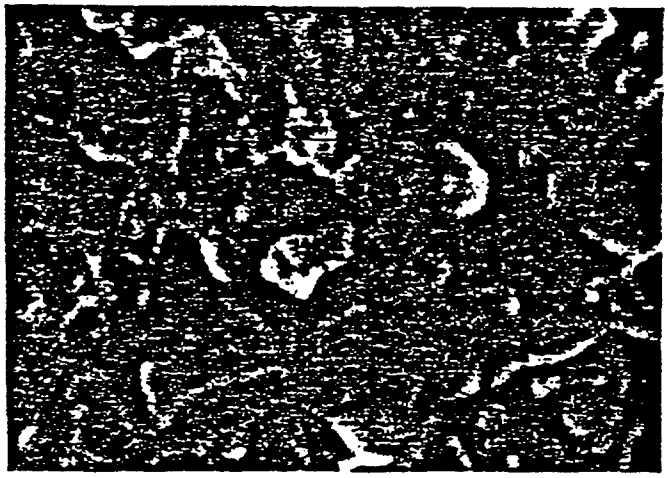
B. Effect of $CdCl_2$ Treatment on the Photoresponse of CdTe/CdS Structures

CdTe grain growth is expected to reduce the bulk and interface state density which tend to influence the spectral response and leakage current of the fabricated device. In order to directly assess the effects of $CdCl_2$ treatment on recombination at the CdTe/CdS junction and in the CdTe bulk, SPV measurements were performed on CdTe/CdS



(a) (b)

1 μm



(c)

1 μm

Figure 2.2.1 SEM photomicrographs of (a) as-grown CdTe, and CdTe annealed in air at 400 C for 35 minutes (b) without $CdCl_2$ and (c) with $CdCl_2$.

Table 2.2.1 **AM1.5 solar cell data for MBE-grown ZnTe/CdTe/CdS devices processed with and without $CdCl_2$ fluxing agent.**

treatment	Voc (mV)	Jsc ($mA-cm^{-2}$)	FF	EFF (%)	Rs $\Omega-cm^2$)
no $CdCl_2$	385	10.5	0.32	1.3	3.6
with $CdCl_2$	720	23.1	0.51	8.6	.90

structures with and without the $CdCl_2$ treatment, prior to back contact (ZnTe + Ni) deposition. Samples of identical thickness from the same growth run, deposited on identical substrates, were used for the SPV analysis. Figure 2.2.2 shows the measured SPV spectra for (a) an as-grown sample, (b) a sample after air anneal and (c) a sample dipped in $CdCl_2$ followed by an air anneal. The as-grown CdTe/CdS structure (curve a) yields a small and flat SPV response prior to the CdTe bandedge ($\lambda \sim 850$ nm), while the air annealed structure without the $CdCl_2$ treatment exhibits a peak near the bandedge. This peak can be attributed to the p-type conversion of CdTe (14) and subsequent formation of a p-CdTe/n-CdS heterojunction after air annealing which aids in the collection of carriers generated close to and within the CdTe depletion layer (recall that light is incident on the CdTe side and not the CdS). However, even though annealing in air without $CdCl_2$ aids in the formation of the CdTe/CdS junction, little or no improvement in CdTe bulk diffusion length is evident based on the similar SPV response for shorter wavelengths below the peak for both the as-grown and air annealed samples. In contrast, the SPV response of the CdTe/CdS structure annealed after the $CdCl_2$ treatment (curve c of Figure 2.2.2) is significantly larger at all wavelengths compared to the structure annealed without $CdCl_2$, suggesting an increase in effective carrier collection length and an improvement in CdTe bulk quality. Furthermore, the peak near the bandedge is even more pronounced after the $CdCl_2$ treatment suggesting additional improvement in the junction quality compared to CdTe/CdS annealed without the $CdCl_2$ dip. The trends in the SPV spectra are consistent with $CdCl_2$-induced grain growth shown in Figure 2.2.1 suggesting that the SPV improvement results from a decrease in the density of grain

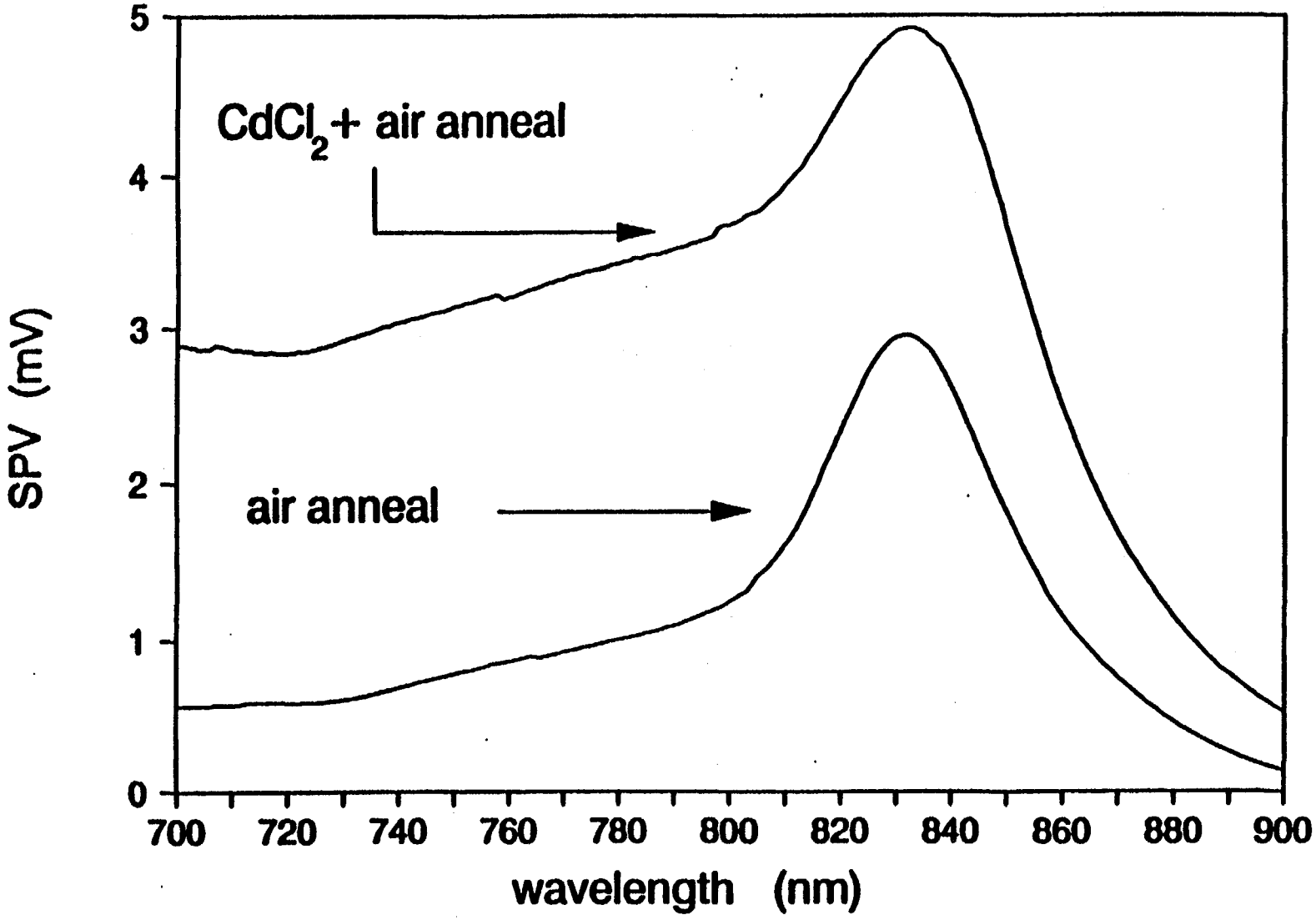


Figure 2.2.2 SPV spectra of as-grown, air annealed, and $CdCl_2$ + air annealed CdTe/CdS structures with light incident on the CdTe surface.

boundary states throughout the CdTe bulk and depletion region. To investigate the role of the $CdCl_2$ treatment on interface quality, bias-dependent spectral response measurements were performed on solar cells fabricated from films annealed with and without $CdCl_2$. Figure 2.2.3 shows the spectral responses for each sample with and without an applied reverse bias, revealing three important results. First, a significant increase in absolute spectral response with the $CdCl_2$ treatment demonstrates reduced interface recombination and increased carrier collection length. Second, while the spectral response of both samples show a wavelength-independent increase with applied reverse bias, the spectral response of the $CdCl_2$ treated samples show a smaller bias dependence, suggesting an improved interface collection function (15) due to reduced number of defect states at or near the CdTe/CdS interface after $CdCl_2$ treatment. Both of these results are consistent with the SPV data. Finally, even after the $CdCl_2$ treatment, appreciable bias dependence in the spectral response is evident suggesting that there is still considerable interface recombination in this 8.6% efficient cell. The identification and elimination of the states responsible for this recombination is necessary to increase device performance further.

C. Effect of $CdCl_2$ Treatment on CdTe/CdS Junction Transport Properties

The dark J-V-T behavior of devices processed with and without the $CdCl_2$ process were analyzed to investigate the effect of the $CdCl_2$ treatment on the diode transport mechanisms in the CdTe/CdS cell. The measured and modeled dark lnJ-V characteristics of both samples are shown in Figure 2.2.4 as a function of temperature.

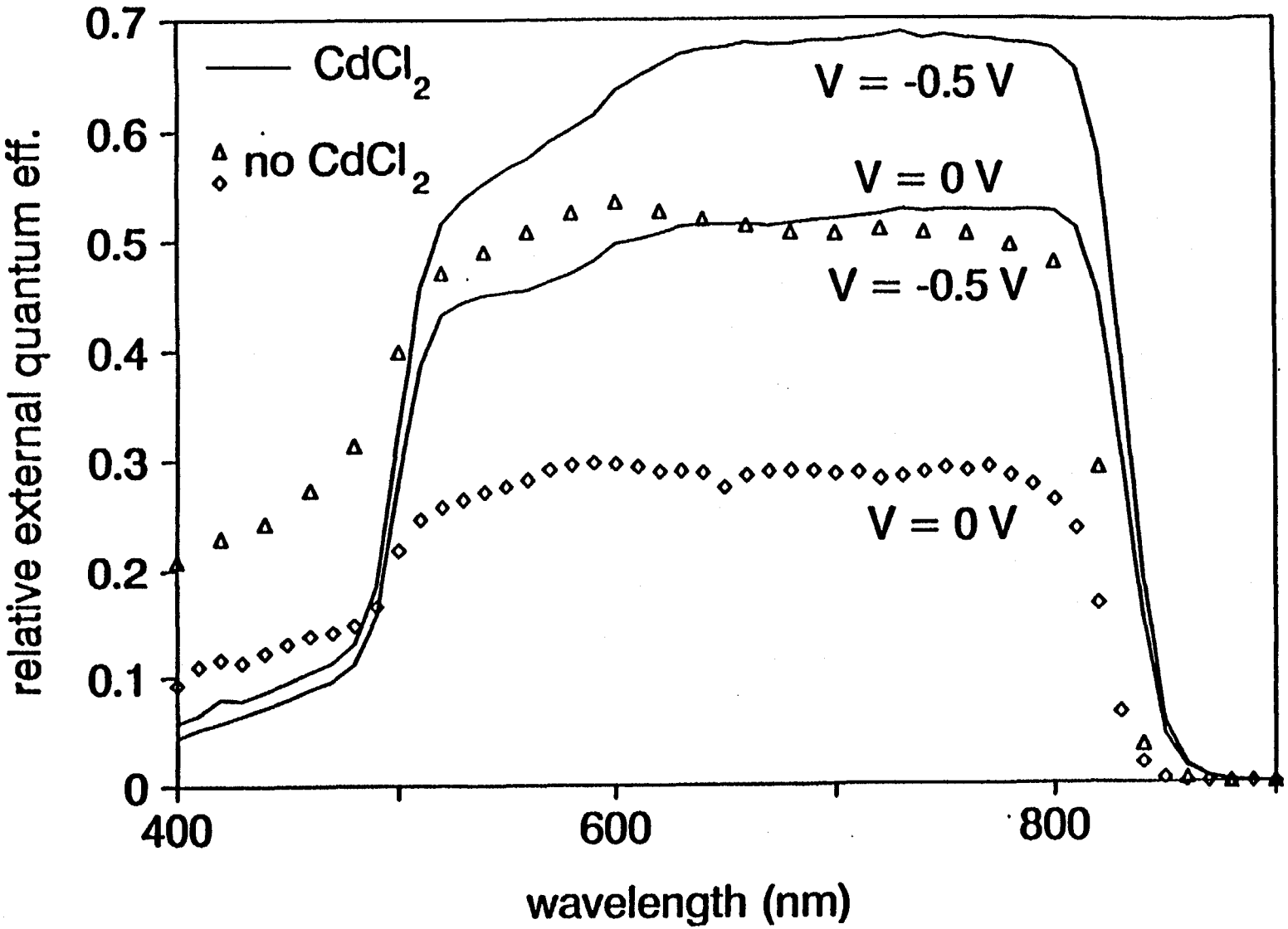


Figure 2.2.3 **Bias-dependent spectral response data of completed Ni/ZnTe/CdTe/CdS/SnO_2/glass solar cells with $CdCl_2$ (solid lines) and without $CdCl_2$ (symbols). The values of the applied reverse bias are noted.**

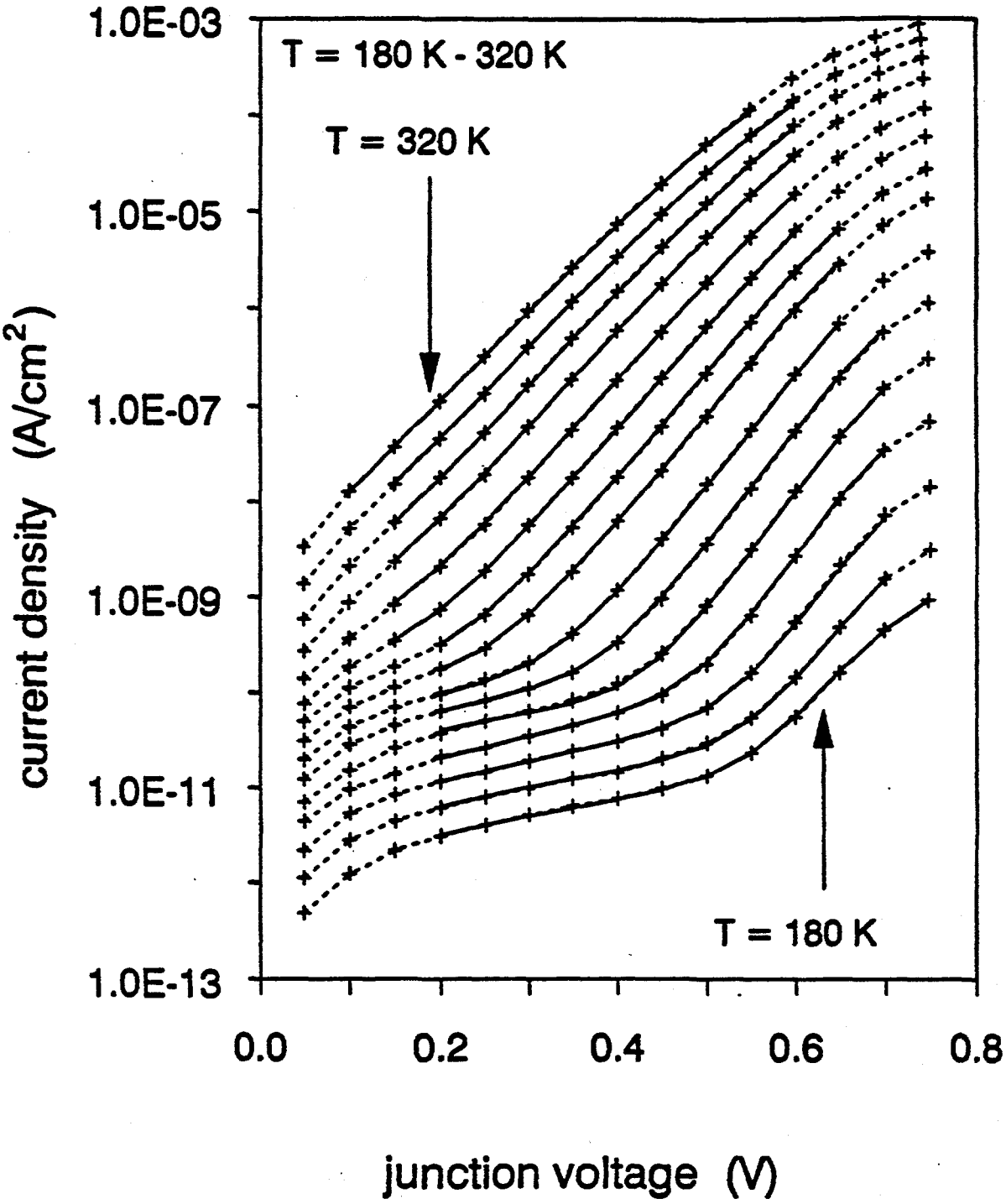


Figure 2.2.4 (a) Measured (symbols) and modeled (lines J-V-T data for (a) $CdCl_2$ + air annealed and (b) air annealed without $CdCl_2$Ni/SnTe/CdTe/CdS/SnO_2/glass solar cells. Shown is the current behavior as a function of junction voltage (V-JR). The average error of each fit is less than 5%.

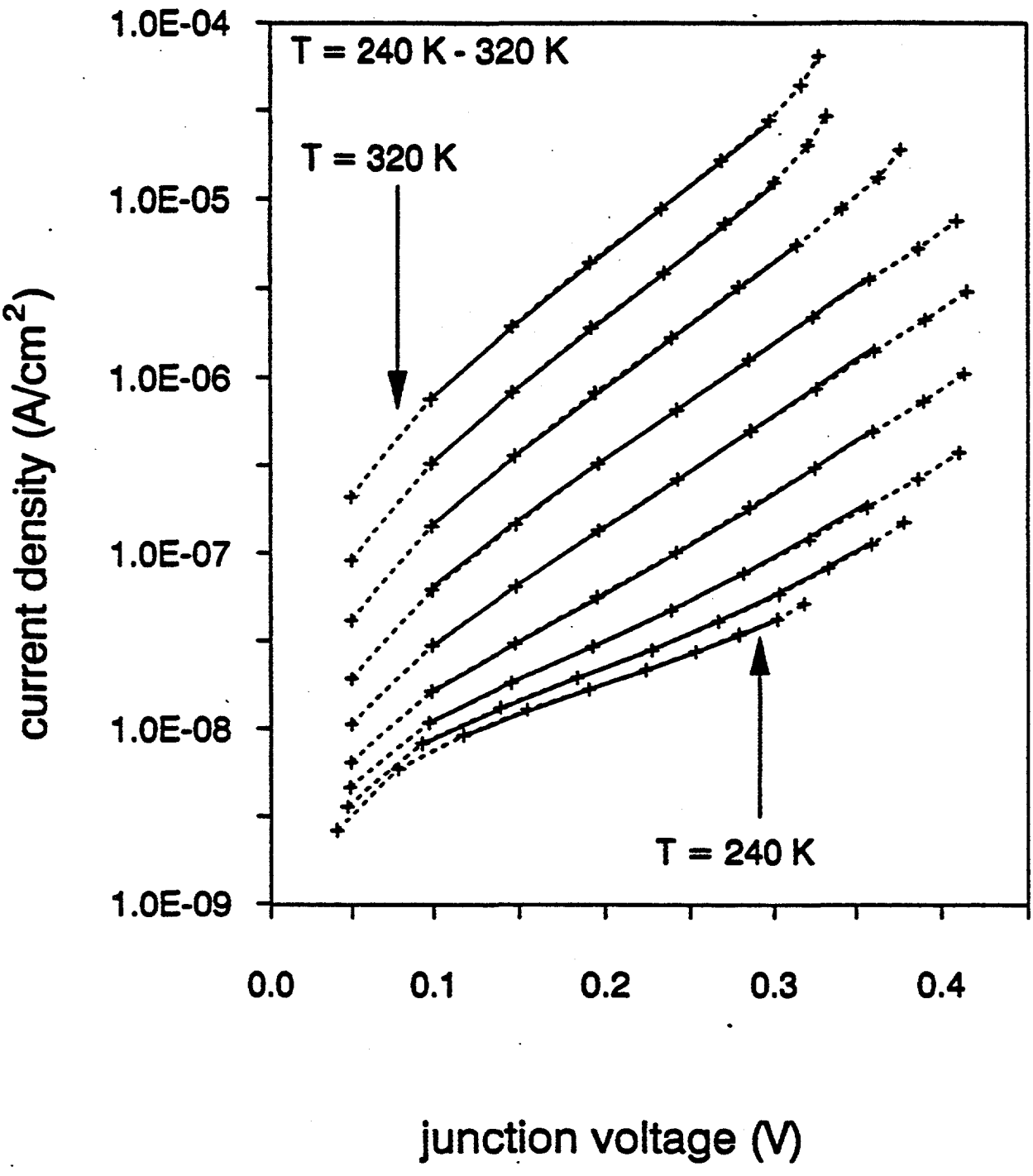


Figure 2.2.4 (b) Measured (symbols) and modeled (lines J-V-T data for (a) $CdCl_2$ + air annealed and (b) air annealed without $CdCl_2$Ni/SnTe/CdTe/CdS/SnO_2/glass solar cells. Shown is the current behavior as a function of junction voltage (V-JR). The average error of each fit is less than 5%.

Each lnJ-V curve was fit to the double diode equivalent circuit model described by eqs. (2) -(4), and the fitting parameters for each cell as a function of temperature are summarized in Tables 2.2.2 and 2.2.3. The lnJ-V characteristics are plotted with respect to the junction voltage (= V-JR_s) to reveal the junction transport. The deviation from linearity at higher bias voltages is due to the non-ohmic behavior of the back Ni/ZnTe/CdTe contact at larger bias voltages. (16) Figure 2.2.4 shows significant differences in the voltage dependence and magnitude of the diode current for devices processed with and without $CdCl_2$, suggesting a change in the dominant mode of current transport. To understand and quantify this difference, the dominant transport mechanisms in each cell are described in the remainder of this section.

The dark current transport in the $CdCl_2$-treated cells above 220 K was best described by a single diode model, viz.,

$$J = J_{01}\{exp[(q/A_1kT)(V - JR_s)] - 1\} + (V - JR_s)/R_{sh} \quad (6)$$

where

$$J_{01} = J_{001}exp(-\Delta E/kT) \quad (7)$$

which is the general form for recombination-controlled current transport. (17) For interface recombination-dominated current transport, the value of A_1 should be ~ 1 for this device structure ($A_1 = 1 + (N_A\epsilon_{CdTe})/(N_D\epsilon_{CdS})$ for interface recombination) and the activation energy, ΔE, of the lnJ_{01} vs. 1000/T plot should be ~ 1.2 eV (built-in voltage of the CdS/CdTe junction). (18) Neither of these conditions were met for the $CdCl_2$-treated devices because $A_1 = 1.75$ and $\Delta E = 0.85$ eV, Figure 2.2.5 and Table 2.2.2. Hence, it is concluded that interface recombination is not the dominant transport mechanism for

Table 2.2.2 Dark J-V-T parameters extracted from fit to eqs. (2) - (4) for MBE-grown CdTe/CdS solar cell treated with $CdCl_2$ fluxing agent. Diode 1 (subscript 1) represent the higher voltage region of the J-V-T data and diode 2 (subscript 2) represent the lower voltage region of the J-V-T curves. α_1 and α_2 represent the slopes of the lnJ-V characteristics and $\alpha_2 = 1/A_2kT$ in the table.

T (K)	J_{o1} (Acm^{-2})	A_1	α_1	J_{o2} (Acm^{-2})	α_2	R_s (Ω-cm^2)
180	9.5×10^{-18}	2.16	29.8	4.3×10^{-13}	9.51	4.0×10^{6}
190	2.6×10^{-17}	2.05	29.8	7.9×10^{-13}	9.71	5.1×10^{5}
200	3.4×10^{-17}	1.90	30.5	2.5×10^{-12}	9.57	1.3×10^{5}
210	1.5×10^{-16}	1.75	31.6	6.5×10^{-12}	9.49	4.0×10^{4}
220	3.2×10^{-15}	1.78	29.6	------	------	9.8×10^{3}
230	3.2×10^{-14}	1.78	28.3	------	------	2.4×10^{3}
240	2.2×10^{-13}	1.77	27.3	------	------	9.5×10^{2}
250	2.1×10^{-12}	1.77	26.2	------	------	3.2×10^{2}
260	9.5×10^{-12}	1.77	25.2	------	------	1.8×10^{2}
270	4.4×10^{-11}	1.77	24.3	------	------	9.8×10^{1}
280	2.0×10^{-10}	1.77	23.4	------	------	6.0×10^{1}
290	8.5×10^{-10}	1.77	22.6	------	------	3.4×10^{1}
300	2.6×10^{-9}	1.75	22.1	------	------	2.4×10^{1}
310	8.1×10^{-9}	1.74	21.4	------	------	1.7×10^{1}
320	2.1×10^{-8}	1.73	21.0	------	------	1.5×10^{1}

Table 2.2.3 Dark J-V-T parameters extracted from fit to eqs. (2) - (4) for MBE-grown CdTe/CdS solar cell not treated with $CdCl_2$ fluxing agent. J-V data below 240 K was dominated by resistance terms and are not listed.

T (K)	J_{o1} (Acm^{-2})	A_1	R_s (Ω-cm^2)
240	2.2×10^{-9}	3.02	3.5×10^{6}
250	4.0×10^{-9}	2.96	8.1×10^{5}
260	9.0×10^{-9}	2.92	2.4×10^{5}
270	2.4×10^{-8}	2.80	8.2×10^{4}
280	8.2×10^{-8}	2.76	2.8×10^{4}
290	2.3×10^{-7}	2.70	1.2×10^{4}
300	4.7×10^{-7}	2.63	6.6×10^{3}
310	9.8×10^{-7}	2.53	4.0×10^{3}
320	2.3×10^{-6}	2.50	1.9×10^{3}

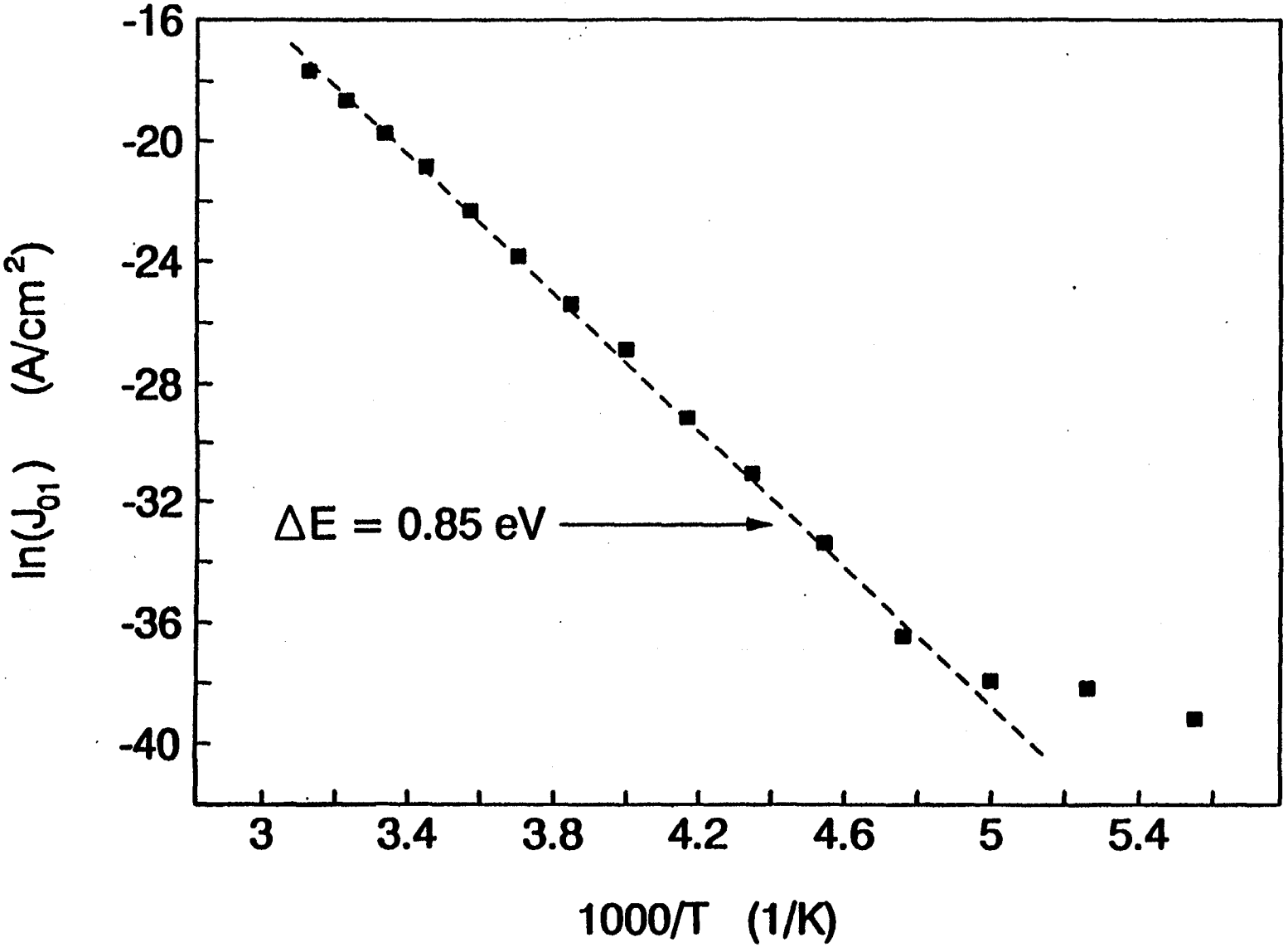


Figure 2.2.5 Plot of lnJ_{01} vs. 1000/T for CdTe/CdS cells have undergone $CdCl_2$ + air anneal.

$CdCl_2$-treated CdTe/CdS devices. If recombination through localized states within the CdTe depletion region is dominant, then a plot of $\ln(J_{01}T^{-2.5})$ vs. 1000/T should yield an activation energy approximately equal to half of the CdTe bandgap. (17,19) Such a plot is shown in Figure 2.2.6, yielding a ΔE value of 0.79 eV, close to half of the CdTe bandgap. Hence it is likely that depletion region recombination dominates current transport in the $CdCl_2$-treated cells. Furthermore, the A_1 value of 1.75 suggests that the dominant path of recombination occurs through states displaced either above or below midgap (A_1 = 2 for a midgap recombination center). The presence and importance of these states will be discussed later. Note that below 220 K the J-V-T behavior exhibits temperature-independent lnJ-V slopes (given by α_1 and α_2 in Table 2.2.2 after correction for series resistance) and weakly temperature dependent diode prefactors (J_{01} and J_{02}), as determined by further computer fitting. These transport characteristics suggest that a tunneling-type behavior is dominant at lower temperatures. Further analysis showed that the observed characteristics at low temperatures were well described by a multi-step tunneling model (20) which required ~ 40-50 tunneling steps through the CdTe depletion region to fit the experimental J-V-T behavior, similar to previously reported results for. (15) Note that two parallel diodes dictate the low temperature transport, as indicated in Table 2.2.2. The dominant mode of dark current transport in cells processed without $CdCl_2$ was found to be significantly different than the $CdCl_2$-treated cells. Analysis of the J-V-T behavior (above 240 K) of the cells processed without the $CdCl_2$ treatment indicates thermally activated current transport, but with a much lower activation energy of 0.56 eV (Figure 2.2.7) compared to 0.85 eV for the $CdCl_2$-treated cell. This low value of ΔE (slope

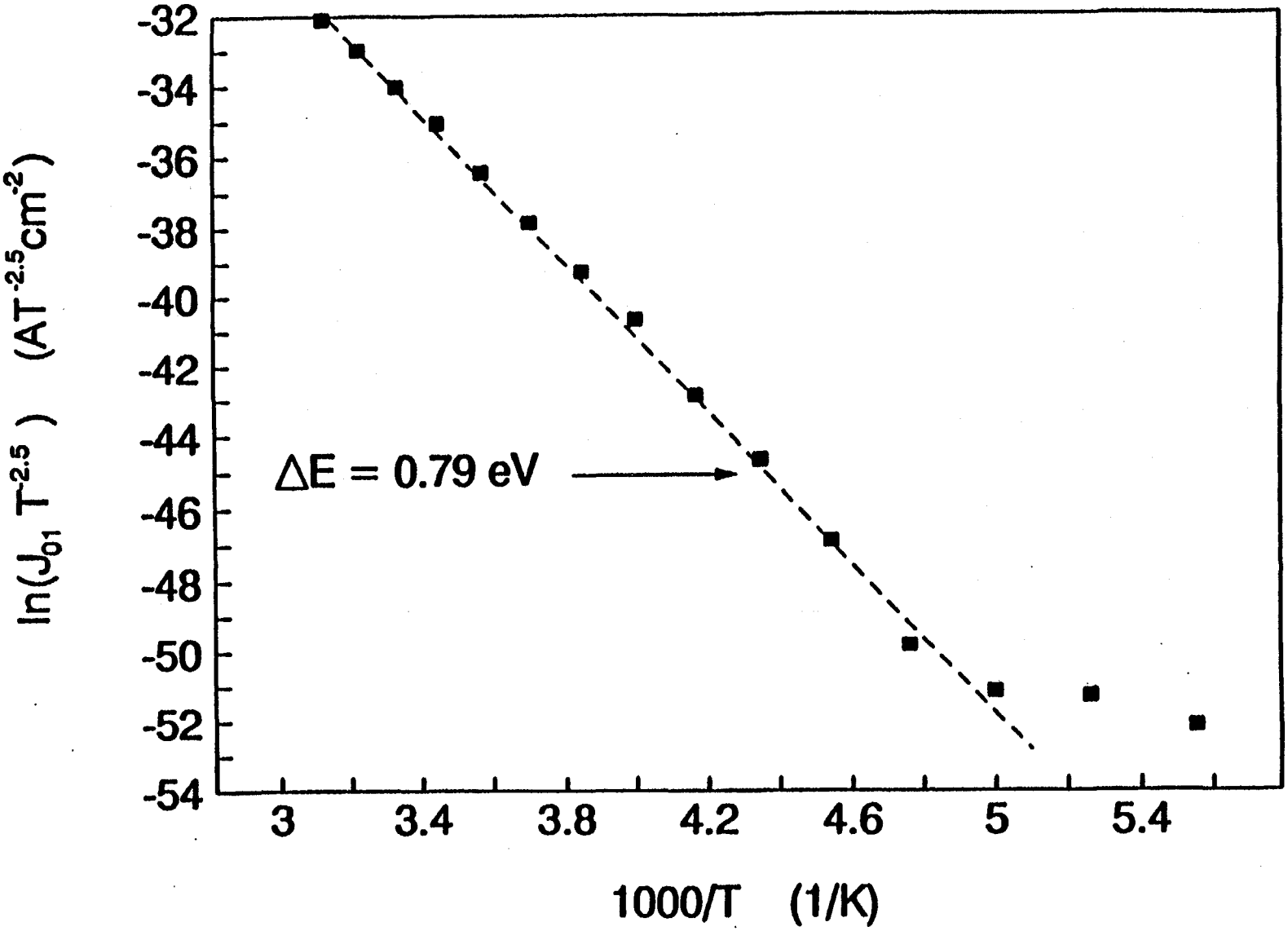


Figure 2.2.6 Plot of $\ln(J_{01}T^{-25})$ vs. 1000/T for CdTe/CdS cells that have undergone $CdCl_2$ + air anneal.

of lnJ_{01} vs 1000/T) is responsible for the large diode current and J_{01} values observed for the cells processed without $CdCl_2$. Furthermore, the current transport behavior cannot be explained by depletion region recombination (in contrast to the $CdCl_2$-treated cell), interface recombination, or direct tunneling. This is evident from Table 2.2.3 which shows that the diode quality factor (A_1) is > 2 and is temperature-dependent (recall that A_1 = 1.75 and was independent of temperature for the $CdCl_2$-treated cell), eliminating the possibility of simple depletion region and interface recombination. In addition, the lnJ-V slope (α_1) is temperature-dependent and J_{01} is thermally-activated (Figure 2.2.6), which eliminates the possibility of direct tunneling as the dominant transport mechanism. Instead, current transport by thermally-assisted tunneling of holes from CdTe into interface states followed by interface recombination was found to adequately explain the observed J-V-T behavior of the CdTe/CdS heterojunctions processed without $CdCl_2$. The J-V-T behavior is well described by the tunneling/interface recombination (T/IR) model of Miller and Olsen (21) which approximates the thermally-assisted tunneling process by a series combination of direct tunneling and pure interface recombination. According to the T/IR model, (21)

$$J = J_{01}[exp[C(V - JR_s)] - 1] + (V - JR_s)/R_{sh} \quad (8)$$

$$J_{01} = J_{001}exp(-\Delta E/kT) \quad (9)$$

$$C = (1 - f)B + f/(\xi kT) \quad (10)$$

where ΔE is the thermal activation energy shown in Figure 2.2.7, B is a temperature-independent tunneling parameter, C is the slope of the lnJ-V curves, and ξ represents the voltage division between the CdTe and CdS. The value of the f parameter quantifies the

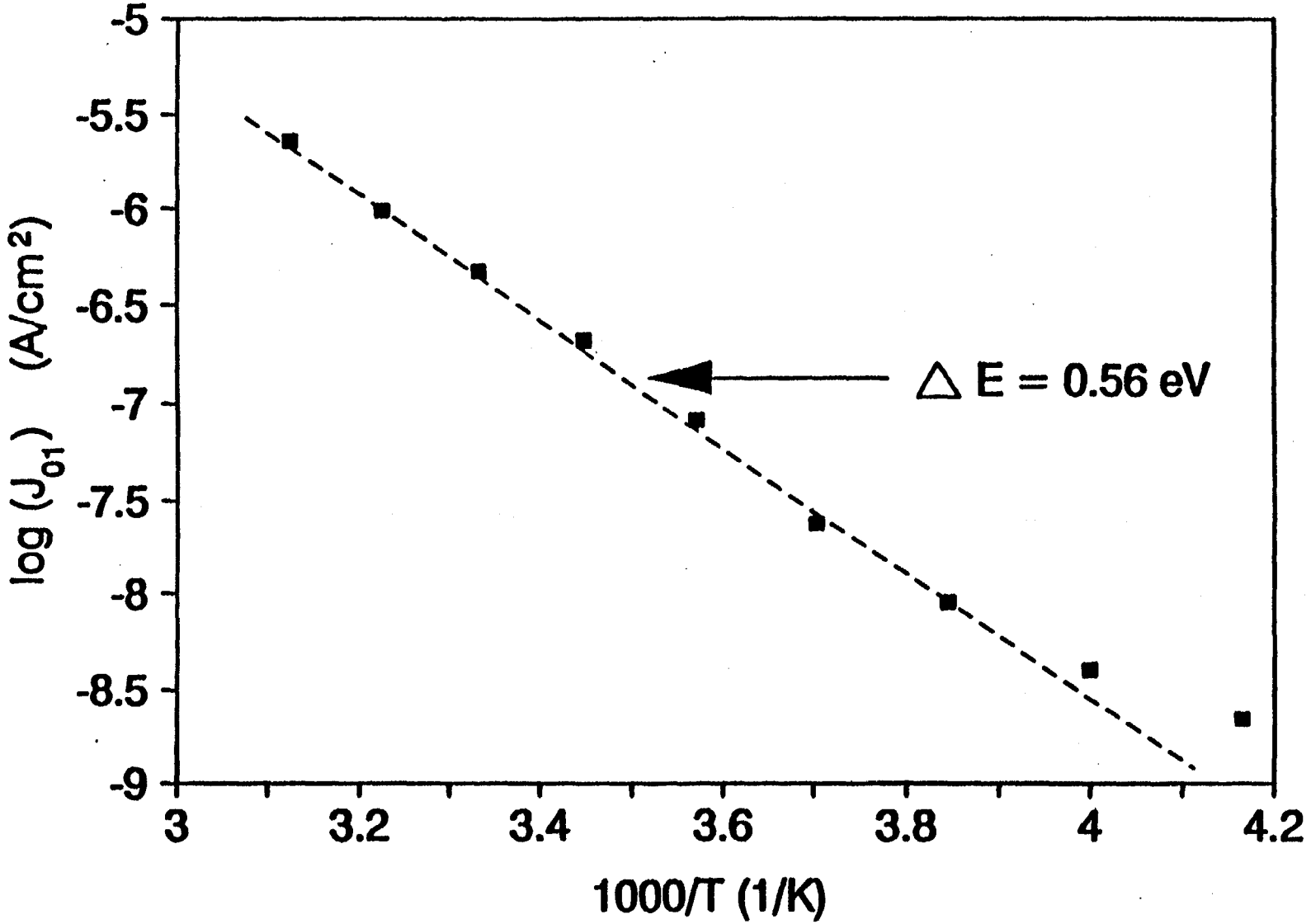


Figure 2.2.7 Plot of lnJ_{01} vs. 1000/T for a CdTe/CdS cell annealed without $CdCl_2$.

degree of tunneling in the observed J-V behavior with f = 1 representing pure interface recombination and f = 0 representing direct tunneling. By plotting the experimentally determined values of C ($=q/A_1kT$ in Table 2.2.3) vs. 1000/T in Figure 2.2.8, the values of (1-f)B and f/ξ in eq. (10) were determined to be 10.3 V^{-1} and 0.266, respectively, indicating that the current transport in the cells processed without $CdCl_2$ is limited by both interface recombination and tunneling, consistent with the lower barrier height observed for these devices. Clearly, current transport via thermally-assisted tunneling, as described by the T/IR model, significantly worsens cell performance of the CdTe/CdS devices in the absence of the $CdCl_2$ treatment. It is apparent that the $CdCl_2$-induced grain growth is necessary to decrease leakage current and increase V_{oc} via reduction of interface state density near the interface. However, even though the CdTe/CdS interface no longer controls the dark diode current transport after the $CdCl_2$ treatment, the bias dependence of the spectral response after $CdCl_2$ treatment (Figure 2.2.3) indicates that interface recombination may still limit the collection of photogenerated carriers. This suggests that the $CdCl_2$ treatment removes enough interface states to alter the diode transport mechanism and reduce the diode leakage current, but is less effective in removing interface states that limit the photocurrent collection across the CdTe/CdS (recall the bias dependent spectral response, Figure 2.2.3). To identify the origin and better understand the role of process-related defects, DLTS measurements were performed on CdTe/CdS cells processed with and without the $CdCl_2$ treatment and are discussed in the following section.

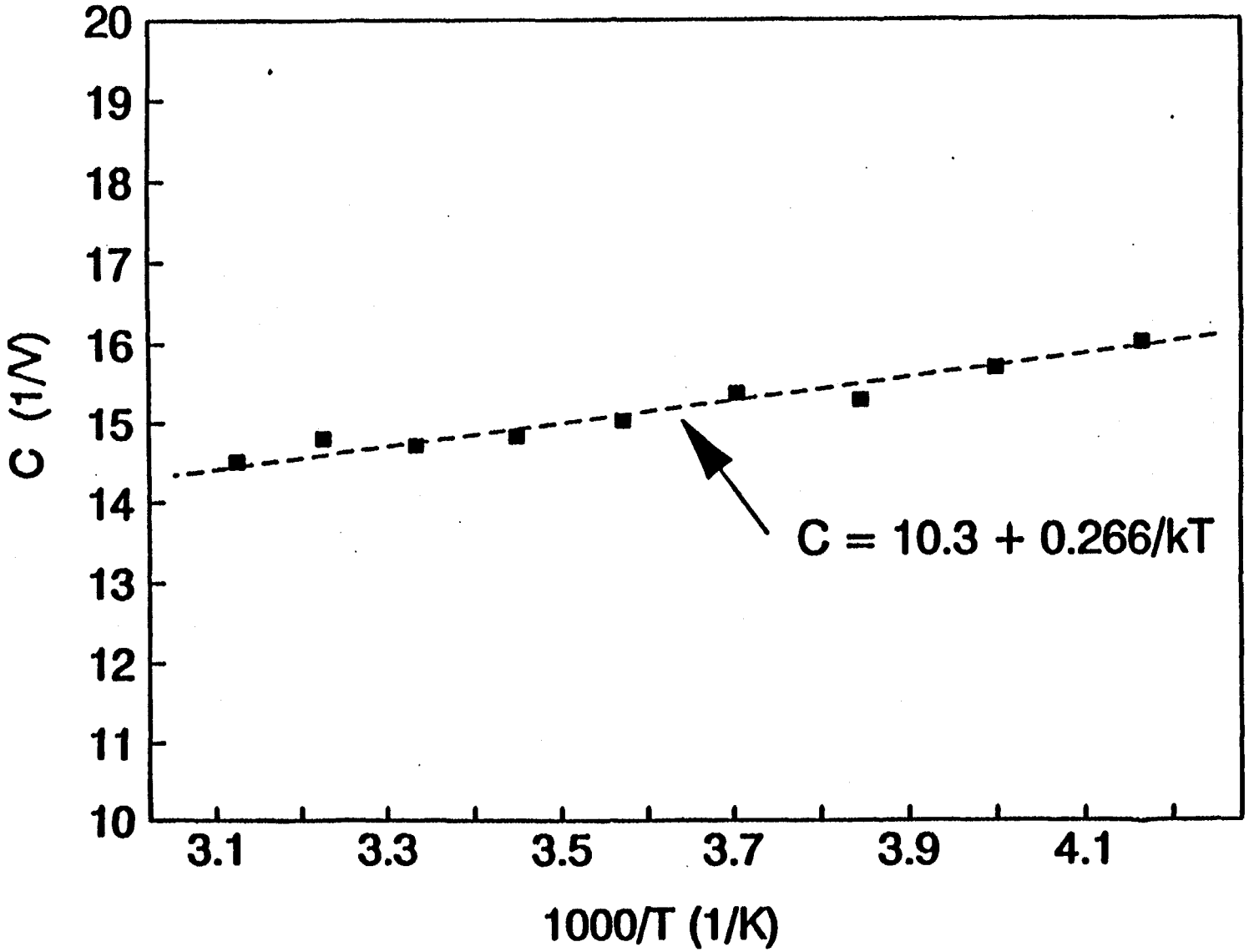


Figure 2.2.8 **Plot of the T/IR model C-factor vs. 1000/T indicating both interface recombination and tunneling limited behavior.**

D. Effect of $CdCl_2$ and Heat Treatment on Defect Generation in CdTe/CdS Heterojunctions

Figure 2.2.9 shows a typical DLTS spectrum obtained for a CdTe/CdS device having undergone an air annealing step with $CdCl_2$ which revealed a hole trap peak at ~ 330 K. DLTS measurements were also performed on CdTe/CdS devices processed without $CdCl_2$, but it was not possible to obtain useful data because of the large series resistance in these samples which dominated the DLTS response. From the Arrhenius plot of $\log(T^2/e_{mp})$ vs. 1000/T, constructed using weighing functions from 4 msec. to 64 msec., the hole trap in the $CdCl_2$-treated device was found to be located at E_v + 0.64 eV (± 0.04 eV) with a cross-section of 8.2×10^{-16} cm^2 and a trap density of 8×10^{13} cm^{-3} (for the trap shown in Figure 2.2.9). This energy level agrees well with Cd vacancy-related defects such as doubly-ionized cadmium vacancies, $V_{Cd}^{=}$, or singly-ionized cadmium vacancy-halogen complexes such as $(V_{Cd}Cl)^-$, both of which have been reported to contribute acceptor-like traps in the range 0.54 to 0.9 eV above the valence band edge in CdTe after heat treatments. (22-28) Since halogen ions are known to readily form complexes with cadmium vacancies to give deep and shallow levels, it is likely that the E_v + 0.64 eV trap results from $(V_{Cd}Cl)^-$ defects. (27,28) However, further measurements are necessary to determine the exact configuration of the defect responsible for this trap. The presence of acceptor-like traps within the CdTe depletion region was found to adversely affect the CdTe/CdS solar cell characteristics. Figure 2.2.10 shows the direct consequences of the density of this defect on the measured V_{oc} and J_{sc} of different CdTe/CdS cells that have undergone the $CdCl_2$ dip followed by heat treatment. It is clear from this figure that the

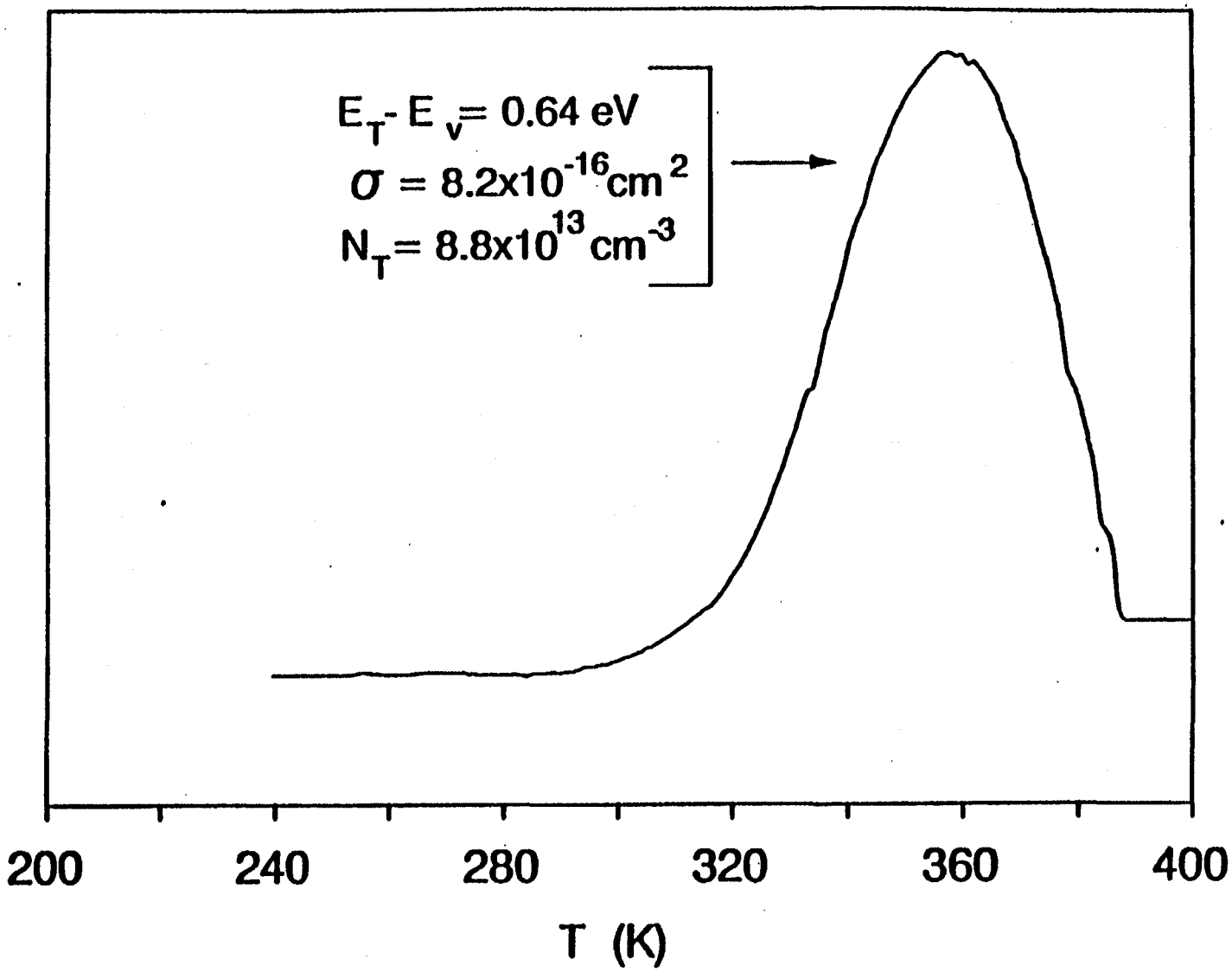


Figure 2.2.9 **Typical DLTS spectrum of a CdTe/CdS cell having undergone an air anneal with $CdCl_2$ using a steady reverse bias of -400 mV and a pulse height of 300 mV, a pulse width of 8 msec. and a rectangular weighing function with a period of 4 msec.**

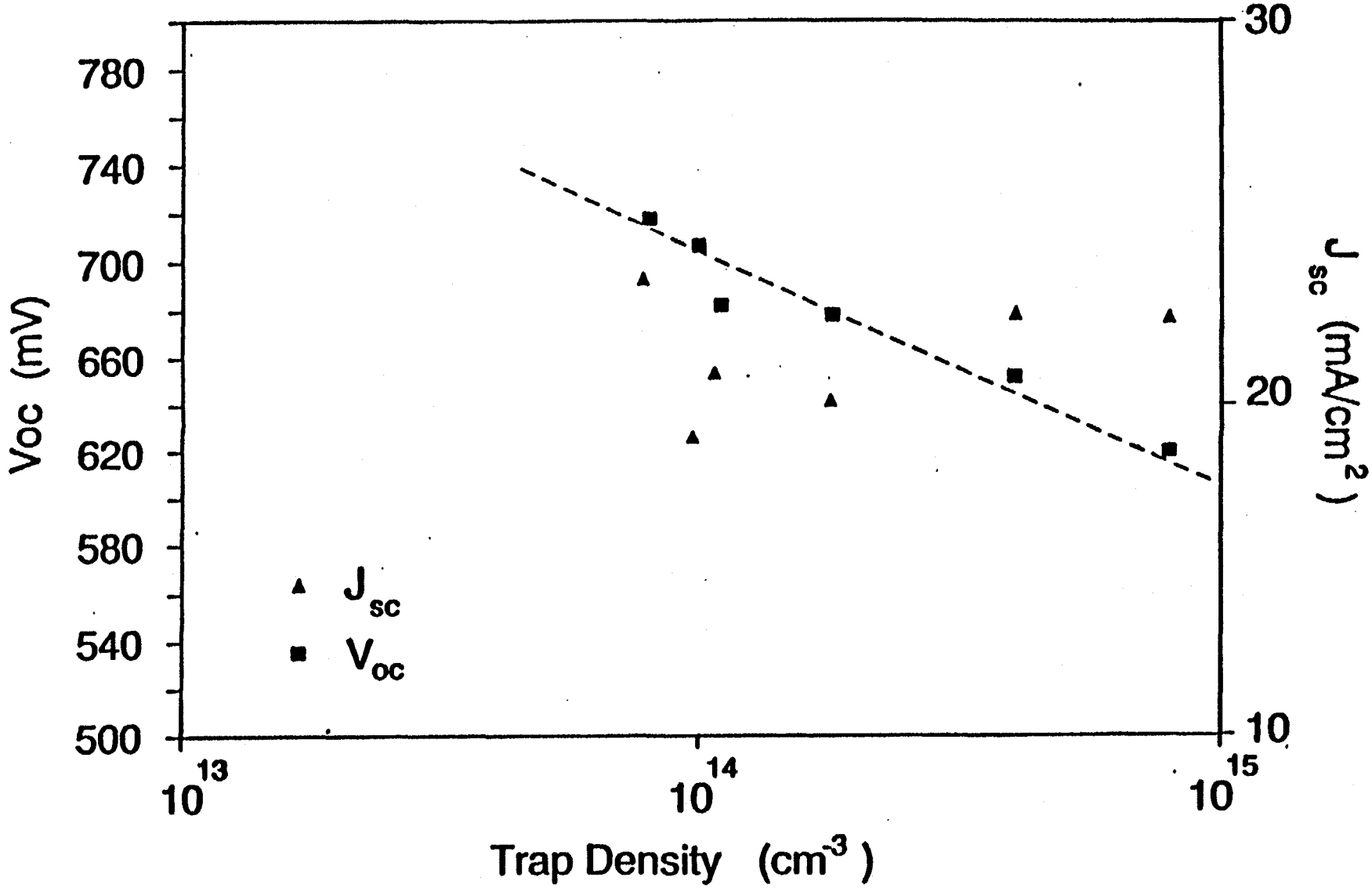


Figure 2.2.10 Measured cell V_{oc} and J_{sc} as a function of ($V_{Cd}Cl$) defect concentration for different CdTe/CdS solar cells that have undergone a 400 C air anneal with $CdCl_2$ as determined by DLTS measurements.

V_{oc} is inversely proportional to the detected trap density while there is no apparent correlation between J_{sc} and the trap density. Presently, it is not clear why the trap density shows a random spatial variation on a given sample with different cells and also from sample to sample since no intentional attempt was made to introduce a variation. It has recently been suggested that such variations can result from non-uniform drying of the $CdCl_2$-methanol solution on the CdTe surface prior to heat treatment. (29) To determine the variation in trap density as a function of depth, DLTS was performed in a multi-bias mode. A decrease in trap concentration from ~ $8x10^{13}$ cm^{-3} to ~ $3x10^{13}$ cm^{-3} was found as the CdTe/CdS interface is approached by decreasing the depletion width. This is consistent with V_{Cd} and/or Cl diffusion from the CdTe surface into the bulk as a result of the 400 C anneal. From Figure 2.2.10, it is evident that the variations in V_{oc} must result from the diode leakage current, which was found to increase with increasing trap density, since J_{sc} showed no such dependence. Recalling that diode current transport in the devices processed with $CdCl_2$ is dictated by recombination via deep states within the CdTe depletion region which is characterized by an A-factor of 1.75, the off-center position of the trap at E_v + 0.64 eV suggests that this level may be responsible for the diode transport mechanism (note that an A-factor of 2 represents a midgap or E_v + 0.75 eV trap in CdTe (17)) which in turn dictates V_{oc}. Hence, the $CdCl_2$ dip and heat treatment greatly improves the cell performance via grain growth, interface state density reduction, and transport mechanism modification, but this process also appears to limit V_{oc} by cadmium vacancy-related defect formation. Further increases in V_{oc} and efficiency can be expected if the generation of this defect can be reduced or eliminated. This may

require further modification or optimization of the current cell processing schemes.

In order to understand systematically the role of chlorine-related defects in CdTe/CdS cells, the concentration of $CdCl_2$ was varied in the range of 0.25 to 1 (saturated). PL measurements were performed on finished devices to investigate the defects produced by different $CdCl_2$ concentrations, because the DLTS measurements were not successful in some cells due to high leakage current near the DLTS peak temperature. Light I-V measurements were performed on the finished devices to monitor the device performance and correlate it with the defects. Table 2.2.4 shows the CdTe/CdS solar cell parameters measured immediately after the fabrication of the cells treated with different $CdCl_2$ concentrations.

It is clear from the table that V_{oc} and fill factor are a strong function of the $CdCl_2$ concentration while J_{sc} shows a weak dependence on $CdCl_2$ concentration. The data in Table 2.2.4 also show that the saturated $CdCl_2$ solution often used by the investigators (1,2) is not the optimum. Figure 2.2.11 shows the PL spectra of CdTe/CdS devices

Table 2.2.4 Variation of CdTe/CdS cell parameters for cells treated with different $CdCl_2$ concentrations.

$CdCl_2$ concentration	Efficiency %	V_{oc} (mV)	J_{sc} mA/cm^2	FF %
0.25	8.8	693	24.2	52
0.50	10.8	707	25.5	59
0.75	9.6	695	25.6	54
1.0	7.02	657	21.7	49

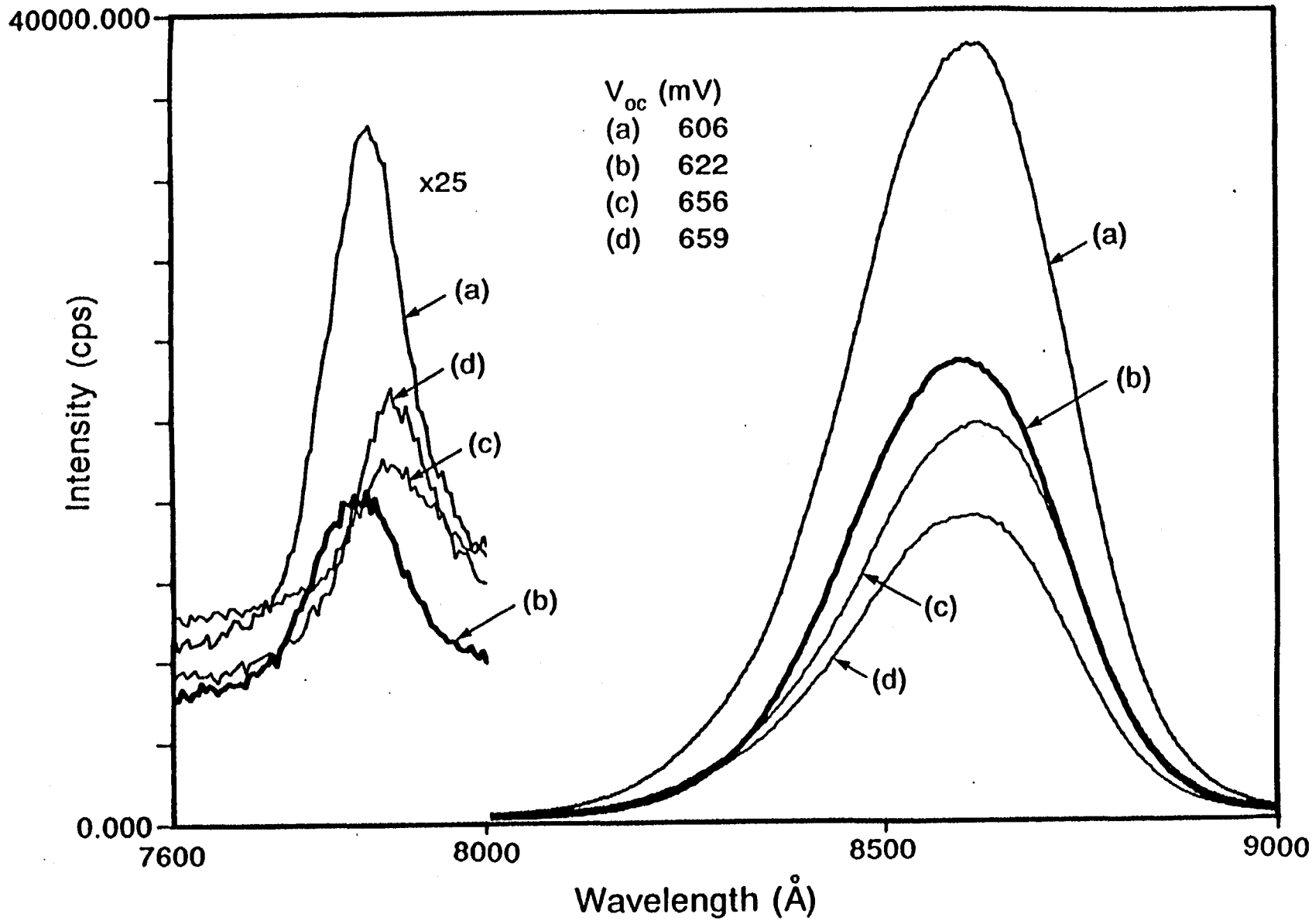


Figure 2.2.11 **PL spectra of CdTe/CdS structures treated with different $CdCl_2$ concentrations, (a) 100% (saturated), (b) 50%, (c) 25%, and (d) 75%. The corresponding measured V_{oc} on these structures are also shown.**

treated with different $CdCl_2$ concentration. PL spectra showed two common features, a peak around 7900 Å and a broad band centered around 8400 Å. In CdTe, the broad band centered around 8400 Å is generally attributed to structural defects, native defects or V_{Cd}-Cl defect complexes. (27,30,31) The peak at 7900 Å is attributed to Cd vacancies.(32) The intensity or the peak amplitude of the broad band at 8400 Å is directly proportional to the defect concentration in the sample. Several investigators have studied the effects of chlorine in single crystal CdTe by PL and DLTS measurements (9,27,30-32). Chlorine is a donor in CdTe and is also known to form defect complexes with Cd vacancies, which are produced during the heat treatment. Chlorine-cadmium vacancy complexes are acceptor type and give rise to shallow and deep energy levels depending on the type of defect complex. According to the literature (27,30-32) the chlorine-cadmium defect complexes have energies in the range E_v + 0.15 - E_v +0.9 eV. Generally, PL measurements give information about shallow levels and DLTS gives information about deep levels. The fact that the PL broad band around 8400 Å has been attributed to V_{Cd}-Cl complex in the literature (32), and the intensity of the PL band and the density of E_v + 0.64 eV DLTS peak both are inversely proportional to V_{oc}, suggests that both the defects are probably chlorine related complexes formed during the $CdCl_2$ treatment. Thus, on one hand $CdCl_2$ treatment is critical to high efficiency CdTe cells but on the other hand it could place an upper limit on the practically achievable efficiency unless the $CdCl_2$ process is modified or optimized.

2.3. Cu/Au Contact Induced Instabilities In CdTe/CdS Cells

Long term stability is critical for terrestrial solar cells. The CdTe/CdS cells are known to be sensitive to moisture induced degradation (1). However, proper encapsulation can mitigate this problem for cells with graphite contacts. We have been using Cu-Au contacts and have noticed considerable degradation in our recent high efficiency (10-12%) cells. We were able to obtain cell efficiencies as high as 12% immediately after the cell fabrication. However, after two to three weeks of storage in the laboratory atmosphere (not in the desiccator), the cell efficiency degraded to ~10%. This degradation in efficiency is associated with significant reduction in V_{oc} and fill factor and a modest decrease in J_{sc}. Table 2.3.1 shows the light I-V data of CdTe cells as a function of storage time. It is clear from the table that after the rapid initial degradation the cell efficiency nearly stabilizes. It was also found that the higher efficiency cells degrade more compared to the lower efficiency cells. Such degradation was observed primarily in cells with Cu/Au contacts (2). ZnTe or graphite contacts to CdTe have been found to be more stable (2).

Table 2.3.1 Solar cell parameters of CdTe/CdS cell as a function of storage time

Cell Parameters	One day	Four Weeks	Br:MeOH etch
V_{oc}(mV)	756	709	742
J_{sc}(mA/cm^2)	24.5	23.8	24.1
FF(%)	64	59	62
Efficiency	11.9	10.1	11.2

In order to understand the contact degradation mechanism further and recover the cell efficiency, the degraded CdTe cells were treated in Br:MeOH etch for seven seconds. It was found that after the Br:MeOH etch both V_{oc} and fill factor values were restored to almost 90% of the original values, as shown in the table 2.3.I This suggests that oxidation of Cu or Te is the probable cause of cell degradation and the Br:MeOH etch is able to reduce those oxides. Formation of such oxides could result from the lack of humidity or moisture control in the laboratory. Further investigation is necessary to determine the exact mechanism, however, our data show that this degradation is not permanent and is reversible to a large extent.

3.0 PROGRESS IN CdZnTe SOLAR CELLS

3.1. A Study of Polycrystalline CdZnTe/CdS Films and Interfaces

3.1.1. Introduction

In recent years, CdTe has become a strong candidate for photovoltaic applications due to its optimum bandgap, high absorption coefficient, and ease of deposition. Cell efficiencies of ~13% have been reported for single crystal CdTe solar cells (1) and greater than 14% for polycrystalline thin film CdTe cells.(2) It has been projected (3) that thin film cell efficiencies in the range of 15-20% can be obtained by a tandem cell design consisting of two cells of different bandgap semiconductors on top of each other (1.7 eV on 1.1 eV). $Cd_{1-x}Zn_xTe$ is a good candidate for the top cell since its bandgap can be tailored between 1.45 eV (CdTe) and 2.26 eV (ZnTe) by adjusting the film composition. However, very few attempts have been made to grow these films in polycrystalline form (4-6) and hence little is known about the properties of such films, particularly when grown on coated glass substrates that are suitable for solar cells. Good control of bulk composition and reduced or no interdiffusion at the CdZnTe/CdS interface is important for high performance devices based on these materials.

In this work, polycrystalline $Cd_{1-x}Zn_xTe$ films were grown by molecular beam epitaxy (MBE) on CdS/SnO_2/glass substrates to form frontwall solar cell structures. X-ray diffraction (XRD), electrochemical surface photovoltage (SPV), and Auger electron spectroscopy (AES) measurements were performed to determine the proper growth conditions for obtaining a uniform bandgap and composition throughout the film and an abrupt film/CdS interface. In this paper we report growth-induced variations in the

composition and interface quality of the heterojunctions formed by MBE and MOCVD grown polycrystalline ternary films.

3.1.2. Growth and Characterization of Films

Polycrystalline $Cd_{1-x}Zn_xTe$ and CdTe films were grown by MBE using a Varian Gen II MBE system. Elemental sources with a purity better than 5N were used for all constituents. The films were grown on CdS/SnO_2/glass and glass substrates which were cleaned by standard degreasing procedures. The substrates were baked in a vacuum of ~ $1x10^{-7}$ torr at 250 C for 2 hours prior to film growth. During film growth, the substrate temperature was kept at 275 C for 30 minutes to commence film growth and increased to 300 C for the remainder of the run. Growth rates were typically ~ 1 um/hr for both the $Cd_{1-x}Zn_xTe$ and CdTe films.

X-ray diffraction studies were performed to estimate the film composition using a Phillips PW1800 automatic diffractometer with 1.504 Å Cu-K_α radiation. The lattice constants, a, of the $Cd_{1-x}Zn_xTe$ films were determined from the XRD data by plotting the lattice parameter, a(θ), against its angular dependence (θ) and determining the intercept according to (7)

$$a(\theta) = 0.5[(\cos^2\theta/\sin\theta) + (\cos^2\theta/\theta)] \qquad (1)$$

where 2θ is the diffraction peak position. The film composition (x) was determined from the lattice constant according to (8)

$$a(x) = 6.481 - 0.381x \quad (A), \qquad \text{for } Cd_{1-x}Zn_xTe \qquad (2)$$

where x is the atomic concentrations of Zn in the $Cd_{1-x}Zn_xTe$.

The absorption edge or bandgap of the films was estimated by a nondestructive electrochemical SPV measurement in which an electrolyte composed of 0.2M NaOH and 0.1M EDTA (ethylenediaminetetraacetic acid) forms a Schottky barrier contact with the film surface. This barrier separates the photogenerated carriers to produce the open circuit voltage as a function of incident wavelength. This technique is also capable of providing information about bandgap variations within the film because the electrolyte/semiconductor junction can be biased so that controlled etch-steps can be made between SPV measurements. Hence, compositional variations in the direction of film growth can be monitored. This technique has been discussed in more detail elsewhere. (9,10) Bandgaps of the films were estimated from the wavelength (λ) at the midpoint of the absorption edge ($E_g(eV) = 1.24/\lambda(um)$) in the SPV response. It should be noted that in certain cases, the sharpness of the absorption edge can be influenced by the diffusion length and film thickness.

To gain further confirmation on the compositional uniformity of the ternary films, AES profile measurements were performed using a Physical Electronics Model 600 Scanning Auger Multiprobe. The angle between the sample normal and the electron beam was 45°. All AES data were taken using a 3 KeV electron beam with a current of 1.0 uA. Sputter profiling was performed using a normally incident 2KeV Ar ion beam at a current density of 28 uA/cm^2.

3.1.3. Results and Discussion

A. MBE-grown polycrystalline $Cd_{1-x}Zn_xTe$ films

In order to achieve optimal composition (x=0.3-0.4) or bandgap (1.65-1.75 eV) for tandem solar cell applications, MBE films were grown with various Zn/(Cd+Zn) ratios. Figure 3.1.1 shows a comparison of XRD spectra of a CdTe film and a $Cd_{1-x}Zn_xTe$ film grown with a Zn/(Cd+Zn) beam flux ratio of 0.4 on CdS/SnO_2/glass substrates. A comparison of the peak positions and relative amplitudes in each diffraction pattern with the tabulated values (10) suggests that in both cases the CdTe cubic structure is the only detectable phase. By determining the lattice parameter (a(θ)) associated with each major $Cd_{1-x}Zn_xTe$ diffraction peak, the lattice constant (a) of the film was determined according to equation (1). By combining this information with the measured bandgap from the SPV (Figure 3.1.3a) for several films grown with various Zn/(Cd+Zn) beam flux ratios, a correlation was established between the growth conditions (Zn/(Cd+Zn) beam flux ratio), film composition, and bandgap for the MBE-grown polycrystalline $Cd_{1-x}Zn_xTe$ films and is shown in Figure 3.1.2. A linear dependence was found between these parameters for the composition range investigated which indicates proper substitution of Zn for Cd in the MBE films. This result is consistent with data reported for single crystal $Cd_{1-x}Zn_xTe$ films grown by other techniques (6,8), suggesting that grain boundaries do not influence the reproducibility and control of film composition. Furthermore, this linear relationship was found to be independent of growth rate and Te flux.

Figure 3.1.3a shows an SPV spectrum of a $Cd_{1-x}Zn_xTe$ film grown on the

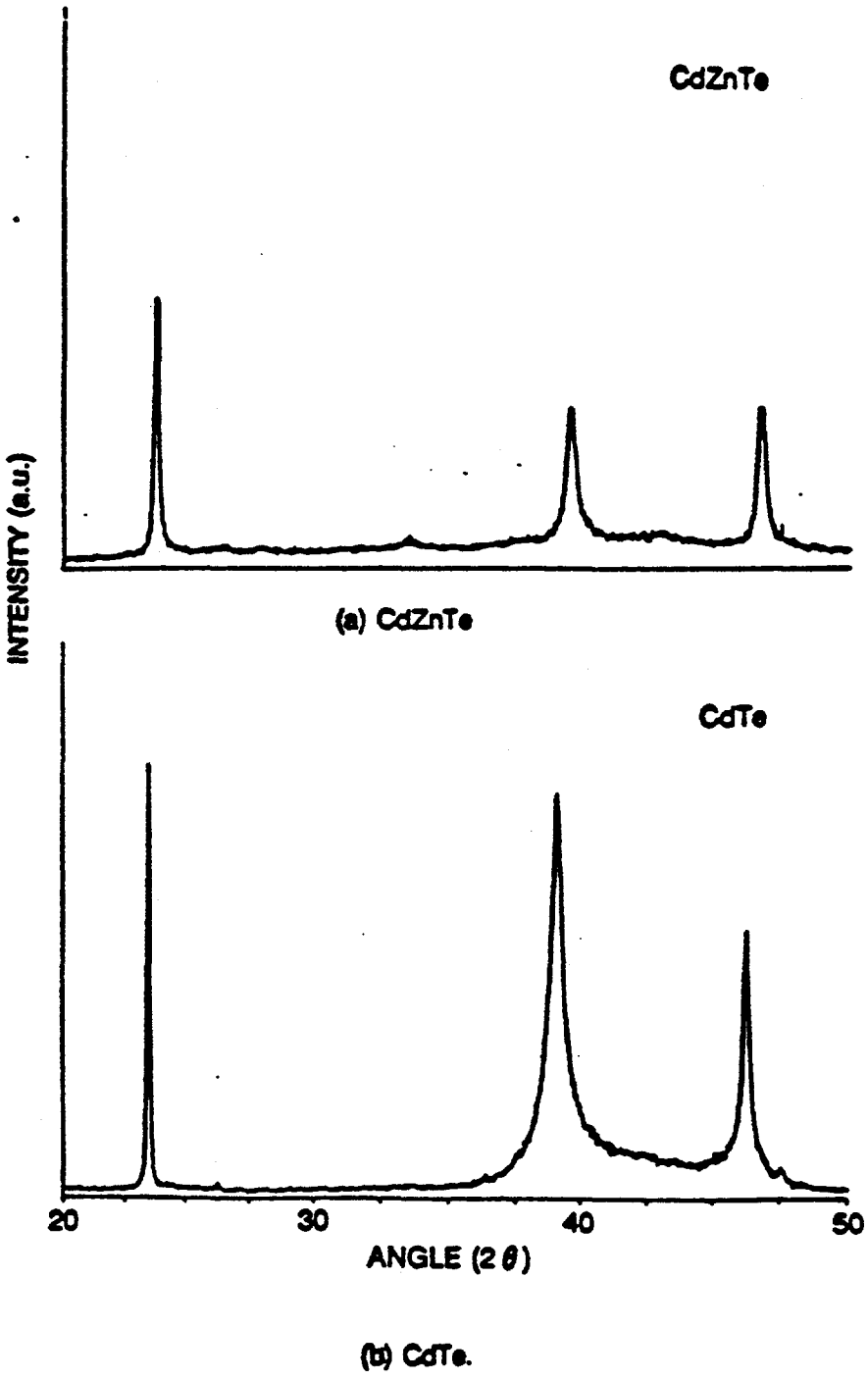


Figure 3.1.1 X-ray diffraction spectra of MBE-grown polycrystalline (a) CdZnTe and (b) CdTe films

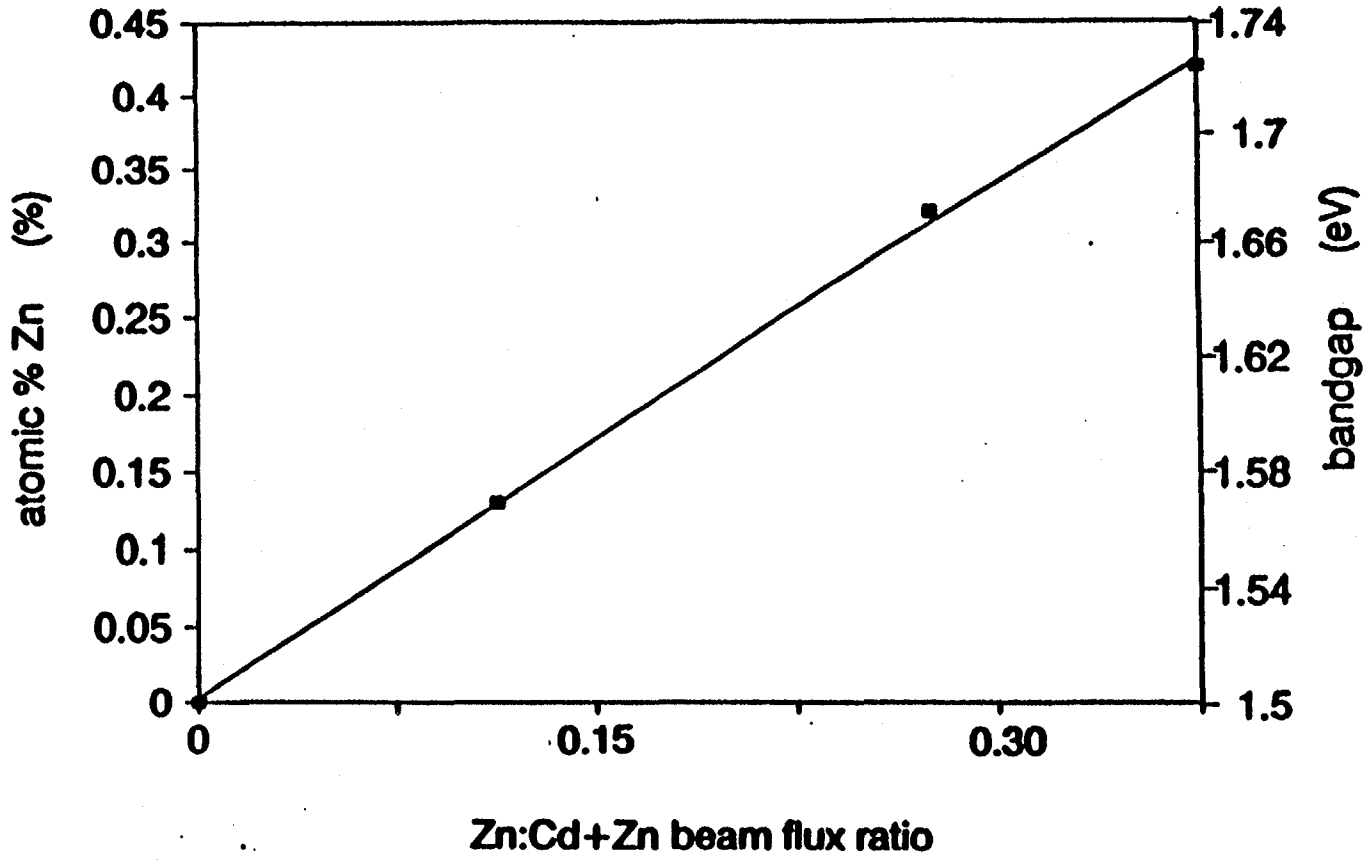


Figure 3.1.2 Concentration of Zn calculated from x-ray data and eq. (2), and bandgap measured by surface photovoltage for MBE-grown CdZnTe films grown using various Zn:Cd+Zn beam flux ratios as shown.

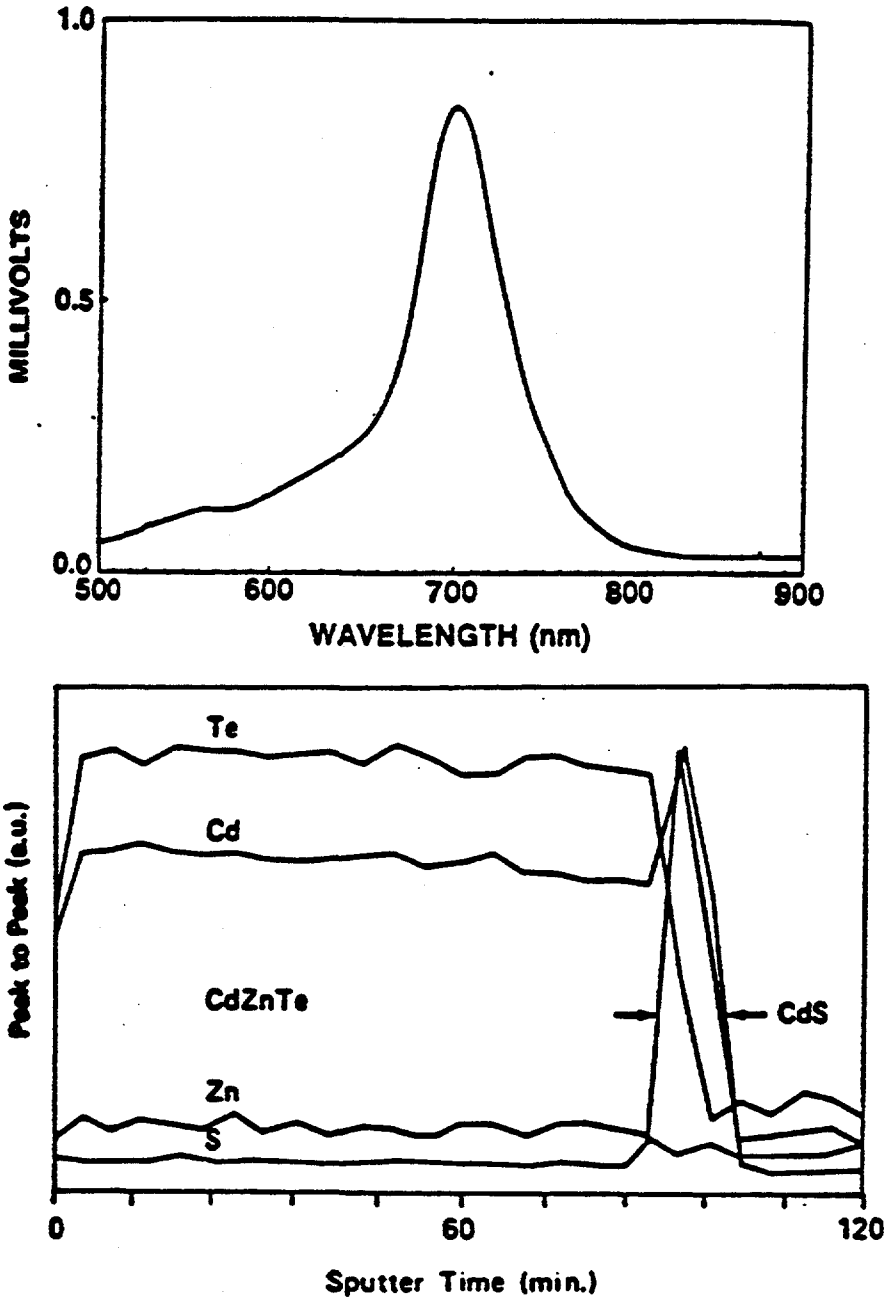


Figure 3.1.3a (a) SPV spectra and (b) Auger depth profile of an MBE-grown CdZnTe film with a bandgap of 1.7 eV on a CdS/SnO_2/glass substrate.

CdS/SnO_2/glass substrate. The sharp absorption edge indicates that the film has uniform composition and negligible sub-bandgap absorption. The compositional uniformity in the direction of film growth was investigated in more detail by Auger depth profiling. Figure 3.1.3b shows a uniform distribution of Cd, Zn, and Te throughout the film thickness, consistent with the sharp SPV cutoff.

3.2. Process Optimization of CdZnTe Polycrystalline Films for High Efficiency Solar Cells

3.2.1. Introduction

Thin film polycrystalline cell efficiencies higher than 20% can be achieved using a tandem cell design. For a two cell tandem design, the optimum bandgaps for the top and bottom cells are 1.7 eV and 1 eV, respectively (1). Considerable progress has been made in the area of the bottom cell, with small area $CuInSe_2$ cell efficiencies in excess of 14% recently been reported recently (2). However, a compatible wide bandgap (1.7 eV) material for the top cell has not yet been developed. CdTe and CdZnTe alloys are considered for top cell applications. CdTe is a promising polycrystalline wide bandgap material that has given small area single cell efficiencies in excess of 14% (3). However, the CdTe bandgap is 1.45 eV instead of 1.7 eV which is optimum for the top cell. Thus, there are two approaches for realizing the goal of 20% efficient polycrystalline cells with a tandem structure. The first approach involves improving CdTe cell efficiencies in excess of 15% and augmenting that with a small amount of power from the bottom cell. The second approach involves developing a 1.7 eV bandgap CdZnTe top cell with efficiency

of ~10% so that to take greater advantage of the bottom cell efficiency due to higher subgap transmission. This paper describes the investigation of growth and process optimization of CdZnTe cells in order to understand the efficiency limiting defects and mechanisms. Future directions are suggested to improve their efficiencies to a point where they can be a potential candidate for ~ 20% tandem cells.

3.2.2. Experimental

A. Film growth

MBE $Cd_{1-x}Zn_xTe$ (x = 0.35, will be referred as CdZnTe) films were grown using a Varian Gen II MBE system and elemental sources were used for all constituents having a purity of at least 5N. The substrates were baked out at 250° C for 3-4 hours before film growth. The substrate temperature was kept at 275° C for 30 minutes to initiate film growth and increased to 300° C for the remainder of the run (4).

B. Cell Fabrication

P-i-n front-wall solar cells were fabricated at AMETEK applied materials laboratory. After a dip in a saturated $CdCl_2$:CH_3OH solution, the CdTe/CdS structures were annealed at 400° C for 30 minutes in air. Annealed films were etched in bromine-methanol solution for 5 sec followed by an evaporation of 1000 Å of Cu-doped p^+ZnTe film. Small area (8 mm^2) Ni contacts were evaporated to form an ohmic contact (5).

C. Material and device characterization

Electrochemical surface photovoltage (SPV) measurement, Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), and transmission measurements were used for optical, physical and chemical characterization of the films. J-V-T, frequency dependent C-V, and bias dependent spectral response measurements were used to characterize device properties.

3.2.3 Results and Discussion

Polycrystalline CdZnTe films with a 1.7 eV bandgap were successfully deposited by MBE on CdS/SnO_2/glass substrates (4). However, CdZnTe solar cells fabricated by the identical process sequence used successfully for high efficiency CdTe cells gave efficiencies of only ~ 4.4%. In addition, the CdZnTe bandgap shifted from 1.7 eV to 1.55 eV and the series resistance (~ 2-6 ohm-cm^2) was 3-5 times higher than in the counterpart CdTe solar cells. Detailed investigations were conducted to understand and remove the source of these problems.

In order to find and eliminate the source of high resistance, depth-resolved AES and ESCA measurements were performed near the CdZnTe surface after annealing (400° C, 30 min. in air without the $CdCl_2$ treatment) and subsequent chemical etching to investigate process-induced changes in the CdZnTe surface which can prevent the formation of good ohmic contacts (6). ESCA analysis and AES profiles in Figure 3.2.1 show that without any post-anneal chemical etch, a significant amount of Cd-O, Te-O and Zn-O are present at and below the CdZnTe surface. After an etch in Br_2:CH_3OH, which

was used in the standard cell fabrication prior to ZnTe/Ni back contact deposition, both Cd and Te oxides were removed from the surface but the Zn-O remained at and below the surface, responsible in part for the high series resistance. In addition, the CdZnTe surface is not as Te-rich (Te/(Cd+Zn)~ 1.2) compared to the counterpart CdTe surface where Te/Cd ratio is ~ 1.5-2. It has been suggested shown that a Te-rich surface can facilitate the ohmic contact formation on p-type CdTe (7).

In an attempt to remove the Zn-O and make the CdZnTe surface Te rich, various chemical etchants were investigated. Figure 3.2.1 shows that a post-anneal saturated dichromate ($K_2Cr_2O_7$:H_2SO_4) etch removed the near surface region that contained Zn-O and yielded a ~ 0.15 um Te-rich surface layer with little or no detectable trace of Cd, Zn, or oxygen. C-V measurements made on the dichromate-etched surface confirmed a much higher carrier concentration of ~ $2x10^{17}$ cm^{-3} in the Te-rich surface layer which gradually dropped down to the bulk doping concentration of ~ $5x10^{15}$ cm^{-3} over a distance of 0.15 um (6). This should eliminate the contribution from high contact resistance to the measured high series resistance.

The next step was to investigate the process-induced bandgap shift observed in processed CdZnTe films. AES depth profiles shown in Figure 3.2.2 and the SPV spectra in Figure 3.2.3 after the standard air anneal, with and without the $CdCl_2$ treatment, clearly demonstrate that it is not the air anneal itself, but the $CdCl_2$ treatment coupled with the air anneal that is responsible for the bandgap shift. Note that the cells were fabricated with the $CdCl_2$ treatment. The Auger profiles show that after the $CdCl_2$ treatment, out-diffusion of Zn from the bulk toward the surface occurs which reduces the bulk Zn

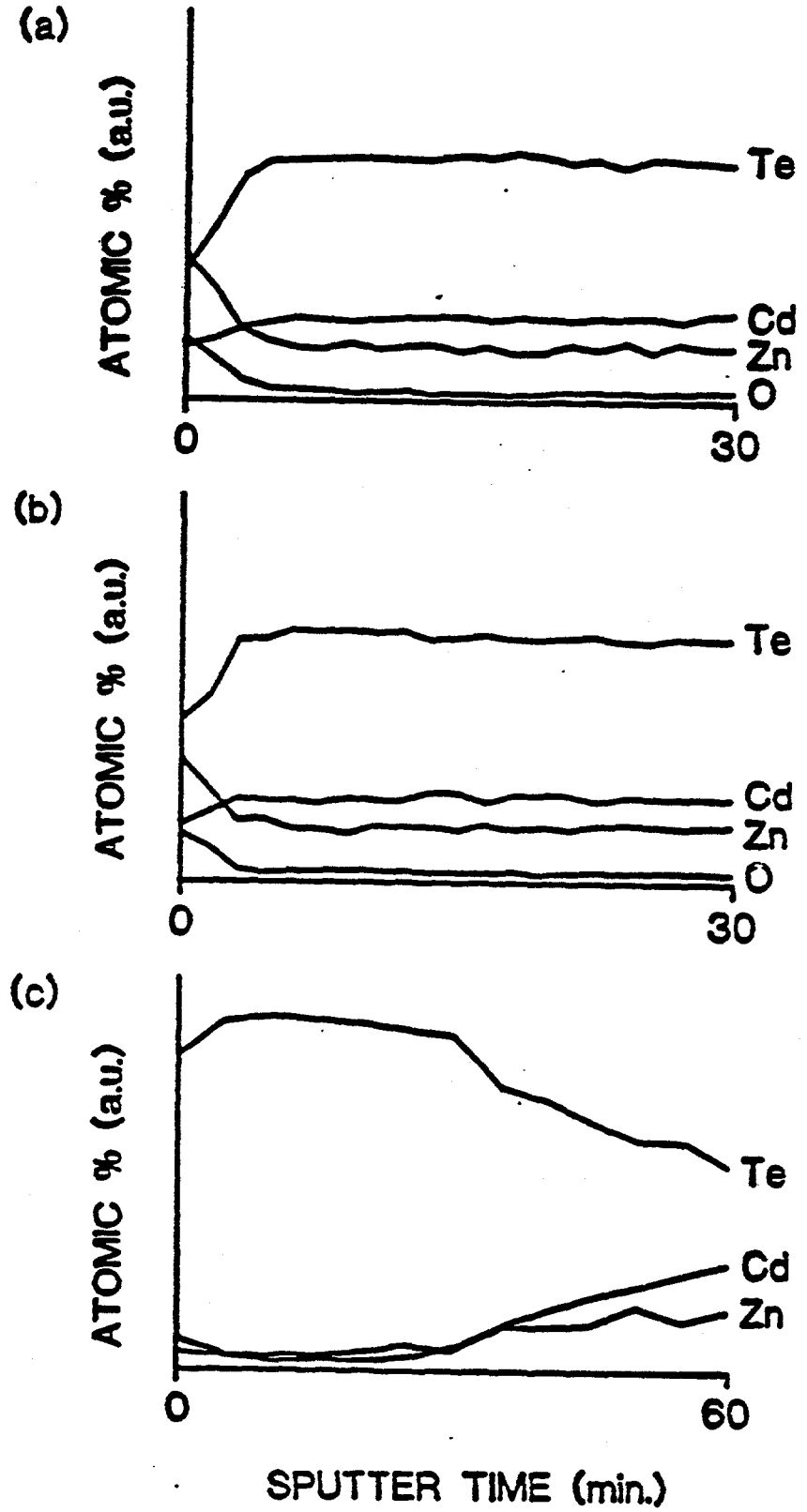


Figure 3.2.1 Auger depth profiles of air annealed CdZnTe films after (a) no post-anneal etch, (b) Br_2CH_3OH etch, and (c) saturated dichromate etch.

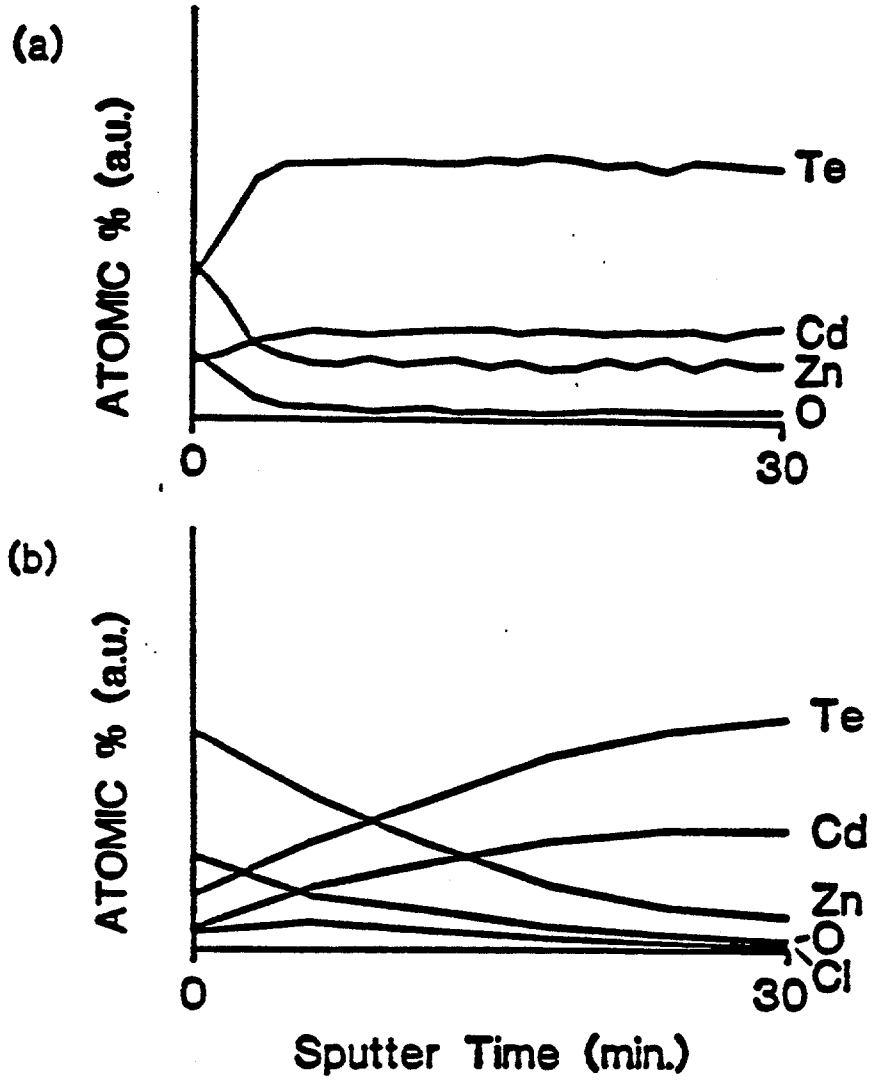


Figure 3.2.2 Auger depth profiles of air annealed CdZnTe films (a) without $CdCl_2$ treatment and (b) with $CdCl_2$ treatment.

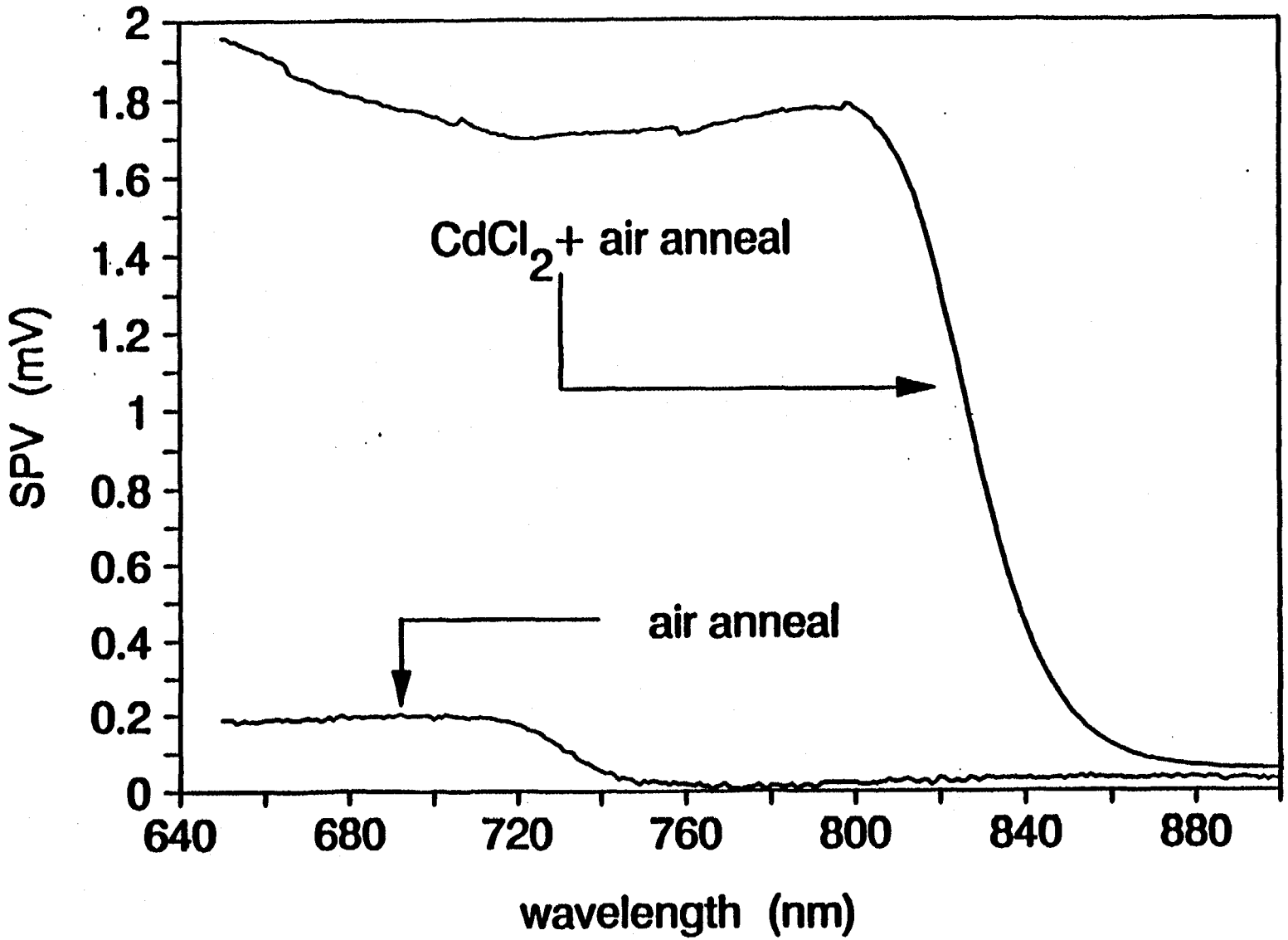


Figure 3.2.3 **Electrochemical surface photovoltage spectra of air-annealed CdZnTe/CdS structures with and without the $CdCl_2$ treatment.**

content and decreases the bandgap, as demonstrated by the shift in the cut-off edge toward the longer wavelength in the SPV spectra of Figure 3.2.3. A proposed model for the phenomenon stems from the fact that thermodynamically, the formation of $ZnCl_2$ is preferred over $CdCl_2$. (8) Therefore, introducing $CdCl_2$ onto the surface and into the CdZnTe bulk triggers the formation of $ZnCl_2$ which has a much higher vapor pressure and lower melting point (318 C (8)) than $CdCl_2$, resulting in the out diffusion of Zn. This process, where Cd from the $CdCl_2$ substitutes for lattice Zn, resulting in $ZnCl_2$ formation can be described by the following equation:

$$Cd_{1-x}Zn_xTe + yCdCl_2 \rightleftharpoons Cd_{1-x+y}Zn_{x-y}Te + yZnCl_2$$

Note that if $y > x$, all of the Zn will be consumed and CdZnTe will reduce to CdTe.

Surface photovoltage data (Figure 3.2.3) taken on the CdZnTe/CdS structures show that if the $CdCl_2$ treatment is bypassed to preserve the bandgap, a very weak photoresponse is observed, resulting in only 1-2% efficient cells. However, the SPV data clearly show that incorporation of $CdCl_2$ during the processing of CdZnTe cells resulted in much higher photovoltages but the cutoff edge (or bandgap) shifted from 1.7 eV to 1.55 eV. The $CdCl_2$ treatment was also found to reduce the series resistance of the CdZnTe/CdS cells by a factor of ~ 10.

The $CdCl_2$ treatment is necessary for obtaining high efficiency CdTe solar cells via grain growth, reduction in recombination, and improved current transport properties. However, the effect of $CdCl_2$ on CdZnTe cell properties is significantly more complicated. Transmission measurements indicate that it is the presence of the $CdCl_2$ during the annealing step of the process induces the observed shift in the CdZnTe bandgap.

Nevertheless, the $CdCl_2$ appears to be necessary to have any efficiency at all, as demonstrated by the comparative cell performance of CdZnTe cells annealed with and without $CdCl_2$.

A model, which follows from a similar argument suggested for polycrystalline CdZnTe films treated with $CdCl_2$, is proposed to explain the bandgap shift observed for the CdZnTe films based on the following key observations. (9-11) The Auger depth profiles show that the presence of $CdCl_2$ during the heat treatment results in extreme out-diffusion of Zn from the bulk toward the surface. This reduces the bulk Zn concentration and causes the observed decrease in the CdZnTe bandgap. Second, the SPV spectra, reveals not only the bandgap shift but also a significant increase in the magnitude of the SPV response which suggests improved photocollection after the $CdCl_2$ treatment, although the improvement is still less than observed for CdTe devices. Third, electron microscopy showed that the grain size of the as-grown CdZnTe films increased from ~0.1 um to ~ 0.3 um after the films were annealed with the $CdCl_2$ treatment. This represents an improvement but significantly less grain growth compared to the CdTe cells. Finally, the formation of $ZnCl_2$ at the annealing temperature is much more likely than $CdCl_2$, by virtue of its lower formation energy. The following model is proposed to describe the formation of $ZnCl_2$ at the expense of lattice zinc:

$$Cd_{1-x}Zn_xTe + yCdCl_2 \leftharpoondown Cd_{1-x+y}Zn_{x-y}Te + yZncl_2$$

Since $ZnCl_2$ has a low melting point (318°C), and a high vapor pressure at the 400°C

anneal temperature (8), it can be deduced that loss of Zn from the film (bandgap shift) occurs via evaporation of $ZnCl_2$ which is formed due to the reaction of CdZnTe with $CdCl_2$ in which Cd from the $CdCl_2$ substitutes for lattice Zn. This reaction reduces the amount of $CdCl_2$ present in the film which explains the poor photoresponse and grain growth due to reduced sintering. From the above discussion, either a modification of the $CdCl_2$ process or a different sintering aid is necessary for obtaining efficient CdZnTe solar cells, while maintaining the desired 1.7 eV bandgap. Alternative methods for achieving this goal in accordance with the model proposed in the previous section are investigated.

Eq. (1) suggests that decreasing the concentration of the $CdCl_2$ solution used prior to the annealing should reduce the bandgap shift. This was experimentally confirmed by steadily decreasing the $CdCl_2$ concentration from the saturated concentration in methanol (1 gram/100 ml), which is known to be optimum for CdTe solar cells (12). However, the improvement in bandgap retention was accompanied by a reduction in the SPV photoresponse due to the reduced grain growth compared to cells processed with the saturated $CdCl_2$ solution. This is consistent with findings for CdTe which also shows a decrease in grain size and photoresponse with decreasing $CdCl_2$ concentration (12). Hence, decreasing the $CdCl_2$ concentration alone is not the solution for the coupled bandgap shift and poor photoresponse. Similarly, it was found that reducing the anneal temperature to slow the chemical reaction and inhibit the formation of $ZnCl_2$ was able to maintain the original 1.7 eV bandgap but again at the expense of poor photoresponse. An anneal temperature of 400°C was found to be necessary for obtaining reasonable photoresponse.

Since the bandgap shift appears to result from the substitution of Cd for Zn, attempts were made to supply excess Zn by dipping the CdZnTe films in solutions of $CdCl_2$ + $ZnCl_2$ of various combinations prior to annealing at different temperatures. Only limited success was obtained using this method since the $ZnCl_2$ readily evaporates from the surface at temperatures greater than 320°C due to its high vapor pressure (8). Annealing at lower temperatures, below 320°C, were performed to retain the volatile $ZnCl_2$, but this resulted in little or no grain growth and poor photoresponse. Thus it appears that $ZnCl_2$ with its high vapor pressure evaporates too fast and behaves as a poor sintering aid under these annealing conditions.

One way to inhibit the evaporation of $ZnCl_2$, and hence Zn out diffusion and poor grain growth, is to perform the anneal in a sealed ambient system containing an overpressure of $ZnCl_2$ instead of the open tube furnace used thus far. This approach was found to be successful in eliminating similar $CdCl_2$-induced effects in polycrystalline CdZnS films. Figure 3..2.4 shows the apparatus assembled for this purpose to emulate a sealed ampule. To supply a controlled overpressure of $ZnCl_2$ into the annealing ambient, an alumina crucible was constructed with four 1 mm holes drilled into the lid. The thickness of the crucible floor was milled down to 1/32 of an inch to insure fast heating of the enclosed $ZnCl_2$ powder. Calculations showed that at least 3.1 milligrams of $ZnCl_2$ powder was necessary to maintain the equilibrium vapor pressure of $ZnCl_2$ in the volume of this annealing chamber. Hence, to insure an overpressure of $ZnCl_2$, 0.2 grams of $ZnCl_2$ powder was loaded into the crucible. The $ZnCl_2$ crucible was placed in the annealing chamber on a quartz plate as shown in Figure 3.2.4. A CdZnTe sample was

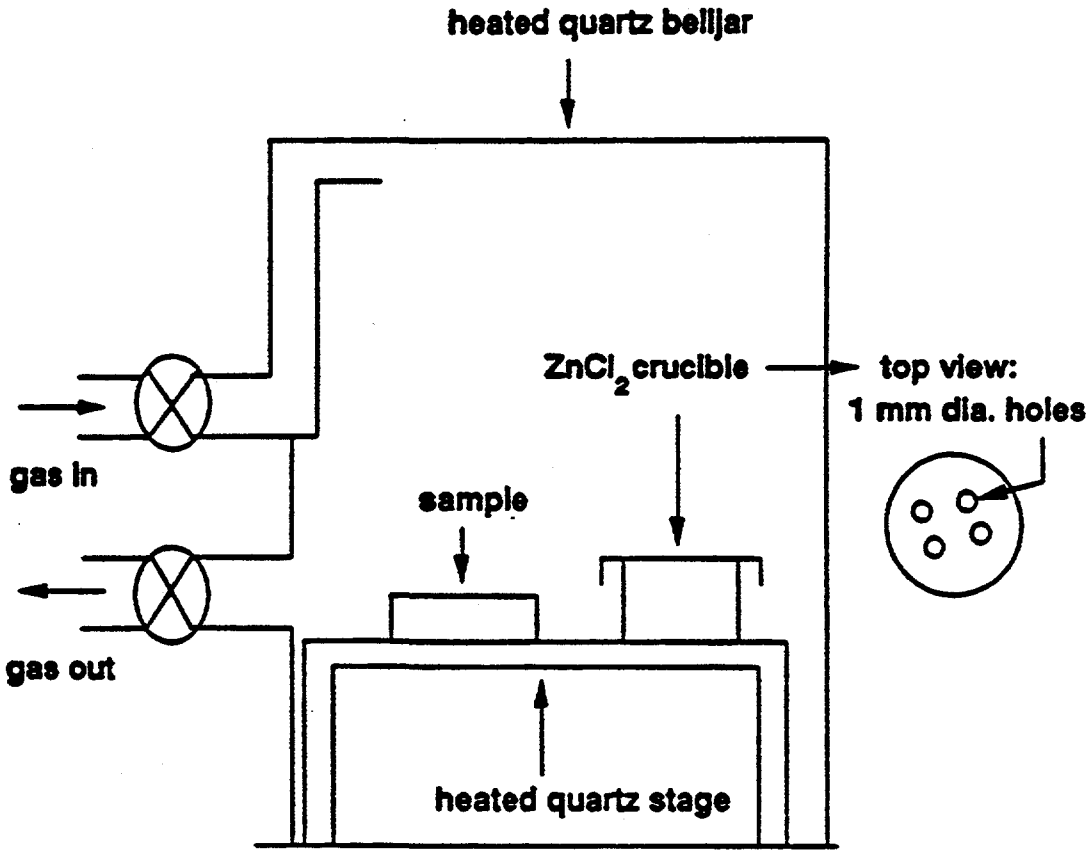


Figure 3.2.4 Simplified Diagram of Closed System Annealing Furnace.

dipped in the saturated $CdCl_2$ solution, air-dried, and then placed on the quartz stage, adjacent to the $ZnCl_2$ crucible in the furnace. The chamber was then sealed and the air was allowed to flow into the chamber for five minutes during which time the valves were closed and the system was sealed. The CdZnTe sample and $ZnCl_2$ crucible were then slowly heated to the desired temperature (400°C) using a heater mounted directly beneath the quartz base plate. To prevent condensation of $ZnCl_2$ onto the walls of the annealing chamber, the quartz bell jar was heated by a wrapped and insulated heater wire. The chamber walls were heated to a temperature of 330°C, which is above the melting point of $ZnCl_2$.

Figure 3.2.5 shows the SPV response of a CdZnTe/CdS structure that was annealed in the system described. The SPV responses for an as-grown film, a film annealed in the open tube furnace after a dip in $CdCl_2$ + $ZnCl_2$, and a film annealed in the open tube furnace after a straight $CdCl_2$ dip are also plotted in Figure 2 for comparison. It is shown that the closed system anneal resulted in smaller bandgap shift compared to the CdZnTe structures annealed in the open tube furnace with both $CdCl_2$ and $CdCl_2$ + $ZnCl_2$ treatments. Furthermore, the SPV response is significantly higher than the response of the sample treated with $CdCl_2$ + $ZnCl_2$ in the open tube furnace. Note however, that the response is still considerably lower than the SPV response of the $CdCl_2$ treated sample annealed in the open tube furnace. This may be due to some competition between the $CdCl_2$ sintering the film and the $CdCl_2$ reacting with the $ZnCl_2$ in the ambient. These observations suggest that a closed system anneal may be necessary to increase the grain size while maintaining the bandgap of the CdZnTe film if $CdCl_2$ is

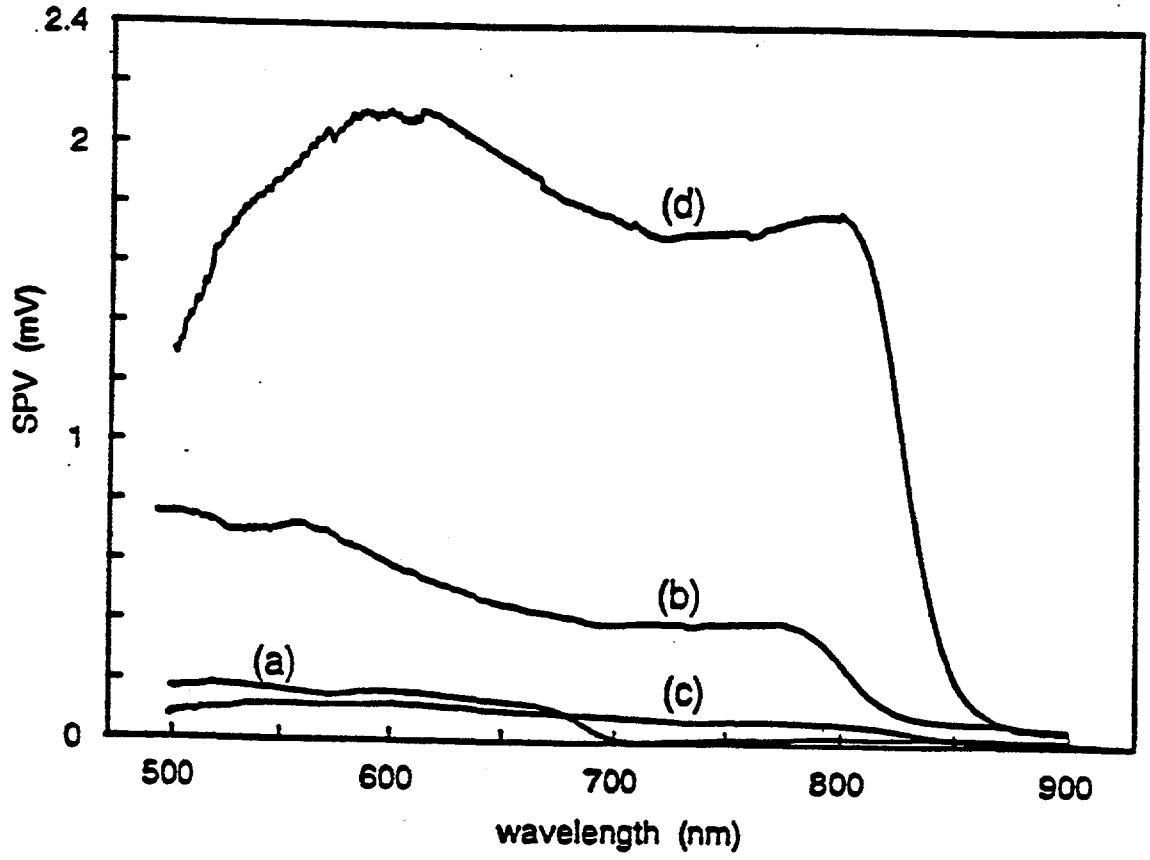


Figure 3.2.5 **SPV Spectra of (a) As-Grown and CdZnTe/CdS Structures Processed Using (b) the Closed System Furnace, and the Open Tube Furnace With (c) $CdCl_2$ + $ZnCl_2$ and (d) $CdCl_2$ Treatments.**

involved in the sintering process. More research is necessary on this promising technique to optimize the conditions in order to achieve an efficient CdZnTe cell with 1.7 eV bandgap.

4. SUMMARY OF THE PROJECT

4.1. Progress in CdTe/CdS Solar Cells

4.1.1. Efficiency Limiting Mechanisms Associated With CdS Films

Oxygen in CdS grain boundaries is known to be a detrimental recombination center. Attempts were made to reduce CdS film by in-situ heat treatment in hydrogen atmosphere in the MOCVD reactor prior to the deposition of CdTe film. We found that annealing of CdS films at temperatures greater than 400° C in hydrogen atmosphere indeed improves the CdTe/CdS cell performance. This is consistent with the results of other investigators who showed that the thermal treatment of CdS in hydrogen atmosphere modifies the transport mechanism at the CdTe/CdS heterojunction. Our XPS results show that this heat treatment removes the oxygen from the CdS and, thereby, reduces the interface states. Besides producing the above beneficial effects, the heat treatment also causes some detrimental effects such as non-uniform Cd/Te ratio on the surface with Cd-deficient CdS surface layer as observed in the Auger spectra. In order to reduce the Cd-deficiency on the CdS surface due to the above heat treatment, attempts were made to grow CdTe films under Cd-rich conditions to replenish the Cd deficiency.

The surface photovoltage spectra (SPV) of CdTe/CdS structures grown under different Te/Cd input gas ratios showed that the SPV response increases considerably as the cadmium concentration increases in the gas phase. Since the SPV response is indicative of V_{oc}, it is reasonable to expect higher V_{oc} on films grown under cadmium-rich conditions. The SPV spectra also showed that the films grown under Te-rich conditions

have slightly lower bandgap compared to the films grown under Cd-rich conditions. The reduction of CdTe bandgap in CdTe/CdS structures was observed by several investigators after the post growth heat treatment and attributed to interdiffusion between CdTe and CdS films. However, our data clearly show that the bandgap reduction in Te-rich films takes place during the MOCVD growth of the CdTe film, prior to the post-growth $CdCl_2$ heat treatment. We propose a model for the bandgap reduction based on sulfur diffusion. The sulfur diffusion gives rise to defect states near the bandedges to broaden the bandedge and decrease the bandgap. Growth of CdTe films under Cd-rich conditions reduces the Cd vacancies and retards the sulfur diffusion into the CdTe films. This reduces the defect states near the bandedge and restores the bandgap of CdTe. Even though we were able to reduce the interdiffusion by growing the CdTe under Cd-rich conditions, the 400° C heat treatment used during the cell fabrication triggered the interdiffusion by forming the Cd vacancies. SPV spectra after the post-growth heat treatment of the films grown in Cd-rich conditions showed a bandgap reduction similar to the as-grown films under Te-rich conditions. Since 400° C heat treatment after the $CdCl_2$ dip is a necessary step for efficient cell fabrication, it may not be possible to avoid the interdiffusion in the current devices unless the cell fabrication procedure is altered. Modified heat treatment such as rapid thermal annealing and/or addition of an interlayer may prevent the interdiffusion to reduce the defects at the interface and restore the bandgap. It is important to recognize that the magnitude of the bandgap shift does not limit the efficiency but the interdiffusion induced defects responsible for the bandgap shift degrade the cell performance.

Another efficiency limiting mechanism is related to the CdS thickness. The CdS film acts like a dead layer for the photogenerated carriers. Thicker CdS films absorb more high energy photons and reduce the J_{sc} of CdTe/CdS cell. In the past we reported 9.7% cell with V_{oc}=726mV and J_{sc} = 22.47 mA/cm_2 on a 2000 Å thick CdS. An attempt was made to improve the J_{sc} by using thinner CdS films. As expected, the thinner CdS film (1000 Å) increased the efficiency to 10.3% from 9.7% by increasing the J_{sc} to 24.19 mA/cm^2. Further reduction in the thickness of the CdS films to 600 Å resulted in a net decrease in the efficiency (8.9%) primarily due to the reduction in V_{oc} (680 mV) and fill factor (0.55) along with some decrease in J_{sc} (23.47 mA/cm^2). Pin-holes in the CdS films can cause low shunt resistance which will reduce V_{oc} and fill factor. In addition, CdS films were deposited on the textured SnO_2 films which can aggravate the pin hole problem in the CdS films. On the other hand, increasing the CdS thickness to 3000 Å increased the V_{oc} to 740 mV and, as expected, reduced the J_{sc} to 22.10 mA/cm^2. However, the cell efficiency increased to 10.9% which happens to be the highest efficiency for MOCVD-grown CdTe/CdS solar cell to date. The advantage of thinner CdS film is clear from the spectral response data, the short wavelength response is higher for the cell with thinner CdS films because more high energy photons are able to reach the CdTe film. These results suggest that to improve the CdTe cell efficiency further, the CdS layer thickness should be optimized or replaced by a combination of thin CdS and wider bandgap material such as ZnO.

4.1.2. Efficiency Limiting Mechanisms Associated With $CdCl_2$ Treated CdTe Film

Significant improvement in CdTe/CdS solar cell efficiency is commonly observed as a result of a post deposition $CdCl_2$ dip followed by a 400° C heat treatment. It is also known that the $CdCl_2$ treatment increases the grain size. However, exact physical mechanism for this improvement is not well understood. A study was conducted using DLTS, I-V-T and PL measurements to understand the these beneficial effects and to investigate potential efficiency limiting mechanism due to $CdCl_2$ treatment. I-V-T measurements showed that this process changes the dominant current transport mechanism from interface recombination/tunneling to depletion region recombination, suggesting a decrease in the density or dominance of interface states due to the $CdCl_2$ treatment. The change in transport mechanism results in an increase in barrier height and reduction in leakage current, supporting the increase in cell efficiency. However, the DLTS measurements showed that depletion region recombination probably occurs through a large density of deep acceptor-like states at E_v + 0.64 eV which could result from the formation of Cd-vacancy related defects during the $CdCl_2$ dip and heat treatment. Traps in the vicinity of E_v + 0.6 eV have been attributed to V_{Cd} and V_{Cd} -Cl related complexes. The presence of the acceptor-like traps within the CdTe depletion region was found to affect the CdTe/CdS solar cell characteristics. The direct consequence of the density of this defect on the measured V_{oc} and J_{sc} of the CdTe/CdS cells that have undergone this treatment is that the V_{oc} is inversely proportional to the trap density while there is no apparent correlation between the J_{sc} and the trap density. This shows that the $CdCl_2$ treatment is indeed important for improving the CdTe/CdS cell performance, however it

appears to introduce a V_{oc} and efficiency-limiting defect whose role must be studied in more detail. It is important to note that in this experiment different trap density was measured on different small area cells fabricated in an identical manner and no controlled attempts were made to vary N_T.

In order to understand systematically the role of chlorine-related defects in CdTe/CdS cells, the concentration of $CdCl_2$ was varied in the range of 0.25 to 1 (saturated). PL measurements were performed on finished devices to investigate the defects produced by different $CdCl_2$ concentrations, because the DLTS measurements were not successful in some cells due to high leakage current near the DLTS peak temperature. Light I-V measurements were performed on the finished devices to monitor the device performance and correlate it with the defects.

It was found that V_{oc} and fill factor are a strong function of the $CdCl_2$ concentration while J_{sc} shows a weak dependence on $CdCl_2$ concentration. The data also showed that the saturated $CdCl_2$ solution often used by the investigators is not the optimum. PL spectra showed two common features, a peak around 7900 Å and a broad band centered around 8400 Å. In CdTe, the broad band centered around 8400 Å is generally attributed to structural defects, native defects or V_{Cd}-Cl defect complexes. The peak at 7900 Å is attributed to Cd vacancies. The intensity or the peak amplitude of the broad band at 8400 Å is directly proportional to the defect concentration in the sample. Several investigators have studied the effects of chlorine in single crystal CdTe by PL and DLTS measurements. Chlorine is a donor in CdTe and is also known to form defect complexes with Cd vacancies, which are produced during the heat treatment. Chlorine-cadmium

vacancy complexes are acceptor type and give rise to shallow and deep energy levels depending on the type of defect complex. According to the literature the chlorine-cadmium defect complexes have energies in the range E_v + 0.15 - E_v +0.9 eV. Generally, PL measurements give information about shallow levels and DLTS gives information about deep levels. The fact that the PL broad band around 8400 Å has been attributed to V_{Cd}-Cl complex in the literature, and the intensity of the PL band and the density of E_v + 0.64 eV DLTS peak both are inversely proportional to V_{oc}, suggests that both the defects are probably chlorine related complexes formed during the $CdCl_2$ treatment. Thus, on one hand $CdCl_2$ treatment is critical to high efficiency CdTe cells but on the other hand it could place an upper limit on the practically achievable efficiency unless the $CdCl_2$ process is modified or optimized.

4.1.3 Cu/Au contact induced instabilities in CdTe/CdS cells

Long term stability is critical for terrestrial solar cells. The CdTe/CdS cells are known to be sensitive to moisture induced degradation. However, proper encapsulation can mitigate this problem for cells with graphite contacts. We have been using Cu-Au contacts and have noticed considerable degradation in our recent high efficiency (10-12%) cells. We were able to obtain cell efficiencies as high as 12% immediately after the cell fabrication. However, after two to three weeks of storage in the laboratory atmosphere (not in the desiccator), the cell efficiency degraded to ~10%. This degradation in efficiency is associated with significant reduction in V_{oc} and fill factor and a modest decrease in J_{sc}. After the rapid initial degradation the cell efficiency nearly stabilizes. It was

also found that the higher efficiency cells degrade more compared to the lower efficiency cells. Such degradation was observed primarily in cells with Cu/Au contacts. ZnTe or graphite contacts to CdTe have been found to be more stable.

In order to understand the contact degradation mechanism further and recover the cell efficiency, the degraded CdTe cells were treated in Br:MeOH etch for seven seconds. It was found that after the Br:MeOH etch both V_{oc} and fill factor values were restored to almost 90% of the original values. This suggests that oxidation of Cu or Te is the probable cause of cell degradation and the Br:MeOH etch is able to reduce those oxides. Formation of such oxides could result from the lack of humidity or moisture control in the laboratory. Further investigation is necessary to determine the exact mechanism, however, our data show that this degradation is not permanent and is reversible to a large extent.

4.2. Progress in CdZnTe/CdS Solar Cells

In addition to the CdTe cells, polycrystalline 1.7 eV CdZnTe films were grown by MBE for tandem cell application. CdZnTe/CdS cells processed using the standard CdTe cell fabrication procedure resulted in 4.4% efficiency, high series resistance, and a bandgap shift to 1.55 eV. Formation of Zn-O at and near the CdZnTe surface is found to be the source of high contact resistance. A saturated dichromate etch instead of Br_2:CH_3OH etch prior to contact deposition has been found to solve the contact resistance problem. The $CdCl_2$ treatment has been identified to be the cause of the observed bandgap shift due to the preferred formation of $ZnCl_2$. A model for the bandgap shift along with a possible solution using an overpressure of $ZnCl_2$ in the annealing

ambient has been proposed. Development of a sintering aid which promotes grain growth and preserves the optimum 1.7 eV bandgap is shown to be the key to successful wide bandgap CdZnTe cells.

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16. Abstract (Limit: 200 words)

This report describes work to improve the basic understanding of CdTe and ZnTe alloys by growing and characterizing these films along with cell fabrication. The major objective was to develop wide-band-gap (1.6-1.8 eV) material for the top cell, along with compatible window material and transparent ohmic contacts, so that a cascade cell design can be optimized. Front-wall solar cells were fabricated with a glass/SnO_2/CdS window, where the CdS film is thin to maximize transmission and current. Wide-band-gap absorber films (E_g = 1.75 eV) were grown by molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) techniques, which provided excellent control for tailoring the film composition and properties. CdZnTe films were grown by MBE, and CdTe films were grown by both MBE and MOCVD. All the as-grown films were characterized by several techniques (surface photovoltage spectroscopy, Auger electron spectroscopy [AES], and x-ray photoelectron spectroscopy [XPS]) for composition, bulk uniformity, thickness, and film and interface quality. Front-wall-type solar cells were fabricated in collaboration with Ametek Materials Research Laboratory using CdTe and CdZnTe polycrystalline absorber films. The effects of processing on ternary films were studied by AES and XPS coupled with capacitance voltage and current voltage measurements as a function of temperature. Bias-dependent spectral response and electrical measurements were used to test some models in order to identify and quantify dominant loss mechanisms.

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